High-Efficiency Flexible Thin-Film Single-Crystal-Like GaAs Solar Cells Based on Cheap Metal Tape

by
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To my wonderful husband Meysam, my sweet boy Daniel and friends

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ABSTRACT

This study introduces the first flexible single-junction III-V photovoltaic solar cells (PVSCs) based on single-crystal-like GaAs thin films on a low-cost metal substrate by direct and continuous deposition, which can bypass expensive single crystal wafer fabrication. A promising SC device performance characteristic with an open-circuit voltage of 560 mV and short circuit current of 19.4 mA/cm^2, resulting in a conversion efficiency of ~7.6%, is demonstrated for the first time. We developed a 2D numerical simulation code to study on the effects of low-angle grain boundaries (GB) in single-crystal-like GaAs thin-film on its photovoltaic performance. The 2D model is capable of investigating the effect of localized recombination centers in the material by defining different regions of defective low-angle grain boundaries and single crystalline intra-grains and shows very well-matched result with experiment. According to the modeling results, increasing the grain size of GaAs from 2 μm to 50 μm can improve efficiency of solar cells from 4.8% to 12.3%. The *Voc* of devices shows more sensitivity to the amount of grain boundary densities than other SC characteristic factors. The 2D model is also employed to study bulk passivation of GBs which shows that thin film single-crystal-like GaAs solar cells whit an efficiency of ~19.7% can be achievable even at small grain size of 2 μm if effective grain boundary passivation is applied. Therefore, we have employed various passivation techniques to increase the efficiency performance of actual single-crystal-like GaAs solar cells. The trioctylphosphine sulfide (TOP:S) solution treatment is the most effective technique for the single-crsytal-like GaAs SC passivation. The study on the effect of TOP:S treatment on the PV performance of newly developed single-crystal-like thin film GaAs showed that the SC dark saturation current after TOP:S treatment decreased from J_o ~2×10^{-3} A/cm^2 to ~3.5×10^{-4} A/cm^2 (at V = -500mV) and a remarkable improvement in efficiency performance of SCs was achieved with an increase of ~24%,

12.8%,14.5%, and 64% for Voc, Jsc, FF, and overall efficiency, respectively. The overall efficiency of flexile single-junction single-crystal-like GaAs thin film SC after TOP:S passivation become 13.5% which is about two times of the previous record for un-passivated SCs with efficiency of 7.6%.

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CHAPTER 1 INTRODUCTION

1.1 History of solar cells

In 1839, Alexandre-Edmond Becquerel discovered the photovoltaic (PV) effect [1]. Later in 1873, Willoughby Smith discovered that selenium could function as a photoconductor. The first working selenium solar cell was invented by Charles Fritz in 1883 and the first modern solar cell made of silicon was invented by Russel Ohl in 1946 [2] and the big jump toward the solar cells like the ones used in panels today came from the work of Bell Labs in 1954 [3]. Earlier solar cells are silicon wafers that transform sunlight energy into electrical power. The modern photovoltaic technology is composed of two different layers (p-type and n-type materials) of a semiconductor material operating based on the principle of electron hole creation in each cell. In this structure, when a photon with a sufficient energy impinges on the p-n junction semiconductor, an electron is ejected by gaining energy from the striking photon and moves from one layer to another which creates an electron and a hole (photogenerated electrical power).

1.2 Photovoltaic materials and technologies

1.2.1 First-generation solar cell-wafer based

The first-generation solar cell technology was produced on silicon wafer. The silicon wafer-based technology is further categorized into two groups of single crystalline and polycrystalline silicon solar cells. Single crystalline solar cell, as the name indicates, is manufactured from single crystals of silicon produced by Czochralski process, the most common production method and are sliced from the big sized ingots.

Polycrystalline Si PV modules are composed of a number of different crystals as the bulk Si are solidified by cooling molten silicon in graphite mold. Despite higher efficiency of single-crystalline Si SC than poly-Si SC, it is the second most common PV which is ranked behind its poly-Si sister due to significantly higher production rate and lower cost of poly-Si. Polycrystalline Si solar cells are currently the most popular solar cells [4].

1.2.2 Second-generation Solar Cells—Thin Film Solar Cells

The second-generation PVs are thin film solar cells which are made by depositing one or more thin layers of photovoltaic materials on various substrates such as glass, plastic or metal. The light absorbing layer of Si-wafer SC is up to 350 μm thick, while thin-film solar cells needs only a very thin light absorbing layers. Their film thickness varies from a few nanometers to tens of micrometers, much thinner than the first-generation silicon wafer solar cells. This allows thin film cells to be flexible, and lower in weight. Thin-film technology is cheaper but less efficient than conventional c-Si technology. However, it has significantly improved over the years. Thin-film solar cells are used in several technologies, including cadmium-telluride (CdTe), copper-indium-gallium-selenide (CIGS) and amorphous silicon (a-Si) [5].

1.2.3 Third-generation solar cells

Third generation are potentially able to overcome the Schockley-Queisser power efficiency limit for single bandgap PVs. These promising technologies are not commercially investigated in detail. Common third-generation PV technologies include multi-layer (tandem) cells made of GaAs or a-Si. Other emerging cells include copper

zinc tin sulfide (CZTS) solar cells, polymer based solar cells, perovskite solar cells, dye sensitized solar cells, nano-crystal based (generally called quantum dot) solar cells and concentrated solar cells [4], [6], [7] (Table 1.1).

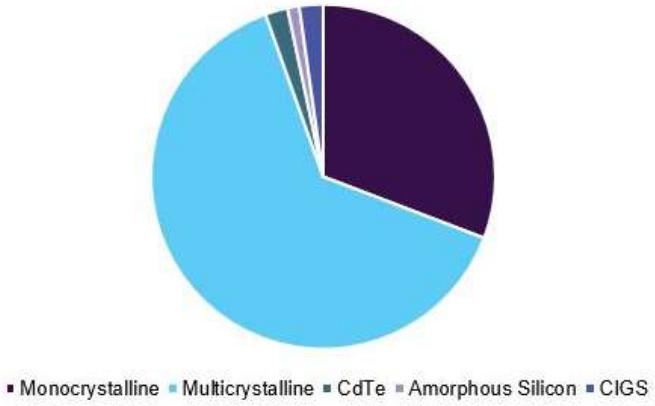


Figure 1.1 Global solar cell market share by product, 2015 (%)

As it mentioned above, several well-known major technological platforms in PV research, development, and manufacturing have been developed for many years. Unquestionably, Si-based SCs on single-crystal wafers are the first and currently dominant in the PV technology, which is the most technically matured platform, have provided reasonable conversion efficiencies (~20%), but are currently priced at unsustainable levels. The others (thin-film SCs) can be further divided depending on the materials such as amorphous Si, Cd-Te, Cu-In-Ga-Se (CIGS), organic materials, and group III-V semiconductors, as listed in Table 1.1. New materials for PV (except the III-V semiconductors (including GaAs single-junction)) have non-single-crystalline structures and share the same characteristics, which include the potential for low cost, higher-margin manufacturing, but low typical efficiencies of generally less than 15%.

Furthermore, the fundamental limits of the conversion efficiencies are also low, suggesting not enough room for further improvement in the efficiency even with the advance of technology due to the nature of those materials. III-V compound semiconductor materials either in the form of single- or tandem structure offer the highest conversion efficiency [8], [9]. However, the use of III-V materials has been limited to specialized applications such as concentrator PV for the utility industry in terrestrial applications and power source of satellites in space applications, mainly because of their very high cost.

Table 1.1 Comparison of currently developed PV technology [10]

Materials	State-of-the-art peak conversion efficiency	Typical conversion efficiency	Cost
Single-Crystalline Si	25.0%	<20%	Low
Polycrystalline Si	20.4%	<10%	Low
Amorphous Si:H	13.4%	<12%	Low
Cd-Te	19.6%	<15%	Low
Cu-In-Ga-Se(CIGS)	20.8%	<20%	Low
Organic materials	11.1%	<5%	Low
PbS quantum dots	8.6%	NA	NA
GaAs (single junction)	26.4%	<22%	High
III-V semiconductors (triple-junction)	37.9% 44.4% (concentrator ×300 sun)	<33%	High

Undoubtedly, GaAs has substantial potential for space and terrestrial PV device applications due to its unique electrical and optical properties, such as, direct energy band gap, high optical absorption coefficient, good values of minority carrier lifetimes and mobilities (in highly pure, single crystal material)[11]–[13]. Tandem SCs based on expensive single-crystalline InGaP/(In)GaAs/Ge structures have been fabricated either in the form of lattice-matched [14], or metamorphic structure [9], [15], to routinely achieve high conversion efficiency >33% and a further improvement is also expected.

Although plenty of records exist for high-efficiency GaAs SCs on single crystal GaAs8 and Ge9 substrates, they are too costly to be employed for large-scale space and terrestrial applications [16], [17]. The high cost is primarily due to very expensive Ge or GaAs single-crystalline wafers to be used as the substrates (or bottom cell) of SC structures, which could amount to one-half to one-third of the total module cost. In order to reduce the fabrication cost, during the past few decades, much effort has been conducted to fabricate high-quality GaAs SCs on single-crystal Si as a low-cost substrate [18], [19]. However, due to the high lattice mismatch (4%) and large thermal expansion coefficient differences between GaAs and Si, high threading dislocation density (TDD) will be generated throughout the GaAs epitaxial layer(s) [20]. TDD at high-angle grain boundaries have been proven as recombination centers to photo-generated carriers leads to the lower minority-carrier lifetime (s) [17], [21].

1.3 Flexible thin-film photovoltaics-substrates

Flexible electronics is emerging rapidly [22], [23]. These devices have the advantages such as low cost, light weight, small size, and high performance to meet the application requirements. In photovoltaic (PV) industry, Si-based solar cells (SCs) and III-V SCs are the main contributors in terrestrial and space applications, respectively. Currently, Si and III-V SCs mostly use expensive single-crystalline wafers (such as Si, Ge, and GaAs) as the substrate. Although, SCs on single-crystalline wafers can reach to the state-of-the-art with very high efficiencies, price, scalability and flexibility of these substrates are the main drawbacks. Flexible III-V SCs can easily resolve the main issues for the single-crystalline-based SCs by reducing the substrate price and making the

flexible and scalable devices. Efficiencies of the current flexible SCs are low and their stability in different environments is also low (see Table 1.1).

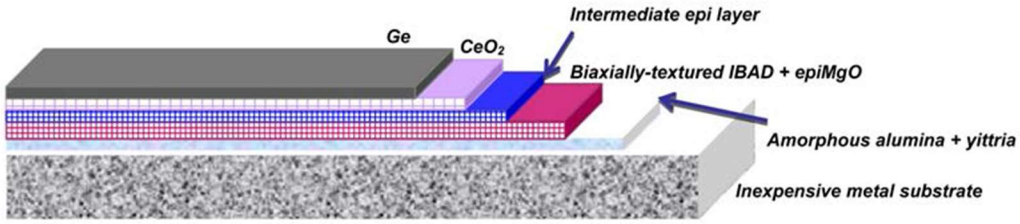


Figure 1.2 Schematic of the multilayer architecture utilized in this work as the template for the growth of GaAs and AlGaAs layers SC structure [25]

1.3.1 Flexible steel substrate

The crystalline-aligned semiconductor films can be only achieved at elevated deposition temperatures.

Among all other existing substrates to be used as templates instead of single-crystal substrates for epitaxial growth of high-performance single-crystal films such as superconductors [24] or semiconductors [25], [26], inexpensive, flexible and scalable metal substrate is the best candidate.

Flexible steel substrates provide us with excellent resistance to high temperature processing and chemicals, and they are impermeable and stiff, so they are less susceptible to the dimensional changes induced in plastic substrates by moisture absorption and the deposition of strained TFT [5], light-emitting diode (LED) [35] or solar cell structures with a large coefficients of thermal expansion (CTE) mismatch.

However, the as-delivered steel foil surface can be very rough, with greater than 1 μm peak-to-peak surface roughness reported, which needs to be reduced, before device processing, either by surface polishing and/or by surface planarization. Al_2O_3 is usually

deposited on metal substrates as a diffusion barrier layer for unwanted elements [36][23].

Hence, the surface capping layer has a double purpose, and, in the use of steel foils to investigate pixel design for flexible AMOLEDs, 75 μm thick, 5 cm × 5 cm steel foils were coated with 1.6 μm of a spin-on-glass followed by 600 nm of PECVD SiN_x deposited at 280°C [37].

A novel approach has been proposed for fabrication of high-efficiency, low cost, flexible and scalable GaAs SCs. This route utilizes high-quality and textured Ge film deposited on low cost metallic template [27]. Described flexible substrate includes single-crystalline-like (nearly single crystalline) Ge film on poly-crystalline flexible substrates through a transition region consisting of oxide buffer layers, which deposited by ion beam assisted deposition (IBAD). The buffer layers play a critical role in the transition (schematically shown in Figure 1.2) by providing highly-textured and highly-crystallographically-oriented materials between semiconductors and metals or ceramics. Textured germanium films on inexpensive, flexible metal substrates have strong potential to be used as a new substrate in the next-generation of GaAs SCs instead of brittle and expensive single crystal germanium [27], [28]. However, the most recent transmission electron microscopy (TEM) studies confirmed that Ge flexible substrate has ~1e9 cm^{-2} defect densities (mostly TDD) which needs to be improved to fabricate a high-quality GaAs SC [28]. Undoubtedly, growing GaAs on flexible Ge substrate will generates high amount of TDD into the active region of the device and, subsequently diminish the minority carrier lifetime and hence efficiency of the SC.

1.4 Current status of flexible thin-film photovoltaics and challenges

In this section, we will discuss on the current trends in state-of-the-art flexible solar cells and key shortcomings for the different solar cell materials and technologies available today. Continuous improvement in developing thin film SCs on flexible substrates paving the way to low-cost electricity. Organic, inorganic and organic–inorganic solar cell materials are deposited over flexible substrates such as paper, polyimide, Mylar and stainless steel for novel applications [29] by high-throughput (often roll-to-roll printing) technologies to afford lightweight, economic solar modules that can be integrated into, not installed on, various surfaces. The three most widely commercialized thin film solar cells are α-Si, CdTe and CIGS. Having a direct band gap is common among these three materials which enables the use of very thin layer of materials [30]. They also have a very low temperature coefficient and all the three technologies can be incorporated into building integrated photovoltaics (BIPV).

The commercial applications of CdTe SCs is slightly limited by the existence of toxic cadmium element in the solar cell material which is harmful to both the producer and the consumer [30]. While a-Si has had the longest time in the commercial sectors, CIGS and CdTe are relatively new technologies, and are more promising in terms of energy conversion efficiency than a-Si. Despite this advantage, the CIGS and CdTe technologies still lag behind crystalline silicon solar cell counterparts in efficiency and reliability.

1.4.1 Amorphous silicon (a-Si)

Since the early 1980s, amorphous silicon solar cells have been used as a reliable power source in consumer products such as digital watches and calculators [31], [32].

Amorphous silicon cells generally feature low efficiency, but are one of the most environmentally friendly photovoltaic technologies, since they do not use any toxic heavy metals such as cadmium or lead. Although α-Si with direct band gap can absorb a significant fraction of sunlight within a thin layer of a few micrometers [33], short orders in amorphous material and the dangling bonds result in short minority carrier diffusion lengths and abnormal electrical behavior.

The amorphous silicon is deposited at low temperature in a way that allows about 10% (atomic) hydrogen to be incorporated, the secret to this technology's success [34]. Without hydrogen incorporation, a-Si has a very high defect density which leads to undesirable semiconductor properties including poor photoconductivity and doping which is critical to engineering semiconductor properties. A significant improvement in the photoconductivity is achieved by hydrogenation of a-Si and doping is also become possible. Hydrogen passivation of a-Si (a-Si: H) can reduce dangling bond densities by several orders of magnitude, thus helping to improve the minority carrier length. However, this hydrogenation is responsible for the Staebler-Wronski light degradation effect [35]. a-Si:H solar cells have been developed since 1970s and steadily climbed in efficiency to about 13.6% in 2015. Since the amorphous silicon is not very conductive, a key feature of the technology is the use of a transparent conductive tin oxide layer between the silicon and the glass.

1.4.2 Copper indium gallium selenide (CIGS)

Favorable electronic and optical properties of copper indium diselenide ($CuInSe_2$) thin-film have been promising for photovoltaic applications since its initial

development. Later it has been found that substituting indium (In) by gallium (Ga) can increase the bandgap from about 1.04 electron-volts (eV) for copper indium diselenide (CIS) films to about 1.68 eV for copper gallium diselenide (CGS) films. Optimal bandgap is achieved by a partial substitution of Ga for In which leads to a substantial increase in overall efficiency. These solar cells are commonly known as a copper indium gallium diselenide [$Cu(In_xGa_{1-x})Se_2$], or CIGS, cells. The laboratory-scale cell efficiencies of CIGS have exceeded 20%, however their commercial modules typically have efficiencies between 12% and 14%.

Figure 1.3 shows the evolution of the CIGS solar cell technology efficiency [35].

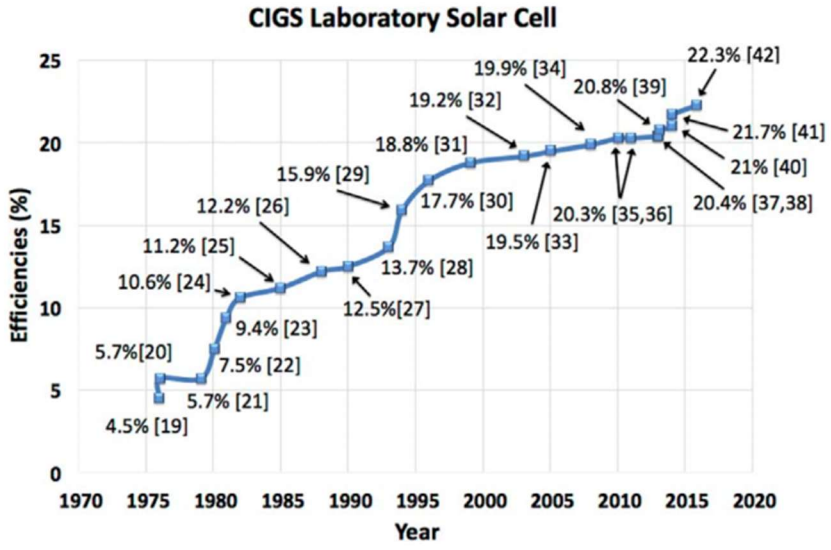


Figure 1.3 Best laboratory photo-conversion efficiencies for CIGS solar cell [35]

1.4.3 Cadmium telluride (CdTe)

Cadmium telluride (CdTe) is a direct band gap material like CIGS with a large absorption coefficient. CdTe is a stable compound which can be produced from a wide

variety of methods. In 1972 (Figure 1.4), the first significant laboratory CdTe cell with 6% efficiency was reported for a thin film graded gap CdTe-CdS p-n heterojunction solar cell. The graded gap junction improved the transport of the photogenerated carriers to enhance the Jsc. Rapid interest in the CdTe resulted in a variety of different fabrication methods including screen-printing methods, vapor growth and vacuum deposition. The final cell properties are generally controlled by junction preparation technique. For example, vacuum evaporation of CdS results in heterojunctions, whereas chemical vapor deposition techniques of CdS produce buried homojunctions [36].

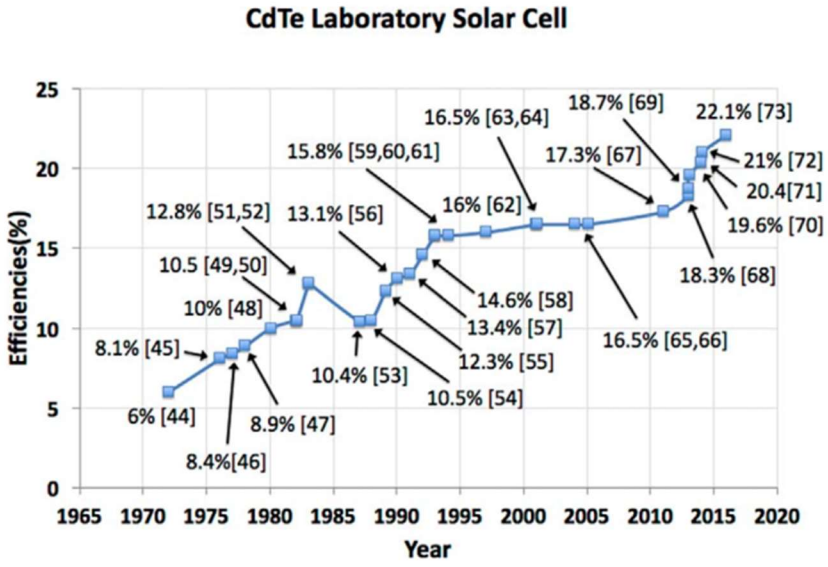


Figure 1.4 Best laboratory photo-conversion efficiencies for CdTe solar cell [35]

1.4.4 Gallium arsenide (GaAs)

III-V compound based solar cells have unsurpassed conversion efficiencies as their bandgaps are tunable to match the solar spectrum. Additionally, the high radiation hardness of III-V materials has made them the leading technology for space applications, even though there are still numerous possibilities for further improvements

[37]. High cost and weight of III-V SCs are of their disadvantages which limit even their space applications. Where lightweight thin film CIGS cells are able to meet the minimum efficiency requirement for space applications in geostationary orbits, which is about 13.5% at AM0, they are used instead of III-V SCs. But for efficiency needs above 20%, the use of III-V compound semiconductors is the only option to satisfy the ever-increasing satellite power needs, however still a reduction of the costs and an increase of the power to weight ratio is highly desired.

Epitaxial lift-off (ELO) technique has been developed to reduce the cost and weight of the III-V solar cells by transferring the thin film III-V layers structure from its wafer substrate. In this technique, a thin $Al_xGa_{1-x}As(x>0.6)$ release layer between the structure and wafer is grown which is later selectively etched away to transfer the III-V structure to a lighter flexible/rigid substrate.

Therefore, the expensive Ge/GaAs wafer substrate can be reused after the lift-off process for several times which cuts part of the SC cost. The grown single-crystal thin-film on wafer can be transferred and cemented on an arbitrary flat carrier for SC device fabrication processes. A significant gain in power-to-weight ratio compared with the common III–V compound semiconductor cells on a wafer substrate can be obtained by choosing a light carrier substrate [38].

The ELO technique has been improved at the Radboud University Nijmegen. The technique initially was able to separate only milli-meter area size of GaAs layers with a lateral etch rate of about 1 mm/h, but it has been later evolved to a process capable to

remove the entire 2-inch epitaxial GaAs layers structure from its substrate with etch rates up to 30 mm/h [39].

However, subsequent fabrication processes of these thin-film structures into actual ELO solar cells was found to be difficult. The standard techniques applied for the processing and interconnect of cells on a substrate have been frequently failed for the thin-film cells on a foreign carrier. Therefore, new processing schemes had to be developed to produce ELO cells [38].

Using the ELO method, the SC structure is grown in reverse order which allows the growth of metamorphic junctions on top of lattice matched grown junctions and therefore making multijunction solar cells [2]. The number of junctions can be extended without affecting the lift-off process. A mirror layer can also be applied on the back of the thin-film cell to reflect non-absorbed photons which can cause 50% reduction in the base layer thickness [3]. The performance of thin film ELO cells has been repeatedly argued to be as good as cells on a wafer substrate. However, still the efficiency of thin film ELO cells somewhat is lower than the efficiency of the best conventional GaAs cell on a substrate. The processing of thin-film ELO III–V cells is also more complicated than for substrate cells, but on the other hand has improved photon confinement possibilities by the use of a backside mirror.

1.5 Single-crystal-like inorganic semiconductor materials

So far by review of current well-established thin-film solar cell technologies, it is clear that there is a lack in photovoltaic technology that can deliver high-quality materials while lowering the fabrication cost and yet showing high-performance solar

cell devices. Among different thin film materials used as active solar cell structure, III-V semiconductors have delivered the highest PV efficiencies of ~29% [40] and ~46% [41] for both single and multi-junction structures, respectively. However, such a high efficiency III-V thin film solar cell devices require single-crystalline epitaxial films. Typically, single-crystal substrates are used for the epitaxial growth of these films, however such substrates are expensive, fragile, and available in limited sizes. So far, the ELO method for reuse of wafer has been the most effective and practical technique in reducing the III-V SC cost. However, this technique still relies on wafer platform for high quality material growth. During the last decade, many research studies have been conducted on the development of new technologies to find universal methods that can deliver single-crystal-like thin films, mainly, Si(Ge) to bypass expensive wafer fabrication [26], [27], [42]. Group IV films with textured microstructure on polycrystalline metal substrates are very prominent; the cost of the substrates is much less, there are no strong size restrictions, the systems are more flexible and scalable [28]. Despite the fact that there is extensive progress in development of biaxially textured thin films via "seed and epitaxy" techniques, but no high-performance solar cell devices have been demonstrated [42].

The new pathway which can be considered one of the strong alternatives in the future's PV technology, utilizes high efficiency III-V semiconductors as an active material, while adopting metallic flexible economical substrates instead of expensive and brittle single-crystalline semiconductor substrates. The scalability of III-V SCs makes them available for mass production via a method so-called "Roll-to-Roll" on the

same high-quality flexible substrates. If such flexible solar cells can achieve sufficient technological maturity, it may not only replace the current single-crystalline Si-SCs for terrestrial applications, but will also create new applications on various sets of devices such as space applications, electronic displays, they can also be manufactured on clothing, which can in turn be used to charge portable electronic devices like mobile phones and media players.

The fundamental material and device characteristic studies on the proposed approach for III-V compound semiconductors on flexible substrate in this dissertation will open a new way for flexible thin-film photovoltaics and other semiconductor-based technology including high-performance, high- power, and flexible optoelectronics with reduced manufacturing cost and versatile applications. This new development, if successful, can lay a foundation for future hybrid-material-based electronic and photonic devices (Figure 1.5).

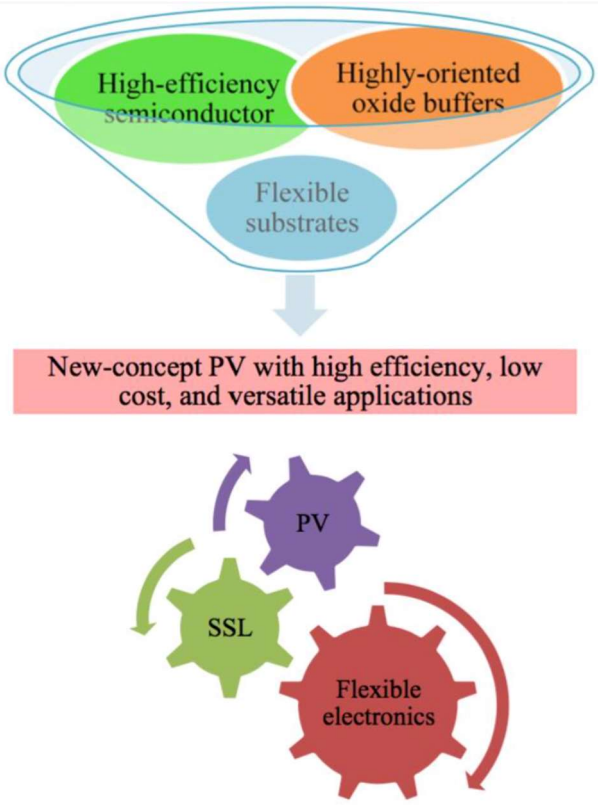


Figure 1.5 Scope of work and impact of new material and device concepts on semiconductor-based green energy systems

1.5.1 Simulation of GaAs Triple Junction SCs on Flexible Substrate

While the single-junction GaAs SC will be developed as a feasibility study of semiconductor PVs on flexible substrates in order to avoid complications associated with epitaxial structure design and growth of multi-junction sub-cells and tunnel junctions, the potential benefit of this approach needs to be further clarified. Considering the same situation as single junction, thickness and carrier concentration for each individual layer has been calculated in the case of triple junction (see the appendix). The theoretical study of the conversion efficiency for the triple-junction SCs on flexible substrates is presented in the appendix, again assuming the materials quality we have so far achieved from the single-junction SC, as described previously. The optimized

structures show conversion efficiency of higher than 30% (see the appendix), which is higher than all the state-of-the-art conversion efficiencies reported for any SC materials (Table 1.1), except for its siblings on expensive single-crystal substrates (37.9%). As we further develop crystalline quality of SC materials in this program, we believe we can achieve better conversion efficiencies close to the value of 37.9% at significantly reduced process cost and larger area.

CHAPTER 2 SOLAR CELLS: MATERIAL AND DEVICE CHARACTERIZATION

2.1 Introduction

In this chapter, important theoretical concepts of solar cell material, device operation, and characterization are briefly explained.

2.2 Semiconductors and junctions

A p-n junction separates the electron and hole carriers in a solar cell to create a voltage. The junction with no external inputs represents an equilibrium among carrier generation, recombination, diffusion and drift in the presence of the depletion region's electric field. some carriers still cross the junction by diffusion. Despite the impediment to the diffusion of carriers across the electric field, some carriers still cross the junction by diffusion. Most of the majority carriers entering the depletion region are moved back towards the region from which they originated. However, some carriers still have high velocity and travel in a sufficient net direction into the junction and can cross it and become a minority carrier. They continue to diffuse away from the junction and before recombining they can travel a distance on average equal to the diffusion length. The diffusion current component is caused by majority carriers' diffusion across the p-n junction depletion region. The minority carriers that reach the edge of the p-n junction region are swept across by the electric field. This current is known as the drift current.

2.3 Solar cell operating principle

A light absorbing material is used in solar cell devices to absorb sunlight photons and generate free electrons via the photovoltaic effect. The photovoltaic (PV) effect is

the basis of the conversion of light to electricity in solar cells. Striking of sunlight on a PV cell imparts enough energy to some electrons to raise their energy level and thus free them. A solar cell is a diode formed by joining a p-type and an n-type semiconductor material. Electrons can diffuse across the p-n junction to the p-side and recombine with holes and similarly holes can diffuse across the junction to the n-side and recombine with electrons giving rise to the diffusion component of the recombination current.

A region of positively ionized donor and negative ionized acceptor atoms, called space charge region (SCR), is formed in the n-side and the p-side when electrons and holes moved to the opposite side of p-n junction, respectively (Figure 2.1). These ionized atoms in the SCR forms an electrical field directed from the n-type region towards the p-type region and cause a built-in potential barrier, V_{bi}, associated with the internal electric field [29]. At some point, the electric field buildup will eventually oppose further diffusion of electrons and holes where the fermi levels in both regions are equal and the junction is at its thermal equilibrium (Figure 2.2). The junction depletion region and the volume of cell material within the minority carrier diffusion length is the active region of a solar cell for collecting the light-generated current [29].

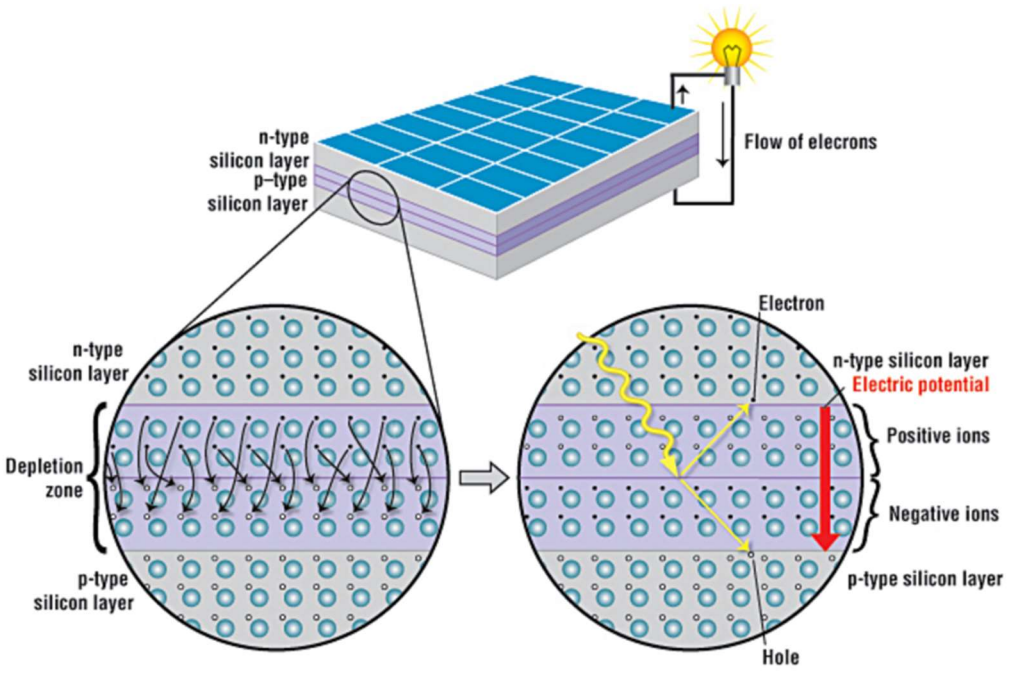


Figure 2.1 Schematic representation of a silicon solar cell, showing the n-type and p-type layers, with a close-up view of the depletion zone around the junction between the n-type and p-type layers

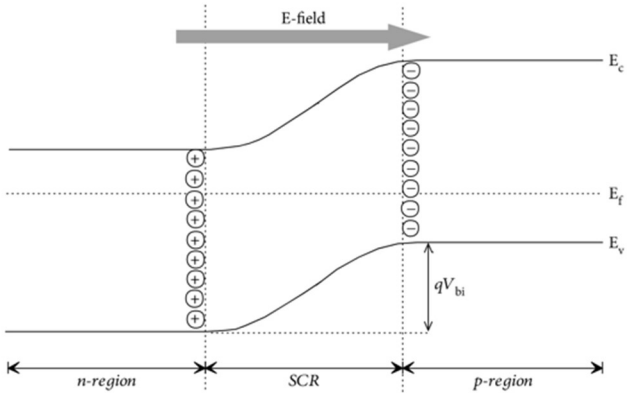


Figure 2.2 Schematic illustration of the energy band diagram of a p-n junction at thermal equilibrium

2.4 Solar Spectrum

The spectrum of the Sun is approximately that of a black body with a temperature of 5780 K which is in the visible range and has a long infra-red tail. However, this spectrum is not used for SC characterization on the Earth as the light must pass through the Earth's atmosphere absorbing a significant portion of the solar radiation before reaching the surface. Also, the solar spectrum changes throughout the day and with location. Therefore, two standard reference spectra are defined for terrestrial use to allow the performance comparison of photovoltaic devices from different manufacturers and research laboratories. One is the AM1.5 Global spectrum which is designed for flat plate modules and has an integrated power density of 1000 W/m^2 (100 $mW.cm^{-2}$) equivalent to average solar irradiation at mid-latitudes such as in Europe or the USA. The other one is the AM1.5 direct plus circumsolar spectrum defined for solar concentrator work which includes the direct sun beam plus the circumsolar component in a disk 2.5 degrees around the sun with an integrated power density of 900 W/m^2.

Considering the solar spectrum, a too large bandgap material will result in a significant number of photons not being absorbed. On the other hand, a too low bandgap means that a large number of photons will be absorbed, but a significant amount of energy will be lost due to the relaxation of electrons to the conduction band minimum.

According to this trade-off, there is a theoretical maximum efficiency of a standard photovoltaic device, as well as an optimum band gap for a photovoltaic material. Shockley and Queisser determined the theoretic maximum efficiency to be approximately 33% in 1961, which corresponds to a band gap of 1.34 eV (~930 nm, the green line in the graph of Figure 2.3).

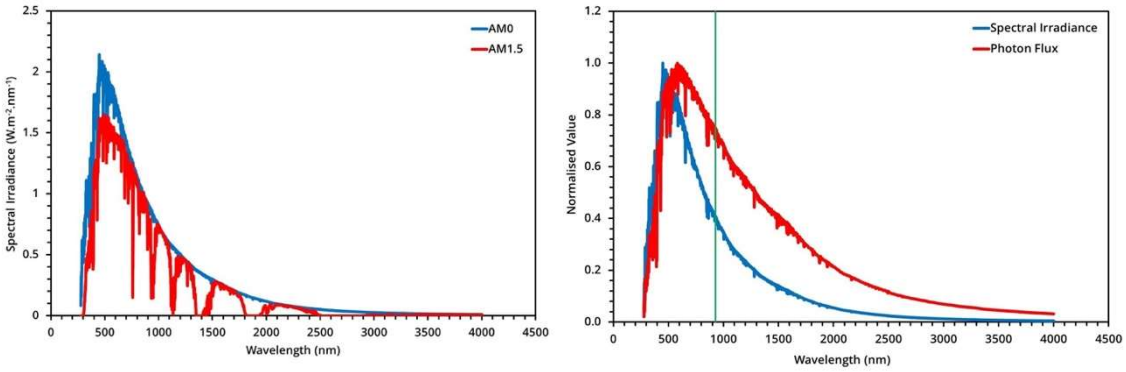


Figure 2.3 (a) The spectral irradiance and photon flux of the Sun b AM0 and (b) AM1.5 solar spectrum. Data courtesy of the National Renewable Energy Laboratory, Golden, CO

2.5 Recombination

The opposite process to generation is called recombination where an electron recombines with a hole and gives up the energy to produce either heat or light. There are three basic types of recombination in the bulk of a single-crystal semiconductor; radiative, Auger [43], and Shockley-read-hall [44]. In silicon-based solar cells, Auger and Shockley-Read-Hall recombination dominate. The recombination processes are associated with the lifetime of the semiconductor materials. Any electron in the conduction band of a semiconductor is in a meta-stable state and will eventually stabilize to a lower energy position in the valence band, an empty valence band state, and remove a hole.

2.6 Surface recombination

Surface of solar cells represent a severe disruption of the crystal lattice, therefore provides a high density of defects for high recombination rate of minority carriers (Figure 2.4).

A depleted region of minority carriers in the vicinity of solar cell surface is formed which causes carriers to flow into this region from the surrounding, higher concentration regions. The value of surface recombination rate is limited by the movement rate of minority carriers towards the surface. The term of surface recombination velocity (cm/sec) is used to specify the recombination at a surface which is on the order of 1e7 cm/sec for most semiconductors. The interruption to the periodicity of the crystal lattice at the surfaces causes dangling bonds, known as defects. Growing a layer on top of the semiconductor surface which ties up some of these dangling bonds can reduce surface recombination which is very common in solar cell design and known as surface passivation.

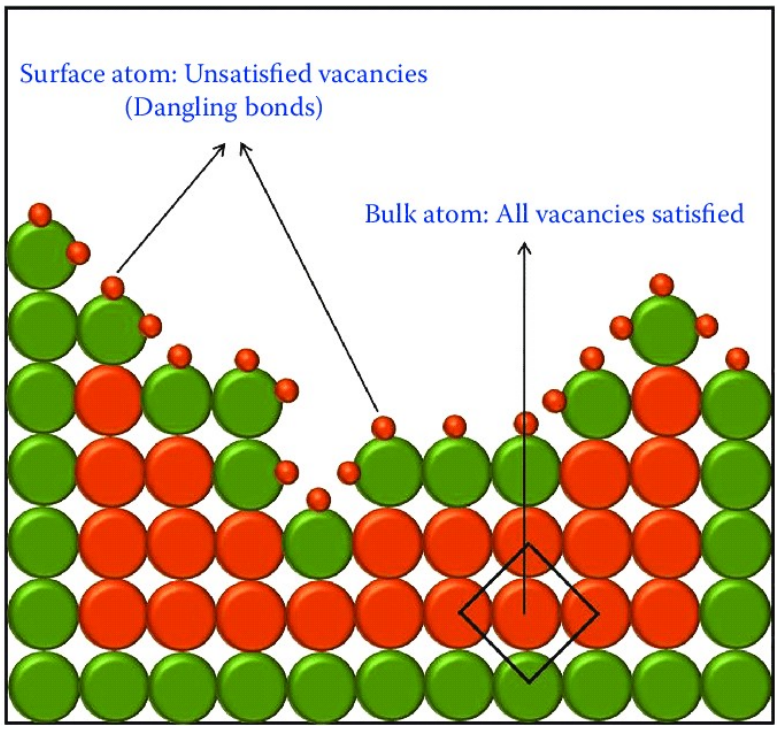


Figure 2.4 A schematic representation of the bulk core atom (red color) satisfied with coordination number, and unsaturated valence atom (green color), refers as dangling bond, responsible for surface energy. High S/V ratio comprises more unsaturated bonds; surface energy.

2.7 Lifetime

A semiconductor lifetime is contingent upon the recombination rate which is dependent upon the minority carriers' concentration and it takes different types of recombination into account. Semiconductor material lifetime is an indicator of solar cell conversion efficiency and thus is a very critical key consideration in choosing materials for SC application.

The electricity generation from incident light on solar cell is the result of the photovoltaic effect at a boundary layer. The incident photons with greater energy than the band gap of solar cell material is absorbed and create free electron-hole pairs. The

excess photo-generated minority carriers may diffuse to the space-charge region, cross the junction and give rise to photocurrent, photovoltage, and power into a load. However, they may be lost by bulk or surface recombination on their way to the pn junction [45].

2.8 Light generated current

In order to produce light-generated current from a solar cell, absorption of incident light together with the collection of photogenerated carriers have to happen. The generated electron and hole carriers in the solar cell by incident light are metastable in the p-type and n-type material, respectively and will only exist for an average length of time equal to the minority carrier lifetime before they recombine.

If they recombine, the light-generated electron-hole pairs are lost and no current or power is generated or extracted from the SC. The minority carriers' collection can happen by the p-n junction which prevents this recombination by spatial separation of the electron and the hole. The existence of an electric field at the p-n junction is the cause of carriers' separation. The light-generated minority carries when reach the p-n junction are swept across the junction by the electric field and become majority carriers on the other side of junction. If the solar cell is short-circuited by connecting its emitter and base, the light-generated carriers flow through the external circuit.

2.9 Collection probability

The probability that a light-generated carrier will be collected by the p-n junction in a certain region of the solar cell and therefore contribute to the light-generated current is known as the collection probability. This probability depends on the travel distance

of minority carriers to the junction compared to the diffusion length (Figure 2.5). For instance, when an electron-hole pair is generated in the depletion region, its collection probability is unity as they are quickly swept apart by the electric field and collected. The collection probability drops as the electron-hole pairs are generated away from the junction. And, if their distance is more than a diffusion length away from the junction, then the collection probability of these carriers is quite low. Similarly, if the carriers are generated closer to a defective region such as a surface (with higher recombination) than the junction, they will recombine and will not contribute into the light-generated current. The surface properties of SCs also affect the collection probability. Figure 2.5 shows the impact of surface passivation and diffusion length on the collection probability.

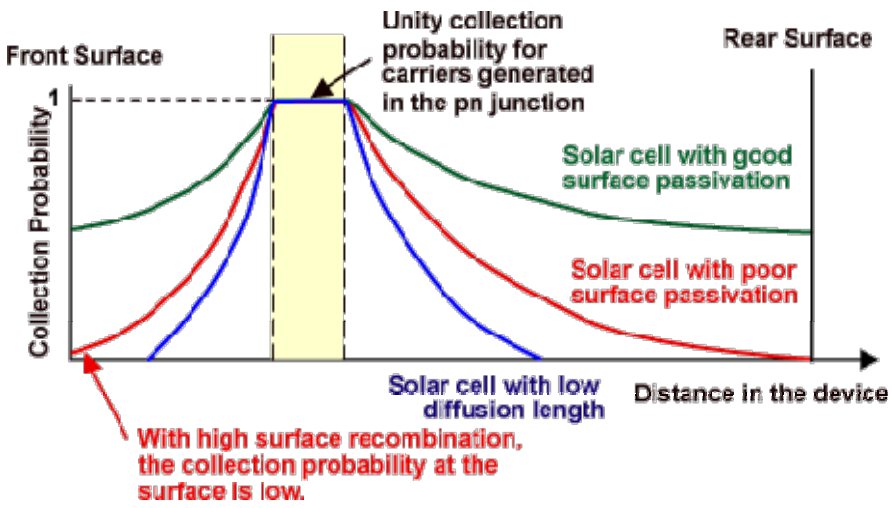


Figure 2.5 Collection probability; the impact of surface passivation and diffusion length [46].

The light-generated current from the solar cell is determined by the collection probability in conjunction with the generation rate in the cell (Figure 2.6). The equation

for the light-generated current density (J_L), with an arbitrary generation rate (G(x)) and collection probability (CP(x)), is

$$J_L = q \int_0^W G(x)CP(x)dx = q \int_0^W [\int \alpha(\lambda)H_0 e^{(-\alpha(\lambda)x)}\, d\lambda]CP(x)dx, \qquad (1)$$

where q is the electronic charge, W is the thickness of the device, α(λ) is the absorption coefficient, and H_0 is the number of photons at each wavelength.

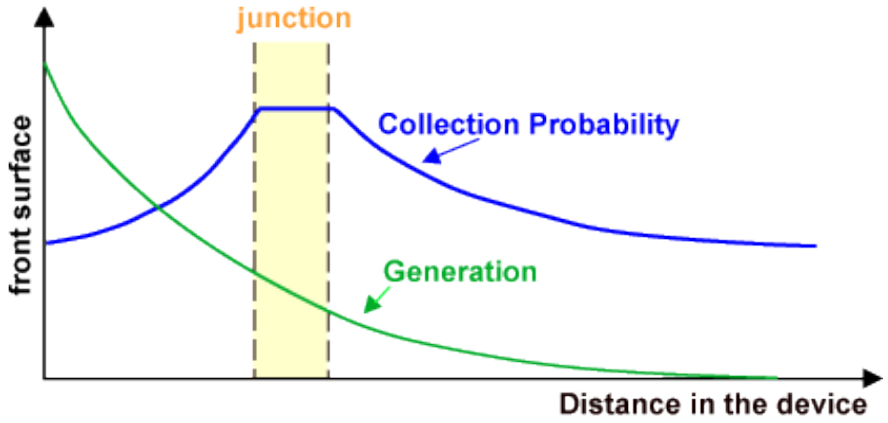


Figure 2.6 The light-generated current depends on the generation of carriers and the collection probability of these carriers [46].

2.10 Quantum efficiency

The quantum efficiency of a solar cell is the ratio of the number of collected carriers by the cell to the number of incident photons of a particular wavelength on the cell. In order to evaluate the amount current that SC exposed to sunlight produces, the cell's quantum efficiency should be integrated over the whole solar electromagnetic spectrum. In the event of multiple exciton generation, quantum efficiencies of greater than unity (100%) may be achieved as the incident photons have more than twice the band gap energy and can create two or more electron-hole pairs per incident photon.

There are two commonly used terms for the quantum efficiency of a solar cell which are external quantum efficiency (EQE) and internal quantum efficiency (IQE). The EQE and IQE refer to the number of charge carriers collected by the SC to the number of incident photons and the number of absorbed incident photons of a given energy, respectively.

2.11 The photovoltaic effect

The collection of light-generated carriers does not give rise to power generation by itself. A voltage must be also generated in the solar cell which is caused by a process known as the photovoltaic effect. A movement of electrons and holes to the n-type and p-type side of the junction is caused by the electric field of p-n junction. There is no buildup of charge carriers in the short circuit condition as the carriers exit the SC device as light-generated current. However, if the light-generated carriers are prevented from leaving the solar cell, the number of electrons in the n-type and holes in the p-type side of the p-n junction increases which creates an opposite electric field at the junction to the already existing field, thereby reducing the net electric field.

Since the electric field represents a barrier to the flow of the forward bias diffusion current, the reduction of the electric field increases the diffusion current. A new equilibrium is reached in which a voltage exists across the p-n junction. The current from the solar cell is the difference between IL and the forward bias current. Under open circuit conditions, the forward bias of the junction increases to a point where the light-generated current is exactly balanced by the forward bias diffusion current, and the net current is zero. The voltage required to cause these two currents to balance is called the

"open-circuit voltage". The following animation shows the carrier flows at short-circuit and open-circuit conditions.

2.12 Solar cell parameters

The main parameters that are used to characterize a solar cell performance are the peak power P_{max}, the short-circuit current density Jsc, the open circuit voltage Voc, and the fill factor FF which are determined from the illuminated J-V.

The current through the solar cell when the voltage across the cell is zero is the short-circuit current, usually written as I_{SC} which is due to the generation and collection of light-generated carriers. The short-circuit current depends on several factors including the area of the solar cell, the intensity and spectrum of incident light, the optical properties (absorption and reflection), and the carrier collection probability.

The short-circuit current density (Jsc $mA.cm^{-2}$) is commonly used rather than the short-circuit current for better performance comparison of solar cell with various sizes.

The equation for the short-circuit current considering several assumptions, which are not true for the conditions encountered in most solar cells, can be approximated as below where there is a uniform generation and the solar cell's surface is perfectly passivated. The equation indicates that the short-circuit current depends strongly on the diffusion length and generation rate,

$$J_{sc} = qG(L_n + L_p)\,, \qquad (2)$$

where G is the generation rate, and Ln and Lp are the electron and hole diffusion lengths respectively. The externally measured current at short circuit conditions is Isc and it is usually equal to I_L, therefore the two are used interchangeably and the solar cell equation

is written with Isc instead of I_L for simplicity. However, in the case of very high series resistance (> 10 Ωcm2) Isc is less than I_L and the solar cell equation with Isc is not correct.

The maximum voltage available from a solar cell is open-circuit voltage (V_{OC}) which occurs at zero current. The equation for V_{OC} for an ideal p-n junction cell is obtained by setting the net current equal to zero in the solar cell equation as

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{I_L}{I_0} + 1\right), \quad (3)$$

where I_L is the light-generated current and I_o is the diode saturation current. To achieve maximum open circuit voltage, I_o needs to be as small as possible. The recombination of light-generated carriers in the semiconductor is the fundamental process determining the Voc of solar cell. The lower the recombination rate in the semiconductor, the higher is Voc. Recombination through trapping levels in the depletion region can limit Voc significantly. Voc is also a function of Ln(Jsc), therefore if one is bad it can affect the other and vice versa.

Another key parameter in evaluating SC performance is fill factor (FF) which is the ratio of the actual maximum obtainable power to the product of the open circuit voltage and short circuit current. Graphically, FF is a measure of the squareness of the IV curve. A solar cell with a higher voltage has a larger possible FF. At both Jsc and Voc operating points, the power from the solar cell is zero and it is the FF in conjunction with them that can determine the maximum power from a solar cell.

2.13 Device IV characterization

2.13.1 Dark IV

Dark IV measurement is critical in investigating the diode properties. Unlike measurement under illumination, dark IV measurement uses inject carriers into the circuit with electrical means not light generated carriers. A simple dark IV measurement of a diode produces an exponential curve. This current vs. voltage graph in the linear scale reveals very little information about the diode, much more information is obtained from a semi-log plot including dominant loss mechanisms in different regions of the IV curve. It should be noticed that the solar cell analysis based on dark IV curves relies on the principle of superposition which is the light IV curve is the dark IV curve shifted by the light generated current in the absence of resistive effects. Also, in the dark IV measurements the current flow (into the cell) is in the opposite direction compared to the light IV (out of the cell) and the current paths (mostly crosses the junction directly under the contacts in the dark case while crosses the junction uniformly in illuminated case) are different which causes a lower series resistance in the dark IV measurement rather than light measurements [47].

2.13.2 Light IV

Under illumination, the dark IV curve ideally is displaced downward by the light-generated current and is considered as the light IV curve. When looking at a characteristic light IV curve, the open-circuit voltage (Voc), short-circuit current (Isc) and the maximum power point (MPP) are of importance.

The V_{OC} is the maximum voltage available from a solar cell which occurs at zero current. The open-circuit voltage corresponds to the amount of forward bias on the solar

cell due to the bias of the solar cell junction with the light-generated current. The Isc is the current through the solar cell when the voltage across the solar cell is zero (i.e., when the solar cell is short circuited) which is due to the generation and collection of light-generated carriers. The MPP refers to the point at which the solar cell can output its maximum power at a specific irradiation level which is at the knee of the IV characteristic curve (Figure 2.7).

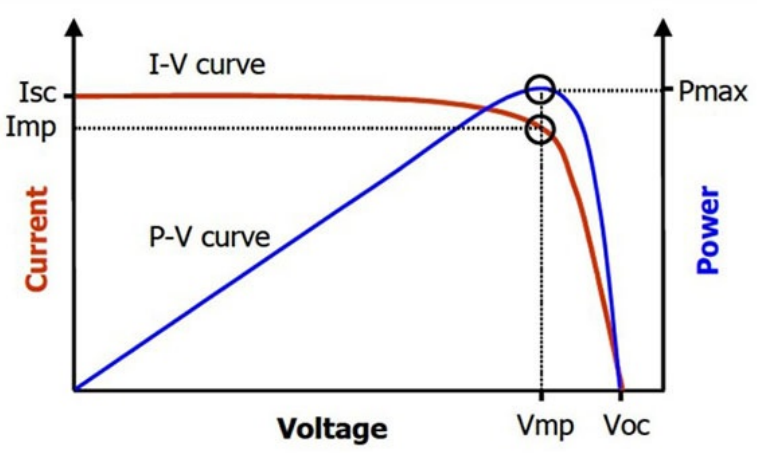


Figure 2.7 The typical I-V and power-voltage (P-V) curves are based on the cell model; Pmax is the maximum power point, while Imp is the current and Vmp is the voltage at the maximum power point [48]

2.13.3 Parasitic resistances

Resistive effects are detrimental to solar cell power output by dissipating power in the resistances. Series resistance and shunt resistance are the most common parasitic resistances (Figure 2.8). High shunt resistance is desired for SC operation as the low shunt resistance provides an alternate current path for the light-generated current which reduces the amount of current flowing through the solar cell junction and reduces the

voltage from the solar cell causing power loss in solar cell. The shunt resistance is mainly due to material defects rather than poor device design.

The main impact of series resistance is to reduce the solar cell fill factor and in the case of excessive high values may also reduce the solar cell short-circuit current. Series resistance comes from the movement of current through the emitter and base of the solar cell, the contact resistance between the metal contact and semiconductor and the resistance of the top and rear metal contacts [49]. The IV curve of the solar cell is given by the following equation in the presence of both series and shunt resistances

$$I = I_L - I_0 \exp\left[\frac{q(V+IR_s}{nkT}\right] - \frac{V+IR_S}{R_{SH}}. \quad (4)$$

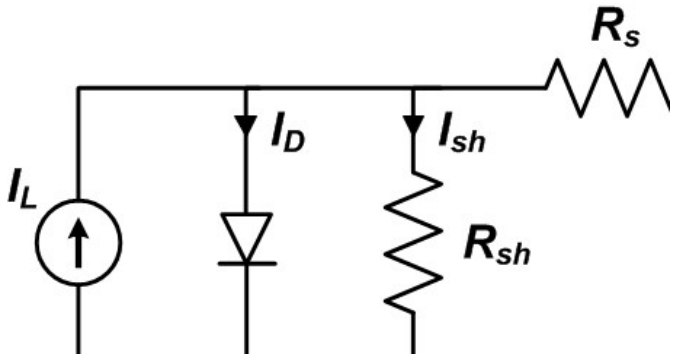


Figure 2.8 Parasitic series and shunt resistances in a solar cell circuit

2.13.4 Ideality factor

The ideality factor (n) of a p-n junction solar cell is an indication of the quality of the cell and how close a diode follows the ideal diode equation. In the case of ideal diode, all the recombination is assumed to occur via band to band or via traps in the bulk areas from the device and no recombination in the junction. The ideal diode equation is

$$I = I_L - I_0[\exp\left(\frac{qV}{nkT}\right) - 1], \quad (5)$$

where the ideality factor is equal to one. However, in non-ideal situation, recombination does occur in other ways and areas of the devices as well. Therefore, the ideality factor deviates from the ideal and is more than unity.

2.14 Optical characterization; reflectance and absorption

There are optical losses in the solar cell when the light is reflected from the front surface or not absorbed in the cell. The entire visible spectrum (350 - 780 nm) can ideally be absorbed as it has enough energy to create electron-hole pairs.

There are several ways to reduce the optical losses (Figure 2.9). For instance, the top surface of the cell can be deposited by anti-reflection coatings or a combination of surface texturing and light trapping can be employed to increase the optical path length in the solar cell. Top contact area on the cell surface blocking light entrance can be also reduced; however, this may result in higher series resistance. The solar cell thickness can also be increased for higher absorption, however, the absorbed light in a distance more than a diffusion length from the junction has a low collection probability and will not contribute to the short circuit current.

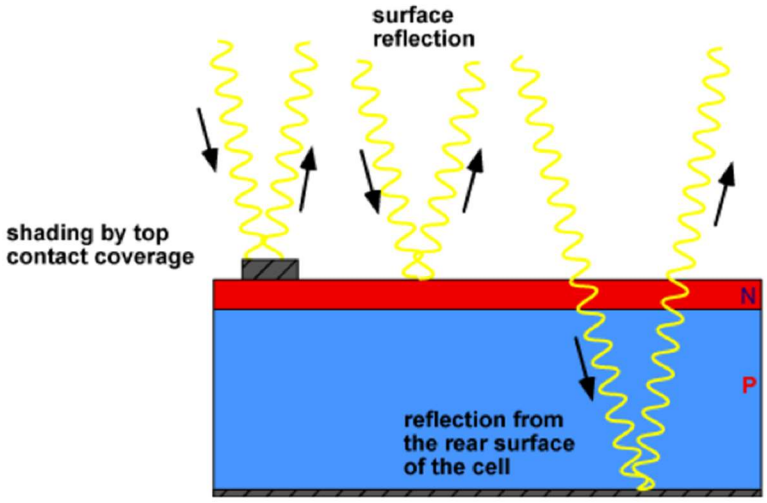


Figure 2.9 Sources of optical loss in a solar cell [50]

2.15 Photoluminescence

Photoluminescence (PL) spectroscopy is used to probe the electronic structure of materials. The intensity and spectral content of the emitted photoluminescence is a direct measure of important material properties including bandgap determination, impurity levels and defect detection and recombination mechanisms. The spectral distribution of PL from a semiconductor can be analyzed to determine the electronic bandgap which provides a means to quantify the elemental composition of compound semiconductor. The high sensitivity of the PL technique provides the potential to identify extremely low concentrations of intentional and unintentional impurities that can strongly affect material quality and device performance. The quantity of emitted PL from a material is related to the relative amount of radiative and nonradiative recombination rates.

Nonradiative rates are typically associated with impurities and thus, this technique can qualitatively monitor changes in material quality as a function of growth and processing conditions.

2.16 Thesis organization

The objectives of this work are to simulate, design, fabricate and characterize next generation of SCs consisting of inexpensive metal template, group III-V semiconductors, and inorganic buffer materials for photon-electron conversion and to develop new-concept high-efficiency low-cost photovoltaic solar cells (PV-SCs) based on high-quality semiconductor structures synthetized on flexible and scalable substrates. In that sense, the flexible GaAs solar cells will be a promising candidate to address the critical need for imminent changes in next-generation PV devices with high conversion efficiency, economic sustainability, and application versatility. Novel innovative approach has been proposed for device structure that can serve as a technical platform for future PV systems with higher efficiency at lower cost (than currently dominant single-crystal Si-based PV systems).

The main focus of next chapters is as follow. In chapter 3, the growth of oxide buffer layers and epitaxial semiconductors on poly-crystalline flexible metal substrate is firstly explained. Secondly, details of the SC device layers structure, critical device design, simulation, and optimization of fabrication steps for proof-of-concept flexible single-crystal-like GaAs SCs are discussed.

The major objectives of simulation for SC devices are testing the validity of proposed physical structures, geometry on cell performance and fitting of modeling

output to experimental results. In this study, simulation is one of the first priorities and the most critical step due to the complications in the cell structure [51]. Two critical parameters need to be optimized are thickness and carrier concentration of each individual layer for the cell design [52].

As of the main target, GaAs single-junction SC is aimed to be fabricated on flexible template. However, some critical steps in SC design needs to be done prior to achieve this target. Preliminary experiments required to be done in order to estimate the amounts of TDD and minority carrier lifetime (as the inputs for simulation) of the GaAs deposited by metalorganic chemical vapor deposition (MOCVD) on flexible substrate. Moreover, resistance of window and emitter layers are expected to play a critical role in SC I-V characteristics, the influence of series resistance [53], specifically, sheet resistance on linear grid design (shadowing effects) need to be evaluated, extensively.

Chapter 4 is focused on the first realization of flexible single junction GaAs SCs based-on developed single-crystal-like III-V thin films. Chapter 5 studies the detrimental effect of low-angle grain boundaries (LA-GBs) of single-crystal-like GaAs materials on the SC performance and later investigates the effect of grain boundary passivation on the efficiency improvement using 2D numerical simulation. In the chapter 6, the effect of various experimental techniques for the passivation of GBs in the single-crystal-like GaAs is explained.

CHAPTER 3 EPITAXIAL GROWTH, SIMULATION, AND DESIGN OF GAAS SINGLE-JUNCTION SC STRUCTURE

3.1 Introduction

In this chapter, the epitaxial growth condition of III-V semiconductor compounds on a polycrystalline metal tape and the materials characteristics are presented. Later, the device design and simulation based on this newly developed III-V semiconductors for a practical high efficiency solar cells are discussed. We will also look into more detail on the critical fabrication steps of GaAs solar cell employing this new material template. The optimized device fabrication conditions are later employed for the first realization of single-crystal-like GaAs SC in the chapter 4.

3.2 Highly-oriented oxide buffers

For direct deposition of single-crystal-like semiconductor films on the flexible metal substrate, critically required is the transformation of crystallinity from poly-crystals of substrate to near-single-crystals of semiconductor layers. An effective approach in order to achieve a high-quality GaAs material in the active region of SC device is the deposition of buffer layers crystallographically oriented in biaxial (both in-plane and out-of-plane) directions. The multilayer architecture for developed flexible GaAs solar cell template in this work is schematically illustrated in Figure 3.1. The multilayer architecture consists of single-crystal-like III-V compounds, group-IV semiconductors and oxide buffer layers deposited on a flexible Hastelloy tape.

The thin Hastelloy C-276 [54] metal tape employed as the flexible substrate is chemically stable at relatively high temperatures of deposition and processing for high-

performance SCs. The Hastelloy tapes offer mechanical flexibility, lightweight, thermal/mechanical/chemical stability (up to 1200 °C), good barriers to moisture and oxygen, and compatibility with large-scale continuous processing for thin-film deposition.

Glass and plastic-based flexible substrates have been widely used in thin film photovoltaic technology. However, they are intrinsically limited in compatibility with the growth environment of oxide and semiconductor layers and conditions for device fabrication processes. For instance, commonly used polymeric substrates with a maximum processing temperature of ~250 ° are not suitable for high-quality thin-film growth and fabrication processes of thin film flexible photovoltaics.

Single-crystal-like semiconductor materials deposited on glass substrate was also reported to have minor polycrystalline features in the films due to limited deposition temperatures up to ~650 °C, which is a glass-transition temperature. Heat treatment above this temperature can cause loss of flexibility in the substrate.

Recently, single-crystal-like thin films on amorphous/polycrystalline substrates has been developed via direct deposition [27], [42] which were mostly obtained via a "seed and epitaxy" technique. In this technique a seed layer (e.g., MgO, CeO2, CaF2, etc.) with biaxial texturing is deposited, followed by other layers on the textured seed by epitaxial growth. In order to achieve high-quality single-crystal-like thin films, various combinations of materials for buffer layers are designed. For instance, a CaF_2 seed layer deposited by ion-beam-assisted deposition (IBAD) has been used for single-crystal-like Ge layer development. However, the resulting buffer structure was porous, which

requires an additional thick capping layer deposited at a very slow rate [65], hence, undesirable for further growth of flexible semiconductor films for GaAs SC devices.

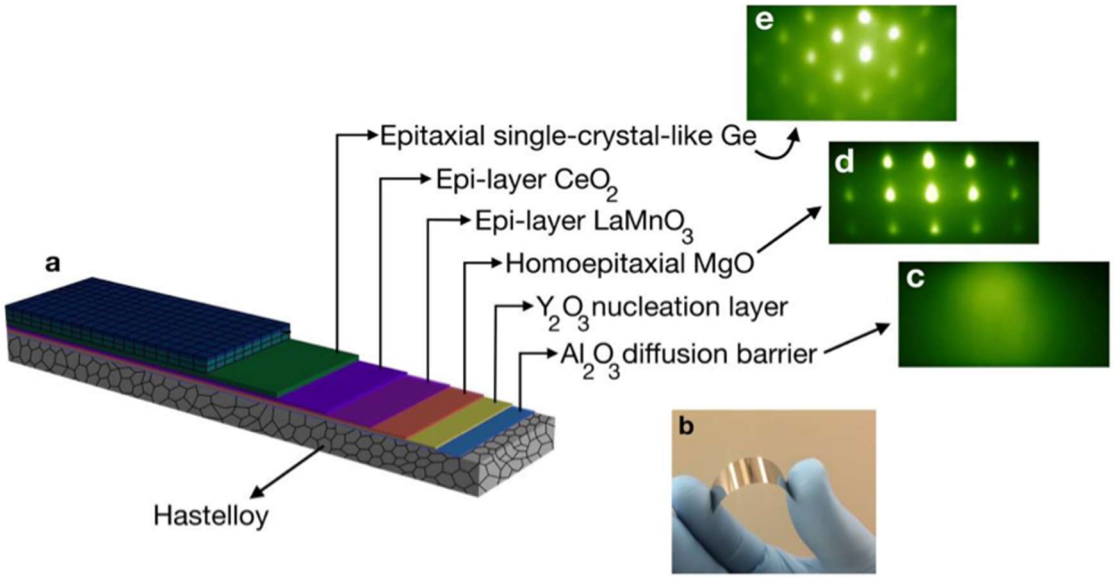


Figure 3.1(a) Schematic illustration of multilayer oxide buffers and semiconductors architecture. (b) Picture of flexible metal tape substrate. (c-e) Crystallinity transformation illustrated by RHEED patterns done by Ying Gao [55].

We developed a novel material technology to enable epitaxial growth of single-crystal- like III-V thin films for GaAs SCs with fast sequential deposition processes of the buffer layers, which is also compatible with R2R continuous deposition. For instance, a tape-feeding speed of R2R process was ~3 cm/min for the deposition of a ~160-nm-thick CeO_2 layer.

Electro-polished Hastelloy tapes with a dimension of 12 mm × 50 μm (width × thickness) were used as flexible substrates. The substrate tape was initially coated with Al_2O_3 (~80 nm) by radio-frequency (RF) sputtering as a diffusion-barrier layer to

suppress the alloy components of the metal such as Ni, Mn, and Cr which may diffuse to the buffer and epitaxial semiconductor layers during the high temperature process.

Then, a Y_2O_3 (~5 nm) layer was deposited as a nucleation-promotion layer by RF sputtering to assist the formation of a highly oriented biaxially textured MgO layer to be deposited later. The Al_2O_3 and Y_2O_3 layers were amorphous. An MgO layer (~10 nm) was deposited by ion-beam assisted deposition (IBAD) to provide a seed with crystallographically selected orientation in both in-plane and out-of-plane directions. In the IBAD process, the substrate is bombarded with a low- energy ion beam, during deposition, and the purpose of this ion beam is to sputter away unfavorably-oriented crystallites, resulting in biaxially-textured thin films. The layer was deposited using Mg target and a reactant gas of O_2 with an assist-ion beam Ar^+ having energy of 1000 eV at an incident angle of 45°.

In-situ reflection high-energy electron diffraction (RHEED) pattern during the deposition of Al_2O_3 (Figure 3.1c) indicates a disordered surface, as expected from the amorphous layer. High-quality cube texture in [001] out-of-plane direction was observed by the sharp spots in the RHEED pattern of the MgO layer. After the formation of biaxially-textured MgO by IBAD, intermediate buffer layers, including homo-epitaxial MgO (~60 nm), $LaMnO_3$ (~50 nm), and CeO_2 (~160 nm) layers were deposited by RF magnetron sputtering. The buffer layers in this study were deposited by continuous roll-to-roll processes. The flexible substrates with the buffer layers were ready for the epitaxy of single-crystal-like semiconductor films. Then, Ge layer was

epitaxially grown on CeO_2 by sputtering or plasma-enhanced chemical vapor deposition (PECVD) at ~600 °C as a semiconductor buffer layer for the epitaxy of III-V layers.

Figure 3.1d shows a RHEED pattern of homoepitaxial MgO. $LaMnO_3$ (orthorhombic perovskite structure) and CeO_2 layers provide structural compatibility with semiconductor (diamond structure) layers and accommodate the lattice mismatch between semiconductor and MgO (rock-salt structure) layers. In-plane lattice mismatch on a (001) plane between MgO (a = 4.212 Å) and Ge (a = 5.658 Å) is –0.256. By introducing the CeO_2 (a = 5.410 Å) layer, the lattice mismatch decreases to –0.044 between CeO_2 and Ge. The improvement of RHEED pattern from MgO to Ge, as shown in Figure 3.1e, suggests subsequent epitaxial growth of $LaMnO_3$ and CeO_2 layers. The achieved single-crystal-like Ge thin film with controlled thickness and carrier concentration is an ideal candidate for III-V thin film growth for PV applications since GaAs and Ge are lattice-matched.

According to RHEED patterns in Figure 3.1(d) and (e), there is an in-plane rotation of a basal plane by 45° between MgO and Ge, possibly for better accommodation of the lattice mismatch. The complete crystal structure evolution from poly- to single-crystalline states is shown in Figure 3.2 where the materials selection and thickness of each layer were optimized and each oxide buffer layer acts as a new template for next layer with improved crystalline quality.

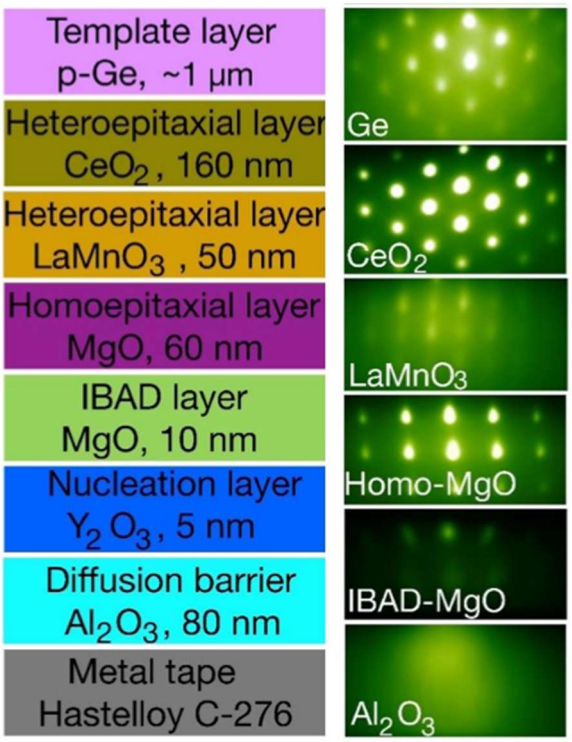


Figure 3.2 RHEED pattern of complete layer structure showing crystallinity transformation from a polycrystalline metal substrate to single-crystal-like semiconductor film

In addition to in-situ surface crystallinity characterization by RHEED, X-ray diffraction (XRD), Raman Spectroscopy and Transmission Electron Microscopy (TEM) characterizations of the films have been also done in order to confirm the epitaxial quality of the transitional buffer layer as well as GaAs thin film. Details of the characterization methods are reported elsewhere. The XRD characterizations confirm that the GaAs film is a nearly single-crystalline material and out-of-plane orientation of the GaAs film is well aligned in a [001] direction. Even though crystallinity of the buffers and epitaxial films are confirmed, there are defects originated from lattice mismatch and thermal mismatch between different layers. Therefore, thin film growth should be optimized in such a way that can reduce the misfit dislocations density. One

applicable way that significantly decreases the density of defects is the increase of the GaAs thickness as the gliding and annihilation of dislocations occur as the film grows thicker.

Other defect mitigation techniques adopted for dislocation density reduction in GaAs thin films includes thermal annealing and insertion of strained buffer layers (Figure 3.3 and 18). Similar approaches were previously employed in GaAs films grown on lattice-mismatched Si substrate [56]. However, in this study there are new unknowns and challenges for the defect-reduction processes due to the flexibility and thermal expansion coefficient of the metal substrate and associated buffer layers. Bending of defects at the strained interfaces by insertion of supper lattice (SL) structure in the GaAs buffer layer is considered one of the most effective techniques for defect reduction [57]. Figure 3.3c shows the SAED pattern of the SL structure embedded in buffer layer, as indicated by the circle in Figure 3.3a. The single-crystalline nature of the film was confirmed by the spotty pattern. The absence of additional secondary spots also indicates that the InGaAs/GaAs was strained and did not relax during growth.

A significant reduction of defect density has been reported for employing a combination of thermal cycling and 20 period SL/300nmGaAs/20 period SL (Figure 3.4b) compared to a sample with only single 100nm InGaAs layer as the defect reduction scheme (Figure 3.4a).

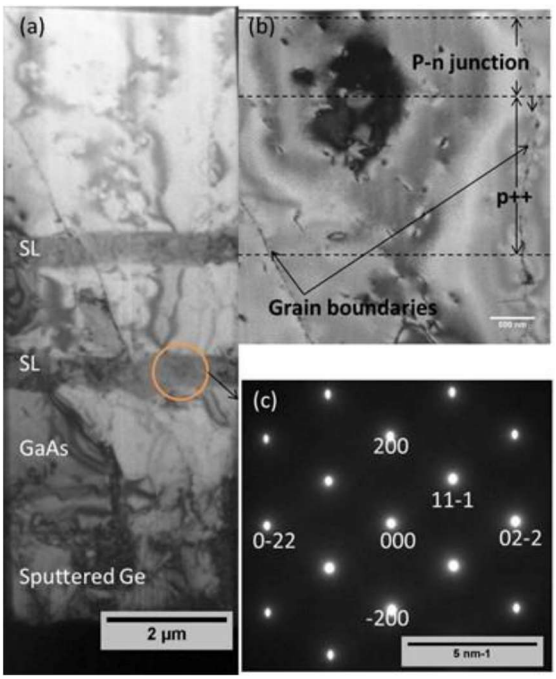


Figure 3.3 (a) CS-TEM image of single junction GaAs SC device grown on defect reduced GaAs templates (b) high magnification image of the top GaAs active layers (c) SAED pattern obtained from the SL region [57]

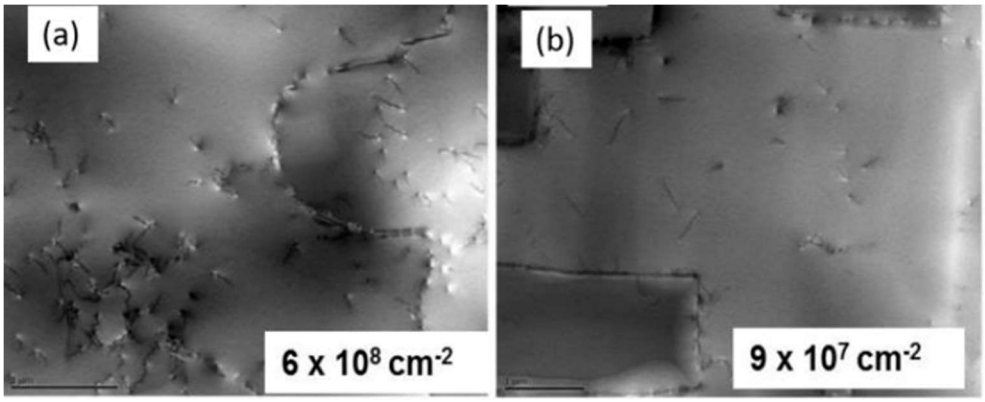


Figure 3.4 PV-TEM of selected samples revealing defect densities [57]

3.3 Epitaxial growth of GaAs

Epitaxial growth of thin film GaAs has been conducted successfully on the flexible substrates using newly-designed-MOCVD system equipped with both traditional batch

chamber for wafers and separate unique roll-to-roll continuous loading of flexible tapes for mass production. As shown in Figure 3.5a, the (Zn-doped) GaAs film (on Ge) on a metal substrate shows a strong (400) preferred orientation. In addition, the film showed sharp in-plane texture, a strong band-to-band photoluminescence (PL) peak at room temperature, and epitaxial film growth with a TDD of ~3×10^7 cm^{-2} (as measured from multiple scans of plan-view TEM, not cross-sectional TEM shown in Figure 3.5b (many related figures not shown here). While this amount of dislocation density is significantly higher than that of a GaAs film on single-crystal wafers (on the order of 10^5 cm^{-2}), the crystalline quality of the materials should be significantly superior to those of poly-crystalline and amorphous materials. Although there are some rooms for reduction of the defects [56], high TDD of GaAs film so far achieved requires new design and modeling of the SC structures.

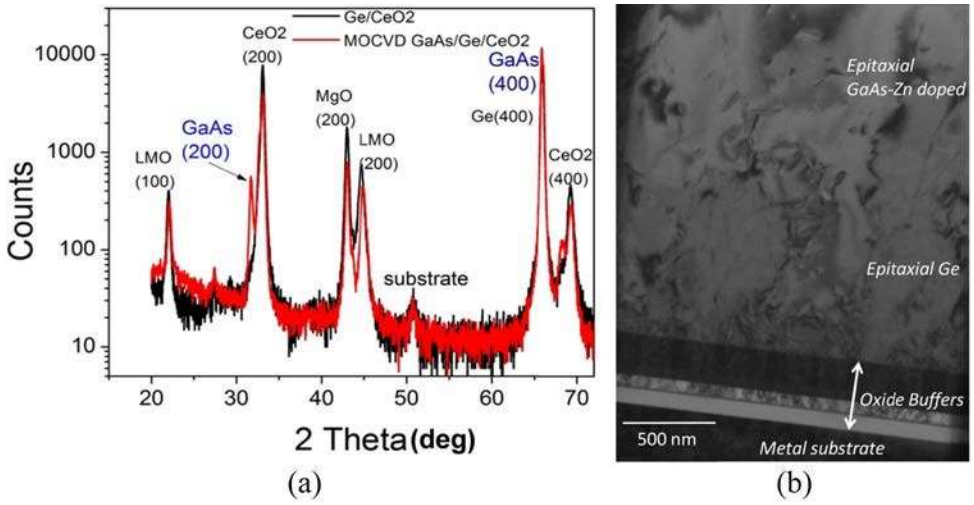


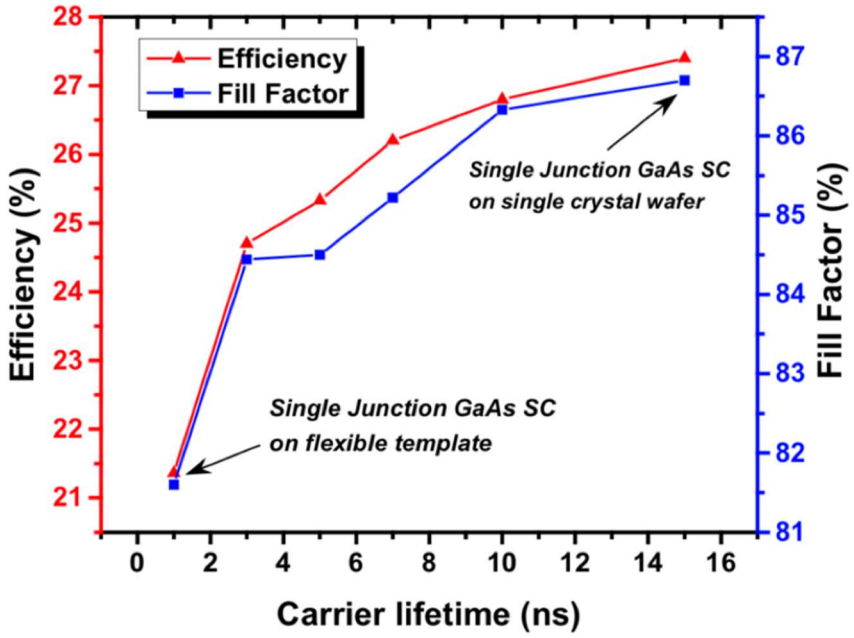
Figure 3.5 (a) Theta-2theta XRD and (b) cross-sectional TEM obtained from single-crystalline-like Ge on a poly-crystalline metal substrate ((a) black) and a GaAs film grown on the template ((a) red).

3.4 Simulation of GaAs single junction SC on flexible substrate

In order to optimize the SC structure on flexible template, estimated minority carrier lifetime (τ_n for electrons and τ_p for holes) and TDD of the primary grown GaAs on flexible substrate should be evaluated. These parameters can be used as inputs for SC simulation. Comprehensive survey of all plausible GaAs SC structures starting from single-crystal wafer to flexible substrate based on their estimated carrier lifetime(s) have been done using STR SC simulator software. Minority carrier diffusion lengths of materials in this program are expected to be different from established values used in the traditional semiconductor SCs. The time-resolved PL measurements of the GaAs film showed the carrier lifetime τ~1 ns, which is 10-20 times lower than single-crystalline GaAs SCs possibly due to a combined effect from rather high TDD and Zn doping. Considering all these factors on the SC performance, thickness and carrier concentration for each individual layer have been theoretically studied.

Figure 3.6 shows simulated conversion efficiency performance vs. carrier lifetime of GaAs single-junction (SJ) solar cells (SCs) using a standard layer structure presented in the table. The devices show significantly lower efficiencies with decreased carrier lifetime, when they adopt the standard design that is used for single-crystalline SC materials. According to the simulation results, thickness is a critical issue in GaAs SC design, particularly, in the case of high TDD. Figure 3.6 clearly shows that efficiency of single-junction GaAs SC is decreasing by reducing τ or increasing TDD [19], [58], [59]. Moreover, the reduction in efficiency is more critical when τ is small enough and that's because of the presence of higher TDD which causes higher number of traps for photo-generated carriers so they can't contribute to the current [17], [58]. In the case of

p^+–p–n structure, minority carriers in the base layer are holes with higher diffusion length ($L_h=\sqrt{D.\tau_p}$). Therefore, higher efficiency in p^+–p–n configuration is expected. Preliminary results showed changes in the thickness for highest TDD will gives us ~21% conversion efficiency under AM 1.5G, 1sun spectral illumination conditions after successful optimization. Figure 3.7 shows an optimized structure of GaAs single-junction SC based on flexible Ge/metal substrates that it has been developed (with τ of 1 ns) and simulated current-voltage (*I-V*) characteristics and power of the SCs. Under AM1.5G, 1 sun conditions, the conversion efficiency is >21%, which is higher than typical efficiency of single-crystalline-Si SCs (see Table 1.1). Moreover, comparative simulation carried out to observe the potential of this new-concept GaAs SC at higher illuminations (see Figure 3.8).



Standard GaAs SC structure based on single-crystal material		
Layer materials	**Layer thickness**	**Doping level (cm^{-3})**
p^+-$Al_{0.2}Ga_{0.8}As$ (window)	5 nm	$N_A = 5\times10^{18}$
p-GaAs (emitter)	0.3 μm	$N_A = 1\times10^{18}$
n-GaAs (base)	3.5μm	$N_D = 1\times10^{17}$
n^+-$Al_{0.2}Ga_{0.8}As$ (back-surface field)	0.2 μm	$N_D = 1\times10^{18}$

Figure 3.6 Efficiency vs. minority carrier lifetime for single-junction GaAs SC on flexible substrate at different TDDs.

Layer	Material	Thickness	Doping level
Window	$Al_{0.2}Ga_{0.8}As$	20 nm	$N_D=5\times10^{18}$ 1/cm^3
Emitter	GaAs	50 nm	$N_D=1\times10^{18}$ 1/cm^3
Base	GaAs	1000 nm	$N_A=1\times10^{17}$ 1/cm^3
BSF	$Al_{0.2}Ga_{0.8}As$	2000 nm	$N_A=4\times10^{18}$ 1/cm^3

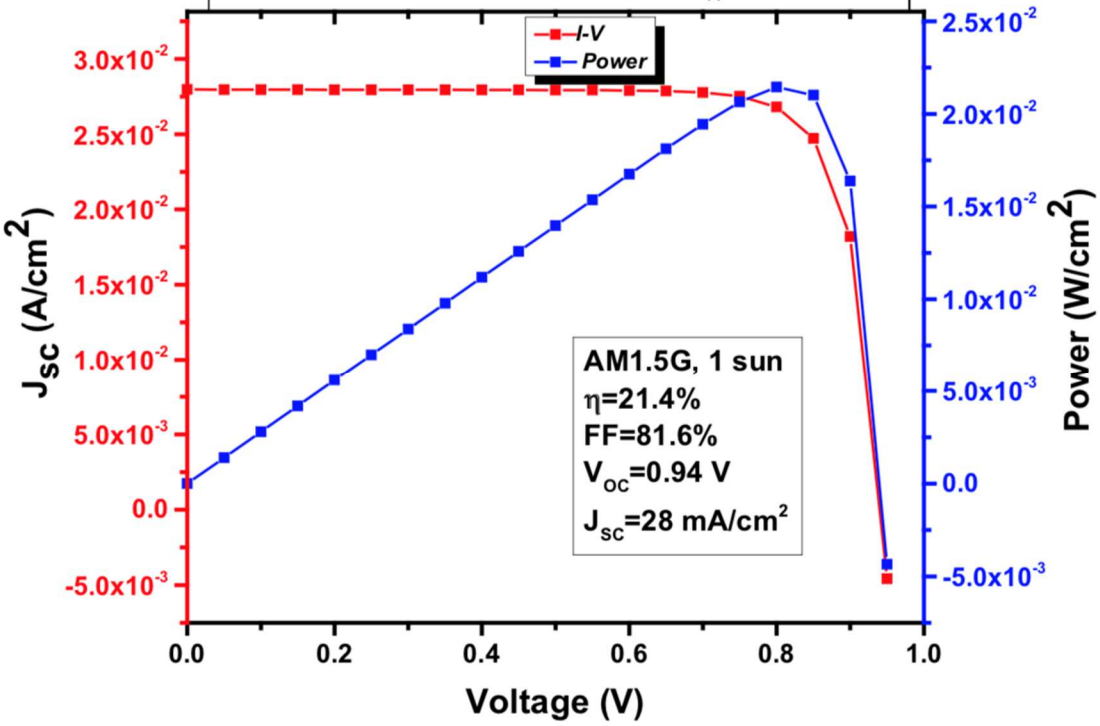


Figure 3.7 Optimized structure of single-junction GaAs SC on currently developed flexible substrate and simulated I-V characteristics of the SC

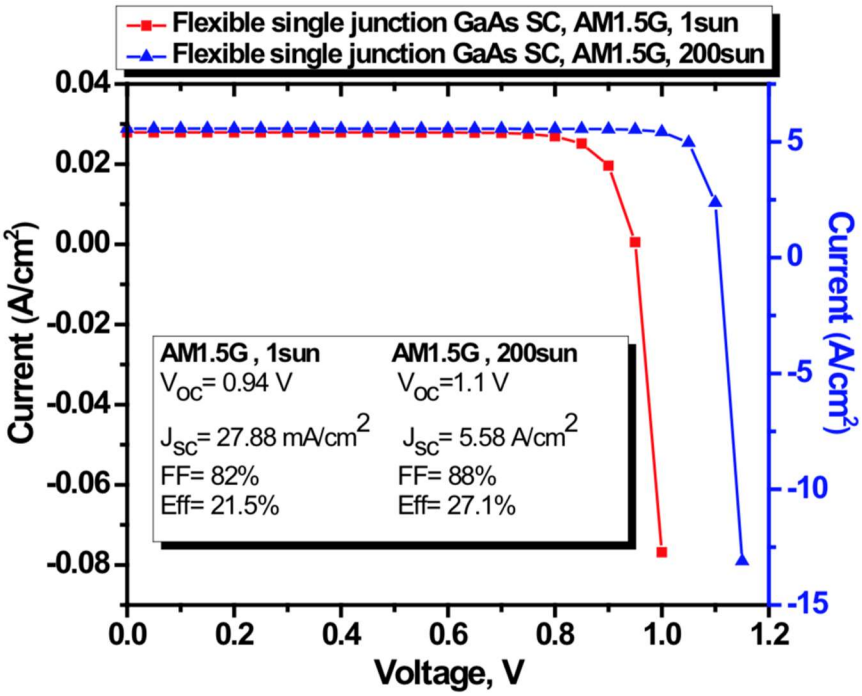


Figure 3.8 Light I-V characteristics of a single-junction GaAs SC on flexible substrate under AM1.5G 1- and 200sun spectral illumination conditions

3.5 Optimization of grid design for proof-of-concept SCs

It is quite known that a standard single-junction SC structure consists of a p-type emitter layer and an n-type base layer (or vice versa depending on carrier life time difference between electrons and holes) along with a wider bandgap window layer and a back surface field (BSF) layer on the top and bottom of the active region, as shown in Figure 3.9. Roughly the same structure will be used in the case of flexible substrate. Technically, the design of single-crystal semiconductor SCs has been optimized [60]; however, in this work, due to the nature of the single-crystalline-like semiconductor SCs on flexible substrate, epitaxial growth and device structures are required to be further optimized. Unlike the SCs on single-crystalline substrates that can be electrically

conductive, ceramic substrates and other resistive buffer layers (even in the case of using metal substrates) will require a front contact for bottom electrode in addition to a front electrode. The resulting device geometry and different charged carrier (electrons and holes) dynamics require new epitaxial structure designs. Linear grid spacing of metal electrode for the bottom contact as well as front contact critically determines the effects from shadowing (smaller spacing) and high sheet resistance (larger spacing). A collecting linear grid pattern for a GaAs SC has been considered. The grid dimensions of the pattern will be optimized for maximum power output form the cell. Grid design issues can be considered into two parts: the first is the choice of a grid pattern, cause there is no general mathematical method of predicting the best form, and the second part of the problem is to optimize the chosen pattern so that the spacing, width, and thickness of the lines results in minimum power loss or maximum power output.

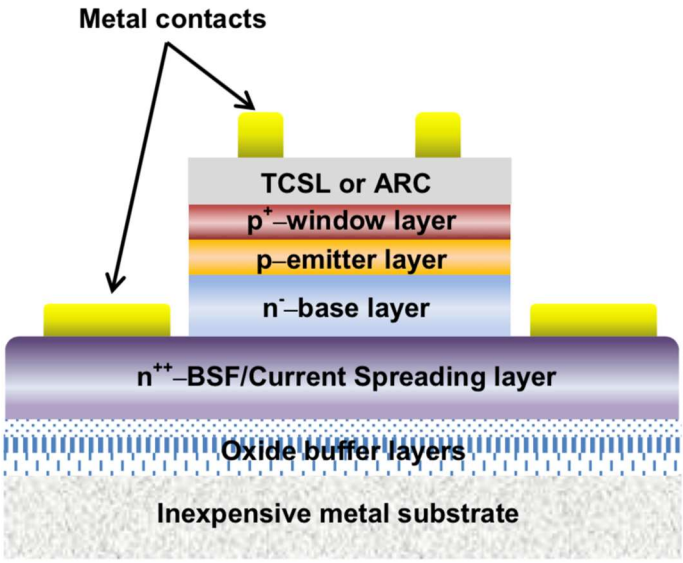


Figure 3.9 Schematic illustration of the initial design for proposed single-junction III-V SC on flexible substrate.

In order to satisfy the design rules for a grid optimization, all sources of parasitic resistive losses in a SC should be considered. There are four sources of parasitic resistive losses which are spreading resistance in the surface sheet under the grid, line loss in the resistance of the grid line, contact resistance loss at the metal-semiconductor contact area, and the grid shadowing.

It is necessary to include a constraint on the thickness of a grid line, stated as the ratio of width/thickness that is technologically practical. It is best to calculate the power loss $\int I^2 dR$ for each contribution. The structure of the linear grid is shown in Figure 3.10. It is simplest structure and forms the basis of computations for more complicated patterns. It has been assumed first that the front surface of the cell carrying the grid is uniformly illuminated by sunlight, and second that the photo-generated current from the junction flows uniformly into the surface sheet and spreads laterally to be collected by the grid lines.

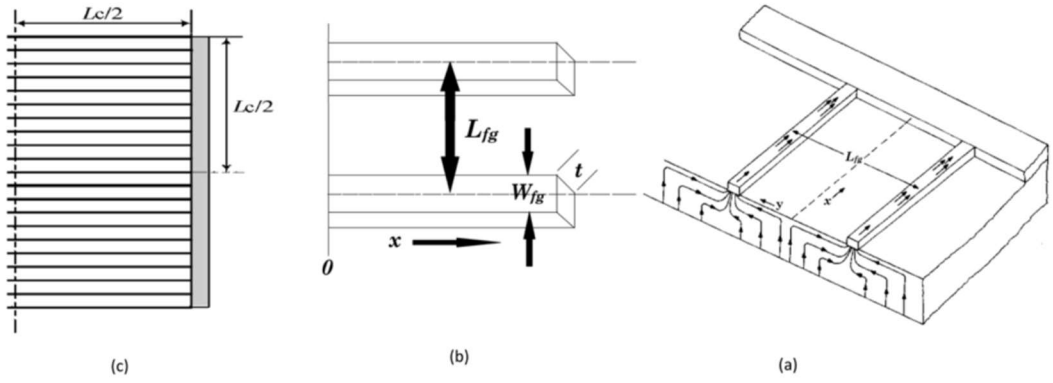


Figure 3.10 Linear grid configuration used in this study

Considering all the four components of power loss, grid spacing (Lfg) and grid width (Wfg) can be calculated by solving the Eq. 6 and 7.

$$\frac{V_m}{J_m} = L_{fg}^3 \left[A + B\sqrt{L_{fg}}\right], \quad (6)$$

where $A = \frac{2\rho_c\rho_s}{n\rho_c L_c^2}$, $B = \frac{\sqrt{2}\rho_s^{3/2}}{3\sqrt{n\rho_m}\,L_c}$, and

$$S^2 = \frac{n\rho_m L_c^2}{2\rho_c L_{fg}^3}, \quad (7)$$

where ρ_c and ρ_s are the top specific contact resistance and sheet resistance, respectively, V_m and J_m can be obtained based on the simulation for p^+-p-n structure in the case of high TDD. Detailed computations are discussed elsewhere.

Metal contact resistivity (ρ_m), shadowing ($S=W_{fg}/L_{fg}$) and L_c are also the known parameters. In order to optimize the grid specifications, sheet resistance needs to be evaluated. If conventional contact design with heavily doped GaAs as a contact layer (see Figure 3.11) is used for the single-junction GaAs SC, calculations showed very large sheet resistance in the order of 10^5 *ohm/square*. Based on the calculations, optimized conditions for grid spacing and width are $\sim 37\ \mu m$ and $\sim 0.7\ \mu m$, respectively. Therefore, the total number of grids will be around ~ 540 in ~ 2 *cm* length of a device, which means current spreading in the window and emitter is critically low, hence too many contacts need to be applied on to compensate current spreading issue. Besides, in the fabrication point of view it is impossible to create 540 grids in just 2 cm length of a device with photolithography. In order to reduce the effect of high sheet resistance in window and emitter layers, transparent current spreading layer (TCSL) can be used.

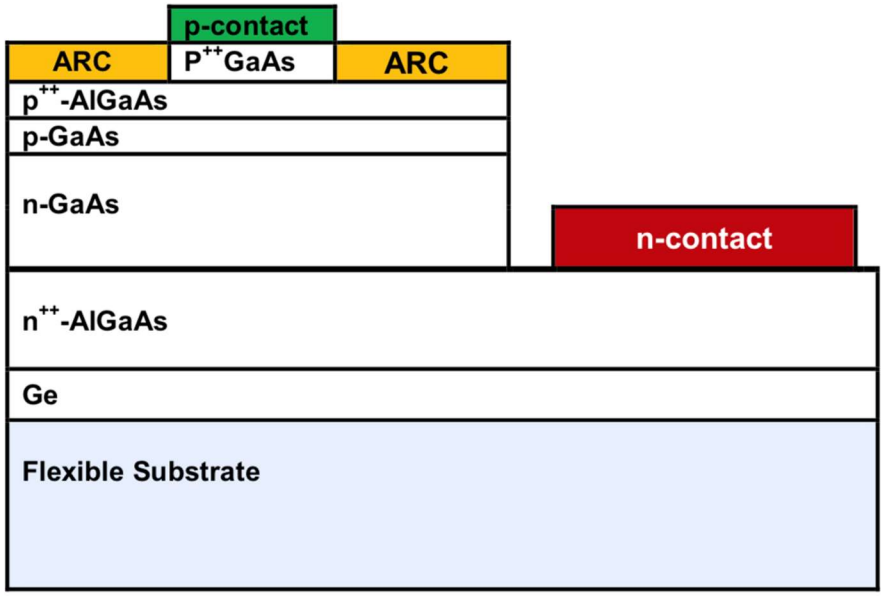


Figure 3.11 Schematic illustration of a single-junction GaAs SC on flexible substrate. Emitter layer (p++-AlGaAs, 1×10^{18} cm^{-3}) is used to calculate ρ_s.

3.6 The Effect of TCSL on Sheet Resistance and Design

The function of the current spreading layer is to ensure that the injected current is spread as evenly as possible across the whole active near surface area of the device [61]. Transparent and conductive oxide (TCO) layers are widely used for many microelectronics applications, such as transparent electrical contacts electrodes in LEDs, touch screens, thin film solar cells, etc. Indium tin oxide (ITO) is one of the most investigated and used transparent conductive oxides due to the high electrical conductivity and high transparency in the visible light wavelength range [62]. Indium Tin Oxide (known as ITO) is a degenerate n- type semiconducting material that has wide applications in optics and optoelectronics, which has lower resistance (orders of magnitude lower) in comparison with p^{++}-GaAs and p^{++}-AlGaAs [63], [64]. As it illustrated in Figure 3.12, TCSL, window and emitter are parallel resistances. Therefore,

total sheet resistance can be written in Eq. 8. According to the previous calculations, sheet resistance of window and emitter layers are orders of magnitude higher than TCSL, so Eq. 8 can be simplified in Eq. 9, hence total sheet resistance for the top contact will becomes equal to the sheet resistance of the TCSL as

$$\frac{1}{R_{sh}} = \frac{1}{R_{sh,window}} + \frac{1}{R_{sh,emitter}} + \frac{1}{R_{sh,TCSL}} \text{ and} \quad (8)$$

$$R_{sh} = R_{sh,TCSL}. \quad (9)$$

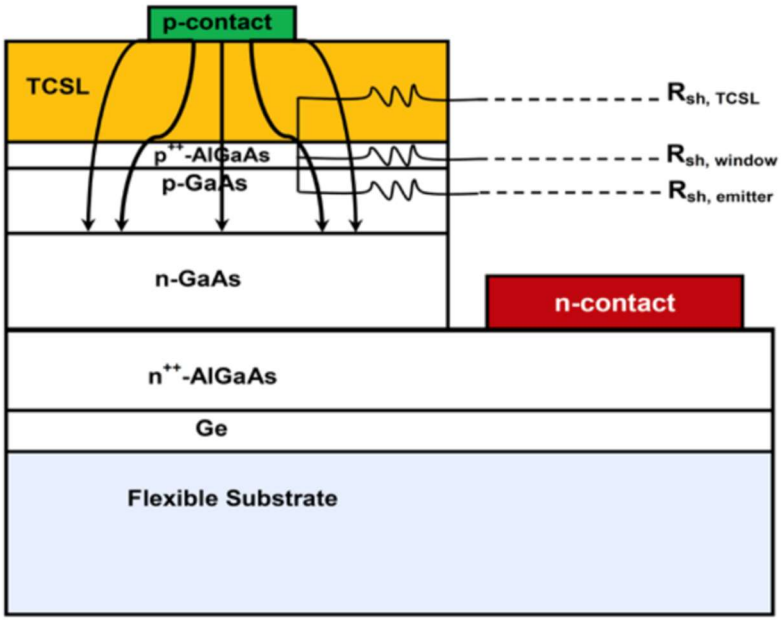


Figure 3.12 Current spreading structures in single-junction GaAs SCs on flexible substrate. Illustration of the effect of a current spreading layer for SCs with a TSCL.

According to the literature [63], by optimization of deposition condition a good sputtered ITO layer will be attained with low sheet resistance (~*100* Ω/□) and a high transmittance of visible light. Considering the sheet resistance of ~*100* Ω/□ for TCSL layer, grid specifications can be calculated using Eq. 6 and 7. Results showed that only

four fingers will be required for *2 cm* length of a device, which corresponds to the $L_{fg} \approx 0.143\ cm$ and $W_{fg} \approx 4\ \mu m$. Therefore, design and fabrication issues can be easily resolved by introducing and engineering of a TCSL into the top-contact.

3.7 Optical Properties of ITO

ITO-on-glass deposited using UHV DC-sputtering with the following conditions: DC power of 100 W, 35 sccm Ar and no Oxygen were flowing during sputtering, and subsequent annealing is carried out on a hot-plate at different temperatures (250 °C, 300°C and 350°C) in air atmosphere. Post-deposition annealing of ITO films causes an increase of the degree of internal order via crystallization. In the case of as-deposited ITO films it can be assumed that the lack of oxygen content during deposition induces an amorphous structure and the film becomes nonstoichiometric without the required amount of oxygen to form a crystalline film [65].The transmittance of the as-deposited films shows a dependency of the O_2 flow, and films deposited without Oxygen shows a very low transparency (see Figure 3.13) due to the Oxygen deficiency. However, it is very difficult to control the Oxygen flow rate in DC- sputter, precisely, and the required oxygen vacancy for highly doped ITO films cannot be attained. Results showed higher sheet resistances for the as-deposited films with higher O_2/Ar which is attributed to formation of oxygen-related interstitial defects. When the amorphous film is annealed, enough energy is supplied for incorporation of the oxygen present in the annealing ambient and a crystalline structure will be formed, hence the conductivity will be increased. The reduction in resistivity due to annealing of ITO films deposited without oxygen is therefore attributed to the out-diffusion of the non- stoichiometric extra

oxygen. Results showed that ITO films deposited without Oxygen and annealed at 350°C for 1 hour on hot-plate in air have highest transmittance and lowest sheet resistance.

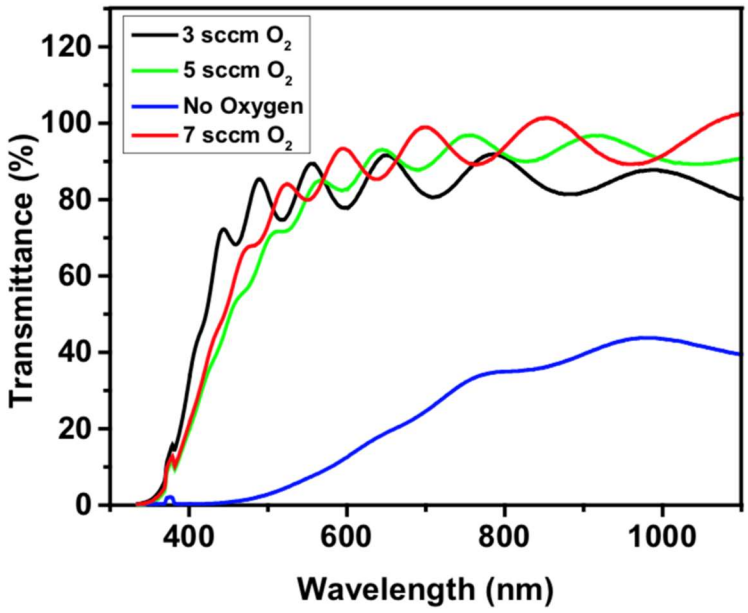


Figure 3.13 Transmittance of the sputtered ITO at different oxygen flow rates during deposition

In order to optimize the optical properties of the ARC both transmittance and reflectance need to be evaluated. In the case of reflectance, FilmStar thin film coating software for a single layer of ITO as ARC and TCSL is used for thickness optimization. Optimized thickness which is corresponds to the minimum reflectance (at the maximum peak in solar spectrum for GaAs SCs which is $\sim 550\ nm$) has been obtained via Fresnel's formula. Figure 3.14 shows the simulated results for the reflectance of ITO layer at

different incident angles. Calculations based on Fresnel's formula confirmed that lowest reflectance (< *5%*) will be achieved when the thickness of the ITO layer is *~70-80 nm*.

3.8 Ohmic Contacts to GaAs SCs

Metal-semiconductor (M-S) contacts are one of the key components in any semiconductor devices. Low- resistance, stable contacts are critical for the high-performance and reliability of photonic and optoelectronic devices, hence major efforts required for their preparation and characterization during device fabrication. Contacts can behave either as a Schottky barrier, or as an ohmic contact, depending on the characteristics of the interface. Schottky barriers act as rectifiers (diode-like), while ohmic contacts provide current linear with applied voltage (i.e., constant resistance).

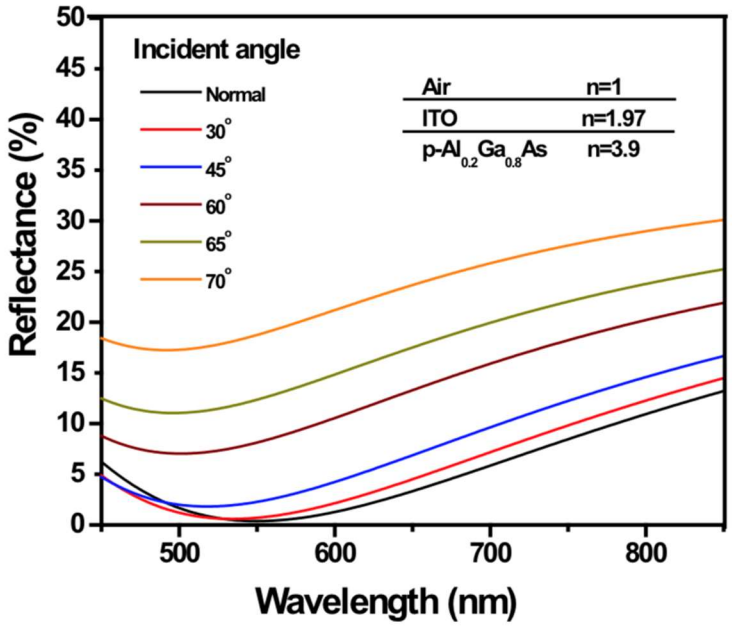


Figure 3.14 Simulated reflectance spectra of the ITO layer as ARC and TCSL as a function of incident angle

3.8.1 Ohmic Contacts to n-type GaAs

The Ni/AuGe/Ni/Au (5nm Ni/100nm AuGe/35nm Ni/300nm Au) contact with a eutectic composition of 88-12 Au-Ge (wt %) and a Ni overlayer is proven to be the most widely used contact to the n-GaAs [66]. Bottom Ni layer improves the adhesion of metal to the GaAs and the top one serves as a wetting agent, possibly enhances Ge diffusion (Ge serves as dopant), and prevents AuGa clustering due to its low surface tension. Thick Au overlayer enhances sheet conductivity, improves surface morphology, and enhances measurement accuracy (protective layer). During alloyed contact formation, Au reacts with substrate Ga to form various alloys, leaving behind a large concentration of Ga vacancies, and Ge diffuses into the GaAs, occupying the Ga sites and doping the GaAs heavily n-type nearby the surface.

The fabrication processes for the ohmic contacts formation have been done with lift-off process is brought in the appendix. Pre-cleaning of semiconductor samples performed via solvent cleaning (Piranha etch) in order to remove the organic contamination and other particles. However, short deep HCl cleaning is used just before metallization in order to remove the Gallium oxide from the surface.

For the investigation of sheet and specific contact resistance of highly doped n-type $Al_{0.2}Ga_{0.8}As$ (BSF layer), TLM patterns consisting of eight electrodes spaced with seven different intervals (d) ranging from 3 to 50 μm were formed on n-type $Al_{0.2}Ga_{0.8}As$ both on GaAs wafer and flexible substrate (see Figure 3.15). In the case of GaAs wafer, the I-V characteristics of the BSF layer were measured with a Signatone probe station and are depicted in Figure 3.16 and ohmic behavior (linearity) of the AuGe contacts onto

the n-type GaAs can be observed. Total resistance (RT) can be determined from the slope of the linear region of the I-V graph.

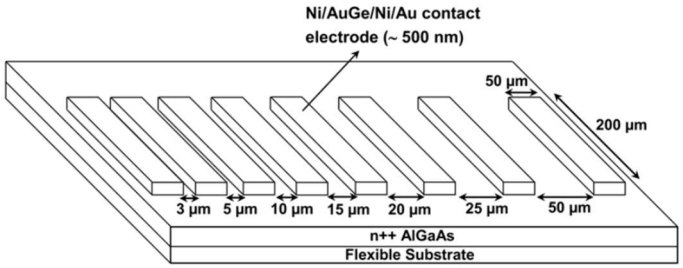


Figure 3.15 Schematic diagram of TLM patterns in GaAs SCs on flexible substrate.

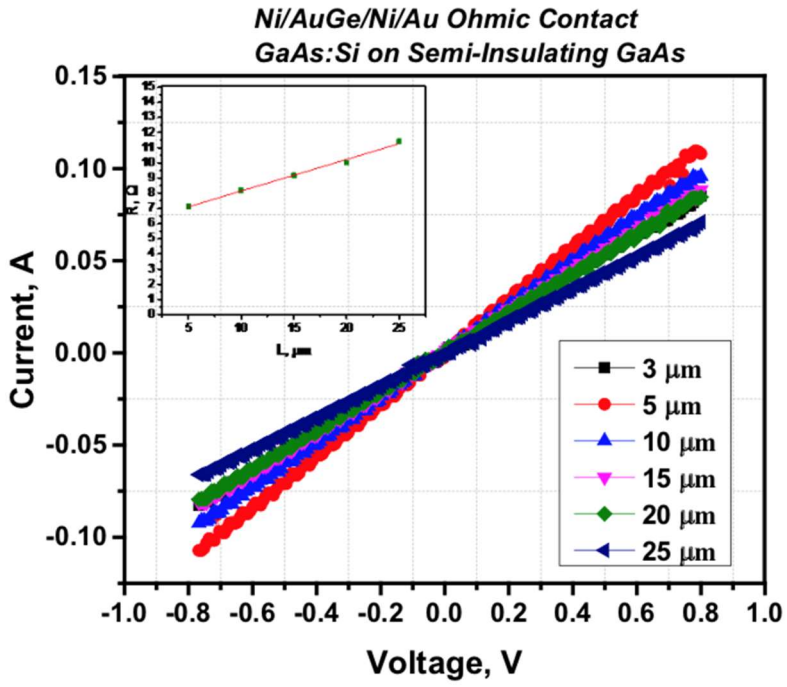


Figure 3.16 I-V characteristics of the AuGe ohmic contact on Si-doped GaAs (also the total resistance vs. gap spacing after RTP annealing is shown)

To determine the ohmic contact parameters (R_{sh} and ρ_c) with the TLM, resistance measurements can be made between any two adjacent contacts as depicted in Figure 3.15 [67]. The total resistance between any two contacts is given by

$$R_T = 2R_c + \frac{R_{sh}.l}{W}, \qquad (10)$$

where R_C is the contact resistance between metal and semiconductor, R_{sh} is the sheet resistance of the semiconducting layer outside the contact, l is the separation of the electrodes, and W is the electrode width fixed at 200 μm in this study. R_C and R_{sh} were estimated from the y-axis intercept and the slope of the R_T-l plot, respectively. According to the TLM measurements and in the case of GaAs wafer, the AuGe ohmic contact on n-type GaAs layer have been fabricated and, $R_{sh} \approx 35\ \Omega/\square$ and $\rho c \approx 6\times10^{-5}\ \Omega.cm^2$ are obtained.

3.8.2 Ohmic contacts to p-type GaAs

The ITO is usually not conducting enough to make a direct ohmic contact but is used as a TCSL with thin metal contact stacks. Due to the nature of the GaAs SCs on flexible substrate, high quality ohmic contacts will be required. According to the literatures [68]–[70], ITO as a degenerate semiconductor and Ti/Au as metal stacks can create a M-S contact on GaN devices with a specific contact resistance $<10^{-5}\ \Omega.cm^2$ resulting a very good ohmic contact after RTA annealing. Due to annealing, for example, at 300 °C for 70 s, Ti generates substantial interaction with Oxygen in n^{++}-ITO layer leading to the formation of TiO_2 crystal just across the interface between Ti and ITO creating more Oxygen vacancies close to the ITO-surface making ITO layer to be even more highly doped. The TiO_2 layer can also prevents an out diffusion of In and Sn from the

M-S interface to the top Au layer (Figure 3.17). Moreover, it prevents the in diffusion of possibly excess Au from the top layer to the M-S interface. Also, in the case of sheet and specific contact resistance of highly doped n-type ITO on glass, TLM patterns similar to that n-GaAs is used. According to the TLM measurements, the Ti/Au ohmic contact on n-type ITO layer have been fabricated and, $R_{sh} \approx \sim 20\ \Omega/\square$ (which satisfy the linear grid design requirement) and $\rho c \approx 10^{-4}\ \Omega.cm^2$ are obtained.

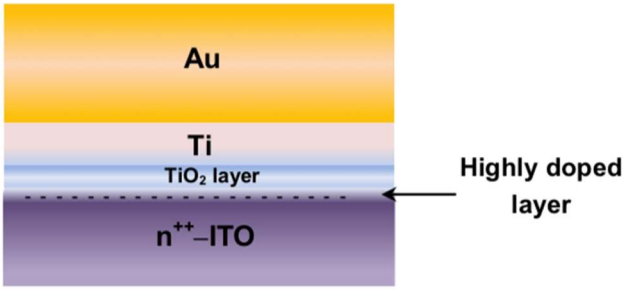


Figure 3.17 Schematic illustration of the ohmic contact formation for the ITO/p-GaAs

3.9 Summary

In this study, high-quality, light weight, inexpensive, flexible and scalable substrates are used to fabricate next generation of III-V SCs. High quality of *n*- and *p*- doped GaAs and AlGaAs are deposited on flexible substrate via a newly designed roll-to- roll MOCVD system (by Dr. Selvamanickam's group in the University of Houston). Simulation of GaAs SJ SCs on flexible substrate using standard structure showed very low conversion efficiency. Therefore, further optimization for GaAs SJ SCs on flexible substrate carried out and successful results obtained, efficiency >21% in the case of AM1.5G, 1 sun, >27% in the case of AM1.5G, 200 sun. Successful lift-off processes for the flexible GaAs SC have been confirmed. Most of the critical issues related to the

device performance were optimized before actual SC fabrication including front illumination design, SC mask design, fabrication of *n*- and *p*-contacts, mesa etch and TCSL design (current spreading). Current spreading issue has been resolved by introducing ITO layer into the SC design. In the next chapters, fabricated flexible SC devices will be characterized, and their performance and presumable issues will be analyzed.

CHAPTER 4 FLEXIBLE THIN FILM SINGLE-CRYSTAL-LIKE GAAS SC ON CHEAP METAL TAPE

4.1 Introduction

Currently dominant crystalline silicon (Si) photovoltaics (PV) faces serious techno-economic challenges, mainly from increasing pressure of lower market price in spite of nearly fixed manufacturing costs of the wafer materials. In addition, wafer-based devices do not offer mechanical flexibility in cells and modules. Solar cells (SCs) based on thin-film technology, which are not dependent on the wafer substrates, have the potential for low-cost manufacturing and flexible PV modules [71]. Thin-film SCs have been developed using non-single-crystalline materials. While they showed promising results in certain characteristics, they have drawbacks, such as low maximum conversion efficiencies (amorphous/microcrystalline Si, SnS, dye sensitized, copper indium gallium selenide, and organic SCs)[40], [72]–[75], poor stability by humidity, heat, light, and oxygen (perovskite SCs)[76], and use of toxic and/or rare element (perovskite and CdTe SCs). To overcome the challenges, necessary is an integration of SC materials with optimum bandgap energy, high absorption coefficient (direct bandgap semiconductors), and high quality (single crystalline) on economical flexible substrates using easily scalable process.

III-V compound semiconductors are the best PVSC materials for high conversion efficiencies with ~29% [40] and ~46% [41] for single- and multi-junction cells, respectively, thanks to their tunable optimum bandgaps and efficient absorption of solar spectrum. However, they are expensive and lack the mechanical flexibility and manufacturing scalability due to their starting platform of germanium (Ge) or gallium

arsenide (GaAs) single-crystalline wafer substrates. In the present study, we integrate the high-quality III-V thin films and low-cost flexible substrate by direct deposition, not by layer transfer [77], [78]. For the deposition, the SC materials (III-V thin films) are to be deposited on non-single-crystalline materials (flexible substrate), which will generally result in non-single-crystalline SC materials. We developed a new PV platform where nearly single-crystalline III-V thin films are directly deposited on the polycrystalline metal substrates using crystallinity-transformational buffer layers [79]. A similar technology platform was used to demonstrate high-performance flexible transistors by the authors [55], [80]. The technique was also employed to fabricate Si SCs; however, the conversion efficiency (~0.85%) was significantly lower than those of its siblings with inferior crystalline quality such as amorphous and microcrystalline Si [42].

4.2 Results and discussion

4.2.1 Single-crystal-like III-V solar cell structure

The epitaxially grown Ge on the oxide buffer layers/Hastelloy flexible tape (explained in chapter 3) is used as the substrate for the epitaxial growth of III-V SC device layers structure.

Whereas the nearly single-crystalline materials, also referred to as single-crystal-like materials, are significantly better than other thin-film amorphous and polycrystalline materials, they are not completely free of crystalline defects, containing dislocations and low-angle grain boundaries. The existence of the defects makes the lifetimes of minority carriers, hence their diffusion lengths shorter than those of single-

crystalline materials. When the layer structure of conventional GaAs SCs is employed in the single-crystal-like SCs, conversion efficiency decreases with reduced carrier lifetimes (explained in chapter 3, Figure 3.6). Another difference in the design of the SCs is the device configuration. The SCs in this study must adopt a lateral device configuration, as opposed to a vertical configuration of typical III-V SCs, due to the existence of electrically resistive oxide buffer between the metal substrate and active device region. The differences in the device geometry and carrier dynamics require new epitaxial structure and device designs.

In the previous chapter, the optimized device design and simulated IV characteristic results were reported for our initial p-up device layers structure. Here, we investigate n-up III-V semiconductors structure for flexible GaAs solar cell fabrication. Therefore, a numerical simulation was also employed for the SC design optimization with n-up structure considering reduced minority carrier lifetimes of $\tau \sim 1$ nanosecond (ns), which is an estimated value based on the time-resolved photoluminescence measurements of developed single-crystal-like GaAs films. The carrier lifetime is similar to ones of GaAs grown on metamorphic SiGe substrates with dislocation density of 10^7–10^8 cm^{-2} [81]. Other material parameters were taken from literatures (Table 4.1). The modeling results suggest that single-junction (SJ) SCs based on the single-crystal-like GaAs can achieve the conversion efficiencies higher than 21% under the AM1.5G and 1-Sun condition (Figure 4.1).

Table 4.1 Materials properties used in the numerical simulation of flexible single-crystal like GaAs SJ SCs

Material	**GaAs**	**$Al_xGa_{1-x}As$, x = 0.2-0.4**
Band gap (eV)	1.424	$1.424+1.247x$ ($x < 0.45$)
Electron affinity (eV)	4.07	$4.07-1.1x$ ($x < 0.45$)
Dielectric constant	12.9	$12.90-2.84x$
Electron mobility ($cm^2/V{\cdot}s$)	600[a)]	600 [a)]
Hole mobility ($cm^2/V{\cdot}s$)	300 [a)]	300 [a)]
Carrier lifetime (ns)	1, 5, 10	1, 5, 10
Lattice constant a (Å)	5.65325	$5.6533+0.0078x$
Surface recombination (cm/s)	10^7	10^7
Radiative recombination coefficient at 300 K (cm^3/s)	7.2×10^{-10}	1.8×10^{-10}
Auger coefficient at 300 K (cm^6/s)	10^{-30}	0.7×10^{-31}
Doping gradients	Uniform	Uniform

Physical models	- Recombination models:
	  - Shockley-Read-Hall (SRH)
	  - Optical (OPTR)
	  - Auger
	- Carrier statistics models
	  - Fermi-Dirac (Fermi)
	  - Bandgap Narrowing (BGN)	

[a)] Experimental value measured in this work. The mobility values are significantly higher than other non-crystalline materials.

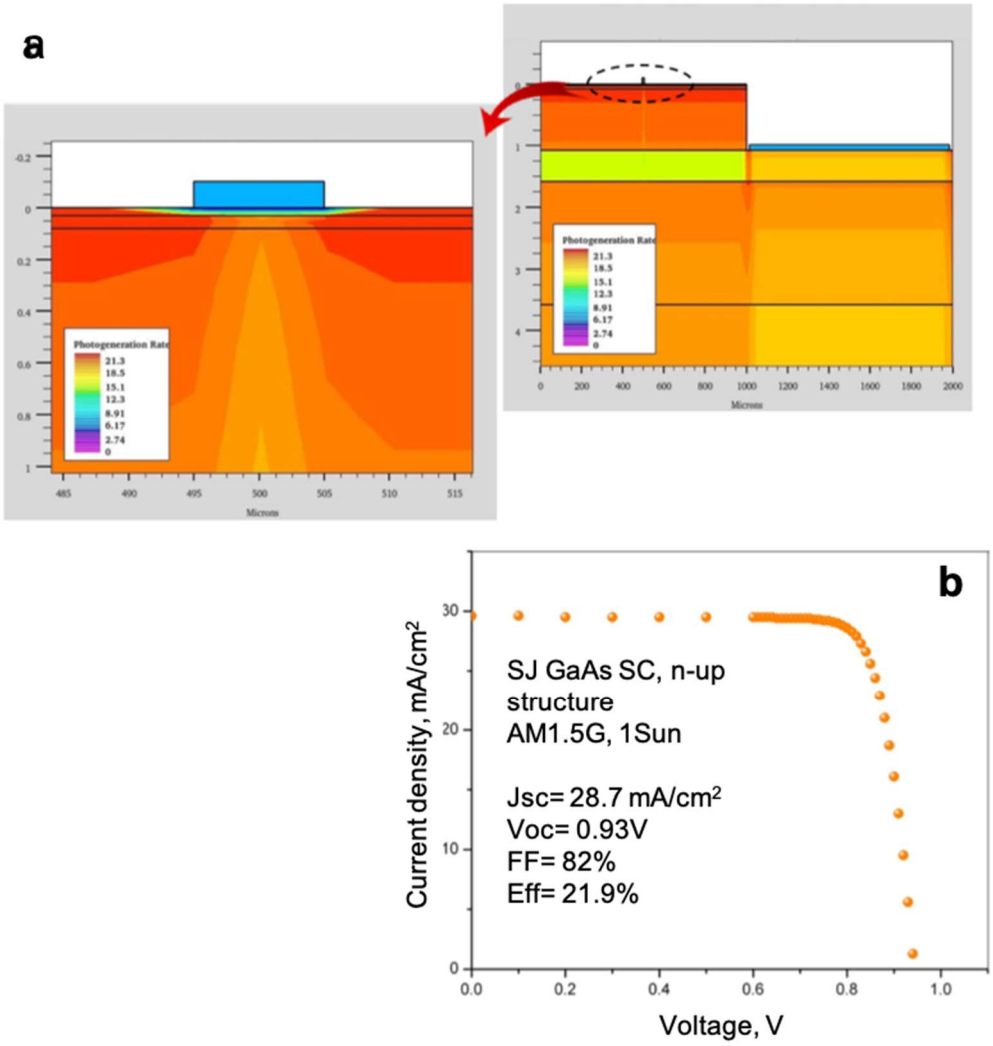


Figure 4.1 (a) 2D profile of photo-generation rate of carriers in the SJ GaAs SC. (b) Simulated J-V characteristic of an optimized SC design shows high photo conversion efficiency higher than 21% from single-crystal-like GaAs SJ epitaxially grown on polycrystalline metal tape.

According to the simulation result, the optimized GaAs/AlGaAs device layers structure has been grown by metalorganic chemical vapor deposition (MOCVD) on the Ge buffer layer. The SC active region consists of unintentionally-doped GaAs (~2 μm), heavily zinc-doped *p*-type GaAs (contact layer p^{++}-GaAs:Zn), p^{++}-$Al_{0.4}Ga_{0.6}As$:Zn (back-surface field [BSF] layer), *p*-GaAs:Zn (base layer), n^{+}-GaAs:Si (emitter layer), n^{++}-$Al_{0.4}Ga_{0.6}As$ (window layer), and n^{++}-GaAs:Si (contact layer). The layers were

grown by MOCVD at growth temperatures of 625–750 °C and a chamber pressure at 20 Torr. For AlGaAs and GaAs epitaxial growth, trimethylgallium (TMGa, $Ga(CH_3)_3$), trimethylaluminum (TMAl, $Al(CH_3)_3$)) and arsine (AsH_3) were used as precursors of group III and group V elements. Diluted silane (SiH_4 balanced in hydrogen) and diethylzinc (DEZn, $Zn(C_2H_5)_2$) were also used for precursors of donor and acceptor dopants, respectively. Hydrogen (H_2) purified by a palladium (Pd) cell was mixed with the precursors as a carrier gas.

4.2.2 SC Device fabrication

The fabrication started with mesa formation by chemical wet etching of (Al)GaAs layers to expose the p^{++}-GaAs:Zn contact layer using an etchant mixture of citric acid and hydrogen peroxide ($CH_3COOH+H_2O_2$). The mesas were defined by photoresist (PR) patterns before the etching. The area of SC devices by mesas were 400×400 and 800×1000 μm^2 (or 0.0016 to 0.008 cm^2) for the measurement of the conversion efficiency. Patterned Ni/Ge/Au ohmic-contact metallization was applied on the n^{++}-GaAs:Si contact layer by electron-beam (E-beam) evaporation followed by PR lift-off. Cr/Au was deposited on the p^{++}-GaAs:Zn for metallization of *p*-type ohmic electrode. This step completed the first stage of the fabrication, referred to as "as-fabricated". The 40-nm n^{++}-GaAs layer on top of window layer was selectively etched, which is the second stage of "etched cap-layer". Then, a stack of ZnS/MgF_2 (48/80 nm) was deposited by E-beam evaporation on the devices as anti-reflection (AR) coating (the third stage of "AR coated"). For the measurement of external quantum efficiency (EQE) and internal quantum efficiency (IQE), separate SCs were fabricated with larger

dimension (3×4 mm^2). For the devices, a tin-doped indium oxide (In_2O_3:Sn or indium-tin oxide, ITO) layer (~ 90 nm) was deposited by DC sputtering at room temperature. The ITO was annealed at ~350 °C for 1 hour in air to achieve transmittance higher than 90%. A stack of patterned Ti/Au metals was deposited on the ITO. The quality of ohmic contacts was evaluated using transfer-length measurement (TLM) method.

4.2.3 Device characterization

Current vs voltage (*I–V*) characteristics of the fabricated devices were measured in a dark room using a solar simulator (Oriel Sol3A, Newport) under AM1.5G illumination 1-Sun condition with 0.1 W/cm^2 power density. This measurement was used to characterize cell performance by short circuit current, I_{SC}, indicating absorption and collection of light-generated carriers and open circuit voltage, V_{OC}, governed by the band-gap of semiconductor and degree of carrier recombination in the cell. Incident light flux of solar simulator was measured using a calibrated power meter and double-checked using a NREL-calibrated solar cell (model 91150V). A quantum efficiency measurement system equipped with a Xe lamp and a monochromator was used to measure the EQE of devices in the range of 400–1000 nm.

Figure 4.2(a) shows a schematic structure with optimized GaAs SJ-SC layers and oxide buffer layers. The oxide buffer layers including MgO, $LaMnO_3$, and CeO_2, are critical to transform the crystallinity from polycrystalline state (Hastelloy substrate) to single-crystal-like state (semiconductor layers) and to manage the strains between oxides and semiconductors. Especially, the MgO layer deposited by IBAD provides a seed with biaxially textured crystal grains, which can be used for the template of

semiconductor epitaxial growth. However, significant lattice mismatch between MgO and semiconductor material does not allow the growth of high-quality semiconductor layers. Therefore, $LaMnO_3$ and CeO_2 were employed as intermediate layers. The mismatch is significantly reduced from –0.256 between Ge and MgO to –0.044 between Ge (or GaAs) and CeO_2. The GaAs layers are nearly single crystalline as shown in Figure 4.2b. In-plane and out-of-plane texture of the GaAs layers were confirmed using ω scan around (004) peak and φ scan around (224) peak, respectively, of x-ray diffraction (XRD) (Figure 4.3). The scheme, processing conditions, and characterization of the buffer layers were described in detail in a previous report on flexible thin-film transistors [55]. The optimization and characterization of III-V semiconductor layers were reported elsewhere [82].

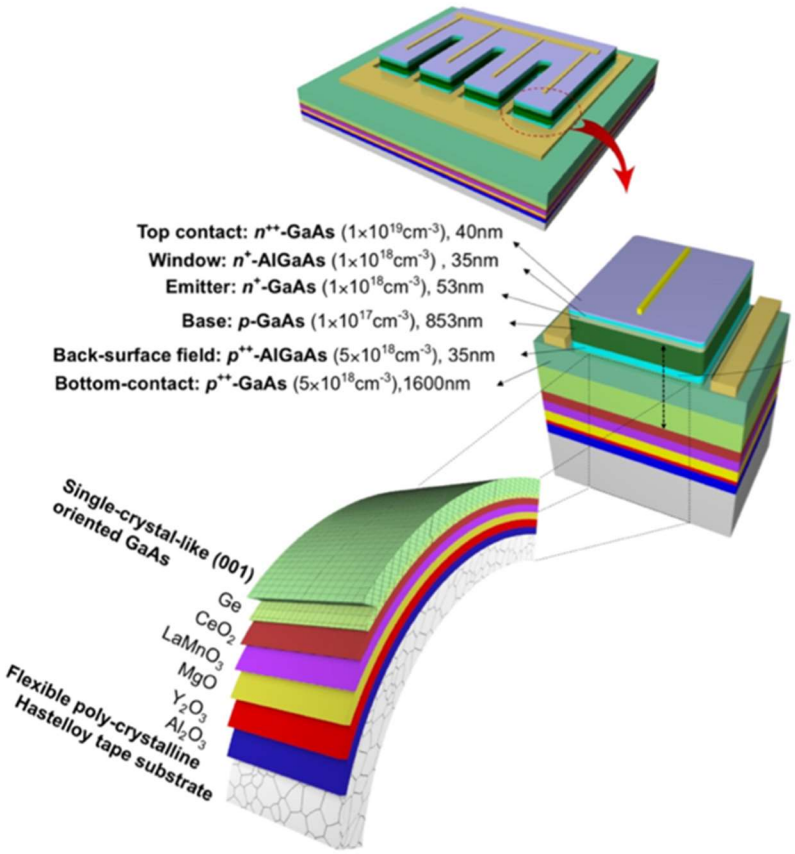


Figure 4.2 (a) Schematic illustration of device and layer structures of flexible GaAs SC

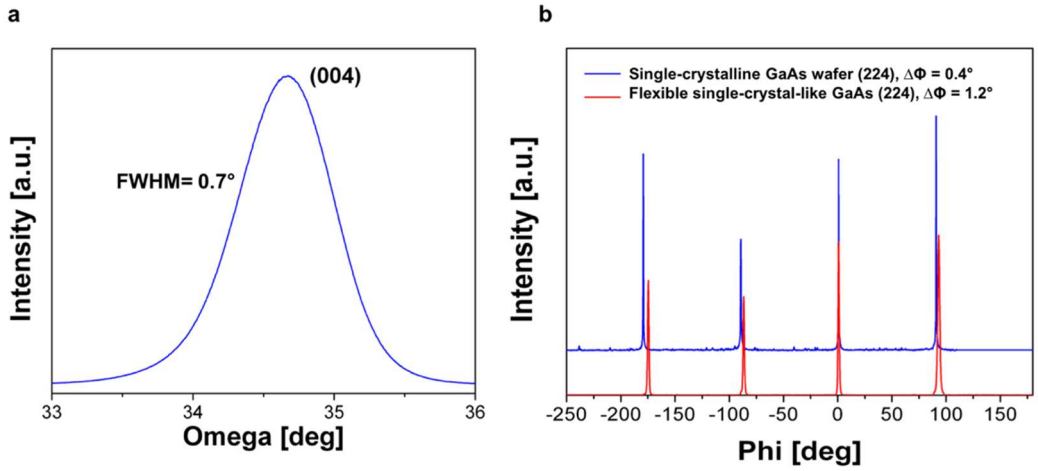


Figure 4.3 Structural properties of single-crystal-like GaAs thin-film layers grown on polycrystalline metal tape employing crystallinity-transitional buffer layers, characterized by high-resolution x-ray diffraction (HR-XRD): (a) Rocking curve ω scan around (004) peak (b) rotational scan (φ scan) around (224) peak

The flexible epitaxial structures were fabricated into devices. The contact of electrodes and semiconductor layers were ohmic and specific contact resistances were low enough not to add parasitic series resistance in the diode (Figure 4.4). A bi-layered AR coating with ZnS and MgF_2 was applied to enhance the light absorption, thus increasing photocurrents (Figure 4.5) [83]. Also, the n^{++}-GaAs layer on top of window layer (*n*-AlGaAs) that was used to improve ohmic contacts was selectively etched. This GaAs layer can absorb part of incident light while not contributing to J_{SC} [84]. As the current SC devices have the lateral device configuration, the effects of side-walls and parasitic series resistance will play a role in the performance characteristics.

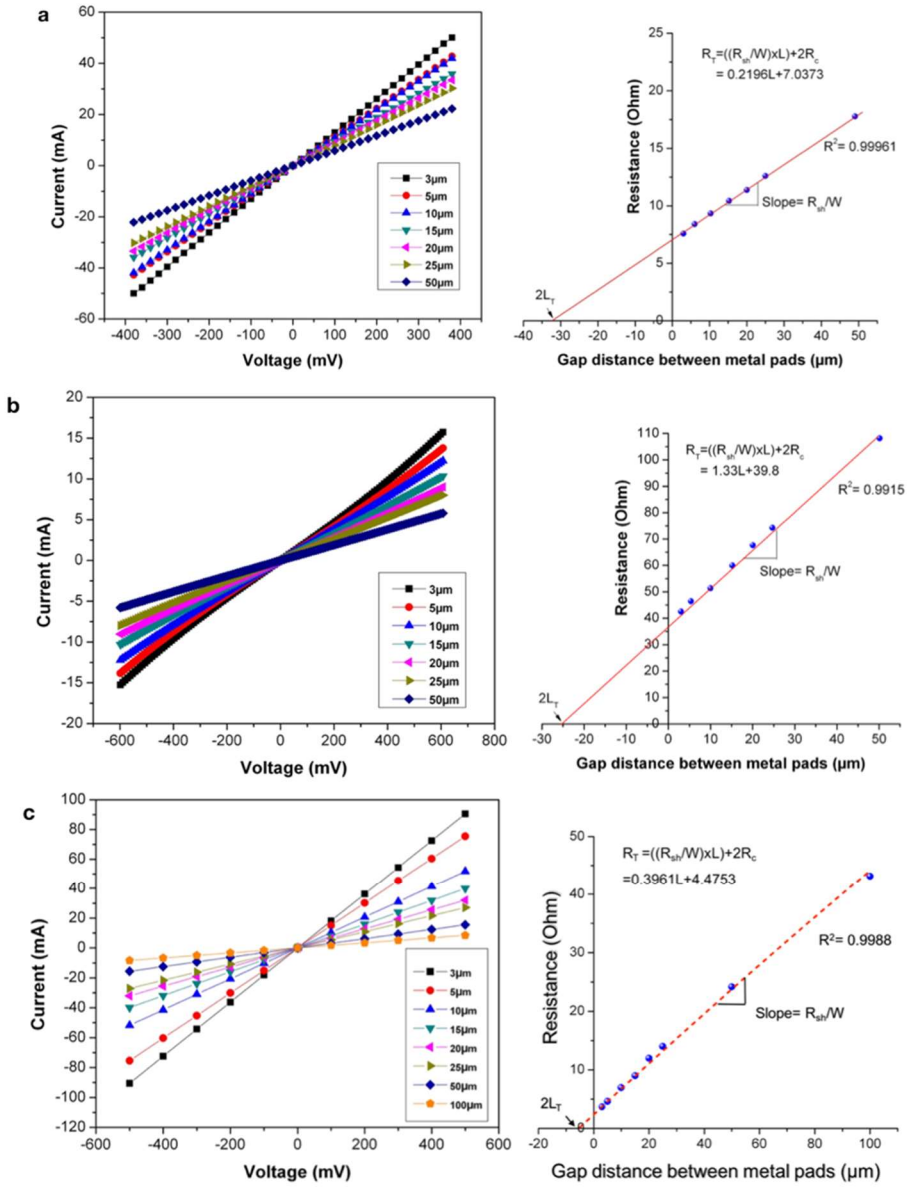


Figure 4.4 Transfer-length method (TLM) measurement and analysis to evaluate contact resistance of electrodes using (a) Ni/Ge/Au on n++-GaAs, (b) Cr/Au on p++-GaAs, and (c) Ti/Au on ITO/n++-GaAs.

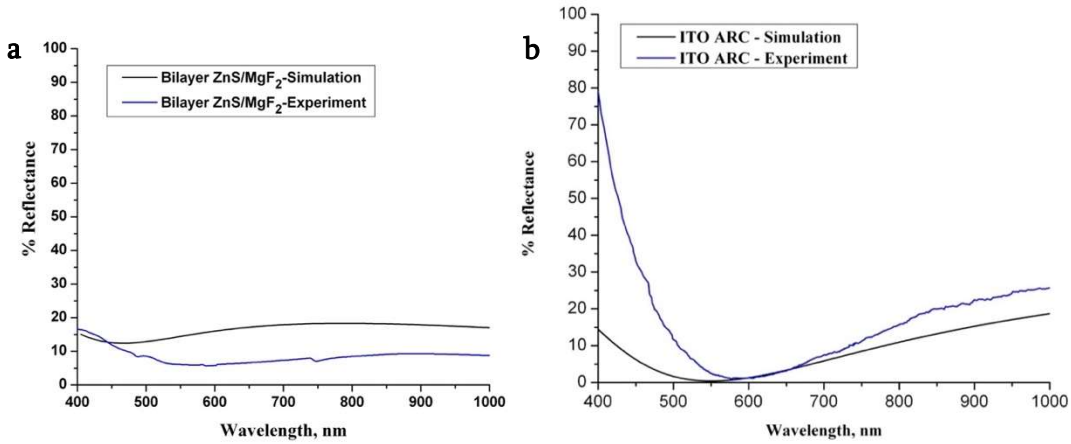
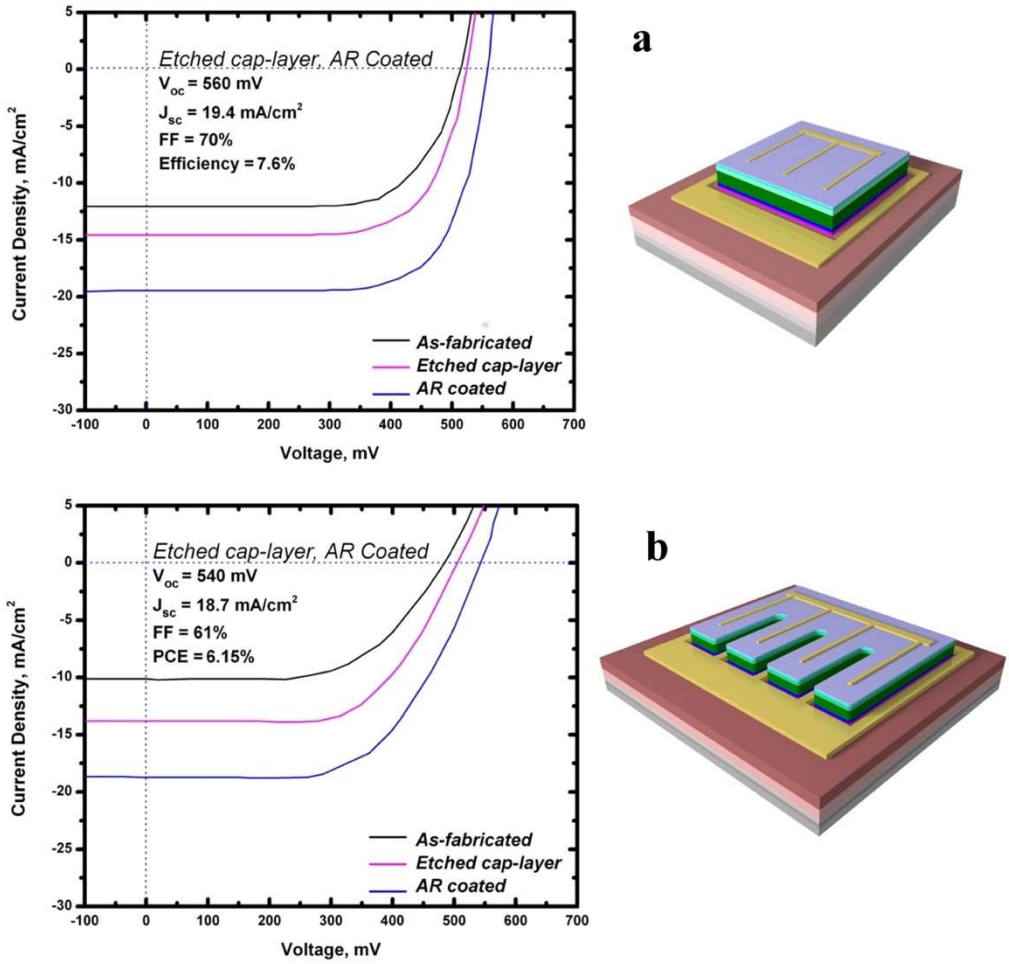


Figure 4.5 Simulated and experimentally measured reflectance percent of (a) bilayer ZnS/MgF2 (48/80 nm) and (b) single layer ITO (90nm) on the SC devices as anti-reflection coating deposited by e-beam evaporation.

Figure 4.6 shows current density vs voltage (*J–V*) characteristics of SC devices with two different mesa sizes. For the estimation of J_{SC}, we only consider the active device area that is not covered by opaque metal electrodes. J_{SC} and V_{OC} increase for the devices after cap layer removal and ARC from the as-fabricated devices. The best conversion efficiency is ~7.6% with an open circuit voltage, V_{OC} = ~0.560 V, a short circuit current, J_{SC} = ~19.4 mA/cm^2, and a fill factor (FF) = ~0.70 (blue curve of Fig. 38a) from the smaller devices with a size of 0.4×0.4 mm^2. Smaller devices (Fig. 38a) generally show higher efficiencies than larger devices (Figure 4.6b) mainly due to higher J_{SC} and FF than those of larger devices (J_{SC} of ~18.7 mA/cm^2 and FF of 0.61). As a result, when the dimension of devices increases, conversion efficiency slightly decreases from ~7.6% to 6.15% for 0.4×0.4 mm^2 and 0.8×1 mm^2 devices, respectively, suggesting that the presence of parasitic series resistance from lateral transport of carriers in the contact layers. A table in Figure 4.6 summarizes the performance characteristics depending on the device sizes and fabrication steps.



Performance characteristics	Fabrication	**a** 0.4×0.4 mm^2 (15% shadow)	**b** 0.8×1 mm^2 (9.5% shadow)
J_{sc} [mA/cm^2]	As-fabricated	12	10
	After cap removal	14.8	14
	After AR coating	19.4	18.7
V_{oc} [mV]	As-fabricated	518	480
	After cap removal	520	505
	After AR coating	560	540
FF [%]	As-fabricated	66	60
	After cap removal	67	60
	After AR coating	70	61
Conversion efficiency [%]	As-fabricated	4.1	2.9
	After cap removal	5.2	4.2
	After AR coating	7.6	6.15

Figure 4.6 Current density vs voltage (J-V) characteristics of different size and design SC devices using single-crystal-like GaAs single junction. (a) 0.4×0.4 mm2. (b) 0.8×1 mm2.

Conversion efficiencies of the flexible SCs are lower than that of defect-free SCs on single-crystalline wafers. Especially, V_{OC} is lower. As a result, bandgap-voltage offset, $W_{OC} = (E_g/q) - V_{OC}$ of the flexible SCs (>0.85 V) is higher than that of wafer SCs (<0.4 V). Dark *I- V* characteristics of the flexible GaAs SC (Figure 4.7) shows dark saturation current $I_0 \sim 3.5\times10^{-4}$ A/cm^2 (at $V = -0.5$ V), which is higher than wafer-based GaAs SCs with $I_0 \sim 10^{-7}$ A/cm^2. The higher saturation currents originate from higher carrier recombination centers which limits the V_{OC}. The major recombination centers are believed to be low-angle grain boundaries in the material [85], [86] and top surface and sidewalls of the device structure. Minimizing leakage current is necessary to simultaneously achieve higher V_{OC} and FF. Besides the expected improvement in J_{SC} (~87%) after the processing steps of GaAs cap-layer removal and ARC deposition, V_{OC} and FF were also improved. The leakage currents were reduced (Figure 4.7). The improvements suggest possible removal of parasitic leakage paths on sidewalls during GaAs cap-layer etching process followed by effective passivation of device top surface and sidewalls with a ZnS layer.

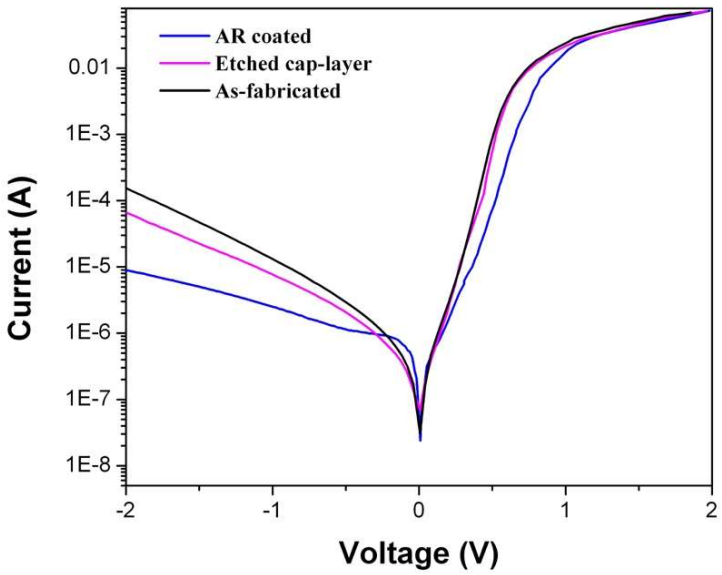


Figure 4.7 Current vs voltage (I-V) characteristics of 0.8×1 mm2 single-crystal-like GaAs SJ SC device after different steps of device fabrication

Figure 4.8 shows the measured EQE and estimated IQE curves together with reflectance of the flexible single-crystal-like GaAs SC (3×4 mm^2). The ITO layer of this device functions as not only a transparent conductive electrode but also AR coating. (Figure 4.5b). The conversion efficiency of this device is lower than those of devices shown in Figure 4.6. The measured EQE of flexible GaAs SC is lower than that of wafer-base GaAs SC for all the wavelengths and deviates from ideal EQE square shape [87]. An EQE of a single-crystalline III-V SC is compared in Figure 4.9. The overall reduction in EQE from the ideal quantum efficiency suggests shorter diffusion lengths and carrier lifetimes of photo-generated minority carriers in the single-crystal-like GaAs than those of single-crystal GaAs due to the existence of additional carrier recombination centers such as low-angle grain boundaries and threading dislocations. Detrimental effect of grain boundaries on EQE performance of GaAs SCs was reported

in a study conducted on SC structures grown on polycrystalline and single-crystalline substrates. The grain boundaries must play a role in the conversion efficiencies and EQE, while we expect less detrimental effect of low-angle grain boundaries in single-crystal-like materials than that of high angle-grain boundaries in polycrystalline materials. The EQE of >50% was measured in the wavelength range of 580–780 nm. The low QE at wavelengths shorter than ~500 nm is due to the inefficient extraction of carriers generated near the window and emitter layers and sidewalls. The un-passivated top and sidewalls' surfaces of the lateral flexible SCs should have high surface recombination rates, affecting high-energy photons absorbed close to the surfaces. In addition, high reflection of ITO for wavelengths <500 nm (Figure 4.5b) is also responsible for larger difference between IQE and EQE curves. Besides the passivation of the surfaces of top and sidewalls, further optimization of the AR coatings will improve the EQE and efficiency of the SCs in this short wavelength range. The observed loss in the EQE of flexible GaAs SC in the infrared (IR) region originates not only from recombination but also from optical losses due to light transmission and reflection for wavelengths longer than 700 nm. The design of single-crystal-like GaAs device structure with thinner layers to compensate for decreased diffusion length might not be efficient to absorb long-wavelength IR photons. There is a tradeoff for layers' thickness between light absorption and carrier collection which can be further optimized with improved materials having longer carrier lifetimes.

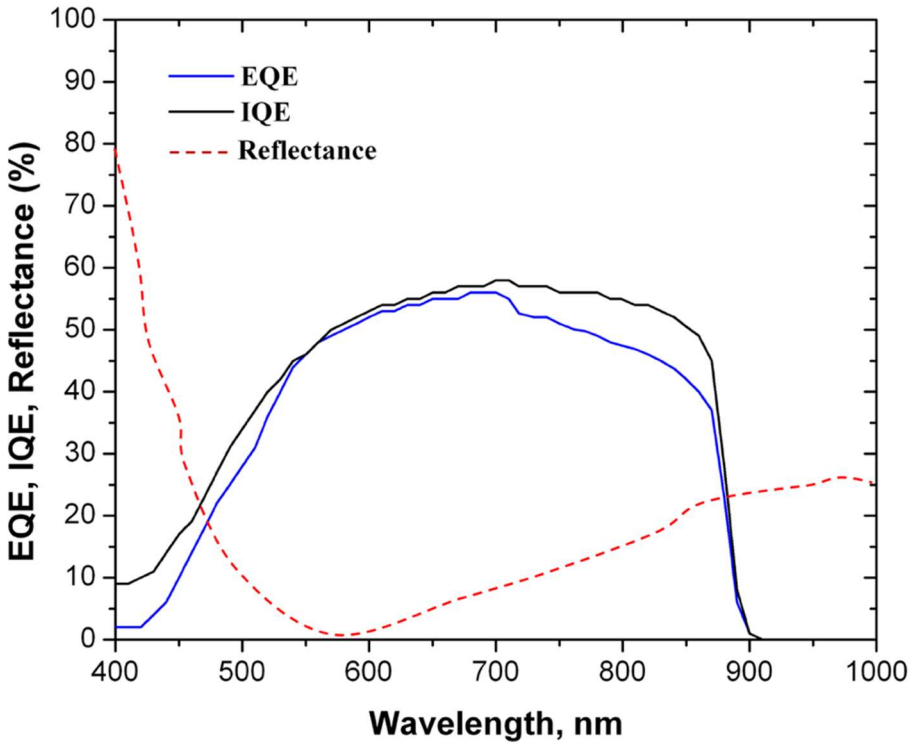


Figure 4.8 Spectrum-dependent EQE and IQE of a flexible GaAs SC. The SC has a dimension of 0.12 cm2 and ITO AR coating. J-V characteristics of this device show JSC = 13 mA/cm2, VOC = 0.355 V, FF = 0.60 and conversion efficiency = ~2.8%.

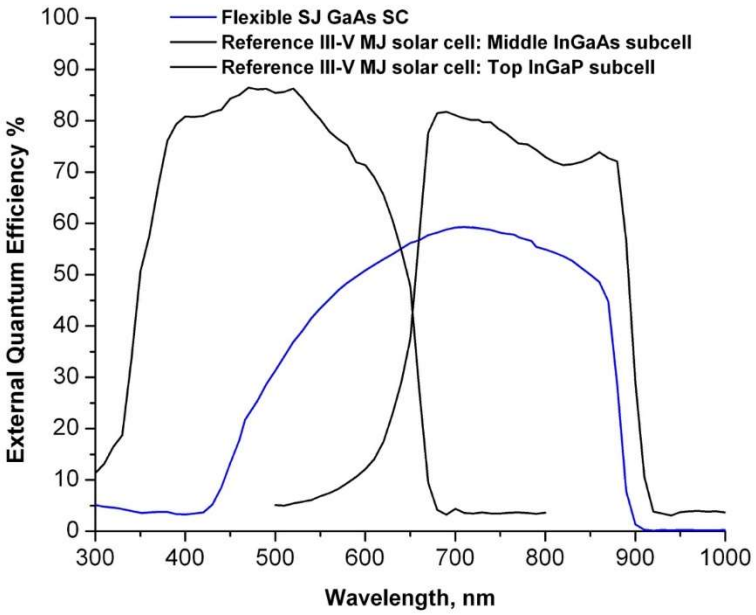


Figure 4.9 External quantum efficiency (EQE) of a commercial multi-junction single crystal III-V solar cell as a reference cell (black curves: top and middle sub cell) and flexible single-junction single-crystal-like GaAs solar cell (blue curve).

The fabricated flexible single-crystal-like thin-film GaAs SJ-SCs show very stable photon-conversion characteristic performance and no efficiency degradation over the time. After keeping the devices in ambient without specific protection/capsulation for longer than 7 months, no performance degradation was observed. Device mechanical stability is a necessity for flexible SC devices to power wearable or portable systems. Therefore, mechanical deformation and bending durability of the flexible single-crystal-like GaAs SCs were investigated. Stress stability of these flexible devices was tested for more than 60 devices by applying bending cycles up to 100 times. Mechanical bending in concave and convex modes with a curvature radius R of ±0.5 cm was applied. The generated in-plane strain under this external tensile and compressive stress condition was calculated as 0.5% (Figure 4.10). The performance characteristics of

tested flexible SCs do not show any degradation after stress bending tests, as shown in Figure 4.11.

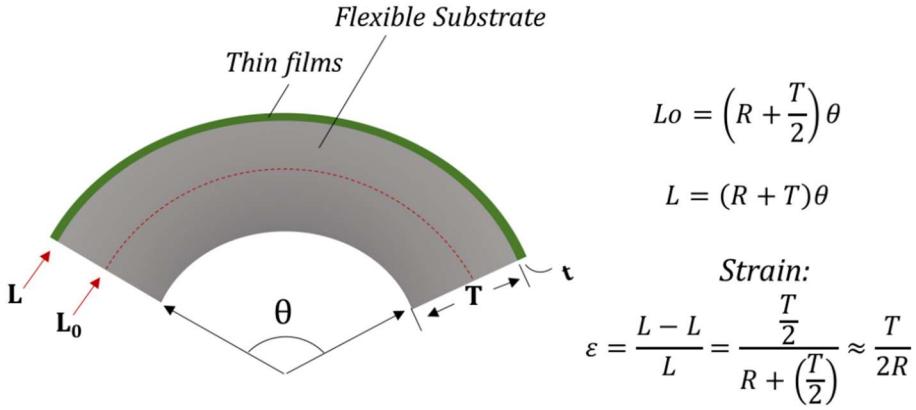


Figure 4.10 External strain calculation in bent thin films grown on much thicker flexible substrates with similar Young's modulus.

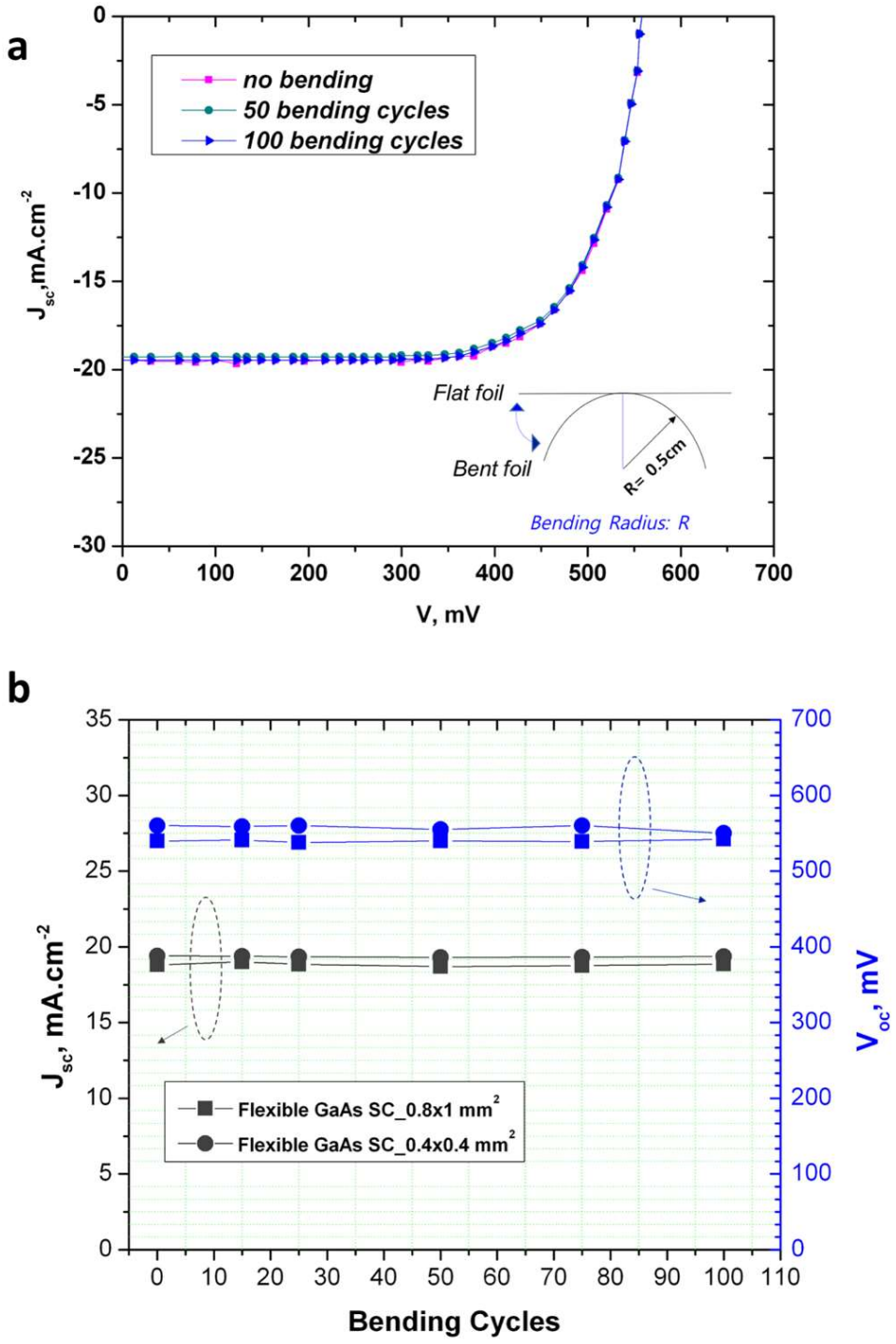


Figure 4.11 Stability of device performance characteristics after mechanical stress: (a) J-V characteristics of flexible GaAs SCs after 0, 50 and 100 bending cycles and (b) change in JSC, and VOC of flexible SC devices after 100 bending cycles.

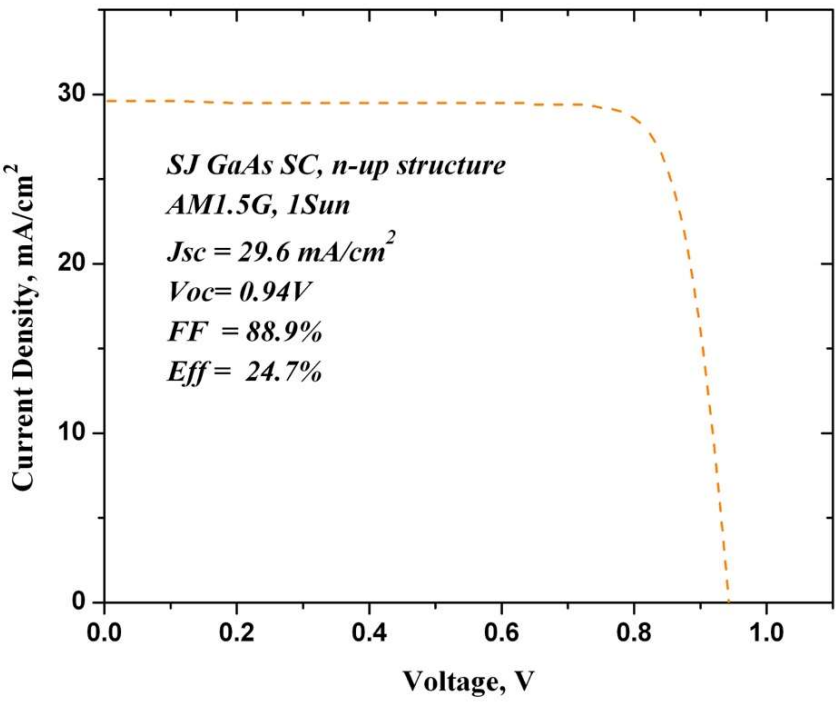


Figure 4.12 Current density-voltage (J–V) characteristic of GaAs SJ SC with optimized device architecture on flexible substrate with carrier lifetime of τ = 5 nm and τ = 10 nm.

4.3 Conclusion

The proof-of-concept device demonstration showed conversion efficiency of higher than 7.5% under the AM1.5G and 1-Sun condition. However, there is still significant room for further improvement of the performance for the flexible single-crystal-like GaAs SJ-SCs. Especially, V_{OC} of the device is lower than expected. The modeling suggests that the efficiency can be further improved higher than 23% and 24.7% when the carrier lifetime is enhanced to 5 ns and 10 ns by further improvement in material quality of single-crystal-like semiconductors (Figure 4.12). We believe that lower V_{OC} of current device is associated with low-angle grain boundaries in bulk materials, and threading dislocations. Improvement in V_{OC} can be achieved through passivation of these recombination sites [88], [89]. Furthermore, according to our studies on J_{SC} of

different lateral device dimensions, the vertical device structure is expected to show significantly higher J_{SC} for all device sizes by decreasing the distance of photo-generated carriers to the contacts. In order to develop vertical devices, oxide buffer layers can be replaced by conducting buffer layers such as $NiSi_2$ and TiN [90].

CHAPTER 5 2D SIMULATION OF FLEXIBLE GAAS SC FOR LA-GB EFFECT

5.1 Introduction

Single-crystalline gallium arsenide (GaAs) compound semiconductors offer the highest energy conversion efficiency among all the photovoltaic (PV) materials [91]. However, their use in large-scale terrestrial applications has been limited due to their high manufacturing cost associated with expensive wafer substrates and their fabrication process. Thin-film polycrystalline GaAs can be adopted by avoiding the use of single-crystalline wafer process for low-cost fabrication [92]. However, the polycrystalline GaAs materials cannot deliver higher efficiencies of solar cells (SCs) than other low-cost PV materials such as poly-silicon (Si), copper indium gallium selenide (CIGS), cadmium telluride (CdTe), and perovskite structures [93]–[97]. To close the technological and economic gap of single-crystalline and polycrystalline GaAs materials, nearly-single-crystalline GaAs thin films on flexible metal substrates have been recently developed [25]. The nearly-single-crystalline (also referred to as single-crystal-like) semiconductor thin films can be directly deposited on the polycrystalline tape substrate with a biaxially textured seed layer as a crystallinity transformation layer between the semiconductor and substrate [98]. The new material platform of thin-film GaAs on metal tape has the potential to offer high conversion efficiencies (by high crystalline quality of the material), low-manufacturing cost (with roll-to-roll fabrication process on an inexpensive metal tape substrate), and application functionality (by mechanically flexible cells) in the SCs. In fact, the similar material platform was already applied in thin-film transistors to demonstrate excellent device performance

characteristics based on the single-crystal-like material [55], [80]. To deliver high-performance high-efficiency PV devices from the new material platform, required is a systematic understanding on the relationship between the characteristics of SCs and the properties of the material. Whereas the single-crystal-like materials have the superior structural quality as compared to polycrystalline materials where a number of randomly oriented crystal grains exists with high-angle grain boundaries in all the directions [92], [99], they are not completely free of crystalline defects [98]. The single-crystal-like materials contain ordered grains with low-angle boundaries aligned in one direction which is believed to be significantly less detrimental than high-angle boundaries in random directions as in polycrystalline materials.

Material and device design parameters affecting SC performance for both single- and poly-crystal GaAs materials were well defined through the experimental and modeling studies [85], [86], [92]. However, there is no theoretical study to understand SC device operation behavior based on the single-crystal-like materials. It is very critical to understand the impact of performance limiting factors such as bulk recombination within the crystalline grains, recombination at the low-angle grain boundaries, and grain size for the design of high-efficiency SCs. Unlike the most *I-V* characteristics modeling studies on polycrystalline material which consider only effective recombination rates or surface recombination velocities [100], the effects of localized traps at the boundary regions have to be considered in the single-crystal-like material.

In the present study, we develop a realistic theoretical model to investigate the performance of single-crystal-like GaAs SCs, determine and quantify the most critical factors on the device efficiency. One-dimensional (1D) and two-dimensional (2D) SC modeling are compared. In general, 1D modeling can do an excellent job in predicting the SC behavior where diode voltages and current densities are spatially uniform in every layer of the device [101]. Here, the 1D modeling also works well for the initial SC device design by employing uniform average properties of the single-crystal-like materials such as minority carriers' lifetimes, carriers' mobility, and surface recombination rates. However, the model inherently is not capable to predict the SC performance accurately, as its pre-assumptions deviate from the actual conditions of single-crystal-like GaAs SCs. The 2D modeling can be effectively used for non-uniform conditions such as carrier diffusion lengths, recombination centers and layers' sheet resistance through the device structure vertically and laterally. In this study, we focus on the effect of low-angle grain boundary (LA-GB, GB in short) regions in the materials. A 2D modeling is developed to incorporate recombination loss at localized defects of the LAGBs in the bulk of the material. The SC efficiency is calculated by estimating the effects of defect states at the GBs on short-circuit current (I_{SC}), open circuit voltage (V_{OC}), and fill factor (FF). Furthermore, the model is validated by experimental results. The effect of GB density on the SC characteristic factors is studied at different grain sizes. Finally, we investigate the effect of the passivation of the GBs on the SC performance.

5.2 Results and discussion

5.2.1 Device structure and modeling

Figure 5.1a shows a schematic structure of thin-film single-crystal-like GaAs single-junction (SJ) SC device. Unlike the conventional vertical SCs on electrically conductive substrates, the device has a lateral geometry due to the presence of electrically resistive oxide buffer layers that are employed for the crystallinity transformation between the device structure and metallic substrate. The lateral device structure results in different dynamics for charge carriers (electrons and holes). A device simulator (Sivaco Atlas) and its associated modules, were used to define the epitaxial structures and device designs. 1D and 2D modeling were performed to study the PV characteristics of the thin-film GaAs SJ-SC based on the single-crystal-like material platform. Figure 5.1b shows the two models based on minority carrier lifetimes for electrons and holes.

In the 1D modeling, uniform material characteristics and device parameters were defined due to the intrinsic limitations of model in considering material inhomogeneity and carriers transport in lateral directions. The minority carrier lifetime as the most critical factor on the SC performance was assumed to be constant throughout the SC layers which is the average carrier lifetime as a function of bulk defect densities. The carrier lifetime of τ_{avg}= 1 ns was used in the model according to an estimated value from time-resolved photoluminescence (TRPL) measurement of a biaxially textured GaAs thin film grown on a metal tape [102]. Other material parameters used in the GaAs device model are summarized in Table 4.1. A 2D modeling for lateral single-crystal-like GaAs SJ-SC was developed considering non-uniformity in the material properties. To define LA-GBs and their affected area in the material, columnar grain regions

vertical to p-n junction in the active device structure were defined. The width of the boundary and affected region was assumed to be 10 nm. Separate material properties in the GB and intra-grain regions, such as minority carrier lifetimes of GB regions (τ_{GB}) and intra-grain regions (τ_G), were incorporated in the 2D modeling (Figure 5.1b). A significantly shorter τ_{GB} (~1 ps) than τ_G (~20 ns similar to ones of single-crystal GaAs [81]) was assumed. Various grain sizes (2–50 μm) were defined in the model to study the effect of boundary density. Different doping concentrations (10^{15} to 10^{18} cm^{-3}) and carrier lifetime (1 ps to 0.1 ns) for the boundary regions were defined to investigate the passivation effect of these recombination centers.

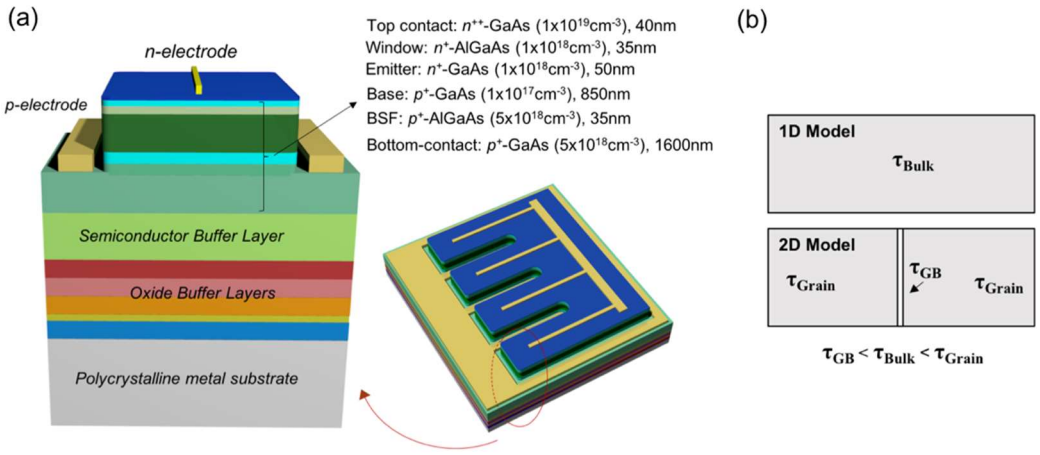


Figure 5.1 (a) Schematic structure and (b) definition of different regions in 1D and 2D models of a lateral SJ-SC using single-crystal-like thin-film (Al)GaAs materials.

In the previous chapter, we demonstrated flexible single-crystal-like thin-film GaAs SJ-SCs with promising photovoltaic characteristics. The devices with anti-reflection (AR) coating and parasitic cap layer removal showed V_{OC} of 0.57 V, short circuit current density (J_{SC}) of 19.4 mA/cm^2, resulting in conversion efficiency of 7.6% under AM1.5G

illumination 1-Sun condition. Before the AR coating and cap-layer removal, the devices showed 4.3% efficiency with V_{OC} = 0.51 V and J_{SC} = 14 mA/cm^2. The SC design was optimized based on 1D modeling using a uniform carrier lifetime of τ_{avg}= 1 ns, which predicted maximum efficiency of ~ 21% as shown in Table 5.1. This efficiency gap between experiment and 1D-simulation result mostly originates from significantly lower V_{OC} of the fabricated devices than the estimated V_{OC} ~ 0.96 V. The effect of localized defects cannot be reflected accurately on the 1D-simulated *I-V* characteristics especially where lateral device geometry imposes lateral transfer of carriers. The capability of taking GB effect into account is the key to obtain accurate simulation results of the single-crystal-like GaAs SC [101].

Table 5.1 J-V results from the 1D modeling of single-crystal-like GaAs SC with 2-μm grain size.

Average Carrier Lifetime (ns)	***Voc* (V)**	***Jsc* (mA/cm^2)**	**Fill Factor (%)**	**Efficiency (%)**
1	0.96	26.7	85.6	21.9
0.1	0.89	26	81	18.7
0.01	0.81	23.4	71	13.4
Experiment	0.51	14	60	4.3

5.2.2 2D modeling and comparison to experimental result of device

The 2D model is developed to quantify the performance of single-crystal-like GaAs thin film SCs more accurately. The same optimized device structure, *i.e.*, the same layers' thickness and doping concentrations in 1D model, is used for the 2D model. Figure 5.2 shows a *J-V* characteristic of the simulated single-crystal-like GaAs SC employing the 2D model. Lateral size of the columnar grain was assumed to be ~2 μm between GBs, representing actual grain size of the material. The average grain size of

typical single-crystal-like GaAs thin film on metal tape is 2 μm as estimated by scanning-electron microscopy. The 2D model predicts the efficiency of 4.8% with V_{OC} = 0.57 V, J_{SC} = 14.3 mA/cm^2, and FF = 0.59, which are close to experimental characteristics of the fabricated SC devices, *e.g.*, V_{OC} = 0.51 V, J_{SC} = 14 mA/cm^2, and FF = 0.6, resulting in the conversion efficiency of 4.3%, as summarized in Table 5.2.

The simulated *J-V* curve is very well-matched with the experimental *J-V* curve in all the parameters, confirming the validity of the 2D model including the critical role of GBs in the device performance degradation. The GBs even with low-angle misorientations can limit the carrier collection efficiency by providing recombination center (lower J_{SC}) and shunting paths (lower V_{OC}).

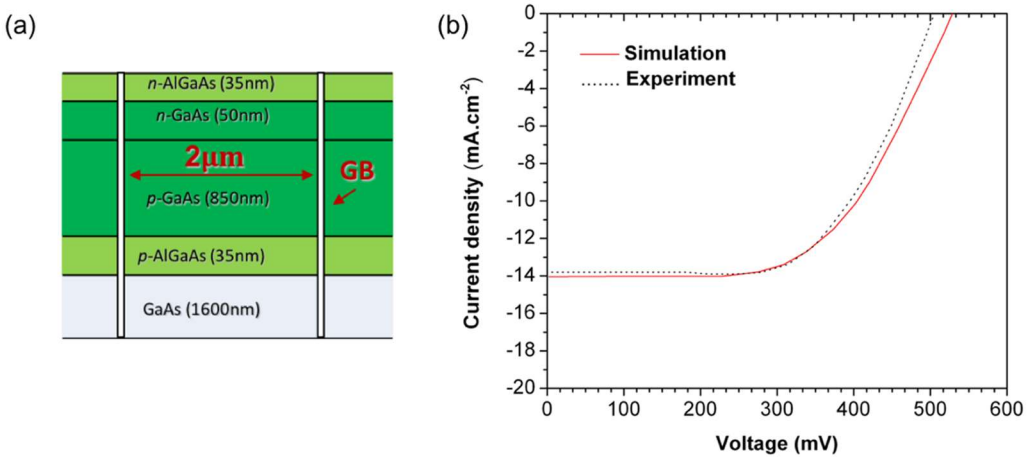


Figure 5.2 (a) Schematic structure of SC device in the presence of GB regions used in 2D modeling and (b) simulated (red line) and experimental (black dotted line) J-V characteristics of flexible GaAs SJ-SC on a metal substrate.

Table 5.2 J-V characteristics of simulated and fabricated single-crystal-like GaAs SC.

SC Device with GBs	*Voc* (mV)	*Jsc* (mA/cm^2)	Fill Factor (%)	Efficiency (%)
Simulated SC -2D model	0.57	14.3	59.4	4.8
Fabricated SC	0.51	14	60	4.3

5.2.3 Grain size effect on I-V characterization of SCs

In order to mitigate the detrimental effect of LA-GB regions on the single-crystal-like GaAs SC performance, the grain boundary density should be reduced through increasing grain size [103]. The effect of 2D density on the SC characteristics of single-crystal-like GaAs is analyzed by the 2D model. Various distances between vertical GB regions are defined to simulate the single-crystal-like GaAs material with different grain sizes. Figure 5.3 shows the effect of grain size on the three characteristic parameters V_{OC}, *FF*, and J_{SC} and overall efficiency of the simulated SC. All *I-V* characteristics of SC are affected by grain size and improved significantly with increasing grain size from 2 µm to 50 µm. However, the V_{OC} and J_{SC} show different improvement trends (Figure 5.3a and b). The J_{SC} shows its major improvement at the initial stage of grain size increase from 2 µm to 15 µm. Conversely, the V_{OC} does not show significant change with grain size increase up to 15 µm. The J_{SC} of SCs reaches to a saturation level ~93% of its maximum value at a grain size of 15 µm. The V_{OC} is improved continuously up to 50-µm grain size; however, it is still 0.3 V less than V_{OC} for the case of the absence of the GBs (red star in Figure 5.3a). The grain size has less effect on J_{SC} than V_{OC} in single-crystal-like GaAs SCs. The most carriers are generated within the shallow region from the surface and the photogenerated carriers can overcome short minority-carrier diffusion length even with decreasing grain size [85].

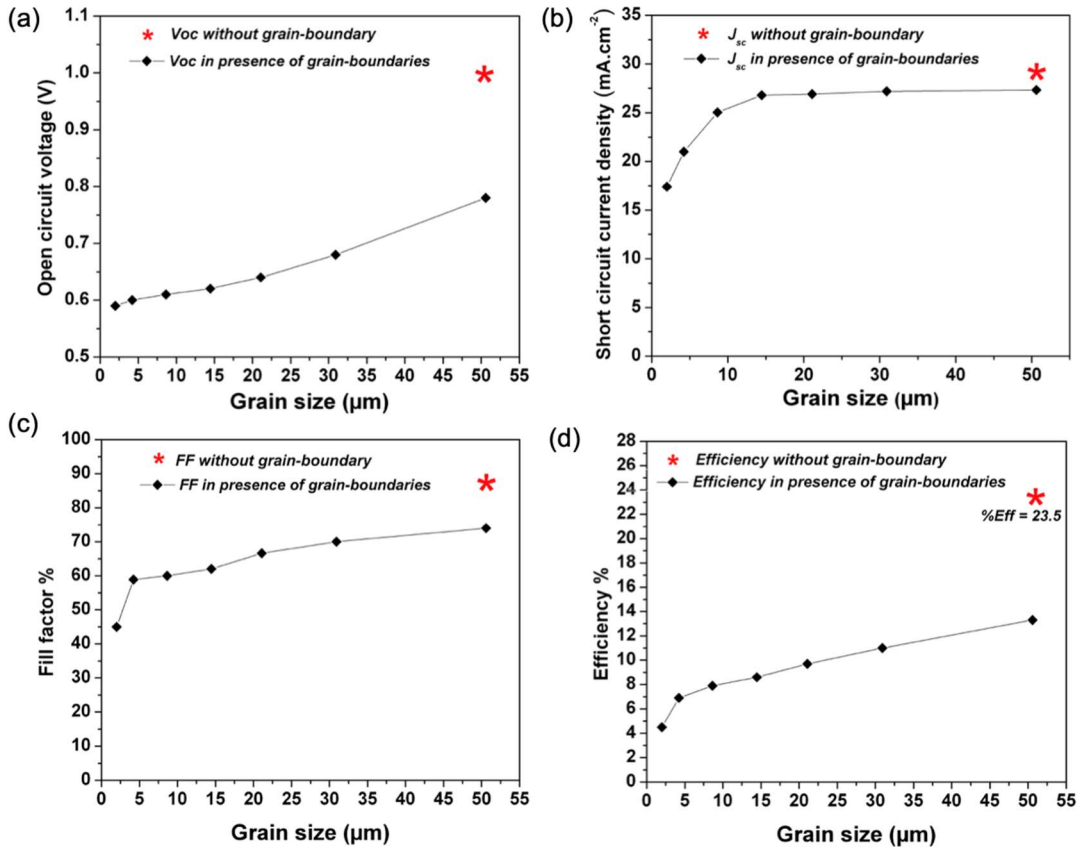


Figure 5.3 I-V characteristic factors of the simulated single-crystal-like GaAs SJ-SC vs. grain size: (a) VOC, (b) FF, (c) JSC, and (d) conversion efficiency. Red star shows an estimated value for the case in the absence of GBs in each factor.

Figure 5.4 shows dark *I-V* characteristics of simulated single-crystal-like GaAs SC with various grain size. The dark saturation current is reduced from $J_0 \sim 2\times10^{-4}$ A/cm^2 (at $V = -0.5$ V) to $J_0 \sim 4.8\times10^{-6}$ A/cm^2 by increasing the grain size from 2 μm to 50 μm. The V_{OC} of simulated SC devices increases from an initial value of ~0.5 V for 2-μm grain size to ~0.8 V after increasing grain size to 50 μm, which is concurrent with reduction in the diode dark saturation current density. In a parallel direction to the GBs,

the defects states at the GBs causes shunt paths and leakage current which is reflected in higher dark saturation current for single-crystal-like GaAs SCs with smaller grain size [99], [104]. The higher J_0 originating from higher carrier recombination centers at the GBs limits the V_{OC} of SCs.

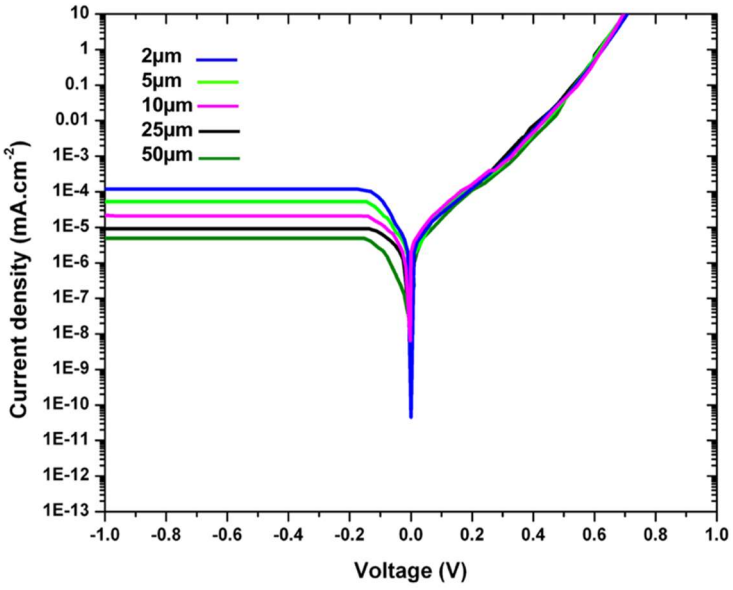


Figure 5.4 Dark J-V curves of simulated single-crystal-like GaAs SJ-SC at different grain sizes.

5.2.4 Recombination rates and current vectors in 2D device structure

Figure 5.5 shows recombination rates and current vectors in the cross-section of the SC structure with GBs. The SC device characteristics in the presence of GBs can be described by considering two cases of current flow parallel and perpendicular to the GBs. In conventional SC modeling, it is usually assumed that the grain structure is columnar with the GB plane normal to the junction and, hence, the case of current flow parallel to the boundaries is of interest [99]. Under these conditions, the value of I_{SC}

remains relatively high closer to that of single-crystal devices while V_{OC} decreases significantly. For the single-crystal-like GaAs SC with lateral device geometry, both parallel and perpendicular current flow to the GBs play roles in the *I-V* characteristics. Figure 5.5 shows high recombination rate around the GBs by Shockley-Reed-Hall (trap-assisted) recombination resulting current direction disturbance near the GBs. This deviation of current vectors toward the GBs is visualized. Figure 5.5 also shows majority carrier transport perpendicular to the GBs in *n*- and *p*-contact layers which encounters high resistance at a potential barrier from energy band bending at the grain boundaries which can increase series resistance and, therefore, reduce the J_{SC} and FF.

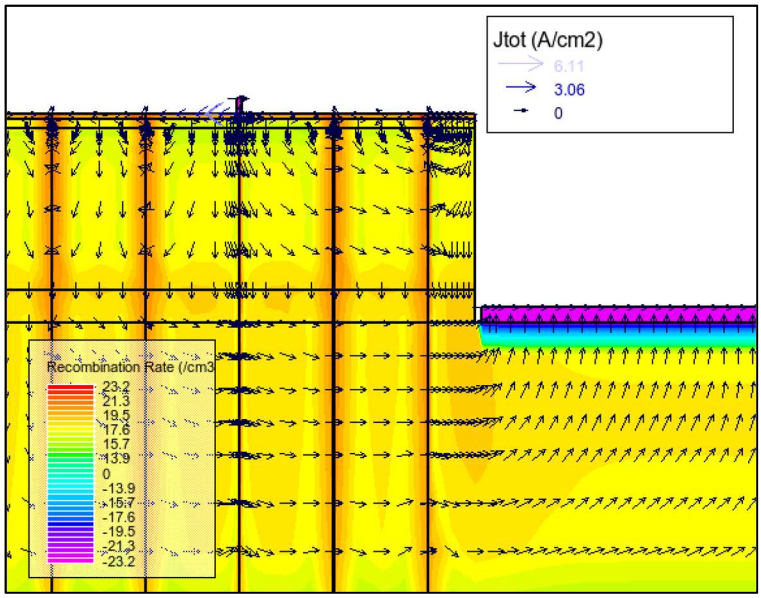


Figure 5.5 Recombination rates and current vectors in the cross-section structure of single-crystal-like SC.

5.2.5 Ideality factor of single-crystal-like GaAs SC

The ideality factor of 2D simulated SC versus applied forward bias was extracted from semi-log plot of dark *J-V* characteristics (figure not shown). They show the values

in the range of 2–4. Ideality factor, known as n-factor, is an indication of p-n junction quality and recombination type in a SC. For simple recombination mechanisms where all the recombination occurs via band to band, the ideality factor has a value of 1 at the ideal diode region of dark *I-V*. Here, ideal diode region is not observed for any bias region of *I-V*. Higher n-factor than 1 for all bias voltages is related to the presence of defect recombination centers in the depletion region and through all device structure with a combination of different recombination types. When the recombination is dominated by extended crystal defects, like dislocations or grain boundaries in SCs, the dark characteristics shows an ideality factor larger than unity over a wide forward bias range. High n-factor not only degrades SC FF, but also results in lower V_{OC}, as it signals high recombination.

5.2.6 Bulk grain boundary passivation

Theoretically, a GB induces localized energy states near the middle of the forbidden band gap. For p-type semiconductors, the Fermi energy level (E_F) is below the localized state which is empty and inoperative. For n-type semiconductors the E_F is above the localized state which is filled. The grain boundary is then an acceptor region and for adjacent grains an electron depletion occurs; eventually a p-type slice can appear at the grain boundary. This charge carrier redistribution induces an electrostatic energy which is responsible for a bending of the energy bands near the GBs [104]. Here, depending on the doping type of (Al)GaAs layers in the SC device structure, defects caused by incomplete atomic bonding and disordered material in the grain boundaries are also expected to result in trapping states inside the (Al)GaAs bandgaps causing

upward/downward energy band bending at the GBs (Fig. 51a). This band bending at GB causes significant local change in the doping level of layers and create space-charge regions in the crystallites and a potential barrier that impedes carrier motion. This band bending phenomenon at the GBs has been reflected in the 2D modeling by defining lower doping concentration for two-order of magnitude at the GB interface regions of layers compared to that of the intra-grains. Fig. 51b and c show energy band diagram at a horizontal cutline, perpendicular to the GBs, in the *p*-base layer of simulated GaAs SC which shows downward band bending at GBs of the layer. In this condition, minority electron carriers in the p-GaAs layer can be captured in the valleys of conduction band in the GB regions where carrier lifetime is only 1 ps and they can be recombined with holes easily. Increasing the doping concentration of GBs up to doping level inside the grains of p-GaAs base layer (10^{17} cm^{-3}) makes band diagram flat so that minority electrons carriers can move more freely (Figure 5.6d).

Preferential diffusion of various gases down to the GB in the polycrystalline materials, known as passivation process, is shown to promote significant reduction in both the density of defect states and the accompanying GB potential barrier and improve their device performance [105]. Various bulk passivation methods for deactivating dangling bonds and reducing carriers' recombination centers at large-angle grain boundaries' interfaces of poly-crystalline materials have been studied. Here, bulk passivation of LA-GBs in the single-crystal-like GaAs SC device structure is also studied by employing the 2D modeling as a potential boost method for PV performance of this material. Here, the effect of grain boundary passivation on the single-crystal-like

GaAs SC characteristics is studied by the 2D modeling. Figure 5.6e shows *J-V* characteristic of simulated single-crystal-like GaAs SC with grain size of 2 μm and carrier lifetime of 1 ps at GB regions (black curve). Increasing the doping concentrations at GBs of each device layer up to its intra-grain's doping level shows that the efficiency of SC can increase almost double (pink curve in Figure 5.6e) due to removing GB potential barrier. If this is combined with higher carrier lifetime at GBs from 1 ps to 0.1 ns (These two phenomena happen concurrently in reality by passivating GBs), efficiency of ~19.7% can be achieved (blue curve in Figure 5.6e and Table 5.3) even for the SCs with very small grain size of 2 μm showing that effective passivation of GB regions could be a critical solution to boost efficiency of single crystal-like thin film GaAs SC. Dark *I-V* characteristics of SCs also shows dark saturation current density reduction from J_0 ~1.3×10^{-5} A/cm^2 (at V = -1 V) to J_0 ~2.9×10^{-6} A/cm^2 by passivating the LA-GBs (Figure 5.7a), which results in V_{OC} improvement from 0.57 V to 0.9 V for single-crystal-like GaAs . Figure 52b also shows improvement in the internal quantum efficiency (IQE) of single-crystal-like GaAs SC after passivating the LA-GB regions.

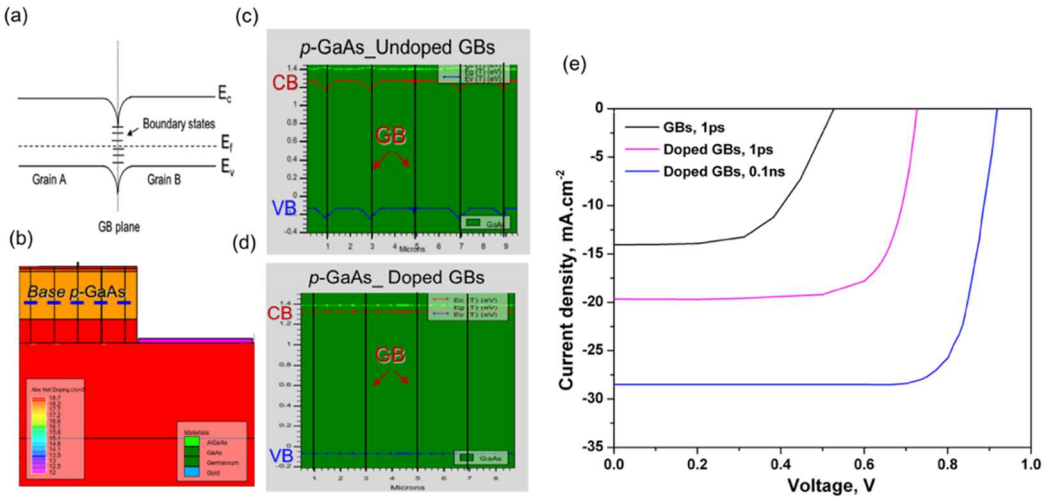


Figure 5.6 (a) A schematic illustration of band bending induced by dangling bonds at a grain boundary (b) cross section image of simulated thin film GaAs SC device structure with layers' doping concentration (c) energy band diagram of p-GaAs layer of the device for GBs doping level of $1\times15cm^{-3}$ and (d) $1\times17cm^{-3}$ (f) I-V characteristics

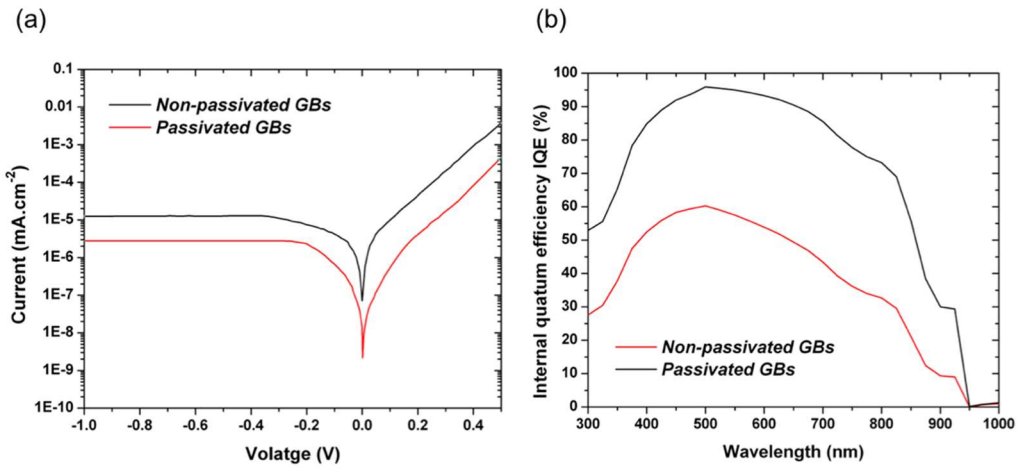


Figure 5.7 (a) Dark I-V and (b) IQE plots of passivated and non-passivated single-crystal-like GaAs SCs with 2-µm grain size.

Table 5.3 Simulated J-V characteristics of single-crystal-like GaAs SC with the effects of GB passivation.

GB carrier lifetime	*Voc* (mV)	*Jsc* (mA/cm^2)	Fill Factor (%)	Efficiency (%)
Unpassivated GB, τ_{GB} = 1 ps	0.57	14.3	59.4	4.8
Doped GB, τ_{GB} = 1 ps	0.73	19.8	74	10.7
Doped GB, τ_{GB} = 0.1 ns	0.9	27	81	19.5

5.3 Conclusion

A numerical device physics model for newly developed single-crystal-like GaAs thin-film solar cells (SCs) enables us to understand effects of key material quality parameters on device performance. We have developed a physical 2D model which can predict single-crystal-like GaAs SC performance with high accuracy whereas conventional 1D model cannot simulate these SCs accurately. By using 2D model instead of 1D, we avoid the need to employ simplifying assumptions such as quasi-neutrality or an effective carrier diffusion length and lifetime.

Our 2D model predictions are supported by experimental results of fabricated flexible single-crystal-like GaAs SCs. The 2D model suggests that low-angle grain boundaries (LA-GBs) are the main recombination centers in the single-crystal-like GaAs material. The *I-V* characteristics of SCs can improve significantly by increasing grain size from 2μm to 50μm. The V_{OC} of devices is more sensitive to GB densities than other performance parameters and it has still much room to be improved even in the presence of large grain size of ~50 μm. The simulation study on the passivating of dangling bonds at GB regions showed a significant boost for SC characteristics especially V_{OC} which improves the efficiency of devices from 4.8% to ~19.7% for

material with relatively small grain size of 2 μm. According to this study, single-crystal-like materials with relatively large grain size and passivated GBs' interfaces can provide us with high device performance comparable to wafer-based materials.

Although the modeling focuses on the understanding of the single-crystal-like GaAs material for SC applications, the results also provide insights applicable to other biaxially textured materials grown on non-native templates for various solid-state devices.

CHAPTER 6 SULFIDE PASSIVATION TREATMENT OF GAAS SC

6.1 Introduction

Gallium arsenide (GaAs) semiconductor has the most favorable bandgap energy than other solar cell (SC) materials for efficient absorption of solar spectrum and offers the highest photo-conversion efficiency combined with the advantages of high radiation resistance and low temperature coefficient. Furthermore, the GaAs-based materials with similar lattice constants and different bandgap energy can be stacked to realize multi-junction tandem SCs with conversion efficiencies higher than 45% [41]. However, such high efficiency can only be achieved from single-crystalline materials epitaxially grown on very expensive Ge or GaAs wafer substrates. Therefore, the use of their SC modules has been limited only in selected performance-sensitive applications, primarily in space technologies. In order to make the GaAs photovoltaic (PV) technology viable for commercial terrestrial market, the costs of manufacturing and materials are required to be significantly reduced [106]–[109].

We have recently developed single-crystal-like GaAs thin films on cheap metal tape [98], [102] using a roll-to-roll continuous deposition process to deliver a cost-effective PVSC technology, which has the potential to offer comparable performance with single-crystal GaAs grown on wafers. Furthermore, the material offers additional functionality and extended applications due to its mechanical bendability. We predicted photovoltaic conversion efficiencies of the single-crystal-like GaAs solar cell on the basis of a numerical 2D model that solved carrier continuity and Poisson equations for the lateral device geometry [110]. The model was also used to estimate the effect of low-angle

grain boundary (LA-GB) density on the SC device performance of single-crystal-like GaAs and further modified for a grain boundary passivation effect study on the cell efficiency. The details of the 2D model are available [110]. Under AM1.5G illumination, the model indicates SC efficiencies of 4.8% to 12.3% for the un-passivated LA-GBs in the GaAs with grain size of 2μm to 50μm. The first solar cell demonstration of single-crystal-like thin-film GaAs showed well-matched IV characteristics with the model prediction. Upon passivation, the model predicts almost a factor of four improvement in efficiency from 4.8 to ~19.5% for the GaAs with grain size of 2μm, assuming negligible trap states and recombination rate at the GB regions [110].

A wide variety of chemical- and physical-based passivation techniques have been reported to reduce surface/bulk defects of poly-crystalline material including Si [111]–[113], GaAs [114], [115], CIGS materials [116], [117], and CdTe [118]. In this work, various passivation treatment techniques were employed on the single-crystal-like GaAs SC fabricated with the same layers structure, doping concentrations and device geometry as used in the model.

Preferential diffusion of various gases down the grain boundaries of polycrystalline materials has been widely used to reduce density of defect states in these GB regions. Several gas/plasma based passivation techniques including hydrogen [119], oxygen [120], helium [121], and SF_6 [122], [123] plasma exposure and D_2, H_2 high pressure annealing (HPA) treatments [124], [125] have been employed. Hydrogen in the form of monatomic hydrogen plasma was reported as the most effective gas in reduction of these energy states in poly-Si [(15)]. SF6 plasma treatment was reported to be effective in

passivation of GaAs surface by forming Ga-F and removing the oxide traps and As-As dimers effectively [123].

The simplest method for passivating GaAs is dipping treatment in reactive S-containing solutions. Among chemical passivation treatments, aqueous sulfide treatment is well-known for efficient passivation of GaAs surface by reducing the density of state [127], [128]. A number of sources of sulfur compounds including ammonium sulfide [88], sodium sulfide [129], sulfur monochloride [127], phosphorus pentasulfide/ammonium hydroxide [130], and selenium sulfide [131] are known to impart a greater or lesser degree of passivity on GaAs surface. The compounds with sulfur in the -2 oxidation state, provide the most efficient chemical passivation for GaAs [132]. According to previous studies, Na_2S aqueous solution works the best for GaAs passivation, however it vigorously etches GaAs and is corrosive to put in contact with a fabricated solar cell [133], [134] Therefore, in this study we employ Trioctylphosphine sulfide (TOP:S, $SP(C_8H_{17})_3$) which is a long chain surfactant molecule commonly used for passivation of colloidal semiconductor nanocrystals [135] and was recently identified by Atwater et. al to enhance photoluminescence of GaAs crystal (011) plane and mitigate efficiency losses in induced fractures of GaAs cells [132].

Here, we study the effect of three different physical passivation techniques of proton implantation, atomic hydrogen injection by electric field, high-pressure deuterium annealing, and the chemical TOP:S passivation treatment on the single-crystal-like GaAs films and SCs in order to find out the most practical and efficient technique in

passivating LA-GBs and thus improving the overall photo-conversion efficiency of cells.

6.2 Material growth and device layers structure

The growth techniques and conditions of biaxially textured buffer materials on metal tape as a template for the epitaxial growth of Ge and GaAs, followed by *p-n* junction device structure layers were described in detail in the chapter 3 and 4 and previous report [102]. The SC active region (Figure 4.2) consists of (in a sequence of epitaxial growth) a unintentionally-doped GaAs layer (~2 μm), a heavily zinc-doped *p*-type GaAs contact layer (p^{++}-GaAs:Zn, $p = 5\times10^{18}cm^{-3}$, ~1.6μm), a p^{+}-$Al_{0.4}Ga_{0.6}As$:Zn back-surface field (BSF) layer ($p = 5\times10^{18}cm^{-3}$, ~32nm), a *p*-GaAs:Zn base layer ($p = 1\times10^{17}cm^{-3}$, ~853nm), an n^{+}-GaAs:Si emitter layer ($n = 1\times10^{18}cm^{-3}$, ~53nm), an n^{++}- $Al_{0.4}Ga_{0.6}As$ window layer ($n = 1\times10^{18}cm^{-3}$, ~35nm), and an n^{++}- GaAs:Si contact layer ($n = 1\times10^{19}cm^{-3}$, ~40nm).

Device fabrication: Figure 6.1 shows the steps of device fabrication. The fabrication of SC devices began with the formation of a mesa to access the bottom contact layer using an etchant mixture of citric acid and hydrogen peroxide ($CH_3COOH + H_2O_2$). The dimension of the mesa is 400 μm × 400 μm (0.0016 cm^2). Patterned ohmic-contact electrodes of Ni/Ge/Au and Cr/Au were applied on the n^{++}-GaAs:Si and p^{++}-GaAs:Zn contact layers, respectively, using electron-beam (E-beam) evaporation followed by a photoresist lift-off process. Then, n^{++}-GaAs cap layer was selectively (to the AlGaAs window layer) etched in $H_3PO_4/H_2O_2/H_2O$ = 4:1:90 etchant for 30 seconds. The

fabricated devices were treated for the passivation of the grain boundaries using various techniques, as described in the next section. Next, a dual-layer anti-reflection coating (ARC) of ZnS/MgF_2 (48/80 nm) was deposited by E-beam evaporation.

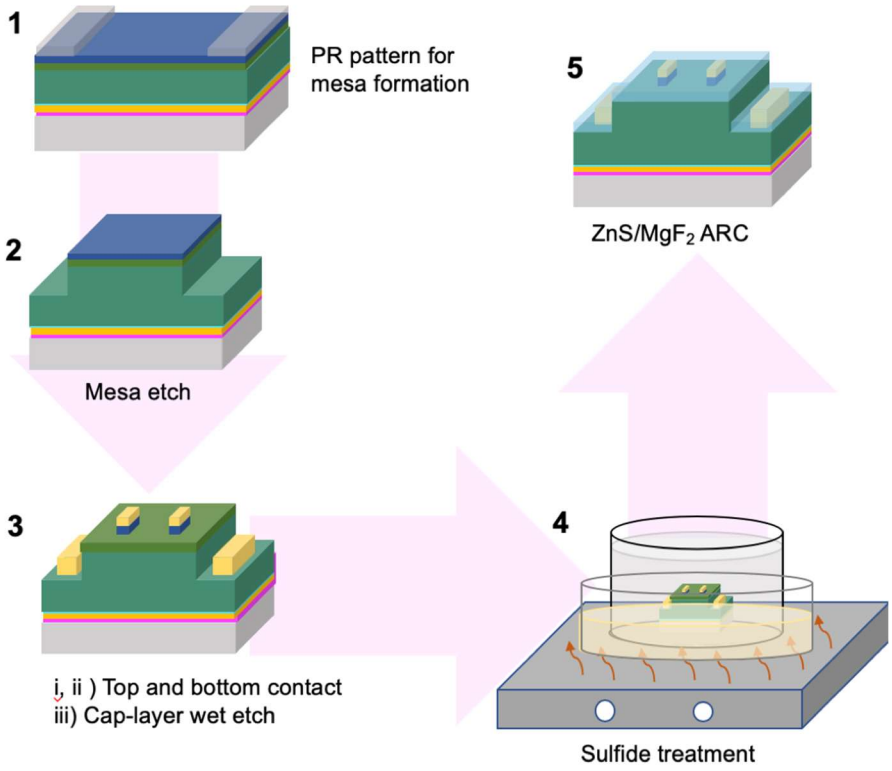


Figure 6.1 Device fabrication and passivation process steps.

Grain boundary passivation; approach (1): Proton implantation was performed using H^+ ions at 3 different energies and doses; *approach (2):* high-pressure deuterium (D_2) annealing was performed in a furnace purged with D_2 gas at a pressure of 30 atm and a temperature of 400 °C for 30 minutes; *approach (3):* deep reactive ion etcher (Oxford, Plasma Lab ICP 180 RIE) was used for the injection of hydrogen ions to the

GaAs films and SCs. Several process conditions including hydrogen (H_2) flow, pressure, RF power, DC bias, ICP power, temperature, and time were explored for optimum conditions of hydrogen plasma treatment; *approach (4):* the TOP:S solution was synthesized in a glovebox filled with argon (Ar), as the solution solidifies with an exposure to air, by combining equimolar amounts of sulfur powder (Aldrich, Lot #11325) and Trioctylphosphine (97%, Aldrich, Lot #16496APV) and stirring while applying gentle heat (60 °C) for 12 hours until the liquid is clear. The TOP:S is an inert, transparent, and insulating viscous liquid with sulfur in its −2 oxidation state. The single-crystal-like GaAs film and fabricated SC device samples (without ARC) were soaked in the pure TOP:S aqueous solution while stirring at ~60 °C, followed by rinsing with anhydrous toluene (Honeywell, Lot #DB853) to remove all the TOP:S but chemically bonded As-S and Ga-S [127] on the surface and grain boundaries prior to the measurement and characterizations.

Device and film characterization: The optical photoluminescence (PL) characterization of the GaAs films was conducted below 20 K using Cryogen Free 10 K systems. The PL spectra were measured by HORIBA scientific iHR320 imaging spectrometer equipped with a Synapse CCD and a filter of 364 nm long pass. A COHERENT Innova 302C 351 nm laser (Type: Krypton) was used for excitation.

Current vs voltage (*I–V*) characteristics of the flexible single-crystal-like GaAs SCs was measured under AM1.5G illumination 1-Sun condition with 0.1 W/cm^2 power density using a solar simulator (Newport, Oriel Sol3A). A calibrated power meter and

an NREL-calibrated solar cell (model 91150V) were used to measure the incident flux light of the solar simulator.

Scanning Kelvin probe microscopy (SKPM) measurements on the GaAs surface were carried out in an atomic force microcopy (AFM) system using electrically conductive Pt-coated cantilevers with OPUS shape tip (MikroMasch, OSCM-PT). The technique relies on an AC bias applied to the tip to produce an electric force on the cantilever that is proportional to the potential difference between the tip and the sample. Topography images were acquired using the frequency modulation technique at the fundamental resonance frequency of the cantilever ~ 70 kHz. Amplitude modulation (AM) KPFM was used for the detection of the contact potential difference (CPD) with an applied bias V_{AC} = 300 mV tuned to the second resonance frequency of the cantilever (f_2 ~ 1.035 MHz). The CPD is the work function (Φ) difference between sample and tip: CPD = $\Phi_{sample} - \Phi_{tip}$. Reference measurements on a cleaved surface of highly oriented pyrolytic graphite (HOPG) were used to calibrate the work function of the tip (Φ_{tip}) and to ensure comparability of the obtained CPD values.

6.3 Results and discussion

In a previous study [102], our first PVSC demonstration of single-crystal-like thin-film GaAs showed promising photovoltaic characteristics with a conversion efficiency of 7.6% under AM1.5G illumination 1-Sun condition. Later, the 2D numerical modeling study [110] on the effect of low-angle grain boundaries (LA-GBs) in the materials on the *I−V* characteristics of single-crystal-like GaAs SC showed that even in the case of highly-textured material with narrow grain boundaries of ~2nm width, carrier traps in

the GB regions are the major non-radiative recombination centers limiting SC performance. Therefore, there are much more rooms for the improvement of the SC performance either by increasing grain size (reducing GB density) or employing an effective technique for passivation of GBs energy states. In this study, we focus on the passivation of GBs for higher device efficiency.

6.3.1 Characteristics after hydrogen treatment

Three passivation techniques of proton implantation, hydrogen plasma, and high-pressure deuterium anneal were employed to passivate the detrimental effect of the grain boundaries in the single-crystal-like GaAs. All the techniques resulted in a certain degree of improvement in selected characteristics of SC performance; however, they also simultaneously caused drawbacks or side-effects that limit the improvement of overall SC conversion efficiency.

Using a proton-implantation technique, deep levels generated by the grain boundaries can be passivated by precisely controlled protons injected over the target depth with optimum concentrations. However, it induces damages to GaAs lattice structure by high energy of protons, which needs high-temperature annealing (~950 °C) for the recovery of the lattice structure.

High-pressure D_2 annealing was employed which could be used on fabricated devices with no damage to metal contact electrodes, material lattice structure, and morphology. One order of magnitude reduction in the leakage current and consequently 50% increase in overall efficiency of low-performance devices with Voc < 200 mV

were observed. However, no significant improvement for higher efficiency devices due to insufficient molecular D_2 injection depth was obtained [124], [125].

Atomic hydrogen passivation by electric field on the GaAs film and SC device has been applied. Using this technique, negligible crystallinity change was confirmed by XRD compared to the proton implantation-induced damage and a deeper monoatomic hydrogen injection into the bulk was expected in comparison with molecular deuterium by HP D_2 annealing [125]. However, several hundred nanometers GaAs was etched by hydrogen plasma.

Both hydrogen ion implantation and hydrogen plasma injection techniques have improved the Voc of SCs significantly by incorporating hydrogen into depth of bulk but the overall efficiency didn't increase much as the Jsc dropped by increase of series resistance possibly due to deactivation of device layers' dopants by reaction to hydrogen and induced damage by high energy ion impact. Thermal shock (Rapid thermal annealing at 950°C for 20s in N2 ambient) for recovery of the material crystallinity and decrease of series resistance has been applied on the hydrogenated devices [136], [137]. While Jsc was recovered after the annealing process, Voc came back to about its original amount as the diffused-in hydrogen might not be quite tightly bound to the GaAs lattice and could scape in high temperature annealing process [126].

6.3.2 I−V characteristics after TOP:S treatment

The effect of sulfide treatment by TOP:S solution was assessed on the SC using light and dark *I−V* characteristics. Figure 6.2 shows the illuminated *I–V* characteristics of the

as-fabricated and TOP:S treated single-crystal-like GaAs SC devices. The fabricated SC before the passivation exhibits V_{OC} = 552 mV, J_{SC} = 18 mA·cm^{-2}, and fill factor (FF) = 0.61, resulting in η = 6.1% (Table 6.1). After employing the TOP:S treatment, its efficiency increases ~64% by the improvement of all the performance parameters (Table 6.2). The TOP:S-treated SC showes V_{OC} = 695 mV, J_{SC} =20.3 mA·cm^{-2}, FF = 0.71, resulting in η = 10%. The improvement in the performance upon passivation reported in the present work is likely attributable to the decrease of grain boundaries trap states. The same TOP:S treatment was also conducted on a reference wafer-base GaAs SC. A negligible change in the I–V characteristics of TOP:S treated wafer SC was observed which suggests that the most of performance improvement for single-crystal-like GaAs SC originates from the passivation of GBs, not device surface/sidewall passivation.

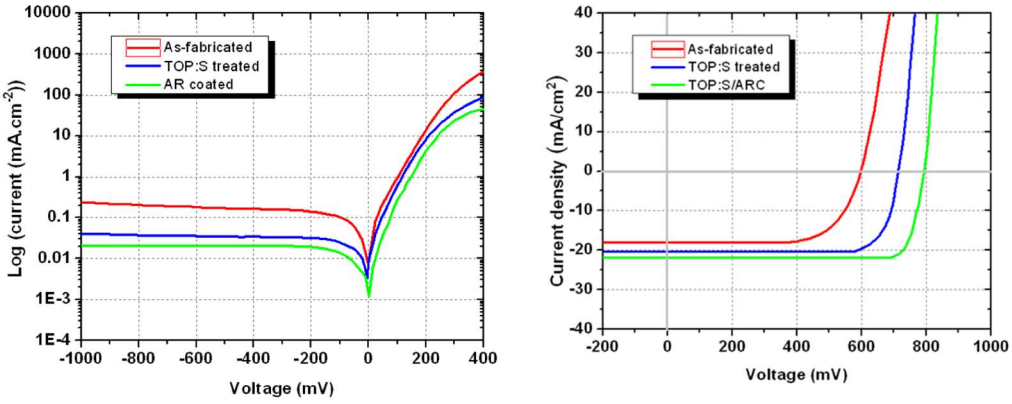


Figure 6.2 a Dark and b Sun J-V characteristics of single-crystal-like GaAs SJ SC device after different steps of device fabrication and post processing

Table 6.1 J-V characteristics of single-crystal-like GaAs SC in as-fabricated, TOP:S treated and AR coated process steps

GB carrier lifetime	*Voc* (mV)	*Jsc* (mA/cm^2)	Fill Factor (%)	Efficiency (%)
as-fabricated	590	18	62	6.1
TOP:S treated	730	20.3	71	10
TOP:S treated/AR coated	786	22	77	13.3

Table 6.2 Increase of VOC, JSC, FF, η of single-crystal-like GaAs solar cell by TOP:S treatment

Device parameter	TOP:S treated SC
ΔVoc (mV)	140 (23.7%)
ΔJsc (mA.cm^{-2})	2.3 (12.8%)
ΔFF (%)	9 (14.5%)
Δη (%)	3.9 (64%)

The most critical advantage of this chemical-base treatment in comparison to the other three physical-base treatment techniques employed on the SC is that the Jsc of TOP:S treated cells not only does not drop but also increases as well as other cell parameters which results in an overall SC efficiency improvement. The reflection percent of bare GaAs film compared to a toluene rinsed TOP:S treated GaAs film showed no difference in the surface reflection of films. Considering the refractive index of toluene (n~1.5) higher than that of air (n~1) and lower than that of GaAs (n~4), this experiment was conducted to confirm that there is no toluene residue anti-reflection effect cooperated in the Jsc improvement of TOP:S treated SCs. While a significant improvement in efficiency upon passivation of single-crystal-like GaAs SC was achieved, it is less than the efficiency predicted by the model, is probably caused by incomplete passivation of the deep level GB states. The IV characteristic improvement for TOP:S treated SCs is very similar to the simulated result where minority carriers' lifetime of 1ps at the

partially passivated GBs is considered. Further studies are under way in efforts to optimize current passivation method and try out other methods for the best passivation approach for single-crystal-like GaAs. Another recognizable improvement in the SC IV characteristics was achieved by deposition of anti-reflection coating of ZnS/MgF_2 on the TOP:S treated devices (Figure 6.2). The V_{OC}, J_{SC} and FF of 786 mV, 22mA·cm^{-2}, and 0.77 were achieved after ARC, respectively and resulted in the overall efficiency of 13.3% (Table 6.1) which is about 1.8 times higher than our previous record on the single-crystal-like GaAs SCs of 7.6% [102].

Dark *I–V* curves (Figure 6.2a) show a reduction in dark saturation current J_o after TOP:S treatment and ARC. Dark I-V characteristics of the as-fabricated flexible GaAs SC shows dark saturation current of J_o ~2×10^{-3} A/cm^2 (at V = -500mV). The J_o decreased to ~3.5×10^{-4} A/cm^2 after soaking the SC in TOP:S solution. About one order of magnitude reduction in the dark saturation current after TOP:S treatment could be related to effective passivation of dangling bonds at the GBs regions resulting in lower carrier recombination centers in the single-crystal-like GaAs. The minimized leakage current in dark condition is reflected in higher V_{OC} and FF for SCs under light (Figure 6.2b). A slight decrease in the dark leakage current (J_o ~2×10^{-4}A/cm^2) is also observed after depositing anti-reflection coating, possibly due to top and sidewall passivation of lateral SC (Figure 6.2a).

6.3.3 Photoluminescence characterization after TOP:S treatment

Photoluminescence (PL) spectroscopy as a nondestructive method of probing materials is a powerful characterization technique for determining material bandgap,

impurity and defects, recombination mechanisms, material quality and crystallinity. PL measurements were performed to probe any change in non-radiative recombination due to treatment by TOP:S. The PL yields from single-crystal-like Zn-doped p-GaAs and Si-doped n-GaAs flexible sample before and after TOP:S treatment is displayed in Figure 6.3. The PL indicates that TOP:S improves the electronic quality of both Zn- and Si-doped GaAs films regardless of its dopant type. The relative enhancement of the PL by 125% after soaking in pure TOP:S solution (Figure 6.3a) indicates a significant decrease in non-radiative carrier recombination in the treated sample. This enhancement of the band-edge luminescence is an evidence of effective passivation of single-crystal-like GaAs by TOP:S, and it is consistent with TOP:S treatment effect on cleaved (011) facet of GaAs wafer [132] and comparable to increases observed for aqueous solution treatments of Na_2S and N_2H_2 as the best-performing treatments previously reported [132], [133], [138], [139].

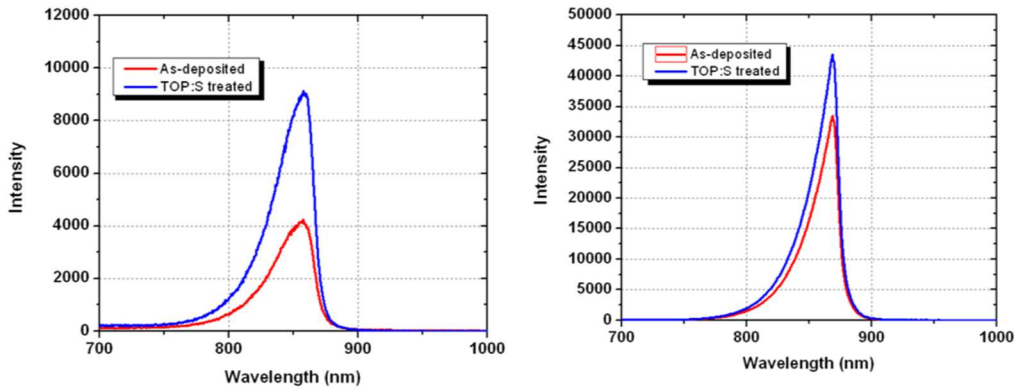


Figure 6.3 PL intensity for as-grown (baseline) GaAs films, and TOP:S treated film (a) p-GaAs and (b) n-GaAs.

6.3.4 Surface potential by SKPM

Scanning kelvin probe microscopy was used to study the effect of chemical TOP:S treatment on the GBs of single-crystal-like GaAs film. Figure 6.4c and d exhibit the surface potential map images of as-grown and TOP:S treated single-crystal-like GaAs films, obtained with morphology simultaneously. The identification of GBs was possible from the surface morphology (topology image Figure 6.4a) of the as-grown single-crystal-like GaAs sample. The CPD profile across GBs was then extracted from the simultaneously acquired CPD map, as illustrated in Figure 6.4c. The CPD variation across the six marked GBs (ΔCPDGB) of as-grown GaAs film is then determined from individual line profiles (see Figure 6.6a).

A potential peak (ΔCPDGB ~ from 30 to120mv) across each of six GBs (Figure 6.6a) is pronounced for the as-grown sample. Whereas, using line profile analysis on the potential map of TOP:S treated film shows a relatively uniform CPD across the whole area (Figure 6.6a).

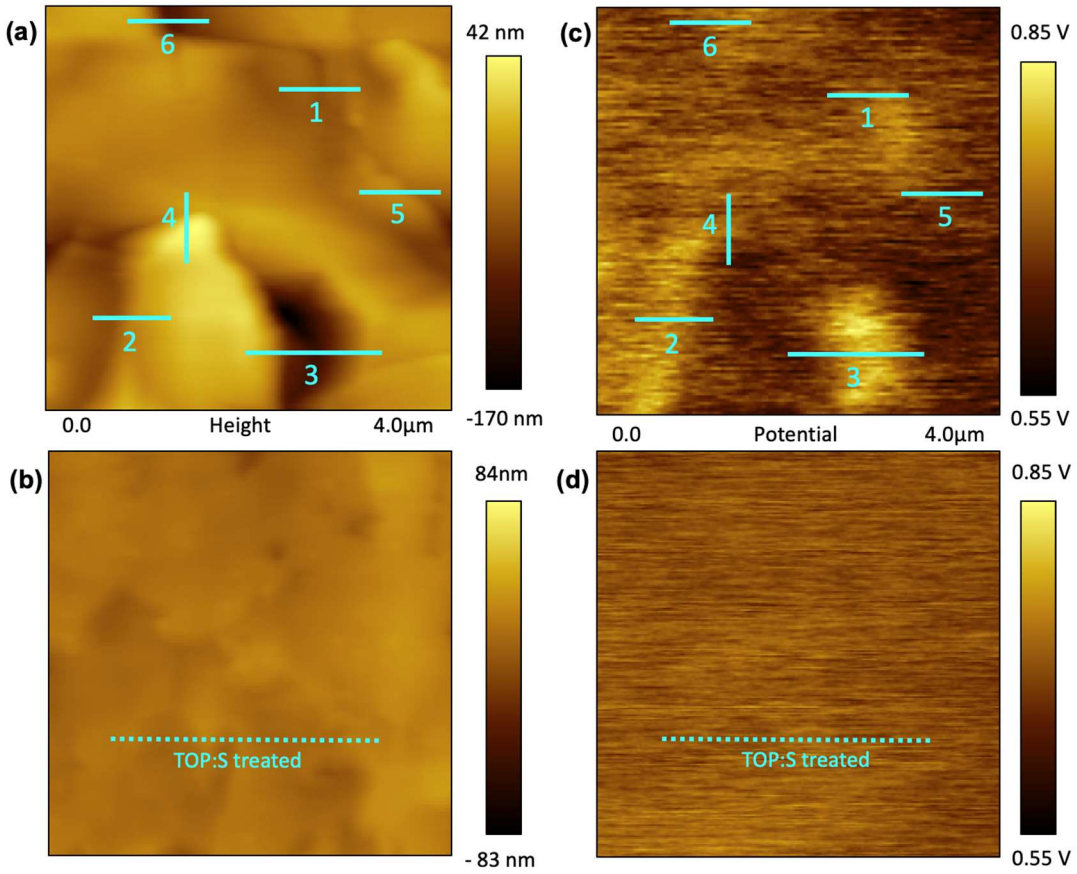


Figure 6.4 SKPM measurements on the single-crystal-like GaAs films (a), (b) topography maps and (c), (d) simultaneously acquired contact potential difference (CPD) maps.

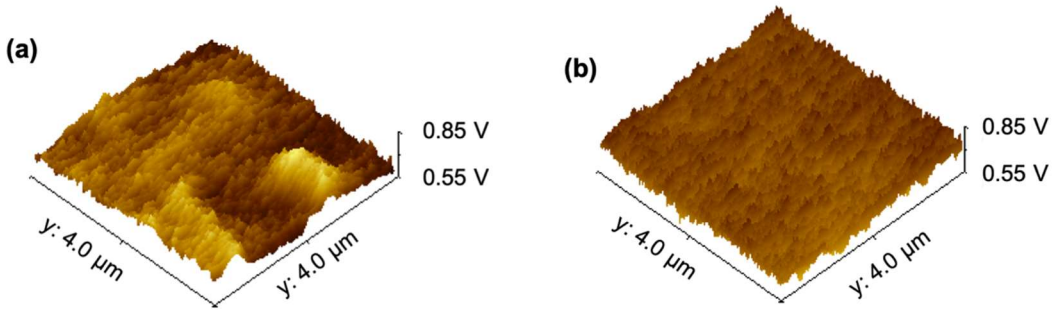


Figure 6.5 3D maps of surface potential (a) before and (b) after TOP:S treatment, respectively.

The 3D map image (Figure 6.5a) of surface potential all over the scanned area of films demonstrates a significant nonuniformity on the as-grown film showing a wide

distribution of surface potential depending on high energy states at local GB regions, as illustrated by the respective red histograms in Figure 6.6b. While the average value of peak maximum and spread from all inspected areas of TOP:S treated GaAs film show a single, narrow distribution (Green histogram in Figure 6.6b).

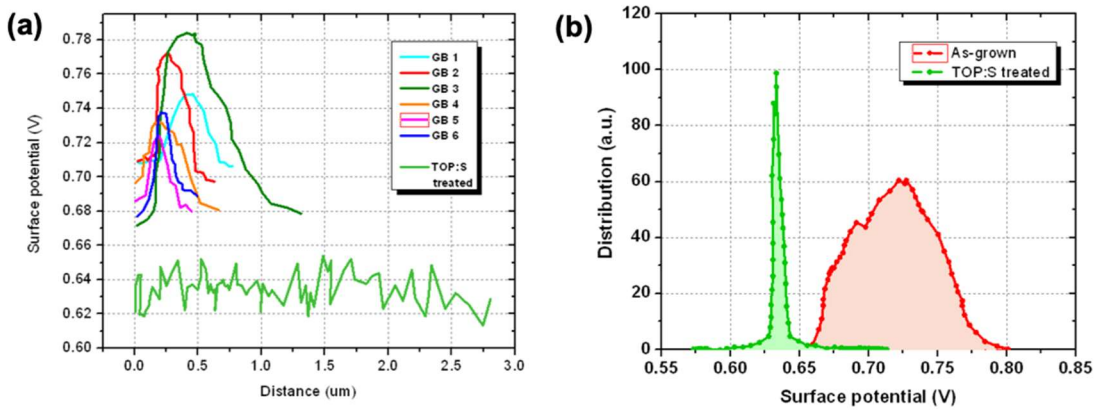


Figure 6.6 (a) Line profiles extracted from the CPD image (the GBs analyzed in this study are marked by blue lines that cross the GB perpendicular in fig. 55a). (b) Histogram of surface potential distribution of as-grown (red) and TOP:S treated GaAs films (green)

It is clearly observed that the TOP:S treated film has a more uniform surface potential distribution than the as-grown film which can be attributed to the passivation of dangling bond defects associated with the GBs and decrease of potential electrons and holes barrier height at these regions. The decrease in GB potential barriers can result in more efficient charge transport and far fewer recombination events, thereby improving the devices' open circuit voltage and short circuit current. Employing the TOP:S treatment on fabricated devices confirmed the effectiveness of passivation process on boosting efficiency performance of single-crystal-like GaAs SC through increasing Voc, Jsc and FF.

6.4 Conclusion

The impact of various passivation treatments of hydrogen ion implantation, hydrogen plasma injection, high-pressure deuterium annealing and TOP:S solution on the PV characteristics of single-crystal-like GaAs was studied. While all the four passivation treatments improved the Voc of SCs, the chemical TOP:S treatment was the most effective technique in passivation of single-crystal-like GaAs by improving all SC parameters and thus increasing the overall efficiency. While potential barrier of (30-120mV) in the LA-GB regions of single-crystal-like GaAs film was observed in CPD map obtained by SPFM, a relatively uniform surface potential over the whole scanned area was observed on the TOP:S treated GaAs film showing reduction of energy states in the GBs. The photo-conversion efficiency of TOP:S treated GaAs SC increased from 6.1% to 10% by improving Voc, Jsc, and FF from 590mV, 18mA.cm^{-2} and 62 to 730mV, 20.3mA.cm^{-2} and 71, respectively. Finally, deposition of ZnS/MgF_2 AR coating on the passivated SC increased the efficiency to 13.5% which is ~2 times higher than the previous efficiency record of flexible single-crystal-like GaAs SC. Higher initial quality of single-crystal-like GaAs material (bigger grain size, lower threading dislocation density and unintentional dopant diffusion from underneath device layers to the p-n junction) would convert higher final photo-conversion efficiency.

CHAPTER 7 CONCLUSION AND FUTURE WORKS

7.1 Summary

While single crystalline materials are ideal for photovoltaic (PV) applications by providing the highest photo-conversion efficiencies, they lack mechanical flexibility and easy scalability. Conversely, currently-developed flexible solar cells independent of any wafer processes have inferior performance characteristics, due to their fundamental limitations in material quality and properties. As these technologies were developed separately, the limitations of each technology were not overcome yet.

Therefore, there is a technology gap between high-performance single-crystalline solar cell devices and less expensive flexible devices for converged and universal solutions of high-performance, economical, flexible, and scalable solar cell modules for large-scale terrestrial and space application.

Here, we proposed a new-concept PV with high efficiency, low cost, and versatile applications employing high quality semiconductors grown on highly-oriented oxide buffers on flexible substrates (by roll-to- roll processing) bypassing costly wafers processes.

High-quality epitaxial III-V compound semiconductors platform for single-crystal-like GaAs solar cell have been developed to address the critical needs for transformative changes in next-generation flexible PVs. The feasibility study on the proposed solar cell and the layers device structure design based on single-crystal-like GaAs have been conducted by using a 1D simulation software. According to the optimized solar cell

structure by simulation, the single-crystal-like GaAs SC device layers structure were grown on single-crystal-like Ge film on epi-ready flexible metal tape.

The initial flexible single-junction single-crystal-like thin-film GaAs solar cell showed an efficiency performance of 7.6% obtained at 1 sun with open circuit voltage (V_{OC}) of 560 mV, current density (J_{SC}) of 19.4 mA.cm^{-2}, and fill factor (FF) of 70%.

Although this initial result was very promising for the newly developed material with very unknown properties affecting device performance, there was a big difference between the efficiency estimated by simulation and experiment results which needed to be further studied in order to be solved. Therefore, a 2D model code capable of taking the effect of local low-angle grain boundaries (LA-GBs) into account more precisely than 1D simulation software has been devolved.

Distinguishing the defective LAGB regions from perfect single-crystal intra-grain areas in the 2D model, the simulated IV characteristics of GaAs SCs showed very-well matched result with the experiment. The model revealed that the LAGB density has a critical impact on SC efficiency. Increasing GaAs grain size from 2µm to 50µm has tripled SC efficiency performance from 4.6% to 12%. While all the SC parameters improved by reducing GB density through increasing material grain size, the V_{OC} and J_{SC} have showed different improvement trends and amount so that the J_{SC} reached to a saturation level ~93% of its maximum value for grain sizes above 15µm while V_{OC} for the grain size of 50µm still left ~0.3V behind its maximum (in the absence of GBs).

The model has been further modified to incorporate a GBs passivation effect on the SC efficiency improvement. The study on the passivation of dangling bonds at LA-GBs

showed a significant improvement for SC characteristics especially V_{OC} resulting in an efficiency boost from 4.8% to ~19.7% for even small grain size of 2 μm. Therefore, there is a significant potential to achieve high SC device performance based on single-crystal-like GaAs comparable to wafer-based materials.

Various passivation treatments of hydrogen ion implantation, hydrogen plasma injection, high-pressure deuterium annealing and trioctylphosphine sulfide (TOP:S) solution have been employed on the single-crystal-like GaAs SCs. Although all the three first methods have resulted in a certain degree of improvement in selected IV characteristic parameters of SC, at the same time they have caused some side-effects that have limited overall SC efficiency improvement.

In this study, the chemical TOP:S treatment has been found to be the most effective technique for passivation of single-crystal-like GaAs which has improved all the SC parameters and thus has increased the overall device performance. The photo-conversion efficiency of TOP:S treated GaAs SC increased from 6.1% to 10% by improving Voc, Jsc, and FF from 590mV, 18mA.cm^{-2} and 62 to 730mV, 20.3mA.cm^{-2} and 71, respectively. The final single-crystal-like SC was obtained after deposition of ARC which delivered an efficiency performance of 13.5%. The efficiency of passivated SCs is about two times of the previous record, 7.6%, for un-passivated devices.

7.2 Recommendations for future works

This newly developed flexible PV technology still has much more rooms for higher efficiencies which can be achieved by further optimization of materials growth, device

design and passivation treatments. Therefore, future works could be focused on following aspects of this technology.

1. Optimization of growth conditions of crystallinity-transitional oxide buffer layers and biaxially-textured semiconductors for lower threading dislocation density (TDD) and unintentional dopant diffusion from underneath device layers to the p-n junction
2. Developing of semiconductor materials with bigger grain size (less dislocation density)
3. Replacing current insulating oxide-buffer layers by conductive buffer layers to be able to employ a vertical solar cell device geometry for better carrier dynamics
4. Exploring of other passivation techniques for more effective reduction of dangling bonds at the GB regions

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APPENDICES

Lift off process for contact electrode metallization:

Steps	process	Process condition(s)	time	Thickness (nm)	Annealing (baking for PR) temperature (°C)
1	LOR5B deposition (using spin coater)	3000 rpm 500 acc	45 sec	500	-
2	Soft baking (hot plate)	-	5 min	-	170 °C
3	S1813 deposition (using spin coater)	4000 rpm 500 acc	1 min		
4	Soft baking (hot plate)	-	1 min	-	110 °C
5	Pattern transfer, Exposure (MJB3)	-	9 sec	-	-
6	Developing (MF319)	Gently agitate	~ 40-45 sec	-	-
7	Hard baking	-	1 min	-	110 °C
8	HCl cleaning	-	~15 sec	-	-
9	Metallization (e-beam evaporation)	Pressure ≈ 1 µTorr Room temperature Variety of currents	Depends on the deposition rate	Au: 300 Ni: 35 AuGe: 100 Ni: 5	-
10	RTP annealing	Using forming gas	~ 70-80 sec at 425 °C	-	425 °C and cooling down to room temperature
11	Post-developing (MF319)	Gently agitate	~ 3-4 min	-	-

Flexible GaAs SC fabrication run sheet

Below is the process flow for growth and fabrication of flexible single-crystal-like GaAs SC:

PROCESS	STEP	Detail	Condition	Date	worker	comment
Sample Prepared	cleaning	Inspection	with Microscope (File name :)			
		cleaning	ACE : 3 min / IPA : 3 min / DI water : 3 min / D2 Dry			
		Inspection	with Microscope (File name :)			
ITO deposition	Remove oxide	Acid Clean	HCl: H2O (1:1) DI rinse, N2 DRY			
	deposition	Base pressure	Low x10^{-7} torr			
		Working Pressure	5X10^{-3} torr			
		Gas	35 sccm			
		Power	100W			
		Presputtering	300 sec			
		Workiing time				
	Measurement	Measure	with α-step			
MESA	Cleaning	cleaning	ACE : 3 min / IPA : 3 min / DI water : 3 min / D_2 Dry			
		Inspection	with Microscope (File name :)			
	Photo lithography	PR coating	Spin Coater, PR: PR1-2000A (positive), RPM: 3000, Time: 40 sec			
		Soft baking	Hot Plate, Temperature : 130 ℃, Time : 90 sec			
		Expose	Aligner, Time : 12sec ,dose : 10 mJ/cmsq, Mask name : 6th mask			
		Develop	Chemical : RD6, time : 40 sec			
		Rinsing	DI water, Time : 3 min, N_2 Dry			
		Inspection	with Microscope (File name :)			
	Ashing	Pre-ashing				
		Pressure	60			
		Power	RF : 60 W, ICP 0 W			
		Time	40 se			
		Gas	O2			
		Inspection	with Microscope (File name :)			

	Post baking	Post baking	Hot Plate, Temperature : 130 ℃, Time : 90 sec			
	Etching	ITO etching	Chemical : TE-100, time : 10 sec			
		Oxide remove	HCl: H2O (1:1) DI rinse, time : 40 sec			
		GaAs Etching	Chemical : GaAs-300, time : 300 sec			
		Inspection	with depth profilermeter (etch depth : W-S1-431=3.4um, F-S1-437= 2.8~3um)			
			with Microscope (File name :)			
	PR Removing	Removing	ACE : 5min/ DI water : 3 min / D2 Dry			
		Inspection	with depth profilermeter (etch depth : W-S1-431=1.6um, F-S1-437= 1-1.5~1.3			
			with Microscope (File name :			
ITO Annealing		cleaning	ACE : 3 min / IPA : 3 min / DI water : 3 min / N_2 Dry			
		annealing	Time : 1200 sec, Temperature: 400°C, O_2 ambient with RTP system			
n-contact	Photo lithography	PR coating	Spin Coater, PR : Aznlof2020 , RPM: 3000, Time: 60 sec			
		Soft baking	Hot Plate, Temperature : 120 ℃, Time: 70 sec			
		Expose	Aligner, Time : 12sec ,dose : 10 mJ/cmsq, Mask name : 6th mask			
		Post baking	Hot Plate, Temperature : 120 ℃, Time: 70 sec			
		Develop	Chemical AZ 300MIF, Time : 30 sec			
		Rinsing	DI water, Time : 3 min, N_2 Dry			
		Inspection	with Microscope (File name :)			
	Ashing	Pre-ashing				
		Pressure	60			
		Power	RF : 60 W, ICP 0 W			
		Time	40 sec			
		Gas	O2			
		Inspection	with Microscope (File name :)			
	Remove oxide	Acid Clean	HCl: H2O (1:1), time: 30sec, DI rinse, N2 DRY			
	Deposition	Deposition	with E-beam			
			Ni (5 nm) /Ge (10nm)/ Au (200nm)			
		Lift-off	ACE (20 min) with US			
		cleaning	ACE : 3 min / IPA : 3 min / DI water : 3 min / D2 Dry			

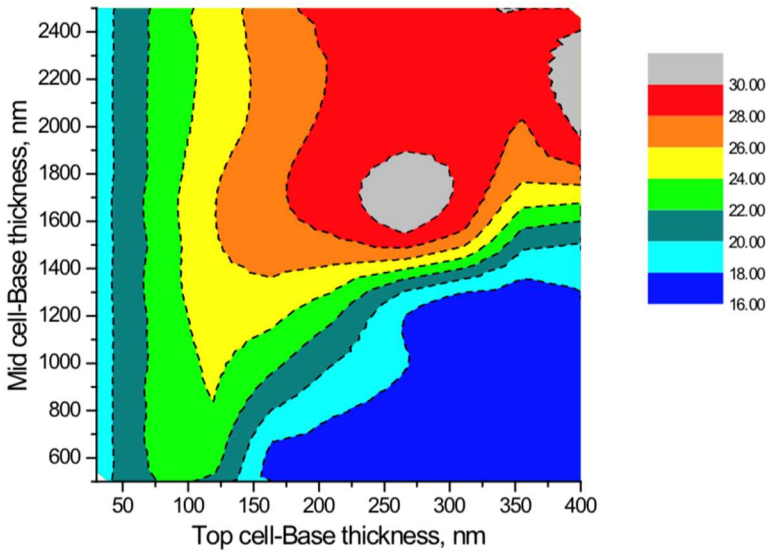
	Measurement	Inspection	with Microscope (File name :)			
		TLM	With I-V measument :			
p-contact	Photo lithography	PR coating	Spin Coater, PR : Aznlof2020 , RPM: 3000, Time: 60 sec			
		Soft baking	Hot Plate, Temperature : 120 ℃, Time: 70 sec			
		Expose	Aligner, Time : 12sec ,dose : 10 mJ/cmsq, Mask name : 6th mask			
		Post baking	Hot Plate, Temperature : 120 ℃, Time: 70 sec			
		Develop	Chemical AZ 300MIF, Time : 30 sec			
		Rinsing	DI water, Time : 3 min, N_2 Dry			
		Inspection	with Microscope (File name :)			
	Ashing	Pre-ashing				
		Pressure	60			
		Power	RF : 60 W, ICP 0 W			
		Time	40 sec			
		Gas	O2			
		Inspection	with Microscope (File name :)			
	Remove oxide	Acid Clean	HCl: H2O (1:1), time: 30sec, DI rinse, N2 DRY			
	Deposition	Deposition	with E-beam			
			Cr (15 nm) /Au (200nm)			
		Lift-off	ACE (20 min) with US			
		cleaning	ACE : 3 min / IPA : 3 min / DI water : 3 min / D2 Dry			
	Measurement	Inspection	with Microscope (File name :)			
		TLM	With I-V measument :			
Analysis	Measurement		장비 : Wafer Level Test, 4145B, I-V			

Multi-junction GaAs SC

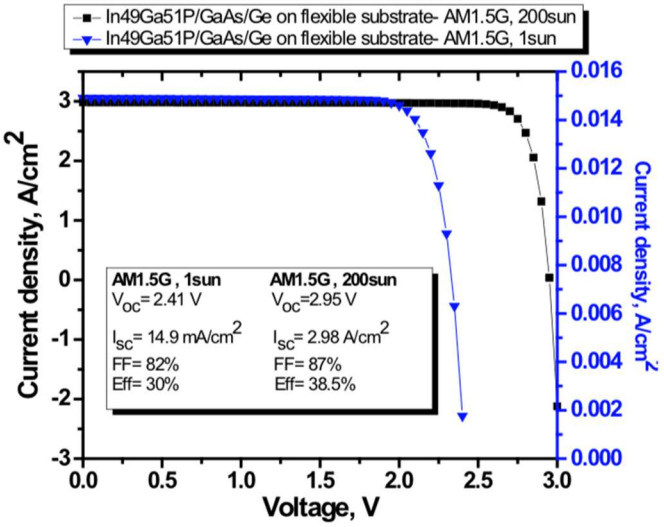
Simulation results for optimized GaAs triple junction SC device structure on flexible substrate

Window	10	p-$Al_{0.2}In_{0.49}Ga_{0.31}P$	6×10^{18}
Emitter	50	p-$In_{0.49}Ga_{0.51}P$	5×10^{18}
Base	**300**	n-$In_{0.49}Ga_{0.51}P$	1.5×10^{17}
BSF	50	n-$Al_{0.2}In_{0.49}Ga_{0.31}P$	2×10^{18}
TJ	5	n-$In_{0.49}Ga_{0.51}P$	1×10^{20}
TJ	5	p-$In_{0.49}Ga_{0.51}P$	5×10^{19}
Window	10	p-$In_{0.49}Ga_{0.51}P$	1×10^{19}
Emitter	150	p-GaAs	8×10^{18}
Base	**1800**	n-GaAs	1×10^{17}
BSF	300	n-$In_{0.49}Ga_{0.51}P$	1×10^{19}
TJ	5	n-$In_{0.49}Ga_{0.51}P$	1×10^{20}
TJ	5	p-$In_{0.49}Ga_{0.51}P$	5×10^{19}
Window	10	p-$Al_{0.2}Ga_{0.8}As$	7×10^{18}
Emitter	300	p-Ge	2×10^{18}
Base	2500	n-Ge	1×10^{17}

Triple junction $In_{0.49}Ga_{0.51}P$/GaAs/Ge solar cell structure on flexible substrate (thicknesses are in nm). Mid- and top-cell base thicknesses are the optimized one for highest conversion efficiency.



Calculation of the theoretical efficiency of a monolithic triple-junction tandem SC on flexible substrates under AM1.5G illumination (1sun) conditions, depending on two major design parameters, e.g., thickness of mid-cell and top-cell.



Light I-V characteristics of a triple-junction GaAs SC on flexible substrate under AM1.5G 1- and 200sun spectral illumination conditions.