HVDC POWER DISTRIBUTION AND PROTECTION ARCHITECTURES FOR SUBSEA ELECTRICAL SYSTEMS

by

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Abstract

Subsea electrification is one of the key building blocks for harnessing deep-water hydrocarbon resources. A subsea electrical system should operate reliably over a long time duration to maximize production and minimize operational cost. State-of-the-art subsea electrical systems utilize high voltage alternating current (HVAC) transmission. Although HVAC is a well-known technology, the large reactive power demand of the transmission cable presents a serious challenge in long-distance transmission. To address these issues, this dissertation proposes a family of novel power distribution architectures based on high voltage direct current (HVDC) technology. A family of novel DC fault protection topologies to be applied in these HVDC architectures has also been proposed.

Current HVAC systems supply power to subsea loads through a high voltage submarine cable. With increasing transmission distance, the reactive power drawn by this HV cable increases manifold, resulting in serious cost implications. The line charging reactive power is eliminated in HVDC submarine cables, which offers substantial cost benefits in long-distance transmission. This dissertation proposes three novel HVDC architectures for long tie-back subsea fields. The solid-state transformer (SST) based modular distribution system provides increased redundancy and fault-tolerant operation.

HVDC system requires fast protection against short-circuit faults. Fault interruption in DC systems is difficult due to the absence of zero-crossing in the fault current. To address this issue, a family of zero current switching (ZCS) hybrid DC breakers has been proposed. The presented circuit-breakers realize arcless breaking operation for mechanical breakers. Fast fault response by the proposed DC breakers has been verified using experimental prototype units.

Subsea production system also uses direct electric heating (DEH) of subsea pipelines

to prevent hydrate formation. The existing DEH technology requires significant VAr compensation due to the highly inductive pipeline. An LCCL resonant inverter (LCCL-RI) is presented in this dissertation to alleviate this issue. The LCCL-RI operates as a load-independent constant current source. Tank capacitors provide the required reactive power compensation. The performance of the LCCL-RI is evaluated in a SiC MOSFET based laboratory prototype.

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Chapter 1

Introduction

1.1 Background and Motivation

Subsea processing entails drilling, conditioning, pumping and compression of hydrocarbons in offshore deep-water. The recent trend in the subsea industry has been focused on more electrification of the production system located on the seabed to provide an efficient and economical solution [1]-[6]. Although deep-water operation brings challenges in terms of the increasing pressure of 10 bar/100 m of depth, it can be alleviated by using pressure-compensated enclosures for the electrical units. Moreover, the advancements in the research of pressure compensated power devices have made the vision of an all subsea power grid a reality [7]-[8]. Nonetheless, the prime objective of a subsea electrical system should be reliable operation with minimum hiatus in the O&G processing.

Subsea deep-water electrical systems employ long-distance transmission networks to transfer electrical power from shore to the subsea loads, such as pump and compressor motors. State-of-the-art subsea power delivery networks are high voltage alternating current (HVAC) systems with a multi-core subsea cable (umbilical), which interfaces the onshore generation to the subsea distribution. For a typical HVAC system, as shown in Fig. 1.1, power is generated onshore and the generator bus voltage is boosted up through a step-up transformer [2]. The HVAC umbilical is employed to transmit power at this HV level up to the subsea distribution transformer. Thereafter, a number

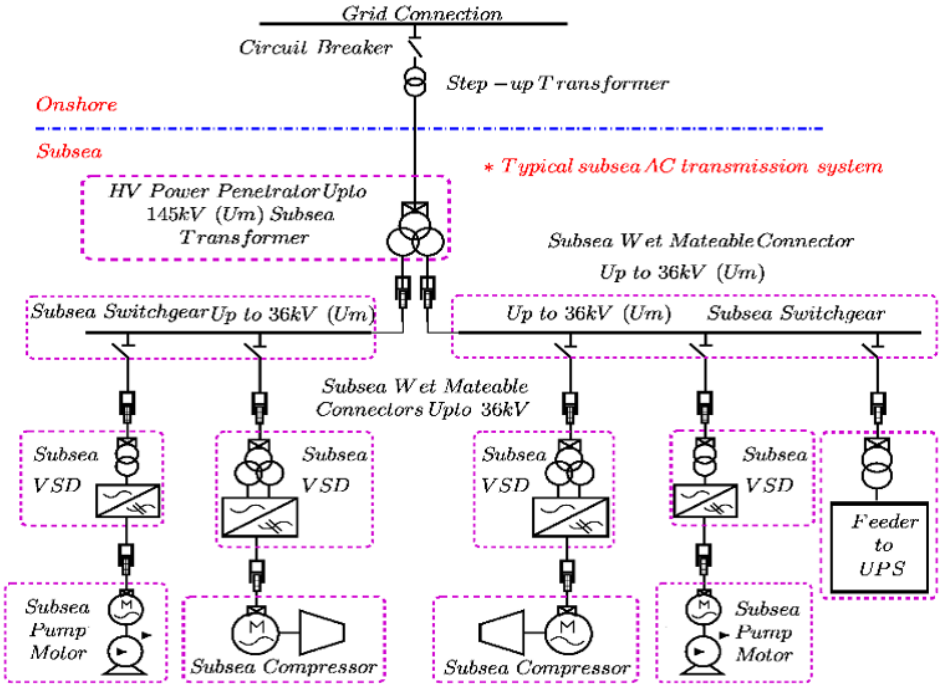


Figure 1.1: A Typical Subsea Power Distribution System

of LV cables interface the subsea variable speed drive (VSD) loads.

HVAC systems are inherently simple in structure and require less number of power conversion stages. However, the HVAC umbilical has a significantly large line-to-ground capacitance. As a result, a line charging current of substantial magnitude is drawn from the source. The charging current increases with longer step-out distances, which may lead to a reactive power demand greater than the active power rating, which is in the order of 100 MW with several pumps and compressors, each rated for about 5 to 10 MW [1]. Beyond a transmission distance of 60 km (break-even distance in subsea), the power processing becomes inefficient and uneconomical due to the high reactive power demand, even with external reactive compensation [6]. Thus HVAC transmission ceases to be a feasible solution for remote, deep-water O&G field.

Reactive power issues for long step-out transmission can be mitigated by low-frequency AC (LFAC) systems of 16.7 Hz or 20 Hz frequency. As the line charging current is proportional to the operating frequency, LFAC systems can employ a

conventional 3-ϕ coss-linked polyethylene (XLPE) based cable for remote offshore systems with reduced VAr requirement from the onshore grid [15]-[18]. Also, the power transfer capability can be improved significantly by LFAC transmission [20]. However, the LFAC architecture requires bulky line-frequency transformers at the sending and receiving end of the transmission cable due to the reduced operating frequency [35]. This results in a large system footprint and low power density, which renders the LFAC system unsuitable for all-subsea units based power distribution.

Another drawback of the existing AC power architectures arises from the point of reliability. Conventional HVAC or LFAC transmission architectures are hub-and-spoke type architectures having a single power receiving point, i.e., the step-down transformer which interfaces the HV transmission and the LV distribution stage. These types of systems are susceptible to a single-point failure. To improve reliability, a ring-type distribution system based on series-connected transformers has been explored in the literature for fault-tolerant operation [14]. Nevertheless, the proposed architecture still suffers from the reactive power issue as the transmission stage remains HVAC. Also, during a fault in one transformer unit, the rest of the healthy series-connected units will be subjected to unbalanced voltage distribution and subsequent overvoltage.

High voltage direct current (HVDC) systems exhibit comparable advantages over AC systems for long-distance transmission as the line charging current is non-existent. It is possible to efficiently transmit bulk power in an HVDC system without voltage sag. Voltage-source converter (VSC) based HVDC multi-terminal architectures can also provide easy interconnection between offshore renewable generation and remote subsea O&G fields [36]-[37]. Subsequently, HVDC transmission for offshore and subsea systems has been extensively investigated [24]-[28]. Also, MVDC architectures using modular multilevel converters have been presented in the literature [29]-[32], which provide added redundancy and fault-tolerant operation of subsea power systems. The

use of subsea HVDC transmission has been bounded to date due to the technology limitation of high voltage DC cable and wet-mate connectors [41], [47]-[48]. However, recent advances in the aforementioned area make HVDC a very promising solution for long tie-back, deep-water subsea systems.

Fast identification and interruption of faults in subsea systems are critical in maintaining reliable operation [46]. Fault interruption can be particularly challenging for DC power systems as the fault current does not experience any natural zero-crossing. Circuit breakers employed in HVDC/MVDC power networks should be capable of fault quenching within 1 millisecond to prevent damage to the power delivery units [49]-[52]. Existing DC circuit breakers are categorized as solid-state circuit breakers (SSCB) and hybrid circuit breakers (HCB) [53]-[58]. An SSCB comprises of only power semiconductor devices and can interrupt fault in a few microseconds. However, the high on-state voltage drop of the semiconductor devices leads to substantial conduction power loss during normal operation and thus a forced cooling arrangement is needed. In the subsea environment, the breaker is placed within the pressure compensated chamber, so the cooling of the devices becomes a challenging proposition. On the other hand, an HCB exhibits negligible conduction loss by employing a mechanical breaker (MCB) but encounters arc formation across the moving contacts of that MCB, resulting in slow fault quenching and reduced life-cycle [59]-[60].

Apart from the faults in the subsea VSD operation, another factor to hamper the reliability of subsea processing is the formation of hydrates inside the production pipeline. Hydrates are typically formed around a critical temperature of 25^{o}C, causing a reduction in the fluid flow. The most efficient and cost-effective method to prevent hydrate formation is known as the direct electric heating (DEH) of the pipeline, where the heating effect of electric current is utilized to maintain the pipeline above the critical temperature. A typical power distribution architecture for DEH application has been

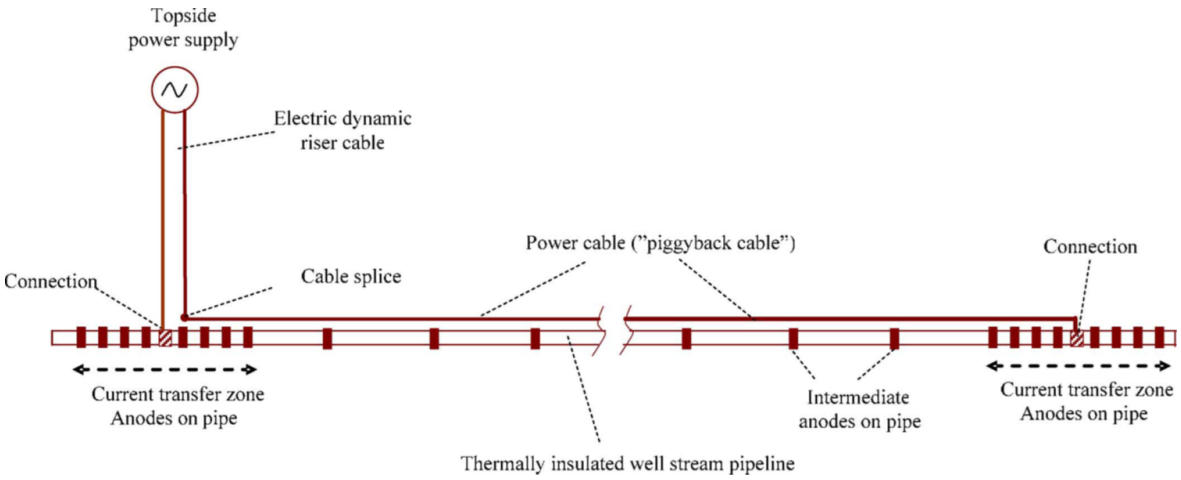


Figure 1.2: A Subsea Direct Electric Heating System

shown in Fig. 1.2 [130]-[135]. A topside power source circulates single-phase current through the subsea pipeline via a pair of piggyback cables, running in parallel with the pipeline. The current return path is through the pipe as well as the surrounding seawater. The single-phase current generates the heat in terms of conduction power loss. Although the existing DEH system is a cost-effective method, it requires a dedicated topside power source with high VA rating due to poor load power factor ($\sim$ 0.25) due to the predominantly inductive impedance of the pipeline. Also, balancing transformer and reactive compensation units are required in the existing DEH system for interfacing the topside power source with the subsea pipeline.

The solution to mitigate the aforementioned challenges in subsea electrification is to employ an HVDC transmission and distribution (T&D) architecture which improves the reliability of operation in terms of redundancy and fault tolerance. This thesis proposes three HVDC power transmission architectures with a modular structure to provide fault-tolerance as well as to minimize the reactive power requirement. A family of resonance assisted, zero current switching hybrid circuit breaker topologies has been developed for fast overcurrent or short-circuit fault interruption in the

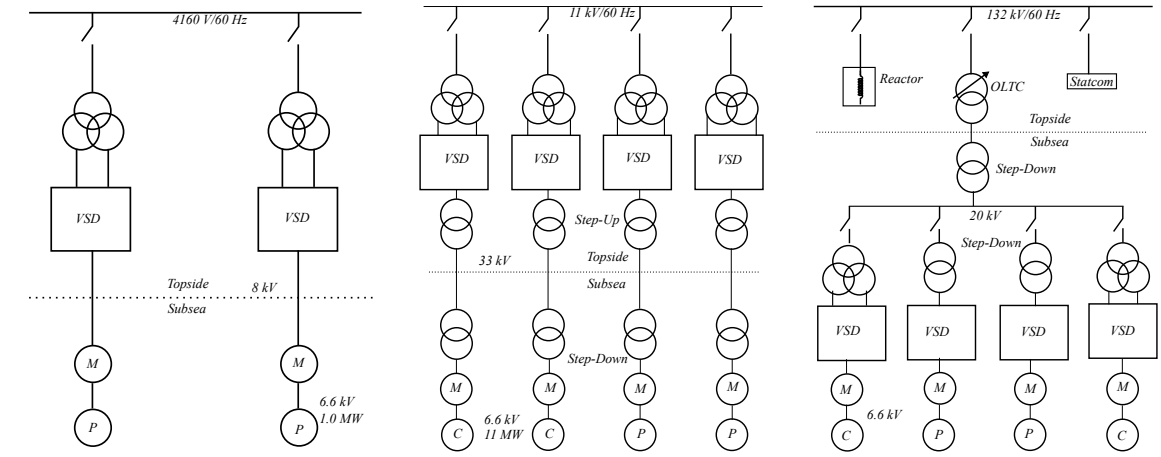


Figure 1.3: Subsea HVAC Architectures. (a) Type-I. (b) Type-II. (c) Type-III.

presented HVDC architectures. Finally, an LCCL resonant inverter (RI) based single-phase constant current (CC) supply has been proposed in this thesis. The proposed CC supply exhibits improvement over the existing DEH solution by providing in-built reactive power compensation as well as short-circuit protection. Moreover, the presented LCCL-RI operates at a frequency much higher than the line-frequency (50/60 Hz) which improves the heating efficiency [136]-[137].

1.2 Review of Subsea Power Transmission Architectures

1.2.1 HVAC Transmission Architectures

Most of the subsea power transmission networks in operation are high voltage AC (HVAC) systems. A typical subsea HVAC system consists of three power delivery stages. In the first stage, the onshore bus voltage is boosted by a step-up transformer to the transmission voltage level. Then the power is transmitted to the subsea distribution unit through the HVAC umbilical. In the distribution stage, a voltage step-down may be needed to supply the pump and compressor drives.

Depending on the location of the components and the power rating, subsea HVAC architectures can be divided into three categories, as shown in Fig. 1.3.

- *Type-I Architecture*: In a type-I HVAC system, the variable speed drives are located in the topside vessel or onshore. Usually, the 3-ϕ AC bus voltage is 4160 V rms, whereas the subsea motors are rated for 6.6 kV rms, hence no step-down subsea transformer is required [9]-[10]. Type-I systems are utilized for short tie-back applications up to 25 km with a total load of 10-20 MVA, such as the BP King multi-booster project [20].

- *Type-II Architecture*: Type-II architecture uses a step-down subsea transformer while the VSDs are located on topside. This system can cater to more number of subsea loads and is suitable for a longer step-out distance up to 50 km. The typical transmission voltage level is 33 kV while the subsea drives operate at 6.6 kV. A common example of a type-II HVAC system is the Asgard subsea compression unit [20].

- *Type-III Architecture*: This architecture is widely utilized for long tie-back subsea fields (up to 100 km), such as the Martin Linge platform [11] or the Ormen Lange compression station [12]. Usually, the transmission voltage level is 132 kV, while multiple step-down transformers may be required to supply several VSD loads. However, this system requires reactive VAr compensation units onshore to account for the cable charging current.

Due to the standardization of high-voltage components and simplicity of operation, HVAC architectures have been popular for subsea power transmission. However, the biggest disadvantage in an HVAC system arises due to the HVAC umbilical charging current, which is proportional to the square of the operating voltage, given by the

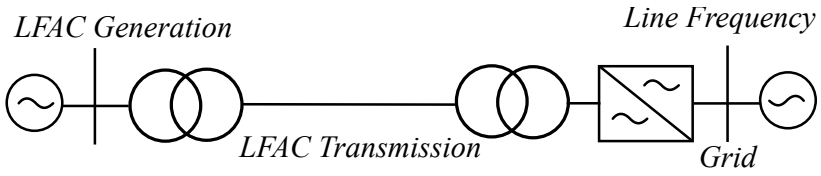


Figure 1.4: LFAC System without offshore frequency converter

equation

$$Q_c = 2\pi f C V_{LL}^2, \tag{1.1}$$

where, C is the line to ground capacitance of the cable, and V_{LL} is the line voltage.

For type-III architecture, the costs and operational complexity associated with reactive compensation may not justify the use of HVAC for long tie-back subsea fields. Moreover, with increasing power demand in multiple subsea field development, transient stability of the power system is affected and requires additional subsea transformers, which escalates the operational cost [13].

1.2.2 LFAC Transmission Architectures

Equation 1.1 indicates that a reduction in the operating frequency leads to a decrease in the capacitive reactive power Q_c without any change in the operating voltage. This leads to the idea of the low-frequency AC (LFAC) system operating at one-third of the grid frequency, i.e., 16.7 Hz or 20 Hz. LFAC systems have been employed for long-distance transmission of offshore wind power to onshore grid [15] -[22]. LFAC systems exhibit several advantages over the line-frequency (50/60 Hz) HVAC system in terms of increased power transfer capability, better voltage stability and reduced charging current which is attractive for long-tieback subsea O&G fields.

Frequency conversion based on phase-controlled cycloconverter is one of the main features in a low-frequency power transmission network. Depending on the frequency of

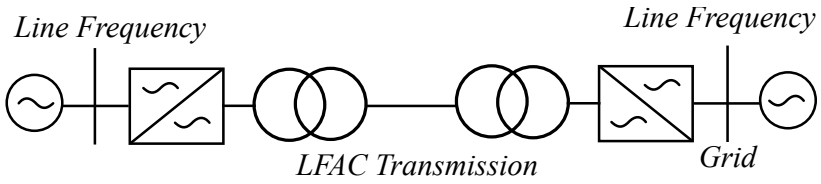


Figure 1.5: LFAC System with offshore frequency converter

offshore generation, LFAC systems are of two types [43]. With back-to-back converters, the offshore wind farm can generate output at 16.7 Hz or 20 Hz, which eliminates the offshore frequency conversion stage. Although a frequency converter along with a low-frequency transformer has to be present onshore to interface the 50/60 Hz grid. Such an LFAC system has been shown in Fig. 1.4. However, in some cases, the wind turbine output is also 50 or 60 Hz, which necessitates an offshore frequency conversion stage, as shown in Fig. 1.5.

Due to the large footprint of the low-frequency transformer cascaded to the frequency converter, subsea units based implementation of the LFAC transmission becomes challenging. One of the examples of a low-frequency subsea transmission is the LFAC roto-converter [20], which utilizes a fractional frequency distribution to reduce cable aging. However, the transmission stage is still HVAC. Besides, the fault level in an LFAC system is significantly higher than the conventional HVAC, which necessitates electrical installations with a high current rating.

1.2.3 HVDC Transmission Architectures

DC systems demonstrate clear advantages over its AC counterparts in high voltage transmission in terms of higher power transfer capability, longer transmission distance and more cost-effectiveness. The global trend has seen an increase in HVDC projects, especially for harnessing renewable sources such as offshore wind power [23]-[28]. HVDC transmission systems use two distinct power converter topologies, namely

the line-commutated current source converters (CSC) and self-commutated voltages source converters (VSC). Line commutated CSCs using thyristor valves are the most prevalent due to higher power handling capability. However, CSCs require a strong synchronous voltage source for commutation and bulky line filters. With the advent of IGBTs, VSCs have garnered more interest due to their superior performance in terms of independent control of active and reactive power [24]. The growth of Silicon Carbide (SiC) devices has made VSC-based transmission a very attractive proposition for long tie-back fields.

The present application of HVDC transmission in subsea O&G has been limited to a handful of projects, such as Troll-A production platform in north sea [6]; HVDC transmission is utilized for a step-out distance of 70 km to drive a high voltage 'motorformer' machine at 300 m water depth. However, the Troll-A configuration is not realizable for deep-water systems due to the large footprint. A subsea DC distribution grid using a front-end active rectifier has been explored in [28]. The proposed system exhibits promising fault-tolerance performance, although the structure is too simplistic without considering voltage buck or boost stages in subsea. Moreover, a tie-back length of 30 km is not an optimum choice of HVDC in terms of cost.

To reduce the system footprint and improve reliability, ring-type architectures have been explored, which employ series-connected open-winding transformers in the distribution stage, shown in Fig. 1.6 [14]. Each distribution transformer is located close to its load. The distribution level AC voltage is divided among multiple transformers. In case of a load side fault, the particular section can be isolated by using a bypass switch connected across the primary winding of the transformer. The transmission stage of this ring-type architecture can be either HVAC (Fig. 1.6(a)) or HVDC using rectifiers at the sending end (Fig. 1.6(b)). Ring-type architectures show higher redundancy and reliability compared to conventional hub-and-spoke type architectures

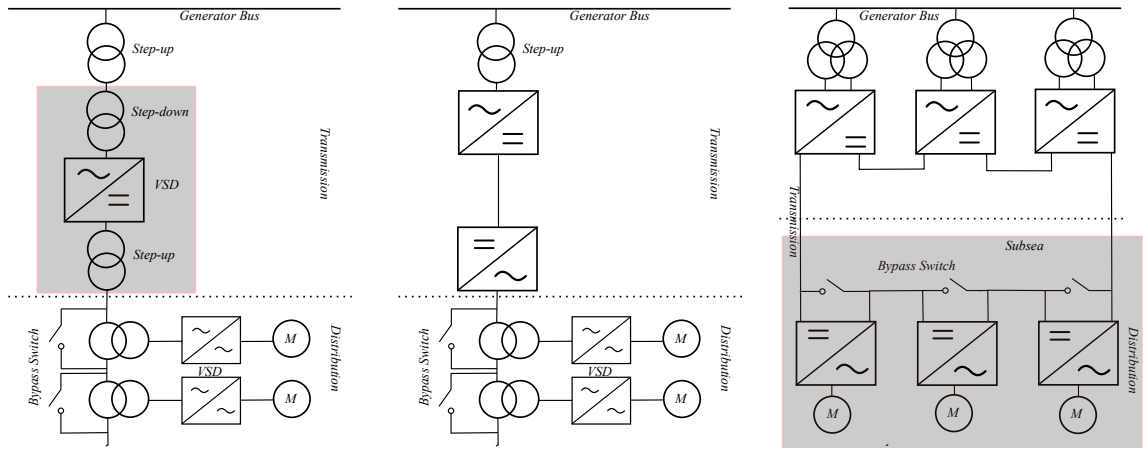


Figure 1.6: Ring Type Architectures. (a) HVAC. (b) HVDC. (c) MSDC.

due to the point-of-load distribution system. Nonetheless, reactive power compensation is still a challenge for AC transmission or distribution. Moreover, overvoltage on series-connected transformers can be an issue in this current-controlled system.

The modular power stages of ring-type architecture provide added redundancy in subsea operation. The modular stacked DC (MSDC) transmission system, shown in Fig. 1.6(c) has been proposed for long-distance subsea applications [29], [30], [32]. MSDC architecture employs several series-connected modular multilevel converter (MMC) modules to obtain a high DC voltage. The power converter modules both at the sending and receiving end are current-controlled, so a change in power set-point results in a change in sending end voltage. The proposed system requires several line-frequency transformers at the sending end as well as a large number of wet-mate connectors and penetrators for the interconnection of multiple subsea fields [6]. MMC based multiterminal HVDC system has been explored for subsea transmission which combines the control of DC voltage and power injection for improved transient performance [31]. However, the proposed structure offers little redundancy due to the single-point distribution.

1.3 Review of DC Circuit Breakers

The main impediment in the growth of DC architecture for medium and high voltage DC transmission is due to the lack of fast and reliable protection against short-circuit faults [49]-[50]. A bolted fault in a DC system results in the rapid ramp-up of the fault current. Moreover, DC fault current does not experience any natural zero-crossing. Therefore, DC circuit breakers should be capable of fast fault quenching to prevent damage to the DC system and maintain grid resiliency. Additionally, a DC circuit breaker should operate with minimal power loss as a closed switch [51]-[57].

DC circuit breakers (DCCB) can be categorized as solid-state circuit breakers (SSCB) and hybrid circuit breakers (HCB). An SSCB utilizes only power semiconductor devices for fast fault interruption. A typical configuration of an SSCB is shown in Fig. 1.7(a) [61]-[62]. The semiconductor switch S conducts the power during the power delivery mode. During the fault, S is turned off and the energy stored in the network inductance L_{dc} is dissipated in the parallel metal-oxide varistor (MOV). The voltage across the switch is limited to the clamping voltage of the varistor. Although the breaking operation is very fast as the switch S can turn off within a few μs, the varistor needs to be properly sized to completely quench the inductive energy and prevent surge voltage across the switch.

SSCBs have been implemented with different power switches, such as thyristors [63], [64], IGCTs [63], [67], IGBTs [65]-[67], [69], cathode-short MOS controlled thyristor [68], SiC JFETs [70]-[71], SiC MOSFETs [72] etc. With the faster switching device, fault interruption time reduces. However, the conduction loss in the switch S reduces the system efficiency and feasibility for a subsea operation due to the forced cooling requirement. Also, the footprint of the parallel MOV escalates for high voltage operation, which again limits the application of SSCBs. A split snubber arrangement reduces

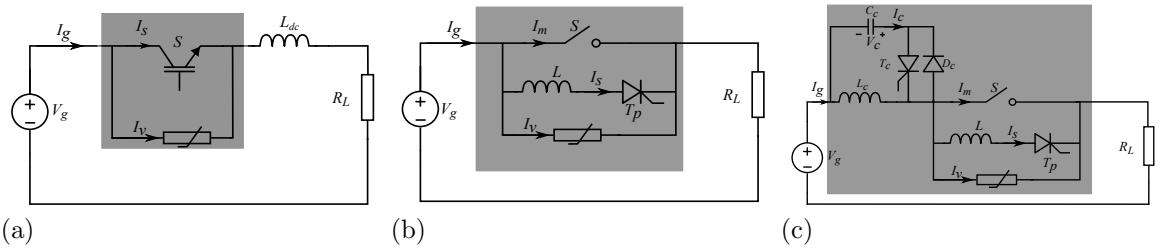


Figure 1.7: DC Circuit Breakers. (a) SSCB. (b) HCB. (c) Forced commutation HCB.

the footprint but at the cost of a higher blocking voltage stress on the semiconductor switch [73].

On the other hand, An HCB is typically constructed using a mechanical circuit breaker (MCB) or contactor in parallel with auxiliary fault commutation branches comprising of semiconductor switches, energy storage elements, and varistors. The schematic of a conventional HCB is shown in Fig. 1.7(b) [53], [75]. MCB S conducts the current during power delivery mode. The auxiliary branch switch T_p is off during this duration. Upon the detection of a fault, S is turned off and T_p is switched on at the same instant. The opening of MCB results in an arc between the moving contacts. The magnitude of arc voltage decides current commutation to the auxiliary branch. T_p is turned off when the MCB contacts are completely open, and the stored energy in the network inductance is dissipated by the parallel MOV branch.

Thus, the fault response time of conventional HCBs relies mostly on MCB contact separation speed, ranging up to several milliseconds. Also, repeated arcing events reduce the lifetime of the HCB. However, the conduction loss is greatly reduced due to the low on-resistance of MCB, which makes HCB a more efficient solution for HVDC applications. The response of the HCB can be improved by incorporating auxiliary static cells [74] or using ultra-fast Thomson-coil actuator-based mechanical switches [82]-[85]. Nonetheless, fault response time below 2 ms has not been achieved yet.

The fault response of a conventional HCB can also be improved by inserting a

fast load commutation switch (LCS) in series with the MCB, as in the case of ABB hybrid HVDC breaker [76]. During normal operation, both MCB and LCS conduct. When a fault is detected, the gating signal of LCS is withdrawn and the current is almost immediately commutated to the auxiliary semiconductor modules. The MCB contacts can now be opened at zero current which removes arcing. However, as the LCS is realized by power semiconductor devices, significant conduction loss still occurs at high power.

The ABB circuit breaker concept has been used in several HCB topologies with different implementations of the LCS and auxiliary semiconductor modules [77]-[81]. Still, HCBs require parallel MOV branch or resistive snubber circuits for dissipating the stored inductive energy and suppressing transient voltage peaks across the MCB. MOVs are susceptible to thermal failures, which affects the reliability of the switchgear. To increase redundancy, multiple MOV based modular HCBs have been proposed in the literature [86], [87].

Improvements in the HCB performance can also be realized using an auxiliary commutation circuit consisting of energy-storage elements to inject a current opposing the fault current. The counter-current injection forces a zero-crossing in the fault current which provides the opportunity for ZCS turn-off of the switch and isolate the faulted path. This category of circuit breakers is known as forced commutation or counter-current circuit breakers (CCCB). A typical forced commutation HCB is shown in Fig. 1.7(c) which retains the hybrid circuit breaker section of Fig. 1.7(b) along with an LC circuit, where the capacitor C_c is pre-charged. Once the fault is detected, thyristor T_c is triggered; the capacitor discharges through commutation inductor L_c opposing the MCB current I_m and forces the opening of MCB contacts around the current zero-crossing. Following the MCB turn-off, stored inductive energy is dissipated in the MOV. CCCB topologies using mechanical air-blast breakers or SF6 breakers have

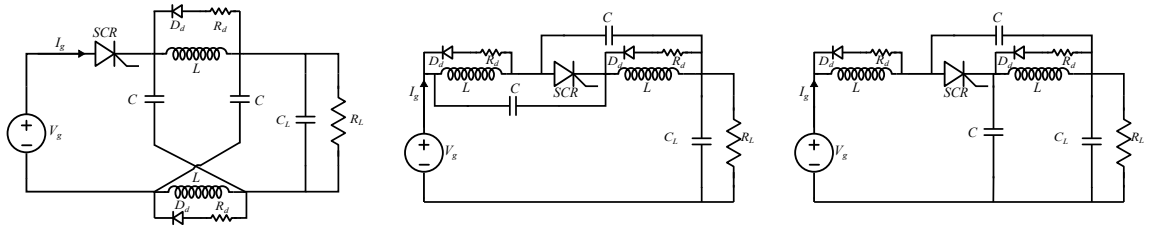


Figure 1.8: Z-source circuit breakers. (a) Classical. (b) Parallel. (c) Series.

been investigated since the 1970s [88]-[92].

The counter-current injection in a CCCB depends on the resonance of the inductor and the capacitor of the auxiliary commutation circuit. Some of the HCB designs use the self-oscillation of the LC network to build up the counter-current and force the current zero [56], [93]. This type of HCB is known as the passive resonance circuit breaker (PRCB). The current commutation in a PRCB always depends on the arc voltage and the interruption time can be in several milliseconds, which makes PRCBs an unsuitable option for subsea DC systems. Other forced commutation breakers use the charged capacitor with switching networks to provide much faster fault interruption; these breakers are categorized as active resonance circuit breakers (ARCB) [94]-[106]. The auxiliary switching network in ARCBs can be implemented by thyristors [96]-[99], IGCTs [100], [101], spark gap bridge [102] or IGBTs [103]-[105]. However, in most ARCB implementations, the MCB is opened first and the counter-current injection is utilized to extinguish the resulting arc. Arc formation reduces the lifetime of the MCB. Also, pre-charging the capacitor requires external circuitry increasing the capital cost.

Counter-current based commutation has also been applied for SSCBs which use thyristor as the main power switch [63], [64], [107]. A distinct subset of counter-current SSCBs is known as the Z-source circuit breaker (ZSCB). A ZSCB consists of an SCR and an impedance source network of inductors and capacitors. Three basic ZSCB

topologies, namely classical, series and parallel ZSCBs are shown in Fig. 1.8(a)-(c). The classical ZSCB [108] limits the source side feed to the fault but does not provide common ground between the DC source and load. The parallel ZSCB [109] incorporates a common ground. However, fault feed from the source increases significantly. The series ZSCB [110] alleviates both of these issues. It also provides a low-pass frequency response, which is advantageous for interfacing DC-DC converters. From these three basic topologies, several unidirectional and bidirectional Z-source DCCBs have been derived [111]-[115].

ZSCBs exhibit fast, autonomous fault response, thereby reducing the requirement of sensing and control circuits. Also, the fault interruption is almost instantaneous, the response time being equal to the reverse recovery time of the SCR. However, the Z-source network is sensitive to load disturbances causing spurious tripping of the breaker. The design of ZSCBs is also influenced by the minimum fault ramp rate. Moreover, the conduction loss in the SCR limits the operation of ZSCBs at high power. To increase efficiency, ZSCBs have been implemented using ultra-fast mechanical switches as the main breaker [116]. However, the turn-off process of the mechanical switch incurs oscillations, necessitating a varistor branch for overvoltage suppression.

Magnetic coupling of transformers or coupled inductors can be utilized for counter-current breakers. A coupled inductor circuit breaker (CICB) has been illustrated in [117]. The auxiliary network consists of the secondary winding of a coupled inductor and a commutation capacitor. The primary winding is in series with the SCR. During a fault, the capacitor discharges through the secondary winding. The reflected capacitor current in the primary winding opposes the fault and forces the SCR to turn off. Several ZSCBs in DC microgrid protection use this approach [118]-[120]. However, all of these coupled-inductor based topologies suffer the same spurious tripping issues as the conventional ZSCBs. Coupled inductor based commutation has also been implemented

for HCBs [121]-[125]. The induced counter-current extinguishes the arc generated due to MCB opening. Nonetheless, arcing reduces the operating life of the HCB which might not be optimal for subsea implementation.

1.4 Review of DEH Power Supplies

Direct electric heating (DEH) is a cost-effective solution to prevent hydrate formation in subsea production pipelines. The principal objective of a DEH system is to generate a heating effect in the form of ohmic loss. Two distinct DEH solutions have been explored over the last two decades by the subsea industries. They are (1) DEH for wet insulated pipelines (DEH-WIP) and (2) DEH for pipe-in-pipe (DEH-PIP) [133].

1. *DEH-WIP*: This DEH technique was developed earlier and is widely used for subsea production. The schematic of a DEH-WIP system is shown in Fig. 1.2. As a portion of the single-phase current is circulated through the seawater, the heating efficiency of DEH-WIP is low.

2. *DEH-PIP*: This technique was developed for the production pipelines insulated by another outer pipe. The pipeline is longitudinally split into several segments. An external source circulates current through each segment, operating as a closed single-phase circuit, to generate heat. DEH-PIP exhibits higher heating efficiency.

Despite the difference in the operation, every DEH system is electrically equivalent to a single-phase AC network with RL load. These DEH systems suffer from a poor power factor due to the predominantly inductive impedance of the pipe. Consequently, large reactive power is required for a very long pipeline, which leads to a high VA rating of the topside source. Additionally, balancing transformer and reactive compensation units are needed, affecting the OPEX and the power density. Hence, future

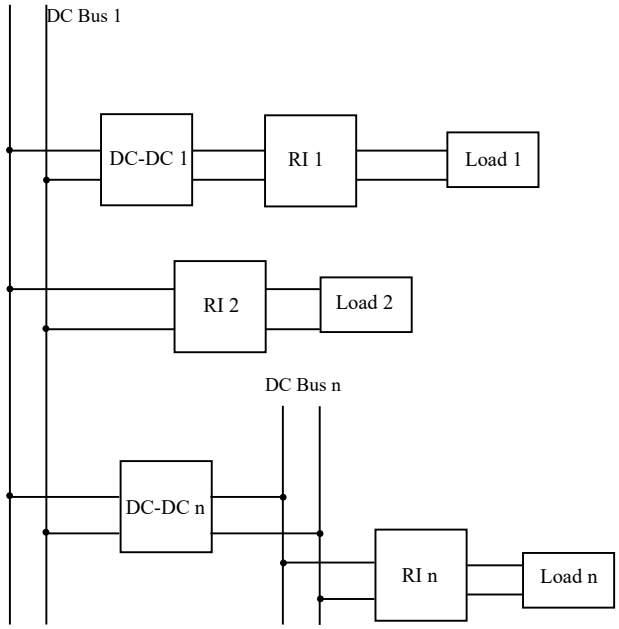


Figure 1.9: Resonant inverter-based DEH network

DEH systems should focus on replacing the external ac source and provide reactive compensation through power electronic solutions.

A DEH system based on single-phase modular multilevel converters (MMC) has been proposed in [138]. Although, an MMC is capable to handle large power, charging and voltage balancing of sub-module capacitors are challenging. Moreover, external reactive compensation is still required. An alternate solution is using resonant inverters (RI) fed from the subsea DC distribution grid. An RI can operate as a high-frequency ac source with in-built reactive compensation by the resonating elements. For a large-scale DEH system, multiple RIs can be interfaced from the subsea DC bus through step-down DC-DC converters, as shown in Fig. 1.9.

1.4.1 Review of Resonant Inverters for Heating Applications

The equivalent electrical model of a DEH system is a single-phase ac network with a lumped RL load. The model is analogous to induction heating (IH) and wireless

power transfer (WPT) systems. However, the resistance variation in a DEH network is comparatively small. A DEH system requires an alternating current of almost constant amplitude to maintain a constant temperature in the pipeline flow. Also, compensating the large load inductance is a priority to minimize the source side VA rating and improve the efficiency of power transfer.

The most common RI topologies used in IH application are series and LCL resonant inverters. A series resonance inverter (SRI) has a load-independent voltage transfer characteristics and can provide zero voltage switching (ZVS) over the entire operating range [142]-[143]. However, the SRI is not suitable for providing a regulated current output. On the other hand, the LCL resonant inverter (LCLRI) has found wide utilization in high-frequency induction heating due to its current regulation and short-circuit protection properties [144]-[148]. However, the part-load efficiency of the LCLRI is low due to large circulating current [150]-[151]. Moreover, the tank current gain is dependent on the ratio of tank inductance to load inductance [145]. This indicates that the input side VA rating is not optimized over the entire load range.

Reactive compensation of coil inductance has been extensively explored in WPT [139]-[141]. The basic compensation topologies can be classified as series, parallel, and series-parallel. The input voltage increases in the series compensation, whereas the parallel compensation increases the input current. The series-parallel tank network provides the best possible compensation as the input VA rating is minimized. An LCCL-LC resonant converter has been investigated for the high-frequency omnidirectional wireless charging application [148], [149]. The LCCL tank structure compensates the primary coil inductance. It achieves a load-independent, constant primary current with ZVS which is conducive to meet the objectives of a DEH system.

1.5 Research Contributions

This dissertation proposes novel HVDC power distribution architectures and protection topologies suitable for electrification of long-distance and deep-water subsea O&G fields. Besides, a novel technique for heating the subsea pipes based on a constant-current output resonant inverter to prevent the forming of hydrates in the pipes has been presented.

In the first part, three modular HVDC power T&D architectures are presented for supplying subsea VSD loads. Proposed T&D architectures mitigate the reactive power issues of AC architectures and minimize voltage sag for long step-out distances. Besides, the modular configuration with individual feeder protection improves the reliability of operation. The DC transformer (DCX) based architecture exhibits fault tolerance and added redundancy. A real-time simulation model of the proposed architecture is developed in the Typhoon HIL platform to illustrate its operation during steady-state and fault.

In the second segment, a family of novel zero current switching hybrid DC circuit breakers is proposed. Proposed HCBs utilize counter-current injection from a series resonant network formed by one winding of a coupled inductor and a charged capacitor. Arcless breaking for a mechanical circuit breaker can be realized due to zero-current turn-off. The proposed HCBs exhibit a fast fault response (5-30 μs). Also, the proposed HCBs mitigate the requirement of varistors for overvoltage suppression. Two 300 V, 25 A laboratory prototypes have been developed to evaluate the performance of the proposed HCBs. The bidirectional embodiment of the proposed HCBs are also presented, and the fault interruption capability is experimentally verified using the laboratory experimental units. The concept of coupled inductor assisted Zero-current switching is further extended to propose two modular DC circuit breakers for the

range extension of fault interruption capability and reduction of fault response time. Instead of a single commutation circuit, multiple series resonant circuits using half-bridge switch modules are utilized for counter-current injection, which reduces the footprint of passive elements. A 100 V, 15 A experimental prototype is developed to achieve the current interruption in the range of 2-10 μs.

In the third section, an LCCL resonant inverter is developed as a constant-current regulator for direct electric heating of subsea pipelines. The proposed LCCLRI operates at the peak tank current gain and supplies a load-independent high-frequency sinusoidal current of constant amplitude. Tank impedance is tuned to realize ZVS of the inverter switches. A SiC MOSFET based 1 kW experimental prototype is built to demonstrate the operation of the LCCLRI as a constant current regulator.

1.6 Dissertation Outline

This dissertation is summarized by the following points.

1. Three modular HVDC T&D architectures for electrification of long tie-back subsea fields are presented in chapter 2. The proposed architectures employ individual DC distribution feeder protection using fast DC circuit breakers. The series-connected transformer based ring distribution is used in architecture-II. Architecture-III realizes solid-state transformers in the distribution grid using cascaded single-active bridge DC-DC converters, which further enhances the redundancy of the subsea grid. The fault-tolerant operation of the proposed DC architectures is validated by a real-time simulation model in the Typhoon HIL platform.

2. Three coupled inductor-based zero-current switching hybrid DC circuit breakers

(CIHCB) for fault interruption in the subsea DC distribution feeder are proposed in chapter 3. Proposed CIHCBs achieve resonant circuit assisted arcless commutation of the main switch. The commutation capacitor is charged to twice the DC bus voltage without any pre-charging circuit. The commutation network is modified in CIHCB 2 and 3 to realize a unipolar voltage profile of the capacitor, thus allowing the use of high energy-density electrolytic capacitors and easy reclosing. This chapter illustrates a design guideline for the CIHCBs. The performance of the proposed CIHCBs is verified using two 300 V, 25 laboratory-based prototypes.

3. Chapter 4 presents three bidirectional coupled inductor-based HCBs (BCIHCB) for fault protection in future offshore grid with renewable generation. The proposed topologies realize arcless DC breaking. BCIHCB 3 is suitable for reclosing operation as the capacitor voltage profile is DC. The current commutation in the bidirectional HCBs is verified by experimental results in a 6 kW prototype unit.

4. Two novel modular DC circuit breakers are proposed in chapter 5 for fast interruption of high fault levels. The modular breakers extend the CIHCB principle for two secondary-side commutation networks. Parallel connection of the primary windings effectively doubles the reflected counter-current. Thus a faster fault response compared to the CIHCBs is realized. The second topology using series-connected primary windings is particularly useful for preventing commutation failure due to insufficient reverse-recovery time in thyristor-based implementations. A 1 kW laboratory prototype is developed to evaluate the response speed of the modular breakers. Experimentally measured response time varies between 2-15 μs.

5. An LCCL resonant inverter is proposed in chapter 6 for the direct electric heating application. The proposed LCCL-RI operates at the peak current gain to source a single-phase alternating current of constant amplitude. The resonant tank network provides reactive compensation for the highly inductive DEH load. The LCCL-RI achieves load-independent current regulation and features inherent short-circuit protection. The tank impedance is tuned for realizing ZVS of the power switches. The operation of the LCCL-RI is evaluated using a SiC MOSFET based 1 kW prototype.

6. Chapter 7 summarizes the dissertation by highlighting the principal features of the research. A brief discussion on the future scope of research concludes the dissertation.

Chapter 2

Modular HVDC Power Transmission Architectures

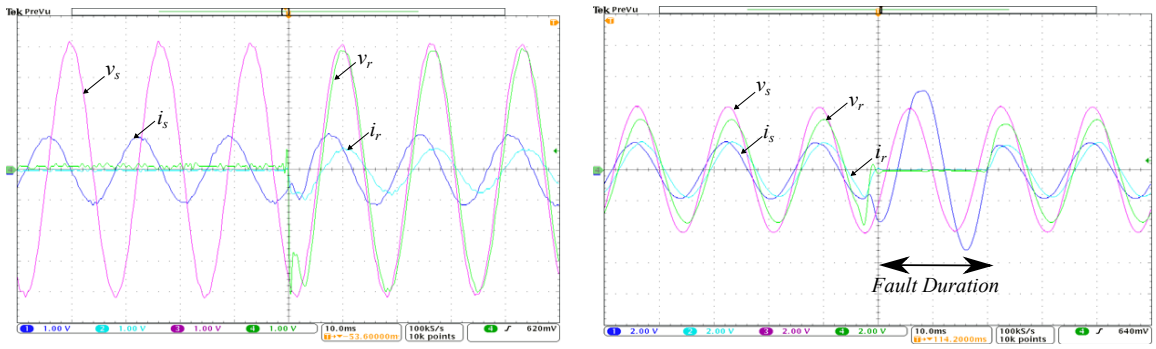
2.1 Introduction

In chapter 1 the current trends in subsea electrification on the long-distance transmission of electric power from the onshore grid to the subsea loads are discussed. HVAC transmission is presently being used for subsea power delivery. However, as discussed in section 1.2, HVAC transmission shows a limitation in long-distance power transmission in terms of reactive power requirement. The type-III HVAC architecture can be deployed for a tie-back length up to 100 km [11], [20] with the installation of reactors and STATCOMs which increases the overall operating cost. Consequently, HVAC may not realize economic benefits for longer tie-back subsea fields. The alternate solutions to HVAC are the LFAC and HVDC technologies. Both these technologies can mitigate the cable charging reactive power problem. The degree of reactive power reduction can be measured using the steady-state VA demand from the onshore source.

Apart from reactive power, another criterion to characterize a transmission system is to evaluate the effect of transients on the power source. Several transient events can occur in a subsea power network, such as inrush, load-side faults, variable torque demand by the subsea VSD loads, etc. The corresponding effects on the source side can be used to quantify the reliability of the power system. For reliable and efficient operation, the adverse effects of these transients on the power quality of the onshore source should be minimum. Hence, a brief comparison of the transmission technologies

Table 2.1: Submarine Power Cable Parameters

V_r	I_r	A_c	R_{ac}	L	C
36 kV	467 A	240 mm^2	0.098 Ω/km	0.33 mH/km	0.30 $\mu F/km$



(a) (b)

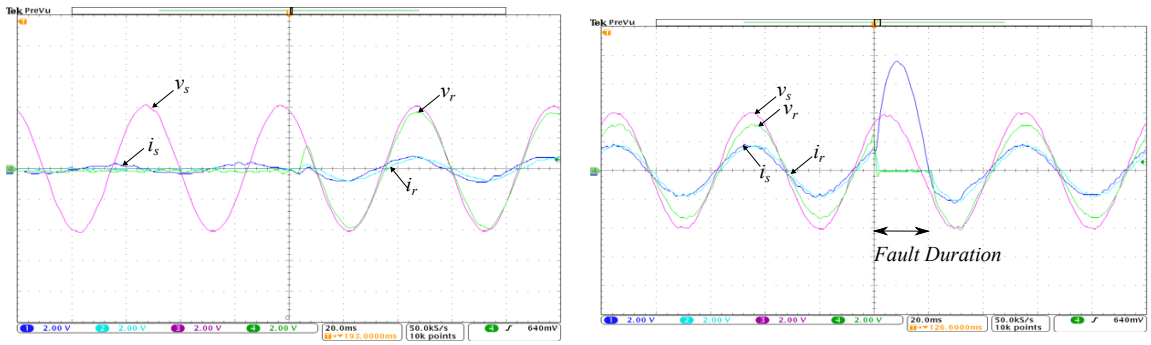
Figure 2.1: Effects of load transients on the HVAC system. (a) Start-up. (b) Fault.

is provided in section 2.2 in terms of the aforementioned criteria to determine the optimum choice for long-tie back subsea power systems.

2.2 Comparison of Subsea Power Transmission Technologies

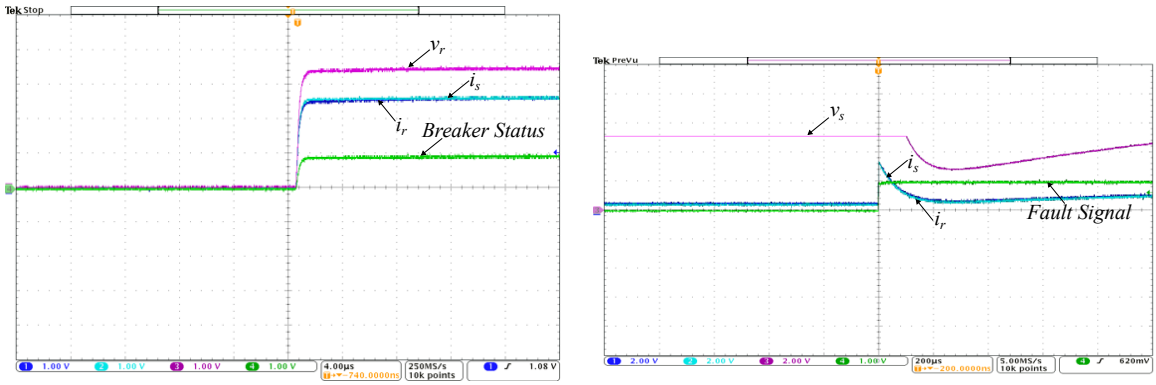
Real-time simulation models are developed in the RTDS platform to compare the source side responses of AC and DC transmission. The onshore grid is represented by a 3 phase AC source. Three principal types of power transmission networks are simulated, namely: HVAC (60 Hz), LFAC (20 Hz) and HVDC. The line voltage of the AC source is selected as 36 kV. A 10 MW constant power load is interfaced to the source by a 100 km long submarine cable whose parameters are taken from the Nexan's submarine cable data [41] and are given in Table 2.1.

Fig. 2.1(a)-(b) show the sending and receiving end voltages and currents of one phase in the 60 Hz HVAC system, during system start-up and a load-side short-circuit fault, respectively. It is observed from Fig. 2.1(a) that the sending end current i_s



(a) (b)

Figure 2.2: Effects of load transients on the LFAC system. (a) Start-up. (b) Fault.



(a) (b)

Figure 2.3: Effects of load transients on the HVDC system. (a) Start-up. (b) Fault.

is substantially large even before the load power flow. The no-load value of i_s is the measure of the cable charging current. This is also indicated during actual power delivery by the phase and amplitude difference between i_s and the receiving end current i_r. Also, due to the inductive network impedance, the difference between the sending and receiving end voltages (v_s and v_r) is substantially large at full load. This voltage sag reduces operating efficiency and may even cause stability issues for long step-out distances. During a momentary line-to-ground (L-G) fault, a substantial increase in the amplitude of i_s is observed in Fig. 2.1(b).

The effects of identical transients in the 20 Hz LFAC system are presented in Fig. 2.2. The pre-energization value of i_s, which also denotes the charging current,

is much lower in the LFAC system, as seen from Fig. 2.2(a). This can also be realized from equation 1.1 as the reactive power Q_c (a measure of the charging current) is directly proportional to the system frequency f. Moreover, the series impedance of the LFAC network is lower compared to the HVAC system, which reduces the voltage sag. These features make the LFAC system an attractive proposition for long step-out. However, the low system impedance of LFAC results in a larger fault level. This is evident from Fig. 2.2(b), where an L-G fault causes a much higher initial peak of i_s. The increase in fault level demands an AC switchgear of higher current rating and larger footprint.

The HVDC system does away with the line charging current, as can be seen in Fig. 2.3(a) that both i_s and i_r are identical. The voltage drop at the receiving end is the lowest among all three architectures, as it depends only on the series resistance of the network. The short-circuit fault response of the HVDC system (Fig. 2.3(b)) shows a sharp rise in i_s magnitude, which requires fast-acting DC circuit breakers. Otherwise, the HVDC system exhibits superiority for long-distance transmission over its AC counterparts.

Besides the evaluation of reliability from the source side transient response, the reliability of the subsea distribution stage should also be assessed for selecting the optimum T&D architecture. Conventional HVAC or LFAC power architectures are hub-and-spoke types that use the subsea step-down transformer as the sole power receiving port. Consequently, the distribution reliability is low as the system is vulnerable to a transformer failure. Ring-type architectures using series-connected transformers [14] or the MSDC system [30] can improve the distribution reliability. However, both these architectures do not incorporate any DC feeder protection, which limits their application for multiple interconnected subsea loads. Moreover, the MSDC architecture employs cascading of several DC-DC and DC-AC stage. This demands a large number

of wet-mate connectors which might affect the system reliability adversely.

To address the above issues, this chapter proposes three modular HVDC T&D architectures for long tie-back subsea systems. The transmission stage is HVDC which interfaces the subsea DC distribution bus through a submarine cable. In HVDC-II, the AC ring distribution using series-connected high-frequency (HF) transformers is adopted to facilitate point-of-load operation [35]. The distribution reliability is further improved in HVDC-III which replaces the HF transformers by HF DC-DC converters (DCX). The series connection of these DCX realizes a solid-state transformer (SST). The SST structure enables a fault-tolerant subsea system, i.e., the power distribution can continue at a reduced rating during a fault. A real-time simulation model of the proposed architecture is developed in the Typhoon-HIL platform to demonstrate the fault-tolerant operation.

2.3 Modular HVDC T&D Architectures

The proposed HVDC T&D architectures for the subsea power grid are illustrated by Fig. 2.4 to Fig. 2.6. The onshore AC source voltage is converted to the transmission level DC voltage through a step-up transformer and a front-end AC-DC conversion stage. The subsea HVDC cable transmits power to the subsea DC distribution bus.

2.3.1 HVDC-I

The HVDC-I architecture, shown in Fig. 2.4, interfaces multiple subsea VSDs (DC-AC converters) from the DC distribution bus through separate DC feeders [35]. Each DC feeder incorporates a DC circuit breaker, which can isolate the feeder within 500 μs in the event of a fault. The DC distribution bus can continue to feed power through the healthy feeders, hence partial power operation is possible.

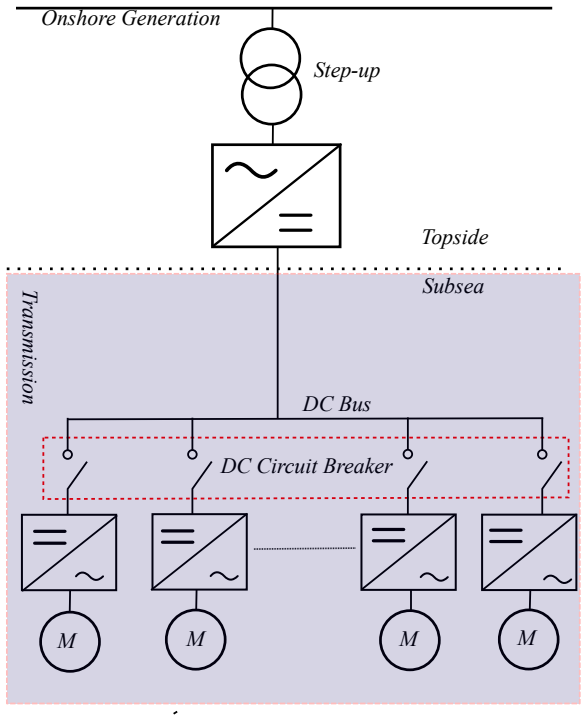


Figure 2.4: Proposed HVDC-I Architecture

2.3.2 HVDC-II

The second architecture, named HVDC-II, employs an AC ring distribution based on series-connected high-frequency transformers (XFMR) as shown in Fig. 2.5 [35]. Each DC feeder from the subsea distribution bus interfaces an inverter which generates high-frequency AC voltage. This inverter feeds multiple series-connected transformers. Each transformer caters to its VSD loads through an AC-AC power conversion stage, which converts the high-frequency AC voltage to variable frequency AC voltage.

The HF operation of the combined inverter and transformer stage could realize a smaller system size compared to a conventional hub-and-spoke type distribution. In addition, the ring distribution facilitates point-of-load operation where the AC-AC power conversion stage is placed very close to the pump and compressor motors. As a result, AC feeder length is minimized which reduces the VA rating of each HF

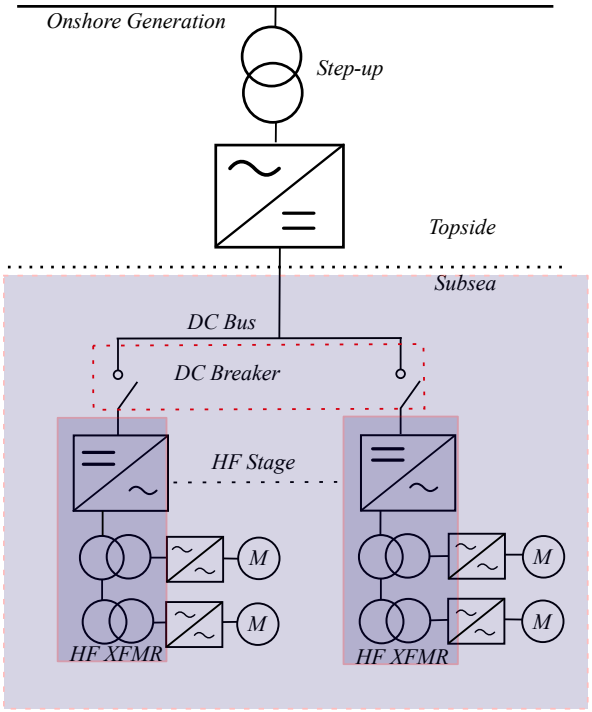


Figure 2.5: Proposed HVDC-II Architecture

transformer. HVDC-II retains the DC breaker based feeder protection. The current controlled operation of series-connected transformers further enhances the reliability by allowing partial load operation within a single distribution feeder.

2.3.3 HVDC-III

The HVDC-III architecture, shown in Fig. 2.6, extends the concept of series-connected ring architecture for a DC distribution system. The HF transformers are replaced by HF isolated DC-DC converters. Each DC-DC converter provides a step-down of DC voltage from the distribution bus level to the input level of a VSD. As a result, the DC-DC converter is also termed as a DC transformer (DCX). The cascading of multiple DCX realizes an SST that is capable of handling high power as well as providing compensation to the disturbances in the subsea distribution grid.

The DC link voltage of each VSD is regulated by the corresponding DCX operating

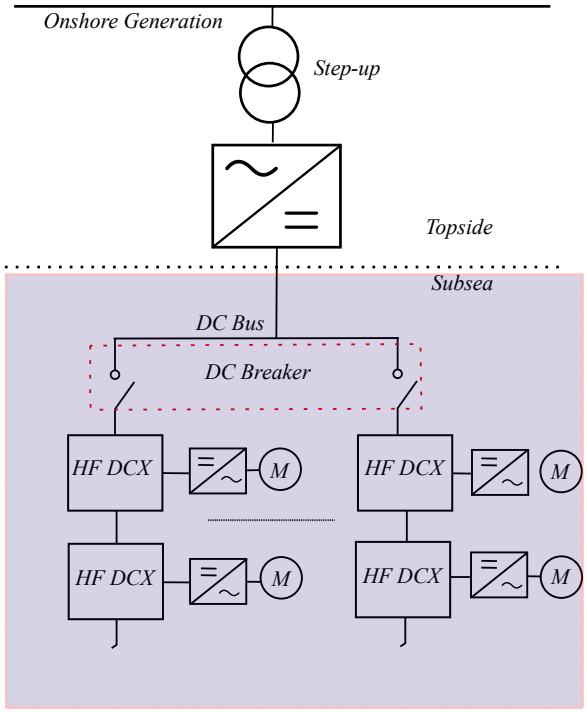
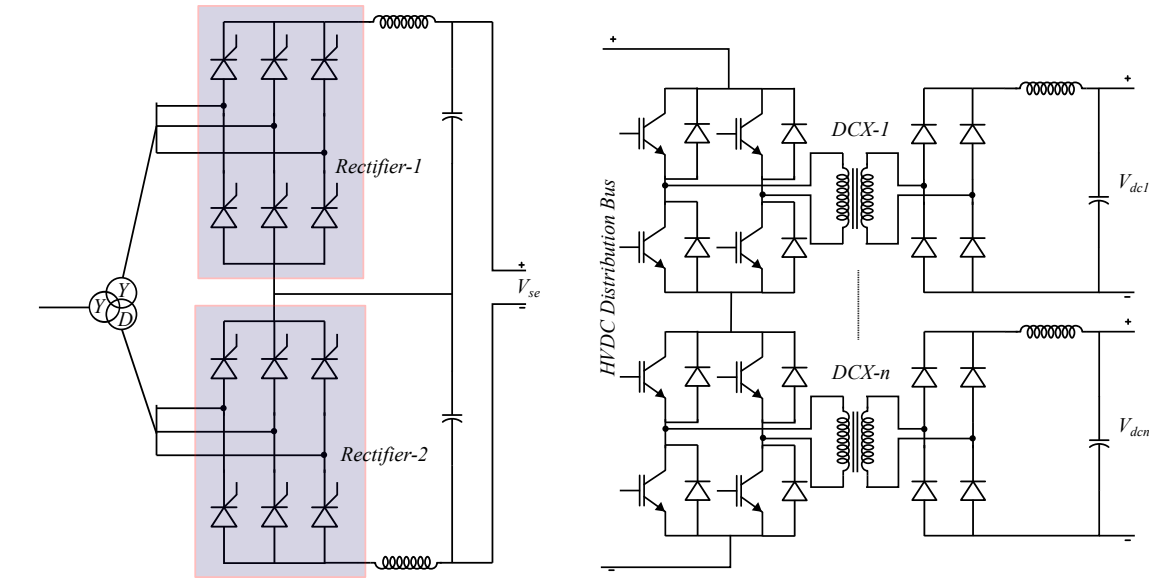


Figure 2.6: Proposed HVDC-III Architecture

with voltage-mode control. During a load-side fault, the DCX reduces its output voltage to zero. Although this causes an increase in the input DC voltage of a healthy DCX, the voltage controller still regulates its output voltage at the nominal value. Thus a single SST can operate in partial power during fault which shows the fault-tolerant capability. The feeder level protection is incorporated by DC breakers.

2.4 Technology Description of the HVDC Architectures

The proposed HVDC architectures employ power conversion stages in the sending and receiving end of the HV transmission cable for delivering the electrical power generated onshore to the subsea VSD loads. The sending end power conversion unit consists of a high-voltage front-end converter. On the other hand, the receiving end power conversion stage comprises of the VSD converters and the SST (for HVDC-III). Moreover, all the architectures include a DC circuit breaker for each DC distribution



(a) (b)

Figure 2.7: Components of HVDC architecture. (a) Front-end converter. (b) SST.

feeder, which will be discussed in detail in the following chapters.

2.4.1 Sending End Power Converter

The sending end power conversion unit consists of the generator bus side transformer and a front-end converter (FEC). The most common topology for the FEC is a diode-based or thyristor-based unidirectional multi-pulse rectifier as the existing subsea systems do not encounter bidirectional power flow. However, for future subsea microgrids integrating offshore renewable sources, regeneration is a common occurrence that demands active rectifier topologies. In this chapter, a 12 pulse bridge rectifier is considered for the onshore rectification, as shown in Fig. 2.7(a). The step-up transformer is a three winding, star-star-delta transformer which provides 30^o phase shift between the input and output line-to-line voltages. The phase-shift between the star and the delta winding currents eliminates lower order harmonics to maintain grid current THD within the specified limit [44], [45].

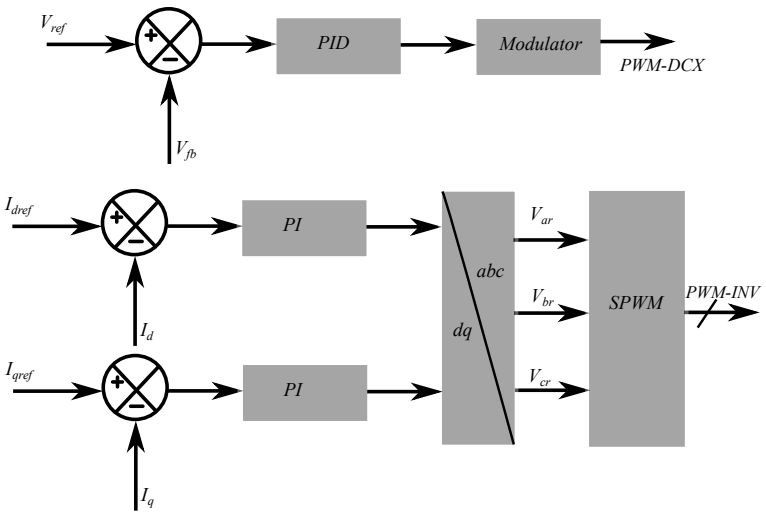


Figure 2.8: Subsea DC Control Architecture

2.4.2 Receiving End Power Converter

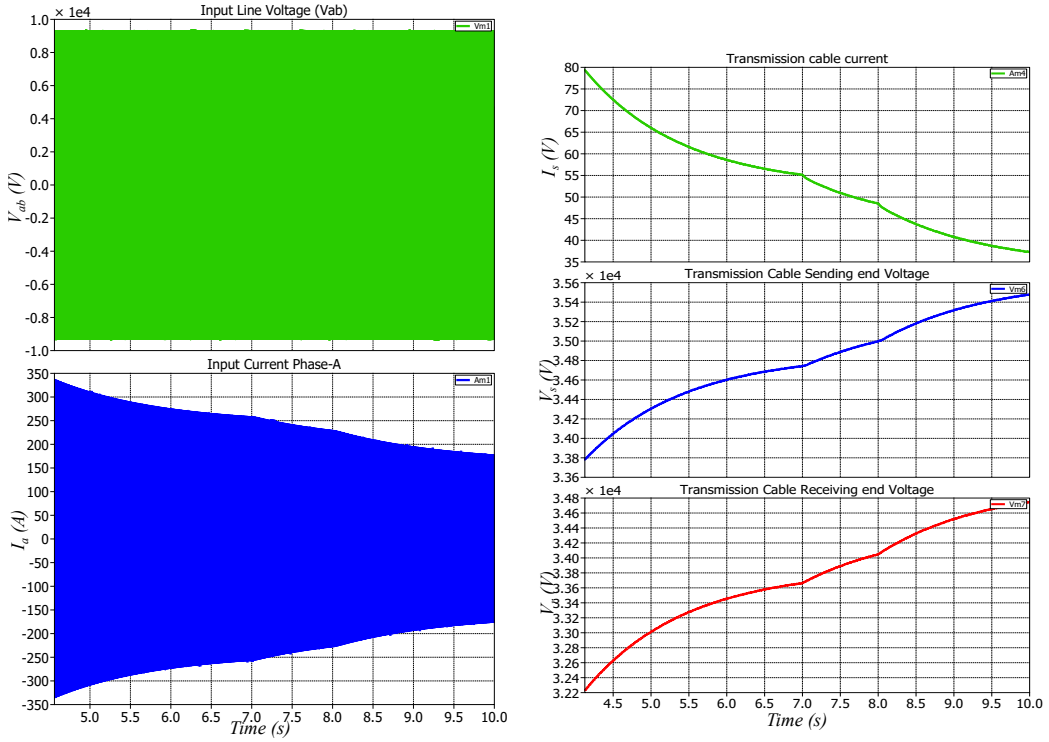
The step-down of the transmission level DC voltage in HVDC-III architecture is accomplished by the SST comprising of multiple cascaded DCX. Fig. 2.7(b) shows the SST structure with two DCX connected in series. Each DCX is an isolated single active-bridge DC-DC converter, having an intermediate high-frequency transformer between the power inversion and rectification stage. A current-fed interleaved single-active bridge converter has been previously proposed for subsea distribution [38]. However, the current-fed structure requires a snubber capacitor across the secondary winding for seamless current commutation. The single active-bridge DCX is a voltage-fed converter that provides smoother switch commutation with better voltage regulation performance and transformer utilization.

The power inversion stage cascaded to each DCX consists of a 2-level voltage source inverter. Each inverter is modulated using standardized current-mode control in the $d-q$ reference frame. In the event of an inverter side fault, the corresponding DCX reduces its output voltage to zero. The rest of the converters in the SST structure can

still regulate their output.

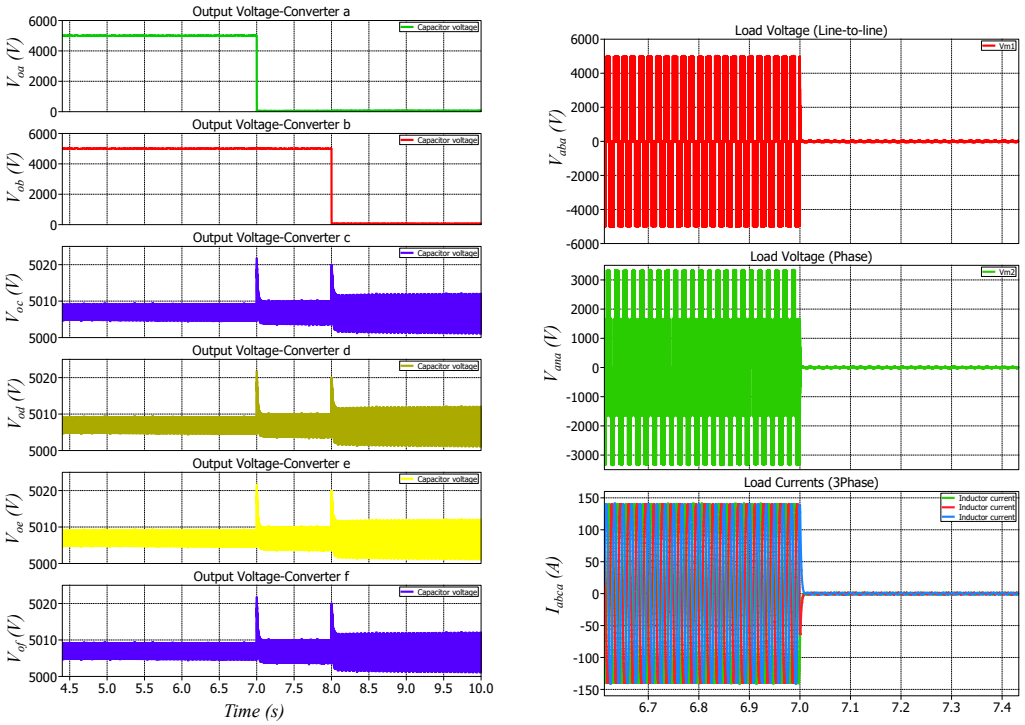
2.4.3 Subsea Control Architecture

In the HVDC-III architecture, the module level controls of DCX and VSD inverter are identical for all the units. The DCX module implements a simple voltage mode control, where the DC link feedback V_{fb} is compared to the reference voltage V_{ref} coming from the master controller. The error voltage is fed to a PID controller for generating modulation signals for active bridge switches. As the voltage-loop PID controller regulates the inverter DC link voltage, the inverter is modulated using the $d-q$ reference frame based current control. The current references (I_d, I_q) are generated from the master controller. The module-level control architecture is shown in Fig. 2.8.



(a) (b)

Figure 2.9: Simulation results for start-up. (a) Onshore grid. (b) Transmission cable.



(a) (b)

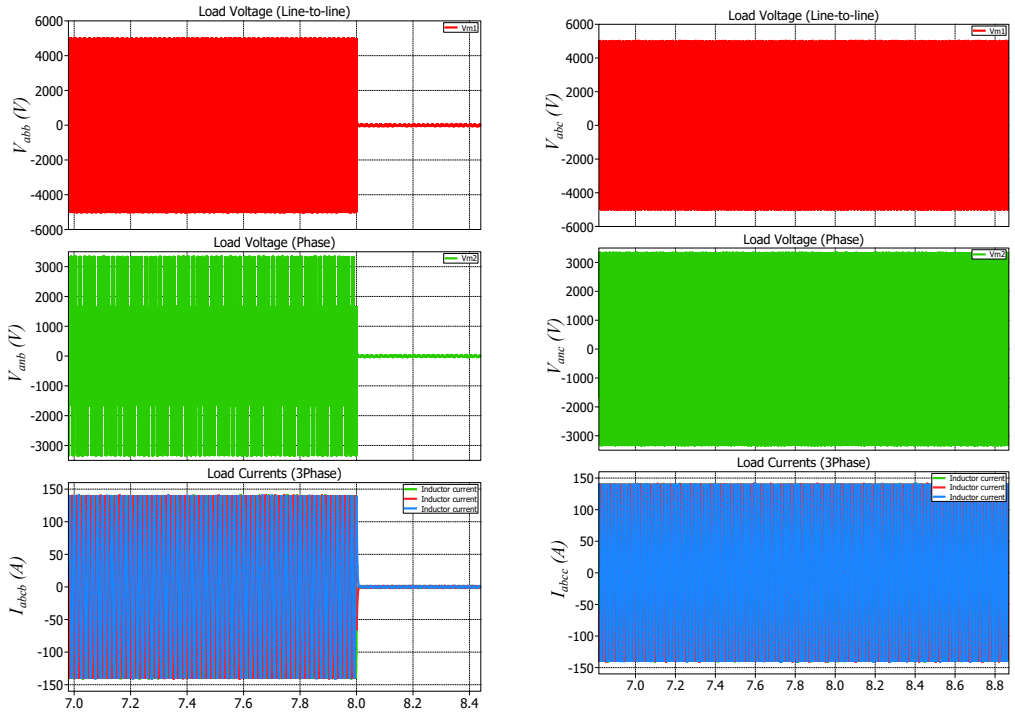
Figure 2.10: Simulated fault transients. (a) All DCX. (b) Converter a.

2.5 Simulation Results

The operation of the HVDC-III architecture with SST is first verified by an offline simulation model in PLECS. The onshore generator is modeled as a 3-phase grid with a 6.6 kV line-to-line voltage. The generator bus voltage is boosted using a 3-winding transformer in star-star-delta configuration to supply a 12 pulse diode rectifier, which is the front-end converter (FEC). The FEC provides a 36 kV high voltage DC at its terminal. Following the DC filter, the FEC is interfaced with a 100 km long HVDC submarine cable. The cable parameters are listed in Table 2.1. The cable is modeled using series π sections, which is the most widely utilized model as it simplifies the load flow equations in the simulation [39], [40]. Other cable modeling techniques such as the Bergeron's traveling wave model or the frequency dependent model could be used

[42]-[43] but at the cost of increasing the simulation run time and complexity. The DC distribution side SST is modeled with 6 cascaded DCX, and each DCX supplies a 3-phase inverter which denotes the subsea VSD load.

Fig. 2.9 shows the voltages and currents in the sending end and the transmission stage for the system start-up. Fig. 2.9(a) shows that the grid-side phase current experiences a large inrush and then decays to a much lower steady-state value. The phase-shifting YD transformer connection reduces the grid current harmonics. Fig. 2.9(b) depicts the transient transmission cable current and the sending and receiving end voltages. The voltage drop at the receiving end is around 2%, which is quite low due to only the series resistance drop.

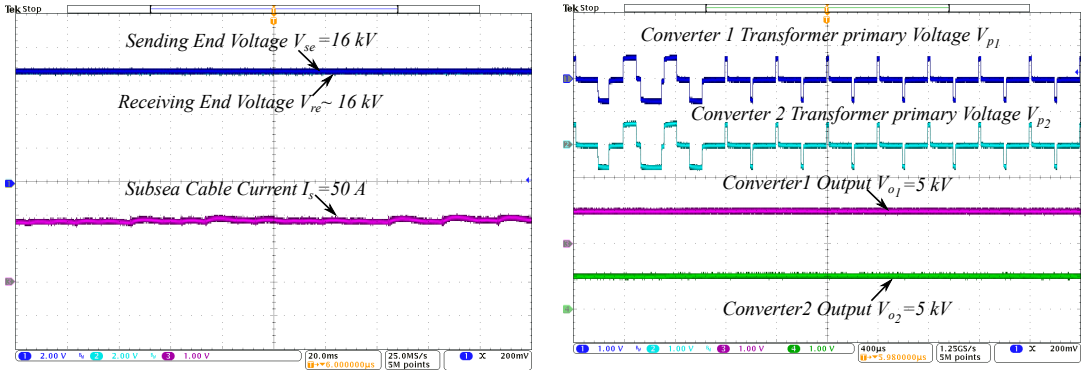


(a) (b)

Figure 2.11: Simulated fault transients. (a) Converter-b. (b) Converter-c.

Fig. 2.10 demonstrates the fault-tolerant operation of the distribution SST. The six series DCXs are termed as converter-a to f. At t=7 s, a short-circuit fault occurs at the

load of converter-a. Fig. 2.10(a) shows that the converter-a reduces its output voltage to zero, which in turn provides a soft-turn off of its associated inverter, as the inverter phase currents are reduced to zero (Fig. 2.10(b)). The rest of the DCX can maintain their output voltages after an initial transient. Converter-b experiences a load-side fault at t=8 s, as depicted in Fig. 2.11(a). Nonetheless, the inverter interfaced from converter-b undergoes soft turn-off. The number of healthy modules decreases to 4, but the individual dc link voltages are still constant, as seen from Fig. 2.10(a). Fig. 2.11(b) shows the inverter-c output voltages and phase currents, which do not experience any deviation even when two consecutive faults occur. Consequently, the SST operation is proven to be fault-tolerant.

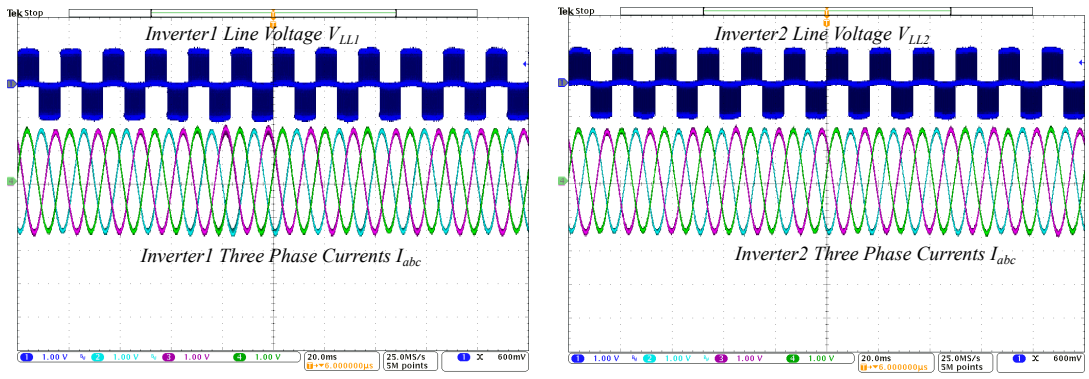


(a) (b)

Figure 2.12: Steady-state HIL results. (a) Transmission cable. (b) DCX. Scale: V_{se}, V_{re}, V_{o_1}, V_{o_2},V_{p_1},V_{p_2} = 5 kV/div. I_s=25 A/div.

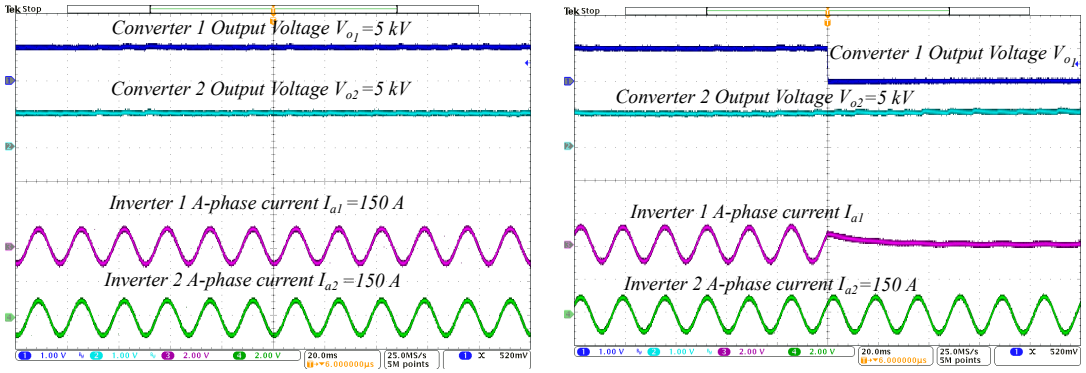
2.6 Hardware-in-the-Loop Evaluation

The proposed SST based HVDC-III architecture is further verified in a hardware-in-the-loop (HIL) based real-time simulation model. The model is identical to the simulation model described in section 2.5, except the SST is formed by 2 series-connected



(a) (b)

Figure 2.13: Steady-state HIL results. (a) Inverter 1. (b) Inverter 2. Scale: V_{LL1},V_{LL2} = 5 kV/div. I_{abc} = 100 A/div.

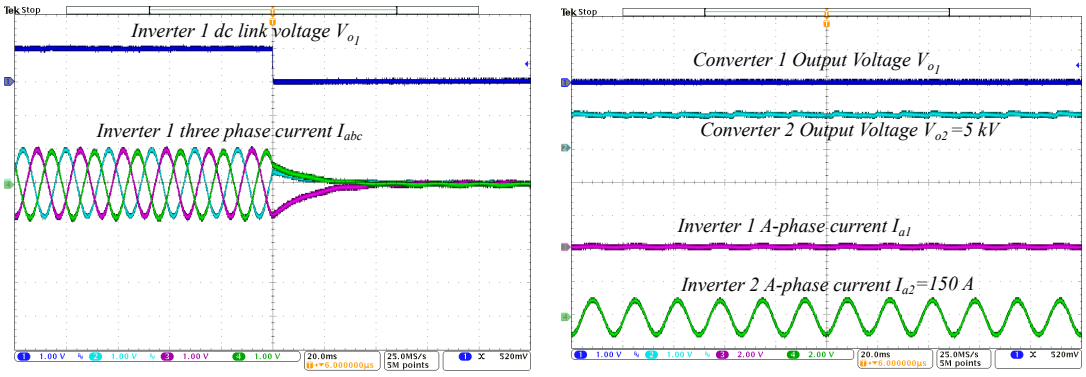


(a) (b)

Figure 2.14: Fault response of DCX. (a) Before fault. (b) During fault. Scale: V_{o_1}, V_{o_2} = 5 kV/div. I_{abc} = 200 A/div.

DCX due to the switch limitation of the Typhoon-HIL platform. Still, this SST structure represents the worse-case redundancy, as a fault in one of the converters would represent 50% outage. The downscaled steady-state waveforms are shown in Fig. 2.12 and Fig. 2.13.

Fig. 2.12(a) indicates that the sending end and receiving end voltages are almost identical and the voltage sag is minimum. Fig. 2.12(b) shows the transformer voltage and output voltage of the DCX 1 and 2, which are maintained at 5 kV. The narrow duty cycle of the transformer primary voltage indicates a high step-down gain. The



(a) (b)

Figure 2.15: Fault response of DCX. (a) During fault. (b) Post fault. Scale: V_{o_1}, V_{o2} = 5 kV/div. I_{abc} = 200 A/div.

load-side inverter waveforms are shown in Fig. 2.13(a)-(b), respectively.

The waveforms during converter 1 fault are shown in Fig. 2.14 and Fig. 2.15. Fig. 2.14(a) depicts the pre-fault dc link voltages and the inverter phase currents. In Fig. 2.14 (b), the same waveforms during the fault are shown. Converter 1 output voltage is forced to zero due to the voltage controller, while inverter 1 also undergoes a soft shutdown. Nonetheless, DC-DC converter 2 and its corresponding inverter still maintain their output. Fig. 2.15(a) illustrates the soft turn-off of converter 1 with the gradual reduction of 3-phase currents. Fig. 2.15(b) presents the post-fault waveforms where converter 2 still maintains reduced power operation under 50% outage.

2.7 Discussion

This section presents a detailed discussion of the performance of the HVDC architectures, in terms of FOMs such as reactive power, operating efficiency, harmonics, the number of wet-mate connectors and cost.

2.7.1 Reactive Power

The HVDC-II architecture employs an intermediate DC-AC conversion stage after the distribution bus. Hence, ac feeders are required to supply subsea loads. However, the ring-type distribution facilitates point-of-load connection which reduces the reactive power requirement. Source VA rating is further reduced in HVDC-III due to DC distribution. The simulation results in section 2.5 reveal that the 3-phase grid supplies 2.02 MVA while the DC side power is 1.98 MW. This indicates that the reactive power requirement is only 20% of the active power rating, compared to even 120% in a standard HVAC architecture. Reactive VAr can be further reduced by using a 24 or 36-pulse converter or an active front-end converter based on high voltage SiC devices.

2.7.2 Efficiency

The modular DC architectures improve transmission efficiency. The simulated sending end and receiving end voltages of the transmission cable exhibit a deviation within 2%. Hence the transmission losses do not exceed 2% of the system rating. The efficiency can be further improved by the developments in DC submarine cable technology.

2.7.3 Harmonics

The switching operation of power converters, such as the front-end rectifier, VSDs, and intermediate converters generate harmonic currents which can be injected into the transmission cable. The harmonic currents can create resonance in the cable which causes undesired distortion of the voltage waveform [44], [45]. The harmonic current injection can be minimized by using multi-pulse rectifiers. The HVDC architectures presented in this chapter employ a 12 pulse front-end-converter, which shifts the current

harmonic spectrum to

$$h_i = 12k \pm 1, \tag{2.1}$$

where k represents a positive integer. With the phase-shifting YD transformer, the 11th, 13th, 17th, etc. harmonics would be canceled. Grid side THD can be further improved by an active rectification stage onshore, which also minimizes the harmonic injection in the line-charging capacitance of the cable. The SST structure in the distribution side facilitates the current-mode control of VSD inverters, which improves the harmonic performance in the distribution side.

2.7.4 Wet-mate Connector Requirements

The use of HVDC transmission for subsea application has been restricted due to the limited voltage ratings of wet-mate connectors and penetrators [47], [48]. Wet-met connectors have the highest probability of failure, thus directly affecting the reliability of subsea systems. With modular architecture and SST deployment, the size of the subsea power converters can be reduced. This facilitates the operation of multiple converters within a single pressure compensated unit, consequently reducing the number of subsea connectors. Moreover, the modular structure reduces the voltage rating of each converter, enabling the use of low voltage wet-mate connectors and penetrators.

2.7.5 Cost

For long step-out operation, the methods to compare cost analysis of HVAC, LFAC, and HVDC systems have been presented in the literature [33]-[34]. LFAC exhibits a cost-effective range over HVDC transmission due to lower converter cost [33]. However, for increasing transmission power, the cost-benefit of LFAC is not realized due to the increase in conductor material. The HVDC converter cost is further reduced by

employing cascaded converters of significantly lower power rating, instead of a large single converter unit.

2.8 Summary

This chapter proposes three HVDC architectures for power distribution to subsea loads which exhibit the following advantages over conventional AC architectures.

- The reactive power requirement from the source is minimized.
- Transmission voltage sag is reduced, which aids long-distance power transmission.
- The modular distribution architecture using solid-state transformers increase the system redundancy and provides fault-tolerance.
- High-frequency operation increases the power density and reduces the converter footprint.
- Modular converters with reduced voltage ratings enable the use of low-voltage wet-mate connectors and penetrators.

The fault-tolerant performance of the proposed SST-based architecture has been demonstrated in a hardware-in-the-loop environment.

2.9 Publications

1. A. Ray, K. Rajashekara and H. Krishnamoorthy, "Novel HVDC Power Transmission Architectures for Subsea Grid," Offshore Technology Conference, 2019.

Chapter 3

Hybrid Circuit Breaker Topologies for Subsea HVDC Grid Protection

3.1 Introduction

The Modular HVDC architectures improve the subsea power transmission by mitigating the reactive power issues and enhancing system reliability, as discussed in Chapter 2. Nonetheless, all of the proposed HVDC architectures require fast fault protection of the distribution feeders. A short-circuit fault in a DC system provides the following challenges for a reliable switchgear design.

- A load short-circuit in a DC system results in a fast ramp-up of the system current from its steady-state value which may cause the instantaneous fault current to surpass the system safety limit within a few milliseconds.
- The fault level in a DC system is much higher compared to its AC counterpart, as the steady-state fault current is only limited by the series resistance of the DC network.
- The fault current in AC systems can be quenched at its zero-crossing. DC fault does not encounter any current zero-crossing.

Therefore, DC circuit breakers should be capable of fast interruption and isolation of the fault to prevent damage to the DC system. Also, the steady-state conduction loss of

a DC circuit breaker should be minimum to eliminate the forced cooling requirement, which is critical for a subsea design. The review of existing DC circuit breakers in section 1.3 shows that solid-state circuit breakers (SSCB) provide fast fault interruption but do not meet the power loss criteria.

Hybrid circuit breakers (HCB) use mechanical breakers (MCB) for current conduction. As mechanical breakers have a very low on-state voltage drop, the conduction loss is greatly reduced. However, the conventional hybrid circuit breaker suffer from slow current commutation [53], [74]-[75]. Also, as the current commutation process involves arcing across the moving contacts, the life-cycle of an HCB is greatly reduced. HCBs with a fast semiconductor switch in the series path can improve the commutation time significantly [76]-[81]. However, the conduction loss substantially increases due to a higher on-state voltage drop of the semiconductor switch.

The commutation performance of an HCB is improved by counter-current circuit breakers (CCCB) which use current injection from a resonating LC circuit to oppose the fault current and force the commutation of the series path breaker. CCCBs can be classified as passive resonance circuit breakers (PRCB) and active resonance circuit breakers (ARCBs). PRCBs use self-oscillation of the LC circuit [56], [93]. The counter-current build-up is slow and the fault response time can be several milliseconds, which is not desirable for HVDC protection.

Current commutation is significantly faster in ARCBs using pre-charged capacitors with switching networks for a faster build-up of counter-current [94]-[106]. The counter-current can also be generated using the magnetic coupling of transformers [121]-[125]. However, the ARCB mechanism involves arc generation due to the opening of MCB long before current zero-crossing. The counter-current is used to quench the arc. Consequently, the operating life-cycle is low, as in the case of conventional HCBs. The pre-charging of the capacitor requires external circuitry which increases

the installation cost. Also, a parallel varistor or snubber circuit is required for ARCBs to dissipate the stored inductive energy. Varistors are bulky and susceptible to thermal failure.

To address these issues, a coupled inductor based hybrid HVDC circuit breaker (CIHCB) is proposed in this chapter. The proposed circuit breaker uses a counter-current injection from a switched resonant LC circuit to realize a ZCS turn-off of the main breaker [126]. The switched-resonant LC circuit consists of the secondary winding of a coupled inductor, a charged capacitor, and a discharging switch. Discharging of the capacitor induces a counter-current in the primary winding to drive the fault current to zero. Arcless breaking operation is realized due to the ZCS of the main breaker. The resonant capacitor is charged to twice the DC source voltage using the circuit elements which eliminates the pre-charging requirement. The proposed CIHCB does not require parallel varistors or snubber circuits for network demagnetization. Two modified topologies are also presented in this chapter for obtaining a unipolar voltage profile of the commutation capacitor [129]. The commutation performance of the CIHCBs has been verified by simulation as well as by experiment using 300 V, 25 A prototype units.

3.2 Coupled Inductor Hybrid Circuit Breaker 1

The proposed hybrid circuit breaker topology 1 (CIHCB1) is shown in Fig. 3.1 [129]. The primary winding $1 - 1'$ of the coupled inductor L is in series with a mechanical switch MS. The secondary winding $2 - 2'$ is connected to a capacitor C and a discharging switch T_1. Another switch T_2 is used for the resonant charging of the capacitor from the DC source. As the CIHCB operation guarantees a natural commutation of both T_1 and T_2, they are implemented by thyristors. L has a 1:1 turns ratio

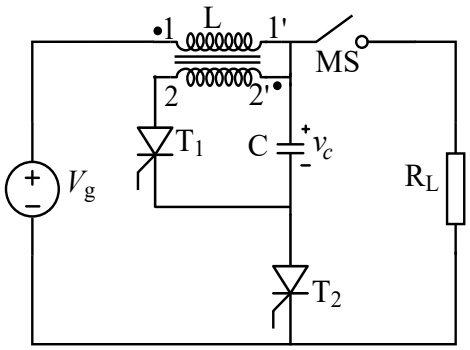


Figure 3.1: Coupled inductor ZCS hybrid DC circuit breaker

for the prototype design, although a n:1 turns ratio can be utilized as well where n >1. Fig. 3.2 depicts the four operating modes of the proposed HCB, while corresponding waveforms are shown in Fig. 3.3.

3.2.1 Mode I ($t_0 < t < t_1$)

At $t = t_0$, T_2 is turned on to create a series resonance of the primary winding $(1-1')$ self-inductance and capacitor C, as shown in Fig. 3.2(a). MS is maintained in open position during this period to ensure that the capacitor has sufficient stored energy for the fault interruption before the actual power flow. Capacitor voltage and current in this mode are given by

$$v_c(t) = V_g(1 - \cos\omega_o t) \quad \text{and} \tag{3.1}$$

$$i_c(t) = \frac{V_g}{Z_o}\sin\omega_o t, \tag{3.2}$$

where $Z_o = \sqrt{\frac{L_s}{C}}$ and $\omega_o = \sqrt{\frac{1}{L_s C}}$ are the characteristic impedance and the resonant frequency of the charging circuit, respectively. L_s represents the self-inductance of the primary winding $1 - 1'$ and is given by

$$L_s = L_m + L_{lk}, \tag{3.3}$$

where L_m and L_{lk} are the mutual and the leakage inductance of winding $1 - 1'$, respectively. T_2 is naturally commutated at the capacitor current zero crossing instant

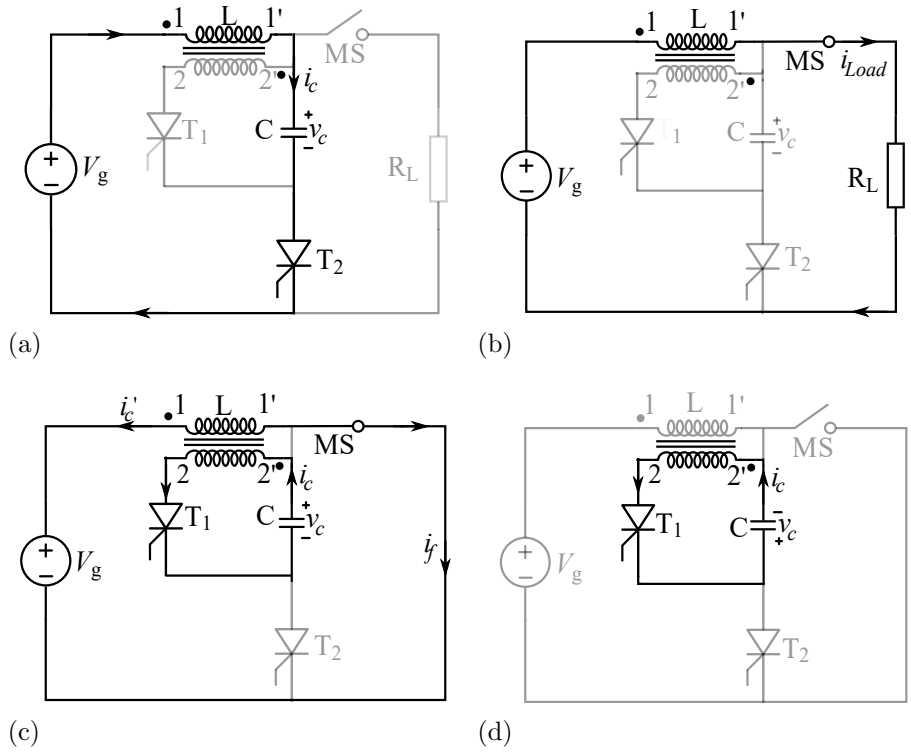


Figure 3.2: Operating modes of CIHCB1. (a) Mode I: capacitor charging. (b) Mode II: MS closed. (d) Mode III: MS commutation. (d) Mode IV: reverse charging of capacitor.

$t = \dfrac{\pi}{\omega_o}$, as shown in Fig. 3.3. Meanwhile, C is charged to a voltage of $2V_g$.

3.2.2 Mode II ($t_1 < t < t_2$)

Following the turn-off of T_2, MS is closed at $t = t_1$ to commence power flow from the DC source to load (Fig. 3.2(b)). The other switches remain off during this mode.

3.2.3 Mode III ($t_2 < t < t_3$)

During a short-circuit fault, the fault current i_f rises and reaches a preset level I_d at $t = t_2$. T_1 is turned on at this instant which enables the commutation capacitor C to discharge through the secondary winding $2-2'$. The capacitor current i_c induces an

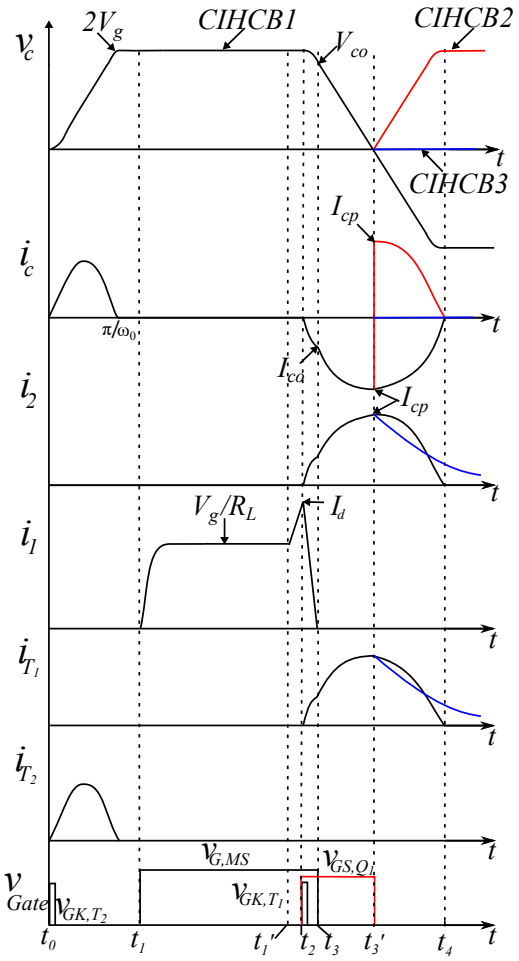


Figure 3.3: Operating waveforms of CIHCB1 (black), CIHCB2 (red) and CIHCB3 (blue).

equal and opposite current in the primary winding $1 - 1'$. Current conduction paths are highlighted in Fig. 3.2(c). The induced primary current forces i_f to zero at $t = t_3$. The opening signal for MS is provided at this instant. The fault extinguishes naturally due to the absence of any active source. The stored inductive energy is utilized for reverse-charging the capacitor, hence the snubber requirement is mitigated.

3.2.4 Mode IV ($t_3 < t < t_4$)

The commutation capacitor continues to discharge through the secondary winding $2 - 2'$ after ZCS turn-off of the main breaker. The discharging circuit is a series

resonant network comprising of the self-inductance of winding $2-2'$ and the capacitor C. Capacitor voltage and current equations are expressed as

$$v_c(t) = V_{co}\cos\omega_o(t-t_3) - Z_o I_{co}\sin\omega_o(t-t_3) \quad \text{and} \tag{3.4}$$

$$i_c(t) = \frac{V_{co}}{Z_o}\sin\omega_o(t-t_3) + I_{co}\cos\omega_o(t-t_3), \tag{3.5}$$

where V_{co} and I_{co} are the instantaneous capacitor voltage and current at the current zero crossing instant ($t = t_3$). As the capacitor current in the discharging mode is considered negative, the absolute values of V_{co} and I_{co} should be used in (3.4) and (3.5). The capacitor voltage v_c transits from positive to negative value after the instant $t = t_3'$ in this mode, as shown in Fig. 3.3. Mode IV ends with the natural commutation of T_1.

3.3 Coupled Inductor HCB 2 with Unipolar Capacitor Voltage

The commutation capacitor C in CIHCB1 is subjected to a bipolar voltage profile, as seen from Fig. 3.3. This implied that electrolytic capacitors cannot be used for the physical implementation of C. Electrolytic capacitors exhibit the highest energy density among different types of capacitors, which helps to reduce the capacitor stack size in the HVDC application. Two circuit breaker topologies, which ensure a DC voltage profile of the commutation capacitor, are presented in Fig. 3.4 (a) and (b).

The coupled inductor HCB2 (CIHCB2), shown in Fig. 3.4(a), is derived by augmenting an H-bridge structure to HCB 1 [129]. Commutation capacitor C functions as a voltage source to the H-bridge, whose output terminals are connected to the terminals of $2-2'$ through T_1. H-bridge devices are realized by IGBT with an antiparallel diode for bidirectional current conduction. Operation of CIHCB2 in four sub-intervals have been illustrated in Fig. 3.5 and Fig. 3.3.

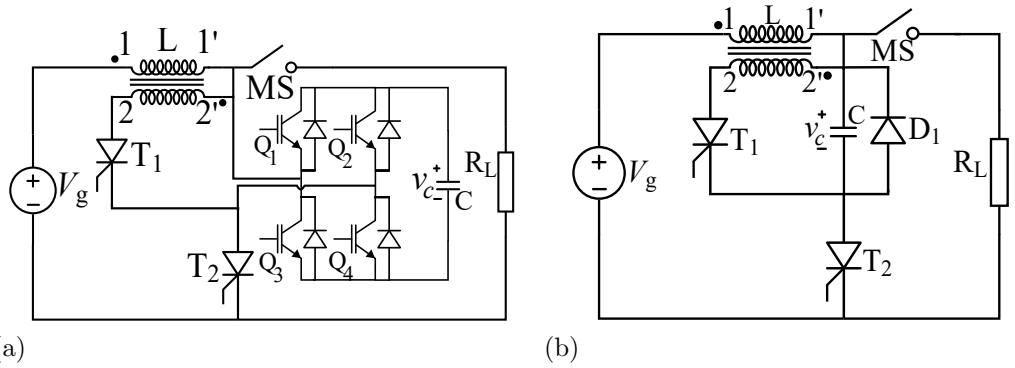


Figure 3.4: Modified CIHCB Topologies. (a) CIHCB2. (b) CIHCB3.

3.3.1 Mode I, II ($t_0 < t < t_2$)

T_2 is turned on while maintaining the H-bridge switches (Q_1-Q_4) in off state. Fig. 3.5(a) shows the charging current path through winding $1-1'$, antiparallel diodes of Q_1 and Q_4, and T_2. Capacitor C is charged to twice the DC bus voltage at the turn-off instant of T_2 ($t = t_1$). Capacitor charging equations are given by equations (3.1)-(3.2). The normal power flow commences in mode-II, which is identical to that of CIHCB1 and shown in Fig. 3.5(b).

3.3.2 Mode III ($t_2 < t < t_3$)

T_1, Q_1 and Q_4 are turned on upon the detection of fault, which results in the discharge of C through winding $2-2'$, shown in Fig. 3.5(c). Due to the opposite magnetic coupling, induced current pulse i_c' in the primary winding forces a zero-crossing of MS current to ensure ZCS turn-off of mechanical switch.

3.3.3 Mode IV ($t_3 < t < t_4$)

Capacitor C continues to discharge through the path $Q_1 - 2'2 - T_1 - Q_4$ following the opening of MS until its voltage v_c falls to zero. The voltage zero-crossing instant

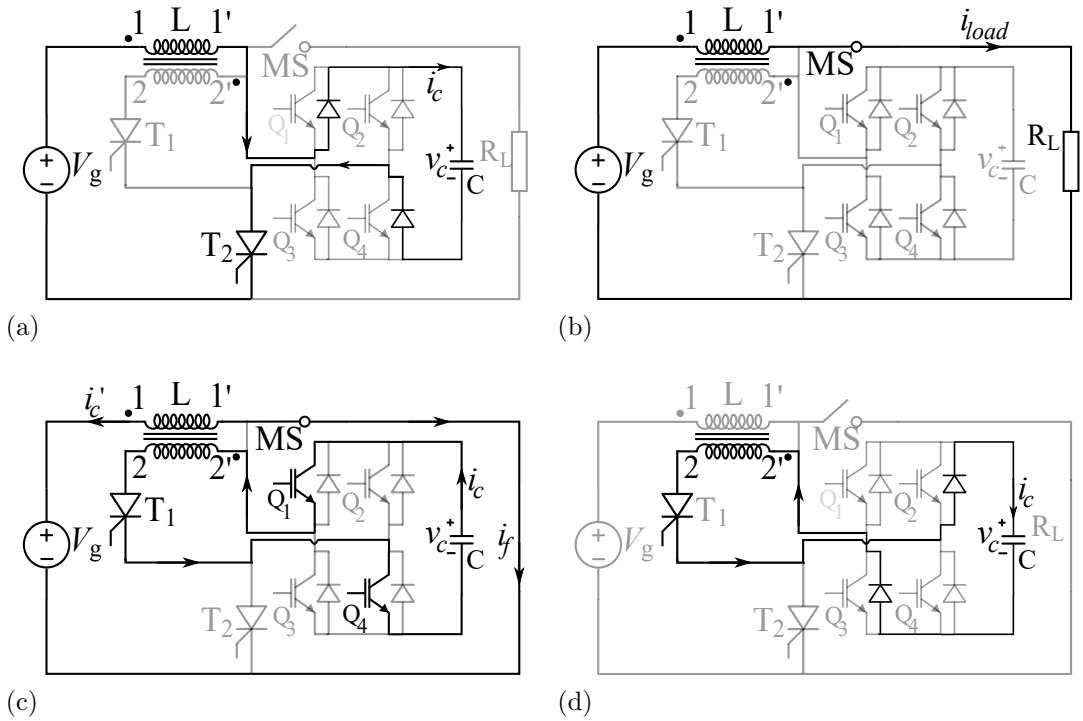


Figure 3.5: Operating modes of CIHCB2. (a) Mode I: capacitor charging. (b) Mode II: MS closed. (d) Mode III: MS commutation. (d) Mode IV: re-charging of capacitor.

$(t = t_3')$ is detected and the gate-pulses of Q_1 and Q_4 are subsequently revoked. As the secondary current i_2 is at its peak at this instant, the stored energy in the secondary winding drives the antiparallel diodes of Q_2 and Q_3 into conduction. As a result, capacitor is charged to a positive voltage until T_1 and the diodes commutate at $t = t_4$ (Fig. 3.5(d)). The capacitor voltage and current in the discharging mode $(t_3 < t < t_3')$ are governed by equations (3.4) and (3.5), while capacitor charging mode $(t > t_3')$ is represented by

$$v_c(t) = Z_o I_{cp} \sin \omega_o (t - t_3') \quad \text{and} \tag{3.6}$$

$$i_c(t) = I_{cp} \cos \omega_o (t - t_3'), \tag{3.7}$$

where I_{cp} denotes the peak value of the current flowing through the capacitor and the secondary winding $2 - 2'$.

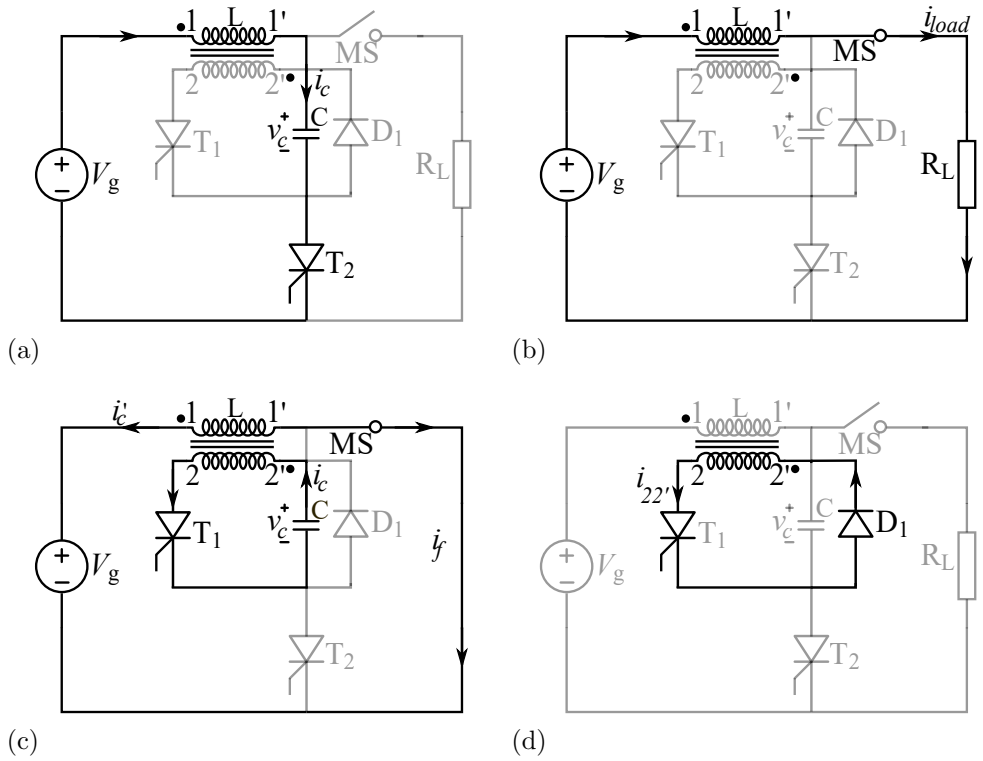


Figure 3.6: Operating modes of CIHCB3. (a) Mode I: capacitor charging. (b) Mode II: MS closed. (d) Mode III: MS commutation. (d) Mode IV: capacitor clamping.

3.4 Coupled Inductor HCB 3 with Capacitor Clamping

A DC voltage profile of the commutation capacitor can also be obtained by inserting a clamping diode D_1 across C in an antiparallel configuration. The modified HCB, designated as coupled inductor HCB 3 (CIHCB3), is shown in Fig. 3.4(b) [129]. The operation of CIHCB3 is identical to CIHCB1 in the first three sub-intervals, as shown in Fig. 3.6(a)-(c). Beyond the zero-crossing instant of the capacitor voltage ($t = t_3'$), D_1 is forward biased, as shown in Fig. 3.6(d). D_1 clamps the capacitor voltage to the forward voltage drop of the diode. Subsequently, secondary current i_2 continues to circulate through the path $D_1 - 2'2 - T_1$ and exponentially decays to zero due to the on-state resistance of the devices as well as the winding resistance. Secondary current

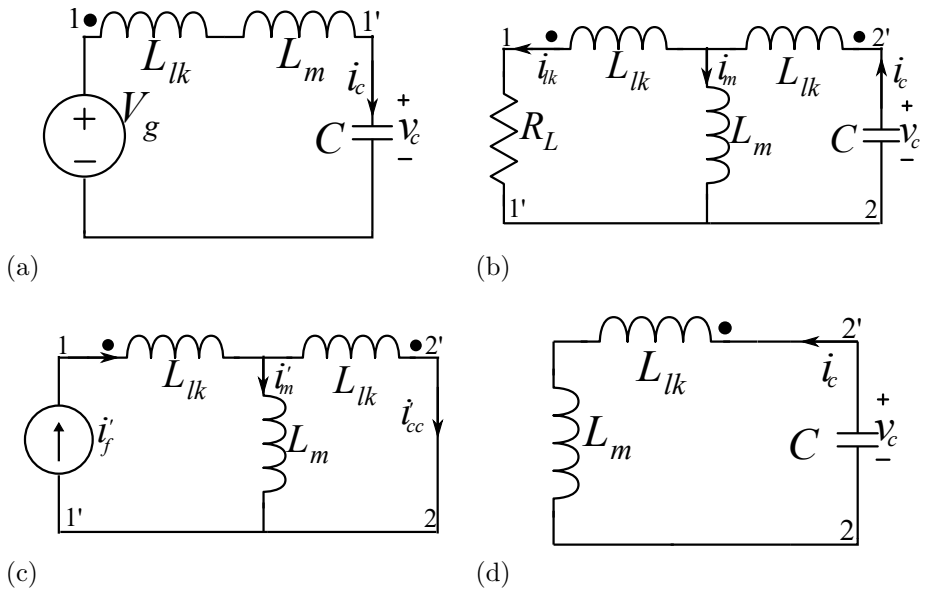


Figure 3.7: Equivalent circuits of CIHCB1 for operating modes. (a) Charging. (b) Counter-current. (c) Reflected fault current. (d) Post commutation.

i_2 can be expressed as

$$i_2(t) = |I_{cp}|e^{-\frac{R_d}{L_s}t}, \tag{3.8}$$

where R_d represents the total resistance of the discharging circuit.

3.5 Analysis and Design of Coupled Inductor HCB Topologies

3.5.1 Design Equations of Coupled Inductor HCB

The commutation performance of the proposed CIHCBs is defined by the amplitude and rise time of the counter-current pulse, which in turn is dependent on the design of the coupled inductor and commutation capacitor. The design equations can be obtained by simplified equivalent circuits referred to secondary winding in each mode. Fig. 3.7 represents these modal equivalent circuits of CIHCB1. The other two topologies have identical equivalent circuits, except in mode-IV. It is assumed that the primary and secondary winding have identical leakage inductance L_{lk} for a 1:1 turns ratio.

3.5.1.1 Capacitor Charging Mode

The equivalent circuit during the capacitor charging mode is shown in Fig. 3.7(a). The charging circuit is a series resonant circuit excited by a DC source V_g, as explained in section 3.2 using equations (3.1) and (3.2). The peak capacitor current and the capacitor voltage at the end of the charging cycle are found to be

$$I_{c_{p,c}} = \frac{V_g}{Z_o} \quad \text{and} \qquad\qquad V_{c,f} = 2V_g. \tag{3.9}$$

Capacitor peak charging current $I_{c_{p,c}}$ can be reduced by increasing Z_o value, which is possible by either increasing L_s or reducing C.

3.5.1.2 Fault Commutation Mode

Equivalent circuit of CIHCB1 in this mode, shown in Fig. 3.7(b), is constructed for interrupting any generic load current. Parameter R_L in the circuit represents the load resistance. The short-circuit fault is a subset of load current interruption for $R_L = 0$. The capacitor discharging current in the circuit of Fig. 3.7(b) can be expressed as

$$i_c(t) = -C\frac{dv_c}{dt}, \tag{3.10}$$

where the negative sign in (3.10) is incorporated as the discharging current is considered negative. Equation (3.10) can be re-written in s-domain as

$$I_c(s) = -sCV_c(s) + CV_{c,f}. \tag{3.11}$$

The nodal voltage and current equations in the Laplace domain are given by

$$V_c(s) = sL_{lk}I_c(s) + (sL_{lk} + R_L)I_{lk}(s), \tag{3.12}$$

$$V_c(s) = sL_{lk}I_c(s) + sL_mI_m(s), \quad \text{and} \tag{3.13}$$

$$I_c(s) = I_{lk}(s) + I_m(s). \tag{3.14}$$

Combining (3.12)-(3.14) yields the expression of capacitor voltage

$$V_c(s) = \frac{sL_sR_L + s^2L_{lk}(L_m + L_s)}{sL_s + R_L} I_c(s). \tag{3.15}$$

The mathematical expressions of capacitor current and voltage as the function of pre-fault capacitor voltage $V_{c,f}$ are found using equations (3.11) and (3.15) as

$$I_c(s) = \frac{C(sL_s + R_L)V_{c,f}}{s^3CL_{lk}(L_m + L_s) + s^2CL_sR_L + sL_s + R_L} \quad \text{and} \tag{3.16}$$

$$V_c(s) = \frac{[sCL_sR_L + s^2CL_{lk}(L_m + L_s)]V_{c,f}}{s^3CL_{lk}(L_m + L_s) + s^2CL_sR_L + sL_s + R_L}. \tag{3.17}$$

Equations (3.16)-(3.17) show that the capacitor current magnitude is directly proportional to pre-fault capacitor voltage. Hence, it is imperative to charge the capacitor well above V_g to ensure successful commutation. In the CIHCB topologies, the capacitor is charged to $2V_g$ to maintain this condition. Closed-form time-domain solutions of capacitor voltage and current can be determined for a short-circuit fault by replacing $R_L = 0$ in equation (3.16) as

$$I_c(s) = \frac{CL_sV_{c,f}}{s^2CL_{lk}(L_m + L_s) + L_s}. \tag{3.18}$$

Mutual inductance L_m and leakage inductance L_{lk} can be expressed as the function of self-inductance L_s and the coupling coefficient k as

$$L_m = kL_s \quad \text{and} \qquad L_{lk} = (1 - k)L_s. \tag{3.19}$$

Using (3.19) in (3.18), the expression of capacitor current can be simplified as

$$I_c(s) = \frac{CV_{c,f}}{s^2CL_s(1 - k^2) + 1}. \tag{3.20}$$

Consequently, capacitor voltage is defined by the equation

$$V_c(s) = \frac{sCL_s(1 - k^2)V_{c,f}}{s^2CL_s(1 - k^2) + 1}. \tag{3.21}$$

Equations (3.20) and (3.21) represent a series resonant circuit formed by the capacitor, secondary winding and the leakage inductance of primary winding. Capacitor current and voltage in time domain are represented by

$$i_c(t) = \frac{V_{c,f}}{Z_{o_1}} \sin \omega_{o_1}(t - t_2) \quad \text{and} \tag{3.22}$$

$$v_c(t) = V_{c,f} \cos \omega_{o_1}(t - t_2), \tag{3.23}$$

where Z_{o_1} and ω_{o_1} represent the characteristic impedance and the resonant frequency of this LC circuit and are given by

$$Z_{o_1} = \sqrt{\frac{L_{eq}}{C}} \quad \text{and} \qquad \omega_{o_1} = \frac{1}{\sqrt{L_{eq}C}}. \tag{3.24}$$

$L_{eq} = (1-k^2)L_s$ denotes the equivalent series inductance of the commutation network. It can be inferred from equation (3.22) that counter-current amplitude increases as coupling coefficient $k \to 1$. Moreover, ω_{o_1} increases with reduction in L_{eq} as k approaches unity, which implies reduced rise time, i.e., faster fault interruption.

The counter-induced current i'_{cc} through the leakage branch of the secondary winding due to rising primary current during fault is computed from Fig. 3.7(c) as

$$i'_{cc}(t) = i'_f(t)\frac{L_m}{L_s}. \tag{3.25}$$

When source inductance is not considered in the DC network, the counter-induced current source i_f can be represented as

$$i'_f(t) = \frac{V_g}{L_s}(t - t'_1). \tag{3.26}$$

Superposition of these two circuits, shown in Fig. 3.7(b) and (c), using equations (3.19), (3.22), (3.25) and (3.26) realizes the effective counter-current sourced by the capacitor as

$$i'_c(t) = \frac{V_{c,f}}{Z_{o_1}} \sin \omega_{o_1}(t - t_2) - \frac{kV_g}{L_s}(t - t'_1). \tag{3.27}$$

Consequently, the condition for successful fault current commutation becomes

$$i'_c(t)|_{t=t_3} \geq i_f(t)|_{t=t_3}. \tag{3.28}$$

3.5.1.3 Evaluation of Fault Response Time

The transcendental equation (3.27) can be simplified for a fast fault response considering $\sin \omega_{o_1} t \approx \omega_{o_1} t$. In that case, the condition for MS commutation can be re-written as

$$\frac{V_{c,f}}{Z_{o_1}} \omega_{o_1} (t_3 - t_2) - \frac{kV_g}{L_s}(t_3 - t_1') \geq \frac{V_g}{R_L} + \frac{V_g}{L_s}(t_3 - t_1'), \tag{3.29}$$

which can be simplified using (3.9) and (3.24) as

$$t_f \geq \tau_{eq} + \frac{(1+k)(1-k^2)}{(1-k+k^2+k^3)}(t_2 - t_1'), \tag{3.30}$$

where τ_{eq} is the equivalent time constant of the primary circuit, given by

$$\tau_{eq} = \frac{L_{eq}}{R_L(1-k+k^2+k^3)}. \tag{3.31}$$

$t_f = t_3 - t_2$ is the fault response time. Time instants t_2 and t_1' can be determined from the knowledge of preset current level I_d, whereas coupling coefficient k is a design parameter of the coupled inductor. For $k \to 1$, t_f is greatly reduced.

3.5.1.4 Capacitor Reverse Charging Mode

The terminals of primary winding $1 - 1'$ are open during mode IV due to the current commutation. This results in the equivalent circuit of Fig. 3.7(d). Capacitor discharging equations (3.4) and (3.5) have been presented in section 3.2. V_{co} and I_{co} are computed using (3.22) and (3.23) as

$$I_{co} = \frac{2V_g}{Z_{o_1}} |\sin(\omega_{o_1} t_f)| \quad \text{and} \qquad V_{co} = 2V_g |\cos(\omega_{o_1} t_f)|. \tag{3.32}$$

The peak capacitor current is expressed as

$$I_{cp} = \frac{V_{co}}{Z_o} \sin \omega_o (t_3' - t_3) + I_{co} \cos \omega_o (t_3' - t_3). \tag{3.33}$$

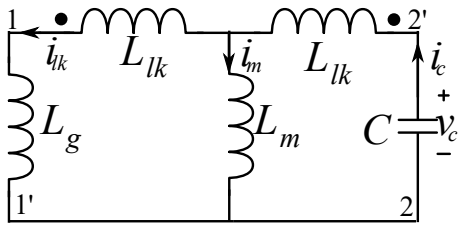


Figure 3.8: Mode III equivalent circuit with source inductance.

Peak capacitor current I_{cp} is an important design parameter for the coupled inductor. It may be noted that for identical circuit parameters, I_{cp} is exactly same for all the three CIHCB topologies. In the case of CIHCB2, the equivalent circuit remains the same as in Fig. 3.7(d) beyond $t = t_3'$, except capacitor current reversal to indicate capacitor charging. The equivalent circuit for CIHCB3 becomes an R-L discharging circuit once the capacitor is clamped by D_1, as explained by equation (3.8).

3.5.2 Effect of Source Inductance on Fault Response

The equivalent circuit during fault commutation interval with a source inductance L_g is shown in Fig. 3.8. From this equivalent circuit, the expression of capacitor current in (3.20) is re-written as

$$I_c(s) = \frac{CV_{c,f}}{s^2 C L_{eq_1} + 1}, \tag{3.34}$$

where the modified equivalent series inductance L_{eq_1} is given by

$$L_{eq_1} = L_s \frac{(1 - k^2 + \frac{L_g}{L_s})}{1 + \frac{L_g}{L_s}}. \tag{3.35}$$

It is observed from equation (3.35) that L_{eq_1} increases for higher value of L_g, which reduces the capacitor current magnitude given by (3.22). This implies a reduction in fault current interruption range as well as increased fault response time of the CIHCBs. The effect of source inductance can be attenuated by selecting self-inductance L_s much larger than L_g so that $\frac{L_g}{L_s} \ll 1$ and $L_{eq_1} \approx L_{eq}$.

3.5.3 Design of Energy Storage Elements

3.5.3.1 Coupled inductor

Principal design parameters for the coupled inductor are the peak and rms currents in the primary and the secondary winding. Peak winding currents are given by

$$I_{1_p} = \max(I_{c_{p,c}}, I_d) \quad \text{and} \qquad I_{2_p} = I_{cp}. \tag{3.36}$$

The rms value of the primary current is $\frac{V_g}{R_L}$. Standard area-product method is employed to design the core and the windings of the coupled inductor.

The design equations reveal that the fault interruption range is enhanced when $k \approx 1$. Therefore, the design effort has been directed to minimize leakage inductance. On the other hand, a larger value of self-inductance reduces the peak current rating and, consequently, the inductor footprint. The C-type silicon steel core is used for laboratory prototype development.

3.5.3.2 Commutation Capacitor

A Large μF value of the commutation capacitor increases stored energy for fault interruption. However, higher capacitance value increases the peak current rating of the passive elements and the switches. Hence, capacitor selection is optimized based on both of these criteria. The capacitor voltage at the end of mode IV for CIHCB1 and 2, respectively, are given by

$$V_{ce} = V_{co} \cos \omega_o (t_4 - t_3) + Z_o I_{co} \sin \omega_o (t_4 - t_3) \quad \text{and} \tag{3.37}$$

$$V_{ce} = Z_o I_{cp} \sin \omega_o (t_4 - t_3'). \tag{3.38}$$

The peak capacitor voltage is defined as $V_{cp} = \max(2V_g, V_{ce})$. Metallized polypropylene film type DC capacitors are used for the laboratory design due to higher peak current

Table 3.1: Simulation Parameters for 36 kV System

Parameters	Symbols	Description
Rated Voltage	V_g	36 kV
Rated Current	I_l	1 kA
Coupled Inductor	L	10.12 mH: 10.79 mH, k=0.94
Capacitor	C	100 μF

rating and very high life cycle of 40000 hours.

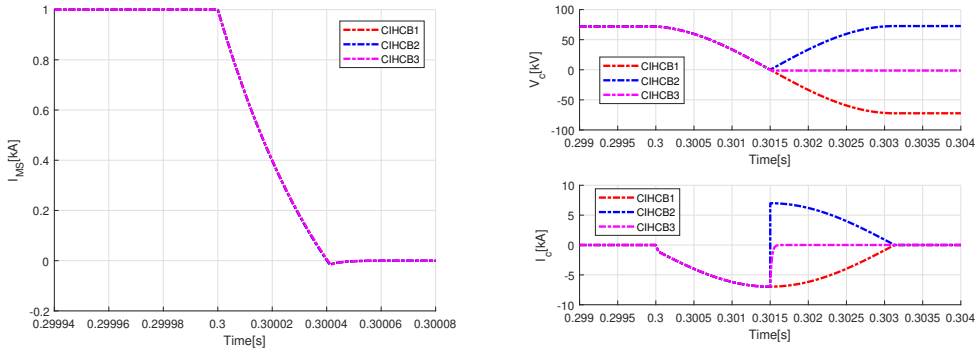
3.6 Simulation Results

The proposed CIHCBs are simulated in PLECS to verify the analysis and design methodology. The simulation is performed for both the 36 kV HVDC distribution and the 300 V prototype to illustrate the scalability of the component design.

3.6.1 Simulation Results for HVDC system

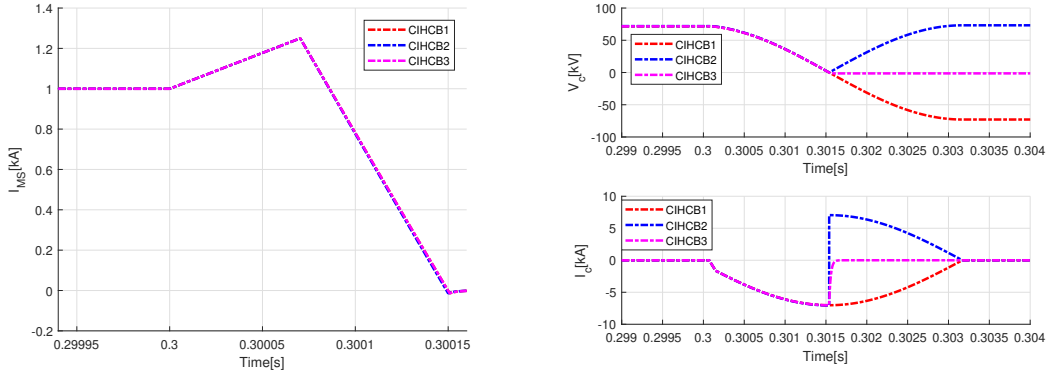
The subsea HVDC distribution bus voltage is selected to be 36 kV. As the subsea pump and compressor motors are rated for 6.6 kV, the number of power converters to provide the required voltage step-down is reduced. The designed parameters for a 36 kV, 1 kA DC system are listed in Table 3.1. Fig. 3.9 and 3.10 show the simulated current commutation process for the CIHCB topologies for resistive load and short-circuit fault interruption, respectively.

Fig. 3.9(a) shows the current through the mechanical switch MS (I_{MS}) during a 1000 A resistive load interruption. The discharging switch T_1 is turned on at t=0.3 s, which forces I_{MS} to zero from its nominal value in 40 μs, which denotes the current commutation time. The current commutation process is identical for all three topologies. Fig. 3.9(b) shows the capacitor voltage v_c and current i_c. It is observed that the capacitor is initially charged to twice the DC source voltage, i.e., v_c attains a value of



(a) (b)

Figure 3.9: 36 kV simulation results for resistive load interruption. (a) MS current. (b) Capacitor voltage and current.



(a) (b)

Figure 3.10: 36 kV simulation results for fault interruption. (a) MS current. (b) Capacitor voltage and current.

72 kV. After T_1 is switched on, the discharging capacitor current has a steep initial slope which denotes the counter-current. Once MS is turned off at zero-current, the capacitor continues to discharge following the mode-IV equations.

Mode-IV operation highlights the difference between the CICHB topologies. In CIHCB1, the capacitor continues to discharge following the voltage zero-crossing. Hence, v_c attains a negative value almost equal to $-2V_g$, as seen from Fig. 3.9(b). For CIHCB2, Q_1 and Q_4 are switched off when v_c=0. This results in the re-charging of the capacitor through the antiparallel diodes of Q_2 and Q_3 which is indicated by the reversal of

Table 3.2: Parameter and Component Details of CIHCB for 300 V System

Parameters	Symbol	Description
Rated Voltage	V_g	300 V
Rated Current	I_L	25 A
Coupled Inductor	L	1.02 mH:1.13 mH
Capacitance	C	100 μF
Components	**Symbol**	**Part Number**
Thyristors	T_1,T_2,MS	TM8050H-8W
Diode	D_1	VS-40EPS08PBF-ND
Capacitors	C	B32778P8206K000

i_c. The commutation capacitor is charged to its initial voltage of $2V_g$, i.e., 72 kV. In CIHCB3, the clamping diode conducts after the voltage zero-crossing. Consequently, the capacitor is bypassed and v_c is clamped to the forward voltage drop of the diode.

Fig. 3.10(a) and (b) show I_{MS} and v_c, and i_c for a short-circuit fault at t=0.3 s. The preset detection level is set at 125% of the nominal load current, i.e., 1.25 kA. The fault commutation time t_f is found to be 150 μs from Fig. 3.10(a). The increase in t_f occurs due to the counter-induction by the primary current i'_{cc}, given by equation 3.26. The counter-induction phenomenon also increases the counter-current required for successful commutation, as seen from the initial slope of i_c in Fig. 3.10(b).

3.6.2 Simulation Results for Prototype System

The CIHCB topologies have also been simulated for a 300 V, 25 A prototype DC system to provide a fair comparison with the experimental results. The simulation results are presented to highlight the mode-I, II and IV operation for resistive load and short-circuit fault interruption. The designed parameters from Table 3.2 are utilized for the simulation. Fig. 3.11 shows the resonant charging of the commutation capacitor from the 300 V DC source. The charging process is identical for all three topologies. The final capacitor voltage is 600 V while the peak capacitor current is almost 94 A.

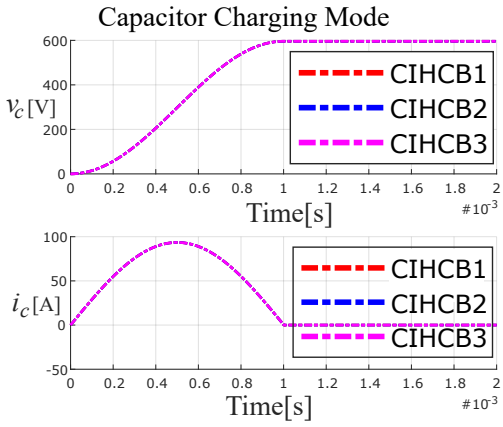
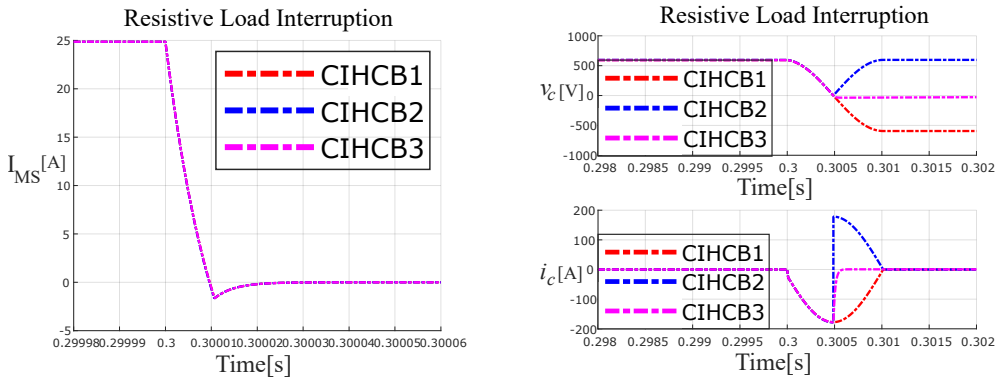


Figure 3.11: Capacitor charging in mode-I.



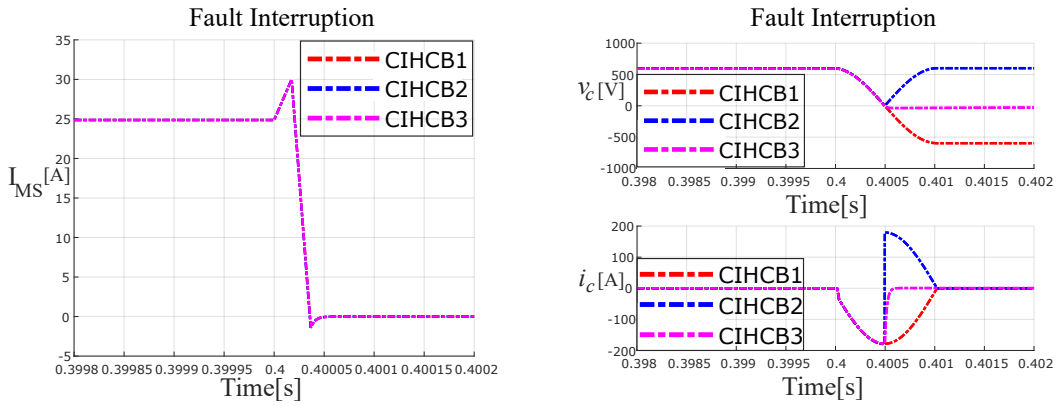
(a) (b)

Figure 3.12: 25 A resistive load interruption. (a) MS current. (b) Capacitor voltage and current.

Peak charging current can be reduced by using a higher number of turns in the primary winding or by reducing the μF value of the capacitor.

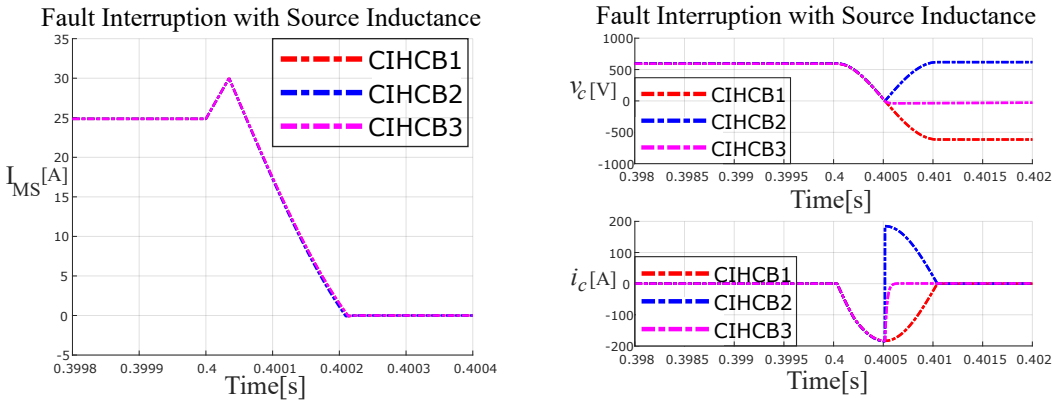
Fig. 3.12(a) shows I_{MS} for the interruption of a resistive load current of 25 A. The current commutation time t_f is observed to be 10 μs. The corresponding capacitor voltage and current are shown in Fig. 3.12(b). Identical waveforms for a short-circuit fault interruption are shown in Fig. 3.13(a) and (b). Due to the counter-induction effect, the current commutation time increases to 25 μs. Also, a higher amplitude of counter-current is sourced by the capacitor for a successful fault interruption.

Fig. 3.14(a) and (b) illustrates the short-circuit fault interruption in presence of a



(a) (b)

Figure 3.13: Short-circuit fault interruption. (a) MS current. (b) Capacitor voltage and current.



(a) (b)

Figure 3.14: Fault interruption in the presence of grid inductance. (a) MS current. (b) Capacitor voltage and current.

grid inductance L_g of 1 mH. The fault response time t_f, in this case, is almost 180 μs which represents a significant increase from the ideal interruption process presented in Fig. 3.13. As L_g is equal to the self-inductance L_s, the equivalent inductance L_{eq_1} in equation 3.35 increases substantially. Consequently, the characteristic impedance Z_{o_1} and resonant frequency ω_{o_1} of the equivalent commutation circuit, shown in Fig. 3.7(a), respectively increases and reduces. This results in a slower commutation process, which is also observed from the reduced initial slope of i_c.

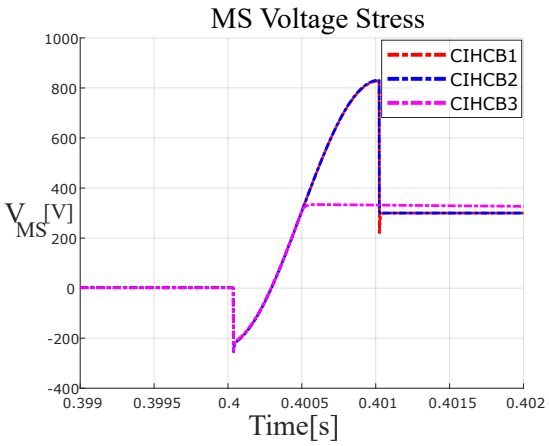


Figure 3.15: Blocking voltage of MS for CIHCB topologies.

The blocking voltage waveform of the mechanical switch is shown in Fig. 3.15. The blocking voltage peak of MS occurs at the end of mode-IV. For CIHCB1 and CIHCB2, the peak voltage stress is $V_{ce} + V_g$. A simplification of the equations (3.37) and (3.38) show that the final capacitor voltage V_{ce} is almost equal to $2V_g$. Consequently, the mechanical switch MS has to be rated for three times the DC bus voltage. The blocking voltage stress is much reduced in CIHCB3, where the clamping diode ensures a maximum blocking voltage of V_g for MS.

3.7 Experimental Validation

The operation of the CIHCBs is also experimentally verified using two 300 V, 25 A prototype units. Table 3.2 provides the test parameters and component details. The coupled inductor is formed by two C-type cores to reduce leakage flux and obtain a higher coupling coefficient. Polypropylene film type DC capacitors are utilized due to their high peak current rating. All the switching devices including MS are implemented by 800 V rectifier-grade thyristors (TM8050H-8W). The transient currents are captured by a Rogowski coil based current transducer with a sensitivity of 10 mV/A. The test setup and the CIHCB1 prototype is shown in Fig. 3.16.

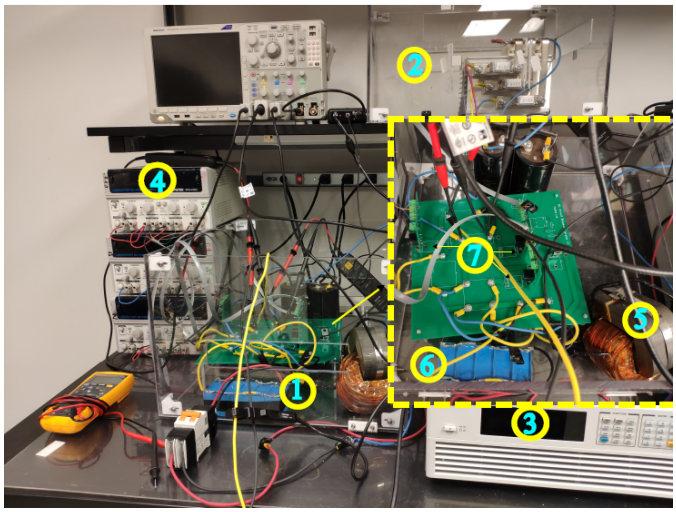


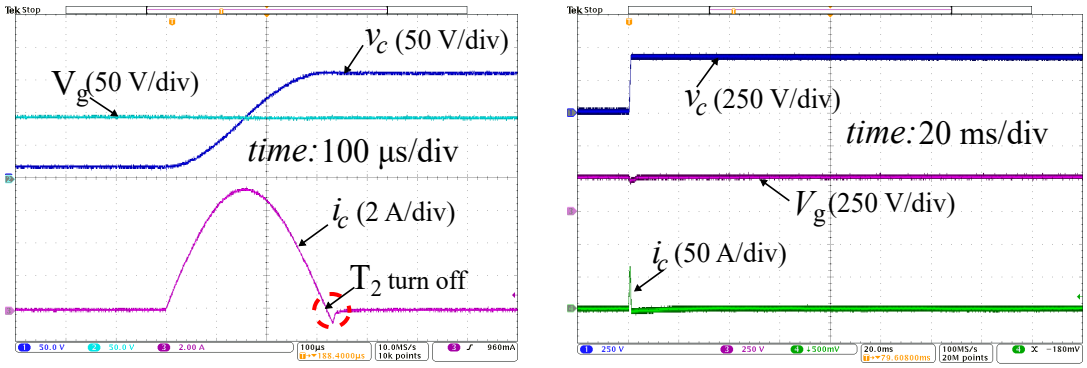
Figure 3.16: Experimental setup. 1. DCCB prototype. 2. Diode Rectifier. 3. DC Power Supply. 4. Power supply for triggering circuits. 5. Coupled Inductor. 6. Commutation capacitor. 7. Thyristors for main and auxiliary switch.

3.7.1 Capacitor Charging

Fig. 3.17(a) and (b) show the resonant charging of the capacitor for DC source voltages of 100 V and 250 V, respectively. The charging process follows the design equations (3.1) and (3.2). The capacitor is charged to a voltage slightly lesser than 200 V due to the ESR drop in Fig. 3.17(a). The thyristor T_2 turns off at the zero-crossing of i_c. Subsequent reverse-recovery of T_2 is indicated by the negative i_c value. Fig. 3.17(b) shows v_c over an extended time scale. The commutation capacitor voltage is maintained around 500 V in floating condition.

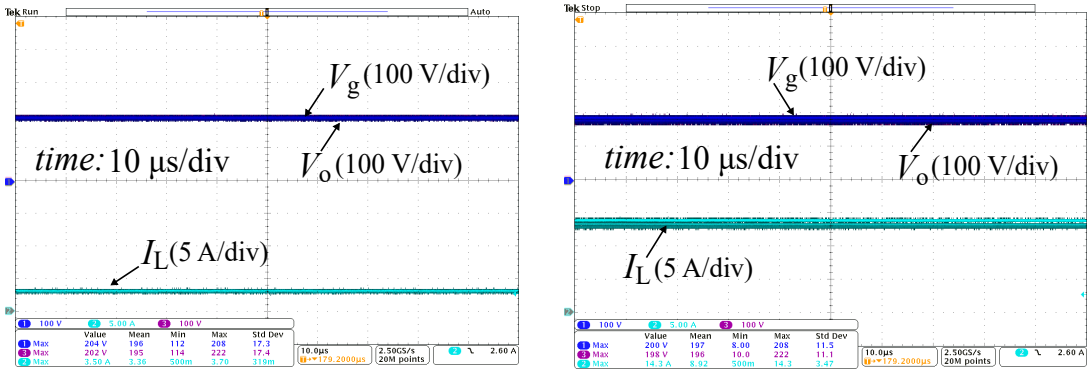
3.7.2 Power Delivery Mode

Fig. 3.18(a) and (b) show the DC input and output voltage during normal power delivery (mode-II) for load currents of 3.5 A and 14 A, respectively. The series voltage drop is measured to be 1 V for an output voltage of 196 V, which implies low conduction loss of about 0.5%.



(a) (b)

Figure 3.17: Capacitor charging mode. (a) V_g=100 V. (b) V_g=250 V.

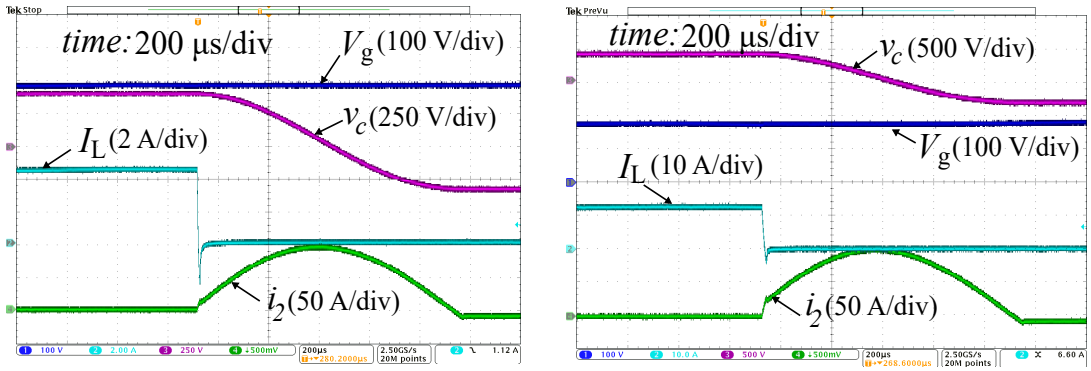


(a) (b)

Figure 3.18: Power delivery mode. (a) I_L=3.5 A. (b) I_L=14 A.

3.7.3 Resistive Load Interruption

The commutation performance of CIHCB1 is demonstrated for resistive load interruption at V_g=200 V. Fig. 3.19(a) illustrates the commutation process for a load current I_L=5 A. The measured counter-current is denoted by i_2, which is equal and opposite to i_c. The current commutation time t_f is found to be 8 μs. The negative segment of load current I_L represents the reverse-recovery current of the thyristor MS. Interruption of 15 A load current is shown in Fig. 3.19(b) with an increased t_f of 15 μs. The increased current level requires a higher counter-current that results in a longer commutation period with the same circuit parameters. Nonetheless, the experimental



(a) (b)

Figure 3.19: Resistive load interruption by CIHCB1. (a) I_L=5 A. (b) I_L=13 A.

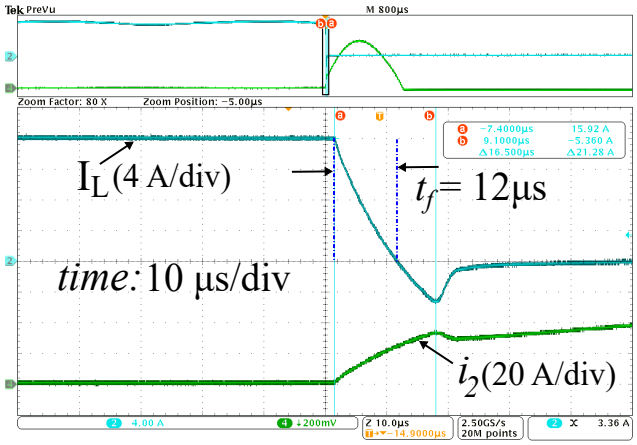
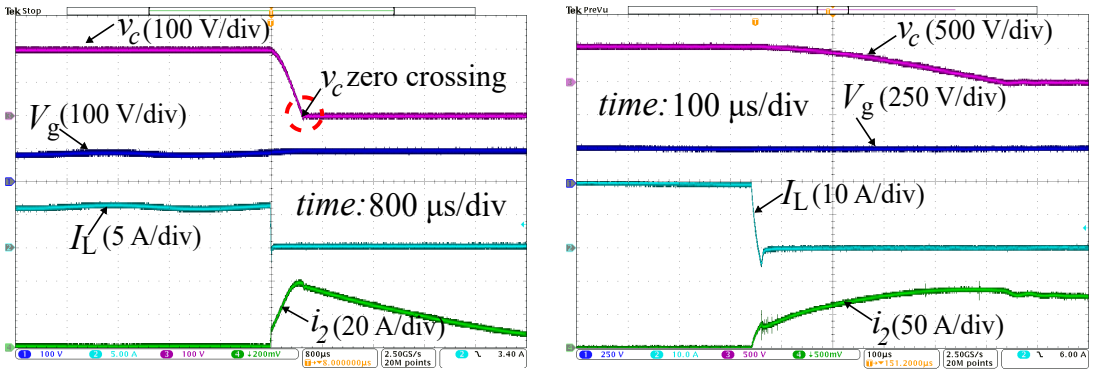


Figure 3.20: Amplified Current Commutation Process for I_L=16 A.

results remain consistent with the design equations and the simulation results.

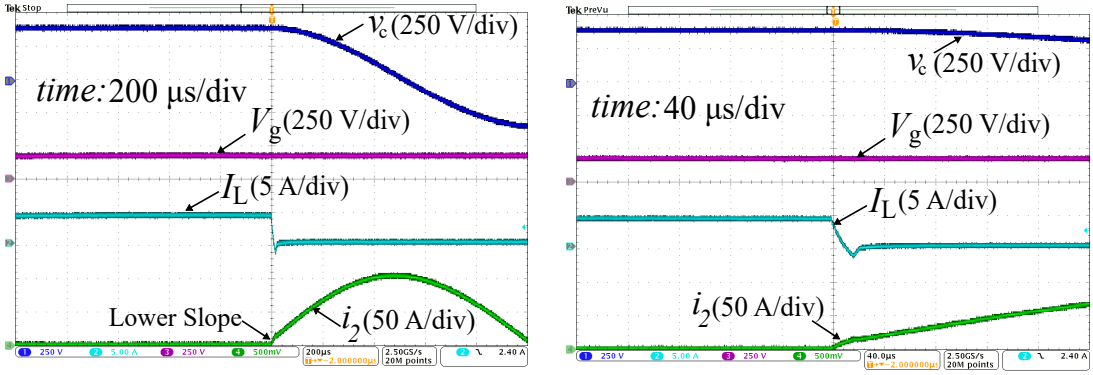
The commutation mechanism in mode-III over an amplified time scale for V_g=300 V and I_L=16 A is shown in Fig. 3.20. The series path thyristor MS turns off in 12 μs, which implies a smaller t_f than the interruption event shown in Fig. 3.19(b). The reduction in t_f is achieved by charging the capacitor at a higher voltage. The initial capacitor voltage $V_{c,f}$ is 550 V, compared to $V_{c,f}$=350 V in the other case. This proves that the pre-fault charging voltage is a deciding factor in the response time of CIHCBs.

Resistive load interruption performance of CIHCB3 is shown in Fig. 3.21. Fig. 3.21 (a) depicts the commutation at I_L =7 A. Secondary current i_2 decays exponentially



(a) (b)

Figure 3.21: Resistive load interruption by CIHCB3. (a) I_L=7 A. (b) I_L=20 A.



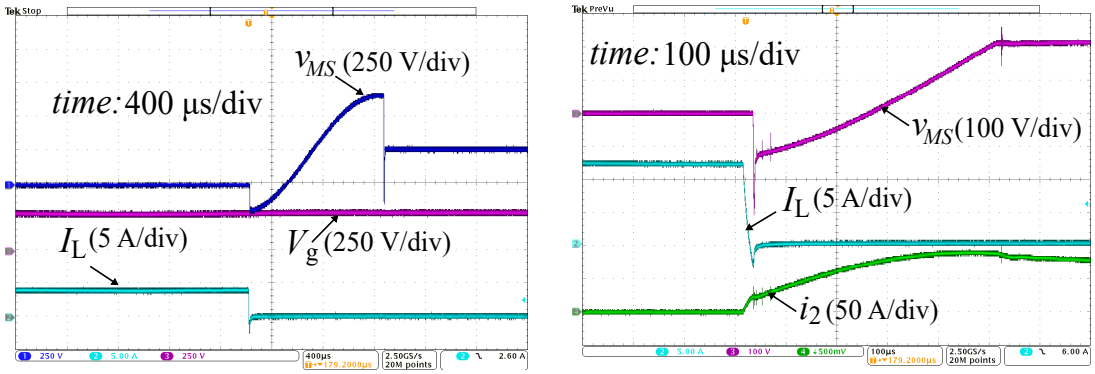
(a) (b)

Figure 3.22: Inductive load interruption. (a) Commutation, (b) Magnified Mode III.

following equation (3.8). The amplified commutation process for I_L=20 A and V_g = 300 V is presented in Fig. 3.21 (b). Thyristor MS commutates in 15 μs. The response time is identical to CIHCB1.

3.7.4 Inductive Load Interruption

CIHCB1 is also tested with an R-L load with an inductance of L_g = 300 μH. This condition is equivalent to the event of current commutation with grid inductance. Fig. 3.22(a) and (b) represent the commutation modes for I_L = 5 A and V_g = 200 V. A reduction in the initial slope of the counter-current i_2 is observed, which results



(a) (b)

Figure 3.23: Blocking voltage of MS (a) CIHCB1. (b) CIHCB3.

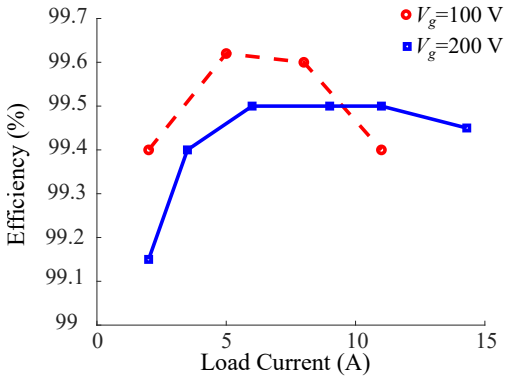


Figure 3.24: CIHCB efficiency as a dc switch.

in an increased current commutation time of 30 μs. These experimental results are consistent with the simulation results presented in Fig. 3.14.

3.7.5 Blocking Voltage Measurement

Fig. 3.23(a) and (b) depict the blocking voltage of MS in mode IV for topology 1 and 3. The dc source voltage V_g is maintained at 250 V. The maximum voltage across MS is computed as 650 V for CIHCB1. In CIHCB3, the peak blocking stress is reduced to 250 V due to the clamping diode D_1. Consequently, semiconductor devices or power relays of lower voltage rating can be used to implement MS.

3.8 Discussion

This section presents a review of the performance indices of the CIHCB topologies, such as commutation performance, efficiency, filter response, etc.

3.8.1 Commutation Performance

CIHCB topologies provide fast interruption and isolation to overcurrent and short-circuit faults. The simulation and experimental results for the 300 V system show that the current commutation time can range from 5 to 25 μs depending on the load current level and the grid inductance. The current commutation time t_f is comparable to Z-source circuit breakers (ZSCB) [108]-[115] and the coupled inductor circuit breakers [117]-[120]. However, t_f is programmable and it depends on the design of the passive elements. This is apparent from the HVDC simulation results with a 10 mH coupled inductor, which results in increased response time in the range of 100 μs. Nonetheless, the value of t_f for HVDC systems is well within the specified limit [49].

CIHCBs show superiority over existing ZSCB topologies by reducing spurious tripping. Although two more switches are used, the inclusion of the discharging switch T_1 provides an additional degree of freedom to mitigate spurious tripping. The charging switch T_2 causes the capacitor to charge to twice the DC source voltage, which enhances the current interruption range and reduces t_f. Also, the charging takes place before energizing the load, which is a more desirable situation if the fault persists. The CIHCB operation ensures that the energy-storage elements do not feed the fault, unlike ZSCBs. The topology 2 can also provide the option of reclosing as the commutation capacitor is re-charged to a positive voltage within the commutation cycle.

CIHCBs also mitigate the requirement of overvoltage protection of the main breaker.

The stored inductive energy ($\frac{1}{2}LI^2$) is translated into stored capacitive energy ($\frac{1}{2}CV_c^2$) during mode-IV, which charges the capacitor to a voltage of $\pm 2V_g$. Hence, a dissipative snubber circuit is not required. The clamping diode suppresses the transient overvoltage in CIHCB3 as the energy is dissipated through the secondary R-L network.

3.8.2 Efficiency Evaluation

The efficiency of the DC circuit breaker is measured in terms of the conduction power loss during power delivery mode. For the implementation of MS, the experimental setup uses an 800 V thyristor with a maximum on-state voltage drop of 1.55 V. The low on-state voltage drop reduces the device conduction loss. The other source of conduction loss is the ESR of the primary winding which is in series with MS. The measured ESR of the primary winding is 23.3 mΩ, which is also very small. Fig. 3.24 plots the efficiency of CIHCBs as a DC switch at different loading conditions with the dc source voltage as a parameter. The maximum efficiency during power delivery mode is measured to be around 99.6%.

3.8.3 Filter Response

The DC circuit breaker (DCCB) is used for feeder protection in the subsea DC grid. In the proposed HVDC architectures, each DCCB interfaces either a DC-AC or a DC-DC converter. Consequently, the DCCB needs to exhibit a low pass filter response while operating as a DC switch. Otherwise, the waveforms of the power conversion stage may be distorted. CIHCB topologies exhibit a first-order filter response as the primary winding of the coupled inductor is in series with MS. The input-output voltage transfer function can be written as

$$\frac{v_o(s)}{v_g(s)} = \frac{R_L}{R_L + sL_s}, \tag{3.39}$$

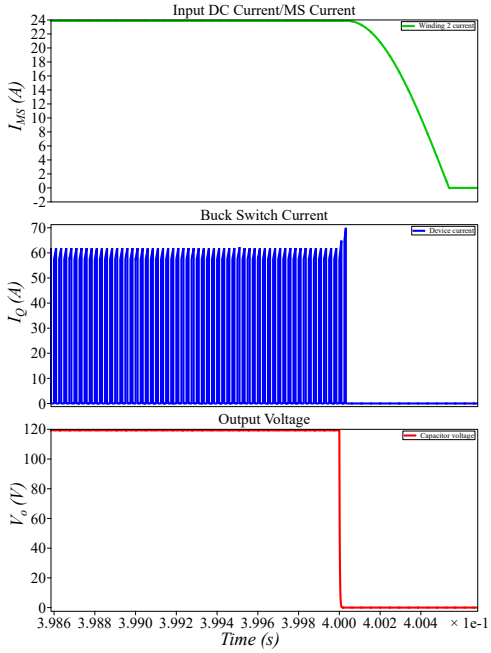


Figure 3.25: Filtering Performance of CIHCB1.

where R_L is the load resistance and L_s is the self-inductance of the primary winding.

The operation of CIHCB1 interfacing a DC-DC buck converter is simulated in PLECS to verify the low-pass filter response. Fig. 3.25 shows the simulated DC source current (I_{MS}) along with the converter input current (I_Q). The continuous source current waveform verifies the low-pass filtering by the CIHCB. Also, the switching operation of the dc-dc converter is not affected by the circuit breaker. During a short-circuit fault at t=0.4 s, both I_MS and I_Q are driven to zero, implying successful current interruption by CIHCB1. Thus, the proposed coupled inductor hybrid breakers prove to be suitable for fault protection in the modular DC architectures.

3.9 Summary

This chapter presents three coupled inductor based DC hybrid circuit breaker topologies, which provide the following advantages.

- Exhibit fast fault response and facilitate zero-current turn-off of the main switch which is suitable for an HVDC implementation.
- Mitigate the requirement of a pre-charging circuit for the capacitor.
- Snubber circuits for overvoltage protection is not required, unlike the conventional hybrid breakers.
- Incur low conduction loss while operating as a DC switch.

The performance of the proposed CIHCBs has been verified by simulation and experimental results.

3.10 Publications

1. A. Ray, K. Rajashekara, S. N. Banavath and S. K. Pramanick, "Coupled Inductor-Based Zero Current Switching Hybrid DC Circuit Breaker Topologies," in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 5360-5370, Sept.-Oct. 2019.
2. A. Ray, S. N. Banavath, S. K. Pramanick and K. Rajashekara, "A Coupled Inductor Based Hybrid Circuit Breaker Topology for Subsea HVDC Transmission Systems," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 7142-7149.

Chapter 4

Bidirectional Hybrid Breakers for Future Subsea Grid

4.1 Introduction

The existing subsea power architectures are designed for unidirectional power flow, from the onshore power source to the subsea VSD loads. The subsea feeders in the modular HVDC architectures presented in chapter 2 do not encounter power flow in the opposite direction. Accordingly, the coupled inductor hybrid circuit breakers (CIHCB) proposed in chapter 3 are designed for unidirectional fault interruption. However, future subsea power networks are envisaged to move towards renewable power. Bulk renewable power sources, such as offshore wind farms, are projected to partially supply the subsea loads to reduce the power demand from the onshore grid [28], [31]. In this subsea microgrid configuration, the HVDC feeders would experience bidirectional power flow. Consequently, the HVDC circuit breaker has to be designed for bidirectional current interruption capability.

Conventional hybrid circuit breakers have been implemented for bidirectional current interruption with current-bidirectional switches in the parallel path to the main breaker [80]-[81]. However, as already discussed in section 1.3, these HCBs show significant drawbacks in terms of arcing, slow commutation speed and reduced life-cycle. The ABB circuit breaker [76] improves the commutation speed at the expense of increased conduction loss. Counter-current breakers for bidirectional operation are also found in literature [97]-[98], [122],[124]. Nonetheless, the current breaking operation

still involves arcing across MCB contacts. These bidirectional HCB topologies require a pre-charging circuit for the capacitor as well as passive snubbers for overvoltage suppression. For subsea implementation, these issues present a significant challenge.

To mitigate the above issues, three bidirectional coupled inductor HCB topologies (BCIHCB) are presented in this chapter. BCIHCB topologies are derived from the CIHCB topologies presented in chapter 3. The first topology (BCIHCB1) uses an auxiliary switched resonant circuit comprising of a three-winding coupled inductor and a commutation capacitor for ZCS turn-off the mechanical switch during a fault [128]. Thus, BCIHCB1 is an extension of the CIHCB1 topology presented in section 3.2 for bidirectional operation. Two modified HCBs are also introduced in this chapter, which can retain the bidirectional current interruption property using 2-winding coupled inductors and a reconfigured resonant circuit. The third BCIHCB topology also ensures a unipolar capacitor voltage profile [127]. All of these proposed topologies exhibit fast current commutation similar to the CIHCB topologies. Simulation and experimental results are presented to illustrate the fault response of the BCIHCB topologies.

4.2 Bidirectional Coupled Inductor HCB 1

The bidirectional coupled inductor based HCB 1 (BCIHCB1) is shown in Fig. 4.1 [128]. L_1 represents the three-winding coupled inductor whose primary winding $1-1'$ is in series with two mechanical switches S_1 and S_2. The secondary windings $2-2'$ and $3-3'$ form two separate series resonant circuit with the commutation capacitor C through thyristors T_1 and T_2. S_1 and S_2 conduct during power delivery mode to minimize the conduction loss. The power flow can occur either from the port A to the port B, known as the forward power mode, or from the port B to the port A which is the reverse power mode. Turns ratio of the coupled inductor is selected to be 1:1:1

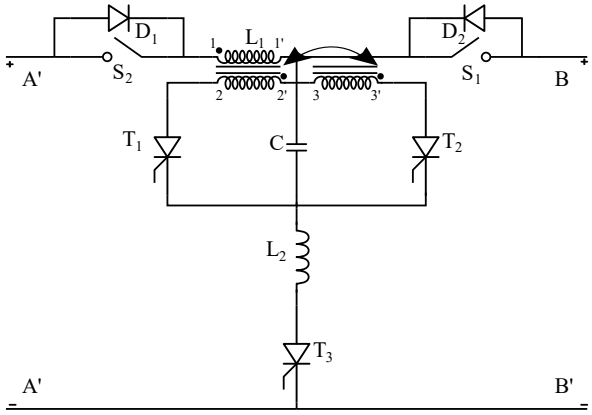


Figure 4.1: Bidirectional Coupled inductor HCB 1

for the prototype design, although a higher number of primary turns can be used to enhance the fault interruption capability. Thyristor T_3 and diodes D_1 and D_2 are used for the resonant charging of the capacitor from the DC link. Fig. 4.2 shows the four operating modes of BCIHCB1 in the forward power mode. Corresponding voltage and current waveforms are shown in Fig. 4.3(a). The reverse power mode is identical in operation and is depicted in Fig. 4.3(b).

4.2.1 Mode I ($t_0 \sim t_1$)

Resonant charging of the commutation capacitor begins at $t = t_0$ when the charging thyristor T_3 is turned on. The charging current path is $D_1 - 1 - 1' - C - L_2 - T_3$, as shown in Fig. 4.2(a). At the end of the resonant half-cycle, D_1 and T_3 are naturally commutated while C is charged to twice the DC source voltage ($2V_g$). Inductor L_2 is used to facilitate a resonant charging in reverse power mode, i.e., when the DC power feed is from the ports $B - B'$. In this case, the current path is $D_2 - C - L_2 - T_3$.

Capacitor charging mode is governed by equations (3.1) and (3.2), although the expressions of the characteristic impedance Z_o and the resonant frequency ω_o differ.

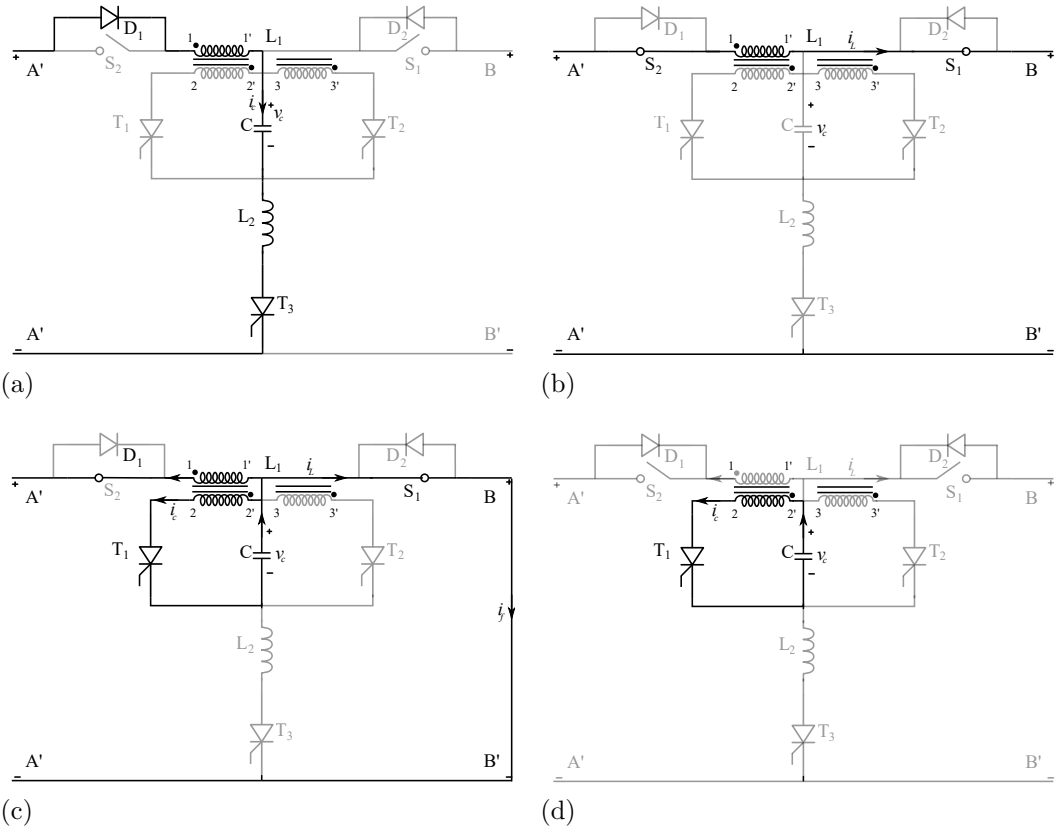


Figure 4.2: Operating modes of BCIHCB1 in forward power mode. (a) Mode I: capacitor charging. (b) Mode II: power delivery. (d) Mode III: current commutation. (d) Mode IV: reverse charging of capacitor.

Z_o and ω_o are expressed for the forward and reverse power mode by the equations

$$Z_o = \sqrt{\frac{L_s + L_2}{C}} \quad \text{and} \qquad \omega_o = \sqrt{\frac{1}{(L_s + L_2)C}} \quad \text{and} \tag{4.1}$$

$$Z_o = \sqrt{\frac{L_2}{C}} \quad \text{and} \qquad \omega_o = \sqrt{\frac{1}{L_2 C}}. \tag{4.2}$$

L_s is the self-inductance of both primary and secondary winding for a unity turns ratio. The above equations show that the peak charging current in the reverse power mode is higher due to a smaller Z_o. This is also observed from the capacitor current (i_c) waveforms in Fig. 4.3(a) and (b).

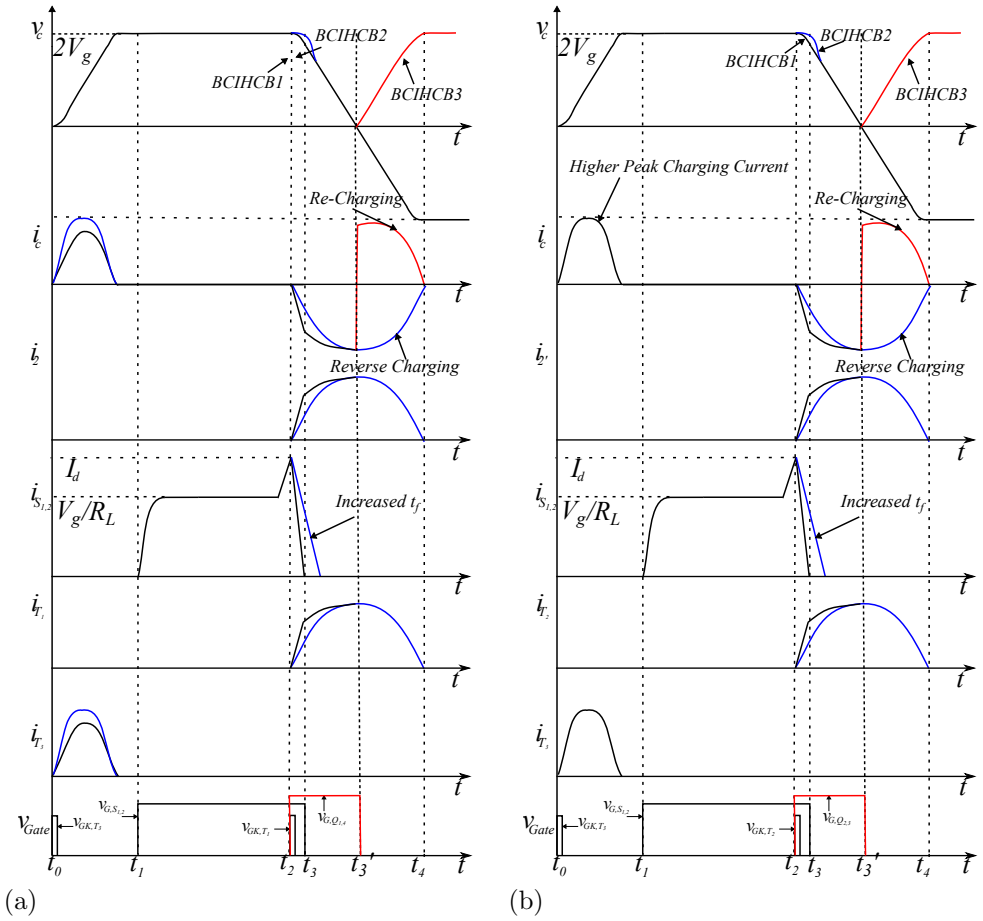


Figure 4.3: Operating waveforms of BCIHCB1 (black), BCIHCB2 (blue) and BCIHCB3 (red). (a) Forward power mode. (b) Reverse power mode.

4.2.2 Mode-II ($t_1 \sim t_2$)

Following the commutation of T_3, closing signals to MCBs S_1 and S_2 are given at the instant $t = t_1$. Subsequently, power flow is established between ports A and B, as shown in Fig. 4.2(b).

4.2.3 Mode III ($t_2 \sim t_3$)

Thyristor T_1 is turned on at $t = t_2$ when the fault current is detected at the preset level I_d . Capacitor C now discharges through the winding $2-2'$. The conduction path

is highlighted in Fig. 4.2(c). The other discharging switch T_2 remains off throughout this mode. The counter-current induced in the primary winding $1-1'$ forces the fault current i_f to zero at $t = t_3$. S_1 and S_2 are switched off at this instant. Consequently, the mechanical contacts can be opened at zero current without arc formation.

In a practical scenario, due to the contact opening delay of mechanical switches, the primary current may become negative. This causes the antiparallel diodes D_1 and D_2 to conduct, which preserves an arcless opening of S_1 and S_2. In the reverse power mode, thyristor T_2 is switched on to create a series resonance between the secondary winding $3-3'$ and the capacitor C. T_1 remains off throughout the reverse power mode.

4.2.4 Mode IV ($t_3 \sim t_4$)

After the opening of S_1 and S_2, a series resonant circuit is formed by the self-inductance of the secondary winding $2-2'$ (or $3-3'$ in reverse power mode) and the commutation capacitor C. Capacitor C continues to discharge until its voltage v_c becomes almost equal to $-2V_g$ at $t = t_4$ when T_1 is commutated. Fig. 4.2(d) illustrates the discharging path. Equations (3.4) and (3.5) govern the profile of v_c and i_c.

4.3 Bidirectional HCB 2 with Two-Winding Coupled Inductor

The BCIHCB1 topology presented in section 4.2 uses an additional inductor L_2 for resonant charging of the commutation capacitor from the DC source in the reverse power mode. However, this inductor is idle during modes III and IV, which points to a lower utilization factor. A more compact magnetic design can be obtained by replacing the 3-winding coupled inductor with two 2-winding coupled inductors, which eliminates the external inductor. The schematic of the modified HCB, denoted as BCIHCB2 is shown in Fig. 4.4, where L_1 and L_2 are the two-winding coupled inductors with unity

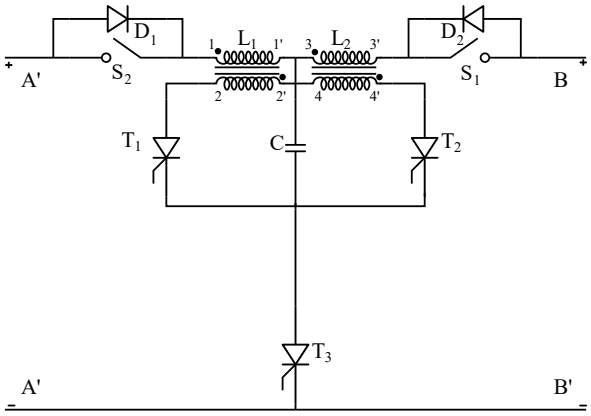


Figure 4.4: Bidirectional Coupled inductor HCB 2

turns ratio. The secondary side discharging network is identical to BCIHCB1, except that the secondary windings $2-2'$ and $4-4'$ are not in the same magnetic core. Also, this modified topology has the same switch count as the BCIHCB1.

Fig. 4.5 shows the operating modes of BCIHCB2 during reverse power operation. The operating principle of this topology is similar to BCIHCB1, except for the capacitor currents and voltages in modes I and III. The peak charging current in mode-I, shown in Fig. 4.5(a), is equal in forward and reverse power mode for identical coupled inductors L_1 and L_2. The characteristic impedance and the resonant frequency of the charging circuit is given by

$$Z_o = \sqrt{\frac{L_s}{C}} \quad \text{and} \qquad \omega_o = \sqrt{\frac{1}{L_s C}}. \tag{4.3}$$

The mode-III current commutation is slower compared to the BCIHCB1 topology, as seen from Fig. 4.5(c). Both primary windings $1-1'$ and $3-3'$ conduct the fault current i_f. However, only one secondary winding is active depending on the power flow direction. In the reverse power mode, winding $3-3'$ resonates with the commutation capacitor through thyristor T_2, while T_1 remains throughout the operation. Consequently, the equivalent inductance of the secondary series-resonant circuit increases, similar to current commutation in the presence of source inductance. This results in

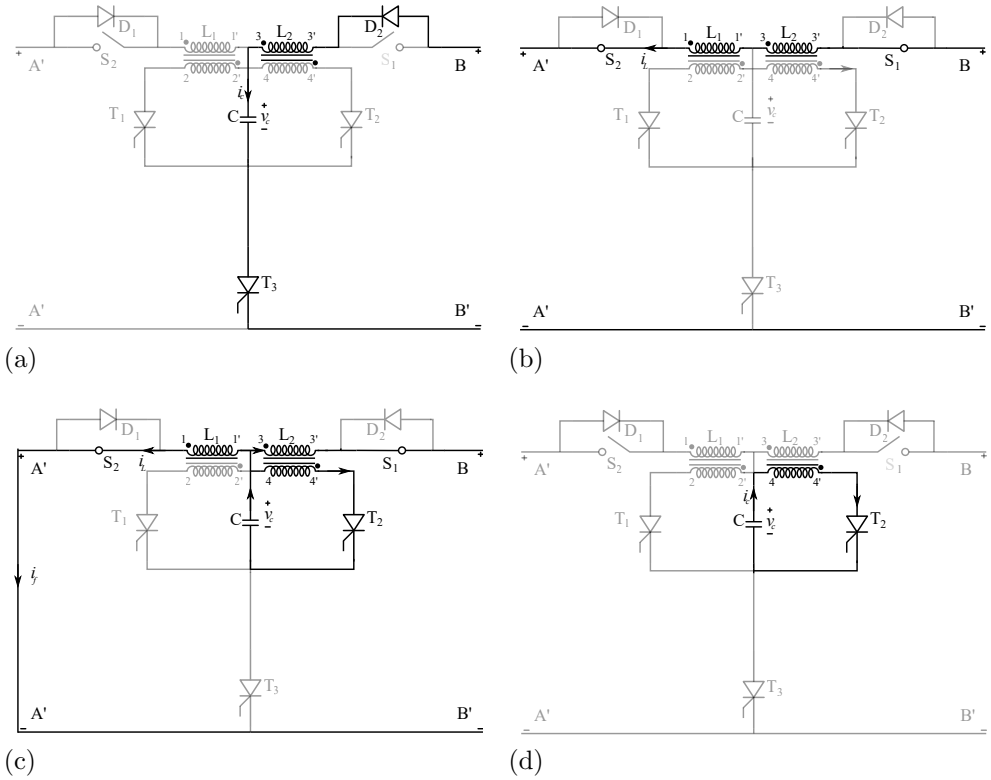


Figure 4.5: Operating modes of BCIHCB2 in reverse power mode. (a) Mode I: capacitor charging. (b) Mode II: power delivery. (d) Mode III: current commutation. (d) Mode IV: reverse charging of capacitor.

a reduction of the counter-current magnitude and an increase of current commutation time t_f. The corresponding waveforms are presented in Fig. 4.3(a) and (b).

4.4 Bidirectional HCB 3 with Unipolar Capacitor Voltage

The bidirectional coupled inductor-based HCB topologies presented in sections 4.2 and 4.3 exhibits an ac voltage profile of the commutation capacitor. This prohibits the use of electrolytic capacitors, resulting in a larger stack size for the HVDC application. A dc voltage profile on the capacitor is obtained by modifying the H-bridge based CIHCB2 topology presented in section 3.3 for bidirectional operation. The resulting bidirectional circuit breaker, denoted as BCIHCB3, is illustrated in Fig. 4.6 [127].

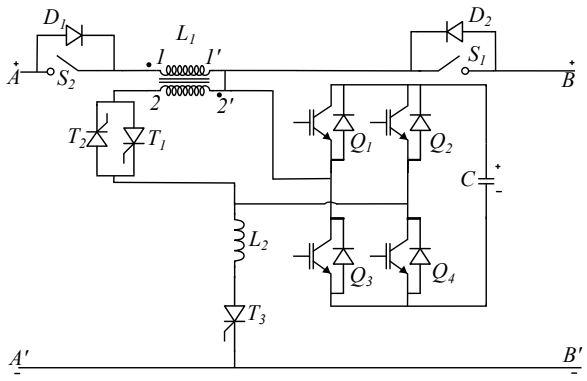


Figure 4.6: Bidirectional Coupled inductor HCB 3

The commutation capacitor C is connected to the input of the H-bridge formed by the current bidirectional switches $Q_1 - Q_4$. Other than the H-bridge, the number of switches remain the same as the previous two topologies. Moreover, BCIHCB3 requires only one two-winding coupled inductor for breaking operation. Nonetheless, capacitor charging in reverse power mode necessitates an external inductor L_2 in series with the charging thyristor T_3. The operation of this topology in the forward power mode is presented in Fig. 4.7. Corresponding waveforms are shown in Fig. 4.3(a) and (b).

4.4.1 Mode I, II ($t_0 \sim t_2$)

The capacitor charging mode is shown in Fig. 4.7(a). In the forward power mode, C is charged through the conduction of D_1, the antiparallel diodes of Q_1 and Q_4 and T_3. The characteristic impedance and the resonant frequency of the charging circuit, in this case, is given by equation (4.1). Diode D_2 conducts during capacitor charging from the ports $B - B'$ in the reverse power mode, while D_1 remains off. The rest of the conducting devices are the same as in the forward power mode. The charging circuit parameters in the reverse power mode is given by equation (4.2).

In mode-II, mechanical switches S_1 and S_2 are turned on at $t = t_1$ to commence the power flow between the ports A and B. All the other switches remain off in the

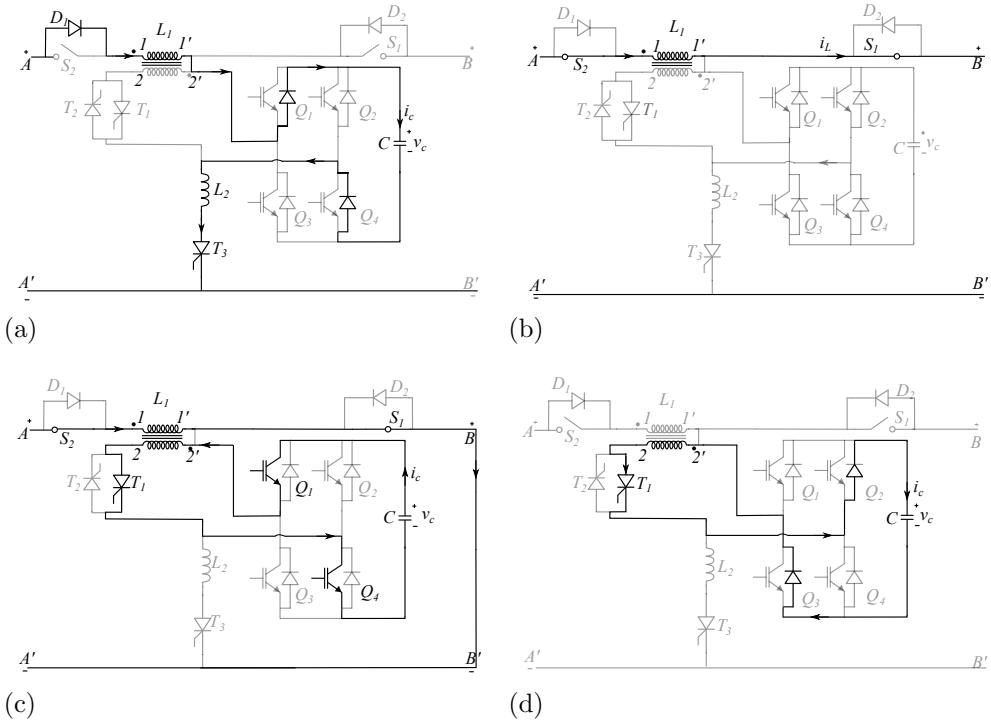


Figure 4.7: Operating modes of BCIHCB3 in forward power mode. (a) Mode I: capacitor charging. (b) Mode II: power delivery. (d) Mode III: current commutation. (d) Mode IV: re-charging of capacitor.

power delivery mode. This mode is shown in Fig. 4.7(b).

4.4.2 Mode III ($t_2 \sim t_3$)

Upon the detection of a fault, thyristor T_1 and the H-bridge switches Q_1 and Q_4 are turned on simultaneously. The counter-current in the primary winding $1 - 1'$ due to the discharging current forces the current through the mechanical switches S_1 and S_2 to zero. The mechanical switches are opened at the instant $t = t_3$. Diodes D_1 and D_2 provide a path for any negative current due to contact opening delay. Thus an arcless breaking operation can be achieved. The conduction path is highlighted in Fig. 4.7(c). In the reverse power mode, Q_3, Q_4 and thyristor T_2 are switched on to generate the counter-current for zero-current turn-off of the mechanical switches.

4.4.3 Mode IV ($t_3 \sim t_4$)

The commutation capacitor continues to discharge through the secondary winding following the main breaker turn-off. When the capacitor voltage v_c falls to zero, the gate pulses to the switches Q_1 and Q_4 are revoked. Subsequently, the secondary current i_2 charges capacitor C through the antiparallel diodes of Q_2 and Q_3, as shown in Fig. 4.7(d). The capacitor voltage attains a final value of $2V_g$, as seen from Fig. 4.3(a). T_1 is commutated at the zero crossing of i_c.

In the reverse power operation, the re-charging of capacitor C is achieved by the conduction of the antiparallel diodes of Q_1 and Q_4 as well as the discharging thyristor T_2. Fig. 4.3(b) illustrates the mode-IV waveforms during reverse power flow. As the commutation capacitor is charged to a positive voltage, BCIHCB3 topology can be used in reclosing operation.

4.5 Design Guidelines of BCIHCBs

The bidirectional circuit breakers can be analyzed by modal equivalent circuits referred to secondary winding, similar to the CIHCBs in chapter 3. The series resonant circuit during the charging mode is the same for all three topologies, except the equivalent series inductance, which can be L_s, L_2, or $L_2 + L_s$ depending on the power flow direction. The peak charging current can be expressed as

$$I_{c_{p,c}} = \frac{V_g}{Z_{o,min}}, \tag{4.4}$$

where $Z_{o,min} = \sqrt{\dfrac{\min(L_s, L_2)}{C}}$ represents the minimum characteristic impedance of the charging circuit.

The principal difference between the proposed bidirectional topologies is observed

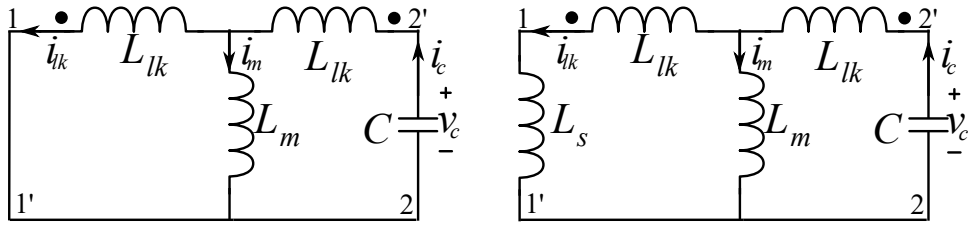


Figure 4.8: Equivalent circuits of BCIHCBs during current commutation. (a) Topology 1 and 3. (b) Topology 2.

during the current commutation in mode-III. The corresponding equivalent circuits for topology 1 and 3, and topology 2 are shown in Fig. 4.8(a) and (b), respectively. The equivalent series inductance of the commutation circuit in the case of BCIHCB1 (BCIHCB3) and BCIHCB2 are given by the equations

$$L_{eq,B1} = (1 - k^2)L_s \quad \text{and} \tag{4.5}$$

$$L_{eq,B2} = (1 - \frac{k^2}{2})L_s. \tag{4.6}$$

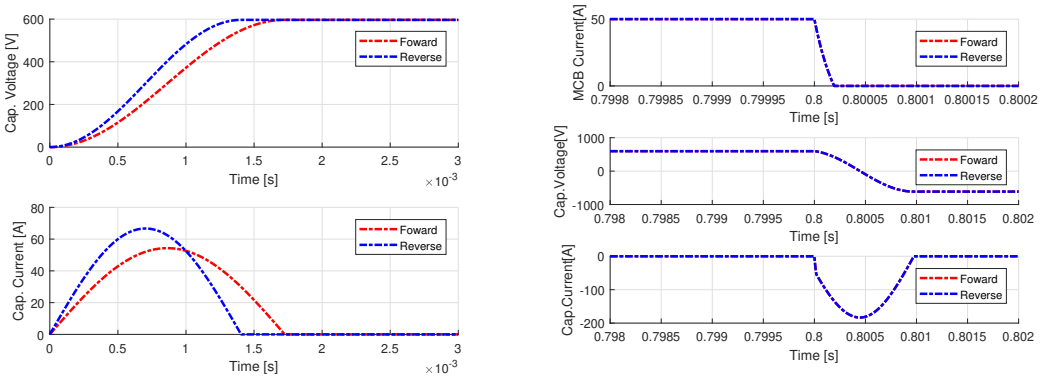
It is apparent from the above equations that $L_{eq,B2} > L_{eq,B1}$, which results in a higher Z_o and lower ω_o of the equivalent series resonant circuit shown in Fig. 4.8. This causes a slower current commutation for the topology 2, which is illustrated in Fig. 4.3. Current commutation failure can be avoided by using a higher number of turns in the primary winding, which reduces $L_{eq,B2}$. Apart from this, component design follows the procedure explained in section 3.5.

4.6 Simulation Results

The BCIHCB topologies are simulated for a 300 V, 50 A DC system. The simulation results demonstrate the breaker operation in the case of resistive load interruption and short-circuit fault in the forward and reverse power mode. The parameters used for the

Table 4.1: Parameter Details for BCIHCB Topologies

Parameters	Symbols	Description
Rated Voltage	V_g	300 V
Rated Current	I_L	50 A
Coupled Inductor 1	L_{s_1}	1.016 mH: 1.129 mH: 1.129 mH
Coupled Inductor 2	L_{s_2}	1.016 mH: 1.129 mH
Coupled Inductor 3	L_{s_3}	10.12 mH: 10.79 mH
Commutation Capacitor 1	C_1	100 μF
Commutation Capacitor 2	C_2	200 μF

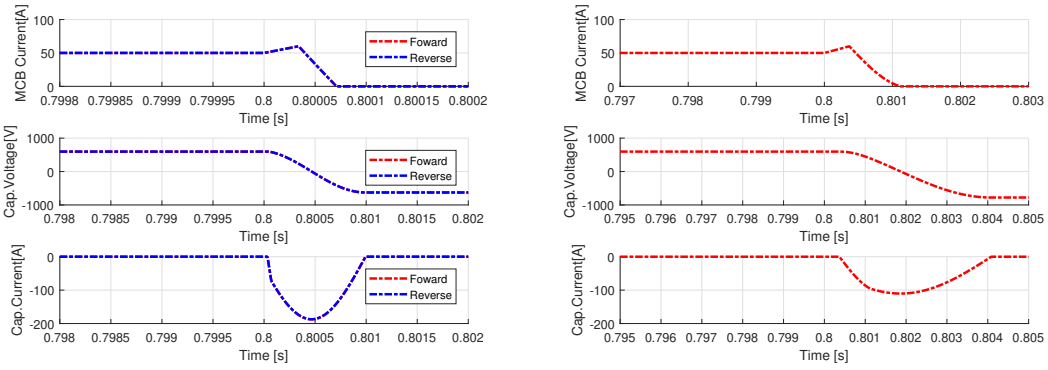


(a) (b)

Figure 4.9: BCIHCB1 simulation results. (a) Charging mode. (b) Resistive load interruption.

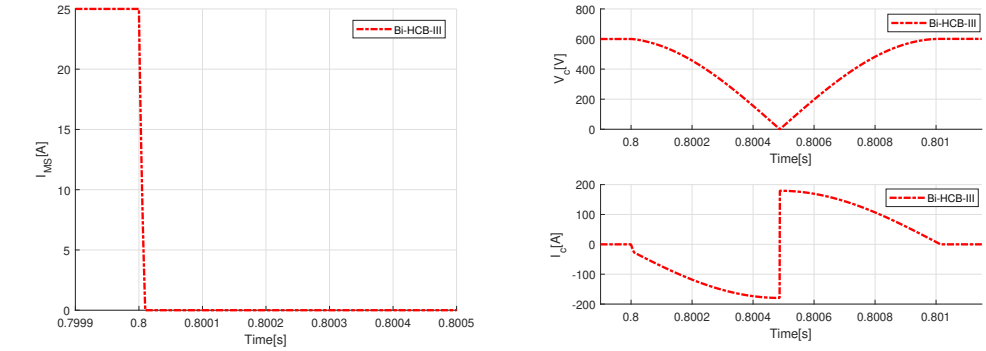
simulation are listed in Table 4.1. The 3-winding coupled inductor 1 (L_{s_1}) parameters along with the C_1 value is used for simulating BCIHCB1. For BCIHCB2, L_{s_2}, L_{s_3} and C_2 values are utilized while the third topology utilizes the parameters L_{s_2} and C_1.

Fig. 4.9(a) shows capacitor charging from 300 V DC source for BCIHCB1. The final capacitor voltage is $2V_g$, i.e., 600 V. The peak capacitor current in reverse power mode is higher due to a lower Z_o value, which corroborates equation (4.2). Fig. 4.9(b) highlights a 50 A resistive load current interruption, where the MCB current $i_{s_{1,2}}$ is forced to zero within 25 μs. Fig. 4.10(a) shows $i_{s_{1,2}}$, v_c, and i_c for a short-circuit fault interruption. Current commutation time t_f increases to around 75 μs, due to a higher counter-current requirement. The commutation performance of BCIHCB2



(a) (b)

Figure 4.10: Fault current commutation. (a) BCIHCB1 (b) BCIHCB2.

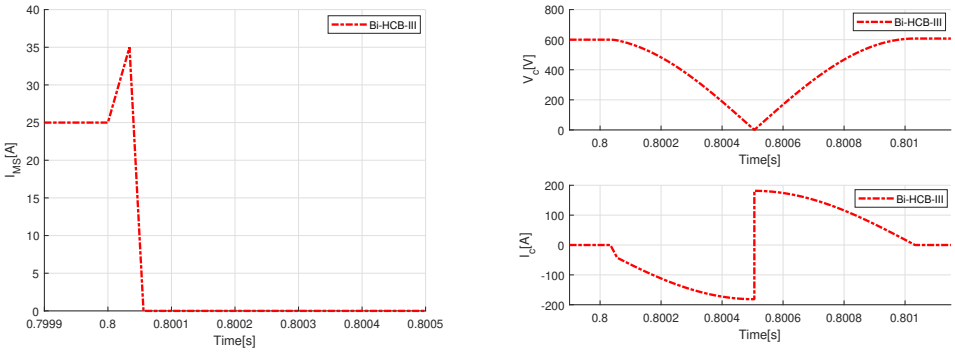


(a) (b)

Figure 4.11: Resistive load interruption for BCIHCB3. (a) Main breaker current. (b) Capacitor voltage and current.

in the reverse power mode is shown in Fig. 4.10(b). The current commutation time t_f is 1.1 ms, due to a larger self-inductance L_{s_2} and the increase in equivalent series inductance of the commutation circuit, as shown in Fig. 4.8(b).

The resistive load interruption process for BCIHCB3 is shown in Fig. 4.11(a)-(b). The main breaker current is forced to zero in 10 μs. The commutation capacitor is charged to a positive voltage of $2V_g$. As a result, BCIHCB3 can also be utilized for reclosing operation. Fig. 4.12(a)-(b) illustrates identical waveforms in mode-III during a short-circuit fault, where current commutation time t_f is found to be 50 μs.



(a) (b)

Figure 4.12: Fault interruption for BCIHCB3. (a) Main breaker current. (b) Capacitor voltage and current.

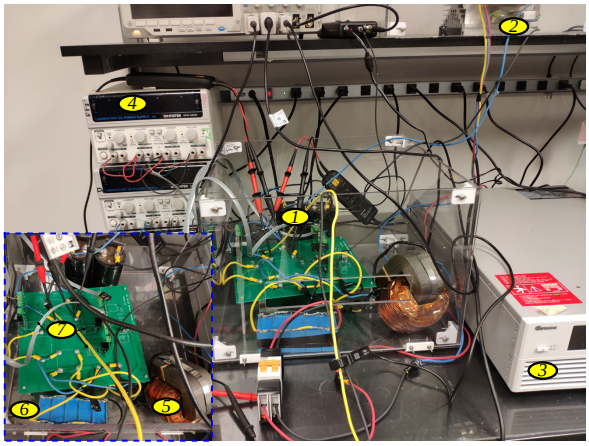


Figure 4.13: Experimental setup. 1. DCCB prototype. 2. Diode Rectifier. 3. DC Power Supply. 4. Driver power supply. 5. Coupled Inductor. 6. Commutation capacitor. 7. Thyristors.

Nonetheless, the fault response time is well below the specification [49].

4.7 Experimental Evaluation

The performance of BCIHCB1 is evaluated using a 6 kW laboratory prototype. As the breaking operation of BCIHCB1 is identical in the forward and reverse power mode, a two-winding coupled inductor with the parameter L_{s_2} in Table 4.1 is used in the test setup. A single switch is used as the main breaker to reduce the gate-driving

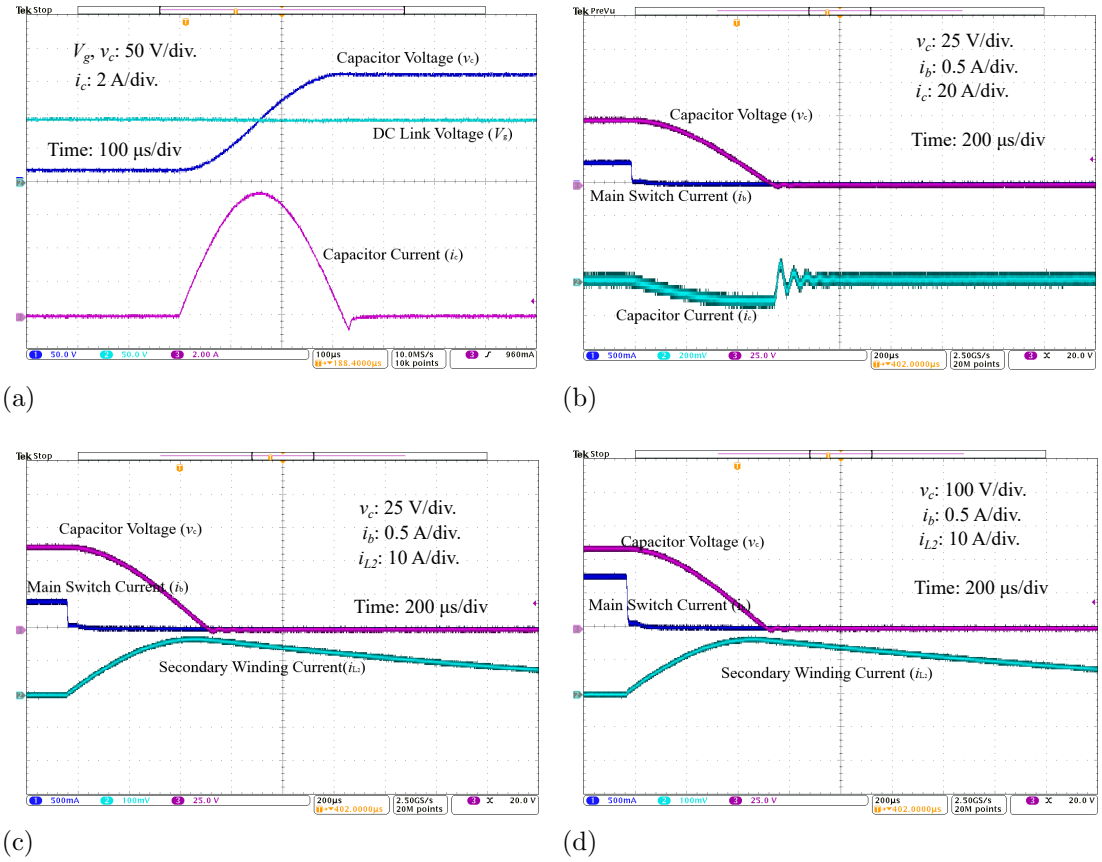
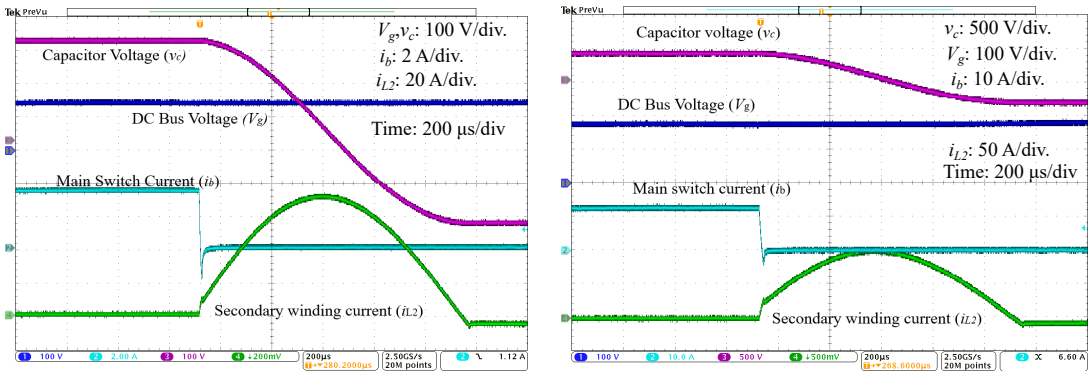


Figure 4.14: Low power results. (a) Charging mode. (b)-(d) Resistive load current interruption.

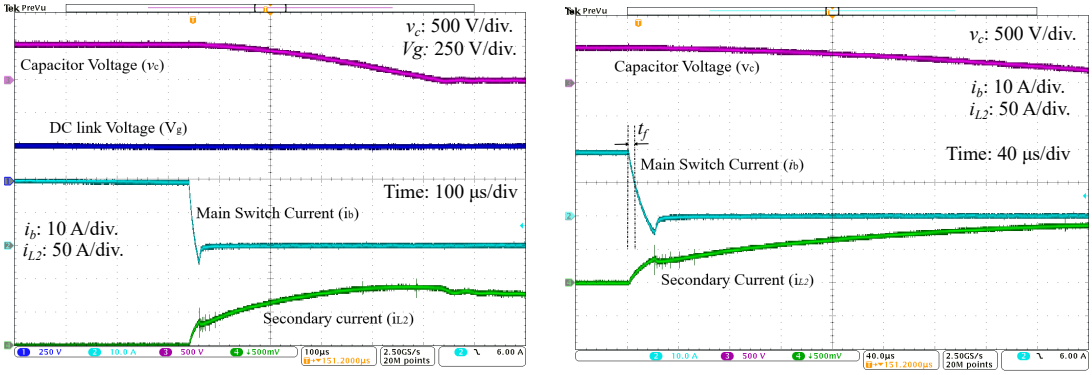
circuitry. Switching devices are implemented by rectifier-grade thyristors (TM8050H-8W). Transient i_c and i_2 waveforms are captured using a Rogowski transducer of 10 mV/A sensitivity. Fig. 4.13 shows the experimental prototype.

Fig. 4.14 depict the test results at low power. Fig. 4.14(a) shows the capacitor voltage and current during the resonant charging mode following the turn-on of T_2. The capacitor is charged to 160 V for a source voltage V_g= 90 V. The small negative value of capacitor current i_c after the current zero-crossing is caused by the reverse-recovery of T_2. After T_2 turns off, the charged capacitor remains in floating condition. The current commutation process for a resistive load of 141 Ω are highlighted in Fig. 4.14(b) and (c). The series thyristor is commutated within 40 μs. The capacitor is bypassed by a



(a) (b)

Figure 4.15: Resistive load interruption without clamping diode. (a) I_L= 4 A. (b) I_L= 13 A.



(a) (b)

Figure 4.16: Resistive load interruption with clamping diode. (a) I_L= 20 A. (b) Magnified mode-III.

clamping diode following the zero-crossing of v_c, which forces i_c to zero as well. The secondary winding current decays to zero exponentially. Fig. 4.14(d) shows the same waveforms for a load resistance of 70 Ω.

Experimental results at high power involve the resistive load interruption test of BCIHCB1 topology with and without clamping diode. Fig. 4.15(a) and (b) highlight the commutation of 4 A and 13 A load currents without capacitor-bypassing. It is observed that the counter-current in Fig. 4.15(b) is higher. Current commutation period t_f increases from 10 μs to almost 20 μs. Also, the capacitor is charged to a

negative voltage which corresponds to the operation described in section 4.2.

Fig. 4.16 depicts current commutation in the presence of a capacitor-bypassing diode. The commutation of 20 A load current is shown in Fig. 4.16(a). The current through the series thyristor (i_b) is forced to zero within 20 μs, as the pre-fault capacitor voltage is higher. When v_c is discharged to zero in mode-IV, the clamping diode conducts and the capacitor is bypassed. The clamping action results in a lower peak value of the secondary current. Fig. 4.16(b) shows 10 A current commutation over an amplified time-scale. The measured value of t_f is around 7 μs.

4.8 Discussion

The proposed bidirectional HCBs provide fast fault response in the range of 100 μs, which is validated by the simulation and experimental waveforms. The BCIHCB1 topology is compared with bidirectional Z-source circuit breaker topologies tested at comparable power levels [112], [114], [115]. The comparison results are tabulated in Table 4.2 which reveals that the proposed CIHCB provides a much faster current commutation ($\sim$ 40 μs). The fault commutation time includes the thyristor reverse-recovery period. Also, the proposed topology incorporates only one inductor and one capacitor, which is significantly less number of components compared to the other topologies. The reduced number of storage elements implies a lower breaker footprint, which is advantageous for subsea implementation within pressure compensated chambers. Also, the $R-D$ snubbers incorporated in the bidirectional ZSCB topologies are not required for BCIHCB topologies.

Similar to the CIHCB topologies in chapter 3, BCIHCB topologies exhibit low conduction power loss during the operation as a DC switch, due to the low on-state voltage

Table 4.2: Comparison of Bidirectional DC Breakers

Category	[112]	[114]	[115]	BCIHCB1
Number of Storage Elements	5	7	5	2
Number of Switches	5	4	4	4
Snubber Required	Yes	Yes	No	No
Response Time	132 μs	190 μs	158 μs	40 μs

drop of the series-path thyristor. Efficiency can be further improved by using mechanical breakers in the series path. Also, BCIHCB topologies behave as low pass filters during the operation as a DC switch, as given by equation (3.25). Hence, the BCIHCB topologies can be easily interfaced with power converters in the subsea distribution feeders.

4.9 Conclusion

This chapter presents three coupled inductor based bidirectional HCBs. The main features of these topologies are listed below.

- Proposed solutions provide fast current commutation with ZCS turn-off of the series path switch. Experimentally measured response time is found to be within 50 μs.
- Arcless breaking operation can be obtained in the case of mechanical breakers.
- Charging of the commutation capacitor does not involve a pre-charging circuit.
- No passive snubber or varistor is required for overvoltage suppression.
- Proposed solutions provide high efficiency while operating as a DC switch.

The current commutation performance is validated by simulation and experimental results.

4.10 Publications

1. A. Ray, K. Rajashekara and S. N. Banavath, "Bidirectional Coupled Inductor Based Hybrid Circuit Breaker Topologies for DC System Protection," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 1138-1145.

2. A. Ray, S. N. Banavath and K. Rajashekara, "Coupled Inductor Based Hybrid DC Circuit Breaker Topologies for DC Grid Application," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, 2018, pp. 1116-1121.

Chapter 5

Modular DC Breakers for Fault Protection in Subsea Microgrids

5.1 Introduction

The development of a reliable, high capacity subsea power grid is the foremost priority for the next-generation subsea processing. The ring-type power distribution system, such as the modular HVDC architectures presented in chapter 2, is the most suitable option for subsea capacity expansion. More number of subsea processing loads, as well as renewable generation, will be electrically interconnected to the subsea HVDC distribution bus in the future, which increases the fault level of the subsea HVDC grid. This necessitates the capacity expansion of the HVDC switchgear.

The coupled inductor-based HCB (CIHCB) topologies in chapters 3 and 4 utilize a single LC resonant circuit for fault interruption. The I^2t capacity of these circuit-breakers is directly related to the stored energy ($\frac{1}{2}CV_c^2$) in the commutation capacitor. Hence, a larger capacitance is required for the desired breaking operation at a higher fault level. However, the increase in μF value reduces the characteristic impedance of the resonant circuit, which results in higher peak current stress of the passive elements and the switching devices. Another practical issue in CIHCB operation is caused due to capacitor leakage. Following the resonant charging mode, the commutation capacitor slowly discharges through its leakage resistance in the floating stage. This causes

a reduction in the pre-fault capacitor voltage. Subsequently, the fault interruption capacity of the switchgear also reduces.

To mitigate these issues, this chapter presents a modular circuit breaker which utilizes multiple synchronously resonating LC circuits to realize counter-current injection-based fault interruption. The proposed modular breaker consists of two coupled inductors whose primary windings are connected in parallel. Meanwhile, each secondary winding is part of a series resonant circuit. The parallel connection of the primary windings effectively doubles the reflected counter-current. The current commutation time is almost halved compared to the CIHCB topologies. The HVDC implementation may utilize more number of coupled inductors in this current-multiplier configuration, which would enhance the fault interruption capability of the switchgear. A modified topology with series-connected primary windings is also presented in this chapter. The series primary configuration is particularly useful for a thyristor-based implementation to prevent commutation failure due to insufficient reverse biasing of the thyristor. A detailed design method is presented in this chapter which addresses the reverse-recovery issue. The commutation performance of the proposed modular circuit breakers is evaluated using a 1 kW prototype unit.

5.2 Modular Circuit Breaker 1

Fig. 5.1(a) shows the schematic of the modular circuit breaker 1 with parallel primary (PP) configuration. The proposed circuit breaker uses two coupled inductors whose primary windings $1_a - 1'_a$ and $2_a - 2'_a$ are connected in parallel to realize a current-doubler network. Each secondary winding interfaces a capacitor and a half-bridge module of IGBTs or MOSFETs. Each capacitor (C_a or C_b) is maintained in charged condition from the DC source through the conduction of the diode (D_a or D_b)

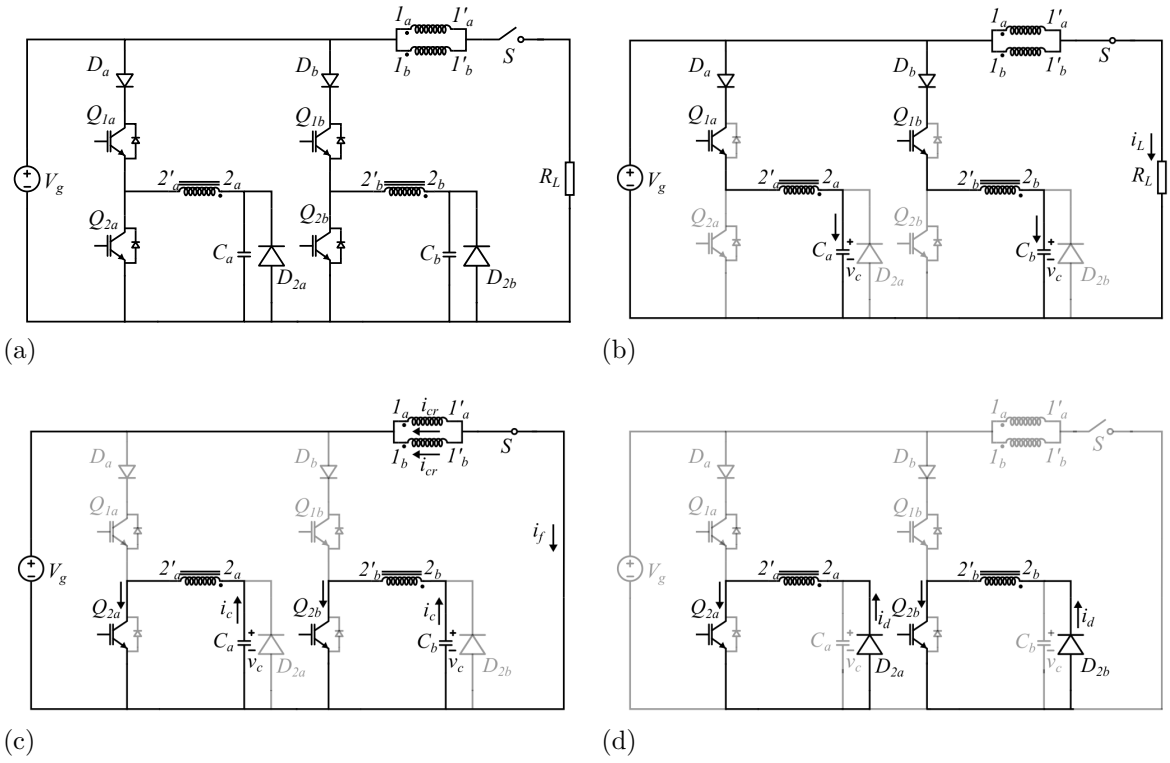


Figure 5.1: Modular DC breaker 1 with PP configuration. (a) Circuit Schematic. (b) Mode-I: charging and power delivery. (c) Mode-II: Commutation. (d) Mode-III: capacitor clamping.

and the active switch (Q_{1a} or Q_{1b}) in the upper half-bridge. This prevents the loss of stored energy due to the self-leakage of the capacitor. The counter-current injection from the charged capacitor during a fault is achieved by the synchronous conduction of the lower half-bridge switches Q_{2a} and Q_{2b}. Due to the parallel primary structure, the counter-current induced on the primary side is doubled. A clamping diode (D_{2a} or D_{2b}) is connected across each capacitor in antiparallel configuration. The clamp circuit reduces the peak blocking voltage of the main switch S during the capacitor discharging mode. Fig. 5.1(b) to (d) illustrates the operation of the proposed modular breaker. Corresponding voltage and current waveforms of the circuit elements are shown in Fig. 5.2.

5.2.1 Mode I ($t_0 \sim t_1$)

The upper-half bridge switches Q_{1a} and Q_{1b} are switched on at $t = t_0$. Charging current i_c follows the path $D_a - Q_{1a} - 2'_a 2_a - C_a$ for the half-bridge leg a, as shown in Fig. 5.1(b). The final voltage on each capacitor is equal to the DC source voltage V_g. The series path breaker S is also closed during this mode to establish power flow between the DC source and the load. Both Q_{1a} and Q_{1b} remain on till the fault detection to maintain a constant pre-fault voltage on the commutation capacitors.

5.2.2 Mode II ($t_1 \sim t_2$)

Gate pulses of the switches Q_{1a} and Q_{1b} are inhibited when a short-circuit fault is detected at $t = t'_2$. I_d denotes the preset fault detection level. The lower half-bridge devices Q_{2a} and Q_{2b} are switched on after a small dead-band period to avoid the short-circuit of the DC source. The capacitors C_a and C_b discharge through the secondary windings $2_a - 2'_a$ and $2_b - 2'_b$. For identical passive elements, the instantaneous counter-currents generated by the resonant circuits are identical and equal to i_c. Due to the parallel primary configuration, effective counter-injection to the fault current becomes $2i_{cr}$. The fault current i_f is forced to zero at $t = t_2$. The current commutation time ($t_f = t_2 - t'_2$) is almost halved compared to the CIHCB topologies. Main breaker S is switched off at the current zero-crossing instant to achieve arcless breaking operation. Fig. 5.1(c) illustrates the current conduction paths during this mode.

5.2.3 Mode III ($t_2 \sim t_3$)

The capacitors C_a and C_b continue to discharge through the secondary windings $2_a - 2'_a$ and $2_b - 2'_b$ as the discharging switches Q_{2a} and Q_{2b} remain in conduction.

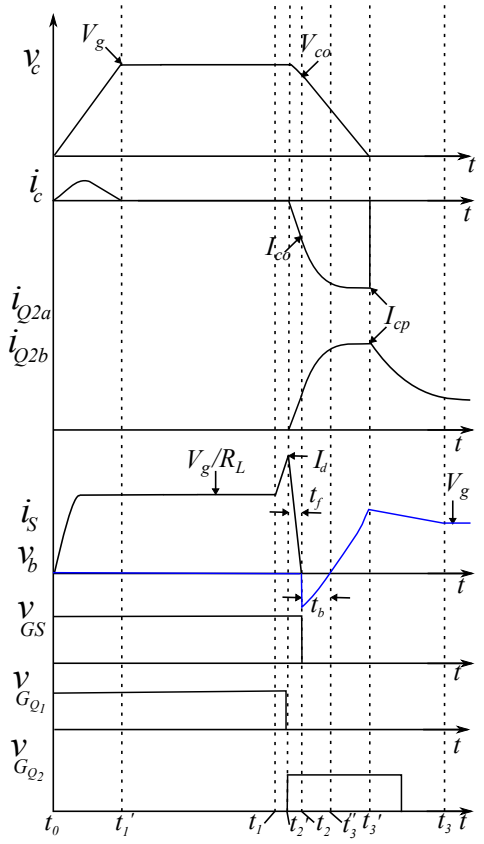


Figure 5.2: Operating waveforms of modular circuit breaker 1.

As the capacitor voltage v_c falls to zero at $t = t_3'$, the clamping diodes D_{2a} and D_{2b} are forward biased. The secondary currents continue to circulate through the paths $Q_{2a} - D_{2a} - 2_a - 2_a'$ and $Q_{2b} - D_{2b} - 2_b - 2_b'$ following an exponential discharging profile, shown in Fig. 5.1(d). The capacitors remain in bypassed condition, which limits the peak voltage stress on the main breaker S to V_g.

5.3 Modular Circuit Breaker 2

The modular circuit breaker 1 presented in section 5.2 provides faster fault response compared to the CIHCB topologies presented in the previous chapters. Fault response time can be further enhanced by increasing the number of parallel-connected windings. For n_p number of primary windings connected in parallel, the effective counter-current

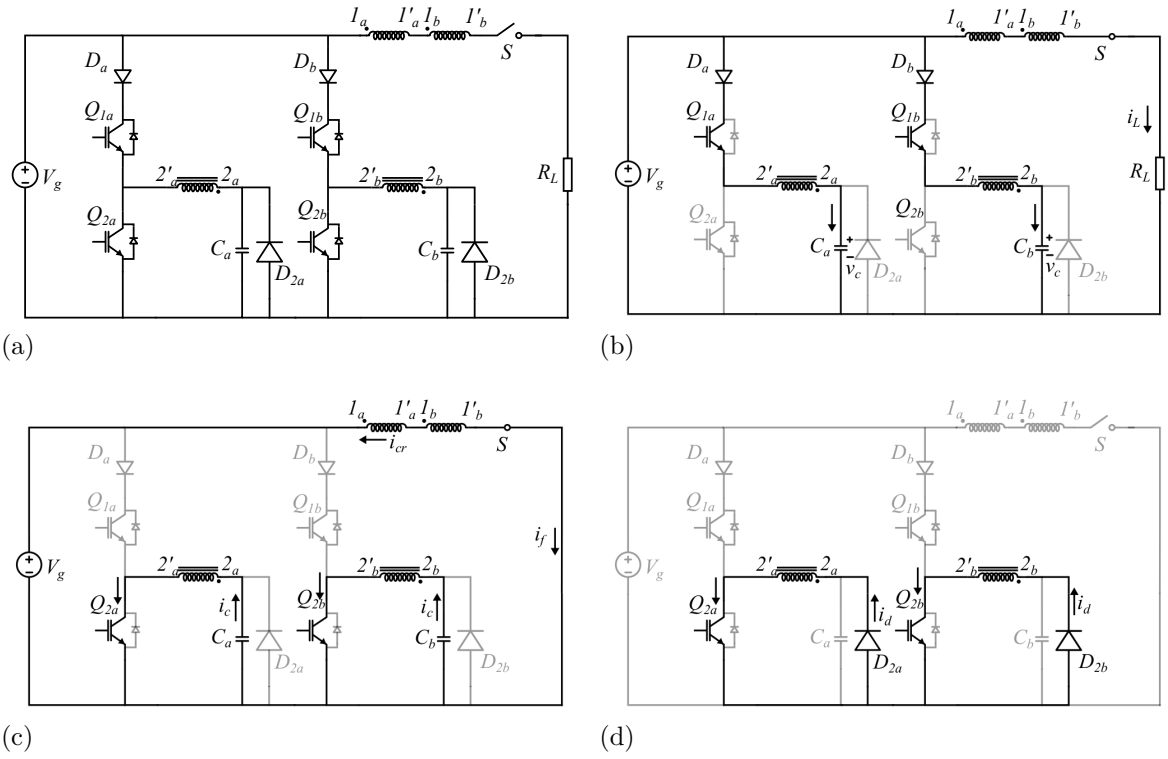


Figure 5.3: Modular DC Breaker 2 with SP Configuration. (a) Circuit Schematic. (b) Mode-I: charging and power delivery. (c) Mode-II:commutation. (d) Mode-III: capacitor clamping.

opposing the fault becomes $n_p i_{cr}$. Conversely, each secondary side resonant network needs to be designed for a counter-current of $\dfrac{i_{cr}}{n_p}$ to realize identical fault response to the CIHCB topologies. However, this design leads to a faster discharging of the capacitor in mode-III. The voltage across the main breaker S in mode-III is given by

$$v_b = V_g - nv_c. \tag{5.1}$$

Each coupled inductor has a turns ratio of n:1, where $n \geq 1$. The duration for which v_b is negative in mode III is known as the reverse-bias time and is denoted by t_b. When the main breaker S is implemented by a thyristor, the condition for successful current commutation is $t_b > t_{rr}$, where t_{rr} is the reverse-recovery period of the thyristor. However, as v_c reduces much faster for the proposed design, t_b is also reduced, which may result in commutation failure at higher fault current levels.

The commutation failure due to insufficient reverse-bias time can be prevented by increasing the reflected capacitor voltage on the primary side. Based on this concept, a modified circuit breaker is presented in Fig. 5.3(a). The modified circuit breaker, termed as modular circuit breaker 2, is identical to the modular circuit breaker 1, except the primary windings are connected in series instead of parallel. The operating modes of this topology with series primary (SP) configuration are depicted in Fig. 5.3(b)-(d). The current conduction paths in modes I, II, III are the same as the modular breaker 1. However, the reflected counter-current on the primary side is i_{cr} instead of $2i_{cr}$. Also, the blocking voltage of the main breaker S in mode III is given by

$$v_b = V_g - 2nv_c. \tag{5.2}$$

Consequently, the reverse-bias time (t_b) is increased which can ensure successful current commutation. With more number of series-connected primary windings, a further increase in t_b is achieved. Hence, the modular circuit breaker with series primary configuration is particularly useful for thyristor-based DC switch implementation.

5.4 Design Guidelines

The proposed modular circuit breakers are analyzed with the help of simplified equivalent circuits referred to the secondary winding in each operating mode, as in the case of CIHCB topologies. However, due to a non-unity turns ratio, the equivalent circuit parameters differ from the CIHCB topologies. The design procedure is simplified by the following assumptions.

- All the passive elements have identical parameters, which reduces the problem to a single equivalent circuit per mode.
- Self-inductance of the primary and secondary windings are related as $L_1 = n^2 L_2$,

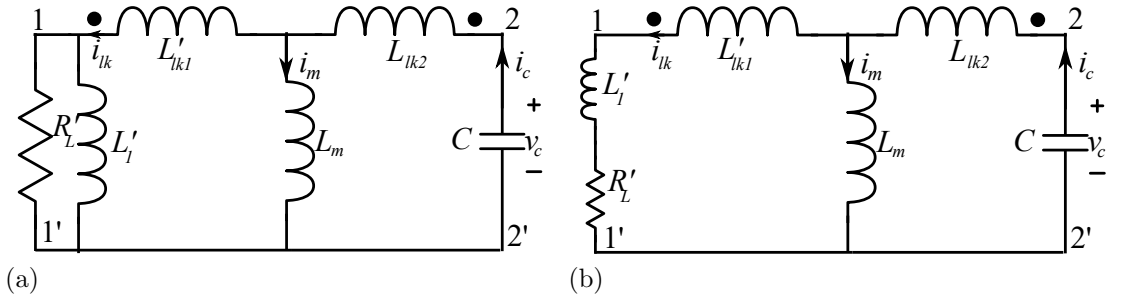


Figure 5.4: Equivalent circuits during current commutation. (a) Modular breaker 1. (b) Modular breaker 2.

where n denotes the turns ratio.

- Equivalent series resistance of the coupled inductors and the switches are neglected.

5.4.1 Current Commutation Mode

Fig. 5.4 (a) and (b) depict the respective equivalent circuits for modular circuit breakers 1 and 2 in the current commutation mode for a load resistance R_L. The principal difference in the two equivalent circuits depends on the connection of the primary windings. L'_1 represents the self-inductance of the other primary winding referred to the secondary winding. Also, R'_L represents the load resistance referred to the secondary winding. These parameters are mathematically expressed as

$$L'_1 = \frac{L_1}{n^2} \quad \text{and} \qquad R'_L = \frac{R_L}{n^2}. \tag{5.3}$$

The leakage inductance of primary and secondary windings are denoted as L_{lk1} and L_{lk2}, respectively. L'_{lk1} represents the primary leakage inductance referred to the secondary winding and is given by

$$L'_{lk1} = \frac{L_{lk1}}{n^2} = L_{lk2}. \tag{5.4}$$

The secondary leakage inductance can also be expressed as

$$L_{lk2} = (1 - k)L_2, \tag{5.5}$$

where L_2 is the self-inductance of the secondary winding and k represents the coefficient of coupling. Mutual inductance of the coupled inductor, referred to the secondary, is given by

$$L_m = kL_2. \tag{5.6}$$

The knowledge of the current and voltage profile of the commutation capacitor is important for evaluating the fault response of the modular breakers. The derivation process follows equations (3.1) to (3.21). The capacitor voltage and current as a function of time for a short-circuit fault (R_L=0) are given by

$$i_c(t) = \frac{V_g}{Z_{e1}} \sin \omega_{e1}(t - t_2') \quad \text{and} \tag{5.7}$$

$$v_c(t) = V_g \cos \omega_{e1}(t - t_2'), \tag{5.8}$$

where, Z_{e1} and ω_{e1} are the characteristic impedance and the resonant frequency of the series resonant network, and they are expressed as

$$Z_{e1} = \sqrt{\frac{L_{eq,2}}{C}} \quad \text{and} \qquad \omega_{e1} = \frac{1}{\sqrt{L_{eq,2}C}}. \tag{5.9}$$

$L_{eq,2}$ is the equivalent series inductance of the resonating commutation network. The difference in fault response of the two modular breakers arises due to different values of $L_{eq,2}$, which are given by the equations

$$L_{eq,2} = (1 - k^2)L_2 \quad \text{and} \tag{5.10}$$

$$L_{eq,2} = (1 - \frac{k^2}{2})L_2. \tag{5.11}$$

Equation (5.10) represents $L_{eq,2}$ value for modular breaker 1 while the same for topology 2 is given by Equation (5.11).

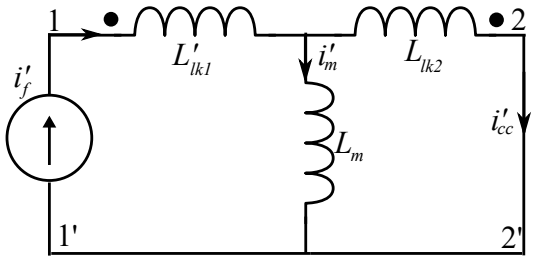


Figure 5.5: Equivalent circuit representing counter-induction by fault current.

The counter-induced current i'_{cc} through the secondary leakage branch due to the counter-induction by the fault current is determined from Fig. 5.5 as

$$i'_{cc}(t) = ki'_f(t), \tag{5.12}$$

where i'_f is the counter-induced current source for modular breaker 1 and 2, respectively, and it is expressed by the equations

$$i'_f(t) = \frac{2V_g}{nL_2}(t - t_1) \quad \text{and} \tag{5.13}$$

$$i'_f(t) = \frac{V_g}{2nL_2}(t - t_1). \tag{5.14}$$

From the superposition of the equivalent circuits in Fig. 5.4 and Fig. 5.5, the expressions of the actual counter-current for topology 1 and 2 are respectively found from the equations (5.15) and (5.16) as

$$i_{cr}(t) = \frac{V_g}{nZ_{e1}} \sin \omega_{e1}(t - t'_2) - \frac{2kV_g}{n^2L_2}(t - t_1) \quad \text{and} \tag{5.15}$$

$$i_{cr}(t) = \frac{V_g}{nZ_{e1}} \sin \omega_{e1}(t - t'_2) - \frac{kV_g}{2n^2L_2}(t - t_1). \tag{5.16}$$

It can be inferred from the above equations that due to a lower Z_{e1} and a higher ω_{e1} value, as well as the current doubling effect, modular breaker 1 can provide a faster fault commutation compared to the topology 2 with series-connected primaries. However, topology 2 reflects a larger voltage opposing the source voltage in the primary, which enhances the reverse-bias time and reduces the probability of commutation failure.

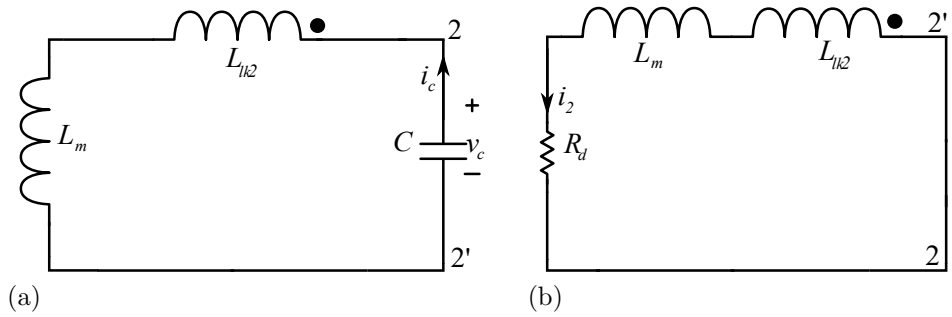


Figure 5.6: Equivalent circuits during mode-III. (a) Capacitor discharging. (b) Capacitor clamping.

5.4.2 Capacitor Discharging Mode

The equivalent circuits in mode-III are shown in Fig. 5.6(a) and (b), to respectively represent the capacitor discharging operation ($t_2 < t < t_3'$)) and the clamping action by the bypassing diodes D_{2a} and D_{2b} ($t > t_3'$). The series resonant circuit in Fig. 5.6(a) is mathematically depicted by the equations

$$v_c(t) = V_{co}\cos\omega_e(t-t_2) - Z_e I_{co}\sin\omega_e(t-t_2) \quad \text{and} \tag{5.17}$$

$$i_c(t) = \frac{V_{co}}{Z_e}\sin\omega_e(t-t_2) + I_{co}\cos\omega_e(t-t_2). \tag{5.18}$$

Characteristic impedance Z_e and resonant frequency ω_e of this circuit are given by

$$Z_e = \sqrt{\frac{L_2}{C}} \quad \text{and} \qquad \omega_e = \frac{1}{\sqrt{L_2 C}}. \tag{5.19}$$

When the capacitor is bypassed by the clamping diode following the zero-crossing of v_c, the secondary current i_2 exponentially decays due to the ESR of the network (R_d) as

$$i_2(t) = |I_{cp}|e^{-\frac{R_d}{L_2}t}, \tag{5.20}$$

where I_{cp} represents the peak capacitor current.

Equations (5.1)-(5.20) are utilized to design the coupled inductor and the commutation capacitor following the design procedure of the CIHCB topologies.

5.4.3 Expression of Reverse-Bias Time

The expression of the blocking voltage in equation (5.1) can be re-written with the help of (5.17) as

$$v_b(t) = V_g - nV_{co}\cos\omega_e(t-t_2) + nZ_eI_{co}\sin\omega_e(t-t_2). \tag{5.21}$$

V_{co} and I_{co} represent the initial capacitor voltage and current when mode-III begins, and they are expressed as

$$V_{co} = V_g\cos\omega_{e1}(t_2-t_2') = V_g\cos\omega_{e1}t_f \quad \text{and} \tag{5.22}$$

$$I_{co} = \frac{V_g}{Z_{e1}}\sin\omega_{e1}(t_2-t_2') = \frac{V_g}{Z_{e1}}\sin\omega_{e1}t_f. \tag{5.23}$$

$t_f = t_2 - t_2'$ is the current commutation time. Also, the reverse-bias time t_b is computed to be $t_b = t_3'' - t_2$, as $t = t_3''$ in Fig. 5.2 represents the zero-crossing instant of v_b. Using these expressions, (5.21) can be re-written as

$$V_g - nV_g\cos(\omega_{e1}t_f)\cos(\omega_e t_b) + nV_g\frac{Z_e}{Z_{e1}}\sin(\omega_{e1}t_f)\sin(\omega_e t_b) = 0. \tag{5.24}$$

For fast current commutation, i.e., low t_f, the angular terms are approximated as

$$\sin(\omega_{e1}t_f) \approx \omega_{e1}t_f \quad \text{and} \qquad\qquad \cos(\omega_{e1}t_f) \approx 1. \tag{5.25}$$

Consequently equation (5.24) can be modified as

$$V_g - nV_g\cos(\omega_e t_b) + nV_g\frac{Z_e}{Z_{e1}}\omega_{e1}t_f\sin(\omega_e t_b) = 0. \tag{5.26}$$

Replacing the values of Z_{e1} and ω_{e1} from (5.9) in (5.26), the expression is simplified as

$$1 - n\cos(\omega_e t_b) + \frac{nZ_e}{L_{eq,2}}t_f\sin(\omega_e t_b) = 0. \tag{5.27}$$

Equation (5.27) can be further simplified into the trigonometrical expression

$$M_b\sin(\omega_e t_b - \alpha_b) + \frac{1}{n} = 0. \tag{5.28}$$

The expression of the reverse-bias time t_b is obtained by re-arranging the above equation as

$$t_b = \frac{\alpha_b}{\omega_e} - \frac{1}{\omega_e}\sin^{-1}(\frac{1}{nM_b}). \tag{5.29}$$

Equation (5.29) represents the mathematical expression of the reverse-bias time t_b for modular circuit breaker 1 in terms of the circuit parameters. Indices M_b and α_b are expressed as

$$M_b = \sqrt{(\frac{Z_e t_f}{L_{eq,2}})^2 + 1} \quad \text{and} \qquad \alpha_b = \tan^{-1}(\frac{L_{eq,2}}{Z_e t_f}). \tag{5.30}$$

Similarly, the reverse bias time for topology 2 with series-connected primaries can be found from equation (5.2) as

$$t_b = \frac{\alpha_b}{\omega_e} - \frac{1}{\omega_e}\sin^{-1}(\frac{1}{2nM_b}). \tag{5.31}$$

Indices M_b and α_b have the same expression as in (5.29), except the values of $L_{eq,2}$ which are given by equations (5.10) an (5.11) for topology 1 and 2, respectively.

From (5.29) and (5.31), it is observed that α_b is higher for topology 2 due to a higher value of $L_{eq,2}$. The negative term of the expression is also smaller, which implies that the modular breaker 2 manifests a longer reverse-bias duration compared to topology 1 with parallel-primary configuration. This increases the probability of successful commutation for thyristor-based implementation of the DC breaker.

The reverse-bias time t_b is particularly dependent on the commutation capacitance value. With a larger μF value, the capacitor discharging becomes slower which increases the reverse-bias time. Fig. 5.7 plots the reverse-bias time t_b for the proposed topologies as a function of the commutation capacitance, for a fixed current commutation time. In line with (5.29) and (5.31), t_b is significantly larger for modular breaker 2. Also, it is observed from the figure that a higher capacitance increases t_b significantly. However, an increase in the μF value increases the peak current stress on the devices and the

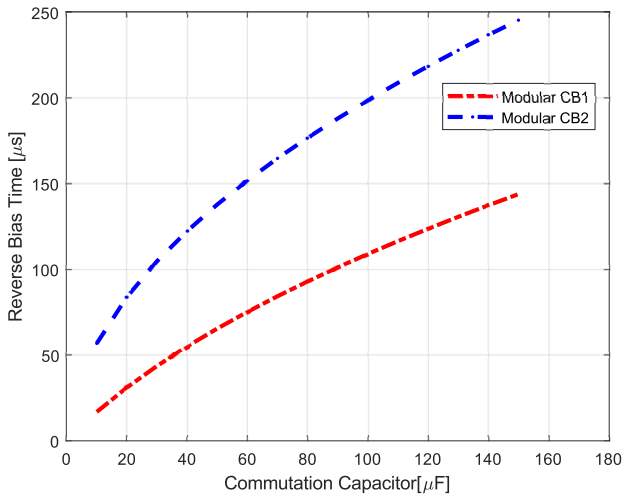


Figure 5.7: Reverse-bias time as a function of commutation capacitance.

passive elements. Hence, a judicious design choice of C is required to ensure successful current commutation without increasing the component ratings.

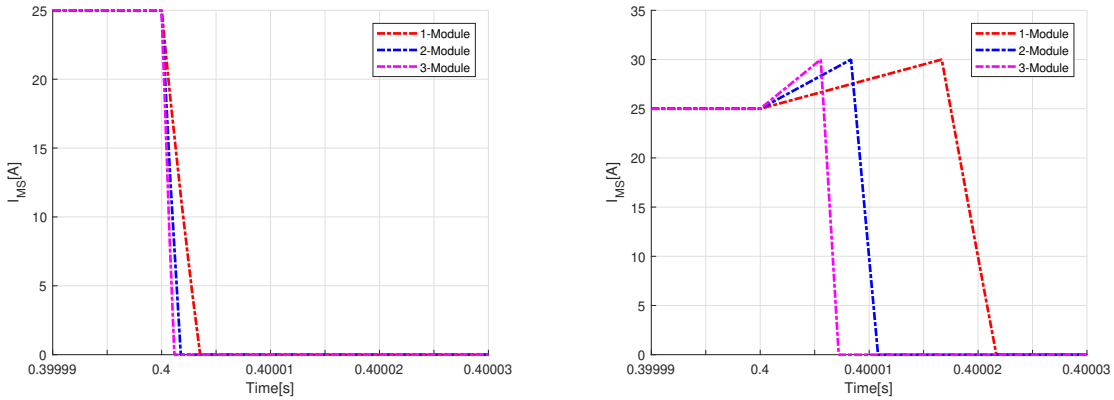
5.5 Simulation Results

The analysis and design of the modular circuit breakers are verified by simulation in PLECS for a 100 V DC system with currents up to 25 A. The parameters used for the simulation are tabulated in Table 5.1. Nonetheless, the proposed design in scalable. In actual HVDC implementation, only the passive element design needs to be modified. Also, the number of windings in series or parallel has to be increased to account for a higher fault current interruption.

Fig. 5.8 (a) and (b) provides a comparison of the current commutation times for a different number of half-bridge modules during resistive load interruption and short-circuit fault, respectively. With only one module, the topology resembles the CIHCB topologies with a single coupled inductor. The 2-module configuration is the proposed modular breaker 1. Current commutation time t_f is greatly reduced for the 2-module

Table 5.1: Parameter and Component Details of Modular Breakers

Parameters	Symbol	Description
Rated Voltage	V_g	100 V
Rated Current	I_L	25 A
Coupled Inductor 1	L_1	871.9 μH : 248.7 μH
Coupled Inductor 2	L_2	962.4 μH : 252.7 μH
Commutation Capacitor	C	100 μF
Components	**Symbol**	**Part Number**
Thyristors	S	TM8050H-8W
Diodes	D_a, D_b, D_{2a}, D_{2b}	VS-40EPS08PBF-ND
Capacitors	C_a, C_b	B32778P8206K000
Half-bridge devices	$Q_{1a}, Q_2a, Q_{1b}, Q_{2b}$	BSM300D12P2E001

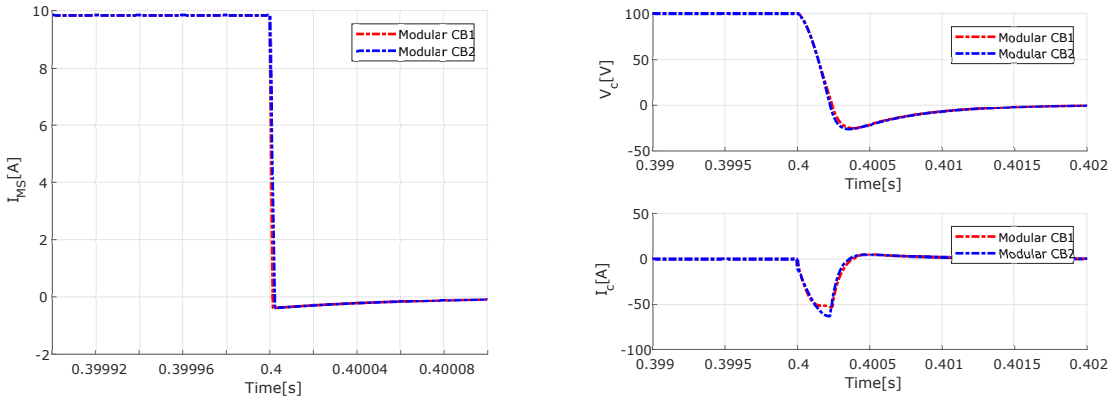


(a) (b)

Figure 5.8: Comparison of current commutation time with different number of coupled inductors. (a) Resistive load. (b) Fault.

design compared to single module design, especially during a short-circuit fault interruption. A further reduction of t_f is achieved by using 3 half-bridge modules. Hence, a progressively faster fault response is obtained by increasing the number of coupled inductors.

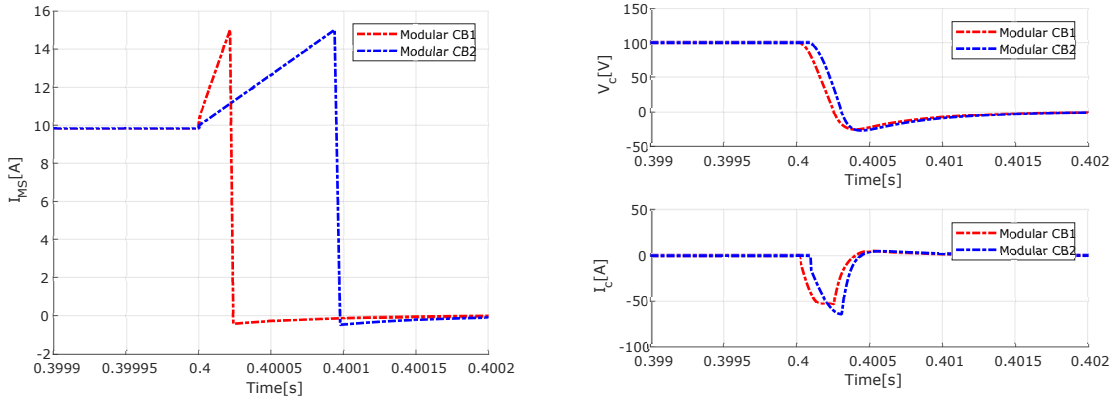
Commutation of 10 A resistive load current for the two modular breakers are shown in Fig. 5.9. Current through the main breaker S is shown in Fig. 5.9(a). Response times of both topologies are almost equal, within 5 μs. Capacitor voltage and current during mode-II and III are shown in Fig. 5.9(b), and they are identical for the proposed



(a) (b)

Figure 5.9: Resistive load current interruption. (a) Main breaker current. (b) Capacitor voltage and current.

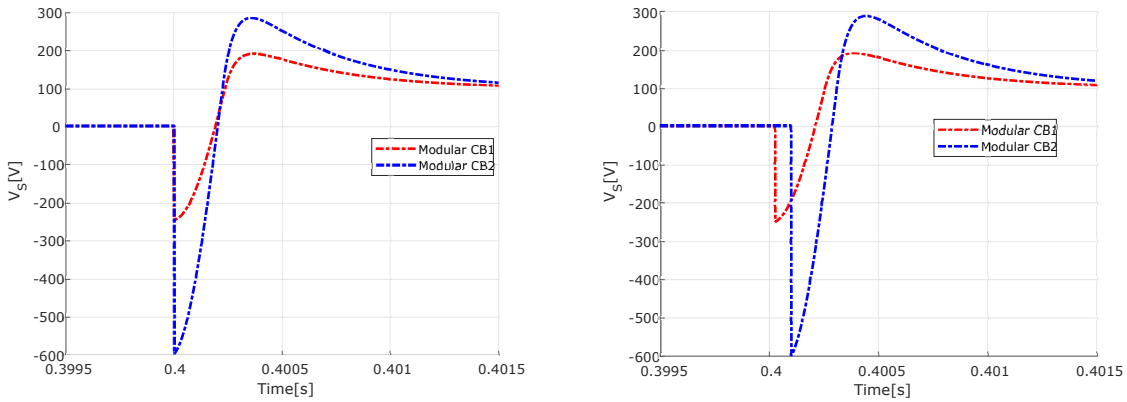
modular breakers 1 and 2. Same waveforms for a short-circuit fault interruption are shown in Fig. 5.10(a) and (b). Fault response time significantly differs in this case, as observed from Fig. 5.10(a). Commutation time t_f is around 20 μs for modular breaker 1 and almost 100 μs for modular breaker 2. This result verifies design equations (5.15) and (5.16). The effect of the current doubling is more pronounced, which significantly reduces the current commutation time for modular breaker 1.



(a) (b)

Figure 5.10: Fault interruption. (a) Main breaker current. (b) Capacitor voltage and current.

Fig. 5.11(a)-(b) depict the blocking voltage profile of the main breaker S during



(a) (b)

Figure 5.11: Blocking voltage profile of main breaker. (a) Resistive load. (b) Fault.

resistive load and short-circuit fault interruptions. The revers-bias duration (t_b) for topology 2 is not substantially longer compared to the first topology. This can be explained by a longer commutation period (t_f) for modular breaker 2. As t_b decreases with increasing t_f, the overall effect of the series-connection of primary windings is not pronounced. However, the peak reverse voltage is much higher in the second topology, which aids in a faster reverse-recovery of the thyristor and increases the probability of a successful commutation process.

5.6 Experimental Evaluation

A thyristor based 1 kW prototype is developed to verify the commutation performance of the proposed modular circuit breakers 1 and 2, as shown in Fig. 5.12. The prototype specification is provided in Table 5.1. The main breaker is implemented by a high-temperature, standard-recovery thyristor (TM8050H-8W). SiC MOSFETs with high peak current capability (BSM300D12P2E001) are used for constructing the half-bridge modules. Transient current waveforms are recorded using a Rogowski coil based transducer of 10 mV/A sensitivity. The gate pulses to the switches are provided

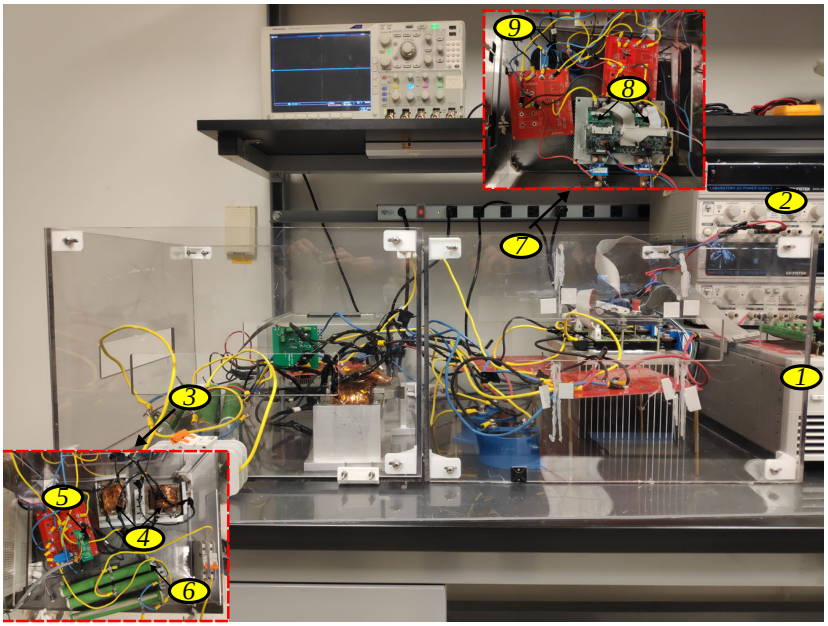
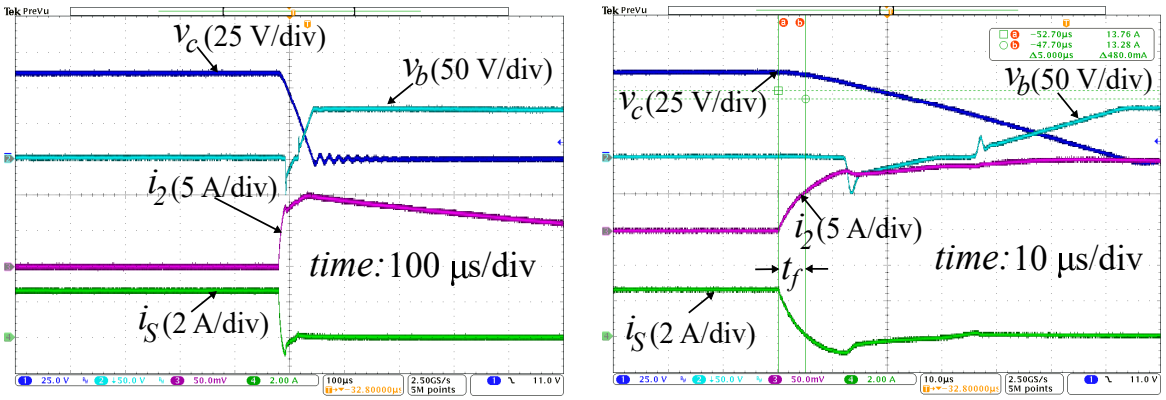


Figure 5.12: Experimental setup. 1. DC Power Supply. 2. Driver power supply. 3. Parallel or series-connected primary. 4. Coupled inductors 5. Main switch. 6. Load. 7. Secondary side. 8. Half-bridge modules. 9. Commutation capacitor.

through a TI TMS320F28379D DSP board and an Altera MAX-II CPLD based control board.

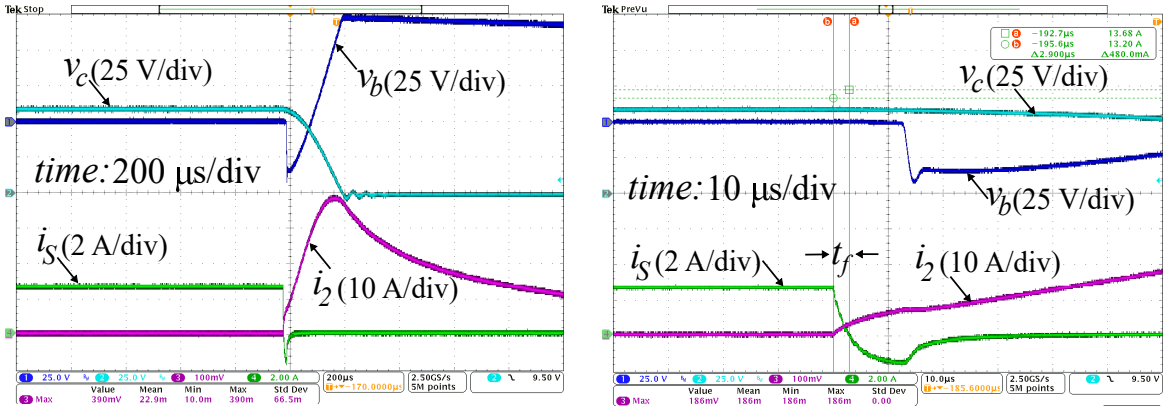
5.6.1 Comparison of Current Commutation Time

The prototype unit is first tested at V_g=60 V and I_S=2.8 A with only one half-bridge module, i.e., one coupled inductor. Fig. 5.13(a)-(b) depict the current commutation process. From Fig. 5.13(b), current commutation time t_f is computed to be 5 μs for a single module-based design. Identical testing conditions are used to determine the commutation time for the proposed modular breaker 1 with two half-bridge modules. Corresponding waveforms are shown in Fig. 5.14. Current commutation time, in this case, is found to be 2.9 μs, i.e., t_f is almost halved with two coupled inductors instead of one. These results closely match the simulation results illustrated in Fig. 5.8 to demonstrate the improvements with a modular circuit breaker design.



(a) (b)

Figure 5.13: Current commutation with one module. (a) I_S=2.8 A. (b) Magnified mode-II.

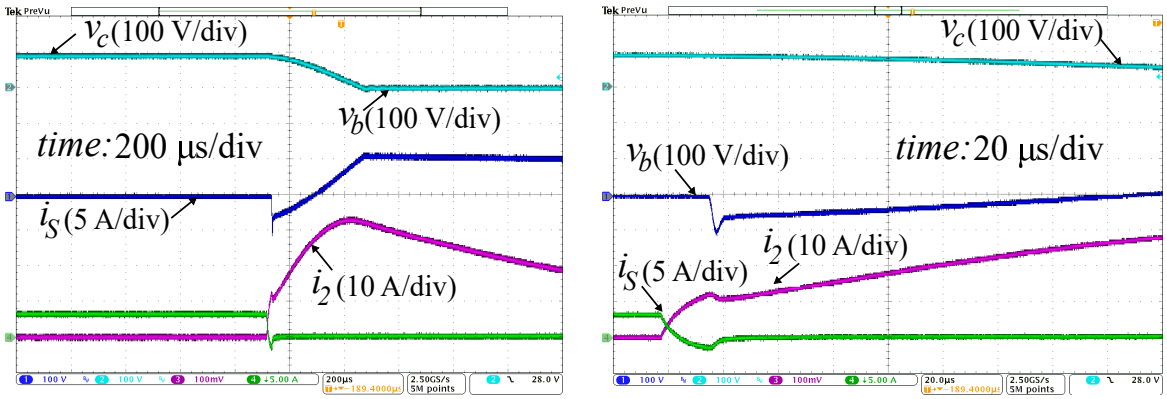


(a) (b)

Figure 5.14: Current commutation with two modules. (a) I_S=2.8 A. (b) Magnified mode-II.

5.6.2 Commutation Performance of Modular Breaker 1

The performance of the modular breaker 1 with PP configuration is verified by resistive load current interruption process at different values of V_g and i_S. Fig. 5.15 (a) and (b) depicts the current commutation process for a load resistance R_L=28.6 Ω at a DC bus voltage V_g=100 V. The proposed design achieves successful current commutation within 8 μs. Also, the peak blocking voltage stress on the main breaker S is limited to V_g. Fig. 5.16 depicts the current interruption mechanism for a smaller

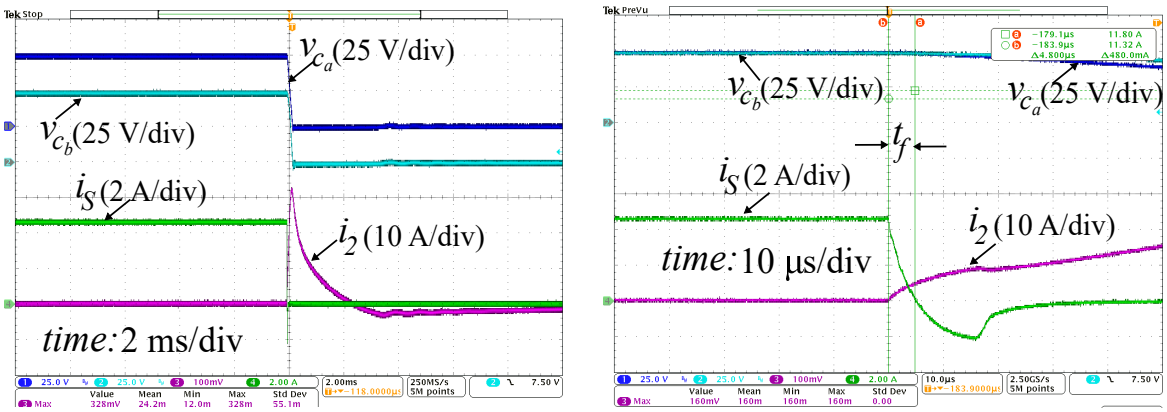


(a) (b)

Figure 5.15: Experimental results at R_L=28.6 Ω. (a) Current commutation. (b) Magnified mode-II.

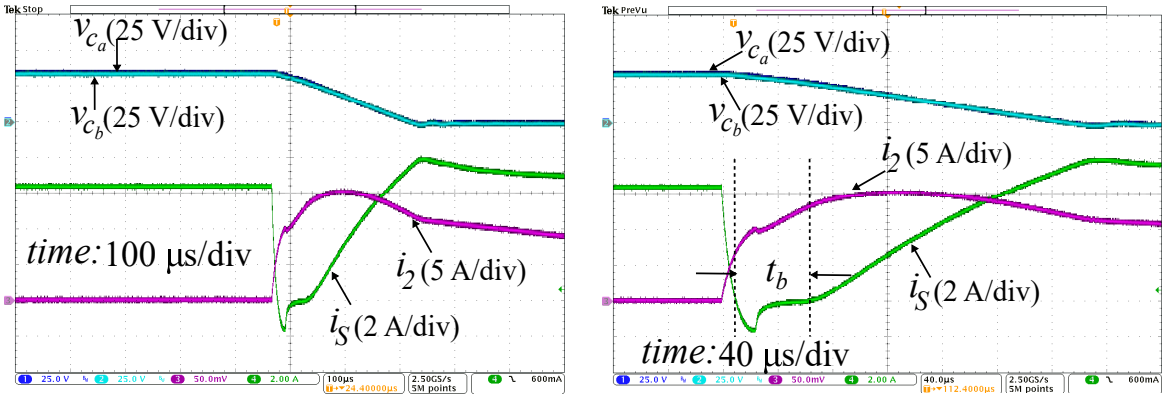
load resistance of 10 Ω. Fig. 5.16(a) illustrates the secondary side resonance in mode-II and III over a 2 ms/div. time scale. Commutation capacitors C_a and C_b have an identical discharging profile. The secondary current i_2 decays exponentially following the capacitor voltage zero-crossing due to the clamping diodes. Fig. 5.16(b) shows the mode-II resonance in a magnified scale. Commutation time t_f is found to be 4.8 μs which closely matches the simulated value.

The proposed modular breaker 1 can provide a distinctly fast fault response. However, as explained in section 5.4, the reverse-bias time is not sufficient at some load currents to complete the reverse-recovery of main thyristor S. Consequently, the current commutation is unsuccessful and the thyristor S returns to current conduction state. Fig. 5.17 (a) and (b) depict commutation failure at V_g=40 V and i_S=6 A. Although the thyristor current i_S is forced to zero in 8 μs, the reverse-bias time of t_b=52 μs is not sufficient to complete the reverse-recovery process of the thyristor S. The experimental prototype uses a standard-recovery thyristor whose turn-off time t_q is almost 150 μs. Hence, thyristor S transits to the conduction mode again. This phenomenon can be avoided by using a fast-recovery thyristor using wide bandgap material or a voltage-controlled switch. Another option to prevent commutation failure is to



(a) (b)

Figure 5.16: Experimental results at R_L=10 Ω. (a) Current commutation. (b) Magnified mode-II.



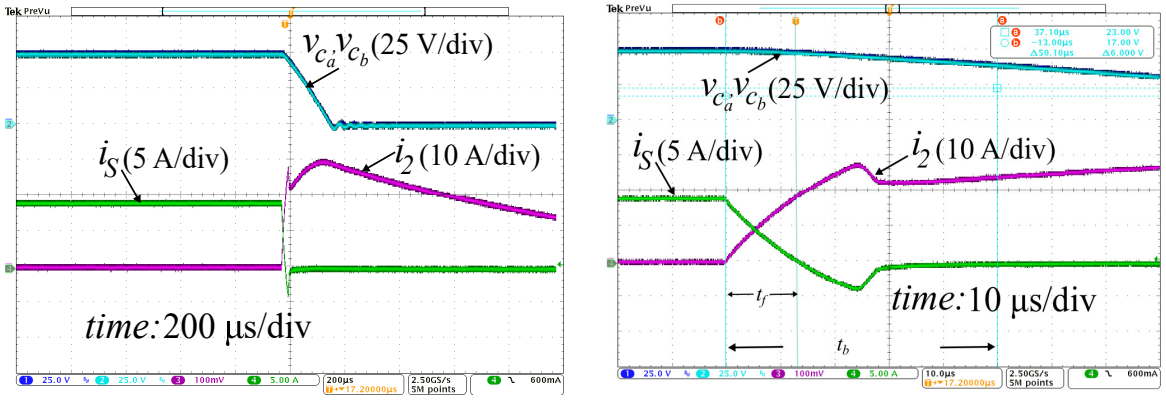
(a) (b)

Figure 5.17: Thyristor reverse-recovery issue. (a) Commutation failure. (b) Magnified mode-III.

employ the modular breaker 2 with series-primary configuration.

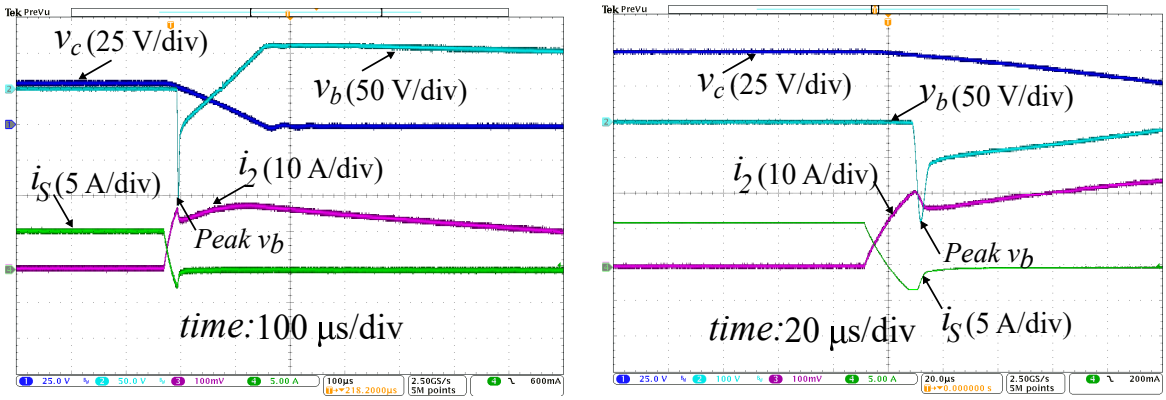
5.6.3 Commutation Performance of Modular Breaker 2

Fig. 5.18 illustrates the interruption of 9 A load current at V_g=50 V for modular breaker 2 with series primary configuration. The commutation capacitors C_a and C_b have an equal capacitance of 100 μF. Conduction of the discharging switches Q_{2a} and Q_{2b} causes a steep initial slope of the secondary current i_2, which is also the measure



(a) (b)

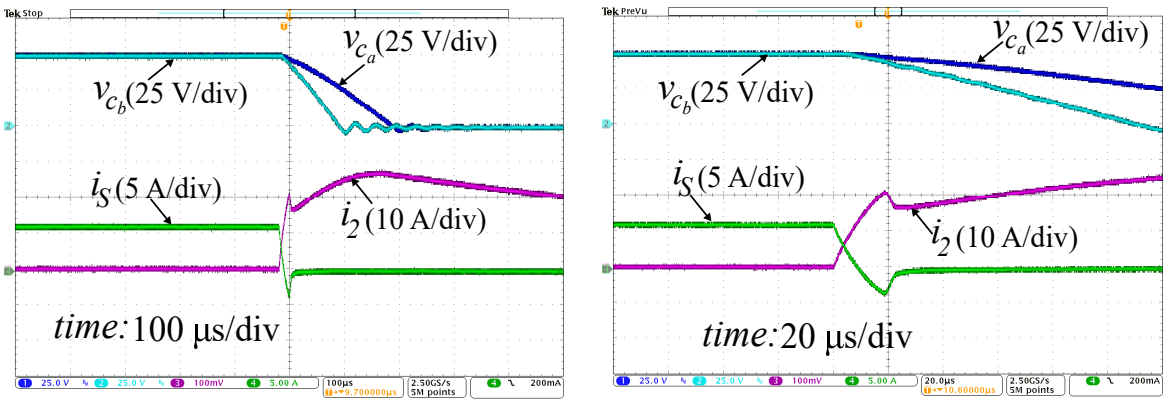
Figure 5.18: Experimental results for modular breaker 2. (a) Current commutation. (b) Magnified mode-III.



(a) (b)

Figure 5.19: Blocking voltage waveforms for modular breaker 2. (a) V_g=30 V. (b) V_g=50 V.

of counter-current, as shown in Fig. 5.18(a). Fig. 5.18(b) depicts the commutation process over a magnified time scale. Commutation time t_f is 12 μs, while the reverse-bias time is t_b=50.1 μs. Nonetheless, this value of t_b is sufficient to complete the reverse-recovery of the main thyristor S. The faster reverse-recovery is caused by a high peak reverse voltage on the switch S, as shown in Fig. 5.19 (a) and (b). It is observed from these figures that the peak reverse voltage on the thyristor is almost 5 times the DC bus voltage. Due to such a high blocking voltage, a faster recombination process is realized. As a result, the thyristor undergoes a short reverse-recovery which



(a) (b)

Figure 5.20: Experimental results for modular breaker 2 with unequal capacitors. (a) Current commutation. (b) Magnified mode-III.

minimizes the possibility of commutation failure.

Fig. 5.20 shows the commutation of 6 A load current for unequal commutation capacitors. The two secondary resonant networks consist of capacitors C_a=100 μF and C_b=40 μF, respectively. Except the different discharging profiles of the capacitors, the rest of the waveforms remain the same as in previous cases. Commutation time t_f is around 12 μs, which demonstrates fast fault response.

5.7 Discussion

Modular breakers with current-doubler or voltage-doubler configuration are capable of faster fault response compared to the CIHCB topologies presented in chapter 3. The modular circuit breaker 1 provides a response time as low as 2 μs. Also, the fault response property is scalable for an HVDC system by modifying the passive element design. Thus, the proposed topologies are suitable for DC grids with possible capacity expansion, as more number of switch modules can be easily retrofitted with the existing design. Moreover, the capacitor leakage problem is eliminated in the proposed modular circuit breakers, which make them suitable choices for subsea operation with a long

Table 5.2: Evaluation of Modular Breakers

Category	CIHCB1	CIHCB2	Modular CB1	Modular CB2
Number of Storage Elements	2	2	4	4
Number of Switches	3	7	5	5
Snubber Required	No	No	No	No
Low-pass filtering	Yes	Yes	Yes	Yes
Response Time	30 μs	30 μs	5 μs	15 μs

lifetime. Like CIHCBs, the presented modular breakers mitigate the requirement of snubber circuit based overvoltage protection. Also, the efficiency is comparable with the CIHCBs. Table 5.2 provides a brief comparison between the CIHCB topologies and the modular breakers.

5.8 Summary

This chapter presents two modular DC circuit breakers with the following features.

- Extremely fast-fault response in the range of 5-10 μs. Arcless breaking is achieved for mechanical breakers.
- Capacitor self-leakage problem is eliminated. Also, snubbers or varistors are not required.
- Retrofitting is easy for an HVDC implementation.

5.9 Publications

1. A. Ray and K. Rajashekara, "Design of Modular Circuit Breakers with Enhanced Fault Interruption Capability for DC Microgrids," submitted to IEEE Journal of Emerging and Selected Topics in Power Electronics.

Chapter 6

A Single Phase Resonant Power Supply for Direct Electric Heating of Subsea Pipelines

6.1 Introduction

Direct electric heating (DEH) is a cost-effective solution to prevent hydrate formation in subsea oil transfer pipelines. A DEH system utilizes the heating effect of alternating electric current to maintain the production flow temperature above the critical temperature. In a typical DEH system, a single-phase current of line frequency and constant amplitude is circulated through the metallic subsea pipelines. The alternating current produces ohmic (I^2R) loss in the pipeline which is manifested as heat. Two types of DEH technologies are found in practice, namely DEH-WIP and DEH-PIP [133]. Nonetheless, all DEH systems can be represented by the same equivalent electrical network, shown in Fig. 6.1 [130].

Although DEH is the least expensive flow assurance method, it encounters several issues in the power processing stage. One of the main drawbacks of a DEH system is a poor power factor. The DEH pipeline is electrically modeled as a single-phase RL load, as seen from Fig. 6.1. As the pipe material is usually carbon steel with high relative permeability (μ_r) value, the pipeline is highly inductive. This results in a load power factor of around 0.25. Thus, a large amount of reactive power is required from the topside source for a long pipeline. To reduce the VAr requirement from the

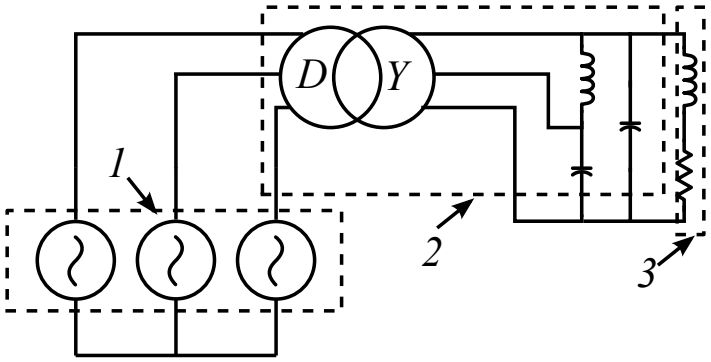


Figure 6.1: Equivalent Electrical Network of a DEH System. 1. Topside source. 2. Load balancing and compensation network. 3. DEH load.

source, external reactive compensation units are required. Also, as the active power demand ranges in MW, the topside source has to be equipped with transformers and load balancing networks for supplying the single-phase current to the DEH load. All of these issues affect the efficacy of the current DEH technology.

Another drawback of the existing DEH system is low heating efficiency. In the DEH-WIP system, the current return through seawater causes heat loss. This problem is alleviated in the DEH-PIP system. Nevertheless, the heating efficiency is still not optimized as the heat generation depends mostly on the conduction power loss. The contribution of hysteresis loss in the pipe to the heating effect is negligible for existing line-frequency based DEH systems. However, recent studies have shown that a higher frequency operation improves the heating efficacy significantly due to the increase in hysteresis loss generation. The hysteresis loss is measured to be one-third of the total power loss in the pipeline at a frequency of 200 Hz [136]-[137]. Hence, a high-frequency current injection is desirable for DEH application.

This chapter proposes a novel DEH power supply, based on high-frequency LCCL resonant inverter (LCCL-RI), to address the aforementioned issues [152]. The LCCL-RIs are supplied from the subsea distribution bus of the modular HVDC architectures presented in chapter 2. The proposed resonant inverter operates as a high-frequency,

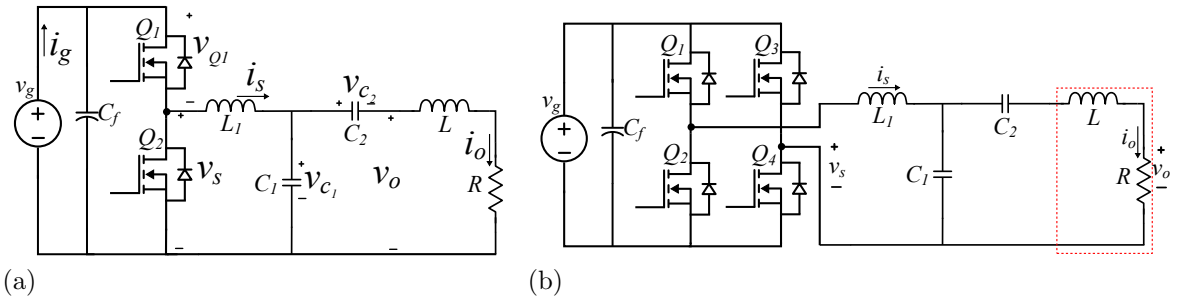


Figure 6.2: LCCL resonant inverter. (a) Half-bridge topology. (b) Full-bridge topology.

constant-current source that eliminates the topside AC source. The constant-current operation is also load-independent. The resonant tank is tuned at the frequency of peak current gain, which minimizes the DC source current and enables ZVS of the inverter switches. The LCCL-RI also exhibits inherent short-circuit protection. The tank capacitors provide compensation of the load inductance. Hence, no external reactive compensation is required. A design guideline to operate the LCCL-RI at the maximum tank current gain is presented in this chapter. A SiC MOSFET based 1 kW prototype unit is developed to evaluate the performance of the proposed LCCL-RI at different loading conditions.

6.2 LCCL Resonant Inverter for DEH Power Supply

The proposed LCCL resonant inverter is shown in Fig. 6.2 (a) and (b) for half-bridge and full-bridge configurations. Both topologies are identical in operation, except for the power handling capability. Load inductance L is included in the series-parallel tank network. The switches Q_1-Q_4 are modulated with 50% duty cycles to excite the resonant tank with a square-wave voltage. The loaded quality factor of the resonant tank is high ($\sim$ 3.5 to 4) due to the large load inductance. Hence, the load current i_o is sinusoidal. The output current becomes independent of the load resistance R if the

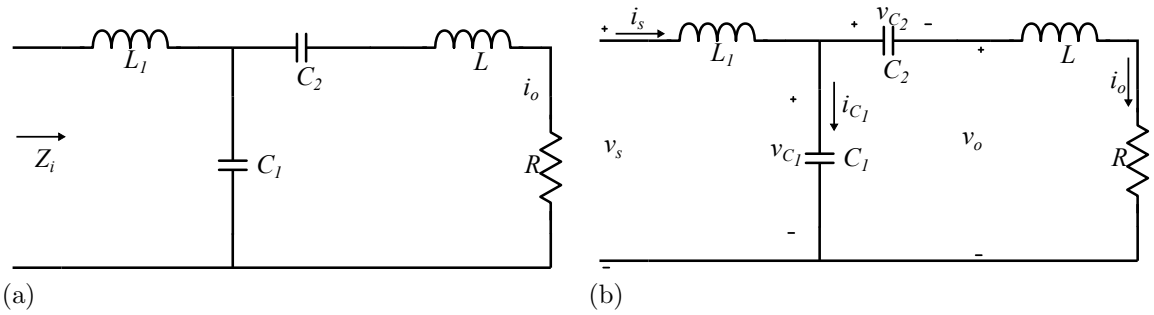


Figure 6.3: LCCL resonant tank. (a) Input impedance. (b) Current gain.

switching frequency f_s is above the corner frequency of the parallel resonant branch consisting of L_1 and C_1 [148]-[149].

The design equations of the LCCL-RI are derived using the fundamental harmonic approximation technique. The LCCL resonant tank is designed to accomplish the following objectives.

- The tank input current i_s is minimized for a constant amplitude of i_o. This is achieved when the inverter is switched at the frequency of the peak tank current gain.
- The tank input impedance is inductive at the operating frequency which ensures ZVS of the inverter switches Q_1 to Q_4.

6.2.1 Tank Input Impedance

The series-parallel tank network is re-drawn in Fig. 6.3(a) and (b) to illustrate the derivation of input impedance and current gain of the tank. From Fig. 6.3(a), the tank input impedance in the Laplace domain can be written as

$$Z_i(s) = sL_1 + [\frac{1}{sC_1}||(\frac{1}{sC_2} + sL + R)]. \tag{6.1}$$

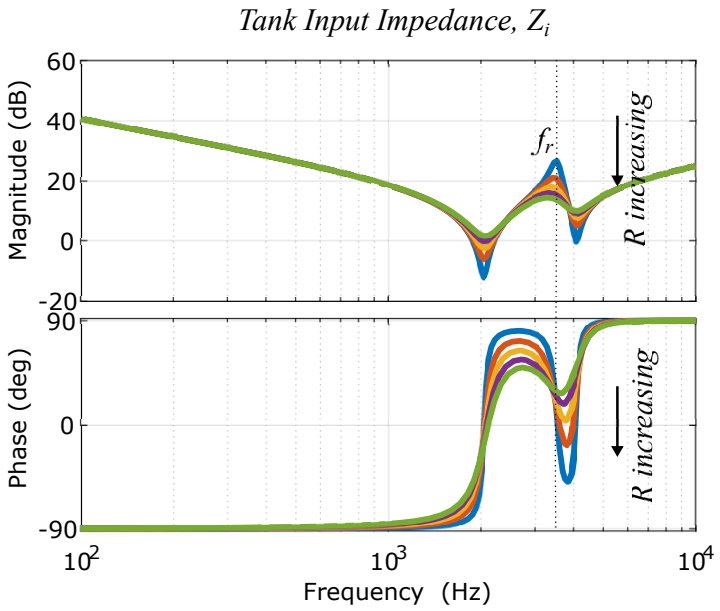


Figure 6.4: Frequency response of the tank input impedance.

Equation (6.1) is further expanded as

$$Z_i(s) = \frac{s^3 L L_1 C_1 + s^2 L_1 C_1 R + s L_1(1+\alpha) + sL + \frac{1}{sC_2}}{s^2 L C_1 + s C_1 R + (1+\alpha)}, \tag{6.2}$$

where $\alpha = \dfrac{C_1}{C_2}$ denotes the ratio of the tank capacitors. The above expression can be re-written as

$$Z_i(s) = \frac{s^4 L C_2 L_1 C_1 + s^3 L_1 C_1 C_2 R + s^2[L_1(1+\alpha) + L] + 1}{sC_2(1+\alpha)(s^2 \frac{LC_1}{1+\alpha} + s\frac{C_1 R}{1+\alpha} + 1)}. \tag{6.3}$$

The tank corner frequencies are defined as

$$\omega_p = \sqrt{\frac{1}{L_1 C_1}}, \qquad \omega_L = \sqrt{\frac{1}{LC_2}}, \quad \text{and} \qquad \omega_r = \sqrt{\frac{1+\alpha}{\alpha L C_2}}. \tag{6.4}$$

Using (6.4), the simplified expression of the tank input impedance is found as

$$Z_i(s) = \frac{\frac{s^4}{\omega_p^2 \omega_L^2} + \frac{s^3}{Q_L \omega_p^2 \omega_L} + s^2(\frac{1}{\omega_L^2} + \frac{1+\alpha}{\alpha \omega_p^2}) + 1}{sC_2(1+\alpha)(\frac{s^2}{\omega_r^2} + \frac{s}{Q_r \omega_r} + 1)}. \tag{6.5}$$

$Q_L = \dfrac{1}{R}\sqrt{\dfrac{L}{C_2}}$ and $Q_r = \dfrac{1}{R}\sqrt{\dfrac{L(1+\alpha)}{\alpha C_2}}$ indicate the quality factors of the load branch and the equivalent series branch, respectively.

The tank input impedance $Z_i(s)$ is plotted against frequency for different load resistance (R) values in Fig. 6.4. Z_i has the maximum amplitude at the corner frequency $f_r = \frac{\omega_r}{2\pi}$. Also, the phase of $Z_i(s)$ is positive at this frequency, i.e., the resonant tank impedance is inductive. Hence, operation at $f = f_r$ will ensure ZVS of the inverter switches.

6.2.2 Tank Current Gain

The current gain of the LCCL tank is expressed as the ratio of load current i_o to the fundamental component of tank input current i_s. The expression of current gain H_i is derived by applying KCL in Fig. 6.3(b). The fundamental component of i_s can be expressed in Laplace domain as

$$I_{s_1}(s) = I_o(s) + sC_1V_{C_1}(s). \tag{6.6}$$

Applying KVL in the load side loop in Fig. 6.3(b), the parallel capacitor voltage is expressed as

$$V_{C_1}(s) = I_o(s)(\frac{1}{sC_2} + sL + R). \tag{6.7}$$

Combining equations (6.6) and (6.7), and using the expressions of the corner frequencies given in (6.3), the expression of tank current gain is simplified as

$$H_i(s) = \frac{i_o(s)}{i_{S_1}(s)} = \frac{\frac{1}{1+\alpha}}{\frac{s^2}{\omega_r^2} + \frac{s}{Q_r\omega_r} + 1}. \tag{6.8}$$

Frequency response of the tank current gain $H_i(s)$ is illustrated in Fig. 6.5 for different R values. It is observed from the figure that the magnitude of the peak current gain decreases with an increase of R. However, the frequency at which the peak current gain occurs is always f_r. The maximum tank input impedance also occurs at f_r irrespective of the load resistance. Hence, the switching frequency of the

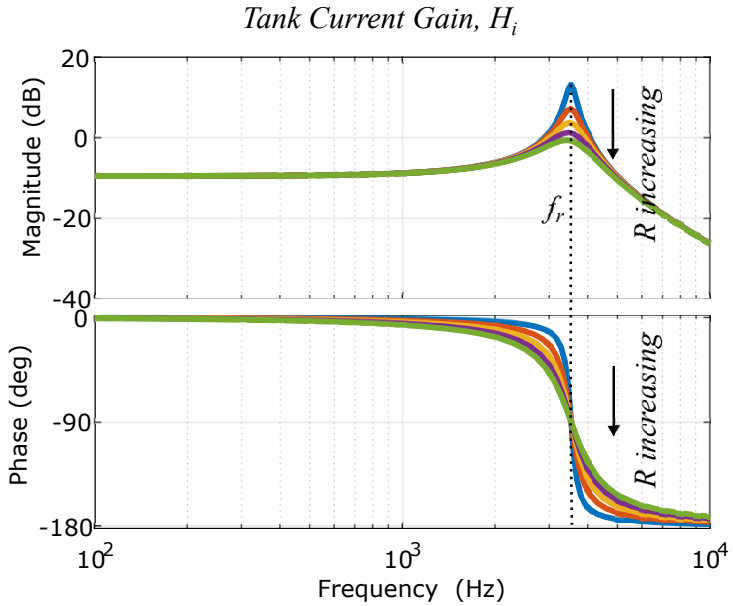


Figure 6.5: Frequency response of the tank current gain.

LCCL-RI is chosen to be f_r to minimize i_{S_1}, and subsequently the DC source current i_g. Moreover as $f_r > f_p$, the load current i_o is independent of the load resistance.

Equation (6.5) reveals that the magnitude of Z_i increases with a large tank capacitance ratio α. However, a large α reduces the amplitude of peak current gain. Hence, the choice of α should be prioritized to maximize H_i. The laboratory-based prototype unit is designed for α=2.

6.3 Simulation Results

Following the procedure explained in section 6.2, the LCCL-RI is designed for two different DEH systems. The first system refers to the rated power condition in a subsea implementation with a constant output current of 500 A peak-to-peak. The second system is the laboratory-based low power prototype with a peak output current up to 10 A. Table 6.1 provides the parameters for the LCCL-RI for both these power ratings. The switching frequency of the LCCL-RI is equal to the corner frequency f_r.

Table 6.1: Resonant Tank Parameters

Design	L_1	L	C_1	C_2	R	f_r	I_{o_p}
Rated Power	2.5 mH	9.2mH	50 μF	13.6 μF	2 Ω	507 Hz	500 A
Prototype	310 μH	622 μH	9.77 μF	5 μF	2.1 Ω	3.51 kHz	10 A

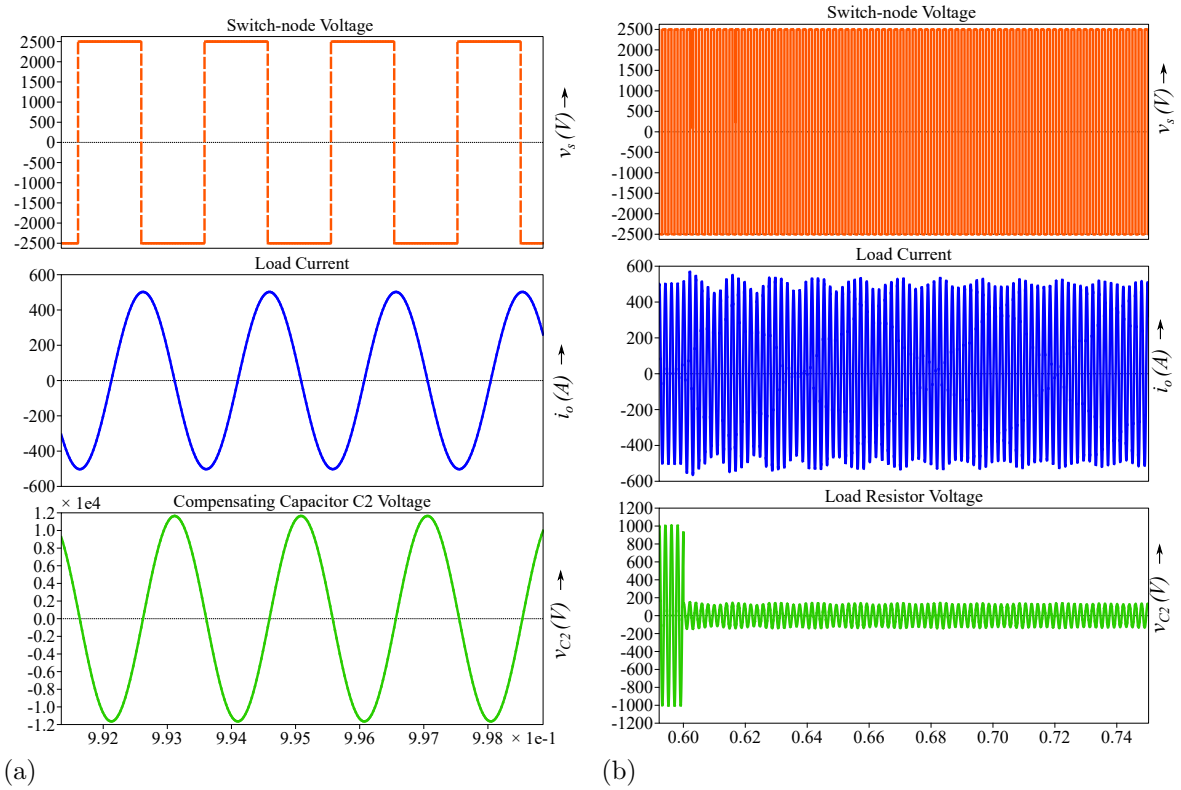


Figure 6.6: Simulation results at rated power. (a) Tank waveforms. (b) Load step-change.

Fig. 6.6 depicts the simulation waveforms at the rated power condition. The full-bridge topology is utilized for this simulation. The steady-state tank waveforms are shown in Fig. 6.6(a). It is observed that the sinusoidal load current i_o has an amplitude of 500 A. Also, i_o lags the zero-crossing of switch-node voltage (v_s) by more than 90^o. However, i_o also lags the fundamental tank input current i_{s_1} by 90^o at $f = f_r$,, which means that i_{s_1} lags the zero-crossing of the switch-node voltage as well. Thus ZVS turn-on of the inverter switches is obtained. Meanwhile, the series capacitor voltage (v_{C_2}) is in phase opposition to the load voltage v_o. Thus, the reactive drop in the

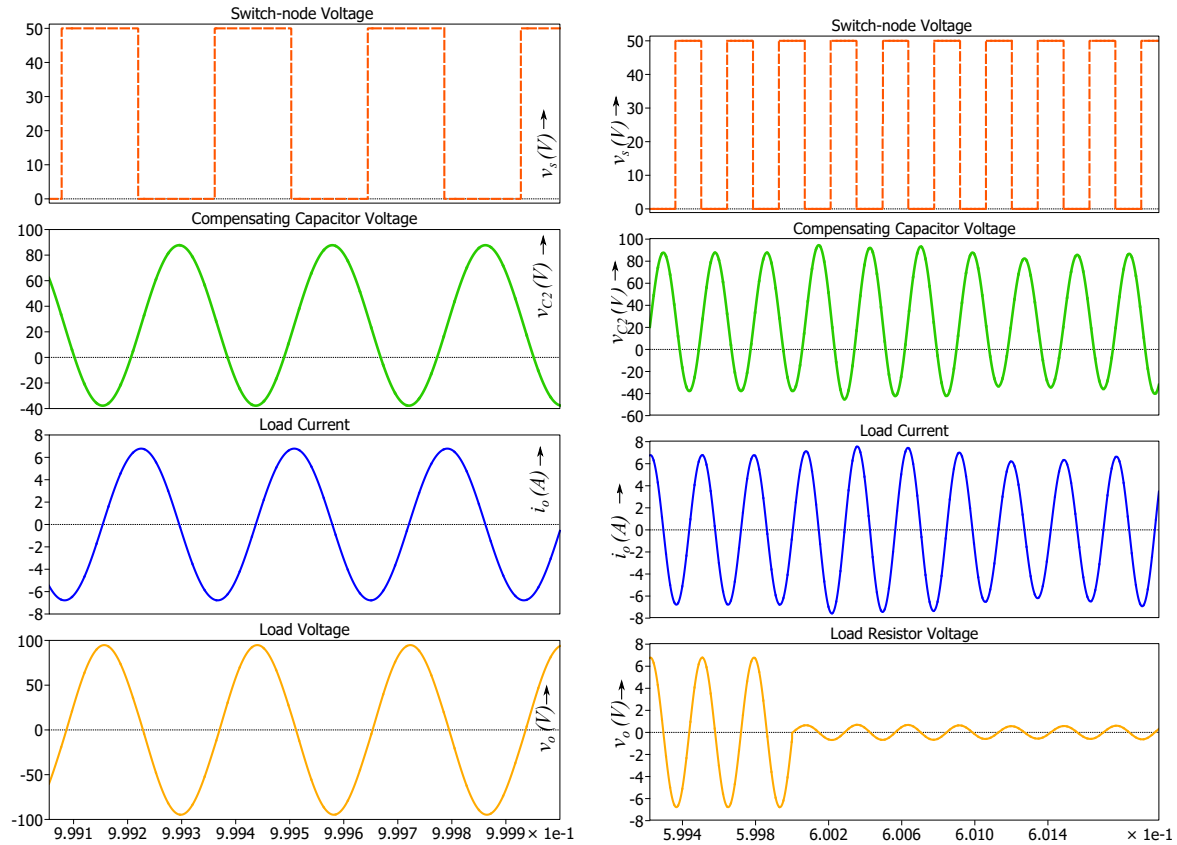


Figure 6.7: Simulation results for the prototype design. (a) Tank waveforms. (b) Load step-change.

output voltage v_o is compensated.

Fig. 6.6(b) highlights the inverter response for a step-change in load resistance, from 2 to 0.3 Ω. The amplitude of output current i_o remains the same after a few cycles of oscillation. Thus, the LCCL-RI acts as a constant current regulator. As the load resistance R reduces, the source current i_s also reduces in amplitude, implying an inherent short-circuit protection capability of the LCCL-RI.

The simulated inverter waveforms for the low power prototype unit are captured in Fig. 6.7(a) and (b). The switch-node v_s is a rectangular wave due to the half-bridge topology. Consequently, a DC offset is observed in the series capacitor voltage v_{C_2}. Nonetheless, the series compensation of the load reactance is still achieved. The tank

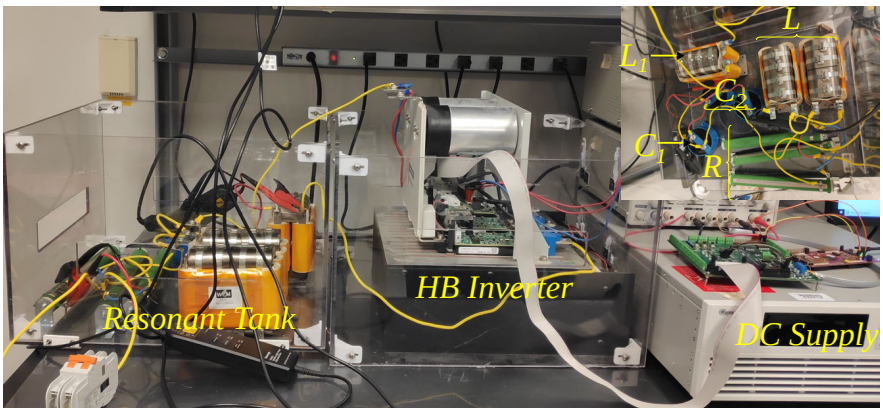


Figure 6.8: Hardware test setup of the LCCL-RI.

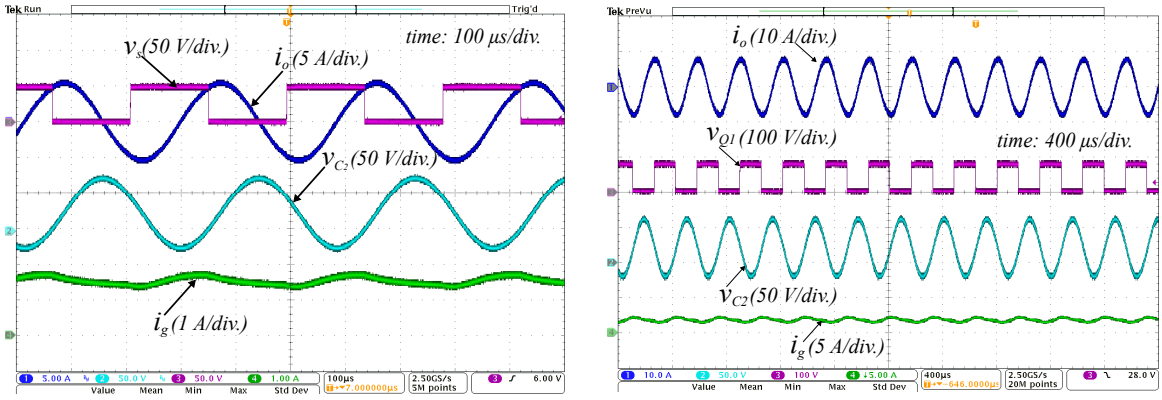
waveforms during the load step-change are shown in Fig. 6.7(b). The load current i_o is restored to its initial amplitude after 3-4 cycles, illustrating the current regulation capability of the inverter.

6.4 Experimental Verification

A SiC MOSFET based 1 kW prototype is developed to evaluate the current-regulation capability of the proposed LCCL-RI, as shown in Fig. 6.8. One SiC power module by AgileSwitch functions as the half-bridge inverter. The modulation scheme is implemented in a TI TMS320F28379D DSP board. An ALTERA MAX-II CPLD based control board is used to provide the gate pulses to the SiC MOSFETs.

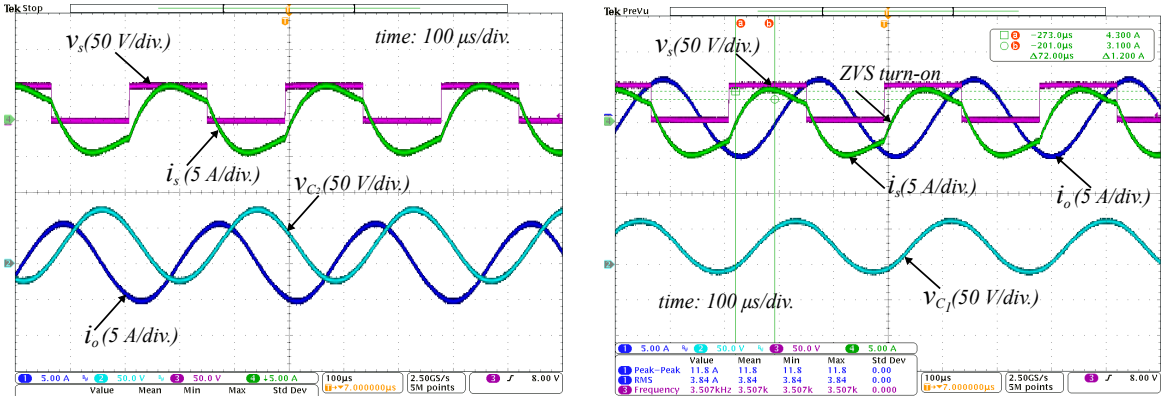
Fig. 6.9 (a) and (b) show the inverter waveforms for peak output currents of 5 A and 8 A, respectively. It is observed that the phase lag between the zero-crossing of switch-node voltage v_s and load current i_o is more than a quarter cycle, due to the -90^o phase of tank current gain $H_i(s)$ at $f = f_r$. Fig. 6.9 (b) depicts the phase relation between i_o and the blocking voltage of Q_1 (v_{Q_1}), which is complementary to v_s. Due to the operation at peak tank current gain, DC source current i_g is small in magnitude.

Fig. 6.10 illustrates the soft-turn on process. It is observed in Fig. 6.10(a) that the



(a) (b)

Figure 6.9: Steady-state Inverter waveforms. (a) I_{o_p}=5 A. (b) I_{o_p}=8 A.

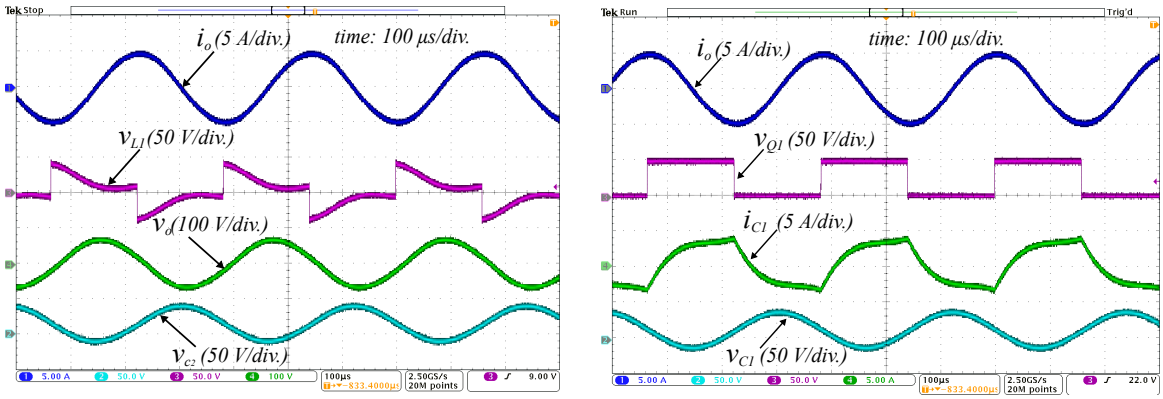


(a) (b)

Figure 6.10: ZVS of inverter switches.

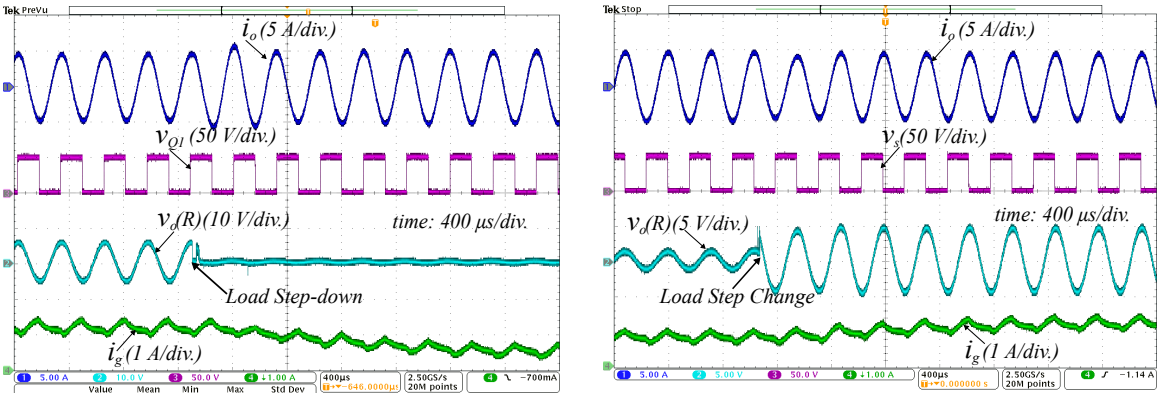
tank input current i_s lags the switch-node voltage, which implies ZVS turn-on of the inverter switches Q_1 and Q_2. Fig. 6.10(b) further illustrates the phase lag between i_s and i_o. The zero-crossing of output current i_o lags i_s by 72 μs, which translates to 90^o for the switching frequency of 3.51 kHz. Tank capacitor voltages v_{C_1} and v_{C_2} are also depicted in Fig. 6.10. Due to the half-bridge structure, both capacitor voltages contain DC offsets.

Steady-state voltage and current waveforms of the resonant tank elements are highlighted in Fig. 6.11 (a) and (b). The load voltage v_o and the series capacitor voltage v_{C_2} are almost 180^o out-of-phase. This demonstrates the series compensation of the



(a) (b)

Figure 6.11: Steady-state tank waveforms.



(a) (b)

Figure 6.12: Response of LCCL-RI against step load change. (a) R decrease. (b) R increase.

load reactance. The voltage across the series inductance (v_{L_1}) denotes the transition of the conduction modes from the lower half-bridge MOSFET Q_2 to the antiparallel diode of Q_1 and vice versa. The parallel capacitor C_1 provides a low impedance path for the harmonics in the tank current i_s, as observed in Fig. 6.11(b).

Fig. 6.12(a) and (b) illustrate the current regulation capability of the proposed LCCL-RI for step variations in load resistance. In Fig. 6.12(a) shows a step-down in R value from 2.1 Ω to 0.3 Ω. The amplitude of i_o is restored to its initial value after a single cycle of oscillation. DC source current i_g also decreases. A step-change of

R from 0.6 Ω to 2.1 Ω results in an increase in i_g (Fig. 6.12(b)) without any changes in i_o amplitude. The transient waveforms closely match with the simulation results and demonstrate the constant-current operation of the LCCL-RI. At load short-circuit conditions, the proposed inverter minimizes the DC source current, which indicates the short-circuit protection capability.

6.5 Performance Evaluation

The proposed LCCL-RI is evaluated in terms of the following performance indices to provide a consistent basis of comparison with the existing DEH technology.

6.5.1 Efficiency

A single-phase R-L load is used in the experiment to emulate the DEH load. The output power loss P_o has two components, namely the power loss in the resistor and the hysteresis loss in the magnetic core of the inductor. The expression of P_o is given by the equation

$$P_o = I_{o,r}^2 R + K_{fe} f^{\alpha_{fe}} (\Delta B)^{\beta} V_{core}, \tag{6.9}$$

where $I_{o,r}$ is the rms value of the load current. V_{core} represents the core volume while k_{fe}, α_{fe}, and β denote the coefficients associated with the magnetic material. It is observed from equation (6.9) that the hysteresis loss component increases with operating frequency. Equivalent heating efficiency of the DEH system can be expressed as

$$\eta_h = \frac{P_o \times 100}{V_g I_g}. \tag{6.10}$$

Fig. 6.13 plots the efficiency η_h for increasing DC source power. It is observed that the efficiency is comparatively low for partial load operation. As the LCCL-RI has

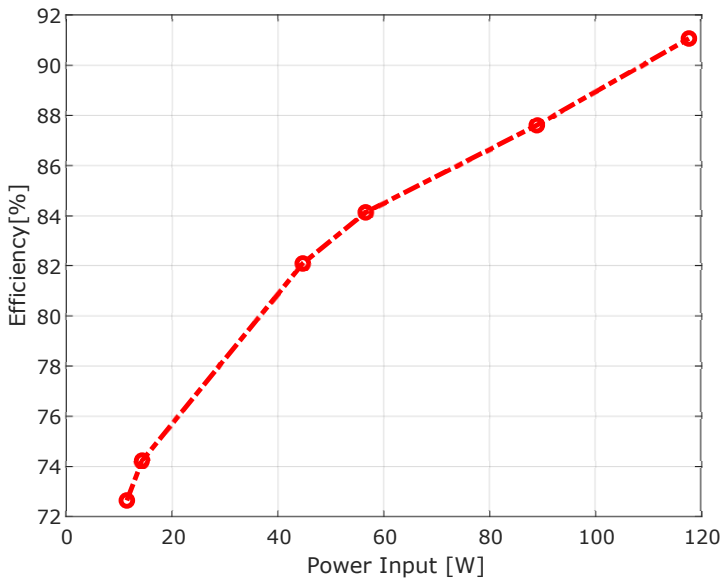


Figure 6.13: Equivalent Heating Efficiency of LCCL-RI based power supply.

a parallel resonant structure, the circulating current loss is higher at low load [150]-[151]. However, the efficiency is much improved at higher loading. Hence, the proposed inverter is suited for constant power operation at or near full load.

6.5.2 Reactive Power Compensation

The experimental results show that the series capacitor voltage is almost in phase opposition to the load voltage v_o, which cancels out the large reactive component of the load voltage. As the reactive compensation is provided by the tank capacitors, no external reactive support is required.

6.5.3 Soft Switching

The simulation and experimental results show that the operation at the peak current gain frequency results in ZVS turn-on of the inverter MOSFETs. Consequently, the switching loss is reduced which enhances the converter efficiency.

6.6 Summary

An LCCL resonant inverter-based power supply has been presented in this chapter for the direct electric heating application. The resonant inverter provides the following advantages.

- Load-independent current regulation.
- Operation at the peak current gain minimizes the DC source current.
- Inherent short-circuit protection due to a parallel-resonant structure.
- ZVS of inverter switches.

The performance of the LCCL-RI is evaluated by simulation and experimental results.

6.7 Publications

1. A. Ray and K. Rajashekara, "A Resonant Current Regulator for Direct Electrical Heating of Subsea Pipelines", in proc. 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 1-6.

Chapter 7

Conclusions and Future Work

7.1 Summary

Subsea electrification is a key building block of the deep-water oil and gas (O&G) processing system. State-of-the-art subsea electrical systems are powered from the onshore grid through a long-distance high voltage AC (HVAC) transmission network. HVAC transmission is a well-developed technology with a simplified architecture. However, HVAC systems exhibit a serious drawback for long step-out distances due to large charging current requirements of the subsea cable. Above a transmission distance of 100 km, HVAC operation becomes unfeasible in terms of power transfer capability and cost. Moreover, conventional hub-and-spoke type HVAC architectures are vulnerable to faults in the subsea distribution transformer, which interrupts the power processing and results in severe economic loss.

High voltage direct current (HVDC) technology shows better performance in long-distance power processing over conventional HVAC architectures. HVDC cables do not encounter line-charging current which enhances the power transfer capability. Above the break-even distance of 60 km in subsea, HVDC transmission shows better cost-effectiveness compared to HVAC systems. Moreover, DC architectures based on modular multilevel converters exhibit higher reliability over conventional HVAC systems. However, fast fault interruption remains the main challenge of subsea implementation of HVDC architecture. Existing HVDC breakers are not particularly suitable in terms

of response time and power loss.

Subsea processing is also affected by hydrate formation in the production flowline. Hydrate formation is prevented by direct electric heating (DEH) technology, which uses the heating effect of electric current to maintain the pipeline above the critical temperature. Although DEH is the most economical solution among existing techniques, the power processing suffers from the high reactive demand of the DEH load. This necessitates the installation of a dedicated power source of large VA rating along with reactive compensation units. Consequently, existing DEH technology is not an optimized solution.

This dissertation proposes three modular HVDC power transmission architectures to address the shortcomings of the existing power architectures for long-distance subsea transmission. The proposed architectures mitigate the reactive power issues and provide fault-tolerant operation. A family of zero current switching hybrid circuit breaker topologies has been developed for fast fault protection in the proposed HVDC architectures. The fault response of the proposed circuit breakers is evaluated using the developed laboratory prototypes for unidirectional and bidirectional systems. Lastly, this dissertation also proposes an LCCL resonant inverter (RI) based constant-current power supply for DEH application. This resonant power supply shows significant improvement over existing DEH technology in terms of reactive power compensation, current regulation, and heating efficiency. The performance of this LCCL-RI is verified using a laboratory-based prototype unit.

7.2 Dissertation Contributions

This section summarizes the contribution of each chapters.

1. Three modular HVDC T&D architectures for long tie-back subsea systems are presented in chapter 2. Distribution feeder protection using fast DC circuit breakers is incorporated in the presented architectures. The ring-type distribution architectures based on series-connected transformers and cascaded DC-DC converters improve the reliability of the subsea power system. The fault-tolerant operation of the proposed HVDC architectures is validated by real-time simulation results in Typhoon-HIL.

2. Three coupled inductor-based ZCS hybrid DC circuit breakers (CIHCB) for fault interruption in the subsea HVDC feeders are proposed in chapter 3. The CIHCBs achieve resonance assisted arcless commutation of the main breaker. The commutation capacitor does not require any pre-charging circuit. A unipolar voltage profile of the capacitor is obtained in CIHCB 2 and 3, which allows the use of high energy-density electrolytic capacitors. The commutation performance of the proposed CIHCBs is verified using two 7.5 kW laboratory-based prototypes. The measured response time ranges from 5-30 μs.

3. Chapter 4 presents three bidirectional coupled inductor-based HCBs (BCIHCB) for fault protection in future offshore grids with renewable generation. The proposed topologies realize arcless DC breaking. BCIHCB 3 is suitable for reclosing operation as the capacitor voltage profile is DC. The current commutation in the bidirectional HCBs is verified by experimental results in a 6 kW prototype unit.

4. Two novel modular DC circuit breakers are proposed in chapter 5 for fast interruption of high fault levels. The modular breakers extend the CIHCB principle for two secondary-side commutation networks. The parallel connection of the primary windings effectively doubles the reflected counter-current. Thus a faster fault response compared to the CIHCBs is realized. The second topology using

series-connected primary windings is particularly useful for preventing commutation failure due to insufficient reverse-recovery time in a thyristor-based implementation. A 1 kW laboratory prototype is developed to evaluate the response speed of the modular breakers. Experimentally measured response time varies between 2-15 μs.

5. Chapter 6 proposes an LCCL resonant inverter for the DEH application. The LCCL-RI operates as a load-independent constant-current source. The resonant tank network provides reactive compensation for the DEH load. The proposed resonant inverter also exhibits in-built short-circuit protection. The tank design enables ZVS of the inverter switches. A SiC MOSFET based 1 kW prototype unit is used to evaluate the performance of the LCCL-RI.

7.3 Scope for Future Work

1. The proposed HVDC power architectures are designed for unidirectional power flow. However, with renewable integration, the subsea feeders will experience bidirectional power flow. Hence a detailed study of the stability of the HVDC system should be performed. Real-time simulation results would be helpful to identify the potential challenges in the bidirectional operation.

2. High Step-down DC-DC converter topologies should be investigated for the possible reduction of the number of power conversion stages in the modular HVDC architecture.

3. The DEH system with interleaved resonant inverters could be tested in a HIL platform.

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