ELECTRO-ENCEPHALOGRAPHIC SIGNAL AVERAGER

A Thesis

Presented to

the Faculty of the Department of Electrical Engineering

University of Houston

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

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by

Jerry Alan Hammer

December 1972

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ABSTRACT

One potential method for obtaining high quality electro-encephalographs is to photographically average the electromagnetic signals of interest. Before any such process can be attempted, however, the concept and feasibility of photographic signal averaging must be demonstrated. The Electro-encephalographic Signal Averager fulfills this purpose. It provides a means to rotate a film-carrying drum through a specified angle at a constant speed. During the constant-speed rotation, optical signals may be recorded on the film. This process may be repeated a preset number of times. The signal averaging time (i.e., the time during which the drum is rotated through a specified angle) may be preset to 100 milliseconds, one second, or ten seconds. By averaging a large number of signals, some average value signal may be detected on the photograph.

The Electro-encephalographic Signal Averager consists of two primary sections: an electronic control system and a servomechanism. The electronic control portion provides all necessary timing signals to permit presetting of the averaging time and the number of times cycling is to occur. It also furnishes appropriate control signals to the servomechanism. The servo assembly is approximated as a second order control system employing both position and velocity feedback. Using a high performance DC motor, a rise time of less than eight milliseconds and a drum rotation linearity of less than one percent was obtained.

TABLE OF CONTENTS

CHAPTER I

INTRODUCTION

An Electro-enphalographic Signal Averager is a device which will in some fashion average the electromagnetic signals emitted by the brain. The purpose of this thesis is to provide a means to photographically average such signals. In order to perform photographic averaging, the signals must be optical in nature. To accomplish this, a lens system and a modulated laser were used. The optical system will not be considered in this thesis; only the averaging device and its operational modes will be covered.

The basic guidelines used in designing and constructing the Electro-enphalographic Signal Averager are as follows:

(1) Signal averaging will be performed by recording the optical signal on a film-carrying drum about which a segment of film is fastened. The film will be of length L such that, $2.5 \leq L \leq 4.0$ inches.

(2) Provision will be made to store a quantity of film within the drum. This reserve will be approximately three feet of 35 mm film.

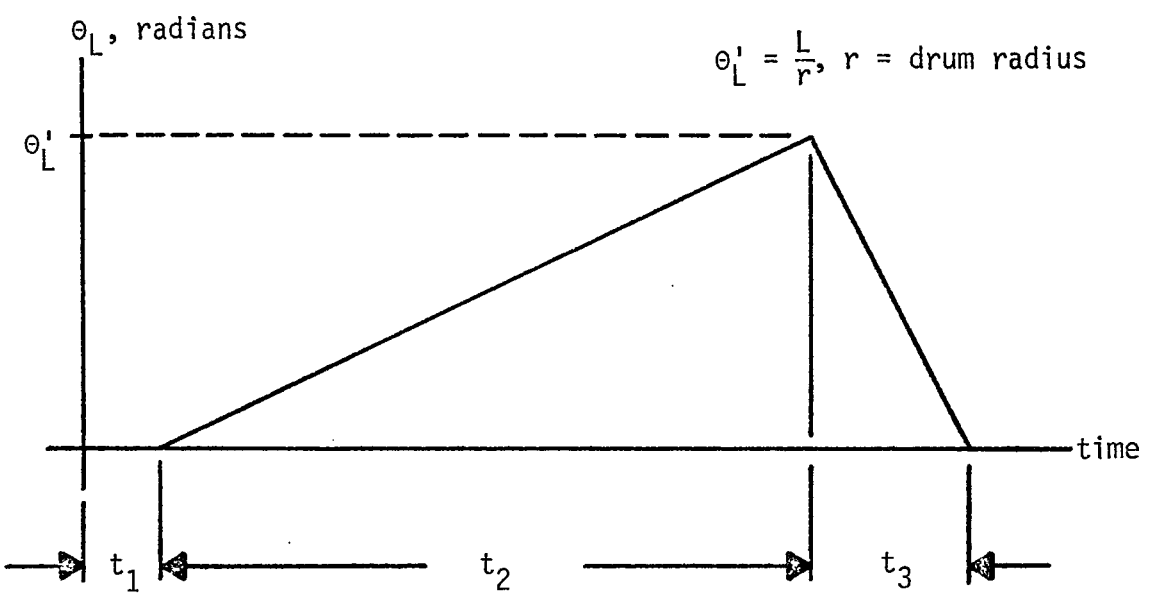
(3) After averaging has been performed on one film segment, a fresh segment may be easily advanced into place so that the averaging process may be continued without the

necessity of changing the film.

(4) The number of signals to be averaged may be preset, i.e., the system will cycle a preset number of times.

(5) A display will be provided to indicate the number of signals which have been averaged at any given time during the process.

(6) The position of the film-carrying drum during each cycle will follow the format given in Figure I-1. The initial response time, t_1, will be less than 8 ms. The averaging time, t_2, may be preset to 0.1, 1.0, or 10.0 seconds. The reset time, t_3, will be equal to 0.1 seconds. The linearity of the position sweep will be approximately one per cent.



DRUM POSITION

FIGURE I-1

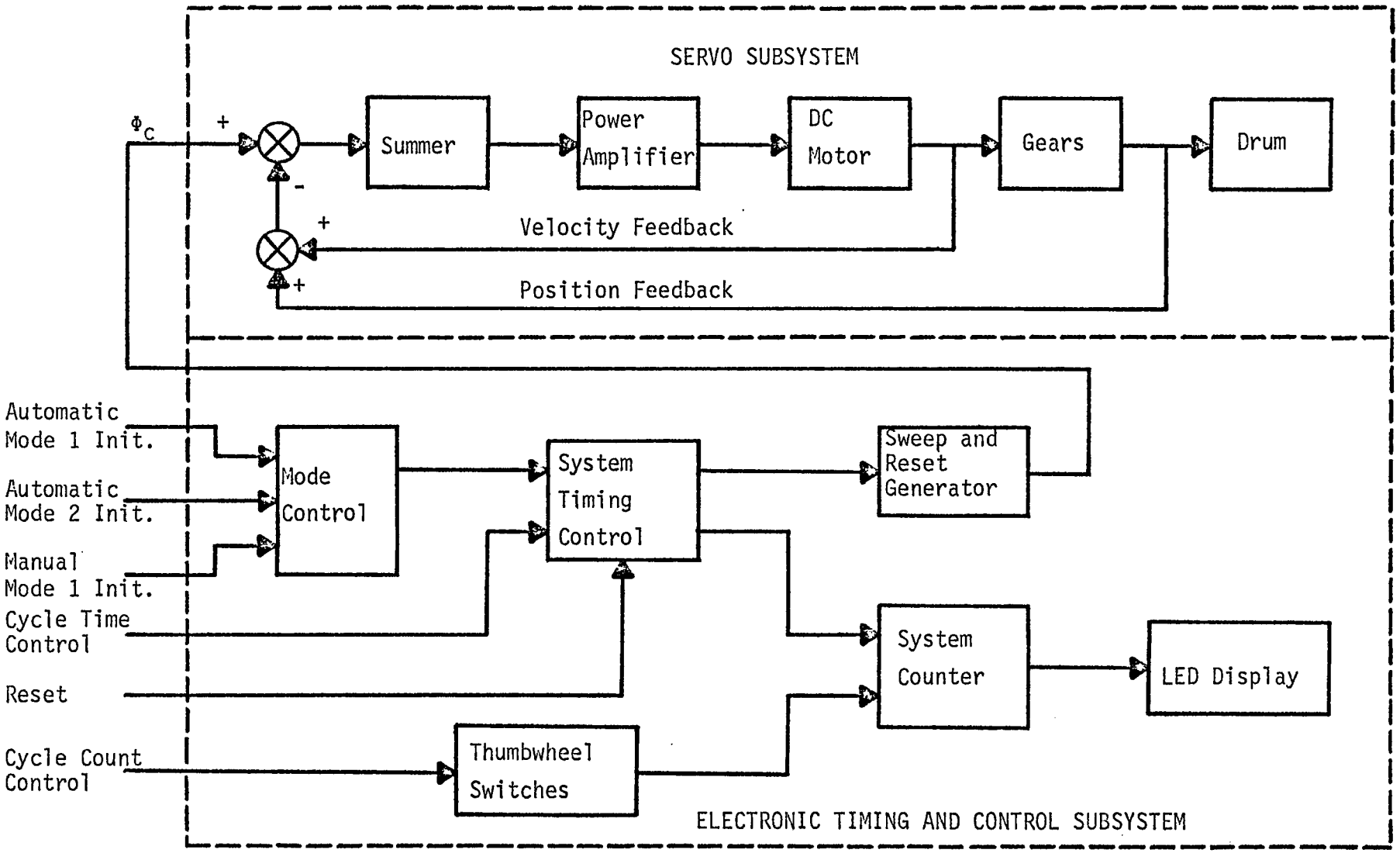
To satisfy the guidelines, both digital and analog circuits were necessary. The digital circuits provide a simple means for generating timing signals needed to control the number of cycles completed, the time duration of each cycle and the display of the cycle count. The analog circuits furnish an electrical signal which will control the drum position. This control circuitry is the subject of Chapter III. A servo mechanism is required to physically position the drum; a feedback control system was employed. Its design and implementation is the topic of Chapter IV. To assist in designing the Signal Averager, two computer programs were written. One provided information concerning drum characteristics, such as size and inertia relationships. A second program simulated the control system for various system constants and plotted the responses. Both programs are outlined in Chapter V. To afford an overview of the Signal Averager before delving into its detailed operation, Chapter II is used to describe its basic operation as well as to give a functional picture of the overall system. Finally the actual system performance is compared to its desired performance in Chapter VI.

CHAPTER II

BASIC OPERATION

The Electro-encephalographic Signal Averager is divided into two primary subsystems: the Electronic Timing and Control Subsystem and the Servo Subsystem. A functional diagram of both, and their relationship to one another is provided in Figure II-1. The Signal Averager is initially activated via the Mode Control inputs. Automatic Mode 1 (or Mode 2) Initiation occurs on the trailing edge of a positive input pulse. The automatic mode lines are available to the user who must furnish the pulse. Only one automatic mode line may be active at any given time. The one to be used during an averaging process is determined by a switch setting on the Control Panel.

A pushbutton (PB1) is provided for Manual Mode 1 Initiation. The first time PB1 is depressed, the Signal Averager is activated; if it is depressed a second time <u>before</u> the system has completed a preset number of cycles (see Cycle Count Control below) the Signal Averager will be immediately deactivated. Cycle Time Control is accomplished via a three position switch which has settings 0.1, 1.0 and 10.0. Each setting corresponds to the length of time over which signal averaging will occur, i.e., a setting of 0.1 will record an optical signal for 100 ms, reset, and then

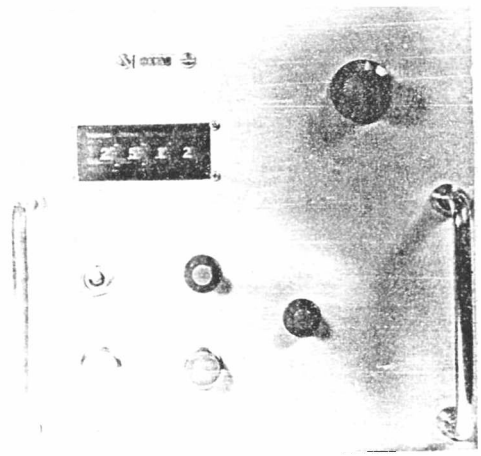


ELECTRO-ENCEPHALOGRAPHIC SIGNAL AVERAGER SYSTEM

FIGURE II-1

repeat the cycle. Similiarly the settings 1.0 and 10.0 will record for one second and ten seconds, respectively, reset and repeat cycling. The reset time in all three cases is 100 ms. The Cycle Time Control should be set only while the system is deactivated; it should not be changed during system operation. The Cycle Count Control consists of a set of four thumbwheel (TW) switches. Each TW switch is individually controlled; they are arranged in increasing order of magnitude from right to left. A setting of 0100 will result in cycling the system 100 times; a setting of 6812 will cycle the system 6,812 times. Upon completion of the preset number of cycles, further operation will be inhibited. However the system will not be deactivated. The Reset pushbutton (PB2) must be depressed to reset and deactivate the system. If PB1 were to be depressed instead, the system would be reactivated but not reset. This method could be used to increment the Cycle Count Control and again activate the system by depressing PB1. Such a procedure is discussed in detail in Chapter III. Each of the manual controls which have been covered are depicted in Figure II-2.

Once activated the System Timing Control circuitry provides all necessary timing signals to the System Counter and the Sweep and Reset Generator. The System Counter provides control signals to the Light Emitting Diode (LED) Display. The display will be zeroed whenever the system is

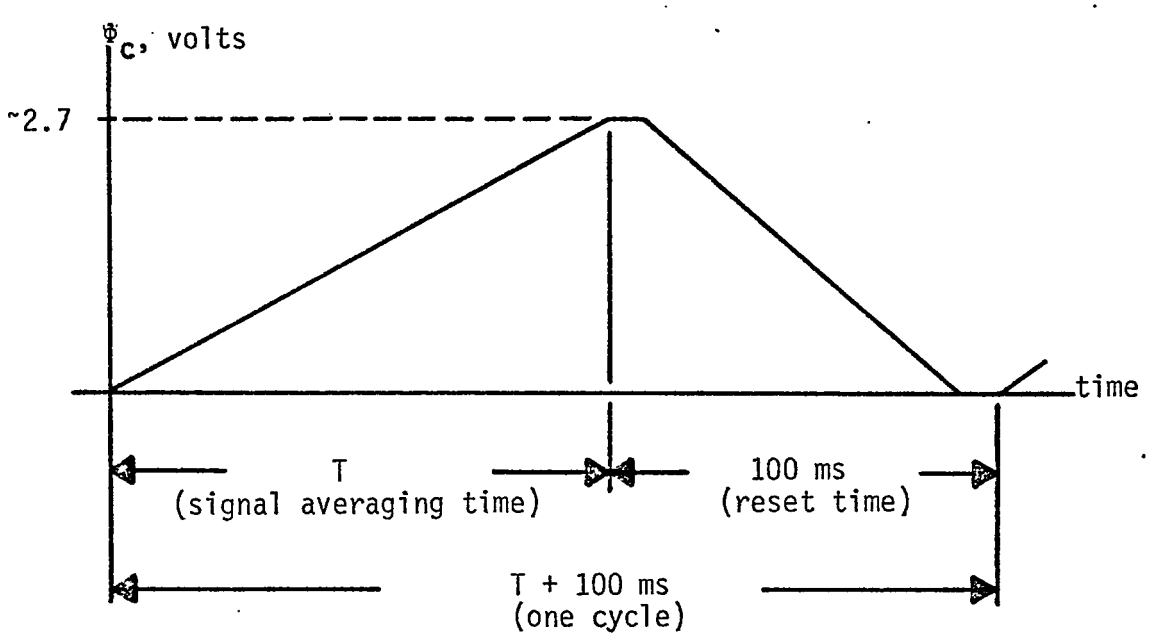


CONTROL PANEL

FIGURE II-2

reset, i.e., its output will read 0000. It will be incremented by one upon the completion of each cycle. Once the TW switch setting has been reached and further cycling has been inhibited, the display read out will correspond to that of the TW switches. This value will continue to be displayed until the system is reset. The System Counter also provides an inhibit signal to the System Timing Control circuit when the preset number of cycles have been completed (this signal is not indicated in Figure II-1, but will be illustrated in Chapter III).

The Sweep and Reset Generator provides the control signal, Φ_c, to the Servo Subsystem. The waveform associated with Φ_c is illustrated in Figure II-3. The length of the



CONTROL SIGNAL

FIGURE II-3

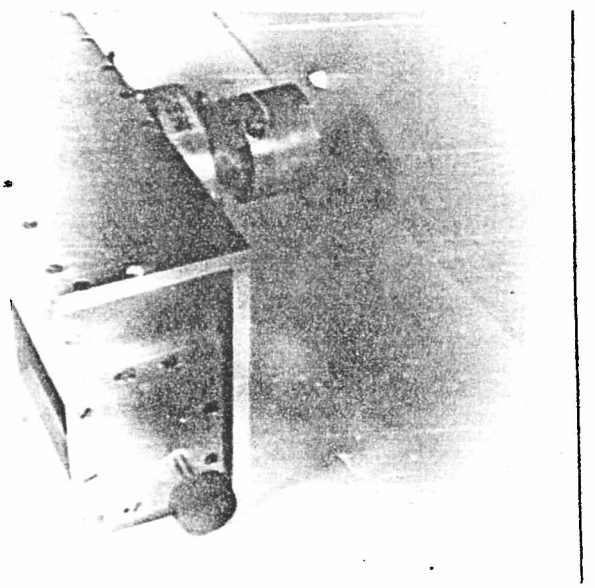
positive going ramp, during which signal averaging will occur, is determined by the Cycle Time Control setting. The remaining portion of the control signal is required to initialize the Servo Subsystem after each averaging cycle. As indicated, its time duration is a constant 100 ms. The control signal is summed with the position and velocity feedback signals; the resulting signal is amplified and serves as the input to the DC motor. The drum position, Θ_L, is then determined by the motor response acting through a gear ratio. The Servo Subsystem may be approximated as a second order control system. By appropriate selection of the feedback constants and the amplifier constant, Θ_L will be linearly related to Φ_c, i.e.,

$$\Theta_L = A\Phi_c + B \ , \qquad (1)$$

where A and B are constants. B represents a constant error term in this system and should be made as close to zero as possible. The selection of A is somewhat arbitrary. In realizing the Servo Subsystem, A = 1 proved to be convenient. Thus the drum position corresponds to Φ_c on approximately a one-to-one basis.

In order to record optical signals on successive film segments, the drum design provides for film storage and advancement. It is, of course, in a light tight container so that the film will be exposed only to the desired optical

signals. The film advance knob, depicted in Figure II-4, permits easy advancement. To insert a new roll of film, the film advance knob mounting plate must be removed. The drum end cap on which two film spools are mounted may then be taken out of the container and a new roll of film inserted. To assist in making this process as simple as possible, the film contained in the drum will not be subject to exposure until after the drum end cap has been loosened and is ready to remove. The act of changing the film must be accomplished in a darkroom environment.



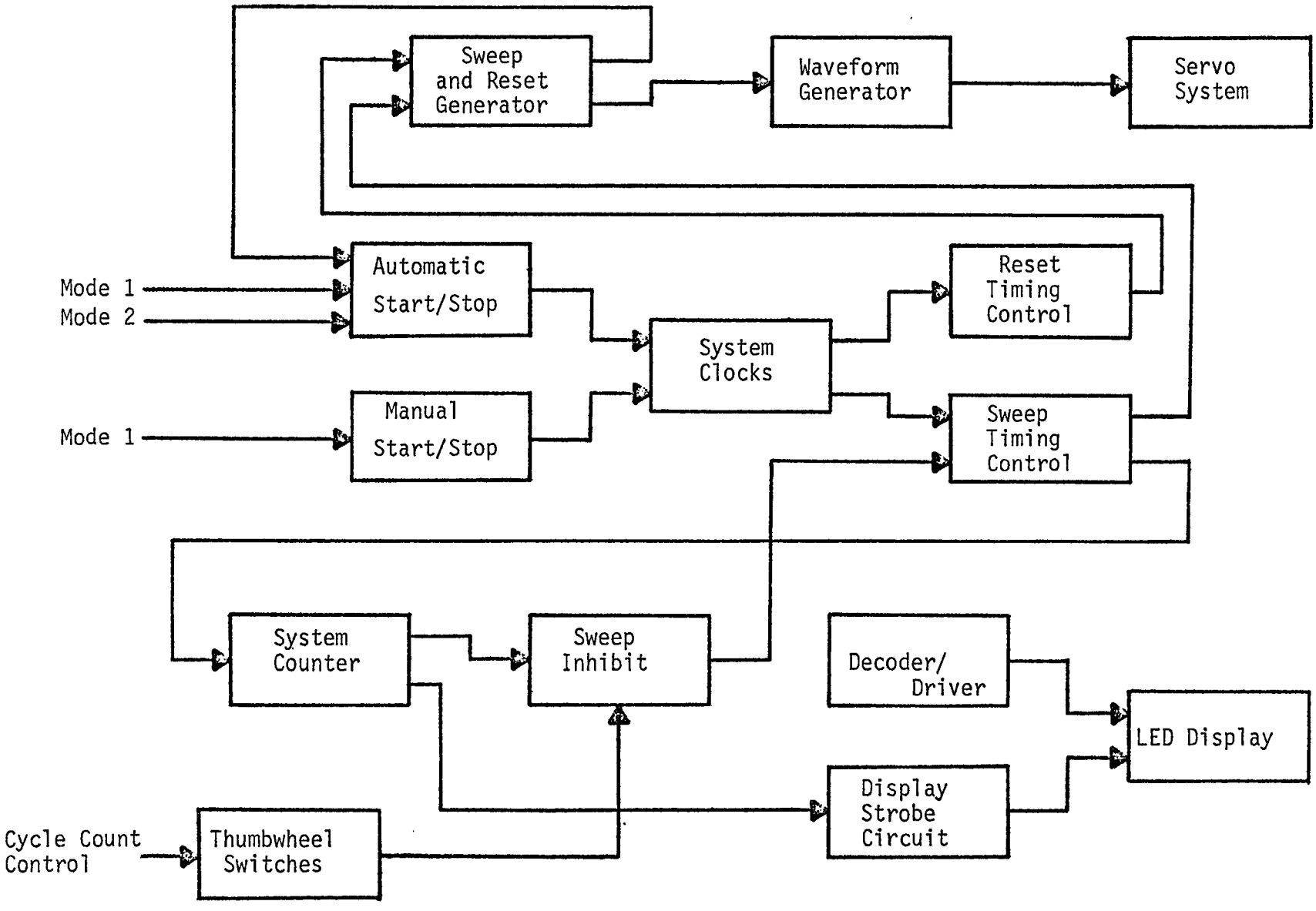
FILM ADVANCE KNOB

FIGURE II-4

CHAPTER III

ELECTRONIC TIMING AND CONTROL SUBSYSTEM

An overall, functional view of the Electronic Timing and Control Subsystem is depicted in Figure III-1. Each of the two inputs to the Automatic Start/Stop will initiate a different mode of operation. Both modes require that the thumbwheel (TW) switches be preset to the desired number of cycles. Both modes require a single pulse (preferably of 1 μs duration or less) to activate the subsystem. However Mode 1 will result in continuous operation, i.e., the system will run continuously until the desired number of cycles indicated on the TW switches has been reached. In Mode 2 the subsystem will be activated for only one cycle; then it will be automatically shut off until the next Mode 2 pulse is received. When the number of Mode 2 pulses accepted is equal to the TW switch setting, further system operation will be inhibited as in Mode 1. Manual operation is quite similiar to Mode 1. Once initiated, via the pushbutton on the Control Panel, the system will cycle continuously until the TW switch setting is reached. One additional capability afforded by manual operation is that the system may be halted at <u>any</u> time. This option may be exercised irregardless of whether the system was activated via Mode 1, Mode 2 or manually.



ELECTRONIC TIMING AND CONTROL SUBSYSTEM

FIGURE III-1

To activate the system is, effectively, to activate the system clocks which serve to establish and maintain all necessary timing relationships for proper system operation. Note that the clocks provide signals to both the Sweep Timing Control and the Reset Timing Control. Beyond this point, the Electronic Timing and Control Subsystem is divided into two primary sections.

The System Counter performs two functions with the Sweep Timing Control signal. First it provides BCD signals to the Sweep Inhibit circuitry where they are compared with the BCD output of the TW switches. When the two are equal, an inhibit signal is generated to prevent further clocking of the Sweep Timing Control. Second, the Sweep Counter furnishes BCD signals to a BCD-to-seven segment Decoder/ Driver. The Decoder/Driver insures that the appropriate number of completed cycles at any given time is exhibited on the LED Display. Because the LED Display consists of four digits with only one set of seven-segment inputs, the Display Strobe Circuit supplies four strobing signals for display control and flicker free operation.

The Sweep Timing Control and Reset Timing Control provide signals with appropriate timing relationships to to the Sweep and Reset Generator. The primary sweep, the time during which signal averaging will occur, will correspond to the setting of the Timing Switch on the Control

Panel. The reset sweep will cause the film-carrying drum to return to its initial position in a fixed length of time. The primary and reset sweeps are summed in the Waveform Generator, the output of which constitutes the controlling signal fed into the Servo Subsystem.

The physical implementation of the Electronic Timing and Control Subsystem may now be considered. As a matter of convenience, the circuitry has been divided into four major sections:

(1) Timing Control

(2) Counter and Display Control

(3) Decoder/Driver and Strobe Circuit

(4) Sweep Generator

The Circuit diagrams to be employed in the ensuing discussion are not intended to be the precise circuits used. Rather they will approximate the actual circuits by omitting components which are not essential to the explaination. In these circuit diagrams the following abbreviations will be utilized:

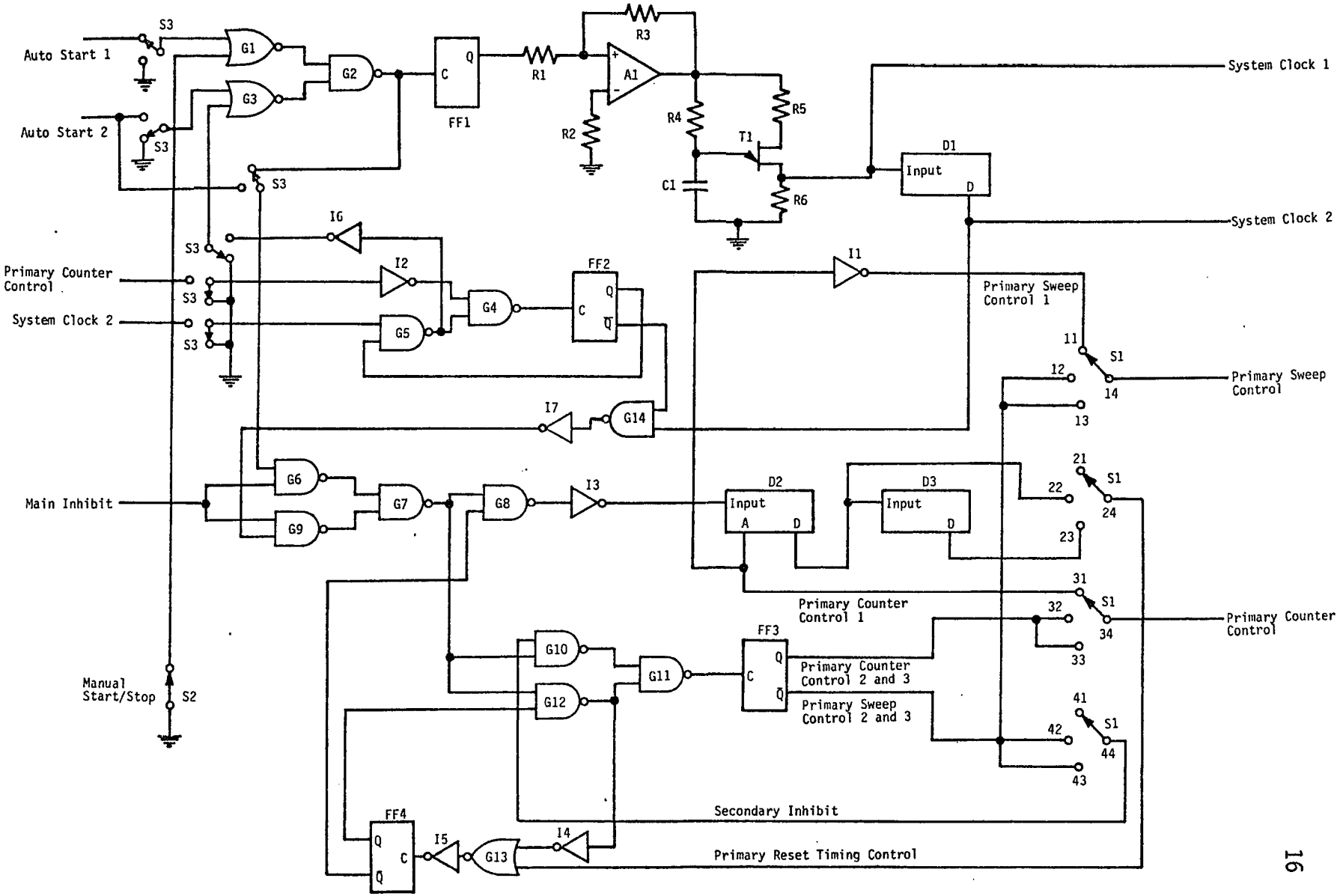
A	operational amplifier
D	decade counter
FF	J-K flip-flop
G	gate

A specific pin on a device, say the Q output of flip-flop X, will be abbreviated as FFX/Q. Positive logic is used throughout the system. Unless otherwise noted, all J and K

inputs to the flip-flops are held to logic 1.

The Timing Control circuitry is illustrated in Figure III-2. Gates G1 and G3 provide the necessary inputs for system activation. Normally all four inputs are held to logic 0. To activate, any one of the inputs is raised to a logic 1, then lowered to a logic 0. This pulse is gated into FF1/C. The FF1/Q output will rise to a logic 1, thus enabling A1 to saturate to +15 VDC and provide power to the UJT relaxation oscillator. The oscillator output is System Clock 1.

The position of switch S3 determines whether Automatic Mode 1 or Mode 2 may be used. One set of S3 contacts (not shown in Figure III-2) will direct the pulse supplied by the user to either Auto Start 1 or Auto Start 2. Auto Start 1 initiates Mode 1 operation. Note that if a second pulse should be inadvertantly received on the Auto Start 1 line, the system will be shut off; no provision has been incorporated in the circuit to prevent such an occurance. The purpose for permitting this condition to exist becomes apparent upon examination of the Manual Start/Stop switch S2 (this switch corresponds to PB1 on the Control Panel). A pulse may be applied to a G1 input by simply opening, then closing S2. The first time this occurs the system is activated by enabling the relaxation oscillator. The second time, the oscillator is shut off. If this second pulse were to be inhibited

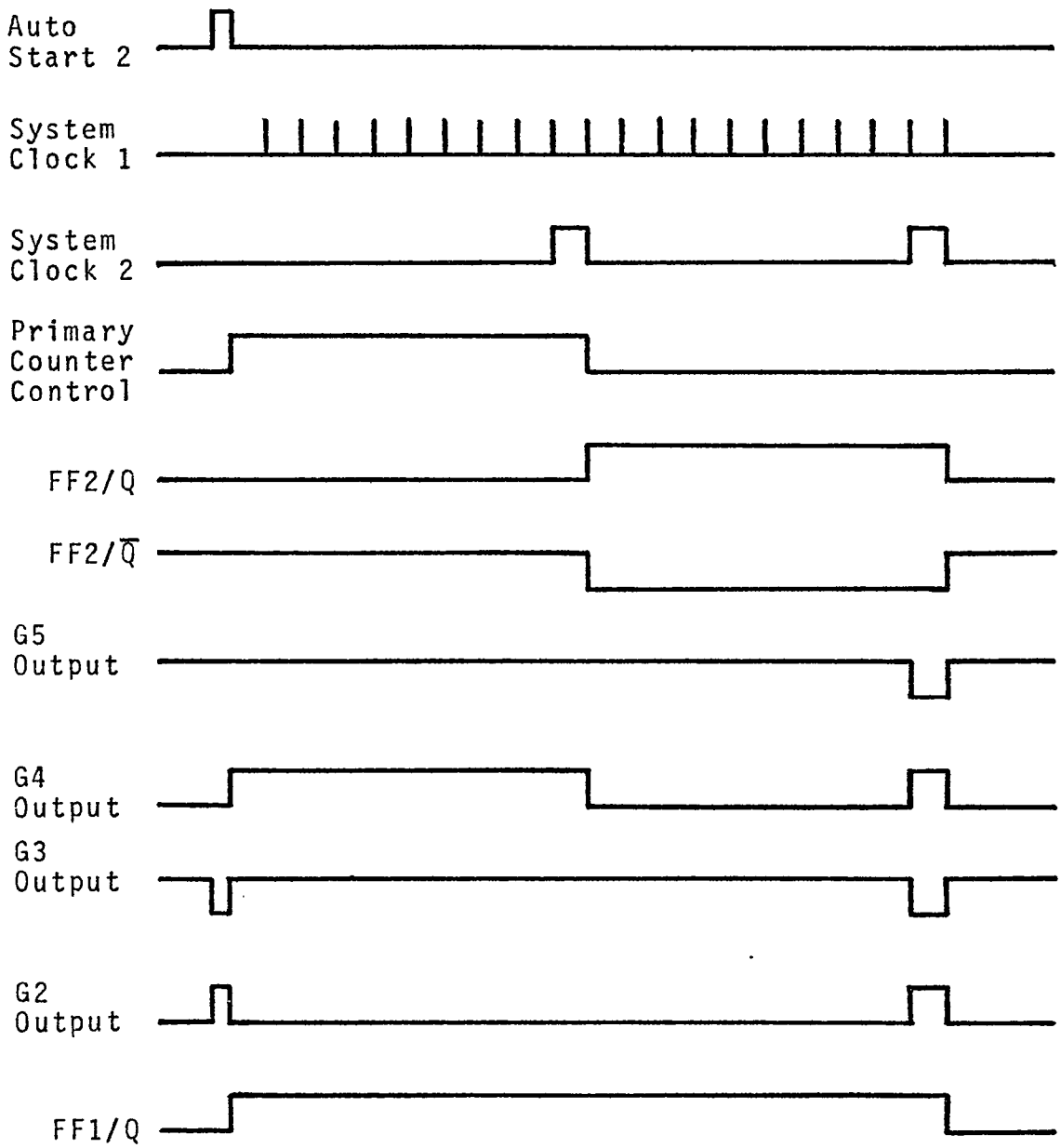


TIMING CONTROL

FIGURE III-2

from affecting the circuit, system operation could not be manually halted without resetting. This method may be used to stop operation while retaining the correct number of cycles completed on the LED Display. Operation of the system in this manner must be exercised with care. When the system is manually stopped the drum may or may not return to its initial position. Therefore the optical signal should first be inhibited. The system may also be reactivated without resetting via S2. Using this technique, irregardless of how the system was halted, the TW switch setting could be incremented to some new value. However if this is attempted, the system should be cycled several times before the optical signal is enabled to assure that no degradation of the photographically averaged signals will occur.

Auto Start 2 corresponds to Mode 2 operation. The waveforms associated with this operational mode are reflected in Figure III-3. Because of the asynchronous nature of Mode 2, some method of stopping and initializing the system after each cycle had to be devised. Switch S3 is employed for this purpose. When S3 is placed in the Auto Mode 2 position, a small circuit consisting of FF2, G4, G5, I2 and I6 are added to the Timing Control circuit. These components will produce the desired results. As in Mode I the trailing edge of the Auto Start 2 pulse will activate the oscillator.

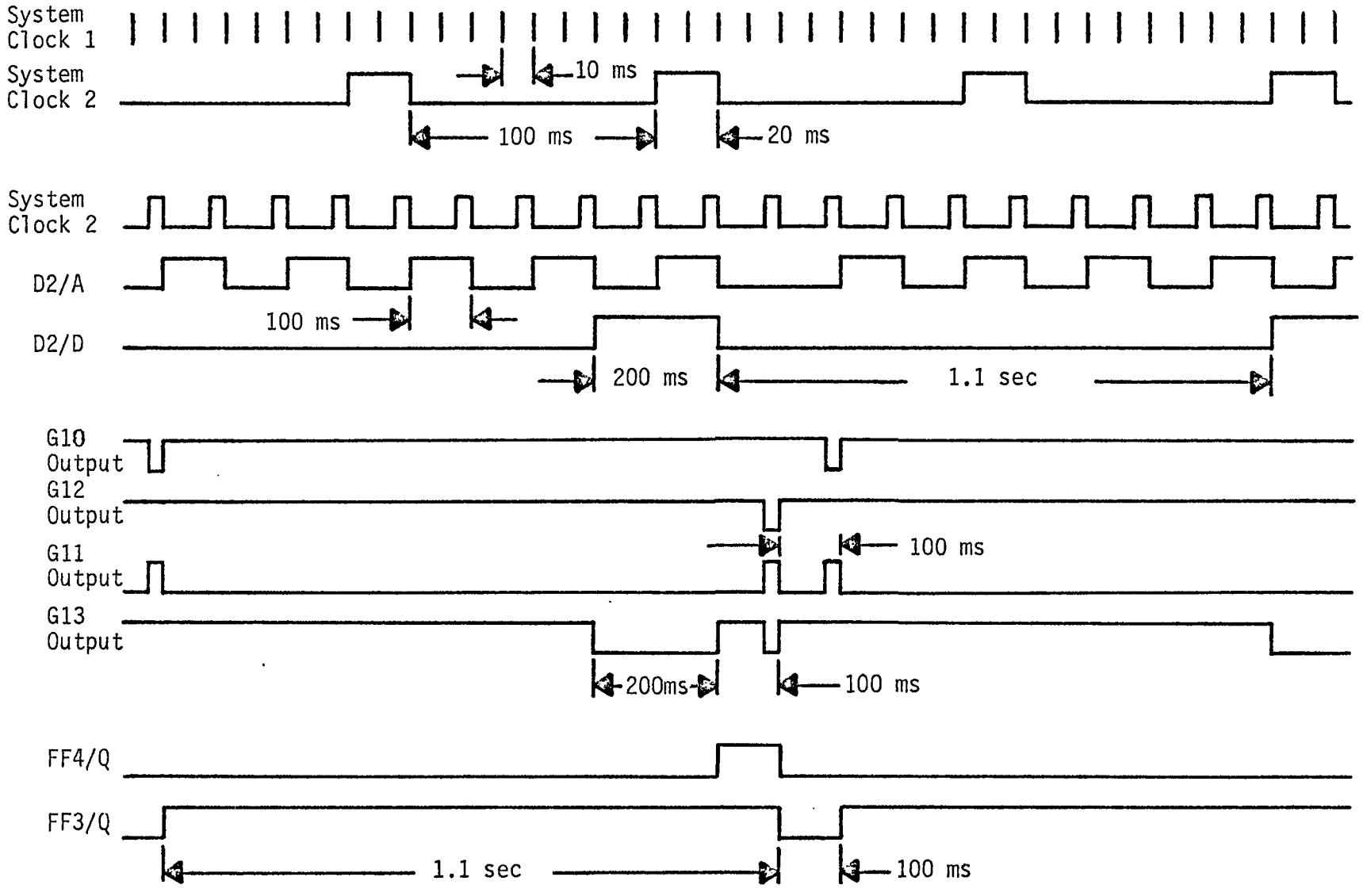


ASYNCHRONOUS (MODE 2) TIMING CONTROL WAVEFORMS

FIGURE III-3

In this case, however, the oscillator will be turned off upon the completion of one cycle. In the specific example illustrated in Figure III-3, the system was set to produce 100 ms primary sweeps. Recall that the reset time is always 100 ms in duration. The selected waveforms and the circuit itself may be used to clarify any question concerning its operation.

System Clock 2 is derived directly from System Clock 1. Clock 1 drives decade counter D1 at a frequency of 100 Hz. Clock 2 is the D output of D1; it produces one 20 ms pulse every 100 ms (see Figure III-4) and thus generates a signal at one-tenth the frequency of Clock 1. Since primary sweep durations are 0.1, 1.0 and 10.0 seconds, System Clock 2 was selected for use in the primary sweep control timing circuit. Clock 2 is initially gated through G9 and G7, at which point it branches in two directions. Before following these two paths, however, two other signals should be considered. The Main Inhibit signal is also gated with Clock 2 into G9. The derivation of the Main Inhibit signal will be covered shortly; suffice it to say that when the number of cycles preset on the TW switch has been reached, the Main Inhibit line shifts from a logic 1 to a logic 0. The logic 0 will inhibit G9. The Main Inhibit is also gated into G6 with the output of G2. Hence the Main Inhibit signal will prevent any other signal from passing beyond G6 and G9. The purpose of gating a start



SWEEP AND COUNTER TIMING CONTROL WAVEFORMS

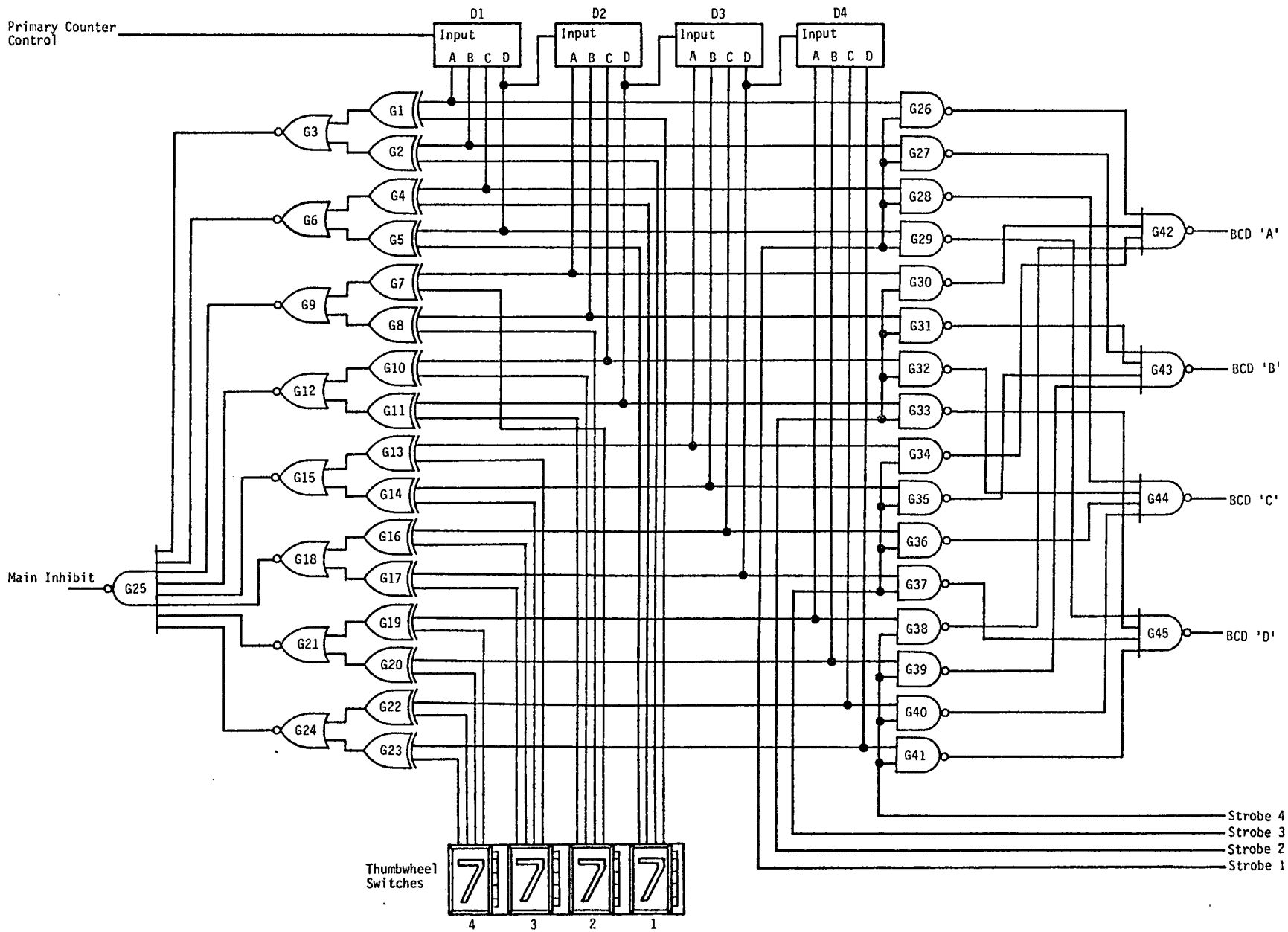
FIGURE III-4

pulse into this point will become clear momentarily.

The relationship between pertinent waveforms associated with the primary sweep control are illustrated in Figure III-4. System Clock 2 is gated through G8 into D2. Since the A output of D2 is a symmetric 5 Hz squarewave, its first half cycle may be used to generate the primary sweep for the 0.1 second setting. Its second half cycle corresponds in duration to the time required to reset the drum, 0.1 second. Hence D2/A provides the Primary Counter Control 1 signal through S1 to the primary counter. After inversion, it supplies the Primary Sweep Control 1 signal through S1. Primary Sweep durations of 1.0 and 10.0 seconds are not as easily obtained. For these two settings, pertinent waveforms are shown in Figure III-4 for a 1.0 second primary sweep. In this case S1 is moved to its second position, i.e., S1/12 is connected to S1/14, S1/22 is connected to S1/24, etc. Initially a start pulse and thereafter a System Clock 2 pulse is gated through G7 into G8, G10 and G12. As before, gating Clock 2 through G8 will result in clocking D2. In this instance D2/A will have no effect on system operation and D2/D will be connected through S1 to G13. Simultaneously the start pulse or Clock 2 will be gated through G10 and G11 to trigger FF3/Q to a logic 1. Gating through G12 cannot occur at this time because it is inhibited by FF4/$\overline{Q}$. The FF3/Q output constitutes the Primary Counter Control 2 (and 3) signal and

is connected through S1 to the Primary Counter. The FF3/$\overline{Q}$ output is the Primary Sweep Control 2 (and 3) signal and is connected through S1 to the Primary Sweep Control. Note that FF3/$\overline{Q}$ also becomes the Secondary Inhibit signal passing through S1 to G10. This provision inhibits G10 from passing Clock 2 pulses and thus clocking FF3 at an undesirable time. The next signal of interest is D2/D which is gated through G13 into FF4. Its trailing edge will occur 0.9 seconds after FF3/Q has been clocked on and will trigger FF4, thus inhibiting G8 and enabling G12. The next Clock 2 pulse, occuring 100 ms later and 1 second after FF3 was clocked, will be gated through G12 into G11 and G13. FF3 and FF4 will then be clocked off simultaneously. As a result, G8 and G10 will be enabled and G12 will again be inhibited. The next Clock 2 pulse, occuring 100 ms later, will clock FF3 on, which will again cause G10 to be inhibited. Thus a new cycle has begun. Note that FF3/Q was on for 1.0 second, the desired Primary Sweep Control 2 duration, and off for 100 ms, the time required to reset the drum. In an identical fashion Primary Sweep Control 3 is obtained using D3/D. In this case FF3/Q is on for 10.0 seconds and off for 100 ms. To summarize, the Primary Sweep Control signal is off for 0.1, 1.0 or 10.0 seconds, depending on whether S1 is in position 1, 2, or 3; it is on for 100 ms, the necessary reset time. The Primary Counter signal is the inverse of the Sweep Control signal.

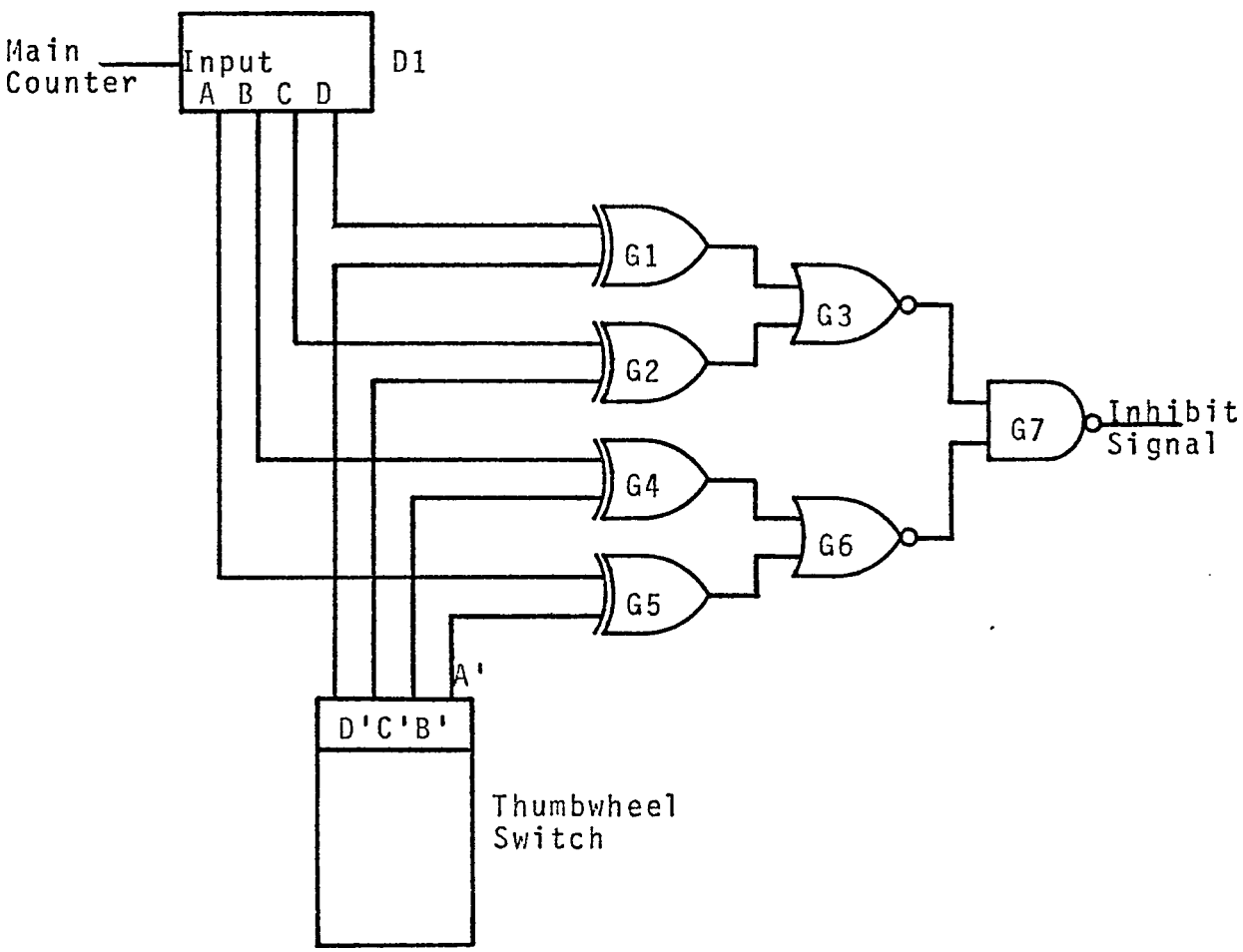
The Primary Counter signal is fed into the first of four cascaded decade counters (see Figure III-5). Each counter provides a BCD output and the output of each successive counter represents a one decade step, i.e., D1 counts from 0 to 9, D2 counts the output pulses from D1/D and therefore may be viewed as the ten's column. Similiarly D3 represents the hundred's column and D4 the thousand's column. Note that each counter, D1 through D4, will have only a BCD output of 0 to 9; the effect of cascading the counters is the reason each successive counter represents one decade. The counters fulfill two functions: first, they provide signals for comparison with the TW switches' BCD output and they furnish BCD signals which are ultimately converted for exhibition on the LED display. To understand the manner in which the Main Inhibit signal is generated, a simplified version of the circuit is shown in Figure III-6; the associated waveforms are depicted in Figure III-7. In the example, counter D1 and TW switch 1 have been isolated from the remainder of the circuit and a two input NAND gate, G7, has been added to the outputs of NOR gates G3 and G6. If D1 is continuously clocked at some periodic interval, which in this case would be the Primary Counter signal, each D1 output would result in the respective waveforms D1/A, D1/B, D1/C and D1/D. Suppose the TW switch has been set to seven; it will have a BCD output representing the digit '7' as reflected in waveforms



COUNTER AND DISPLAY CONTROL

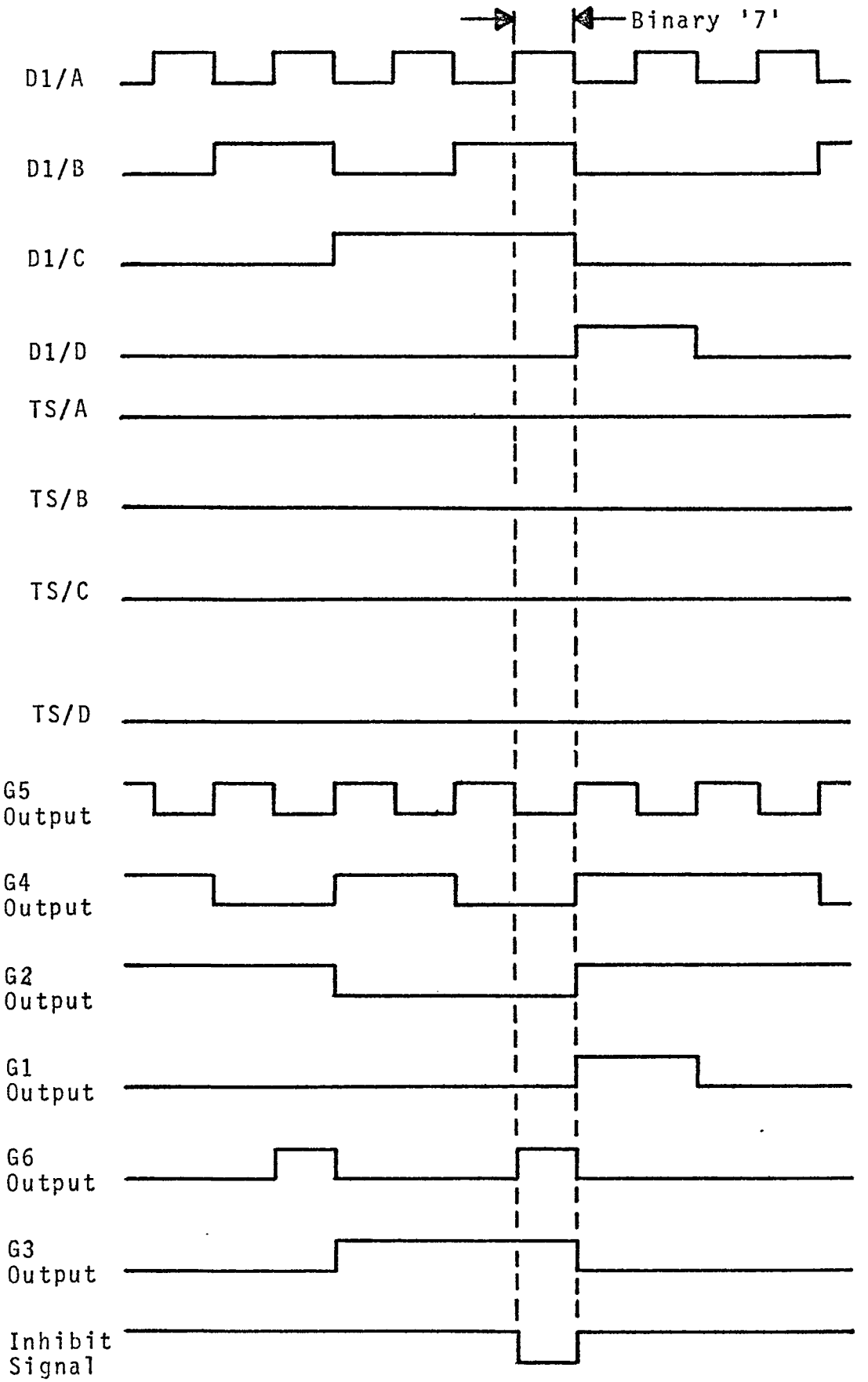
FIGURE III-5

TS/A, TS/B, TS/C and TS/D. The A outputs of D1 and the TW switch are compared in the exclusive OR gate G5. Similiarly comparison of the B, C and D outputs are made in gates G4, G2 and G1, respectively. When any two of the compared signals are different the exclusive OR output is a logic 1; otherwise it is a logic 0. The results of these four comparisons are given in Figure III-7. Next the outputs of G1 and G2 are compared in G3 while the outputs of G4 and G5 are compared in G6. Note that the output of G3 (or G6) can go to a logic 1 if and only if the outputs of both G1 and G2



MAIN INHIBIT CIRCUIT OPERATION

FIGURE III-6



MAIN INHIBIT CIRCUIT WAVEFORMS

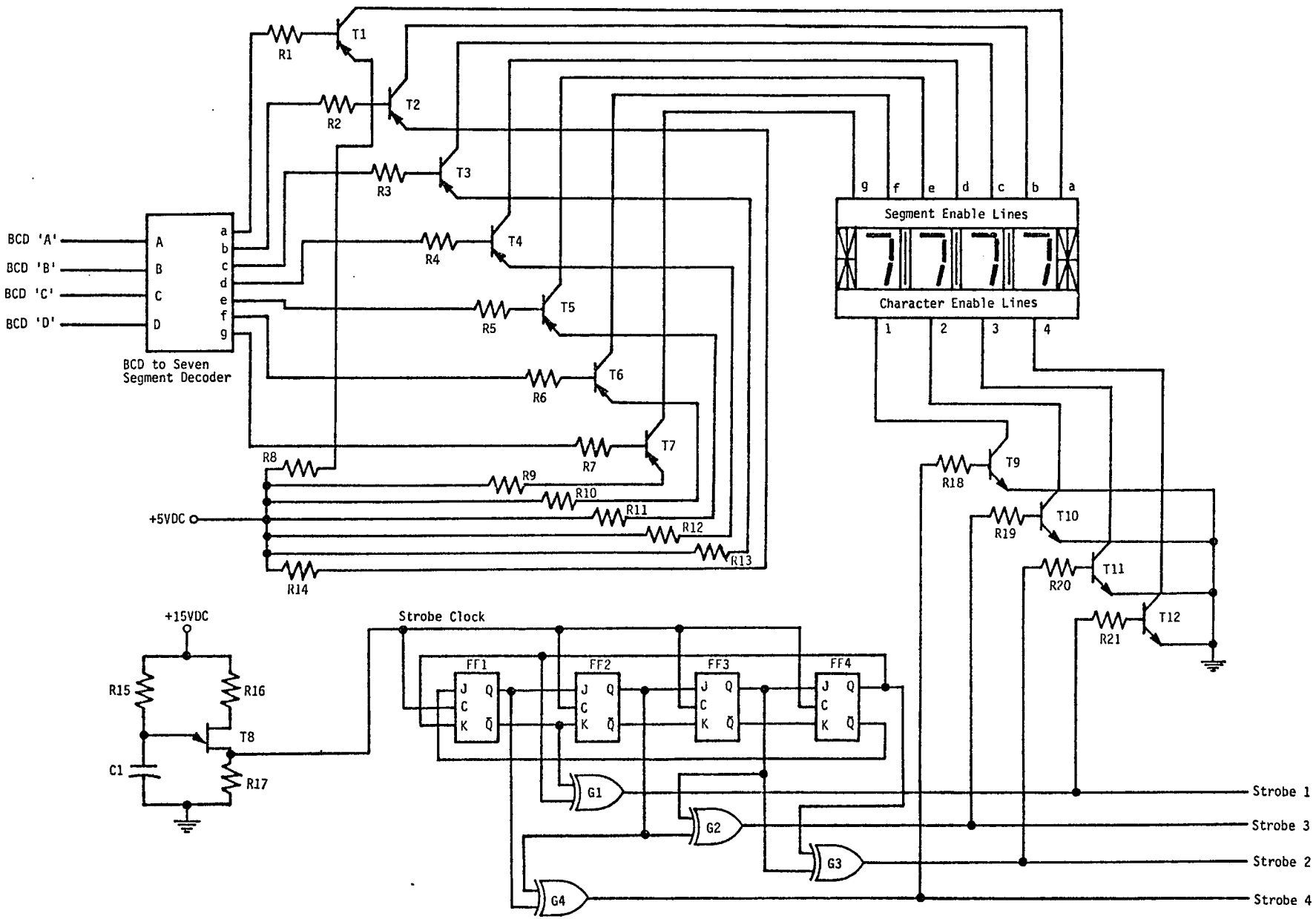
FIGURE III-7

(or G4 and G5) are at logic 0, i.e., the comparison of the C outputs and the D outputs (or the A and B outputs) indicated D1 and TW switch 1 are identical. Finally, the G3 and G6 outputs will result in a logic 0 on the G7 output if the four original comparisons prove to be identical. In the example, a logic 0 occurs when the D1 BCD output matches the TW switch 1 BCD output: that is, a binary seven has occured on the D1 outputs. The appropriate Boolean expression for this condition is,

$$\text{Inhibit Signal} = \overline{AA' + BB' + CC' + DD'}$$

In the actual circuit, Figure III-5, comparisons between each counter output and each TW switch output are gated into a single NAND gate, G25. When the sixteen counter outputs identically match the sixteen TW switch outputs, G25 will drop to a logic 0 and inhibit G6 and G9 in Figure III-2. This action will preclude any further clocking on the Primary Counter line. The system should then be reset and activated if additional cycling is desired. A change in the TW switch setting alone would enable additional cycling without resetting the system. However, such action could only be initiated manually as previously explained.

The second function performed by the primary counters will be illustrated after first examining the strobe circuit (see Figure III-8). The strobe circuit consists of a



DECODER/DRIVER AND STROBE CIRCUIT

FIGURE III-8

relaxation oscillator, four flip-flops and four exclusive OR gates. Unlike the oscillator used for timing control, the strobe oscillator is operational any time the system is receiving power. Its output, the Strobe Clock, triggers all four flip-flops simultaneously. Note that the output of each flip-flop furnishes the signal to the J and K inputs of the successive flip-flop. The output of FF4 is looped back to FF1. In this fashion four signals are generated, each being 90° out of phase with the preceding one as illustrated in Figure III-9; note that FF2/Q lags FF1/Q by 90°, FF3/Q lags FF2/Q by 90°, etc. Significantly, FF4/Q may be thought of as lagging FF1/Q by 270°, or leading it by 90°. The four strobe signals, Strobe 1 through Strobe 4, are derived from the flip-flop outputs. The Boolean expression for each strobe signal is as follows:

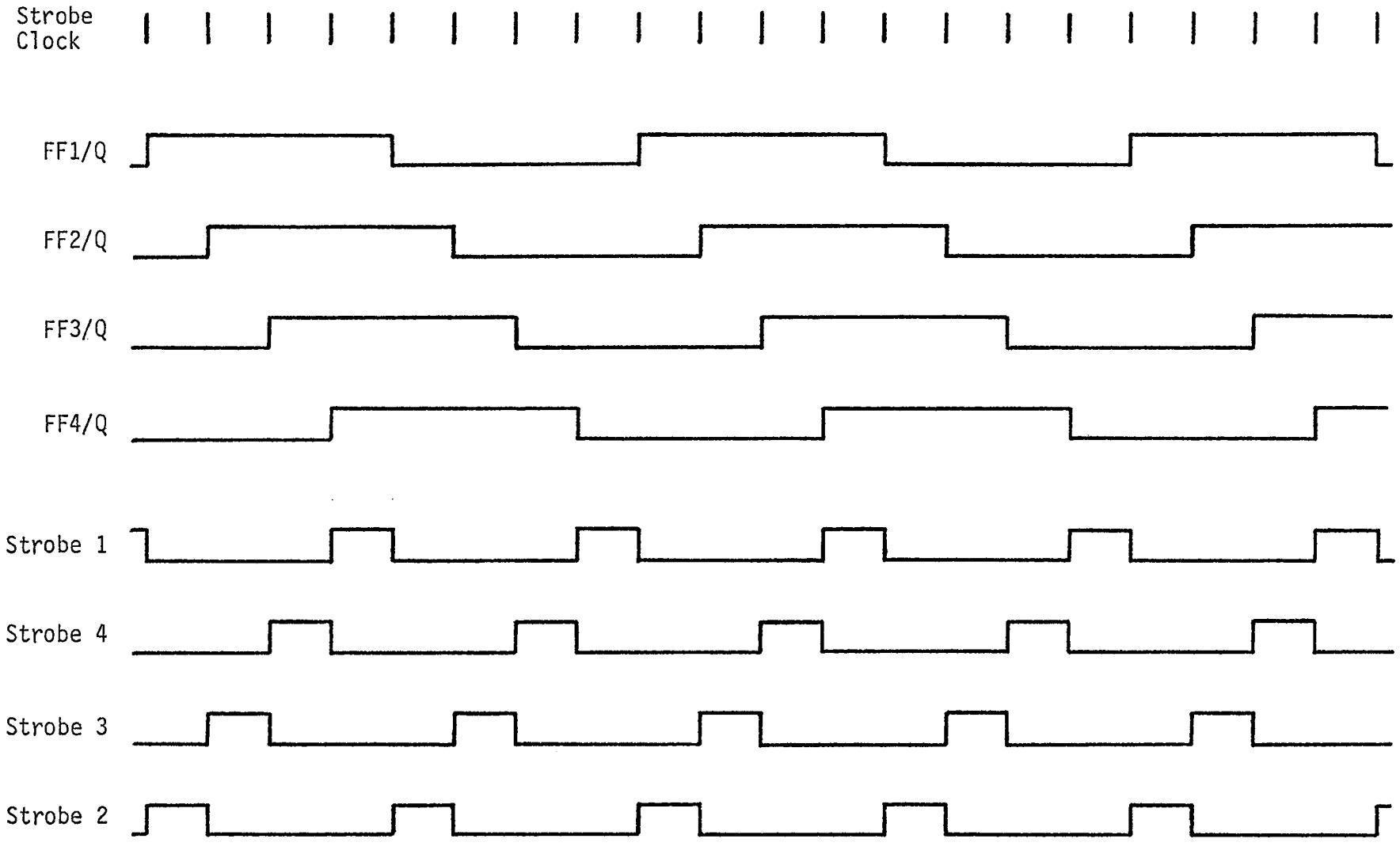
$$\text{Strobe 1} = \overline{Q}_1\overline{Q}_4 + Q_1Q_4$$

$$\text{Strobe 2} = \overline{Q}_3Q_4 + Q_3\overline{Q}_4$$

$$\text{Strobe 3} = \overline{Q}_2Q_3 + Q_2\overline{Q}_3$$

$$\text{Strobe 4} = \overline{Q}_1Q_2 + Q_1\overline{Q}_2$$

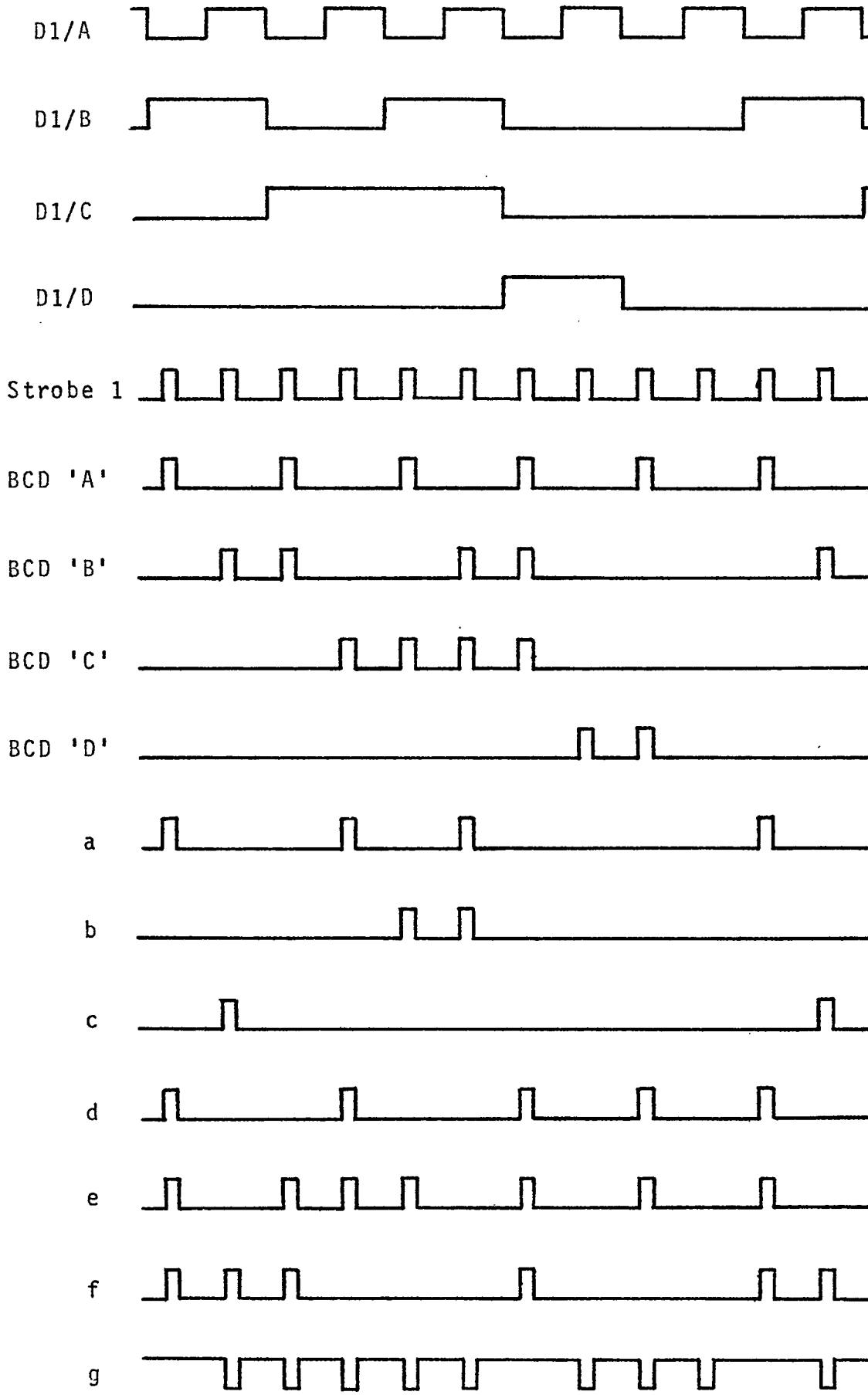
The resulting waveforms may be compared in Figure III-9. One and only one strobe signal is at a logic 1 at any given time.



STROBE CIRCUIT WAVEFORMS

FIGURE III-9

The requirement for four signals, each being out of phase with any other, can be easily grasped by reconsidering Figure III-5 and the waveforms in Figure III-10. For convenience, consider only the outputs of counter D1 and the Strobe 1 signal. Waveforms D1/A through D1/D are shown in the continuous clocking mode (Mode 1). Gates G26 through G29 receive the signals D1/A through D1/D, respectively. However these gates are inhibited by the Strobe 1 signal except for the one-quarter cycle time period during which Strobe 1 is at a logic 1. During this enable time, the outputs of G26 through G29 provide inputs to gates G42 through G45. The remaining three inputs to the latter gates are always enabled (at a logic 1) due to the inhibitive effects of the other strobe signals on gates G30 through G41. Hence the outputs of G42 through G45 will be identical to that of counter D1 for one-quarter of each strobe period. In a similiar manner, counters D2 through D4 will be sampled once each strobe period for a time duration equal to one-quarter of a strobe cycle. The resulting signals in this example are shown in the figure as BCD 'A' through BCD 'D'. In actual operation the BCD 'A' signal, as are the others, is somewhat more complex in that its value (a logic 1 or logic 0) could change as often as every one-quarter strobe cycle. The BCD 'A' signal would appear as in the figure if and only if all of the outputs of

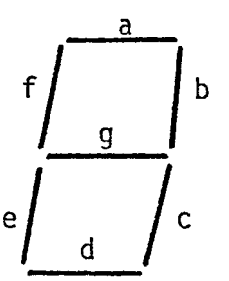


STROBE 1 DECODER WAVEFORMS

FIGURE III-10

counters D2 through D4 are held to logic 0.

Waveforms BCD 'A' through BCD 'D' are the inputs to the BCD-to-seven-segment decoder (see Figure III-8). The decoder converts the four BCD inputs into seven output signals, a through g. The segment corresponding to each signal is indicated in Figure III-11. For the simple example used above, the outputs of the decoder would be as shown in Figure III-10. The effect of the decoder output may be understood by considering the signals a through g when the BCD input signals have some specific value, say '7'. In this instance, signals d, e, f and g are at logic 1 levels while signals a, b and c are at logic 0 levels. This will result in biasing transistors T1, T2 and T3 on while T4 through T7 are off. Observe in Figure III-11 that segments a, b and c will produce the digit '7' on the display. The LED display requires, however, that each of the four characters be enabled before any display can be realized. In other words power is supplied to the various segments of all four characters simultaneously. A ground return path for current

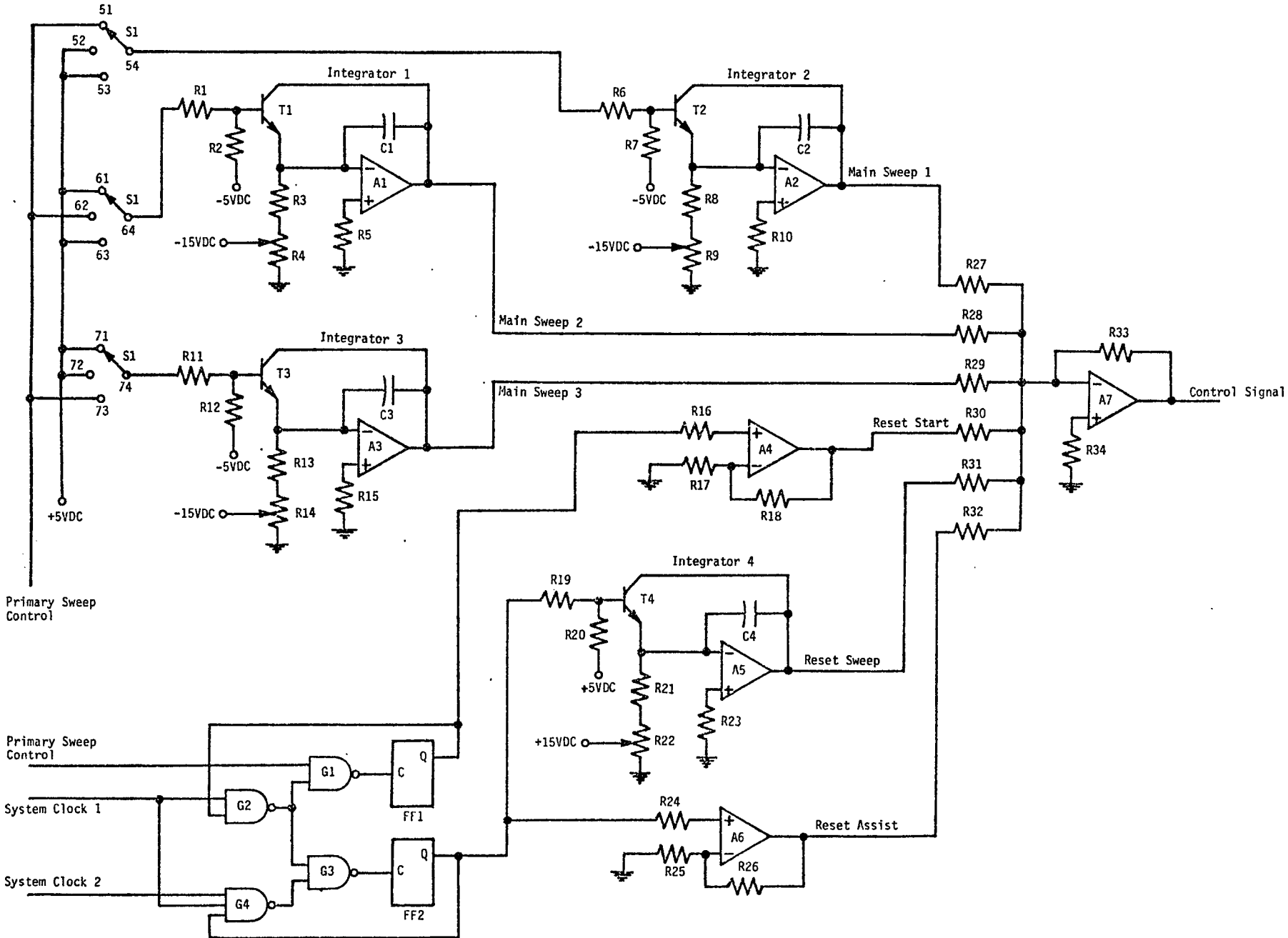


SEVEN SEGMENT DIGIT

FIGURE III-11

may be supplied to each character individually. In this example, since D1 corresponds to digits in the one's column, only character 1 of the LED display should be enabled. For this reason the Strobe 1 signal is used to enable the LED character 1 line by biasing transistor T12 on. Similiarly character lines 2, 3 and 4 are enabled only when the decoder input corresponds to the outputs of counters D2, D3 and D4, respectively. Although each digit in the display is on for only one-quarter of a strobe cycle, the display does not give the appearance of being swept to an observer, i.e., the strobe frequency is sufficiently high to preclude detection by the human eye.

One of the primary functions of the Electronic Timing and Control Subsystem is to provide a control signal for the Servo Subsystem. The control signal must provide the primary sweep during which photographic signal averaging is to occur and some means for resetting the drum to its initial position. This is accomplished in the Sweep Generator circuitry depicted in Figure III-12. Recall that the Primary Sweep Control signal is a logic 0 for 0.1, 1.0 or 10.0 seconds and a logic 1 for 100 ms during each cycle. Depending upon the position of switch S1, one of three electronic integrators will receive the Primary Sweep Control signal. Suppose S1 is in position 1, as shown in the figure. In this instance, transistor T2 will receive a signal which

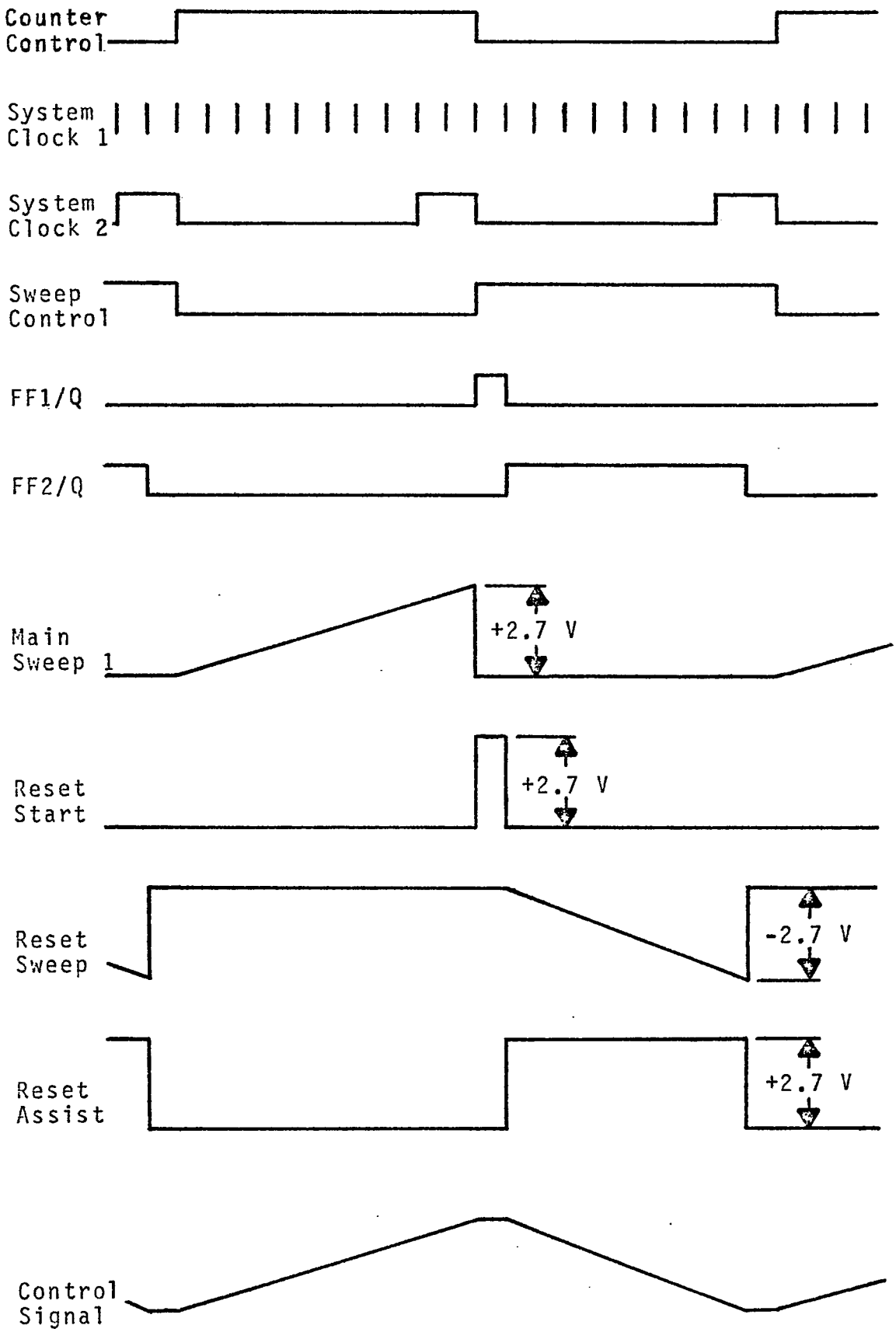


SWEEP GENERATOR

FIGURE III-12

is first at a logic 0 for 100 ms, then at a logic 1 for 100 ms. During the first half cycle T2 will be biased off and amplifier A2 will integrate the negative voltage signal applied to its inverting input. The result will be a 100 ms ramp at the A2 output. During the second half cycle, T2 will be biased "on" and force the A2 output to 0 VDC. While the 100 ms ramp is being generated, T1 and T3 have been biased on via application of +5 VDC through S1. The A1 and A3 outputs are therefore held to 0 VDC as long as S1 is in position 1. If position 2 of S2 is selected a 1.0 second ramp would appear at the output of A1 with a minimum of a 100 ms time period before the next 1.0 second ramp could begin. Similiarly position 3 of S1 will result in a 10.0 second ramp at the A3 output while the A1 and A2 outputs are held to 0 VDC.

The 100 ms reset signal may be divided into three sections. The first 10 ms is simply a DC level which will match the amplitude of the Main Sweep signal. During this time, the angular motion of the drum will be stopped. The next 80 ms of the reset period will be used to generate a negative ramp; this period corresponds to returning the drum to its initial position. The last 10 ms of the reset period serves as a "buffer" time to permit any transients to die out before the next cycle is started. The manner in which this was accomplished may be followed in Figure III-12 and

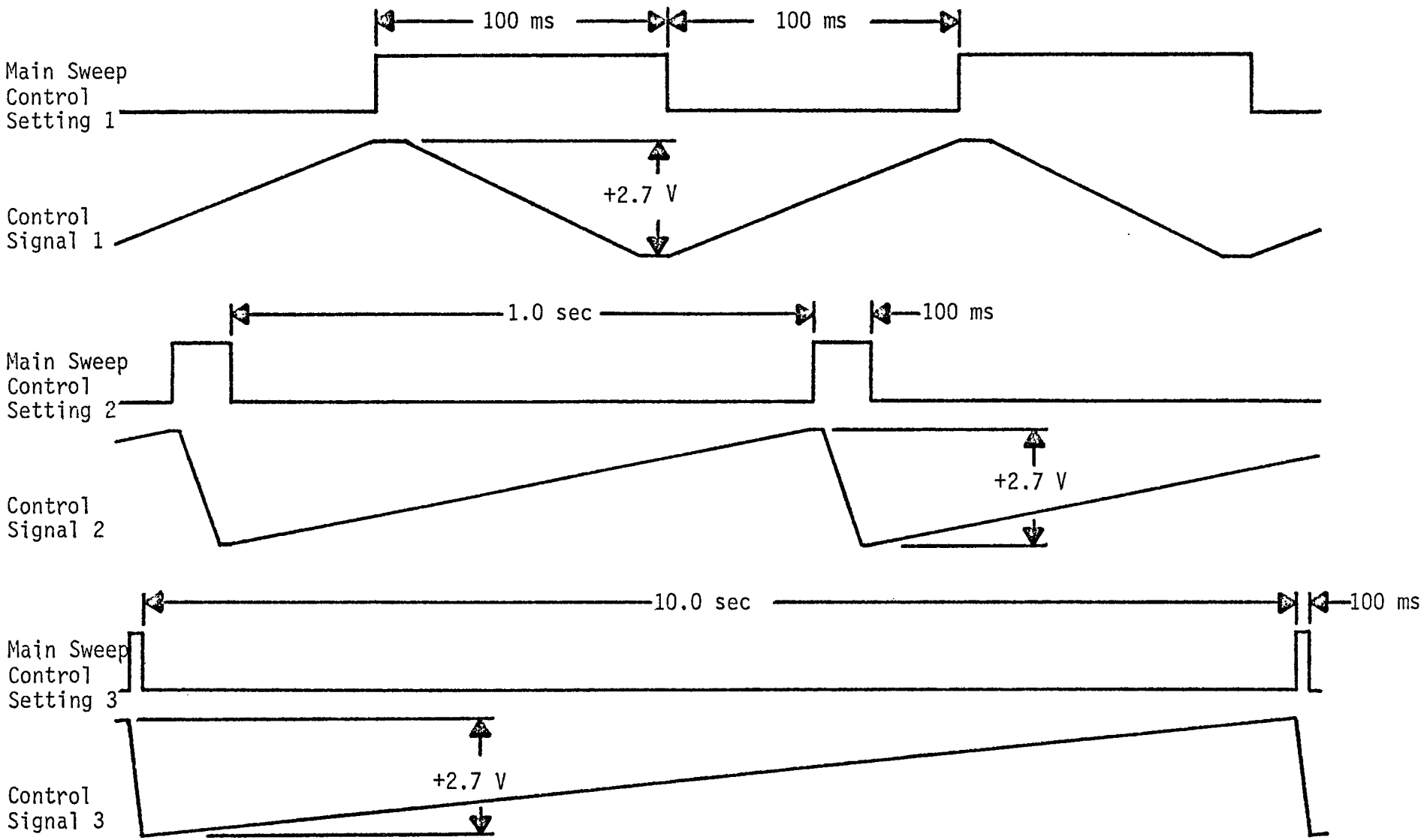


SWEEP GENERATOR WAVEFORMS

FIGURE III-13

Figure III-13. The FF1 and FF2 clock signals are gated through G1 and G3, respectively. The Primary Sweep Control signal inhibits G1 until the primary sweep is completed, at which time it clocks FF1/Q to a logic 1. Gate G2 is consequently enabled and permits the next System Clock 2 pulse to clock FF1/Q off and FF2/Q on. Gate G2 is again inhibited and G4 is enabled. Clock 1 and Clock 2 will combine to trigger FF2/Q off 80 ms later. The FF1/Q signal will be amplified to match the amplitude of the Main Sweep signal. The FF2/Q signal results in a negative going ramp at the output of Integrator 4, the Reset Sweep signal, and a positive 80 ms pulse to "lift" the Reset Sweep amplitude to match that of the Reset Start pulse.

Finally the Main Sweep, Reset Start, Reset Sweep and Reset Assist signals are summed and form, at the A7 output, the desired Control Signal. In the example illustrated in Figure III-13, all analog waveforms and their associated control signals are shown for generating a primary sweep of 100 ms. Each of the three control signals produced by the Sweep Generator is depicted in Figure III-14. Note that the control signals are not time-scaled to one another, although some general ideal of their differences can be visualized.



SWEEP GENERATOR CONTROL SIGNALS

FIGURE III-14

CHAPTER IV

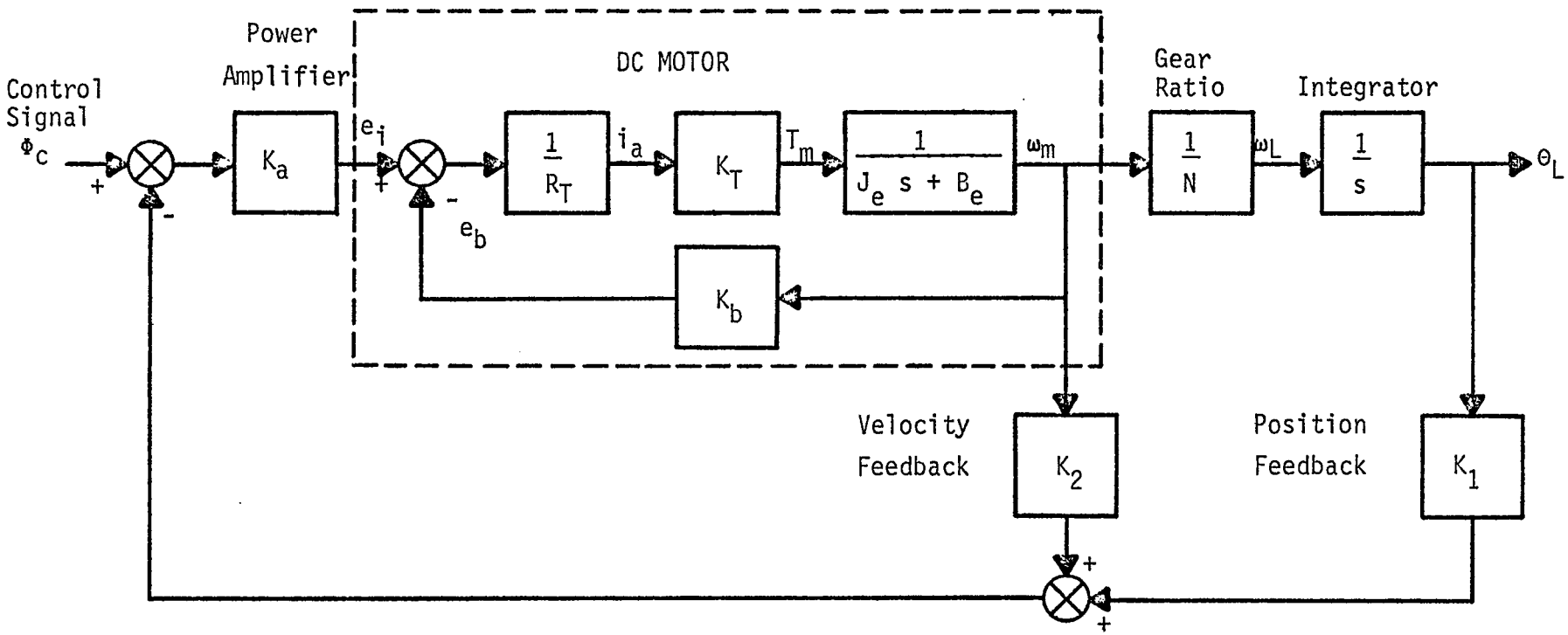
SERVO SUBSYSTEM

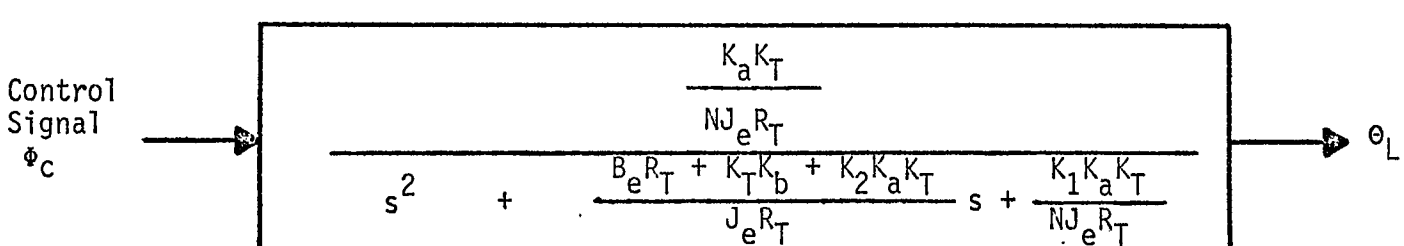
The function of the Servo Subsystem is to transform an electrical signal into an angular displacement of a film-carrying drum. To visualize how this is accomplished, a block diagram of the Servo Subsystem and the result of its reduction is provided in Figure IV-1. The significance of each system constant is listed in Table IV-1. The overall transfer function is that of a second order system and takes the form,

$$G(s) = \frac{K\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \qquad (1)$$

Several commonly employed assumptions were made in order to arrive at this simplified form; each will be noted as the various system components are examined.

The effect of the load (that is, the film-carrying drum) on system performance is primarily dependent upon the inertia and drag it presents to the system. To minimize its effect is equivalent to minimizing its inertia and drag. The concept used to design the drum is illustrated in Figure IV-2. The slots permit film storage within the drum while a film segment may be wrapped around a portion of the





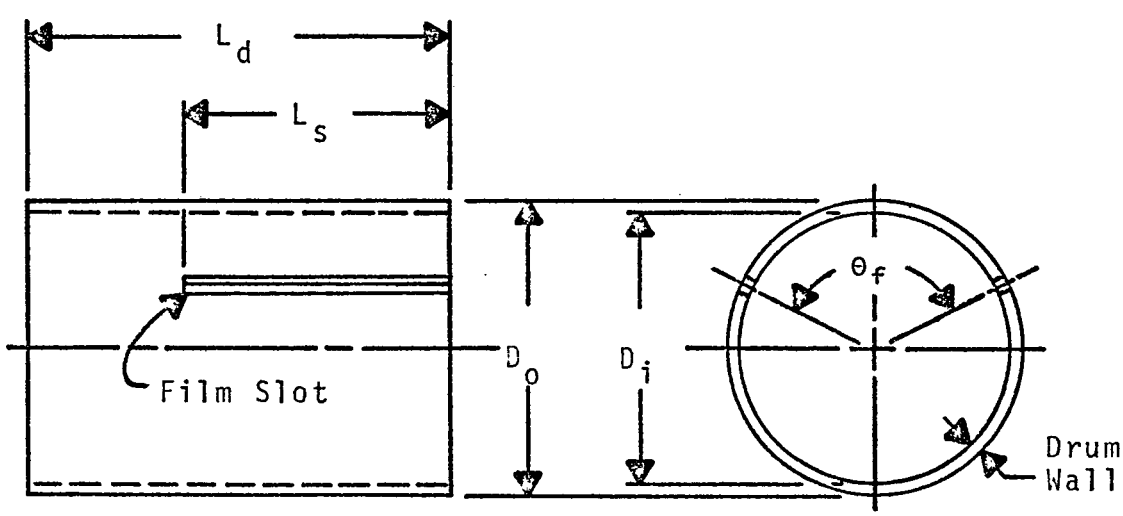
SERVO SYSTEM TRANSFER FUNCTION

FIGURE IV-1

drum exterior. The drum's inertia along its radial axis is given by ,

$$J_L = \frac{\pi L_d \rho}{32} (D_o^4 - D_i^4) \qquad (2)$$

In equation (2) the effect of the film slots has been neglected; ρ is the density (mass per unit volume) of the material from which the drum is constructed. Note that the diameter and wall thickness is critical to minimizing drum inertia. There are two controlling factors in determining the drum diameter: the drum exterior circumference must be greater or equal to 2.5 inches in order to expose the desired length of film, and the drum interior must provide sufficient space to store a quantity of film which can be easily



DRUM DESIGN CONCEPT

FIGURE IV-2

advanced. The former requirement necessitates that,

$$L_\Theta = \frac{1}{2} D_o \Theta_f , \quad L_\Theta \geq 2.5, \tag{3}$$

where Θ_f is in radians. To assist in determining a suitable diameter, a computer program was used to generate the radius, circumference and inertia of a drum for various values of L_Θ and Θ_f. To allow for worst case conditions, the drum was assumed to be made of solid aluminum. Note that assuming the drum is solid implies $D_i = 0$. Such an assumption takes into account the paraphernalia which will be contained inside the

System Constant	Significance
K_a	power amplifier gain
R_T	motor input impedance and pwr amp output impedance
K_T	torque constant
J_e	motor and reflected load inertia
B_e	motor and reflected load drag
K_b	back emf constant
N	gear ratio
K_1	position feedback constant
K_2	velocity feedback constant

SYSTEM CONSTANTS

TABLE IV-1

drum. The program will be discussed in Chapter V; for now, only its results will be considered. The L_θ requirement was found to be satisfied for any $D_o \geq 0.8$ inches. However a minimum value for D_i, a problem not considered in the program, could be determined only by first selecting a means for storing and advancing film. This problem was resolved by a decision to use two identical spools. One spool provides for storage of unexposed film; the other acts as a take-up spool and provides a means for manually advancing the film. Thus in establishing a requirement for the inside drum diameter, the diameter of the two spools must be taken into account. Further the diameter of a supporting rod through the center of the drum must be included in establishing a minimum D_i. The net result was to select $D_i \geq 1.75$ inches. By selecting two inch outside diameter aluminum tubing, two essential requirements were satisfied: the minimum desired D_i is achieved while leaving a sufficient drum wall (0.125 inches), and the material is of low density and relatively high strength. Upon selecting $D_o = 2$ inches, the following quantities could be obtained directly from the computer program:

$J_L = 0.03$ oz-in-sec^2

$L_\theta = 2.75$ inches

$\theta_f = 160$ degrees

The remainder of the drum assembly design was simply a matter of interfacing the spools and supporting rod with the drum. This was accomplished by end capping the drum with one-quarter inch thick disks which could be fastened to the supporting rod. The spools are attached to one end cap and spring loaded against the other. One end of the take-up spool is extended well beyond the end of the drum and slotted so that it can be mated with a film advance knob.

Refering to Figure IV-1, note that five of the nine system constants are directly dependent upon the motor characteristics. Its selection, therefore, was of utmost importance to anticipated system performance. Its open loop time constant, inertia and drag should be minimal; its power, torque, speed and acceleration must be adequate to drive the load at the required rates. To this end, the characteristics of a series of Micro Switch high performance DC motors were examined. Of the motors studied, two were tentatively selected for use in a computer simulation of the Servo Subsystem. Their significant features are tabulated in Table IV-2. Motor I was selected for its higher power and torque output. Motor II was chosen for its lower inertia and damping, and its higher speed. As might be supposed, Motor I is somewhat more expensive than Motor II; hence if the desired system performance can be achieved with Motor II, it would be the preferable choice.

Before performing a computer simulation of the Servo Subsystem, equation (1) and its implications should be considered. The closed loop time constant and settling time are given by, respectively,

$$T_c = \frac{1}{\xi\omega_n} = \frac{2J_eR_T}{B_eR_T + K_TK_b + K_2K_aK_T} \qquad (4)$$

$$T_s = 4\ T_c \qquad (5)$$

Characteristics	Motor I	Motor II	Units
Rated Power	215	92	watts
Rated Torque	135	32	oz-in
Rated Speed	2160	3900	rpm
Terminal Resistance	0.5	1.0	ohms
System Inertia	0.00375	0.00044	oz-in-sec^2
Mechanical T_c	2.0	1.55	ms
Torque Constant	11.3	6.0	oz-in/amp
Back emf Constant	8.35	4.41	volts/krpm
Damping Constant	1.65	0.25	oz-in-sec/rad

MOTOR CHARACTERISTICS

TABLE IV-2

Here, ξ is the damping ratio and ω_n is the undamped natural frequency of the system. By judicious selection of ξ, the overshoot of the transient response may be tightly controlled. To obtain the best overall response, $\xi = 0.7$ was selected. This, combined with a desired 8 ms settling time, results in,

$$\omega_n = 714 = \frac{B_e R_T + K_T K_b + K_2 K_a K_T}{1.4\ J_e R_T} \tag{6a}$$

$$\omega_n = \left[\frac{K_1 K_a K_T}{N J_e R_T}\right]^{\frac{1}{2}} \tag{6b}$$

In equation (6a), the constants K_T and K_b are controlled solely by the motor characteristics. If the output impedance of the power amplifier is small compared to the input impedance of the motor, R_T may be approximated by the motor input impedance. Further the system inertia and drag, J_e and B_e respectively, may be approximated by that of the motor if the inertia and drag of the drum and gear are neglected. These assumptions are commonly used in order to arrive at initial estimates for the remaining system constants, namely K_1, K_2, K_a and N. Because the amplifier gain, K_a, is controlled primarily by other considerations and because K_2 appears nowhere else in the transfer function, equation (6a) may be immediately solved for K_2:

$$K_2 = \frac{1000\ J_e R_T - B_e R_T - K_T K_b}{K_a K_T} \qquad (7)$$

To determine a value for K_1, the steady state error for the system should be taken into account. As has already been discussed the input control signal will be a ramp; the drum position is to be related to the input ramp by some constant "A" plus an error term "B" (refer to Chapter II). The steady state error for the system described in equation (1) is given by,

$$E_{ss}(\infty) = \underset{s \to 0}{\text{Limit}}\ \frac{1}{s}\left[A - \frac{K\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}\right] \qquad (8)$$

$$E_{ss}(\infty) = \underset{s \to 0}{\text{Limit}}\ \frac{1}{s}\left[\frac{s^2 + 2\xi\omega_n s + (A - K)\ \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}\right] \qquad (9)$$

For all values of $K \neq A$, the steady state error becomes infinite. And since,

$$K = \frac{1}{K_1},$$

it follows that $K_1 = A$. As a matter of convenience $A = 1$ was selected. Thus the drum position has a one-to-one correspondence with the input control signal. Finally equation (6b) may be solved for the ratio K_a/N :

$$\frac{K_a}{N} = 509796 \left[\frac{J_e R_T}{K_1 K_T}\right] \tag{10}$$

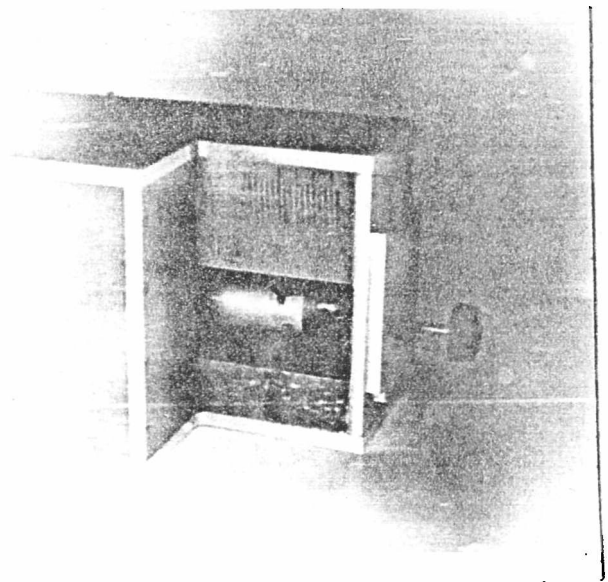
Previously the assumption was made that load inertia and drag could be neglected. The validity of that assumption may now be examined. The effect of the gear ratio on the load inertia and drag is to reduce it by a factor of $1/N^2$. However any arbitrary value for N which might be selected must take into account the rated speed of the motor to be used and the fact that the maximum frequency of operation will be approximately 5 Hz. On this basis the upper limit on the gear ratio turns out to be N = 7 for Motor I and N = 13 for Motor II. An estimate of the required amplifier gain may be calculated directly from equation (10).

With initial estimates for all system constants determined, a computer program was written to generate and plot the time domain response of the system. Through this program, which will be outlined in Chapter V, a number of time domain responses were obtained by varying, individually and jointly, the initial system constants. In this fashion, estimated worst case conditions could be simulated. The results indicated that Motor II, combined with a gear ratio of N = 12.5 and an amplifier gain between 100 and 1000, should be sufficient to achieve the desired system response.

Implementation of the Servo Subsystem required that

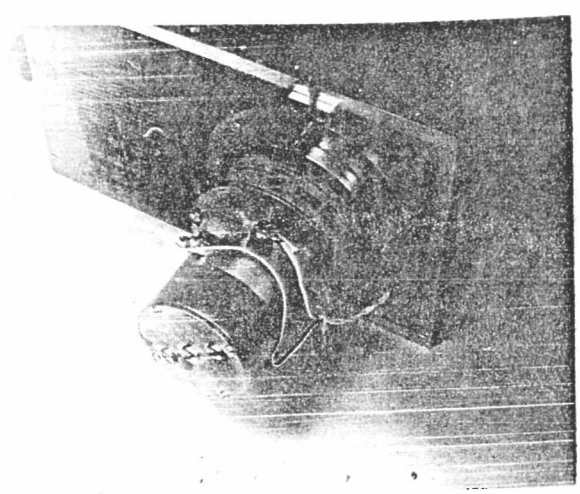
certain mechanical components be designed while others could be selected "off the shelf." The housing (which must be light tight) for the drum and related paraphernalia was constructed with three-eighth inch aluminum plating. It is pictured in Figure IV-3 and Figure IV-4. The drum is located just inside the opening shown in the housing; the opening, of course, will be sealed when the optics assembly is attached. The motor is shown mounted to the housing in the latter picture.

A tachometer was supplied as an integral part of the motor. Thus the velocity feedback constant, K_2, was obtained by tapping the necessary voltage from the tach output. To derive the position feedback constant, K_1, a 360^0 potentiometer was mounted beside the drum supporting rod. Through a one-to-one gear ratio, the potentiometer output was forced to vary directly with drum position: that is, the potentiometer output voltage is incremented by one volt for each radian traversed by the drum. The mechanical configuration is illustrated in Figure IV-5 and Figure IV-6. The gears and supporting brackets were off the shelf items. A standard complimentary symmetry power amplifier was used to obtain the gain constant, K_a. By employing operational amplifiers at the input of the power amplifier, the gain could be easily varied over a wide range of values. Of all the system constants K_1, K_2 and



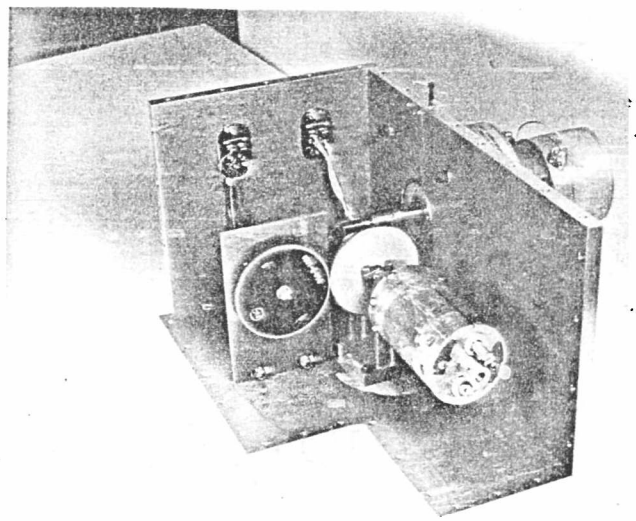
SERVO ASSEMBLY HOUSING

FIGURE IV-3



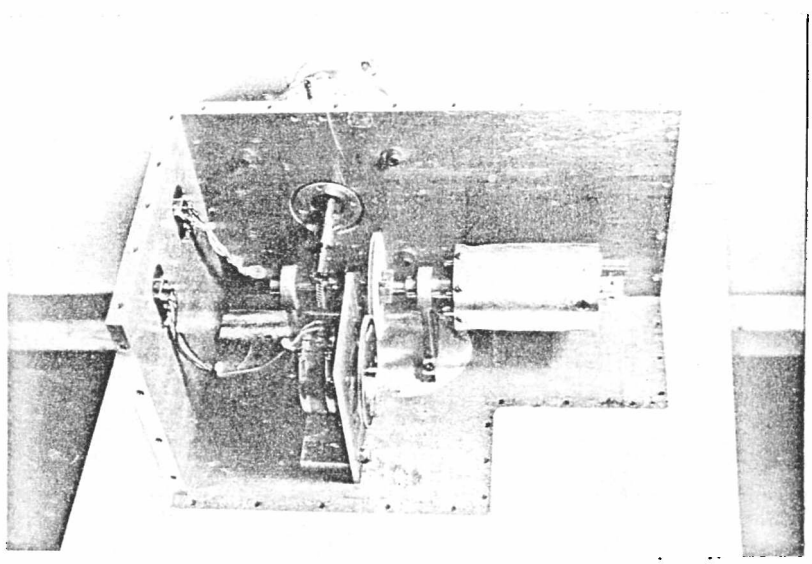
SERVO ASSEMBLY HOUSING - MOTOR MOUNTING

FIGURE IV-4



SERVO ASSEMBLY

FIGURE IV-5



SERVO ASSEMBLY

FIGURE IV-6

K_a are the ones which can be most readily adjusted. For this reason, they were used to calibrate the overall system response of the servo assembly. Their final values are noted in Chapter VI.

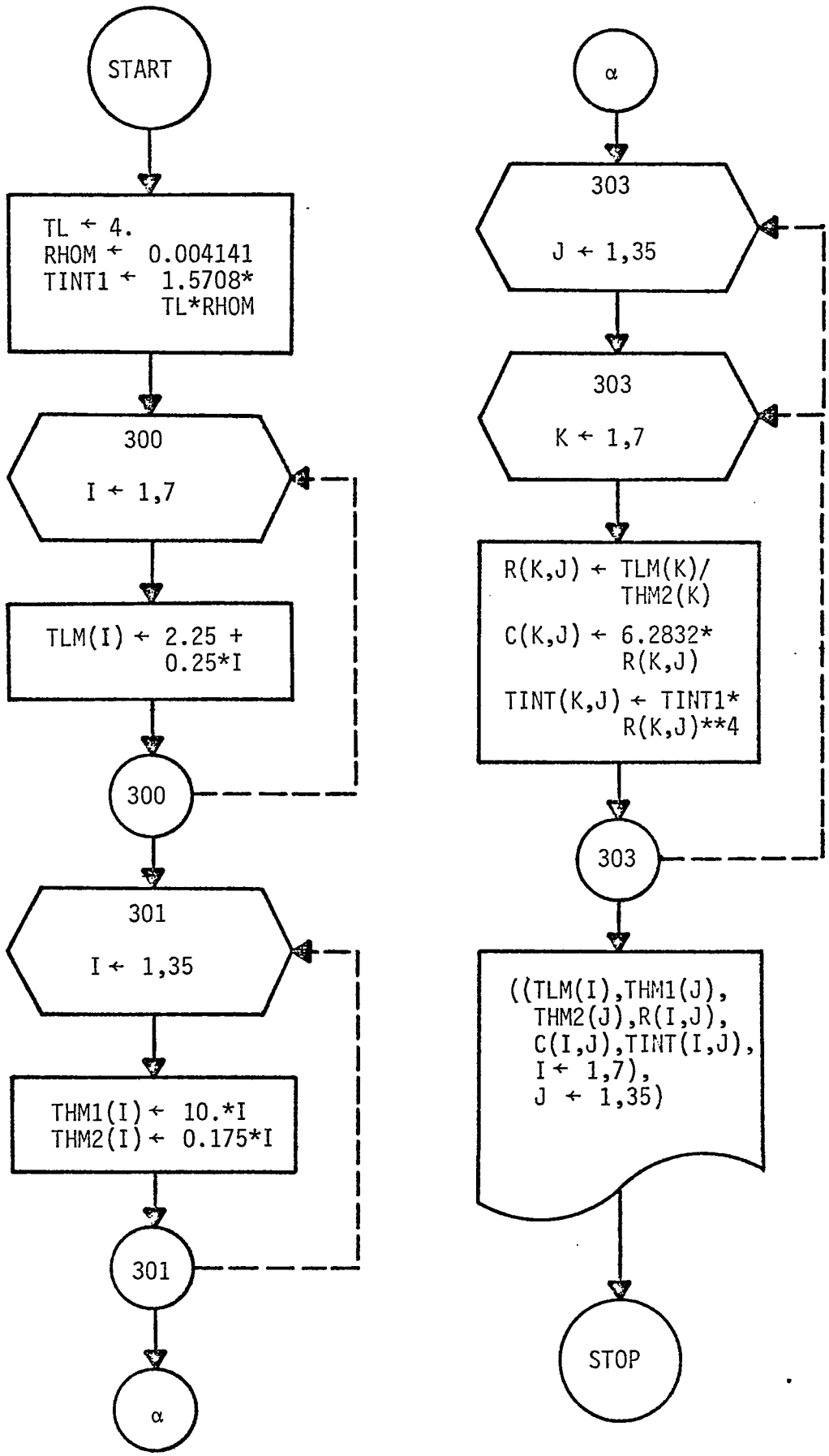
CHAPTER V

COMPUTER AIDS

Two computer programs were developed to assist in designing the Electro-encephalographic Signal Averager. The first generated data to be utilized in selecting appropriate dimensions for the film-carrying drum. The second program provided computer simulation of the Servo Subsystem's time domain response for a variety of system constants. It contains a plot routine so that the system response may be portrayed graphically.

A flow diagram for the Drum Data program is shown in Figure V-1. TL is the drum length. RHOM is the mass density of aluminum. TINT1 is a constant required to calculate drum inertia (see equation (2) in Chapter IV). The first vector generated, TLM, corresponds to L_θ; it is assigned values between 2.5 and 4.0 inches. Next THM1, which corresponds to θ_f in Figure IV-2, is assigned values between 10 and 350 degrees; THM2 stores the corresponding angles in radian measure. Finally values for drum radius,circumference and inertia are calculated for all combinations of L_θ and θ_f.

Figure V-2 is a flow diagram for the System Simulation program. It employs a Runge-Kutta algorithm to numerically solve a system of state variable equations. For the second



DRUM DATA PROGRAM

FIGURE V-1

order system considered here, only two state equations are required. Initially the system and program control constants are read. The meaning of each constant is given below.

N.....the number of state equations

NP.....the number of data points to be calculated

IPROB.....the problem number associated with a particular set of constants

ST.....the starting time

DT.....the time increment to be used in the algorithm

CJE.....the system inertia

CBE.....the system drag

RT.....the combined amplifier output and motor input impedance

CB.....the back emf constant

CT.....the torque constant

CN.....the gear ratio

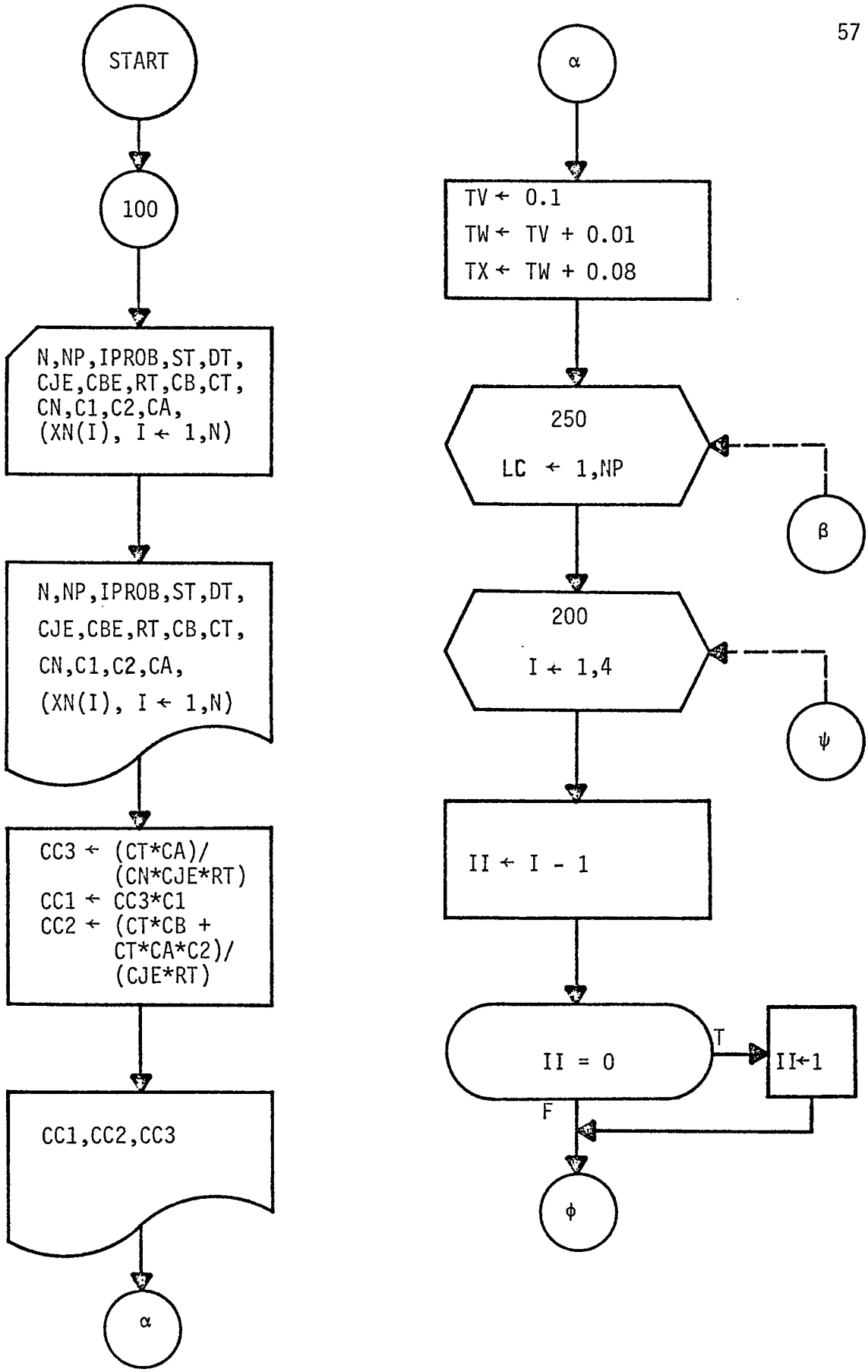
C1.....the position feedback constant

C2.....the velocity feedback constant

CA.....the gain constant

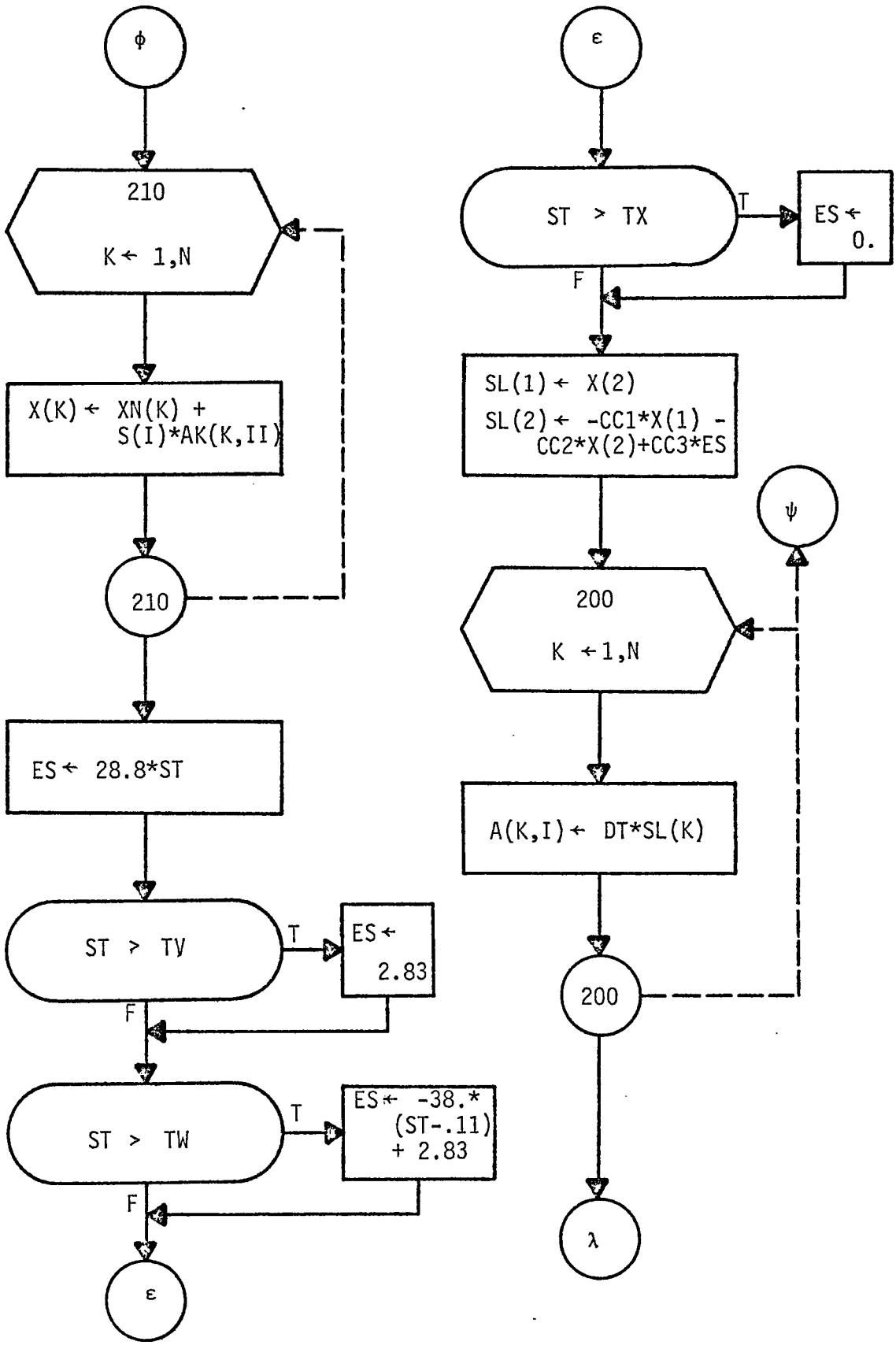
XN.....the initial values assigned to each state variable

Next the coefficients required in the state equations are calculated from the system constants. TV, TW and TX are assigned values to be used in the algorithm to assist in generating the control signal Φ_c. The first DØ loop



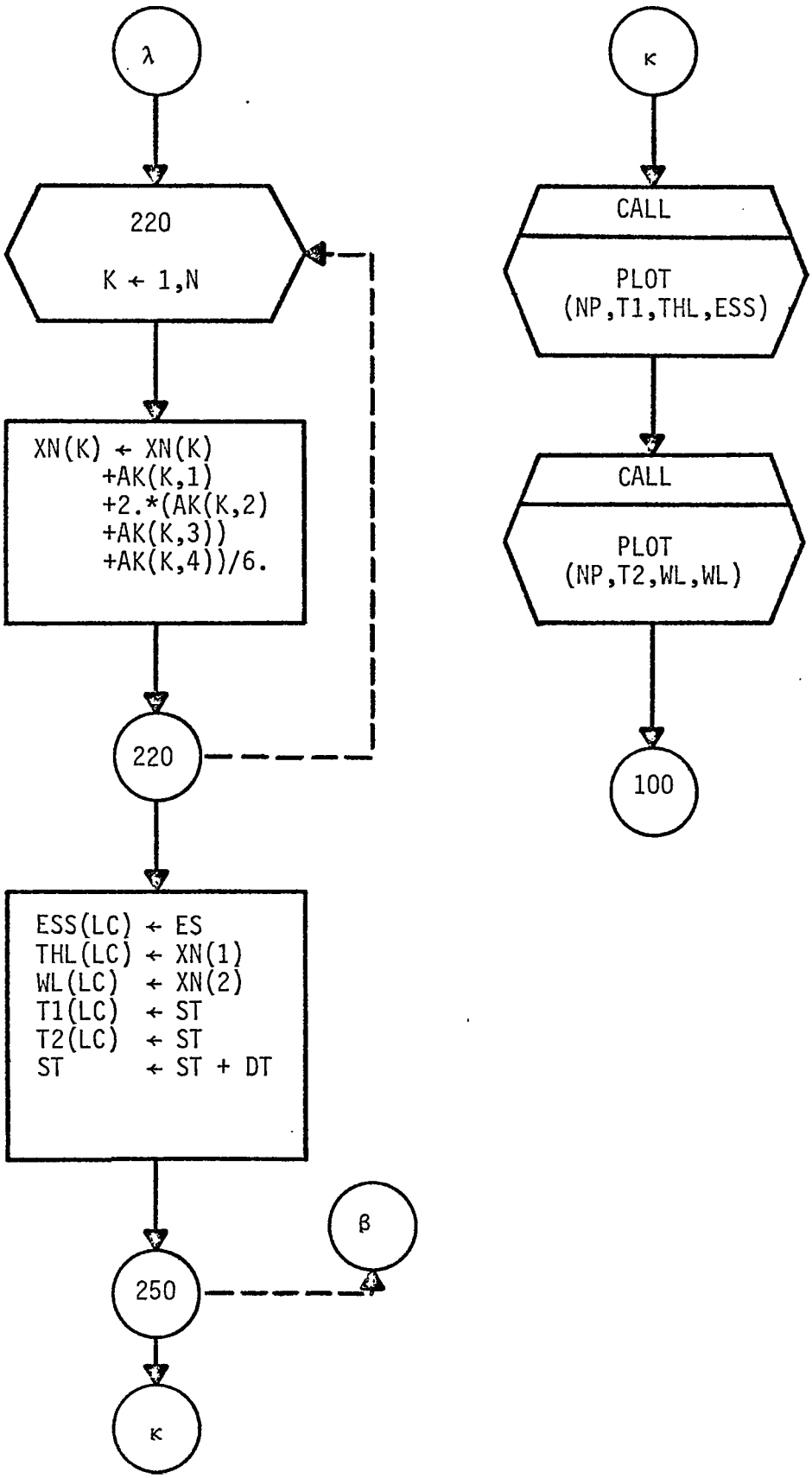
SYSTEM SIMULATION PROGRAM

FIGURE V-2



SYSTEM SIMULATION PROGRAM

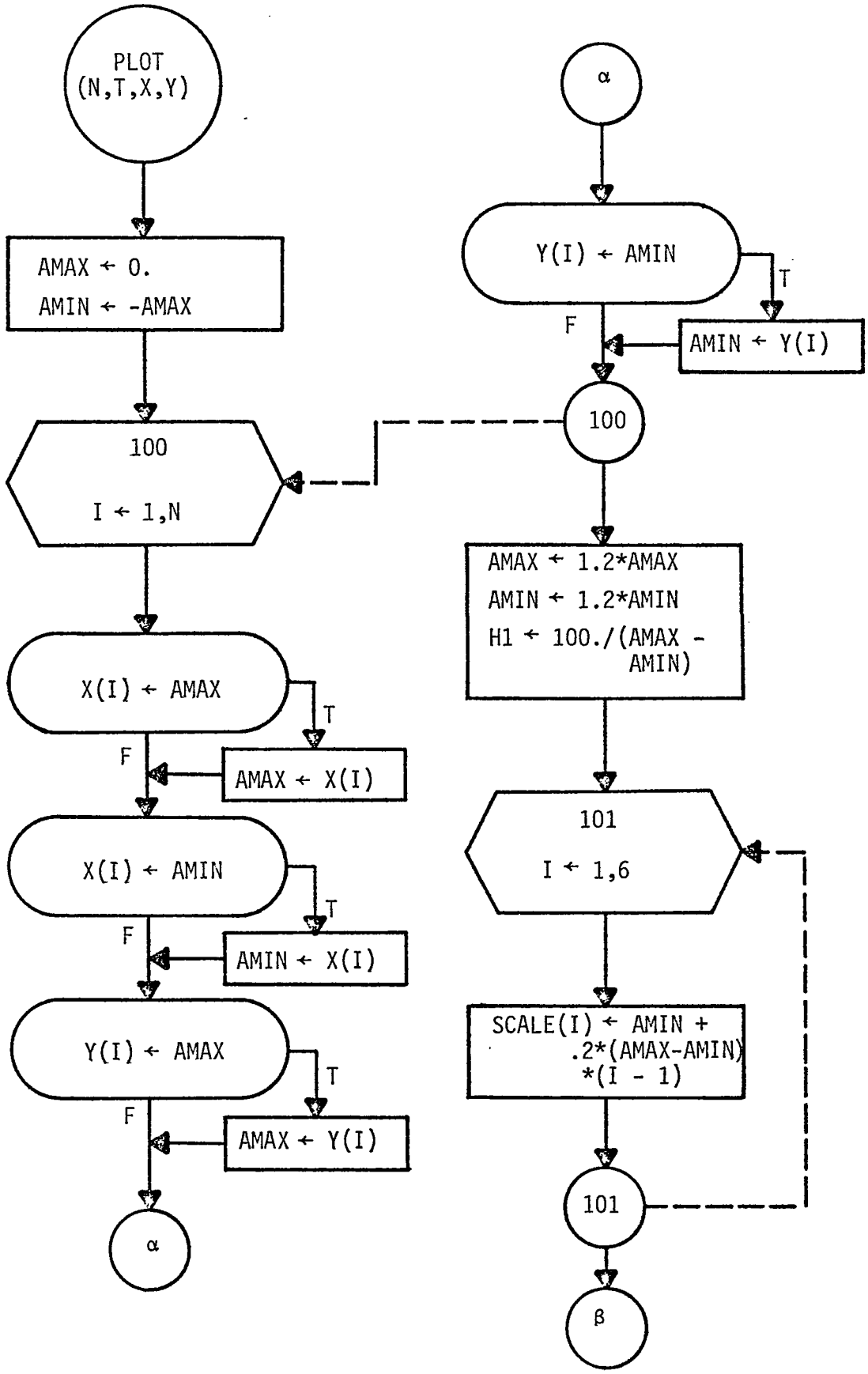
FIGURE V-2 (CONT.)



SYSTEM SIMULATION PROGRAM

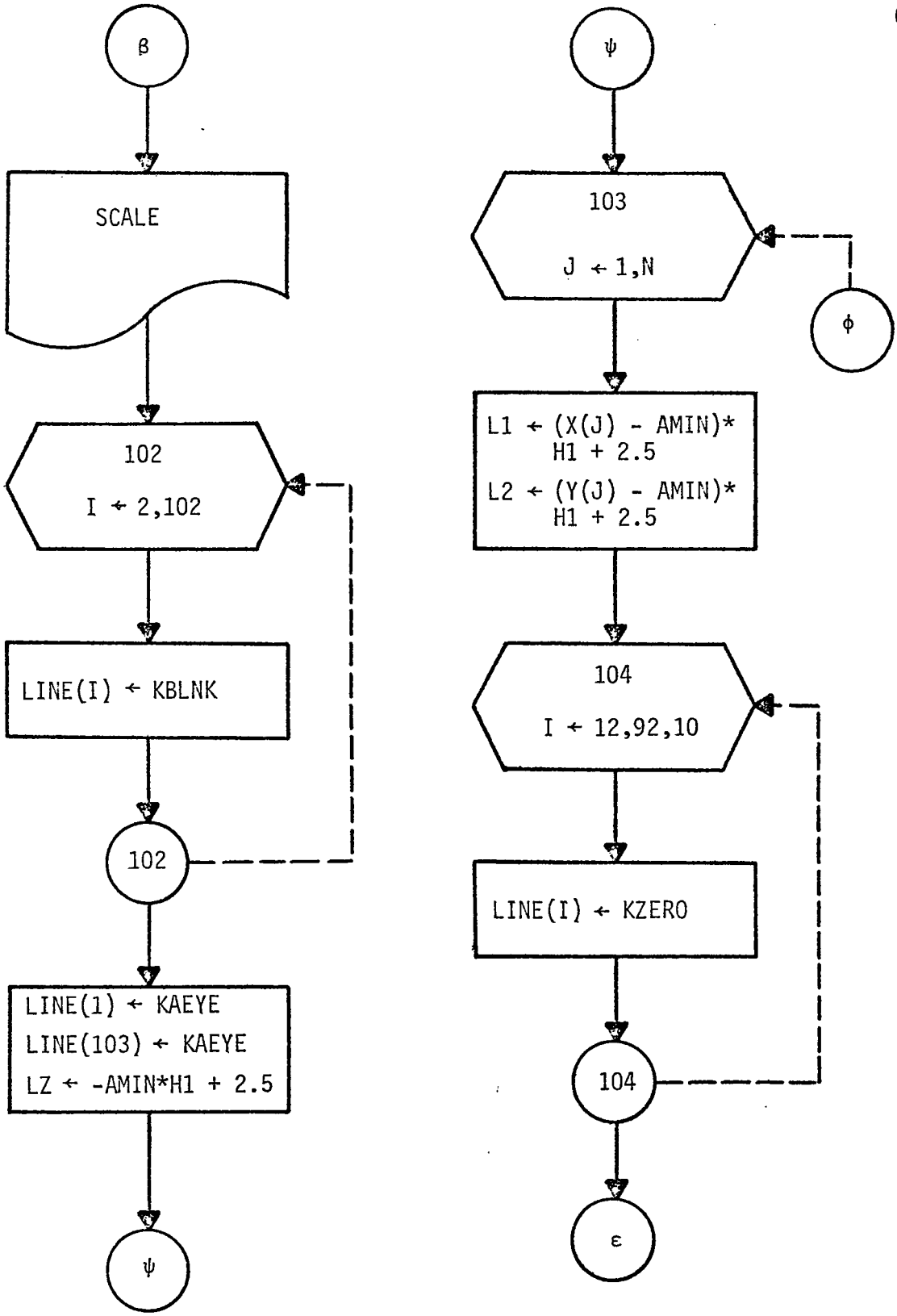
FIGURE V-2 (CONT.)

encountered is the beginning of the Runge-Kutta algorithm. It is straightforward and may be easily followed. Note that ES represents the control signal at any given time during the process. The vectors ESS, THL and WL are used to store the calculated data points for the control signal, the drum position and the drum speed, respectively. T1 and T2 store the incremental times associated with each data point. Upon completion of the algorithm, subroutine PLØT is called to generate a graphical representation of the data. The subroutine was not written for this program. It is a commonly used routine which has an unknown origin. Its flow diagram is given in Figure V-3 as a matter of completeness.



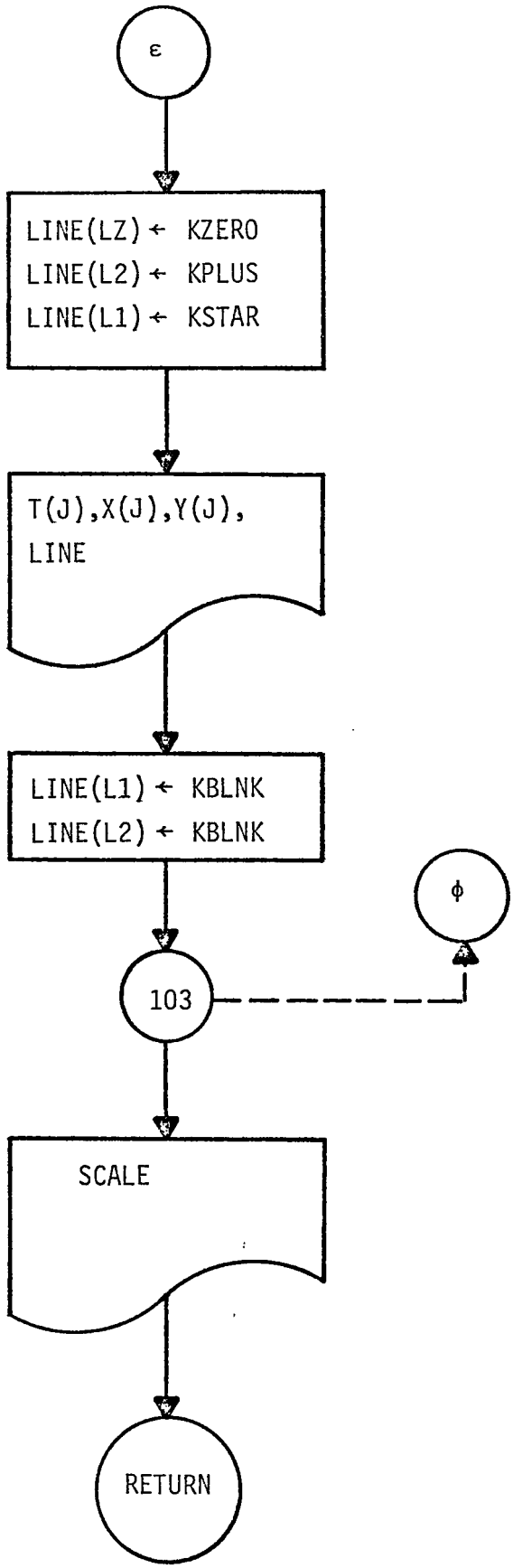
SUBROUTINE PLØT

FIGURE V-3



SUBROUTINE PLØT

FIGURE V-3 (CONT.)



SUBROUTINE PLØT

FIGURE V-3 (CONT.)

CHAPTER VI

TEST AND EVALUATION

Testing of the Electro-encephalographic Signal Averager was accomplished in three phases. First the Electronic Timing and Control Subsystem was examined at numerous points in the circuitry to verify that its operation was as predicted. The second phase consisted of calibrating, then monitoring the Servo Subsystem; in particular, the drum position was compared to the Control Signal, Φ_C. As a final test, the Signal Averager was used to photographically record several electronically generated signals.

A large number of randomly selected TW switch settings were used to confirm that the Main Inhibit signal was generated at the appropriate time, i.e., the system halted operation upon completing a preset number of cycles. For low TW switch settings (less than 100), valid operation was substantiated by observing the LED Display and by counting, on a storage oscilloscope, the actual number of generated Control Signals. For high TW switch settings, only the LED Display was employed to confirm proper operation. In all cases the system performed as anticipated.

Each Control Signal was carefully examined on a storage oscilloscope to determine whether any significant non-linearities could be detected. The linearity of each Main Sweep, as well as the Reset Sweep, was less than one percent. In fact the non-linearities were so small that they could not be precisely determined. In addition to these

obvious checks, numerous signals throughout the Electronic Timing and Control Subsystem were monitored; proper functioning of all operational modes (Mode 1, Mode 2 and Manual) was confirmed. No deviation in expected performance was found in any of the tests.

The Servo Subsystem was tested using each of the three control signals. Its response was calibrated by varying the position and velocity feedback constants as well as the gain constant. As expected the best response was obtained with a position feedback constant of $K_1 = 1$. The velocity feedback constant, K_2, and the gain constant, K_a, were varied over a wide range of values. To determine an optimal combination of the two, the drum position was monitored at the position potentiometer output and compared to each Control Signal. An optimal response was obtained for $K_2 = 0.000018$ and $K_a = 1200$. These selections resulted in an initial response time (t_1 in Figure I-1) of approximately eight milliseconds, a value which satisfies the original design criteria. Using these constants and certain other parameters obtained from testing the Servo Subsystem, the equations developed in Chapter IV may be used to estimate the actual system inertia and drag:

$$J_e = 0.0022 \quad \text{oz-in-sec}^2$$

$$B_e = 0.94 \quad \text{oz-in-sec/rad}$$

These values are somewhat higher, by approximately a factor of between three and four, than originally assumed. However the difference did not cause significant degradation of estimated system performance.

To illustrate its photographic capability, the Signal Averager was used to record several electronically generated signals. No problems were encountered in this process.

Extensive testing will be required to determine whether photographic signal averaging will yield superior electro-encephalographs to those obtained by other methods. However the concept and feasibility of photographic signal averaging has been demonstrated.

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