Multi-Phase DC Power Supply Topologies with Fast Response for Telecom and Point-of-Load Applications

by
Srikanth Yerra

A dissertation submitted to the
Department of Electrical and Computer Engineering,
Cullen College of Engineering
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

Chair of Committee: Dr. Harish S Krishnamoorthy

Committee Member: Dr. Kaushik Rajashekara

Committee Member: Dr. Yuhua Chen

Committee Member: Dr. Xingpeng Li

Committee Member: Dr. Joshua T. Hawke

University of Houston
May 2021

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor, Dr. Harish S. Krishnamoorthy for providing the opportunity to conduct my PhD research at the Power Electronics, Microgrids, and Subsea Electrical System (PEMSES) Center at the University of Houston. His invaluable mentorship and guidance helped me to explore the challenging research areas throughout my PhD studies. He has provided me all the facilities to conduct my research independently and provided me the opportunities to explore and grow professionally. I am greatly indebted to Prof. Kaushik Rajashekara and Dr. Joshua T. Hawke for their invaluable guidance during the initial stages of my research. I do not have words to express my thanks to both Dr. Krishnamoorthy and Prof. Raja for their valuable support to overcome the difficulties in my professional and personal life. I am privileged to have a PhD committee involving Dr. Kaushik Rajashekara, Dr. Yuhua Chen, Dr. Xingpeng Li, and Dr. Joshua T. Hawke. I extend my sincere gratitude for their insight and guidance in this research work.

I would like to thank my master's thesis advisor Dr. Kumaravel S., and Dr. Saly George at the National Institute of Technology Calicut, and Prof.(ret.) K. A. Gopal Rao, for their encouragement to pursue my PhD. I would also like to thank my undergraduate faculty, Dr. Srinivas Rao Gorantla, Dr. Srinivasa Kishore Babu Yadlapati, Ms. Suman Chowdary, Dr. Subba Rao Mopidevi, and other faculty members at Vignan University, for their support and motivation to pursue my higher studies.

I would like to acknowledge the students and postdocs of the PEMSES research group, who contributed to my professional and personal enrichment. I would like to thank Dr. Gnana S. Kulothungan, Dr. Krishnaraj Potti, Dr. Sathish Naik Banavath, and Dr. Sumit Pramanick for their valuable advice. I thank Venkat, Partha, Anindya, Shilei, Amin, Yu Yao, Vinay, Jean, Tania, Amir, Steven, Arun, Mingjian, Cunzhi, Hussain, and other students of the PEMSES lab for making learning easy and joyful at the PEMSES lab.

I extend my gratitude to all my colleagues from Gayatri Vidya Parishad College of Engineering, Canoo, Modern electron, and Halliburton, where I have worked/interned at various points of time, for providing me with deep knowledge and career guidance.

Finally, I thank my parents Suseela, Mohan Rao, my sister Pushpalatha, brother-in-law Subbarao, relatives, and friends for their unconditional love and support throughout my studies. I express my sincere gratitude to my uncle Subbaramaiah, brother Ram Yerra and my cousin Venkat Kankanala. Without their motivation and guidance in the early stages of my education, I couldn't have reached this milestone in my life.

Srikanth Yerra
Houston, May 2021

ABSTRACT

The evolution of the 4G/5G communication networks along with high-speed computing and datacenter facilities increased the demand for compact, efficient, and reliable power supplies with faster output response speeds. The advancements in high-speed semiconductor switching devices and magnetics have constantly raised the scope for the design of efficient, compact power supplies with a faster dynamic response. These opportunities and requirements are contributed to undertake the research proposed in this work.

In high-speed radio frequency (RF) communication applications, when supplied with a constant power source the radio frequency power amplifier (RFPA) dissipates energy in the form of heat. This power loss increases proportionately with the speed of the communication system. This needs more cooling and makes the overall system bulky. In this work, efficient power supply topologies with fast varying output voltage are proposed to modulate the drain power supply of an RFPA and reduce the loss dissipation. Multilevel converters are explored as a suitable option for this application and high-frequency gate drive circuits are proposed. A cascaded switching capacitor-based three-level multi-phase converter is proposed to eliminate complex switching capacitor voltage control circuitry. A modified PWM technique is introduced to maintain a linear relationship of output to the input voltage. Zero voltage switching (ZVS) output filter design is proposed to reduce turn-on switching loss and maintain current self-balancing in the multi-phase converter.

Point-of-load (POL) regulators are used in the DC power distribution of data centers to convert high DC bus input voltage (12 V – 48 V) to the low POL output voltage (1.2 V – 6 V). The load current demand fluctuates rapidly over a wide range, and if it's not properly taken care of, the output voltage fluctuates and may damage the sensitive load equipment. In addition, data centers consume a large amount of power which leads to the development of high-efficiency power converters to remain cost-effective. In this work, a single-stage efficient POL converter is proposed to address the high-speed load current transients and regulate the output voltage. A variable switching frequency scheme is proposed to improve the light load efficiency and current self-balancing is used to improve the power-sharing in the multi-phase converter.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. INTRODUCTION

1.1 Introduction

The world has seen a tremendous rise in computing speeds, data transfer rates in the last decade driven by the widespread adoption of high-speed communication networks such as 3G and 4G. The recent advancements in 5G enable high-speed communication and enabling several breakthrough technologies such as the Internet of Things (IoT), autonomous driving, and connected cars. According to a new report by Reports and Data, the globally connected car market is expected to reach USD 197.12 Billion by 2026 [1]. To meet these growing high-speed communication requirements and data demands the autonomous cars and IoT devices need to be equipped with high-speed computing and communication facilities along with the erection of high-speed communication base stations. RF transmitter system, which transmits the signal is the essential part of the communication system. To meet the performance objectives such as peak to average power ratio (PAPR) of this high-speed RF transmitter system an efficient, compact, and high bandwidth power supply is required.

Data centers, also known as server farms, storing most of the world's digital information. The availability of this data is of crucial importance to data center customers as an unreliable data service will not survive the fierce competition. A reliable power supply and distribution architecture immediately draw attention in this regard. The load current of the high-speed computing facilities is highly transient and requires an efficient voltage regulator. Furthermore, data centers consume large amounts of

electrical energy in trying to keep up with the energy demand associated with the rapid performance increase of the server technology itself. However, increasing energy prices are forcing data centers to re-evaluate their energy consumption and increase their electrical efficiency to remain profitable [2].

Envelope tracking power supply and point of load (POL) regulators are the two major power supply types that meet the fast-varying output voltage and current transients respectively. These power supply architectures are discussed in the later sections of this chapter and a research statement is formulated at the end.

1.2 **RF Transmitter System**

A high-speed wireless communication system consists of an RF transmitter to amplify and transmit the baseband RF signal. The basic block diagram representation of a traditional RF transmitter system supplied with a fixed DC voltage source is shown in Figure 1-1. The Power Amplifier (PA) in the RF transmitter system is the most essential component of the communication base station, which amplifies and transmits the input RF signal. To achieve fast wireless access speeds, spectrally efficient and complex modulation schemes are used, which requires that the RFPA be highly linear to preserve the modulation and, then transmit the data (in-band linearity). Unfortunately, highly linear PAs demonstrate low efficiency and hence increased power consumption and heat dissipation in the form of loss [3]. The efficiency of the PA further deteriorates when amplifying signals with a high peak to average power ratio (PAPR). When operating with a constant drain supply voltage, RFPA dissipates power in the form of

heat and requires a large cooling system. High-speed communication systems – such as 4G and 5G, with a high PAPR – produces higher loss that increases the size of the cooling system and RF transmitter. The PAPR of various communication standards is given in Table 1-1 [4]. The spectral efficiency increases with the carrier bandwidth (BW) so as the PAPR.

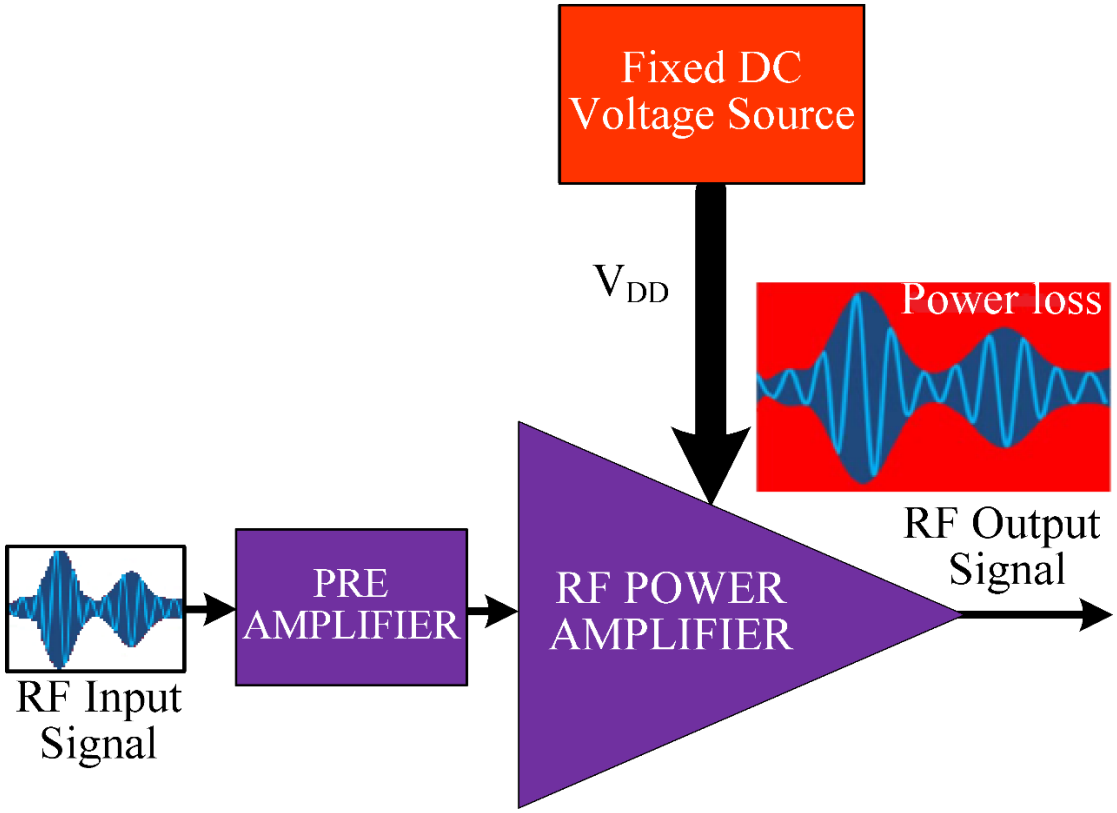


Figure 1-1: Basic block diagram representation of a traditional RF transmitter system supplied with a fixed DC voltage source.

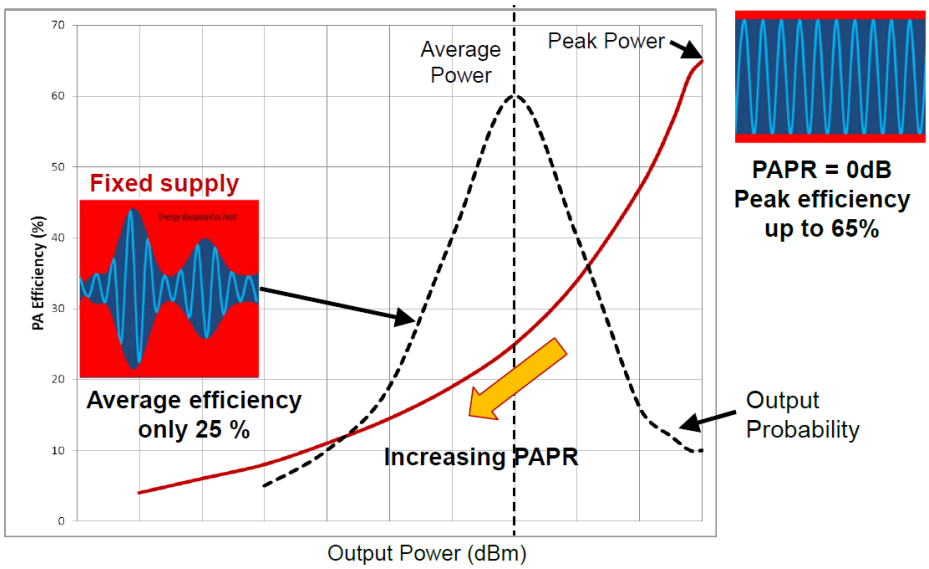


Figure 1-2: Effect of PAPR on the efficiency of RFPA (Adapted with permission from the Efficient Power Conversion [4]).

The effect of PAPR on the efficiency of the RFPA is shown in Figure 1-2. The average efficiency of the RFPA is very low (~ 25 %) when supplied with a fixed drain voltage source.

1.2.1 Methods to Improve the Efficiency of RFPA

Various power supply architectures are introduced in the last decade to meet these improved PAPR and to manage the tradeoff between enough linearity, and low power consumption [5]. These are broadly classified into three categories:

- Load modulation, where the load resistance is modulated over output power to increase average efficiency
- Linear amplification using nonlinear components, where the PA always operates with a non-variable input drive amplitude and, hence, at maximum efficiency

- Supply modulation, where the drain voltage (V_{DD}) is modulated to enhance efficiency.

Load modulation is further classified into dynamic load modulation [6] and Doherty modulation [7]. Outphasing [8] is one of the forms of linear amplification using nonlinear components [3] gained interest in recent years due to the improvements in the digital signal processing capabilities. Polar transmitter [9], envelope tracking (ET) [10], [11], envelope elimination and restoration (EER) [12] are various drain supply modulation techniques. Combinations of these supply modulation techniques have been investigated in [13], [14].

Table 1-1: PAPR of various communication standards [4]

	Standard	**Launched**	**Typical Carrier BW (MHz)**	**Typical Spectral Efficiency (bps/Hz)**	**Approx. PAPR (dB)**
2G cellular	GSM	1991	0.2	0.17	0.0
2.75G cellular	GSM+EDGE	2003	0.2	0.33	3.5
3G cellular	WCDMA FDD	2001	5	0.51	7.0
Digital TV	DVB-T	1997	8	0.55	8.0
Wi-Fi	IEEE 802.11a/g	2003	20	0.9	9.0
WiMAX	IEEE 802.16d	2004	20	1.2	8.5
Wi-Fi	IEEE 802.11n	2007	20	2.4	9.0
3.5G cellular	HSDPA	2007	5	2.88	8.0
3.9G cellular	LTE	2009	20	8.00	10.0

1.3 Envelope Tracking Power Supplies

ET found more extensive application among the other techniques due to its better linear characteristics and relaxed requirements on the supply modulator [11], [15]. ET is very much a technology of the present and has found commercial success for high bandwidth supply modulation techniques [16]–[18]. Figure 1-3 shows the simplified block diagram of a basic ET transmitter in which the drain supply voltage is modulated to track the envelope of the RF input signal. The envelope of the input RF signal is extracted through an envelope extractor and fed to the ET power supply as a reference signal, which is supplied with a fixed DC voltage source.

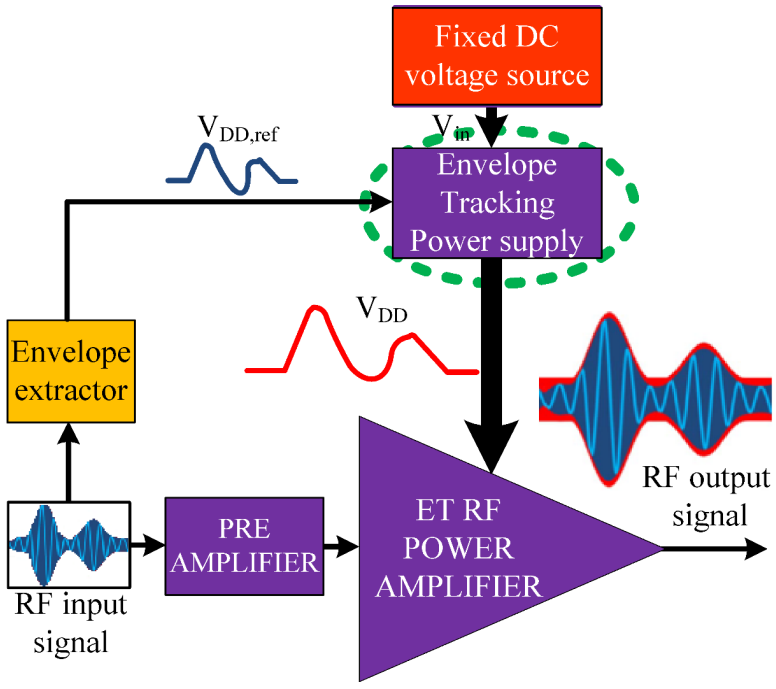


Figure 1-3: Basic block diagram representation of an RF transmitter system supplied ET power supply modulator.

To achieve high efficiency of the RF transmitter system, the ET power supply is expected to operate with high efficiency. Figure 1-4 shows the effect of ET on the efficiency of RFPA. The average efficiency, where the output has the highest probability is improved to ~50 %.

Various ET power supply topologies have been reported in the previous research publications. Based on the architecture, they are classified into three main categories namely, linear amplifier structure [19]–[22], switching converter structure [23]–[42], and linear assisted switching converter structure [42]–[53].

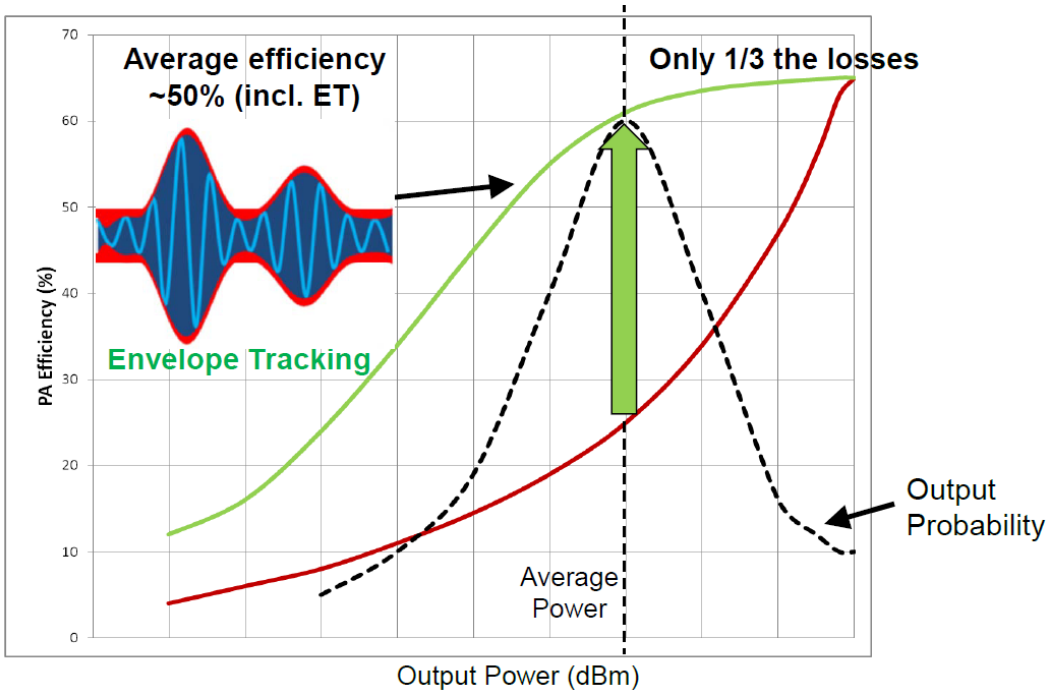


Figure 1-4: Effect of ET on the RFPA efficiency (Adapted with permission from the Efficient Power Conversion [4]).

1.3.1 Linear Amplifier based Envelope Tracking

Linear amplifiers provide high bandwidth and low output voltage ripple for ET power supply applications. They have very good envelope tracking capability with no spectrum disturbances. But, the efficiency of linear amplifiers is not very high and is limited to a theoretical maximum of 78.5 % [15]. The efficiency of the linear amplifier decreases with the output voltage [51]. Moreover, the higher PAPR of the ET signal would further deteriorate the efficiency of the linear amplifiers. Hence, linear amplifier alone is not an effective solution for high power ET applications such as base station communication systems.

1.3.2 Linear Assisted Switching Converter based Envelope Tracking

To improve the efficiency of ET power supply linear assisted switching converter-based ET is proposed. They are also known as hybrid ET power supplies in which the switching converter process the high power low-frequency components of the envelope signal where as the linear amplifier tracks the high bandwidth ET signals of low power. With proper band separation, the linear assisted switching converter provides the combined benefits of accurate tracking of high bandwidth envelope signal at improved efficiency. Figure 1-5 shows the basic architecture of linear assisted buck converter ET power supply topology. Several buck converters are interleaved to obtain increased effective switching frequency (also bandwidth) as well as the output power. The switching buck converter tracks the lower bandwidth (~ 10 %) envelope and

supplies the majority of the output power (~ 90 %), whereas the linear amplifier supplies the remaining power at the highest bandwidth (~ 90 %).

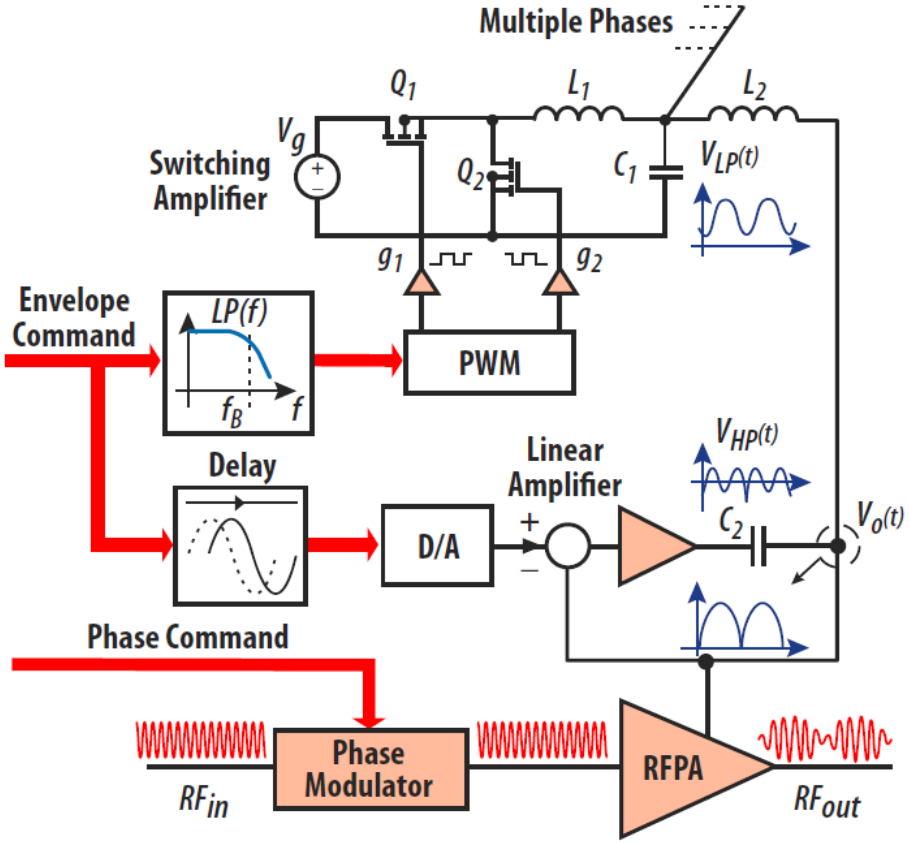


Figure 1-5: Basic architecture of Linear Assisted Switching Converter based Envelope Tracking Power supply.

1.3.3 Switching Converter based Envelope Tracking

Switching converters provide high efficiency than linear amplifiers. Therefore, switching converters are preferred to construct the ET power supply. Buck converter in open-loop control mode is preferred in the construction ET power supply due to its simple structure. Moreover, the control to output voltage has a linear relationship and is

easily scalable for high bandwidth and high PAPR applications. Several single-phase [39], [40] and multi-phase [24], [27], [38] power supply structures have been presented in the literature. Various types of Low pass filter (LPF) designs are [54], [55] used to filter the switching ripple and to track the envelope signal accurately.

Switching converters need to be switched at a high switching frequency to accurately track high bandwidth envelope signals. In general, the bandwidth of the output LPF is selected as $1/5^{th}$ of the effective switching frequency of the converter to maintain proper switching ripple attenuation. The bandwidth is in direct relationship with switching frequency and results in increased switching loss at the high switching frequency for high voltage ET applications. Recently, the evolution of wide band-gap devices, such as eGaN FETs led to the design of high-frequency switching converters [44], which enabled higher bandwidth ET at improved efficiency. A 10 W synchronous buck converter was designed with GaN high electron mobility transistors [23] to switch up to 40 MHz with an efficiency of 90 %. A multi-phase buck converter was designed in [24] using eGaN FETs to track large signal bandwidth of 20 MHz for 4G LTE base stations. The output voltage of the envelope varied up to 28 V and the total efficiency is 92.3 % when delivering a 67 W average output power from 30 V input. For high voltage and high bandwidth ET, the switching loss dominates and leads to poor efficiency if traditional two-level converters are used. Hence several, multi-input and multi-level topologies are introduced to overcome this issue.

1.4 Multi-level Switching Converter for ET

To reduce, the switching losses for higher bandwidth and higher voltage ET applications, multiple-input multi-level converters have been proposed. A MASH-controlled multilevel power converter using multiple input voltage sources was proposed in [25]. Power digital to analog converter concept using three input voltage sources to produce 8-level output voltage with GaN-on-Si switches was introduced in [26]. The output voltage tracked envelope bandwidths of up to 10 MHz with a resolution of 6 V. A monolithic multi-input multilevel converter tracking 10 MHz LTE envelope signal with well-damped level-to-level transients is proposed in [41]. A major drawback of such multi-level topologies for ET applications is that they need multiple voltage sources. Also, the output voltage is in steps deviates from the reference envelope signal. This additional output voltage leads to reduced RFPA efficiency.

1.5 Point of Load Regulators

The rapid growth of the computing and telecommunication market is challenging a more compact, efficient, and high-power density solution for intermediate bus converters [56]. The DC distribution architecture shown in Figure 1-6 has been suggested as an efficient method of power delivery for a data center [57]–[59]. This concept is inspired by the absence of reactive power, the possibility of efficient integration of small, distributed generation units, e.g. fuel cells and photovoltaic arrays, and also, all the loads operate using a low DC voltage [60]. The DC bus voltage level varies according to the amount of energy required by the data center. A 48 V DC bus is

commonly used in telecommunications facilities and would require bulky conductors. Therefore it is impractical to distribute DC power to large loads at 48 V but this problem can be overcome by increasing the distribution voltage to 480 V and stepping it down on the server cards to lower values (43 – 53 V) on an intermediate DC bus [61]. This intermediate DC bus can be used to reduce the transformation ratio between the DC bus voltage and the final voltage required by the microprocessor load. The point-of-load (POL), or voltage regulation modules (VRM) are DC-DC converters that regulate the respective output voltages to the required tolerance without providing galvanic isolation.

Point-of-load voltage regulators with reduced noise and faster dynamic response are key components in the high-speed computing and data center power supply applications. Therefore, the performance of power converters needs to be improved to mitigate the issues with noise and power losses at high current values. In general, the POL regulator systems typically use two-stage conversion (for example, 48 V to 12 V and 12 V to 5 V) as shown in Figure 1-7. Many researchers proposed two-stage conversion-based topologies [62], [63] for this purpose. With such an architecture, the efficiency of the conversion system is lower, especially during the light load operation. Moreover, the two-stage conversion results in lower power density. To overcome these issues, the research focus was shifted to the development of single-stage POL conversion approaches.

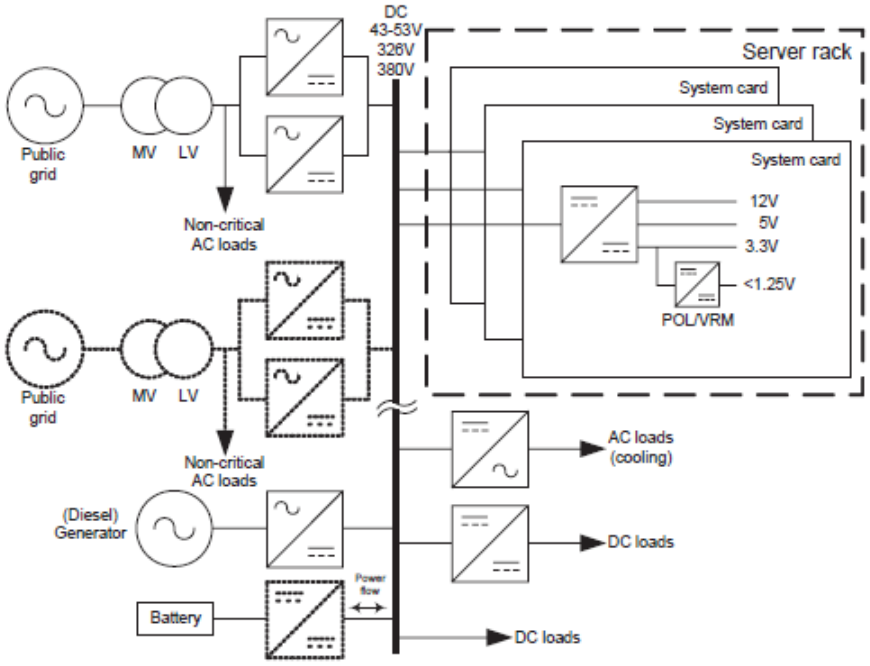


Figure 1-6: Typical DC distribution architecture of data centers (Courtesy: www.leonardo-energy.org) [2].

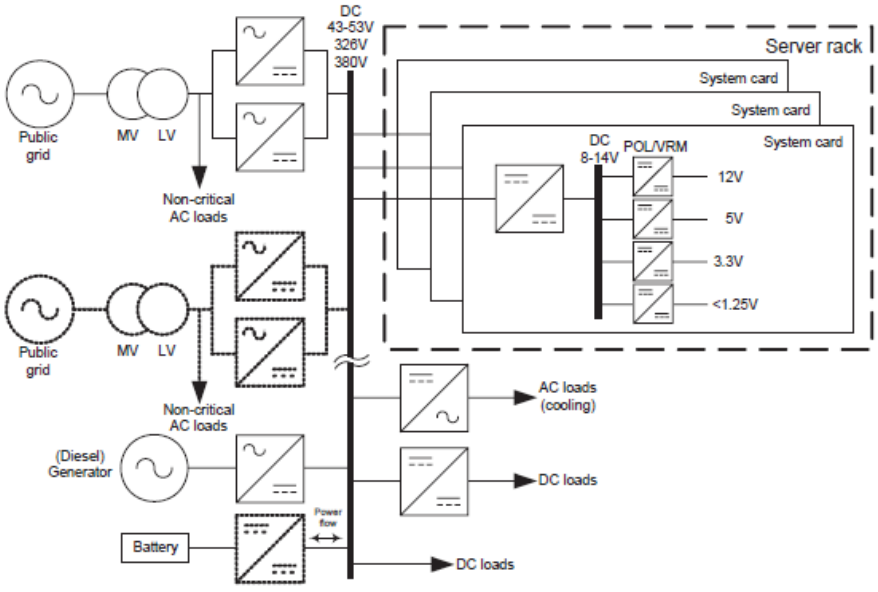


Figure 1-7: DC distribution architecture with the intermediate bus (Courtesy: www.leonardo-energy.org[2]).

1.6 **Research Objective**

A high bandwidth ET converter that uses traditional buck converter topologies suffers from switching loss at the high switching frequency of operation. The device voltage rating is a limiting factor to the usage of traditional buck converter for high voltage ET applications. Various multi-level converter architectures that use multiple input voltage sources are proposed in the literature to overcome the limitations of traditional two-level buck converters. But the use of multiple-input voltage sources increases the cost and complexity of the system. The losses associated with these multiple isolated sources contribute to the poor overall system efficiency of the RF transmitter system.

The converter, which supplies step wave output voltage contributes to loss in RFPA as shown in Figure 1-8. And also, the two-stage POL regulators have poor efficiency. To overcome this issue, various single-phase and multi-phase three-level buck converters are proposed in this work. Zero voltage switching (ZVS) LPF design is proposed to reduce the switching loss while ensuring current balancing in the multi-phase converter.

The power converter topologies are derived with the motivation to combine the advantages and mitigate limitations of multi-phase buck and multi-level buck converters presented in the literature. In addition, a single-stage POL conversion concept is proposed in this work, to mitigate the efficiency issues associated with the two-stage conversion approach in the data center DC power distribution architecture.

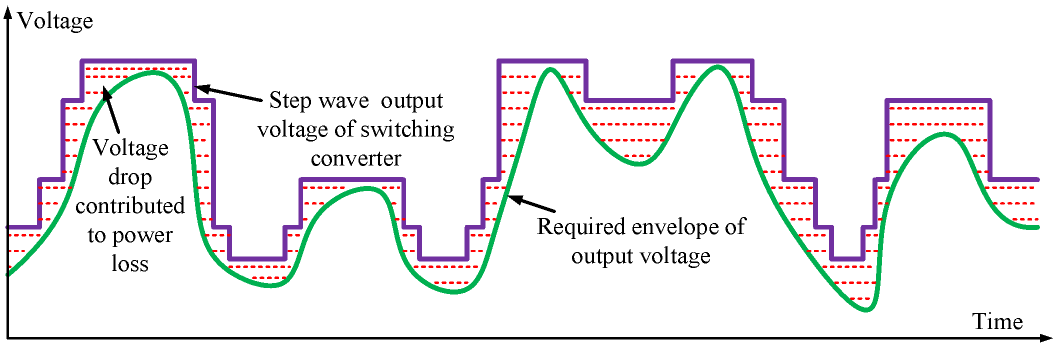


Figure 1-8: Tracking error and loss associated with step wave output voltage of the multi-level ET converter.

1.7 **Dissertation Outline**

This dissertation is organized into seven sections. Chapter 1 introduces the need for efficient power supply requirements of modern cyber-physical systems. Various combinations of power supply architectures and their pros and cons are discussed. The advantages of using wide bandgap MOSFETs in switching converters for high bandwidth power supply applications are presented and various multi-input and multi-phase buck switching topologies are reviewed. The section concludes with a description of the research objective.

Several converter configurations and a simple gate driving technique for ET is proposed in chapter 2 to chapter 5. A single-stage POL regulator is presented in Chapter-6. The outline of this proposal is presented in this section.

In chapter 2, a flying capacitor-based three-level (FCTL) buck converter is studied as a potential candidate for high voltage envelope tracking application. A fourth-order Legendre-Papoulis filter is used to track envelope signal bandwidth of up to 8 MHz. A prototype of the proposed high-frequency FCTL was built with minimal gate

loop and power loop inductance. The details of the PCB layout to minimize the effect of parasitics are presented. The efficiency of the proposed design is then compared with the conventional two-level buck equivalent. Finally, the section is concluded with simulation and experimental verification.

A simplified gate driving strategy for an FCTL buck converter is proposed in chapter 3. The proposed gate drive technique uses a single auxiliary DC power supply and novel cascaded bootstrap architecture to supply the gate voltages. A hardware prototype of the proposed concept is developed and results are presented up to a switching frequency of 40 MHz. The gate drive performance is verified at various load currents.

In chapter 4, a flying capacitor-based multi-phase three-level buck converter envelope tracking power supply is proposed to track 4G LTE envelope signal of bandwidth up to 20 MHz. Power loss models are developed to optimize the converter design for efficiency. Zero voltage switching (ZVS) and a current self-balancing mechanism are proposed. Simulation results are provided to verify the proposed concept

A cascaded switching capacitor-based multi-phase three-level buck converter is proposed in chapter 5 as a drain supply modulator to eliminate the need for a capacitor voltage control mechanism. EPC8000 family eGaN MOSFETS are used to enable the multi – MHz high switching frequency of operation of the converter. A fourth-order low pass LC-filter is designed to enable the zero-voltage switching and also to track the

envelope signals of bandwidth up to 20 MHz. Simulation and experimental results are provided as proof of concept.

In chapter 6, a single-stage three-level interleaved buck converter for improved point-of-load performance is proposed. Zero voltage switching (ZVS) and a current self-balancing mechanism are proposed to eliminate the multiple current control loops. Variable switching frequency operation is introduced to improve the efficiency under light load conditions. A detailed converter loss modeling and Simulation results at output voltages of 3.3 V and 5 V are presented. The current self-balancing and voltage regulation are verified under dynamic load changes.

2. FLYING CAPACITOR BASED THREE-LEVEL BUCK CONVERTER FOR ENVELOPE TRACKING

2.1 Introduction

High frequency-switching converter-based envelope tracking DC power supplies are widely adopted in modern 4G/5G communication base stations to improve the efficiency of radio frequency power amplifiers. Flying capacitor three-level (FCTL) buck converters supplied with single input DC voltage source, have been utilized in various applications due to their high-power density, reduced switching losses, and reduced output ripple voltage compared to the conventional buck converters. Flying capacitor-based multi-level buck converters enable the usage of low voltage gallium nitride (GaN) field-effect transistors (FETs) and extended their operation to multi-MHz switching frequency in telecommunication and data center applications.

In this chapter, an FCTL buck converter supplied with a single input DC source is investigated as a potential candidate for higher voltage ET applications (such as in 4G/5G communication and military RADAR. EPC8004 [64], 40 V eGaN FETS characterized with less switching loss, are used as power stage devices. A fourth-order Legendre-Papoulis filter is designed to track the envelope signal of wide bandwidth at a nominal voltage ripple. The proposed concept has the following advantages:

- Reduced device-level voltage stress leads to lower switching loss while operating at the high switching frequency,

- Reduced output ripple and output filter size lead to improved bandwidth tracking capability,
- Reduces device-level switching frequency for the same open-loop bandwidth requirement.

This chapter is organized as follows. The operation and design of the converter are explained in section 2.2. The selection and design of the fourth-order low pass filter are discussed in section 2.3. Simulation results are presented in section 2.4 and section 2.5 describes the PCB layout and experimental results of the hardware prototype.

2.2 Flying Capacitor Three-Level Buck Converter

The power stage architecture of a three-level buck converter along with a fourth-order output filter for ET application is shown in Figure 2-1 [29]. The RFPA behavior is modeled as a resistive load R_L [65] since it is equivalent to a constant resistor when supplied with an ET power supply. EPC8004 40 V GaN switches are used as power stage devices. The input voltage can be varied up to 48 V and the output voltage varies up to 42 V according to the reference envelope signal.

2.2.1 Operation of Three-Level DC-DC Converter

The power stage operation of the three-level converter is described in this section. The converter consists of four switches named S_1, S_2, S_3, and S_4 respectively. For better efficiency of the converter, especially at the high switching frequency, all the switches are realized by eGaN FETs. The two bottom devices S_3 and S_4 operate in

synchronous rectification mode. Therefore, the converter always operates in continuous conduction. The gate pulses to the top two devices, S_1 and S_2 have the same duty cycle 'D' but phase-shifted by 180^o. The gate signals of switch pairs S_1, S_4 and S_2, S_3 are complementary, as shown in Figure 2-2.

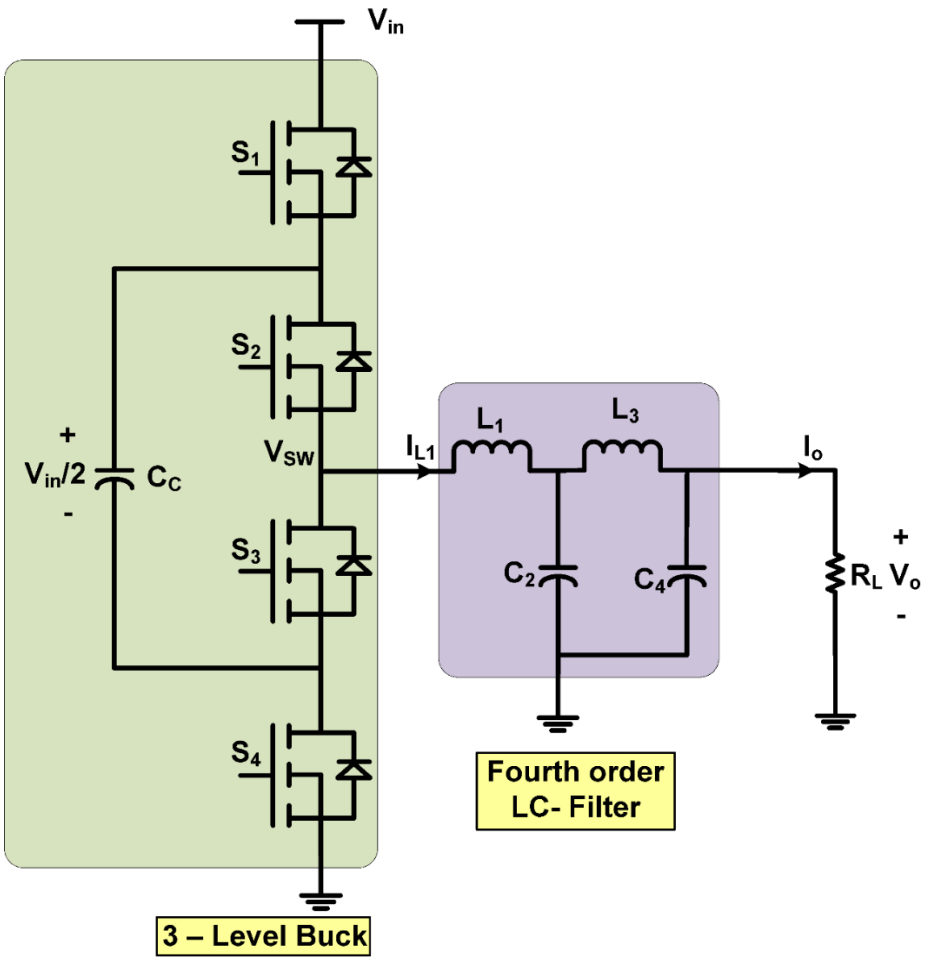
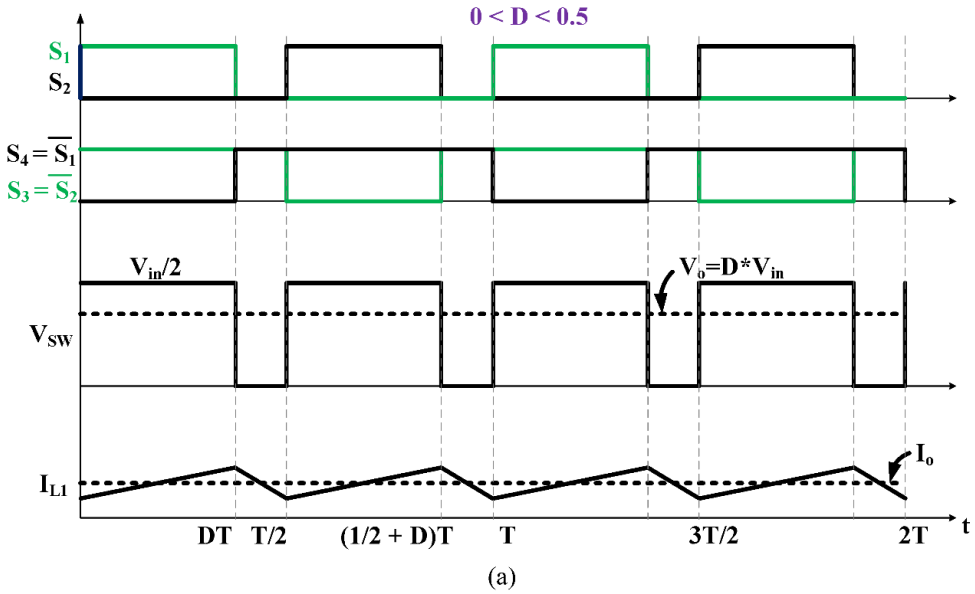
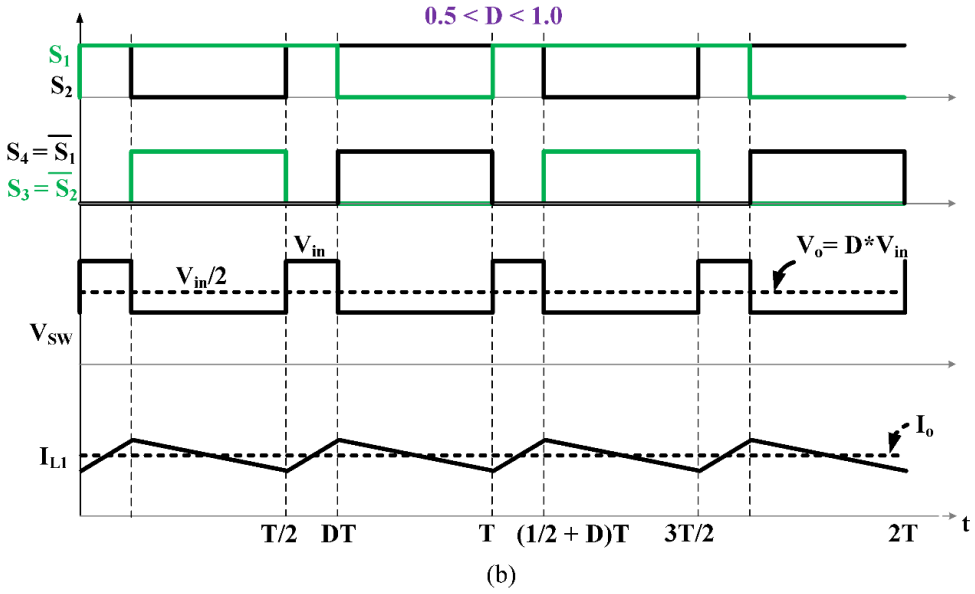


Figure 2-1: Flying capacitor-based three-level buck converter with fourth-order LC low-pass output filter.



(a)



(b)

Figure 2-2: Model switching waveforms of the FCTL buck converter. (a) $0 < D < 0.5$. (b) $0.5 < D < 1.0$.

For the duty cycle is in the range of $0 < D < 0.5$, the switch node voltage switches between 0 and $V_{in}/2$ whereas for a duty cycle range of $0.5 < D < 1.0$, switch

node switches between $V_{in}/2$ and V_{in}. There are six different operating modes of the converter over the duty cycle range $0 < D < 1.0$. Figure 2-3 and Figure 2-4 show the circuit operation along with the devices in conduction during the six operating modes.

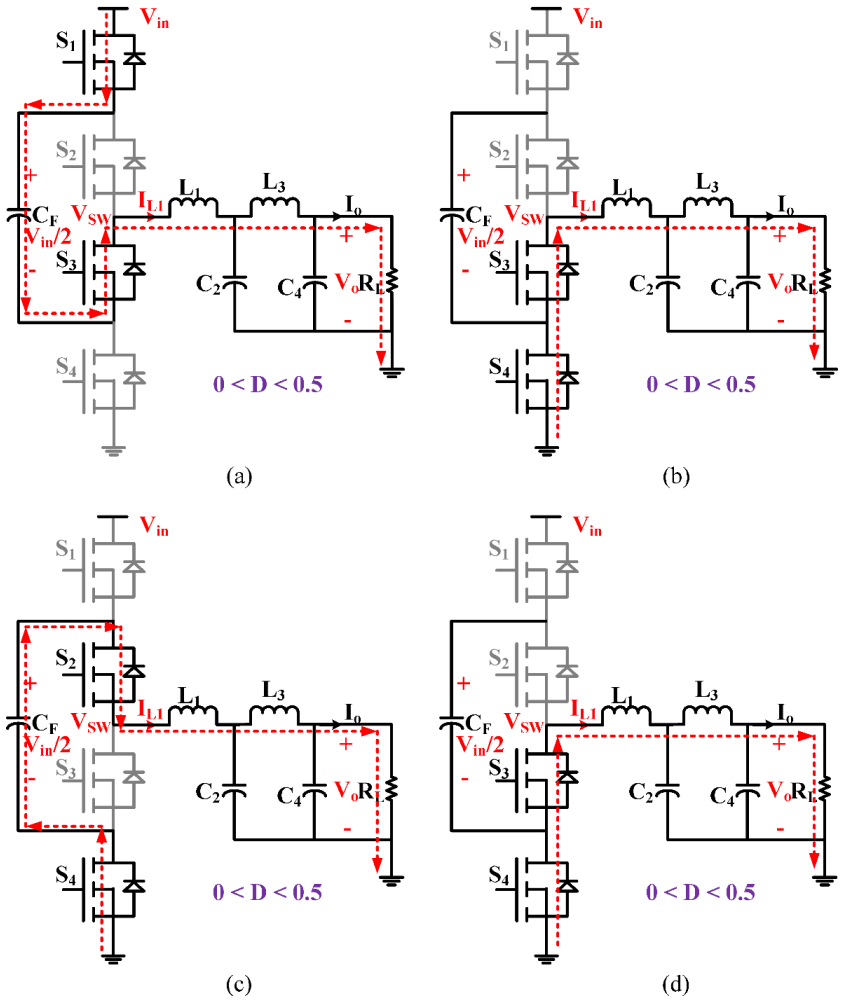


Figure 2-3: Different modes of operation of the FCTL buck converter for the duty cycle range $0 < D < 0.5$. (a) Flying capacitor charging mode. (b) Inductor current freewheeling mode. (c) Flying capacitor discharging mode. (d) Inductor current freewheeling mode.

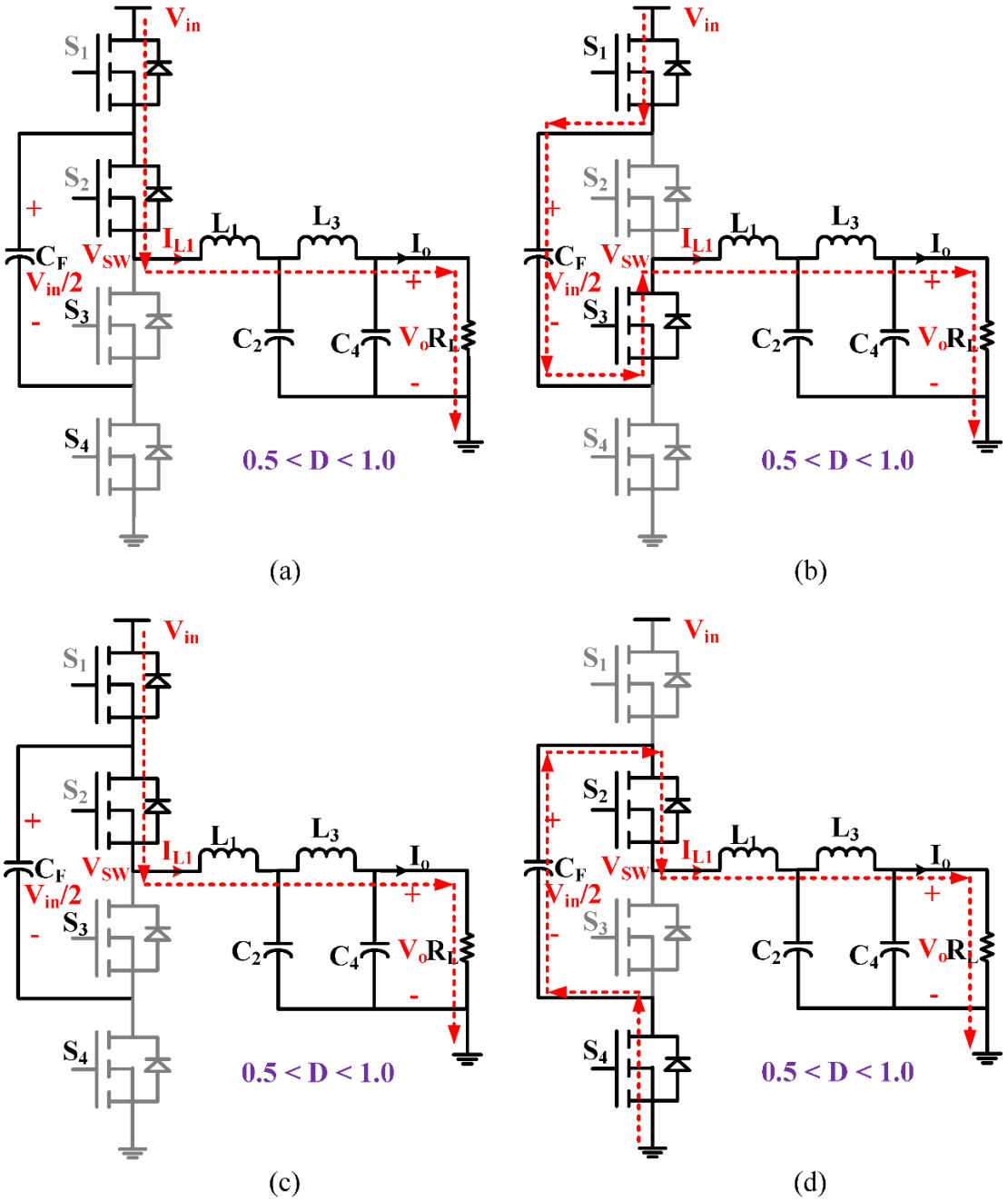


Figure 2-4: Different modes of operation of the FCTL buck converter for the duty cycle range $0.5 < D < 1.0$. (a) Inductor charges through the input voltage. (b) Flying capacitor charging -Inductor discharging. (c) Inductor charges through the input voltage. (d) Flying capacitor discharging and inductor discharging.

The frequency of the switch node voltage is twice the device switching frequency. This phenomenon reduces the size of the filter requirements and increases the open-loop bandwidth of the converter as the output voltage varies dynamically at wider bandwidth in ET applications. The voltage stress on the devices is also reduced to half of the input voltage. This in turn reduces the switching losses and improves the overall efficiency of the converter for high voltage ET applications. To properly switch the converter at three voltage levels of 0, $V_{in}/2$ and V_{in}, the flying capacitor voltage always needs to be balanced at $V_{in}/2$.

2.2.2 Flying Capacitor Voltage Balancing Scheme

The block diagram of the capacitor voltage control scheme is shown in Figure 2-5. The capacitor voltage is sensed by sampling the switch node voltage with reference to the ground at the instants when the switch node voltage is equal to the flying capacitor voltage. A detailed control scheme can be found in [29]. The gate pulses to S_1 is obtained directly from the duty cycle d by using digital PWM developed in FPGA. And the gate pulses to S_2 are obtained by adding a gain limited value of Δd to duty cycle as a correction to regulate the flying capacitor voltage at half of the input voltage, $V_{in}/2$.

2.2.3 Device Selection and loss comparison

The extraordinary electron mobility and low $R_{DS(on)}$ of the GaN devices enable the realization of converters with high switching frequency and better efficiency.

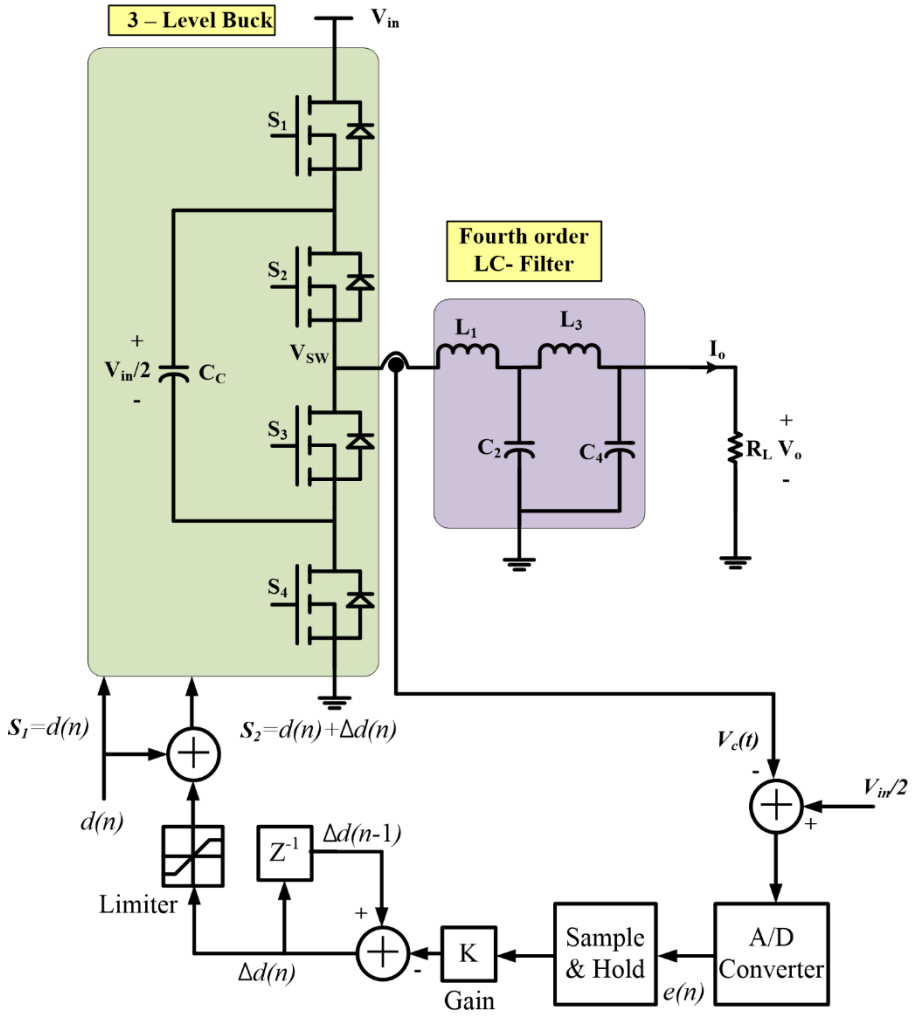


Figure 2-5: FCTL buck converter with a control scheme to regulate the flying capacitor voltage at half the input voltage.

EPC8004 eGaN FET has ultra-low $R_{DS(on)}$ of 110 $m\Omega$, a total gate charge of 370 pC, zero reverse recovery charge, and an ultra-small footprint of 2.1 mm × 0.85 mm [64]. These exceptional switching characteristics and conduction losses make it a suitable option for the selected three-level converter topology.

Both FCTL and two-phase-two-level buck converters offer similar equivalent switch node frequency for the same device switching frequency and consist of an equal number of GaN FETs in their power stages.

Hence, Figure 2-6 shows the model-based efficiency [66] comparison of FCTL and two-phase two-level buck converters over a wide range of duty cycles and switching frequency with an input voltage of 30 V and the load resistance of 12 Ω. ZVS filter inductor value is used in the efficiency model of the two-level converter to account for current balancing in the phases along with ZVS turn-on of top side FETs [55].

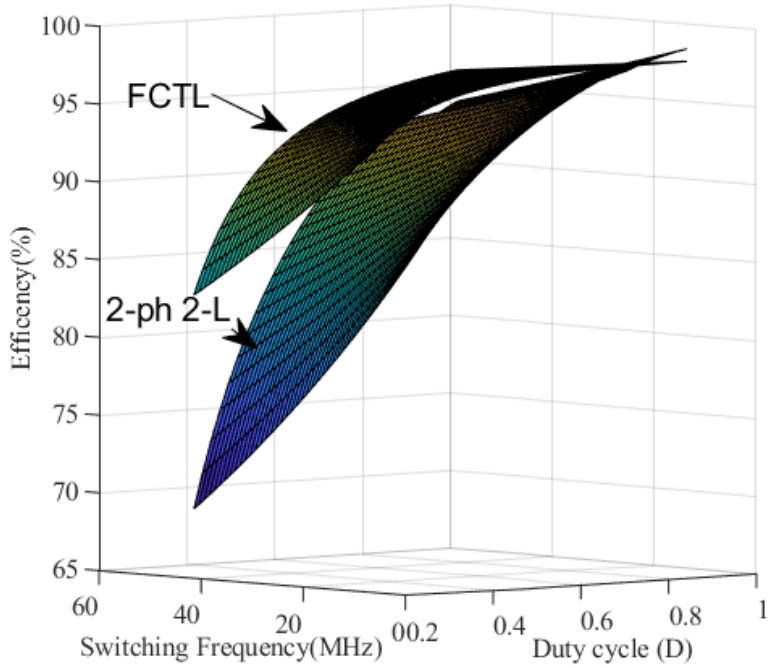


Figure 2-6: Efficiency comparison of FCTL buck and two-phase conventional two-level buck converter. FCTL buck converter exhibits better efficiency over a wide range of duty cycles and switching frequency.

The datasheet parameters of EPC8004 GaN FET are considered in this loss model. From Figure 2-6, the FCTL buck offers slightly better efficiency over a wide

operating range, which is primarily due to the reduced voltage stress across the power device. Texas Instruments' LMG1210 gate driver [54] with adjustable dead time and switching frequency capability of up to 50 MHz is used to drive the eGaN FETs. A novel gate driving strategy is proposed and a detailed analysis is presented in Chapter-3.

2.2.4 Envelope Signal

For this work, a reference tracking envelope was selected from [54]. It is characterized by

$$V_{ref}(t) = 0.5 + 0.1\sin(\omega_{BW}t) + .167\ \sin(0.6\,\omega_{BW}t) + 0.3\ \sin(0.2\,\omega_{BW}t). \quad (2.1)$$

The equation (2.1) is comprised of fundamental, third, and fifth harmonics. The bandwidth (BW) of the envelope signal is denoted by ω_{BW} and is dictated by the highest tracked frequency—in this case, the 5th harmonic. For accurate tracking of the envelope signal, a minimum switch node voltage frequency of five times the bandwidth ω_{BW} is recommended.

2.3 **Fourth-Order Output Filter Design**

In the case of ET RF transmitter systems, the BW of the envelope signal ranges up to several tens of MHz. To track high-BW envelopes, the open-loop bandwidth (i.e., responsivity) of the switching converter must be high as well. This can be achieved either by increasing the total effective switching frequency or reducing the ratio of switching frequency to bandwidth. However, these methods may increase voltage

distortion and reduce converter efficiency. Therefore, the ET power supply's low pass filter (LPF) must track the wide bandwidth envelope while maintaining high rejection of the switching frequency oscillations and associated harmonics. Additionally, the efficiency of the converter needs to be maintained with a nominal output voltage ripple. Figure 2-7 illustrates how the three-level buck converter has half the output ripple voltage when compared with its equivalent counterpart, the two-phase two-level buck converter. In other words, the size of the LPF components of a three-level buck can be reduced for the same output voltage ripple. This is because the switch node voltage frequency of an FCTL buck is twice the device switching frequency.

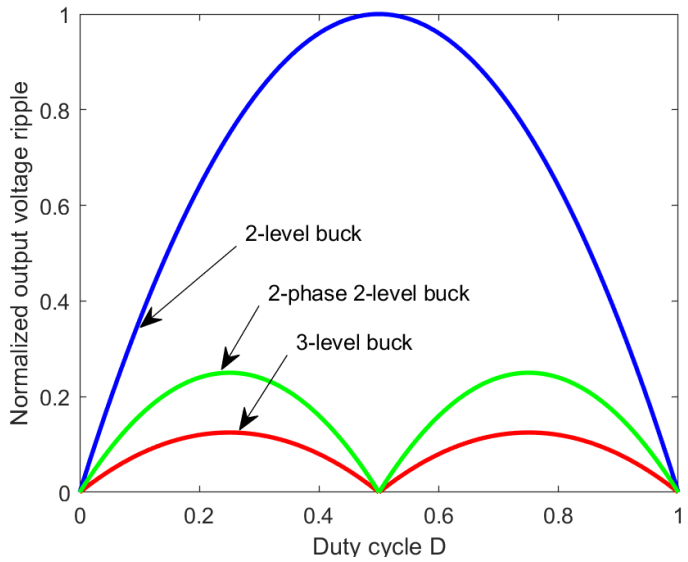


Figure 2-7: Comparison of conventional and FCTL buck converters' voltage ripple variation with respect to the duty cycle for the same filter component values.

There are many types of LPFs available, but some are not suitable for ET applications. For example, a Cauer filter cannot attenuate the ripple over a wide range

of frequencies, whereas a Chebyshev filter exhibits variable gain in the passband. However, Butterworth, Bessel-Thomson, and Legendre-Papoulis are three appropriate filter types for ET applications. The merits and demerits of these filters are characterized in terms of stopband attenuation, group delay, and quadratic error [54]. A fourth-order Legendre-Papoulis filter is a better option for band-limited ET applications as it has better performance characteristics. Also, the higher-order filters have better stopband attenuation. The filter design for this work is carried out based on [67] and the normalized filter element values for various filter orders with the normalized angular cutoff frequency $\omega_c = 1rad/s$ and R_L = 1 Ω are given in Table. I.

Table 2-1: Normalized elements of Legendre-Papoulis filter.

Filter order	$\mathbf{l_1}$	$\mathbf{c_2}$	$\mathbf{l_3}$	$\mathbf{c_4}$	$\mathbf{l_5}$	$\mathbf{c_6}$
1st	1	-	-	-	-	-
2nd	1.4142	0.7071	-	-	-	-
3rd	1.5909	1.4270	0.7629	-	-	-
4th	1.6120	1.6616	1.4292	0.6399	-	-
5th	1.6372	1.7509	1.7358	1.3945	0.6445	-
6th	1.6348	1.8088	1.8233	1.6795	1.3486	0.5793

From Table I, the actual filter parameters L_x, C_x (where $x = 1,2, \ldots 6$) for a load resistance of R_L and the angular cutoff frequency of ω_c are calculated from

$$L_x = \frac{l_x R_L}{\omega_c} \tag{2.2}$$

and

$$C_x = \frac{c_x R_L}{\omega_c}. \tag{2.3}$$

The filter values of a fourth-order Legendre-Papoulis filter with a total effective switching frequency of 40 MHz and an angular cutoff frequency of 1.821 times the envelope BW are calculated and listed in Table II. A fourth-order ZVS filter is also designed by following the procedure in[68]. The filter values of a fourth-order ZVS and Legendre-Papoulis filter types for a total effective switching frequency of 40 MHz and an envelope bandwidth of 8 MHz are calculated and listed in Table II. The bode magnitude plots ZVS and Legendre filter types are shown in Figure 2-8, which have a similar passband response, and switch node frequency attenuation of 50 dB and 40 dB respectively.

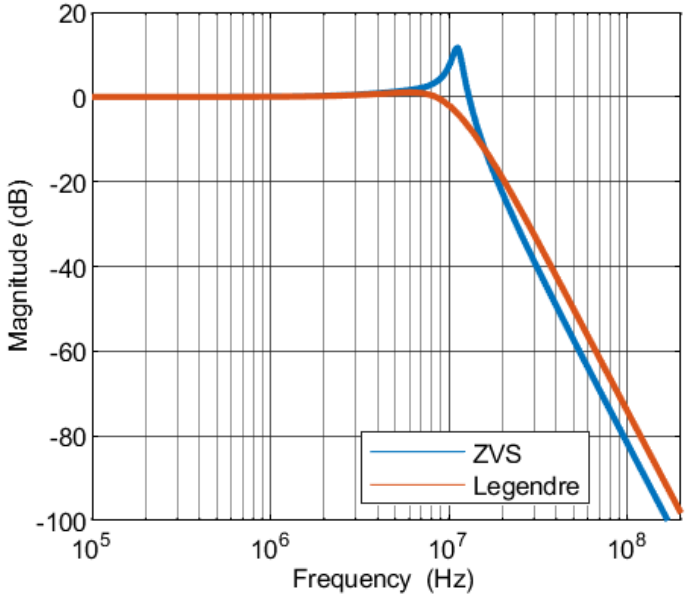


Figure 2-8: ZVS and Legendre fourth-order type filters' bode magnitude plots for 8MHz bandwidth.

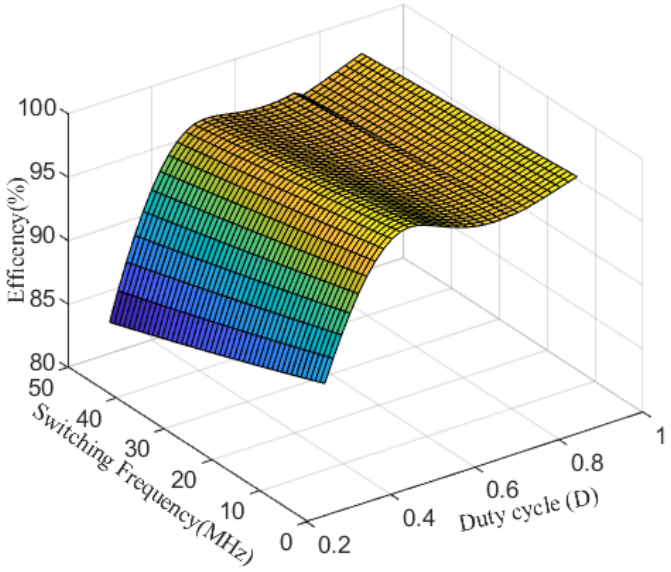
Table 2-2: Fourth-order filter parameters to track 8 MHz bandwidth signal.

Bandwidth	**R_L**	**L_1**	**C_2**	**L_3**	**C_4**
8 MHz	12 Ω	208 nH	1.48 nF	184 nH	.57 nF

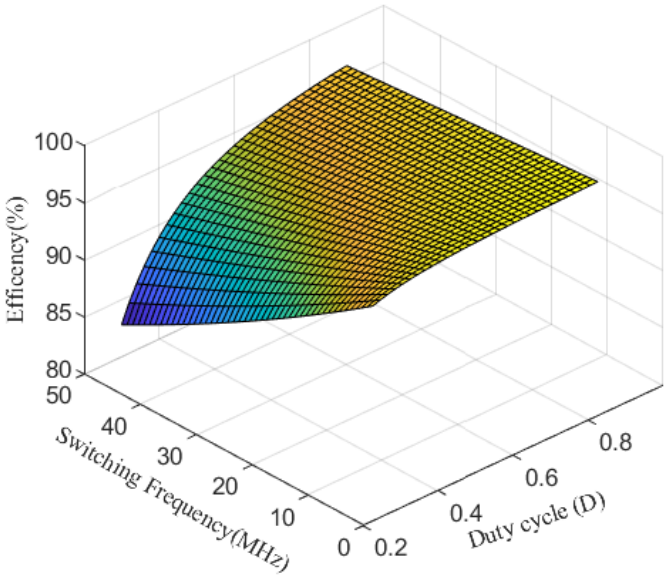
Figure 2-9 shows the model predicted efficiency plots of the FCTL buck converter at the various switching frequency and duty cycle values for ZVS and Legendre output filter types. For the input voltage $V_{in} = 28\ V$ and load resistance of 12 Ω, the Legendre filter type have slightly better efficiency at 20 MHz switching frequency. Therefore Legendre filter parameters are used in the experimental prototype. This is because the high RMS current of the ZVS inductor yields more conduction loss than the reduction in switching loss. A more detailed loss modeling is provided in Chapter 6.

2.4 **Simulation Results**

An FCTL DC-DC converter was simulated in LTSpice using SPICE models of EPC8004 to verify the switching performance of the converter. Figure 2-10 and Figure 2-11 show the simulation waveforms of voltage across the switches, inductor current, and switch node voltages at the duty cycle $D = 0.4$ and $D = 0.7$ respectively. By properly balancing the capacitor voltage at 24 V, the voltage stress across the devices is limited to 24 V when supplied by a 48 V DC source. When the FETs are switched at 20 MHz, the converter realizes a total effective switching frequency of 40 MHz. The maximum switching frequency is limited by the gate driver, not by the switches.



(a)



(b)

Figure 2-9: Efficiency plots of FCTL buck converter at the various switching frequency and duty cycle with output filter as (a) ZVS and (b) Legendre at V_{in} =28 V.

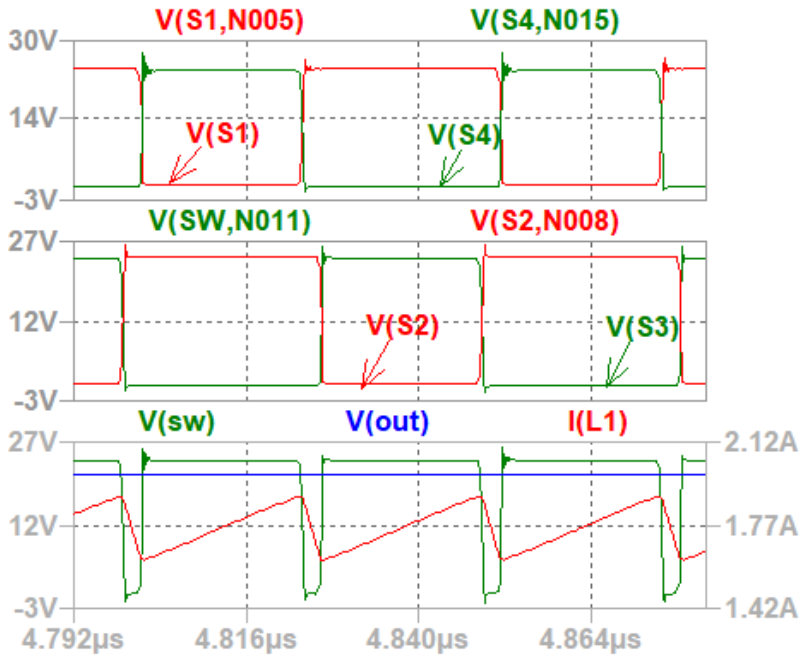


Figure 2-10: SPICE Simulated waveforms of the FCTL converter at duty cycles D =0.4 with EPC8004 eGaN FET models and V_{in} = 48 V.

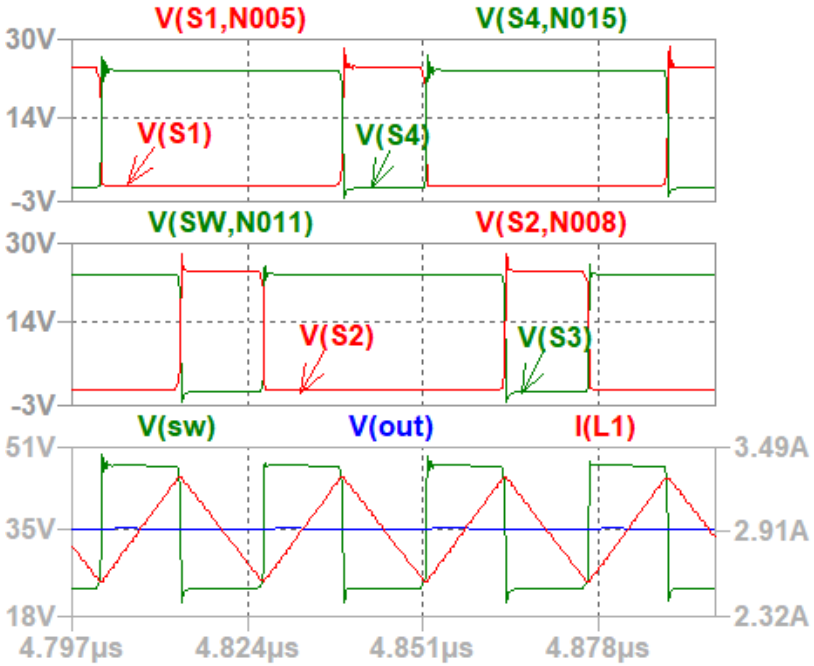


Figure 2-11: SPICE Simulated waveforms of FCTL converter at duty cycles D = 0.7 with EPC8004 eGaN FET models and V_{in} = 48 V.

Figure 2-12 and Figure 2-13 show the simulation results of the three-level converter with a fourth-order Legendre-Papoulis filter tracking an 8 MHz envelope signal when supplied by 48 V and 30 V DC voltage sources, respectively. The switch node V_{sw} switches between voltage levels of 0 and $V_{in}/2$ or $V_{in}/2$ and V_{in} at a frequency of 40 MHz, based upon the reference envelope signal.

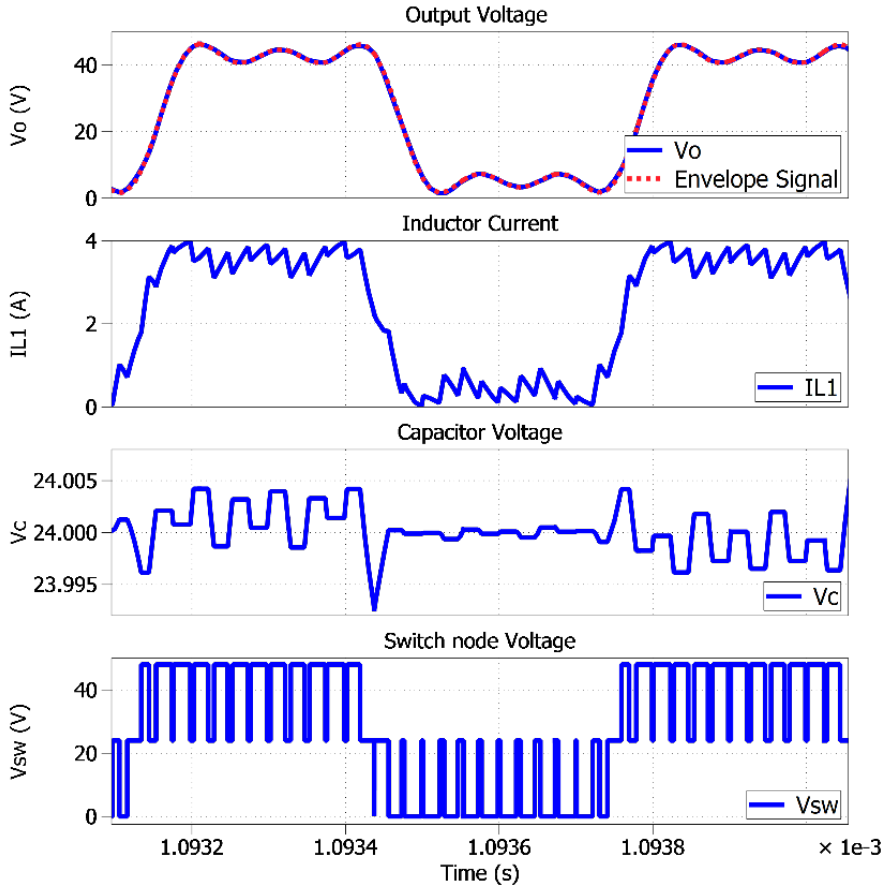


Figure 2-12: Simulation results obtained with three-level buck converter tracking 8 MHz BW envelope signal 48 V DC input voltage.

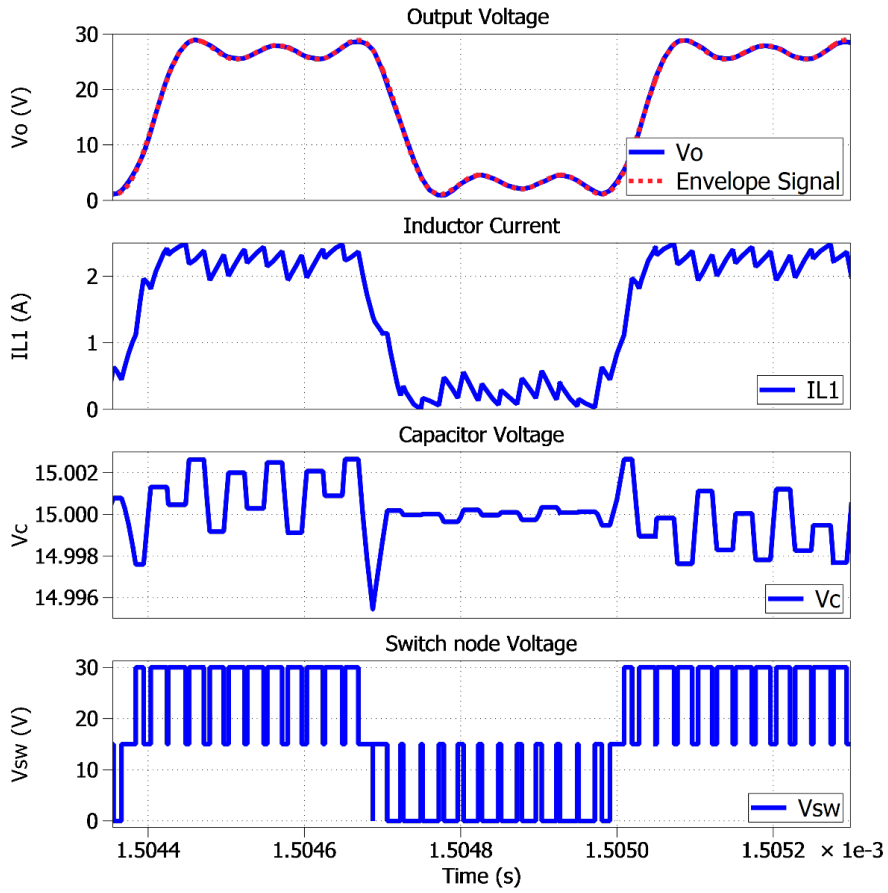


Figure 2-13: Simulation results obtained with three-level buck converter tracking 8 MHz BW envelope signal with 30 V DC input voltage.

2.5 **Experimental Prototype and Results**

A single-phase prototype of the FCTL buck converter was built using two LMG1210 gate driver ICs and four EPC8004 GaN MOSFETs as shown in Figure 2-14. The major components used in the prototype are listed in Table 2-3. The PCB design was iterated multiple times to minimize the parasitic gate drive loop inductance and power loop inductance. Figure 2-15 shows the earlier prototype versions developed in the process of the optimal layout. In the prototype shown in Figure 2-14, the GaN FETS

are placed on the top and bottom side of the PCB to minimize the parasitic loop inductance.

Table 2-3: List of main components used in FCTL buck converter.

Component	Part number	Ratings
GaN FETs	EPC8004	40 V, 110 mΩ
Gate driver ICs	TI's LMG1210	200 V, Half-bridge
Bootstrap capacitors	TDK, YFF18PC0J474MT0H0N	0.47μF, 6.3 V, Feed Through Capacitor
Bootstrap diodes	NXP Semiconductors, BAT46WJ,115	100V, 250MA, Schottky
Inductors	Coil craft RF air core, 2222SQ-181, 2222SQ-221	180 nH, 220 nH
Flying capacitor	Multi-layer ceramic, 0603, 0402	2.2 uF, 1 uF, 4.7 uF, 0.1 uF
Signal isolator IC	ISO721MD	---
High-speed comparator	Texas Instruments LMH7322	160 ps rise & fall time, 700 ps delay time
FPGA	Intel Stratix V GX transceiver evaluation kit	12.5 Gbps

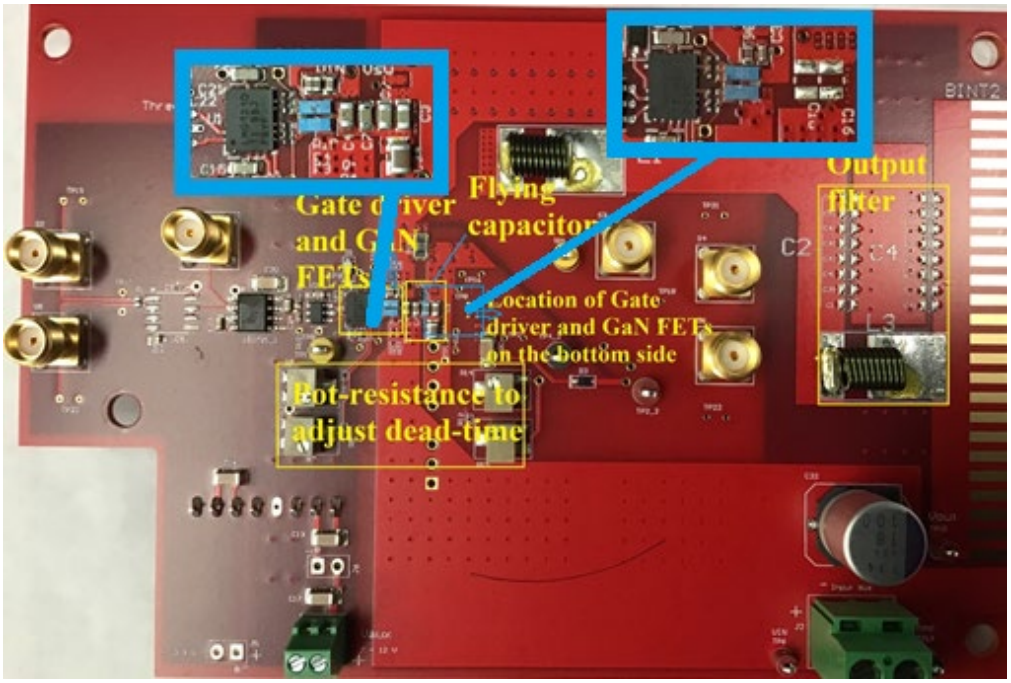


Figure 2-14: Experimental prototype of the FCTL buck converter.

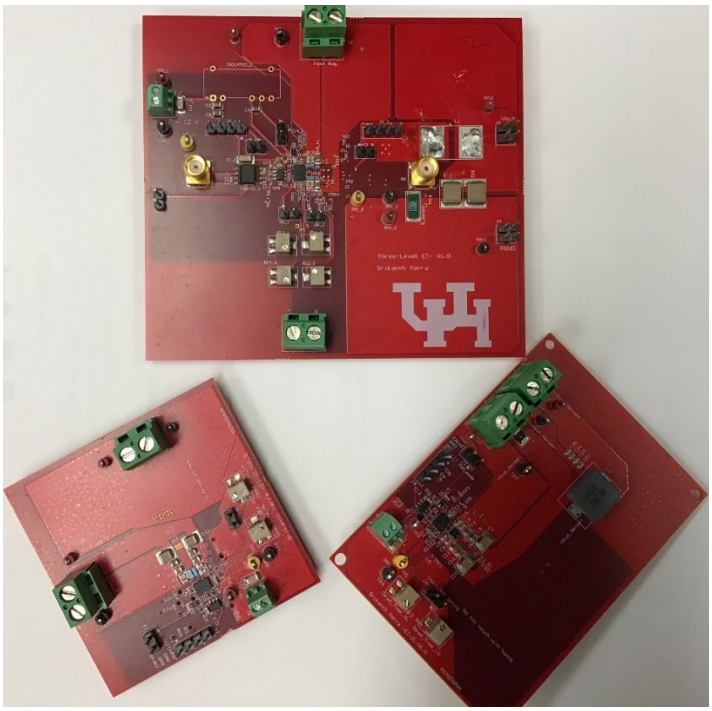


Figure 2-15: Prototype versions developed in the process of optimal layout and design.

A primary DC source and an auxiliary DC power source are used to supply the input power and gate drive power to the prototype. The two gate driver ICs are also, placed at optimal locations and close to the GaN devices. The gate pulse trace and the return trace are routed in the adjacent layers to minimize the gate loop inductance. Also, the power loop parasitic inductances are minimized with the optimal routing of power traces. MSO56 2 GHz bandwidth scope and TDP1000, 1 GHz bandwidth probes are used to measure the switching performance of the converter. High-resolution PWM signals are generated using the Intel Stratix V GX transceiver evaluation kit, which has data rates of up to 12.5 Gbps.

The gate pulses to S_1 is obtained directly from the duty cycle, d, by using digital PWM developed in FPGA. And the gate pulses to S_2 are obtained by adding a gain limited value of Δd to duty cycle as a correction to regulate the flying capacitor voltage at half of the input voltage, $V_{in}/2$ as given in [30]. The flying capacitor has been chosen with a sufficiently large value to tightly regulate the voltage with a nominal ripple. LMH7322 high-speed comparator IC is used to sense the flying capacitor voltage at a high sampling rate. The analog sensed voltage is converted to low voltage differential signals (LVDS) and fed to LVDS receivers of the FPGA evaluation kit.

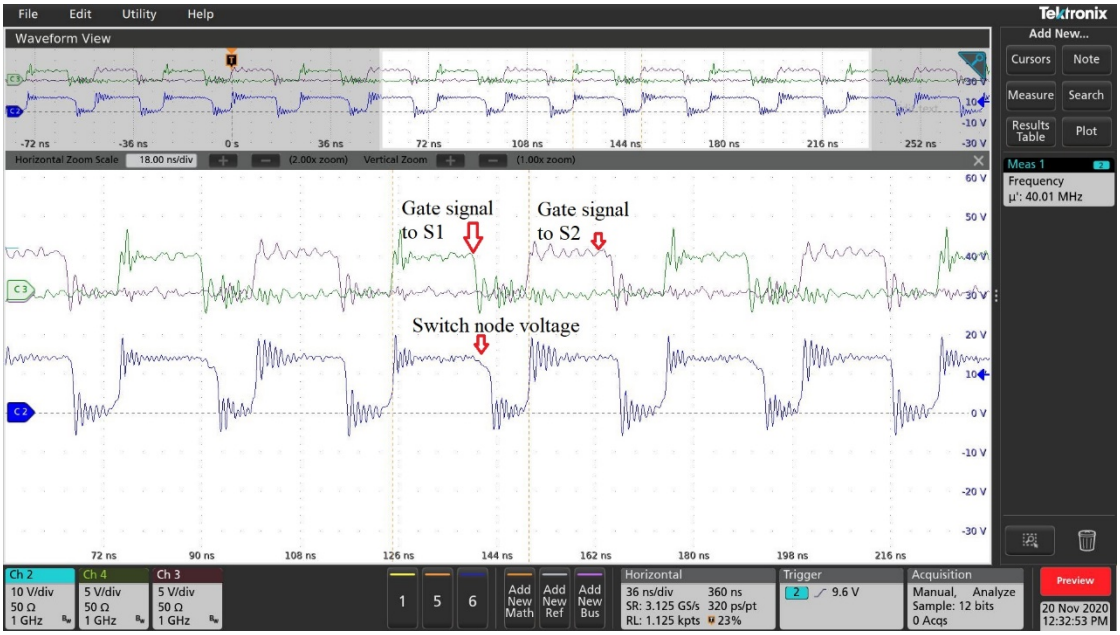


Figure 2-16: Experimental results of the FCTL converter at the duty cycle of 0.3 with 30 V input DC supply. The gate pulses to the top side devices S_1 and S_2 are at 20 MHz and interleaved by an angle of 180°. The switch node voltage switching between 0 V and 15 V with twice the device switching frequency at 40 MHz.

The experimental switch node voltage waveform of the converter at 20 MHz device switching frequency is shown in Figure 2-16 and Figure 2-17. The test points to measure the switch node voltage along with the voltage probe terminals provides minimal ringing in the measured voltage waveform.

This is primarily due to the resonant network formed by the parasitic loop inductance of the test point traces and the probe capacitance ($\sim 3.9\ pF$) as shown in Figure 2-18. The switch node voltage and output voltage of the converter tracking 8 MHz bandwidth envelope signal are shown in Figure 2-19.

Figure 2-17: Experimental results of the FCTL converter at the duty cycle of 0.75 with 30 V input DC supply. The gate pulses to the top side devices are at 20 MHz and interleaved by an angle of 180°. The switch node voltage switching between 15 V and 30 V with twice the device switching frequency at 40 MHz.

The input DC voltage applied to the converter is 28 V, and the output voltage varies from 4 V to 24 V. For the gate pulse switching frequency of 20 MHz, the switch node voltage switches between either 0 V and 14 V or 14 V and 28 V at 40 MHz.

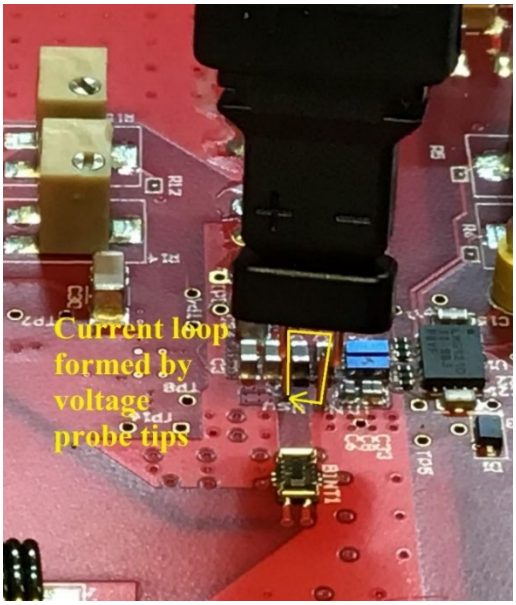
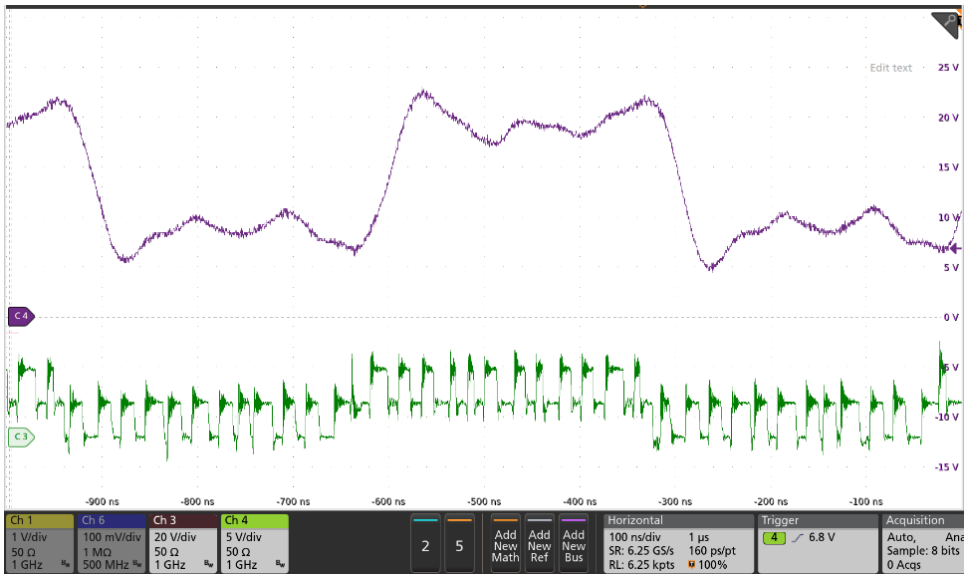


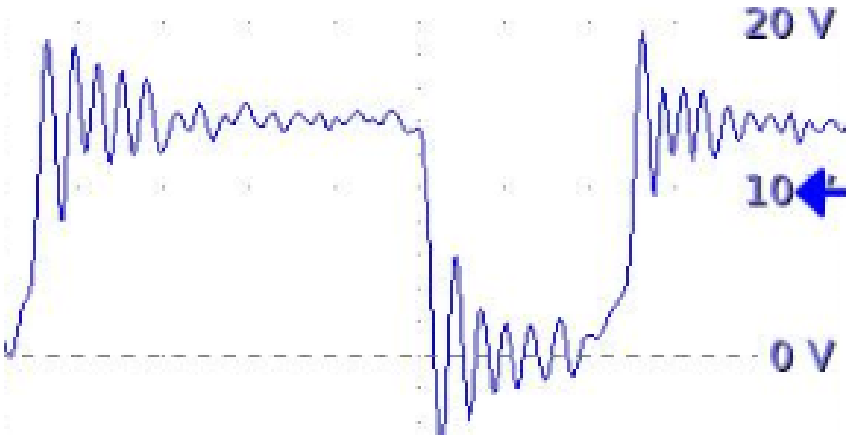
Figure 2-18: Loop inductance formed by the voltage probe tips.

The efficiency of the FCTL buck converter is measured at three different duty cycles of 0.25, 0.5, and 0.75, and over the range of output power. The input DC voltage is 28 V and the switching frequency is 20 MHz. The measured efficiency is plotted in Figure 2-20 along with the model predicted efficiency. The predicted and measured efficiencies follow very closely. The very slight deviation can be attributed to the path losses, ohmic drops due to increased R_{dson} at higher temperature and due to the auxiliary circuits. The maximum measured efficiency is 96 % and it is over 90 % for most of the operating range of 0 to 25 W. The total average efficiency of the converter

while dynamically tracking the 8 MHz bandwidth envelope signal is 93 % with an average output power of 22 W.



(a)



(b)

Figure 2-19: (a). Experimental results. Ch3: Switch node voltage at 40 MHz (scale: 20 V/div). Ch4: Output voltage (scale: 5 V/div.) while tracking 8 MHz bandwidth envelope signal (Time scale: 100 ns/div). Probe bandwidth set to 1 GHz. (b). Close up of switch node voltage (Time scale: 3.6 ns/div).

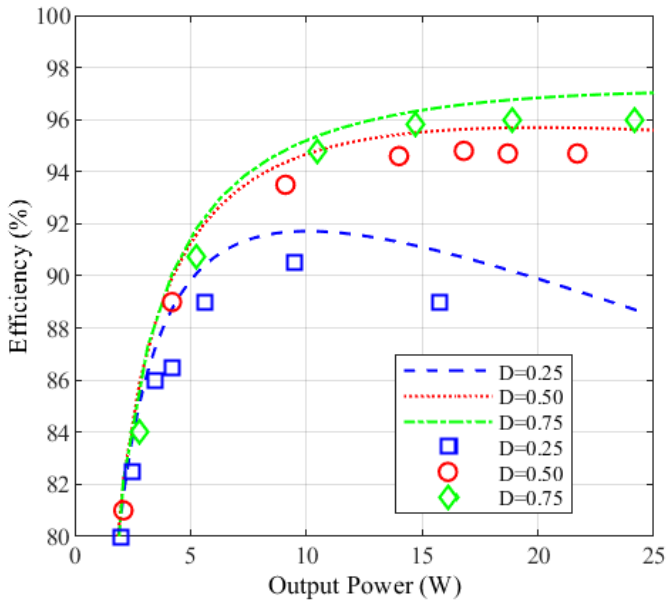


Figure 2-20: Efficiency of the four-phase ET prototype: V_in= 28 V, f_s= 20 MHz, measured (markers) and predicted (dashed lines).

2.6 **Summary**

A three-level DC-DC converter for high voltage ET application was studied in this chapter. The design was developed based on an analytical model and Legendre filter values were used for better efficiency of the converter. EPC8004 ultra-fast, high-efficiency GaN switches were used as power stage devices. The designed fourth-order Legendre-Papoulis filter allowed the converter to track envelope signals of BW up to 8 MHz with proper switching frequency attenuation. The selected converter has the benefits of reduced device voltage stress, reduced filter component size, and halved switching frequency requirement for the same BW when compared with conventional two-level buck converter without the need for multiple voltage sources. An experimental prototype was built, and the results of switch node voltage and output

voltage tracking an 8 MHz bandwidth envelope signal are provided as proof of concept. The proposed design is scalable with multiple three-level converters that can be interleaved to track the envelope signals of higher BWs and PAPR.

3. SIMPLIFIED GATE DRIVING STRATEGY AND LAYOUT CONSIDERATIONS FOR HIGH-FREQUENCY THREE-LEVEL BUCK CONVERTERS

3.1 Introduction

Flying capacitor (FC) based multi-level buck converters enable the usage of low voltage semiconductor devices in numerous applications as they reduce the voltage stress across the devices. The utilization of gallium nitride (GaN) FETs on FCTL extended its operation to multi-MHz switching frequency in telecommunication and data center applications. However, the gate driving circuit of a multi-level buck converter requires a dedicated DC power supply, a gate driver IC, and a signal isolator IC for each semiconductor device, which reduces the power density and increases the complexity. In this chapter, a simple gate driving strategy is proposed for FC-based multi-level buck converters. The proposed gate drive technique for the FCTL buck converter requires only two half-bridge gate driver ICs to drive the four GaN MOSFETs. A novel cascaded bootstrapping architecture with a single DC-DC converter is proposed to meet the DC power supply requirements of the half-bridge gate driver ICs. Moreover, the number of PWM input signals and isolator ICs is reduced to half. The initial prototype is built and tested up to 40 MHz PWM switching frequency. Experimental results are presented as a proof of concept.

3.2 Gate Driving of Multi-Level Converter

Applications such as data centers and telecommunication require a high bandwidth power supply. To meet the high bandwidth requirements, the converter switching frequency must be increased. Since most of the converter switches are floating, the power supply to the gate driver poses a substantial hardware challenge. Most of the previous works utilized multiple on-chip isolated DC-DC converters to drive the floating switches [69]–[72], which may be optimal for high power low switching frequency (several kHz to 1MHz) of operation. However, for low power and high frequency (up to several MHz) applications, the size of the isolated DC-DC converter can be several times larger than the GaN FET. Using multiple isolated DC-DC converters increases the size of the gate drive circuit and leads to overall power density reduction in the case of high-frequency design.

Bootstrap is the other widely used method to supply the high side gate driver of the two-level converter. Several gate drive techniques are derived based on this method [73], [74] to drive the floating switches of the multi-level converter. Various complex charge pumping methods that use low-dropout regulators (LDOs) and multiple diodes are proposed in [75], which may cause increased hardware complexity and reduce the power density of the converters - especially at high switching frequencies. A simpler cascaded synchronous bootstrapping is proposed in [76], [77] with cascaded bootstrap diodes and external synchronous GaN FETs. This method reduced the complexity, but

the gate voltages are not regulated and the bootstrap capacitor voltages are limited by the direction of the inductor current and voltage drop across the bootstrap diodes.

The previous methods either overcharge and/or under-charge the higher-level bootstrap capacitor due to the cascading bootstrap diode drops and high forward drops of the GaN body diodes. To overcome these problems, a cascaded synchronous bootstrapping is proposed in [74]. This method replaces the voltage regulators and cascaded bootstrap diodes with synchronous GaN FET that has a much lower voltage drop. But, this method uses an extra half-bridge gate driver for the floating switches of the FCTL converter.

To improve the power density and reduce the number of parts in the gate drive circuit, a simplified gate driving strategy for a high-frequency FCTL buck converter is proposed in this chapter. The proposed gate drive technique requires only two half-bridge gate driver ICs to drive the four GaN MOSFETs. A novel cascaded bootstrapping architecture with a single auxiliary DC power supply is proposed to meet the power supply requirements of the half-bridge gate driver ICs to drive the FCTL buck converter's floating switches. Moreover, the number of PWM input signals and isolator ICs is reduced to half. The initial prototype is built and tested up to 40 MHz pulse width modulation (PWM) switching frequency. Experimental results are presented as a proof of concept. The proposed gade drive technique has the following advantages:

- Reduced number of half-bridge gate driver ICs and part count,
- Independent input mode and PWM mode of the gate driving

- Adjustable dead time capability in the range of picoseconds and matched propagation delay time of ~14 ns, and
- High switching frequency operation up to 40 MHz.

The design, operating principle, and experimental results of the proposed gate drive strategy are explained in the later sections.

3.3 **Proposed Gate Driving Strategy**

The basic circuit diagram of the proposed gate driving strategy of an FCTL buck converter is shown in Figure 3-1. It consists of two half-bridge gate driver ICs (LMG1210) indexed as GD1 and GD2, which are driven by two 180° phase-shifted PWM signals PWM1, PWM2. The proposed gate driving technique uses LMG1210 half-bridge GaN FET driver IC, which is designed for ultra-high frequency applications such as RF envelope tracking [78]. The functional block diagram of the LMG1210 gate driver IC is shown in Figure 3-2. The advanced features of this gate driver IC make the proposed gate drive technique operable either in PWM mode or independent gate driving mode with onboard adjustable dead time capability. An optimal bootstrap diode can be selected to charge the high-side bootstrap capacitor due to its external placement to the IC. Finally, the internal LDO regulates the gate drive voltage at 5 V irrespective of the auxiliary supply voltage.

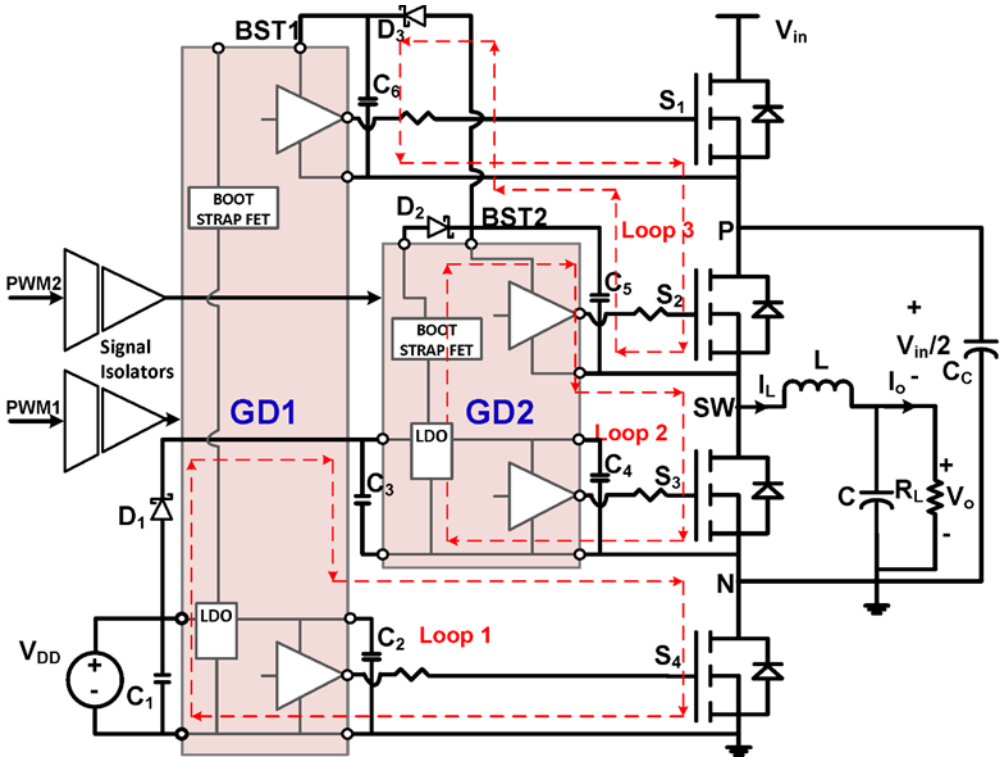


Figure 3-1: Basic Circuit diagram of the proposed gate driving strategy for the FCTL buck converter.

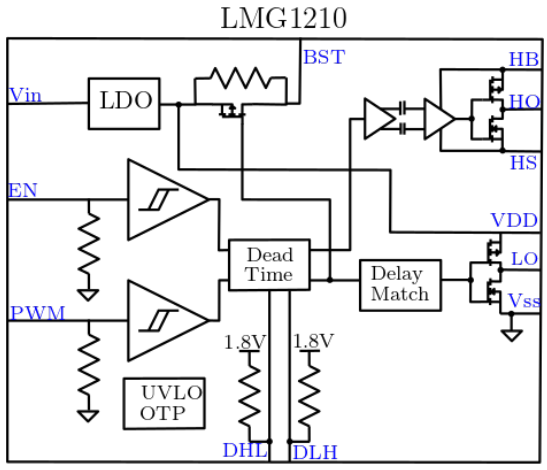


Figure 3-2: The functional block diagram of LMG1210 gate driver IC.

When driven with PWM signals, the two driver-ICs GD1 and GD2 generates two complementary gate pulse pairs to drive GaN switch pairs, S_1, S_4 and S_2, S_3

respectively. The external bootstrap diodes D_1, D_2 and D_3 give the flexibility to choose low- voltage drop Schottky diodes with lesser reverse recovery loss. The LMG1210 also has an internal low impedance FET that activates the bootstrap operation only when the low side switch is on. Hence, it avoids the overcharging of the high-side bootstrap capacitor during dead time. But, the 1 kΩ resistor connected across the internal bootstrap FET slowly charges the bootstrap capacitor even before the low side switch is on. Also, the deadtime can be controlled in the range of picoseconds by adjusting the two potentiometer resistances connected at pins DHL and DLH [78]. An optimal deadtime needs to be set without ample trade-off with the efficiency of the power converter. The proposed gate drive circuit is powered with the single auxiliary voltage source V_{DD} and cascaded bootstrap architecture.

3.4 Operating Principle

To study the influence of load current on gate voltage levels, the circuit operation and bootstrap charging is analyzed using four current loops (loop1, loop2, and loop3) and KVL.

Loop - 1: Consider the loop formed by the $V_{DD} - D_1 - C_3 - S_4$. The gate voltage of S_4 is regulated at 5V by the internal LDO of GD1. The capacitor C_3 is charged from V_{DD} through the diode D_1 when S_4 is on. By applying KVL in loop 1, the voltage across the capacitor C_3 is given by

$$V_{C3} = V_{DD} - V_{D1} + I_L R_{ds\_on}. \tag{3.1}$$

The forward voltage drop across the bootstrap diode D_1 is compensated by the voltage drop across the switch S_4. Either way, the voltage across the capacitor C_3, doesn't affect the gate voltage of S_3 as it is regulated by the LDO of the GD2. Therefore, the gate voltages of S_1 and S_2 are regulated at 5 V irrespective of output current.

Loop – 2: Consider the second loop formed by the GD2's LDO – bootstrap FET - $D_2 - C_5 - S_3$. The upper bootstrap capacitor C_5 charges from LDO of GD2 through the internal low impedance synchronous FET and external bootstrap diode D_2 when S_3 is on. Capacitor C_5 also charges slowly through the 1 kΩ resistor connected across the internal bootstrap FET even when S_3 is off. By applying KVL in loop 2, the voltage across the capacitor C_5 is given by

$$V_{C5} = V_{LDO} - V_{D2} + I_L R_{ds\_on}. \tag{3.2}$$

The forward voltage drop across the bootstrap diode D_2 is compensated by the voltage drop across the switch S_3, which varies with the inductor current I_L. Hence, the diode D_2 should be selected with a proper forward voltage drop if the voltage drop across the switch S_3 is high. The synchronous bootstrap FET turns on only when S_3 is on and prevents the overcharging of the capacitor C_5 during dead time.

Loop - 3: The gate voltage of the top switch S_1 is given by the voltage across the capacitor C_6. By applying KVL to the loop-3 formed by $C_5 - D_3 - C_6 - S_2$, the voltage across C_6 is given by

$$V_{C6} = V_{C5} - V_{D3} - I_L R_{ds\_on}. \tag{3.3}$$

The uppermost bootstrap capacitor C_6 charges through the bootstrap diode D_3 from the capacitor C_5 during S_2 is turned on. The forward voltage drop across the bootstrap diode D_3 and switch S_2 may under charge the bootstrap capacitor C_6 to a voltage below 5 V at higher load currents. The drop in gate voltage varies with the current through S_2. Therefore, the proposed gate drive circuit is tested at various load currents to make sure that the gate voltages stay within the operating limits of the EPC8004 GaN FET. The results are presented and discussed in the later section.

3.5 **Prototype and Experimental Results**

A prototype of the proposed concept using two LMG1210 gate driver ICs and four EPC8000 family GaN MOSFETs was built as shown in Figure 3-3. The two gate driver ICs are placed on top and bottom of the PCB and close to the GaN devices as shown in Figure 3-3 and Figure 3-4. GD1 is placed on the top side and GD2 is placed on the bottom side of the PCB. The gate pulse trace and the return trace are routed in the adjacent layers to minimize the gate loop inductance as well as the gate voltage ringing. ANSYS Q3D is used to optimize the layout for minimal power loop stray inductance.

The power plane routing is divided into two parallel paths to minimize the commutation loop inductances of the two loops as shown in Figure 3-5. Loop one is formed by the two complementary switches S_1, S_4 and the input DC link capacitor.

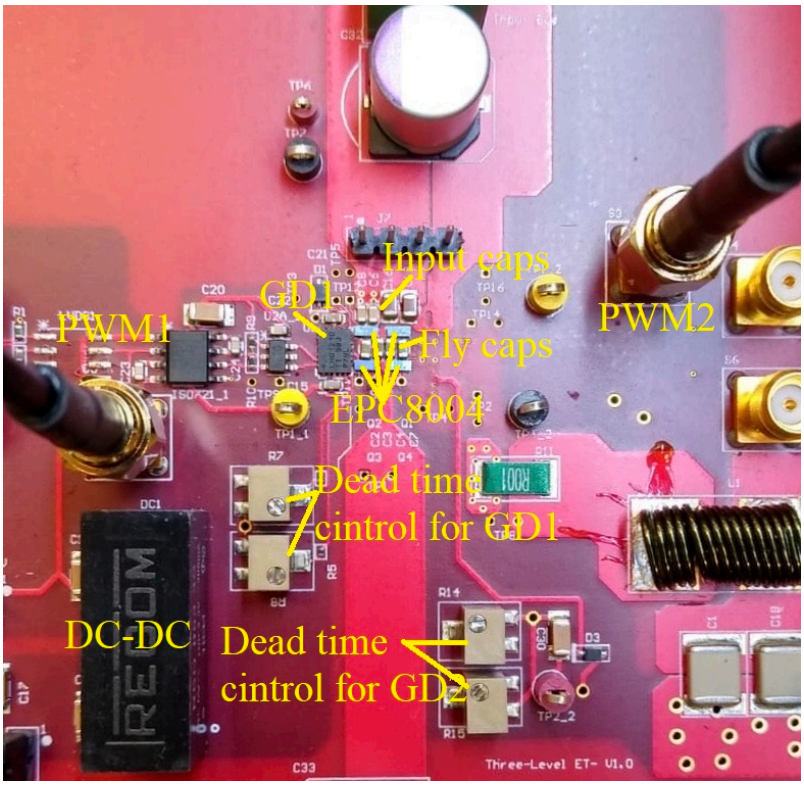


Figure 3-3: Topside of the prototype PCB to verify the proposed gate driving technique.

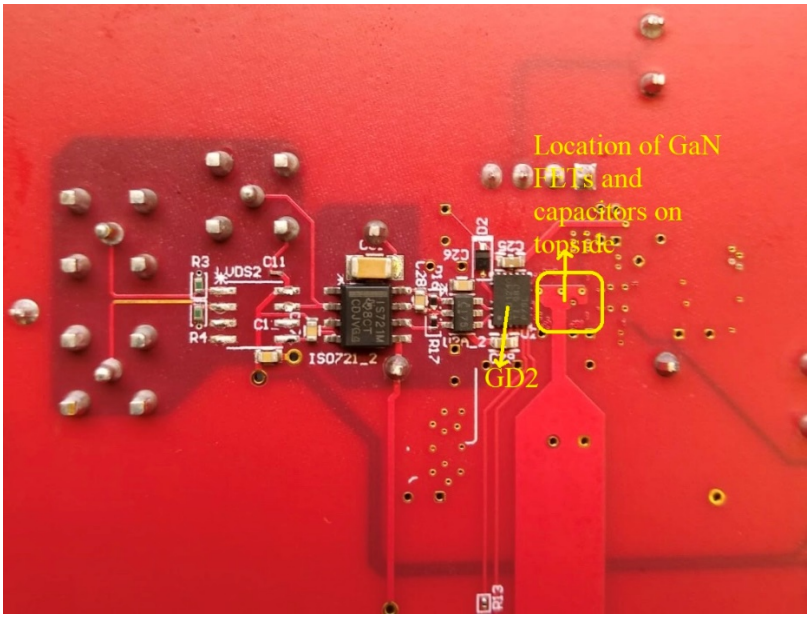


Figure 3-4: Bottom side of the prototype PCB to verify the proposed gate driving technique.

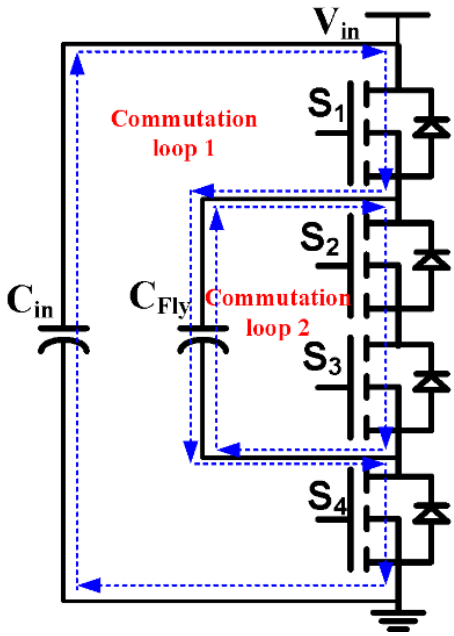


Figure 3-5: Commutation loops FCTL buck converter.

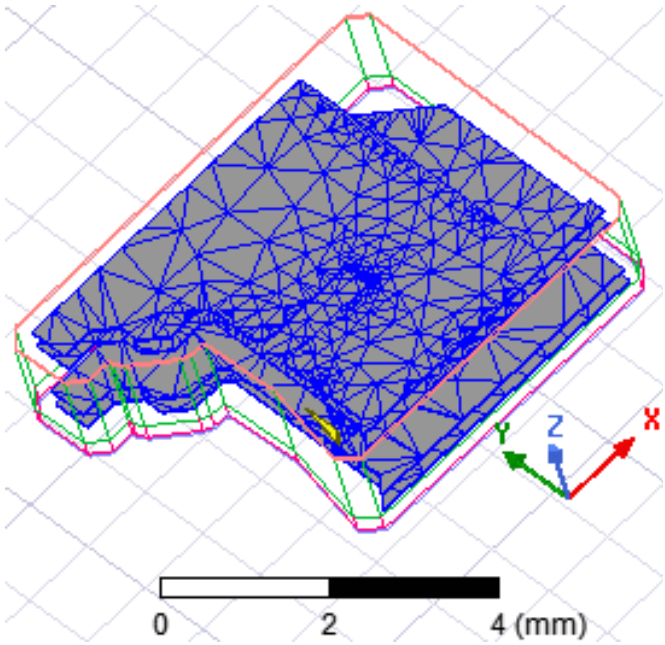


Figure 3-6: The portion of the PCB layout extracted to Q3D, where the power and ground planes are routed on the PCB.

The flying capacitor along with S_2, S_3 forms the second commutation loop. To minimize the loop inductance the input DC voltage plane and the power ground return planes are routed in the adjacent layers of PCB. The input DC voltage plane is routed on the top and bottom layers and the power ground plane is routed on the two inner copper layers. The positive (P) and return paths (N) of the flying capacitor are also routed in a similar passion to mitigate the second commutation loop inductance. X7R type multi-layer ceramic capacitors of footprints 0402 and 0603 are used. The 0402 capacitors are placed closer to the GaN FETs to reduce the commutation loop area. Figure 3-6 shows the portion of the 4-layer PCB extracted to the ANSYS Q3D simulator, where the GaN FETs and DC capacitors are placed and routed. The commutation loop 1 consists of input DC positive and ground return planes routed next to each other in two pairs over the four layers of the PCB. Power loop stray inductance of loop 1 is calculated over a 1 GHz frequency range and plotted as in Figure 3-7. The value of the stray inductance at 20 MHz switching frequency is 390 pH. The parasitic inductance of commutation loop-1 is also estimated through the experimental switch-node waveforms (Figure 3-14) using (3.4):

$$L_{CL1} = 1/(4\pi^2 f_{ring}^2 C_{oss}). \tag{3.4}$$

Where f_{ring} is the measured switch node ringing frequency (here, 1.2 GHz) and C_{oss} is the FET drain-to-source capacitance, which is considered as 32 pF from the EPC8004 data sheet [64]. The calculated value of parasitic inductance is 550 pH. A cumulative mismatch of ~30 % is observed between the measured and estimated inductance values,

which can be attributed to the lead inductance of the circuit elements such as FETs and DC link capacitors, voltage probe tip-inductance, and capacitance, which are not considered in the ANSYS simulation. In practice, the C_{oss} values are usually a bit higher than the datasheet. Hence the calculated value of L_{LC1}, which uses datasheet value of C_{oss} is slightly higher. The second commutation loop is also routed in a similar passion by placing the positive and negative planes of the flying capacitor in the adjacent layers.

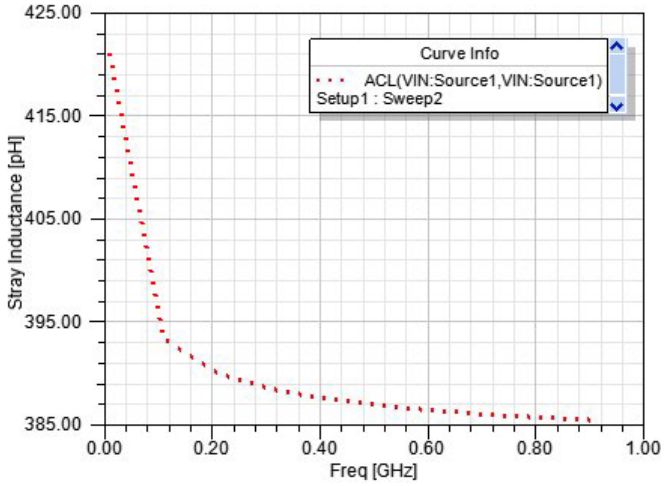


Figure 3-7: Commutation loop-1 inductance of power and ground planes of PCB layout.

3.5.1 Experimental Results

The experimental results of the gate driver up to 40 MHz switching frequency are presented in this section. Tektronix's MSO5-series 2 GHz bandwidth scope and TDP1000, 1 GHz differential voltage probe is used to record the gate voltage pulses.

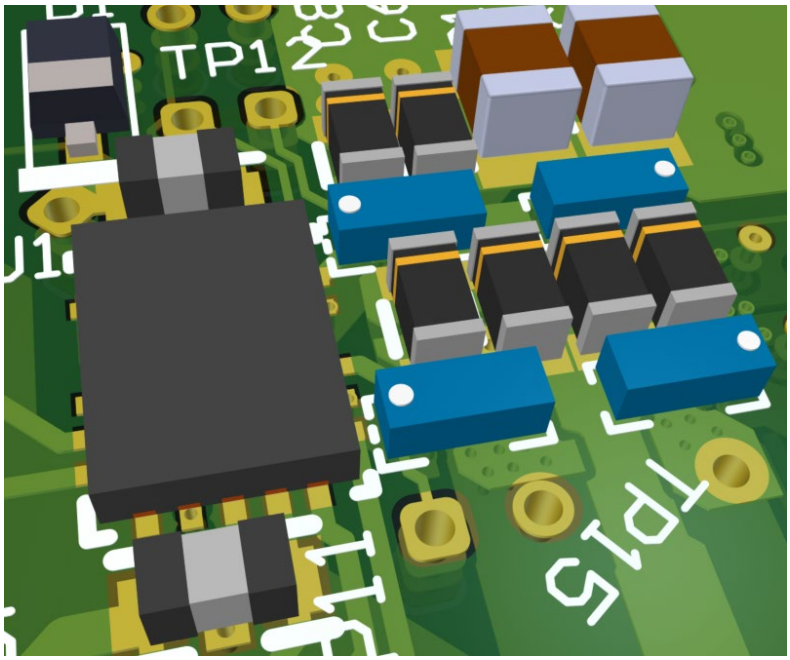


Figure 3-8: Placement of GD1 and EPC GaN MOSFETs on the top side of PCB.

Figure 3-9 shows the gate voltages of all four switches of the FCTL converter with a duty cycle below 50 % at 20 MHz. The gate pulses to switch S_2 are phase-shifted by an angle of 180° from S_1. The gate pulses to S_1, S_4 and S_2, S_3 are complementary pairs, whose dead time is controlled by adjusting the onboard potentiometer resistances. The switching frequency is increased to 40 MHz and the recorded gate voltages are presented in Figure 3-10.

To verify the performance of the proposed gate drive technique, the gate voltages are recorded at various load currents. Figure 3-11 shows the measured gate pulse to switch S_1 over a load current range of 0.45 A to 2.4 A. The gate voltages are within the limits of EPC8004 GaN FET [64]. The steady-state gate pulse voltages of S_2, S_3 and S_4 are also measured across the corresponding bootstrap capacitors at various

load currents and plotted as shown in Figure 3-12. The gate voltages of S_3 and S_4 are regulated at 5 V by the internal LDOs of the gate driver ICs, whereas the gate voltages of S_1 and S_2 are not directly regulated by LDO and varies slightly with load current. The steady-state gate voltage of S_1 measured across C_6, decreases with the increase in load current due to the R_{dson} drop across S_2 as given by (3.3). In contrast, the R_{dson} drop of S_3 aids to the gate voltage of S_2 and increases slightly with the increase in load current as represented in (3.2). Overall, the gate voltages of all the switches are maintained well within the operable limits of EPC8004 GaN FET.

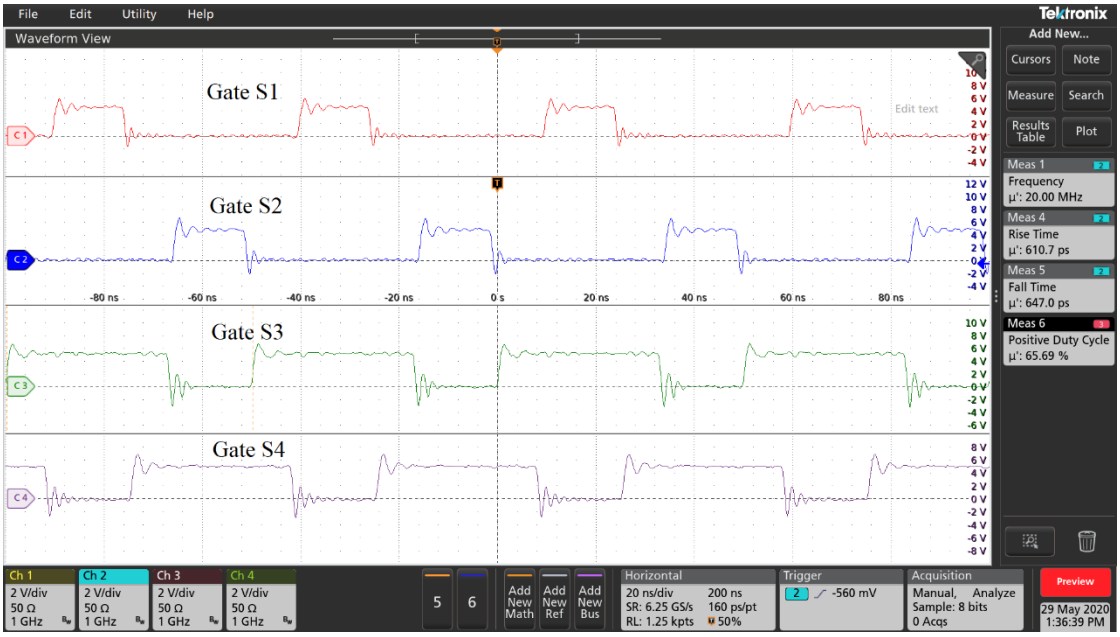


Figure 3-9: Measured gate pulses of the proposed gate drive technique at 20 MHz. Gate pulses to S_1 and S_4 are complementary. Gate pulses to S_2 and S_3 are complementary (x-axis:20ns/div).

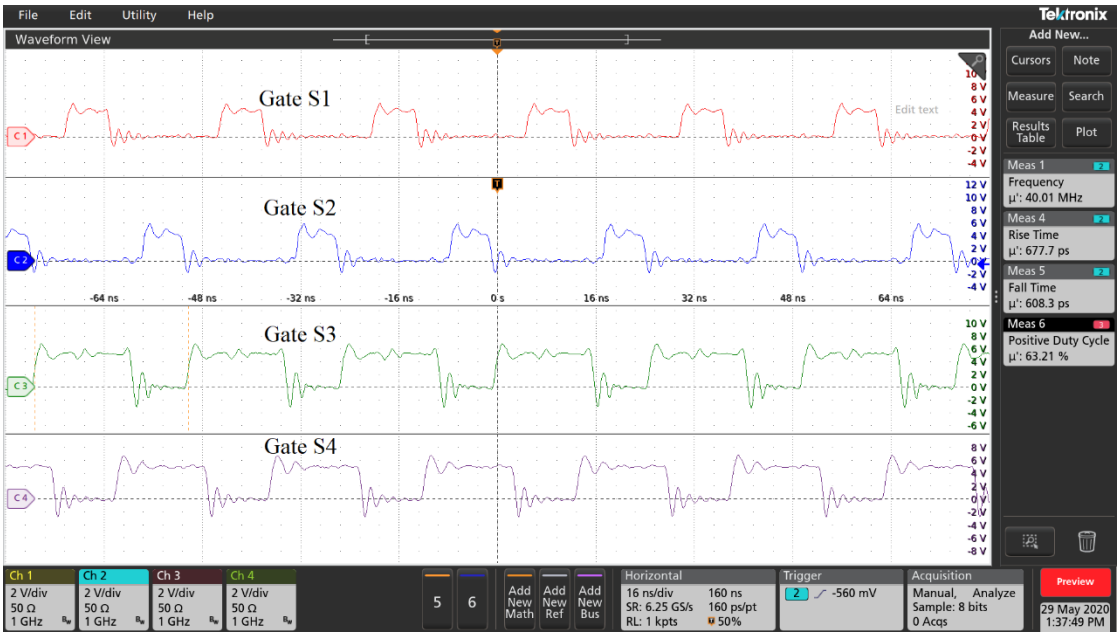


Figure 3-10: Gate pulses measured at 40 MHz (X-axis:16ns/div).

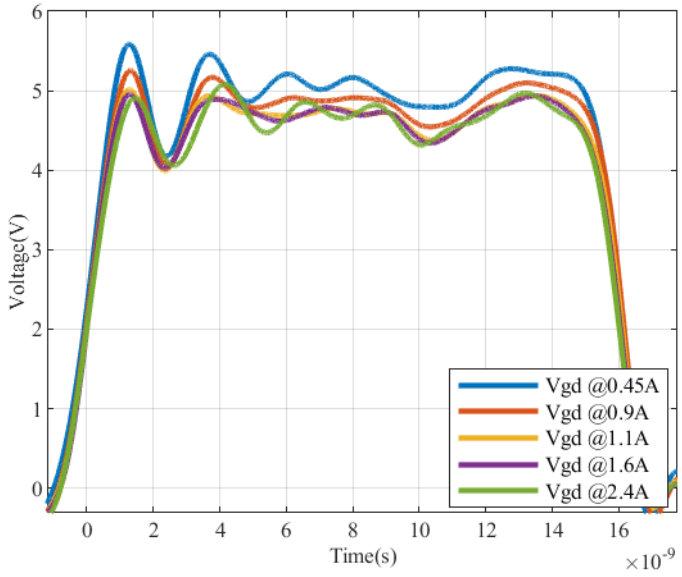


Figure 3-11: Measured gate pulse voltage of the switch S_1 at various load currents.

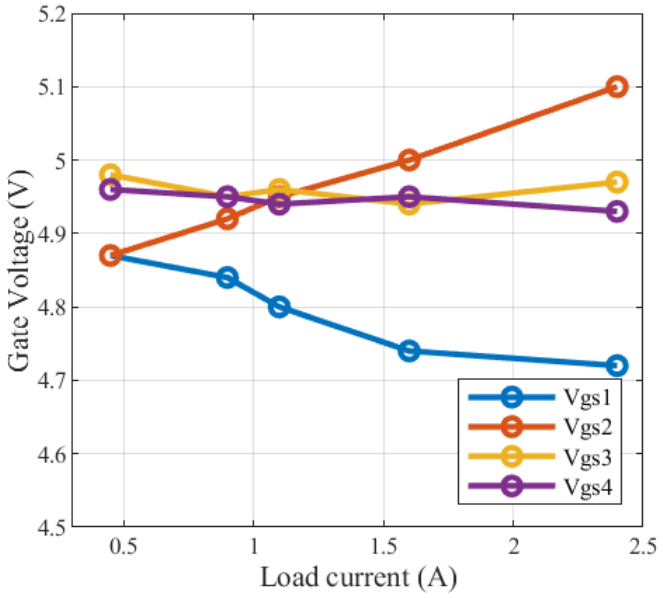


Figure 3-12: Measured gate voltages of switches all the GaN MOSFETs at various load currents.

Figure 3-13 shows the input and output PWM signals of the GD1 and GD2 at 25 MHz. The propagation delay introduced by the LMG1210 half-bridge driver IC and delay of PCB trace is measured as 14 ns for both the gate driver ICs. Matched propagation delay is one of the vital aspects as the unmatched propagation delay can lead to inaccurate switching of the converter. The switch node voltage and the gate pulse of switch S_1 are shown in Figure 3-14. The switch node voltage is switching between 0 and 15 V at 40 MHz when supplied with 30 V DC input voltage, while the gate pulse frequency is only 20 MHz. The test points to measure the gate signals are located a bit away from the gate driver. Hence, minimal ringing is observed in the measured gate pulse voltage which is primarily due to the parasitic loop inductance formed by test point traces and the probe capacitance.

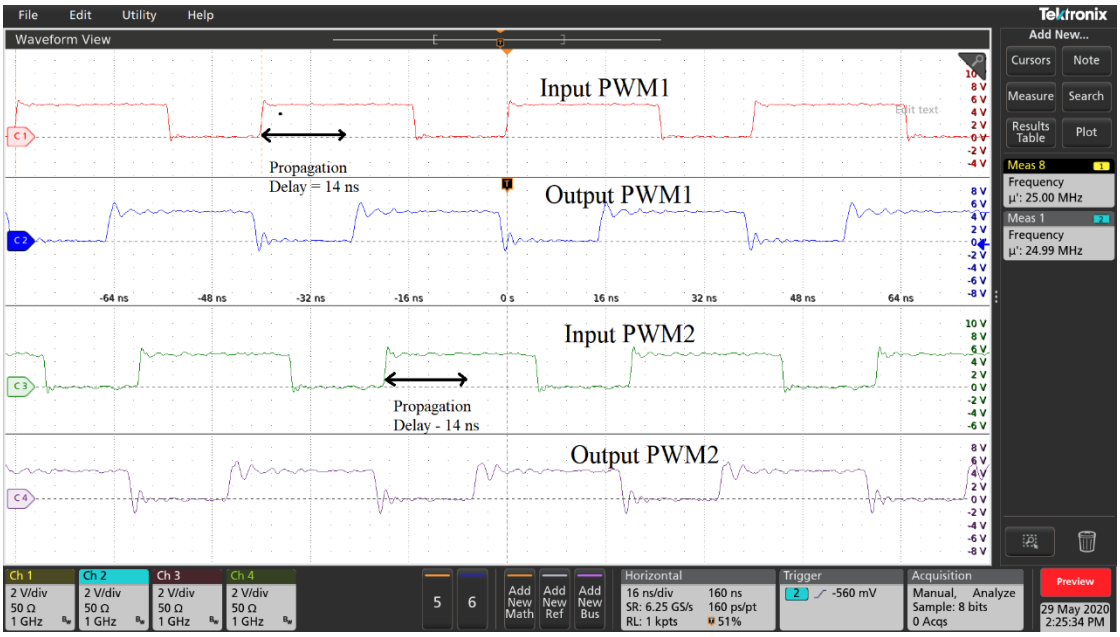


Figure 3-13: Measured input and output PWM signals of the proposed gate drive technique with gate driver propagation delays at 25 MHz (X-axis scale:16ns/div).

Table 3-1: Comparison of the proposed gate drive method with the existing state-of-the-art cascaded bootstrap techniques.

Gate drive technique	**No. of half-bridge gate driver ICs**	**No. of External LDOs**	**No. of external Bootstrap FETs/Diodes**	**No. of bootstrap capacitors**	**No. of Gate signal isolators**	**Highest switching frequency reported**
This work	2	None	0/3	4	2	40 MHz
Charge pump method [70]	2	1	0/4	7	4	140 kHz
Cascaded Synchronous Bootstrap [71]	3	None	3/3	5	4	500 kHz

Table 3-1 shows the comparison of the proposed gate drive method with the existing state-of-the-art cascaded bootstrap gate drive techniques for flying capacitor multi-level converters. Here the number of levels considered for the comparison

purpose is three. The proposed gate drive technique uses a minimum number of components and reduces the gate driver size and PCB layout complexity associated with high-frequency switching.

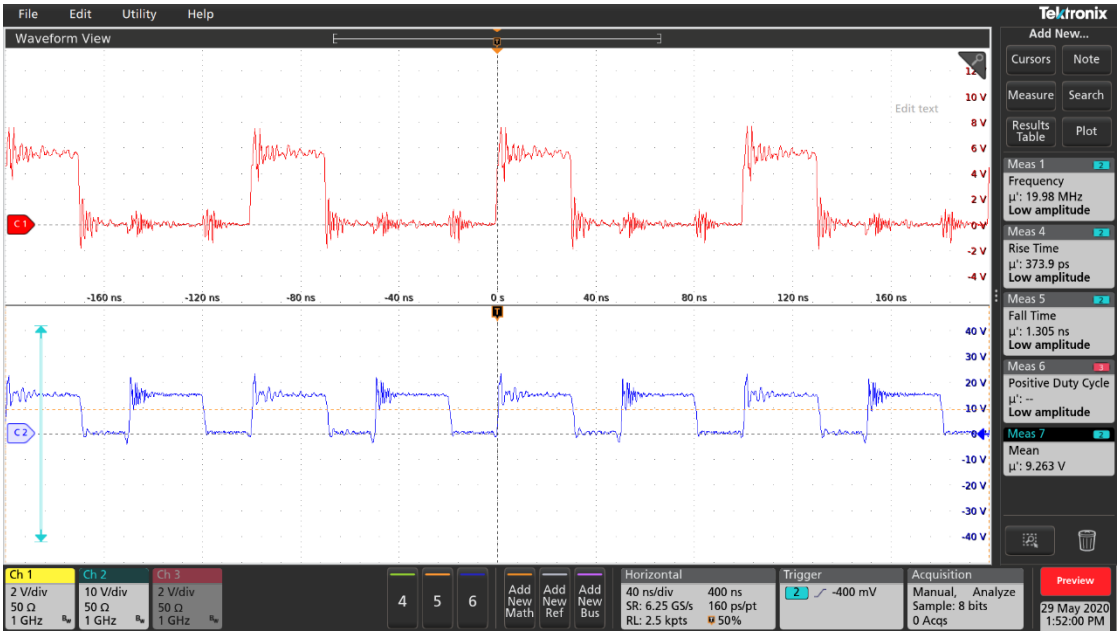


Figure 3-14: Experimental waveforms. Ch1: Gate signal. Ch2: Switch node voltage. The frequency of switch node voltage (40 MHz) is double the gate signal switching frequency (20 MHz).

3.6 **Summary**

A novel gate driving strategy is proposed for a flying capacitor three-level buck converter. The prototype was implemented with a reduced number of half-bridge gate driver ICs and component count when compared with the closest existing literature. The proposed gate driving method works in PWM mode with two input PWM signals. The dead time of the gate drive output signals can be adjusted using potentiometer resistances provided on the prototype. The proposed technique also operates with an

independent gate pulse to each of the four switches. The gate voltages measured at various load currents are within the operable limits. Experimental results at the various switching frequency of operation show the effectiveness of the proposed concept at Multi-MHz operation.

4. FLYING CAPACITOR BASED MULTI-PHASE THREE-LEVEL BUCK CONVERTER ENVELOPE TRACKING POWER SUPPLY

4.1 Introduction

A flying capacitor-based single-phase three-level buck converter is designed in the previous chapter to track high voltage envelope signal of maximum voltage 42 V and bandwidth of 8 MHz while switching at 20 MHz switching frequency. To improve the bandwidth further the switching frequency has to be increased. This leads to increased switching losses at the high switching frequency. Moreover to supply high power applications single converter is not sufficient due to the limited current-carrying capability of GaN FET.

A multi-phase buck converter with the interleaved operation is proposed in [27], [67] to meet the high bandwidth and high-power processing requirements. The interleaved mode of PWM improves the effective switching frequency without the need for an increase in device switching frequency. Therefore the size of the output low-pass filter components reduces and the bandwidth of the filter increases predominantly. A conventional two-level multi-phase buck converter is shown in Figure 4-1. For an *N*-phase interleaved two-level buck converter the gate switching pulses of each phase are interleaved by $360^0/N$ concerning the corresponding gate pulses in the adjacent phases. This leads to an effective ripple frequency of N times the device switching frequency.

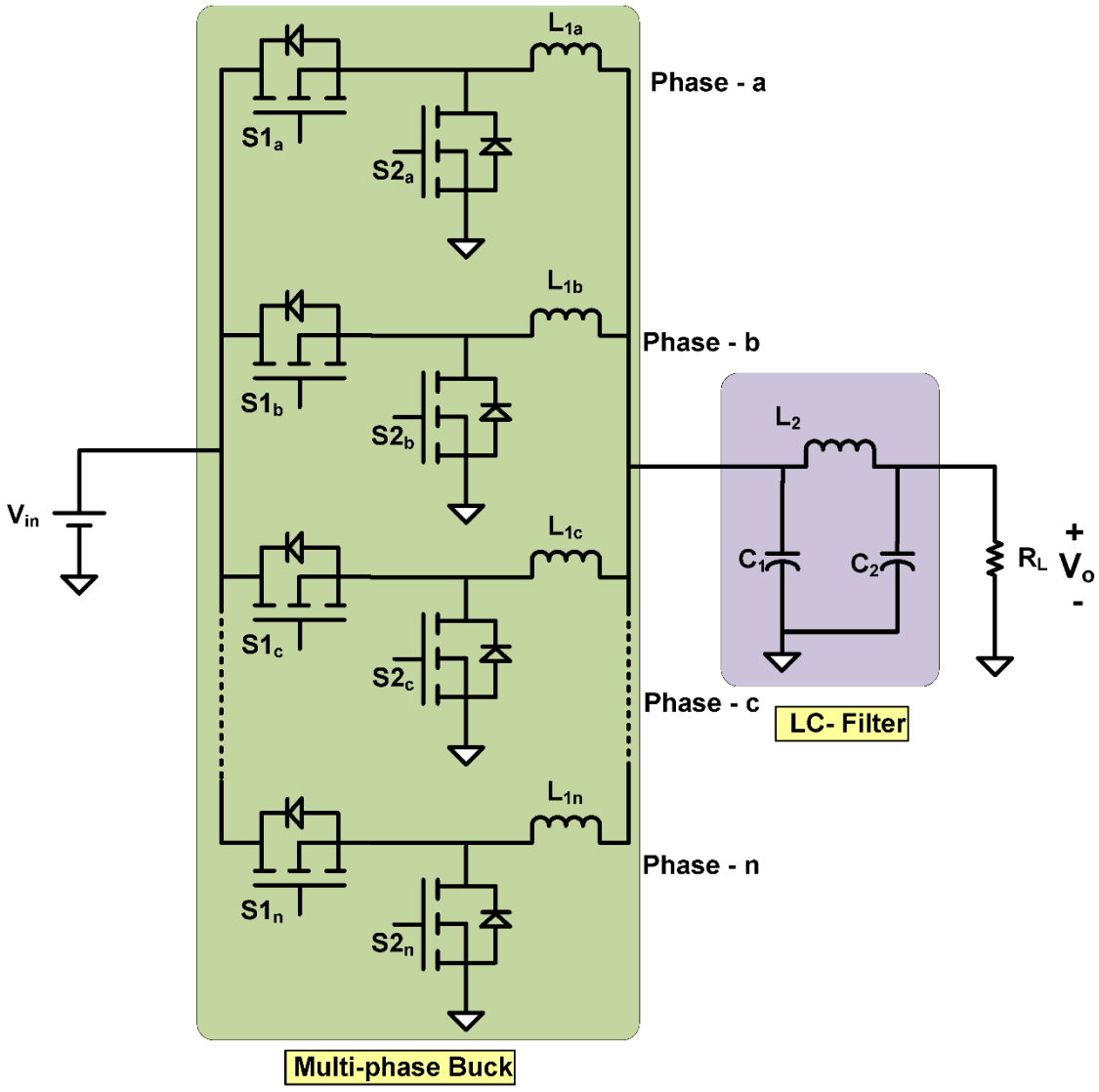


Figure 4-1: Conventional multi-phase two-level buck converter.

4.2 Flying Capacitor Multi-Phase Three-Level Buck Converter

The interleaved multi-phase operation is adopted to the flying capacitor-based three-level buck (FCTL) converter to meet the need for high power and bandwidth. Figure 4-2 shows an *N*-phase flying capacitor-based three-level buck converter with fourth-order LC low-pass output filter. As opposed to conventional *N*-phase interleaved

two-level buck converter the gate switching pulses of the *N*-phase FCTL buck converter are interleaved by $360^{\circ}/2N$. Also, the interleaving in PWM yields an effective ripple frequency of $2N$ times the device switching frequency. This is twice the value when compared with regular *N*-phase two-level buck.

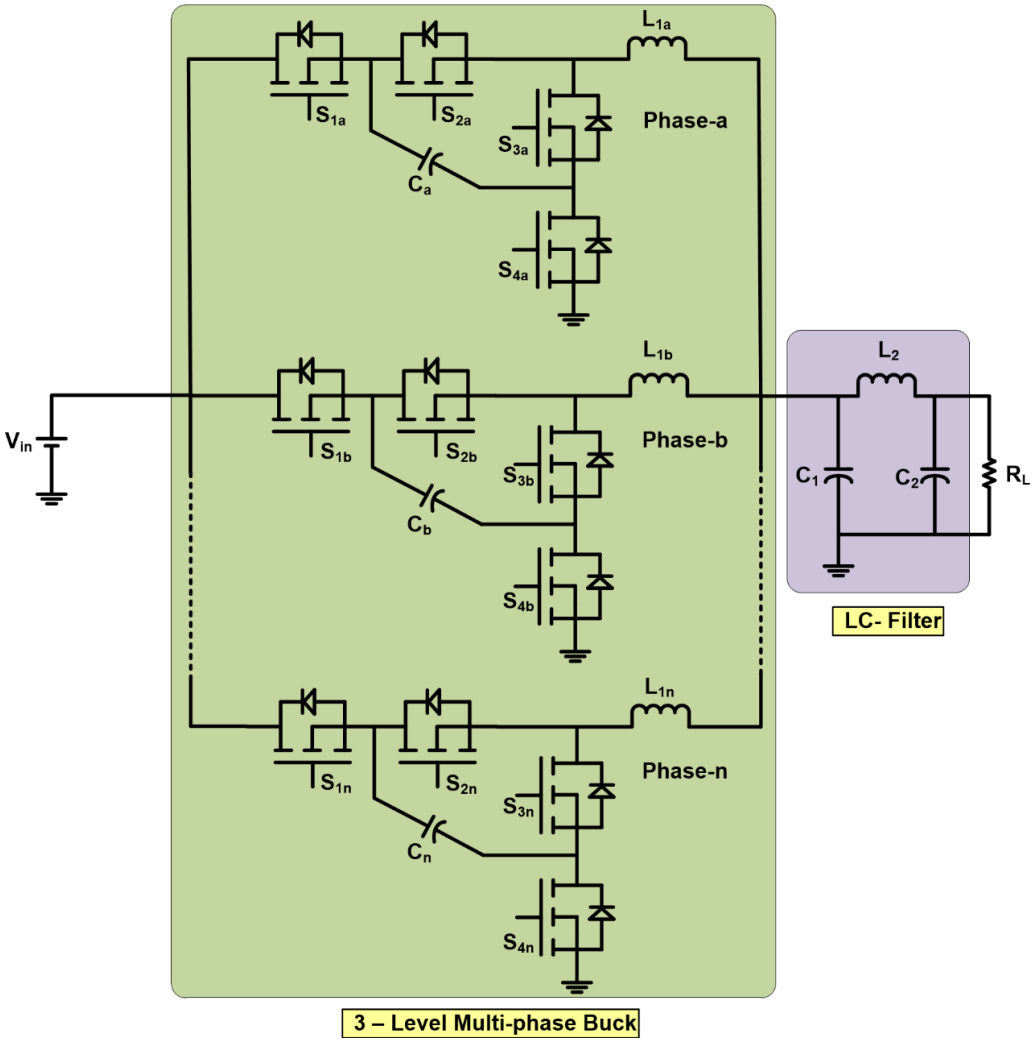


Figure 4-2: Flying capacitor-based multi-phase three-level buck converter with fourth-order LC low-pass output filter.

4.3 **Power Stage Design**

The power stage architecture of the two-phase three-level buck converter along with the ZVS fourth-order output filter for ET application is shown in Figure 4-3. The RFPA behavior is modeled as a resistive load R_L [65]. Each converter consists of four switches $S_{1x}, S_{2x}, S_{3x}, S_{4x}$ (where $x = a, b$). The two bottom devices S_{3x} and S_{4x} operate in synchronous rectification mode and hence, continuous conduction of the converter throughout the duty cycle range. The gate pulses to the top two devices, S_{1x} and S_{2x} are similar, with a duty cycle D, but phase-shifted by 180°. The switch pairs S_{1x}, S_{4x} and S_{2x}, S_{3x} are switched in a complementary manner, as shown in Figure 4-4 and Figure 4-5. Phase – b gate pulses are delayed 90° to achieve interleaved operation. By proper control of the voltage across the flying capacitor at $V_{in}/2$, the switch node voltage of each phase switches between 0 and $V_{in}/2$ for duty cycle range $0 < D < 0.5$ as shown in Figure 4-4. For the duty cycle range $0.5 < D < 1.0$, the switching node switches between voltage levels $V_{in}/2$ and V_{in} as shown in Figure 4-5. Moreover, the switching node frequency of each phase is twice the device switching frequency, and the two switch node voltages V_{swa} and V_{swb} are phase-shifted 90° apart. Therefore, the total current I_T has an effective ripple frequency of four times the device switching

frequency, which leads to filter size reduction, and improved open-loop converter bandwidth.

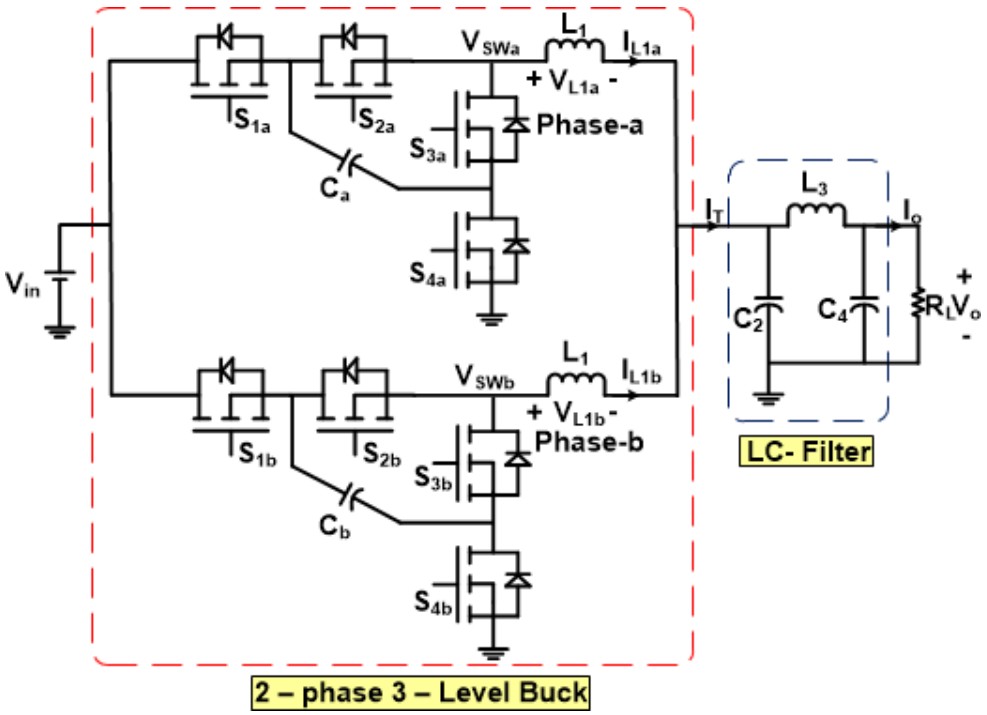


Figure 4-3: Power stage of flying-capacitor based two-phase three-level buck converter.

4.3.1 Device Selection

EPC8000 series eGaN FETS [62], [63] are selected due to their ultra-small footprint, low switching loss, and zero reverse recovery charge. The effective switching frequency for a two-phase three-level buck and an equivalent four-phase two-level buck converter is the same for the same per phase device switching frequency. The number of switching devices used in both designs is also the same. Hence, the power loss models are developed for both the converters, and efficiency analysis is performed with EPC8004 and EPC8009 GaN FETs as switching devices.

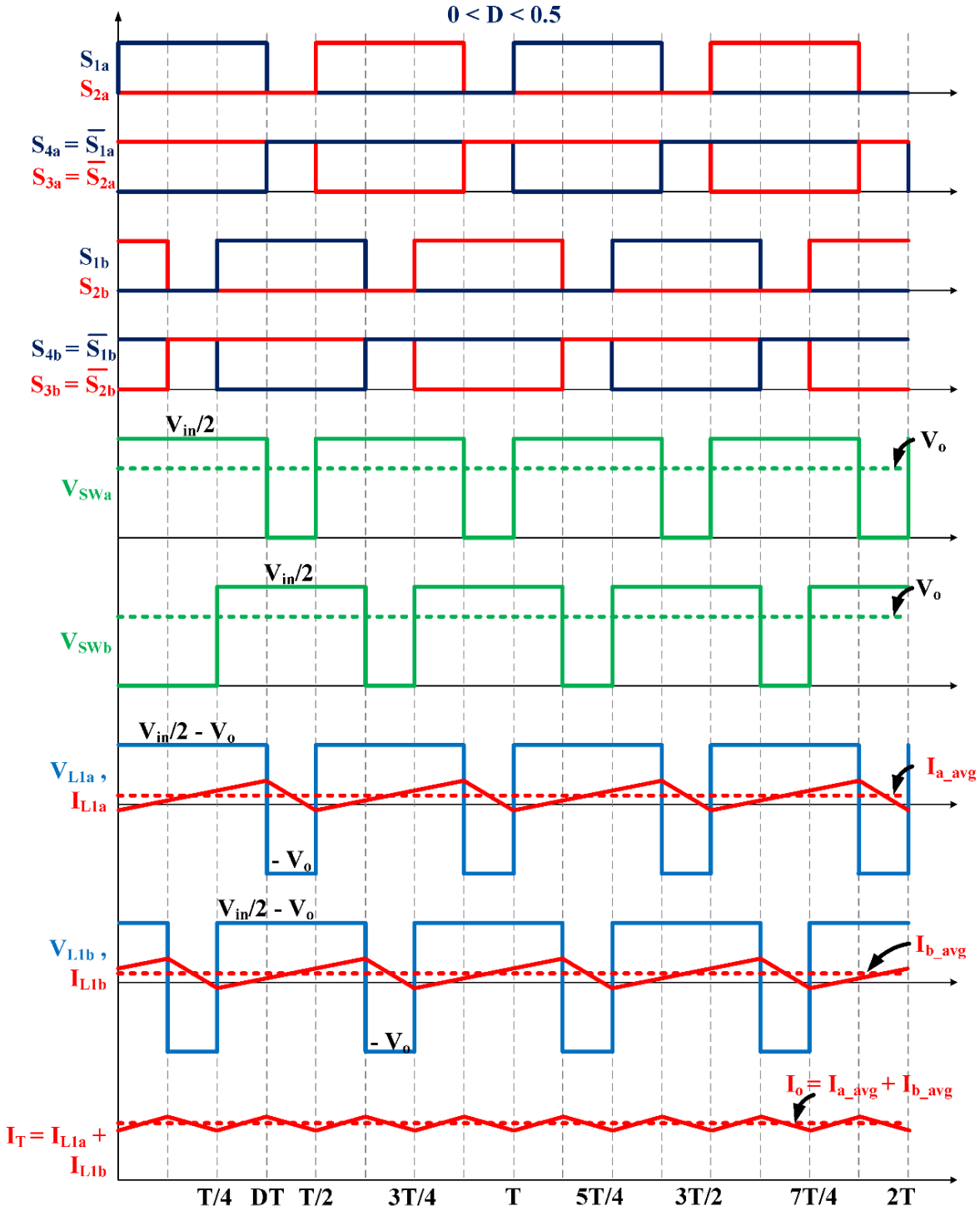


Figure 4-4: Model switching waveforms of the two-phase three-level buck converter for $0 < D < 0.5$.

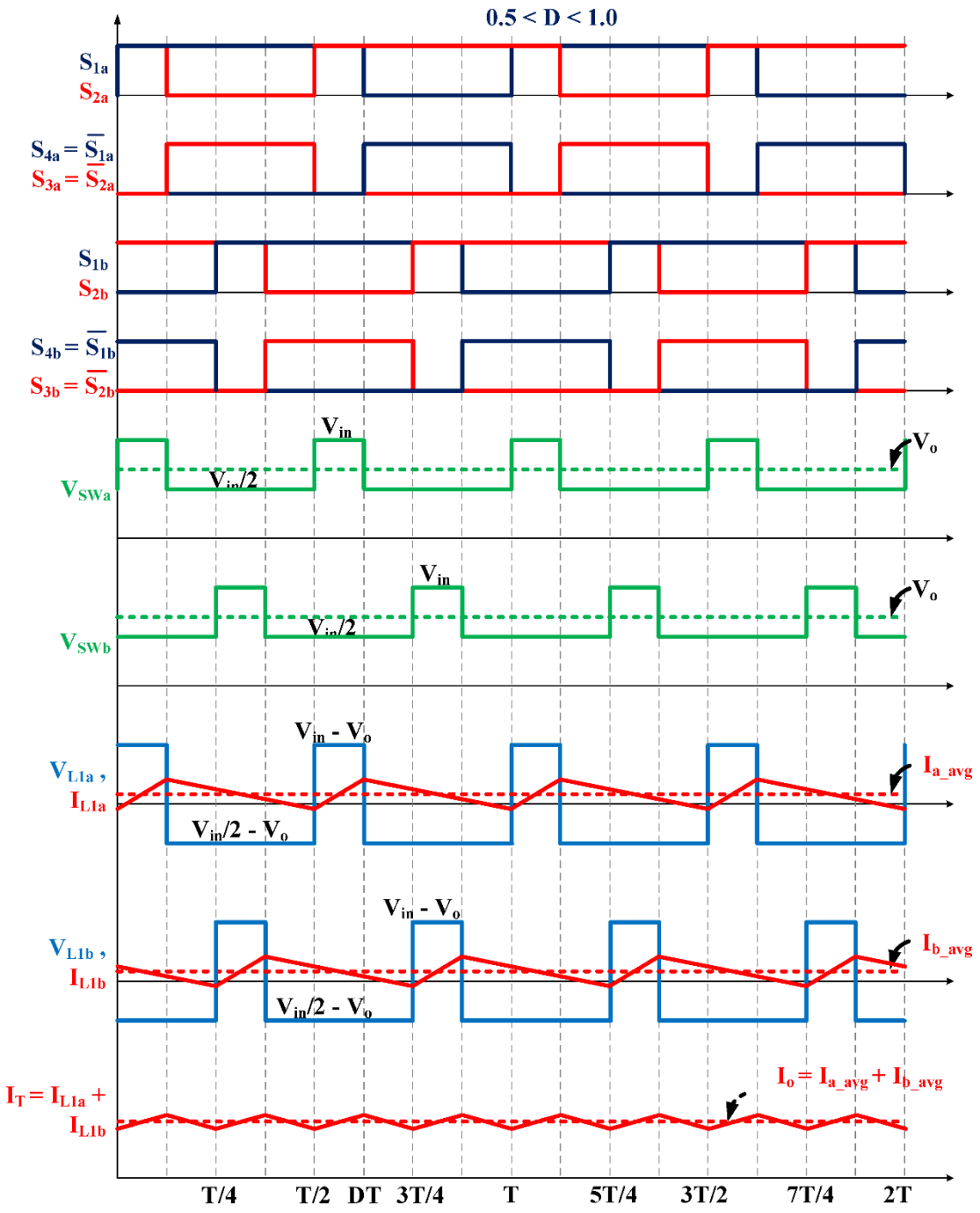


Figure 4-5: Model switching waveforms of the two-phase three-level buck converter for 0.5 < *D* < 1.0.

For the designed maximum power rating of 115 W, Figure 4-6 and Figure 4-7 depict that the proposed three-level design has better efficiency when compared to its conventional two-level counterpart at high switching frequencies of up to 50 MHz. This is because the proposed three-level buck converter has reduced voltage stress on the switching devices. This makes the three-level design a better choice for higher bandwidth ET applications. Moreover, with the EPC8004, the proposed design exhibited a better efficiency. Texas Instruments LMG1210 gate driver [79] with adjustable dead time and switching frequency capability of up to 50 MHz is used to drive the eGaN FETs.

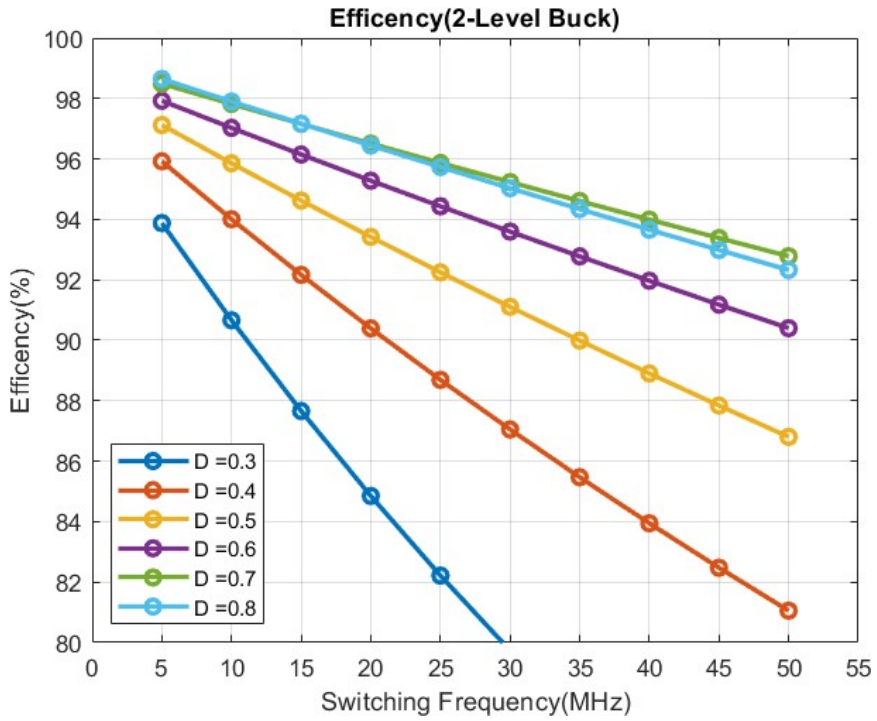


Figure 4-6: Switching frequency Vs efficiency of conventional four-phase two-level buck design.

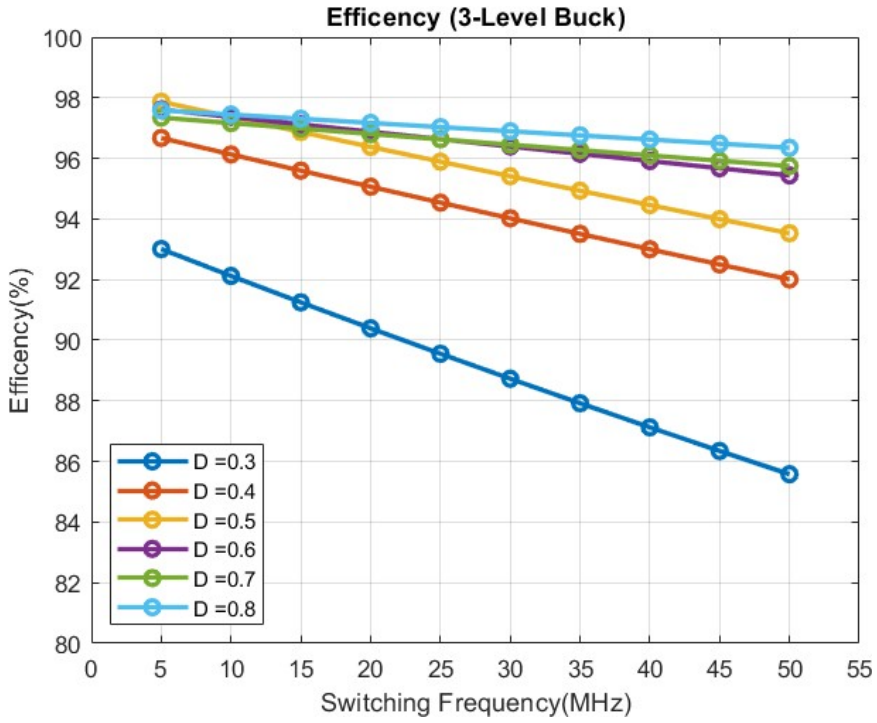


Figure 4-7: Switching frequency Vs efficiency of proposed two-phase three-level buck design.

4.4 Inherent Phase Current Balancing

Butter-worth, Bessel–Thomson, and Legendre–Papoulis are some of the traditional higher-order filter types that can be used in ET applications to full fill the needs of bandwidth and switching ripple attenuation. And also the filter component values can be easily calculated from standard transfer functions for a specific cut-off frequency [80], but the zero voltage switching (ZVS) conditions are not met. This leads to unbalance phase currents and reduced efficiency. The design of the ZVS low pass filter for a two-phase three-level buck converter with a bandwidth of 20 MHz is presented in this section.

For the proposed three-level buck converter design, the top two devices S_{1x} and S_{2x} that connects the inductor L_1 to input DC bus/capacitor positive terminal are referred to as High Side MOSFETs (HSM), and the bottom two devices S_{3x} and S_{4x} that connects the inductor L_1 to ground/negative terminal of the flying capacitor are termed as Low Side MOSFETs (LSM). ZVS turn-on of the LSMs is possible by inserting a proper delay in the gate signals to these low-side devices. But, the turn-on of the high side devices is dissipative. This is due to the lack of negative inductor current to charge/discharge the parasitic capacitance across the devices. In the proposed design, the ZVS turn-on of the HSM is achieved by designing the L_1 inductor value in such a way that it carries a peak-to-peak ripple current more than twice the value of its average current. By selecting a proper ZVS inductor value L_1, the phase currents are also balanced without using any current control loops.

For instance, consider the period during which S_1 and S_3 are in conduction and $0.5 < D < 1.0$. When S_3 is turned off, the inductor negative peak current charge/discharges the parasitic capacitance across S_2 and S_3 as shown in Figure 4-8 and Figure 4-9. This makes the switch node voltage V_{in} and in turn the voltage across S_2 to zero as if it is turned on. And the time to charge/discharge these switches to $V_{in}/2$ is inversely proportional to the inductor negative peak current i_{neg-pk} and is given by

$$t_c = \frac{2C_{oss}}{i_{neg\_pk}} V_{in}/2, \tag{4.1}$$

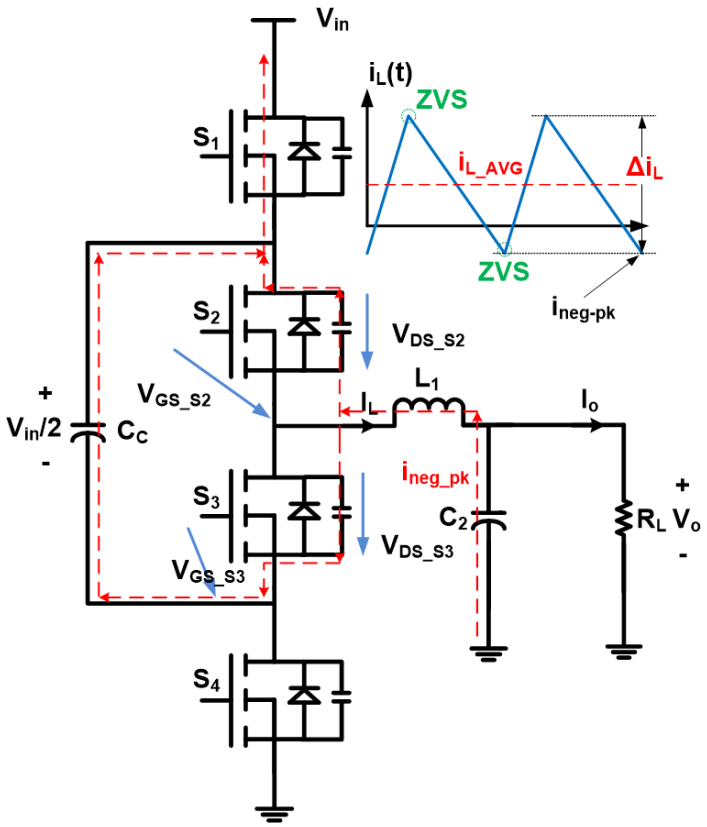


Figure 4-8: Power stage of the three-level synchronous buck during the turn-off of LSM.

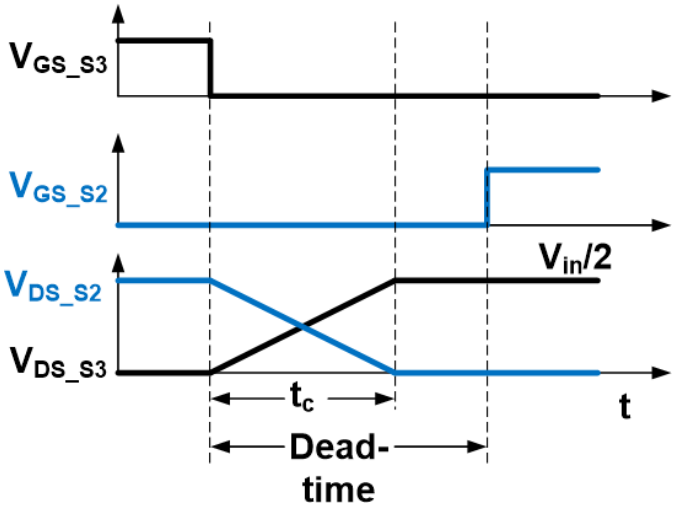


Figure 4-9: Primary waveforms of the three-level synchronous buck during the turn-off of LSM.

where C_{oss} is the device output capacitance. The positive difference of ($Deadtime - t_c$), increases the effective duty cycle and leads to an increment in the average inductor current of that phase. The phase with less average current (higher absolute value of i_{neg_pk}) has the lesser charging time, t_c. This leads to a higher effective duty cycle of that phase and increases the average current carried by it. This phenomenon works as a virtual negative feedback effect and maintains phase current balance inherently.

4.5 ZVS Filter Design

The basic circuit diagram of the multi-phase three-level buck converter is shown in Figure 4-2. In this section, a detailed ZVS filter design guide for a multi-phase three-level converter for high bandwidth envelope tracking application is discussed.

4.5.1 Filter Design for Single-Phase Three-Level Buck Converter

To achieve ZVS operation, the inductor negative peak current should be less than zero at all load currents. To achieve ZVS operation, the inductor negative peak current should be less than zero at all load currents. At $L_1 = L_{1\max}$ the inductor ripple current is equal to its static current. Here, $L_{1\max}$ of a three-level buck converter is derived as

$$L_{1max} = \min\left[\frac{V_{in}(1-D)(D-1/2)}{2 I_{L1} f_s}\right], \text{ for } 0.5 < D < 1.0 . \tag{4.2}$$

The inductor quasi-static current I_{L1} is approximately calculated as

$$I_{L1} = \frac{DV_{in}}{R_L}, \tag{4.3}$$

where I_{L1} is inductor static current, V_{in} is the input voltage, R_L is load resistance, D is the duty cycle, and f_s is the switching frequency. By substituting (4.3), (4.2) can be further simplified in to

$$L_{1max} = \min\left[\frac{R_L(1-D)(D-1/2)/D}{2f_s}\right]. \tag{4.4}$$

Hence, by designing the filter's inductor value $L_1 < L_{1max}$, the inductor ripple current is always greater than the inductor quasi-static current. Hence, the inductor current discharges to below zero and changes its direction. During the dead-time, this negative inductor current flows back into the MOSFETs output capacitance (C_{oss}) and charges or discharges them to half the input voltage. This phenomenon leads to the ZVS turn ON for the top side MOSFET and current balancing among phases. A detailed explanation is presented in the previous section 4.4.

For ET power supply D varies over a wide range from D_{min} to D_{max}. By choosing D_{max} as the maximum duty cycle for ZVS operation, L_{1max} can be calculated using (1). Then, the inductance L_1 should be selected such that it is less than L_{1max}. The remaining filter components (L_3, C_2, and C_4) are designed for the required cut-off frequency and flat passband response. For a three-level buck, the switch node voltage (V_{sw}) frequency

is twice the device switching frequency f_s. Hence, the switching ripple attenuation at the effective switching frequency $2f_s$ is given by

$$A(j\omega_s) = 40\log\frac{2f_s}{f_{02}} + 40\log\frac{2f_s}{f_{01}}, \tag{4.5}$$

where, f_{01} and f_{02} are the two resonant frequencies which are defined as

$$f_{01} = \frac{1}{2\pi\sqrt{L_1 C_2}} \tag{4.6}$$

and

$$f_{02} = \frac{1}{2\pi\sqrt{L_3 C_4}}. \tag{4.7}$$

Here $f_{02} < f_{01}$, and

$$f_{02} \approx f_c, \tag{4.8}$$

where f_c is filter cut-off frequency. The flat passband response is obtained by selecting a low-quality factor Q_2 associated with R_L at f_{02}. The expression for Q_2 is

$$Q_2 = R_L\sqrt{\frac{C_4}{L_3}} < 1. \tag{4.9}$$

From (4.8) and (4.5), f_{01} can be solved by determining the required cut-off frequency f_c and approximate switching frequency attenuation. Then C_2 can be determined by plugging f_{01} value in (4.6). The values of L_3 and C_4 are obtained by

solving (4.6) and (4.9). To validate the accuracy of the approximations made, the condition $f_a > f_{02}$ needs to be validated. Where f_a is obtained from the filter bode plot phase asymptote as

$$f_a = 10^{-1/2Q_1} f_{01}, \tag{4.10}$$

and the quality factor Q_1 at f_{01} is given by

$$Q_1 = R_L \sqrt{\frac{C_2}{L_1}} < 1. \tag{4.11}$$

This condition will make sure that the poles at f_{01} having a minimal impact on the response near the cut-off frequency. The condition $f_a > f_{02}$ holds in most of the cases if the effective switching frequency of the switch node voltage is greater than four times the cut-off frequency ($2f_s > 4f_c$). If the condition $f_a > f_{02}$ is not met, the design needs to be verified using frequency response and adjust the filter design appropriately, as given in section 4.5.3.

4.5.2 Fourth-Order ZVS Filter Design of Multi-Phase FCTL Buck Converter

The Thevenin's and Superposition equivalent circuit of the *N*-phase interleaved three-level buck converter is shown in Figure 4-10 [81]. Where $L_1^{'}$ is the equivalent inductance given by

$$L_1^{'} = L_1 / N. \tag{4.12}$$

The phase shift operation of the interleaved buck converter is modeled as $T_D(s)$ and given by

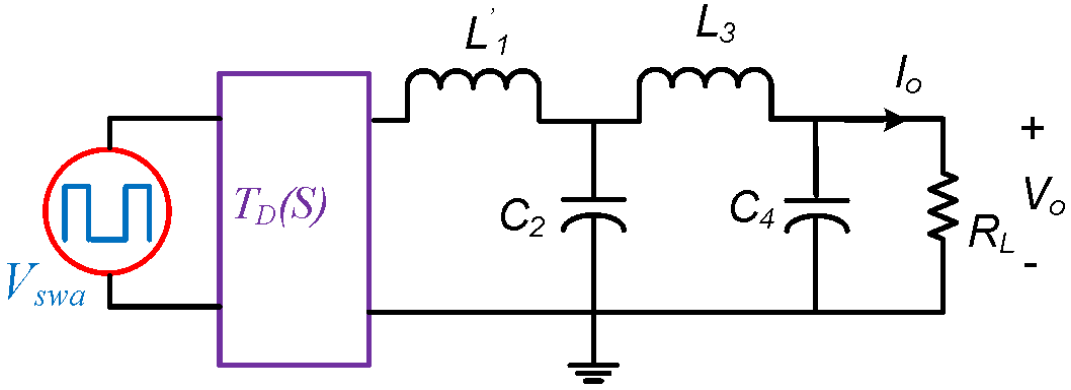


Figure 4-10: Thevenin's and Superposition equivalent circuit of the N-phase interleaved three-level buck converter.

$$T_D(s) = \frac{1}{N}\sum_{k=1}^{N} e^{\frac{-T_s^{'}}{N}(k-1)s}, \tag{4.13}$$

where $T_s^{'} = 1/f_s^{'}$ and $f_s^{'}$ is the switch node voltage frequency, which is twice the device switching frequency. In a multi-phase interleaved 3-level buck converter the phase shift to the PWM signal of i^{th} phase is given by

$$\varphi_i = \frac{i-1}{2N}2\pi. \tag{4.14}$$

The effective switching frequency ripple ($f_{s,eq}$) of an N–phase 3-level buck converter that needs to be attenuated by the filter is given by

$$f_{s,eq} = N2f_s. \tag{4.15}$$

If the phase currents are balanced, the approximate inductor quasi-static current in each phase is

$$I_{L1} = \frac{I_o}{N} = \frac{DV_{in}}{NR_L} \ . \tag{4.16}$$

By substituting (4.15) in (4.4), the maximum limit to inductance L_{1max} to achieve ZVS for *N*-phase three-level converter is given by

$$L_{1max} = min\left[\frac{2NV_{in}\left(1-D\right)\left(D-\frac{1}{2}\right)}{2I_{L1}f_{s,eq}}\right],\ 0.5 < D < 1.0\,. \tag{4.17}$$

By substituting (4.16), (4.17) can be further simplified in to

$$L_{1max} = \min\left[\frac{2N^2R_L\left(1-D\right)\left(D-1/2\right)/D}{2f_{s,eq}}\right]. \tag{4.18}$$

The attenuation constraint at the effective switching frequency $f_{s,eq}$ for an *N*-phase filter is obtained as

$$A\left(j\omega_{s,eq}\right) = 40\log\frac{f_{s,eq}}{f_{02}} + 40\log\frac{f_{s,eq}}{f_{01}^{'}} \ , \tag{4.19}$$

where,

$$f_{01}^{'} = \frac{1}{2\pi\sqrt{L_1^{'}C_2}}\,. \tag{4.20}$$

The verification equation becomes $f_a^{'} > f_{02}$, where

$$f_a^{'} = 10^{-1/2Q_1^{'}} f_{01}^{'}, \tag{4.21}$$

and the modified quality factor $Q_1^{'}$ at $f_{01}^{'}$ is given by

$$Q_1^{'} = R_L \sqrt{\frac{C_2}{L_1^{'}}} < 1 \,. \tag{4.22}$$

Based on these equations a detailed step-by-step procedure is provided below to find out the fourth-order LC-filter component values for the required bandwidth.

4.5.3 Design Procedure

The above design equations are based on certain approximations. Therefore, the final design parameters need to be adjusted based upon the actual frequency response of the filter. For example, the frequency response of the filter during the passband will be undesirable if the quality factor Q_2 at f_{02} is either too high or too low as shown in Figure 4-11. Therefore, the value of Q_2 needs to be modified by adjusting the L_3 and C_4 values based on (4.9). The detailed step by step procedure of the filter design is given below:

Step-1: Choose the filter cut-off frequency based on $f_{s,eq} > 4f_c$, the desired attenuation $A\left(j\omega_{s,eq}\right)$ at the effective switching frequency, and the number of phases *N*.

Step-2: Fix the duty cycle range for ZVS operation and calculate L_{1max} based on (4.18) and choose $L_1 < L_{1max}$.

Step-3: Choose the quality factor Q_2 at f_{02} and solve for L_3 and C_4 using (4.7), (4.8) and (4.9).

Step-4: Calculate $L_1^{'}$ using (4.12) and solve for C_2 based on (4.19) and (4.20).

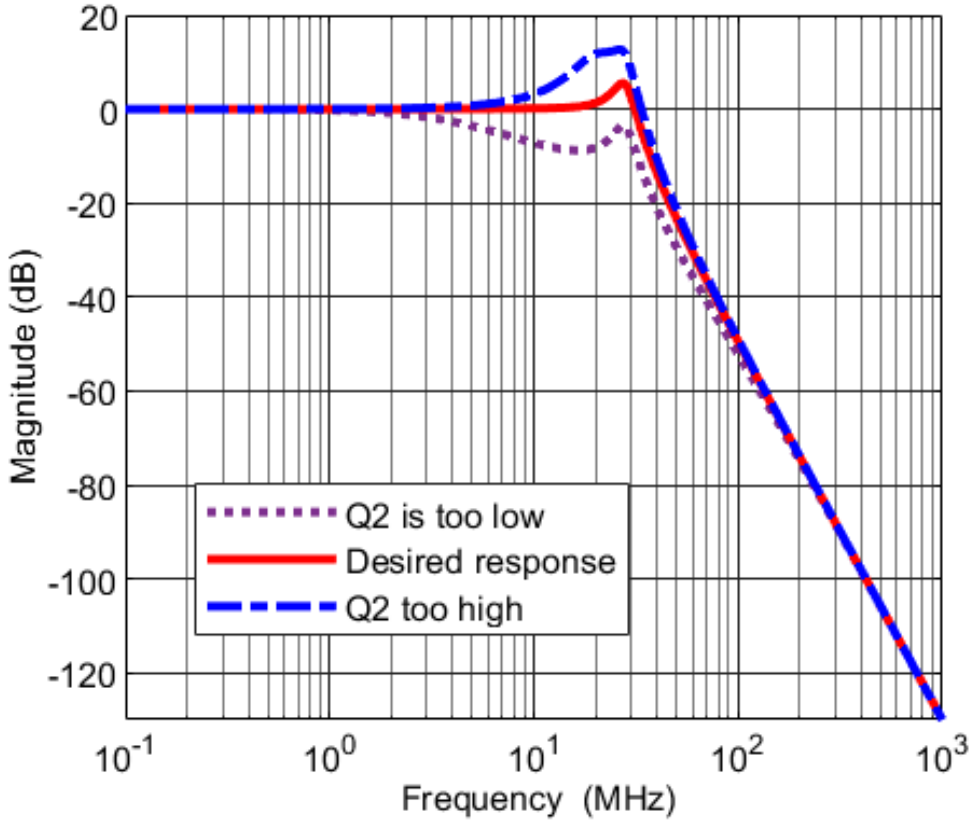


Figure 4-11: Magnitude frequency response at various Q_2.

Step-5: Verify the design by checking the condition $f_a^{'} > f_{02}$. If the condition is not met, check the filter frequency response, and iterate the design parameters L_3 and C_4 until the desired frequency response is achieved.

A fourth-order ZVS filter is designed for a two-phase three-level buck converter with an envelope signal bandwidth of 20 MHz, and a device switching frequency of 25 MHz ($f_{s,eq} = 100\,MHz$). The input voltage to the converter is 30 V, the load resistance is 6.6 Ω and the duty cycle range for ZVS is 0.2 to 0.8.

Table 4-1: Legendre and ZVS fourth-order filter component values with 20 MHz bandwidth

Filter Type	R_L	L_1	C_2	L_3	C_4
Legendre	6.6 Ω	90 nH	1.08 nF	80 nH	.41 nF
ZVS	6.6 Ω	16 nH	4 nF	66 nH	.96 nF

The filter component values designed for an effective switching frequency attenuation of 50 dB are provided in Table 4-1. A standard fourth-order Legendre-Papoulis filter is designed at 20 MHz bandwidth and the filter component values are also provided in Table 4-1.

The frequency response of magnitude for ZVS and Legendre filters is shown in Figure 4-12. They exhibit similar flat responses in the 20 MHz passband. The ZVS filter magnitude response resonates around 27 MHz. But this does not impact the tracking performance as the envelope signal is band-limited at 20 MHz and the resonance is well below the effective switching frequency.

The phase shift in PWM of the converter provides a notch in the magnitude frequency response. This attenuates the per phase switch node frequency component of 50 MHz and provides a better ripple rejection in the output voltage. Figure 4-13 shows

the phase-frequency response of ZVS and Legendre -Papoulis filter. It is noticed that the ZVS filter provides a slightly lower and constant group delay in the passband when compared to the Legendre filter type.

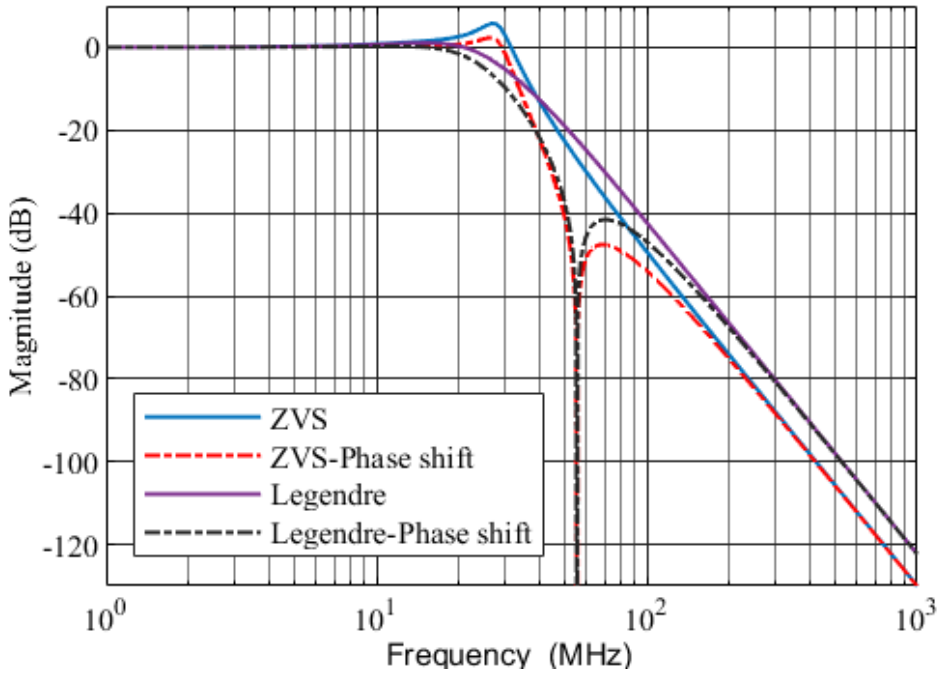


Figure 4-12: Comparison of the frequency response of magnitude.

4.6 **Simulation Results**

A two-phase three-level DC-DC converter is simulated using PLECS. EPC8004 is used as a power semiconductor device due to its low on-state resistance and switching losses. Figure 4-14 shows the switch node voltages and inductor currents of the proposed two-phase three-level buck converter when tracking the envelope signal with 20 MHz bandwidth. The switch node voltages are switching either between (i) 0 V and 15 V or

(ii) 15 V and 30 V, based upon the input envelope command. Hence, voltage stress across the GaN MOSFETs is limited to half of the input voltage.

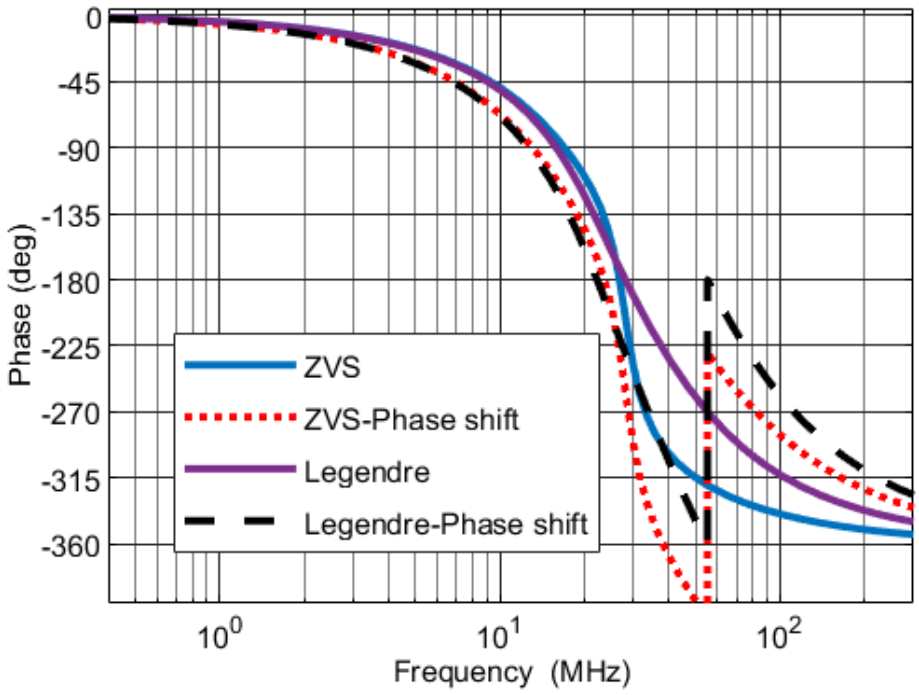


Figure 4-13: Comparison of the frequency response of phase.

4.6.1 ZVS and Legendre Filter Types

The inductor peak currents vary with the variation of duty cycle or both ZVS and Legendre filter types as shown in Figure 4-15. The high peak inductor currents of the ZVS filter lead to increased conduction loss compared to Legendre. However, the switching loss is greatly reduced using the ZVS filter which leads to better efficiency at the high switching frequencies (> 10 MHz).

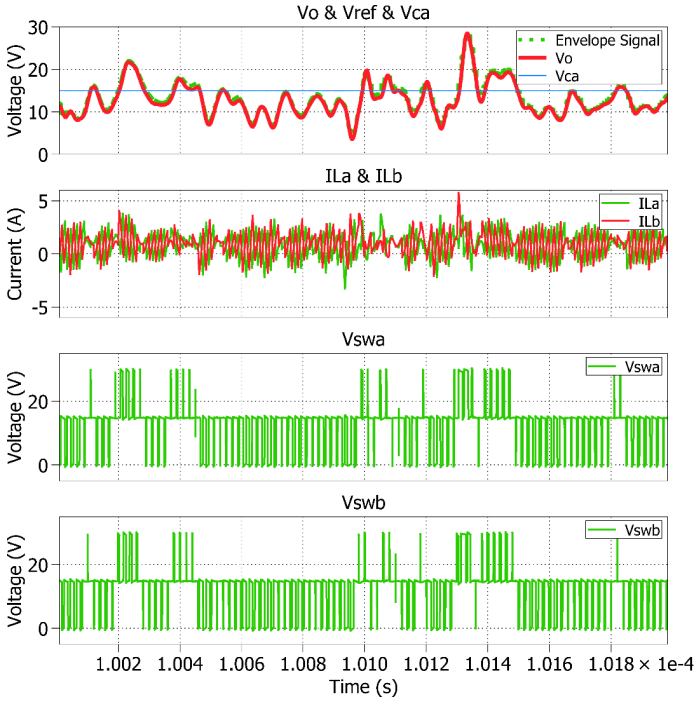


Figure 4-14: Switch node voltages and inductor currents of the two-phase three-level buck with ZVS output filter when tracking 20 MHz bandwidth envelope signal.

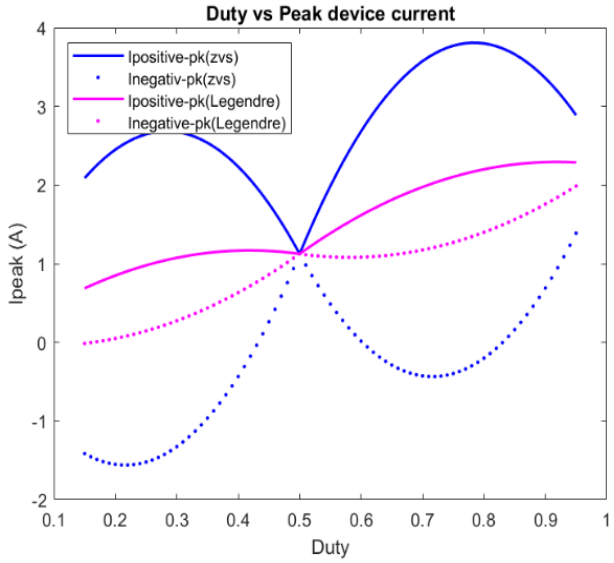


Figure 4-15: Variation of peak inductor currents with Duty cycle for a two-phase three-level buck converter with ZVS and Legendre output filter types.

The ZVS operation of the proposed ZVS filter and Legendre filter are shown in Figure 4-16 and Figure 4-17 respectively. The ZVS turn-on of the bottom side MOSFETs is achieved by allowing proper dead time, whereas the ZVS turn-on for the top side switches can only be achieved using the ZVS filter [82], whereas the ZVS turn-on of topside MOSFETs is not possible by using the Legendre filter.

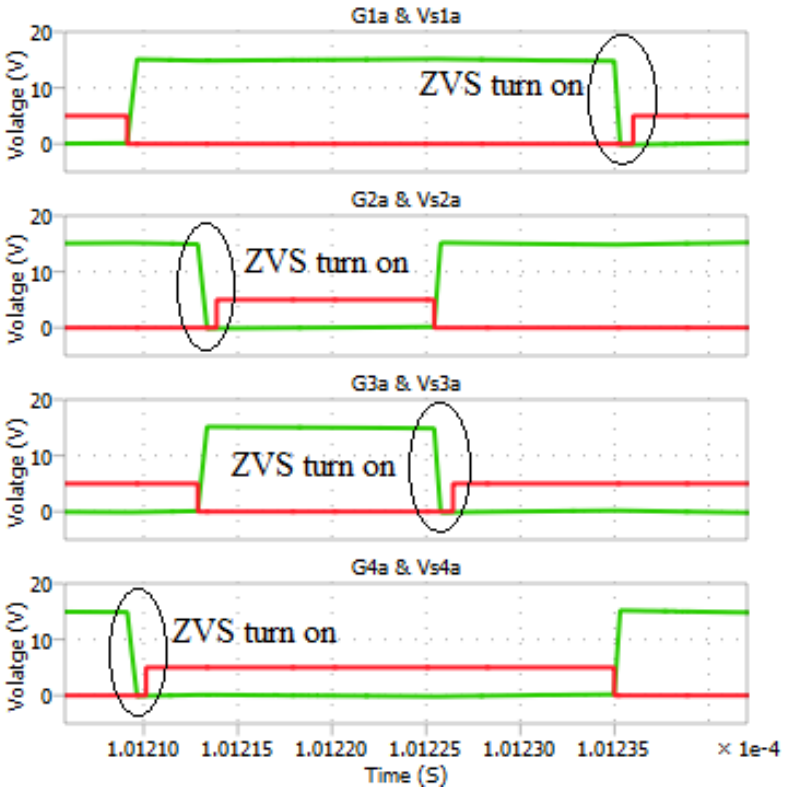


Figure 4-16: ZVS turn-on of all the GaN FETs with proposed ZVS filter design.

The switching loss of the converter with the Legendre output filter is constant and higher than that of the ZVS filter as shown in Figure 4-18. This is due to the lack of ZVS turn-on of topside MOSFETs in the case of the Legendre filter. For duty cycle ranges from 0.44 to 0.6 and from 0.85 to 0.95, there is no negative current through the

ZVS inductor (no ZVS turn-on of top MOSFET) and the converter's switching loss with ZVS filter is the same as that of the case with Legendre filter. But, the overall switching loss of the converter is less using the ZVS output filter as shown in Figure 4-18. Moreover, the proposed ZVS filter design provides current self-balancing among the phases. Therefore ZVS filter is a better option for multi-phase high bandwidth ET applications.

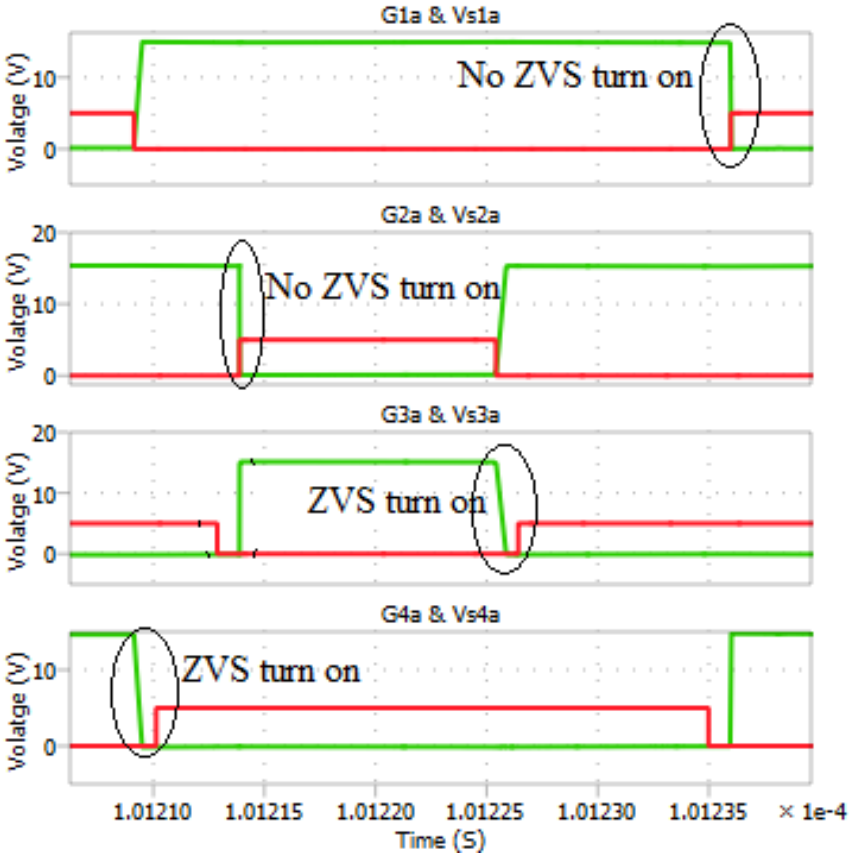


Figure 4-17: Lack of ZVS turn-on of high-side GaN FETs with Legendre filter design.

The output voltage of the converter with Legendre and ZVS filter designs while tracking a 20 MHz bandwidth, 4G LTE envelope signal is shown in Figure 4-19 and

Figure 4-20 respectively. For a device switching frequency of 25 MHz, the switch node voltage of each phase is switching at 50 MHz and the total current I_T has an effective ripple frequency of 100 MHz.

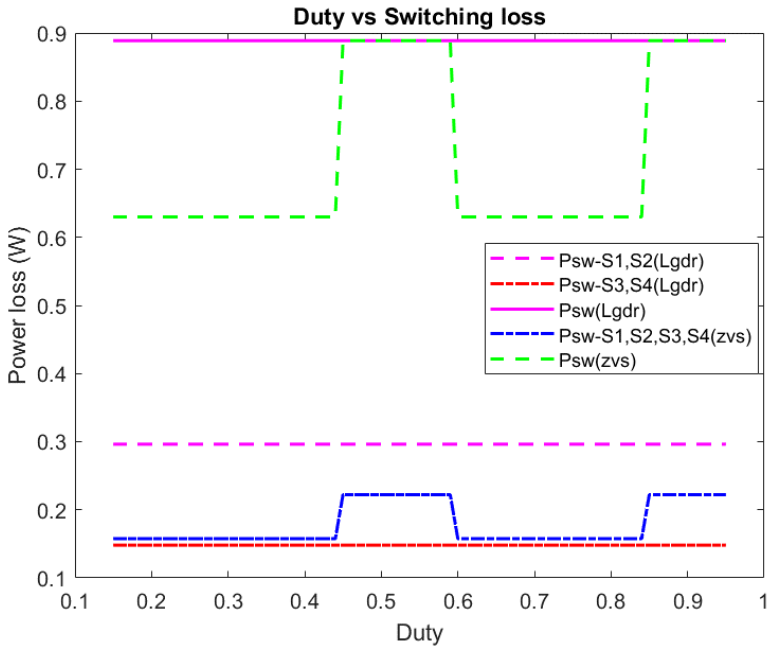


Figure 4-18: Switching loss comparison of the proposed two-phase three-level buck converter with ZVS and Legendre output filters.

This ripple frequency is five times the target maximum bandwidth of 20 MHz and allows the accurate tracking of the envelope signal. The converter output voltage varies from 4 V to 28 V when supplied by a 30 V DC input source. It is noticed that the two-phase three-level converter with the ZVS output filter has slightly better tracking capability when compared with the Legendre output filter.

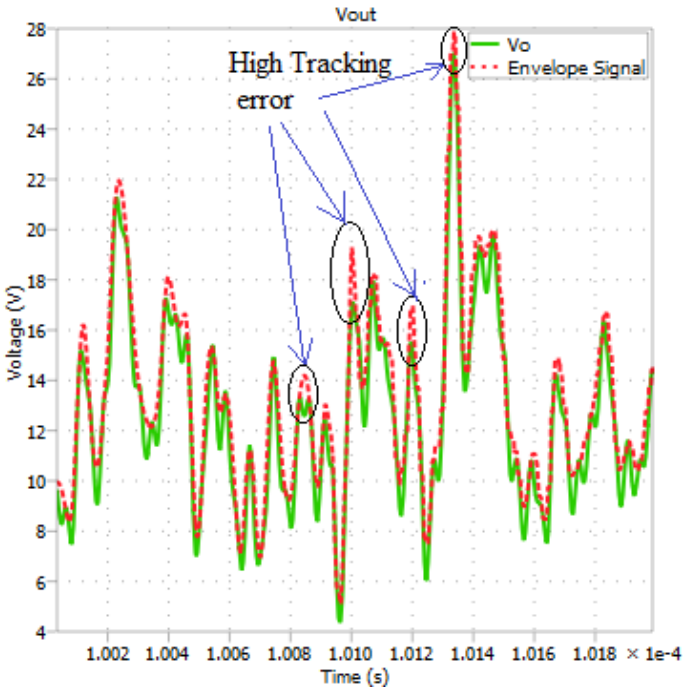


Figure 4-19: Output voltage of the two-phase three-level buck converter with Legendre output filter tracking a 20 MHz bandwidth 4G LTE envelope signal.

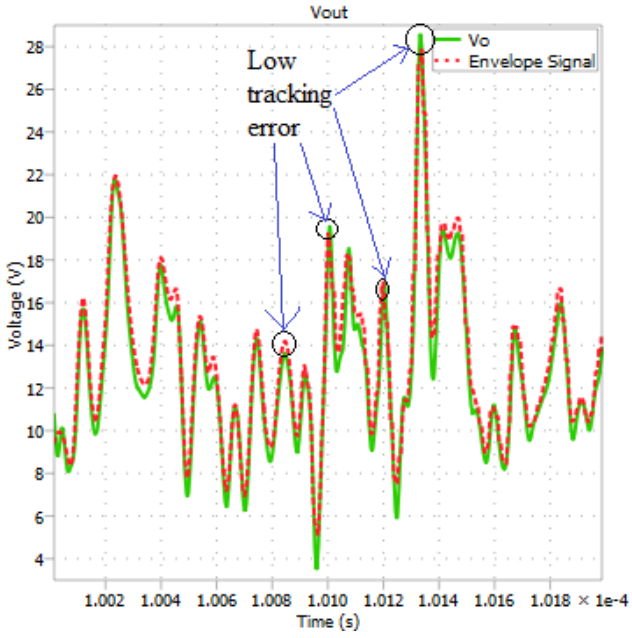


Figure 4-20: Output voltage of the two-phase three-level buck converter with ZVS output filter tracking a 20 MHz bandwidth 4G LTE envelope signal.

4.6.2 Comparison with Conventional Two-Level Counterpart

The switching loss (including gate drive loss) and conduction loss separation along with the total loss of the proposed two-phase three-level buck converter are compared with its equivalent four-phase conventional buck converter with the same power amplifier load (modeled as constant load resistance [83]) as shown in Figure 4-21. The switching (mostly during turn-off) loss of the proposed converter is far lower than the switching loss of the conventional two-level converter. Moreover, the switching loss is constant for most of the duty cycle range except during a specific part, where the ZVS turn-on of top-side MOSFETs is lost.

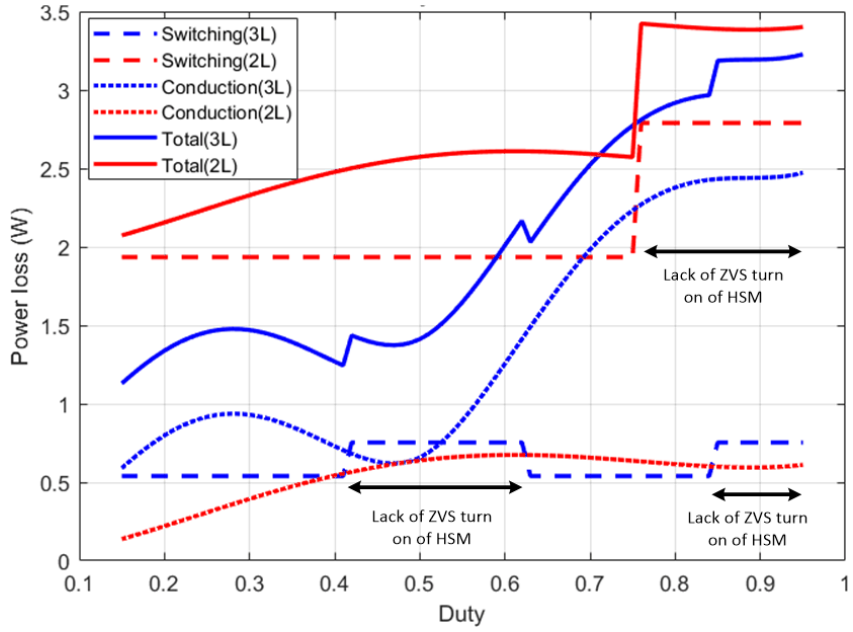


Figure 4-21: Switching loss and conduction loss comparison of the proposed three-level converter with its equivalent two-level converter at the designed maximum power rating of 115 W.

In contrast, the conduction loss of the proposed converter is slightly above its conventional counterpart. Further, the conduction loss is mostly increasing with an increase in the duty cycle. In conclusion, the total loss of both the converters increases with the rise in the duty cycle, but the overall loss of the proposed converter is less than its equivalent two-level buck converter. Figure 4-22 shows the efficiency comparison of both proposed and conventional converters with EPC8004 and EPC8009 GaN MOSFETs as switching devices. The proposed converter with EPC8004 ($R_{dson} = 110m\Omega$) exhibited slightly better efficiency than with EPC8009 ($R_{dson} = 130m\Omega$) devices, due to the less on-state resistance of the former. In contrast, the conventional two-level equivalent demonstrated a slightly better efficiency with EPC8009 ($C_{oss} = 19pF$) as a switching device due to its less drain to source capacitance when compared with EPC8004 ($C_{oss} = 23pF$). The overall efficiency of the proposed design is greater than the conventional buck design. Moreover, there is a drop in the efficiency over a certain range of the output voltage due to partial ZVS turn-on of the GaN MOSFETs. The proposed converter has recorded a peak efficiency of 97.5 % at 115 W and the total average efficiency is 94.5 % at 26 W of average power. Also, the efficiency of the proposed design is above 90 % for most of the operating range and has a PAPR of 10 dB.

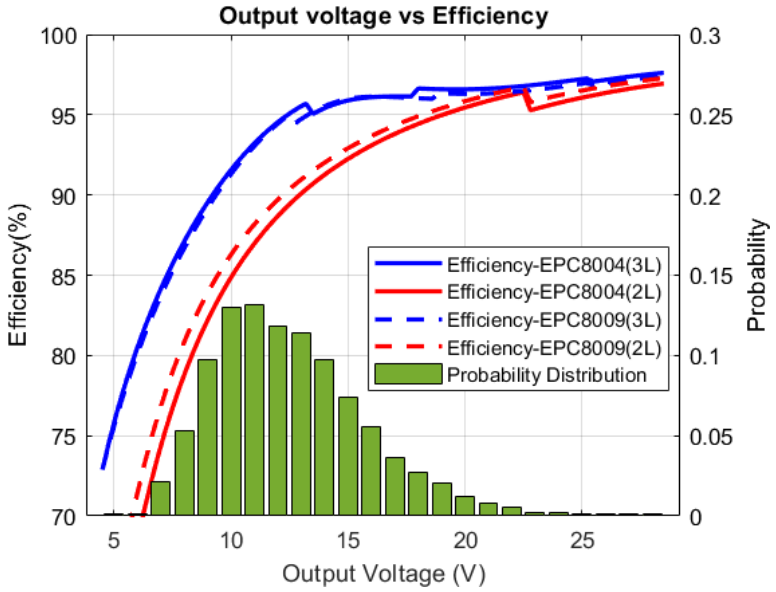


Figure 4-22: Output voltage Vs Efficiency of the two-phase three-level buck and its equivalent conventional two-level buck.

4.7 **Summary**

In this chapter, a multi-phase interleaved buck converter concept was adopted to flying capacitor-based three-level buck converter to meet the high power levels and bandwidth needs of the ET power supply. The design of a two-phase three-level buck converter for a higher bandwidth ET application was presented. Power loss models were developed to aid the optimal design of the converter. A ZVS low pass filter design was proposed to track a 20 MHz LTE envelope signal and also inherent phase current balancing in a multi-phase three-level buck. Power loss models and efficiency comparisons show that the proposed three-level buck converter has a better average power efficiency over the two-level buck option for the designed rating and PAPR. Simulation results were provided to validate the proposed ZVS concept and converter

design. Moreover, the proposed design is easily scalable for high-power ET applications and can achieve higher bandwidth and PAPR.

5. CASCADED SWITCHING CAPACITOR BASED MULTI-PHASE THREE-LEVEL BUCK CONVERTER FOR COMMUNICATION ENVELOPE TRACKING

5.1 Introduction

The FCTL buck converter needs active voltage balancing of the flying capacitor, and the complexity of the control scheme increases with switching frequency. At a high switching frequency of operation, the availability of control circuit parts is limited due to the increased bandwidth requirement and may contribute to the increased cost of the converter. The PCB layout complexity of the control circuit increases with the increase in switching frequency. Finally, the sensed voltage signal across the flying capacitor should be noise-free to have accurate control.

To overcome these issues a cascaded switching capacitor-based multi-phase three-level buck converter is proposed in this chapter. The low pass ZVS output filter design is adopted from Chapter 4 with slight modifications. A modified PWM scheme is proposed to maintain the linear relationship between the reference envelope signal and modulated output voltage. Due to this reason, the modified PWM scheme enables the easy adoption of the proposed converter to ET applications. The proposed converter has the following advantages.

- Elimination of active voltage control of switched-capacitor.
- ZVS turn on and inherent phase current balancing.

- Reduced device voltage stress and turn off switching loss.
- Higher output voltage than the DC input voltage.
- Reduced conduction loss when compared with other multilevel topologies.

5.2 Proposed Cascaded Switching Capacitor Based Three-Level Buck

The basic circuit diagram of the proposed multi-phase cascaded switching capacitor converter is shown in Figure 5-1.

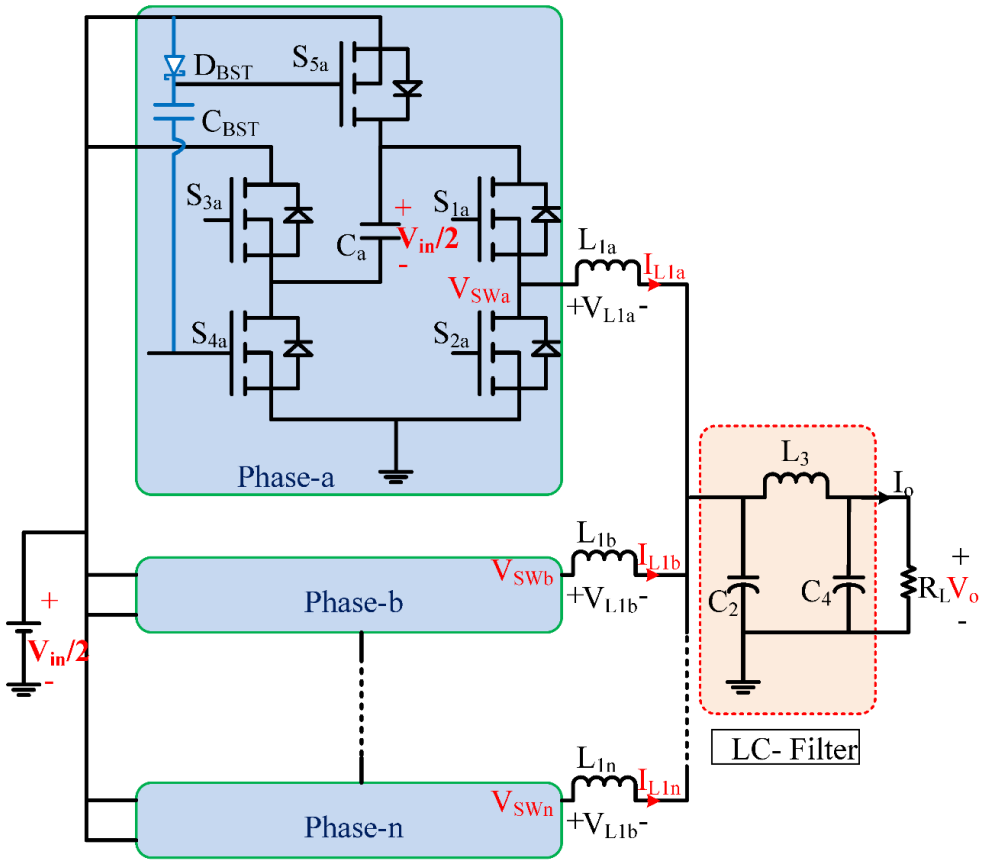


Figure 5-1: Cascaded switching capacitor-based multi-phase three-level buck converter.

Each phase consists of two half-bridges (HB) and one auxiliary switch to charge the cascaded switching capacitor C_x. (HB1: S_{1x}, S_{2x}, HB2: S_{3x}, S_{4x}, and auxiliary switch S_{5x}. Where $x = a, b, \text{---} n$). The two switches of each HB switch in complementary with proper dead time. Two high-frequency half-bridge gate driver ICs drive the gates of these two half-bridges and the gate of switch S_{5x} is driven by the same gate signal of switch S_{4x}. For the same output voltage, the input DC voltage required for the proposed cascaded switching capacitor-based converter is half of the input voltage required for traditional two-level and FCTL buck converters.

This section describes the various operating modes of the converter. The operation of one phase of the proposed multi-phase converter is explained the remaining phases also follow the same principle but the gate pulses are phase-shifted by $360^{\circ}/N$ with respect to their neighboring phases (Where N is the number of phases). For simplicity and comparison with the existing three-level buck converter, the input voltage is considered as $V_{in}/2$ in this work. The proposed converter has four operating modes over the range of duty cycle of $0 < D < 1.0$. The circuit operation during these four modes is shown in Figure 5-2, Figure 5-3 and explained in this section.

Mode-1 ($0 < D < 0.5$ and S1 is ON): For duty cycle D below 0.5, S_3 is always off and S_4, S_5 are always in conduction as shown in Figure 5-2. Switches S_1 and S_2 operate in a complementary manner and the switch node voltage switches between 0 and $V_{in}/2$ as shown in Figure 5-4. During mode-1 of operation, S_1 is in conduction and the load current is supplied by the parallel combination of switching capacitor and input

voltage source as shown in Figure 5-2(a). Therefore the switch node voltage is equal to input voltage $V_{in.}/2$. The switching capacitor discharges to load through S_1 until the end of mode-1, where S_1 is turned off and S_2 is turned on.

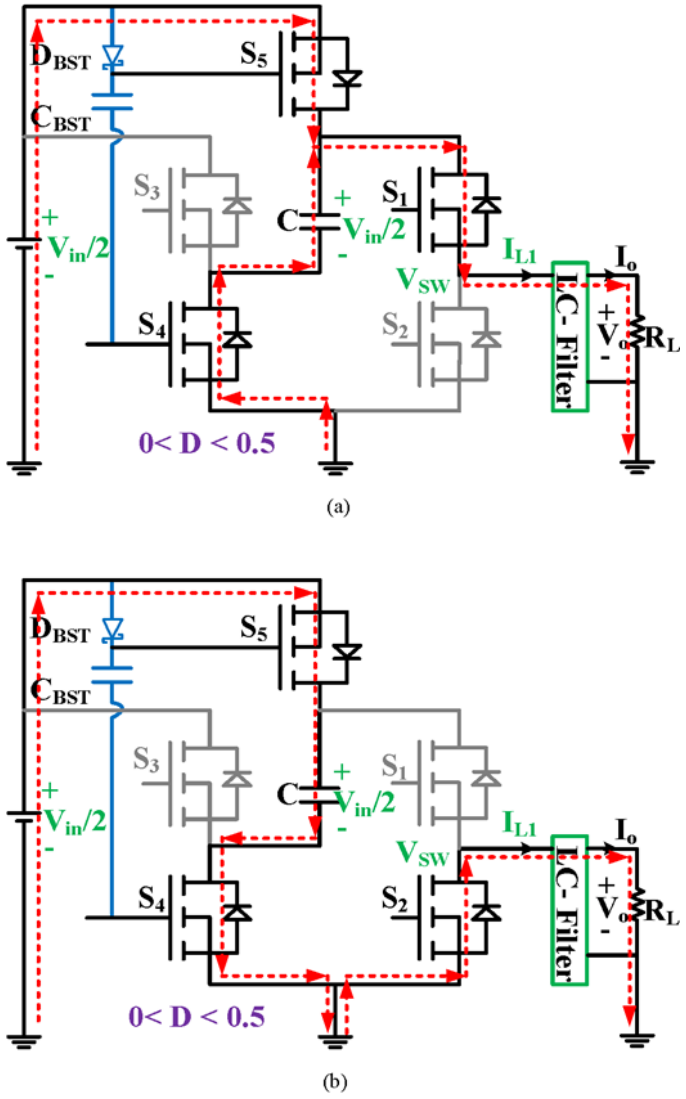


Figure 5-2: Operation of the converter during $0 < D < 0.5$. (a) The switching capacitor is discharging through switches S_1 and S_4. (b) Switching capacitor is charging through switches S_1 and S_4 and inductor current freewheeling through S_2.

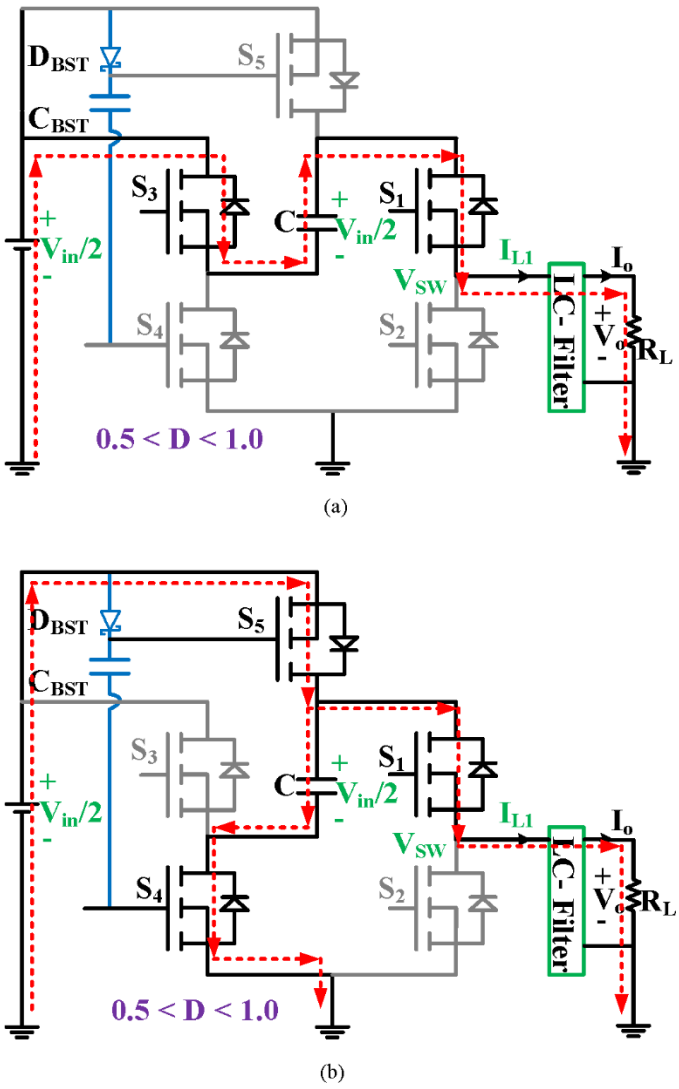


Figure 5-3: Operation of the converter during $0.5 < D < 1.0$. (a) The switching capacitor is discharging in series with the input voltage source and through switches S_1 *and* S_3. (b) The switching capacitor is charging through switches S_4 and S_5.

Mode-2 ($0 < D < 0.5$ and S_2 is ON): During Mode-2 of operation, S_1 is turned-off and S_2 is turned on. The switching capacitor charges through S_5 from the input voltage source as shown in Figure 5-2(b). The inductor current freewheels through S_2 and the switch node voltage is 0 V. The model switching waveforms are shown in Figure

5-4. At the end of mode-2, switch S_2 is turned off and S_1 is turned on. For duty cycle below 0.5, the converter operates in mode-1 and mode-2 only.

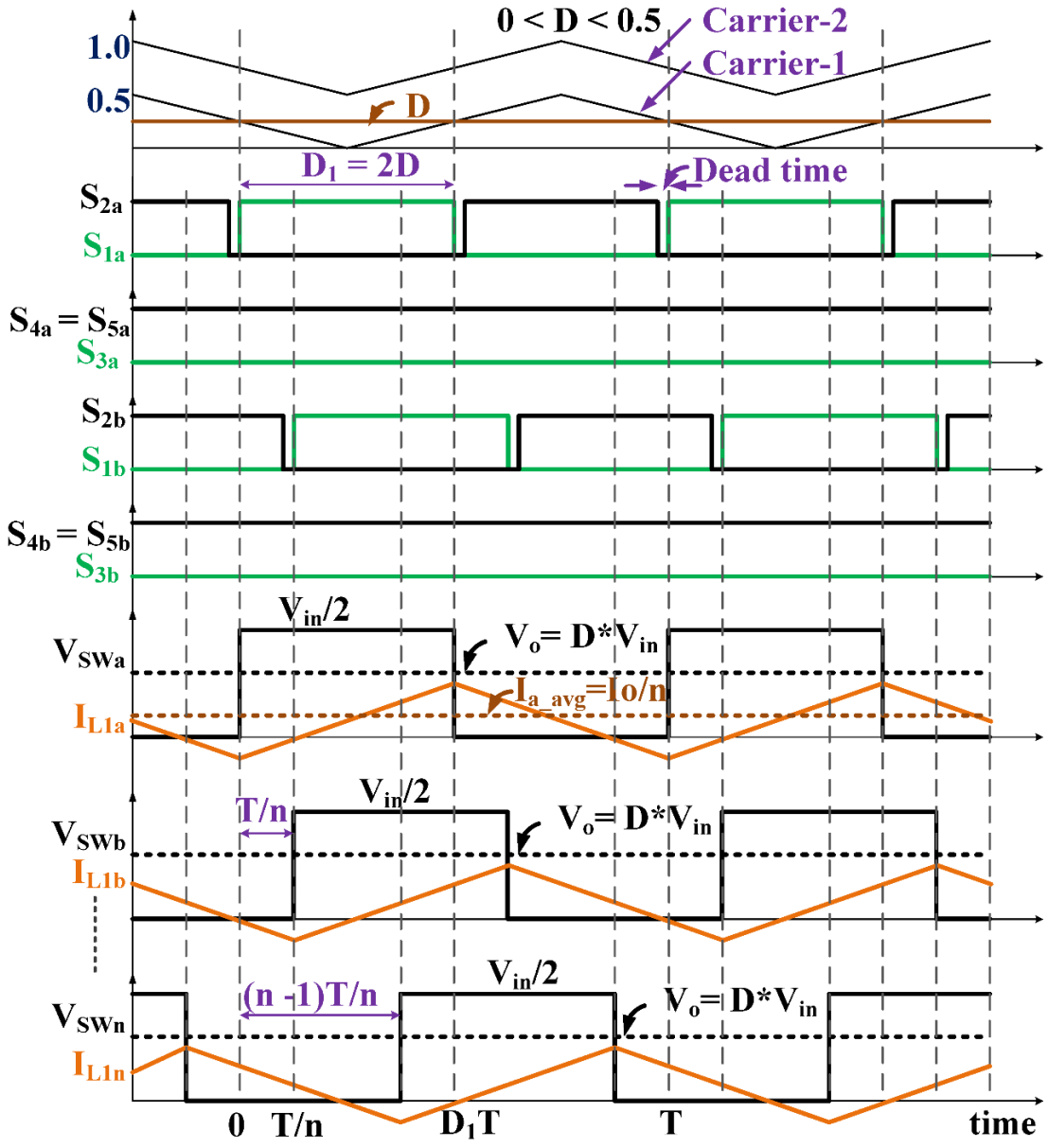


Figure 5-4: Proposed Modulation scheme and model switching waveforms for the duty cycle in the range $0 < D < 0.5$.

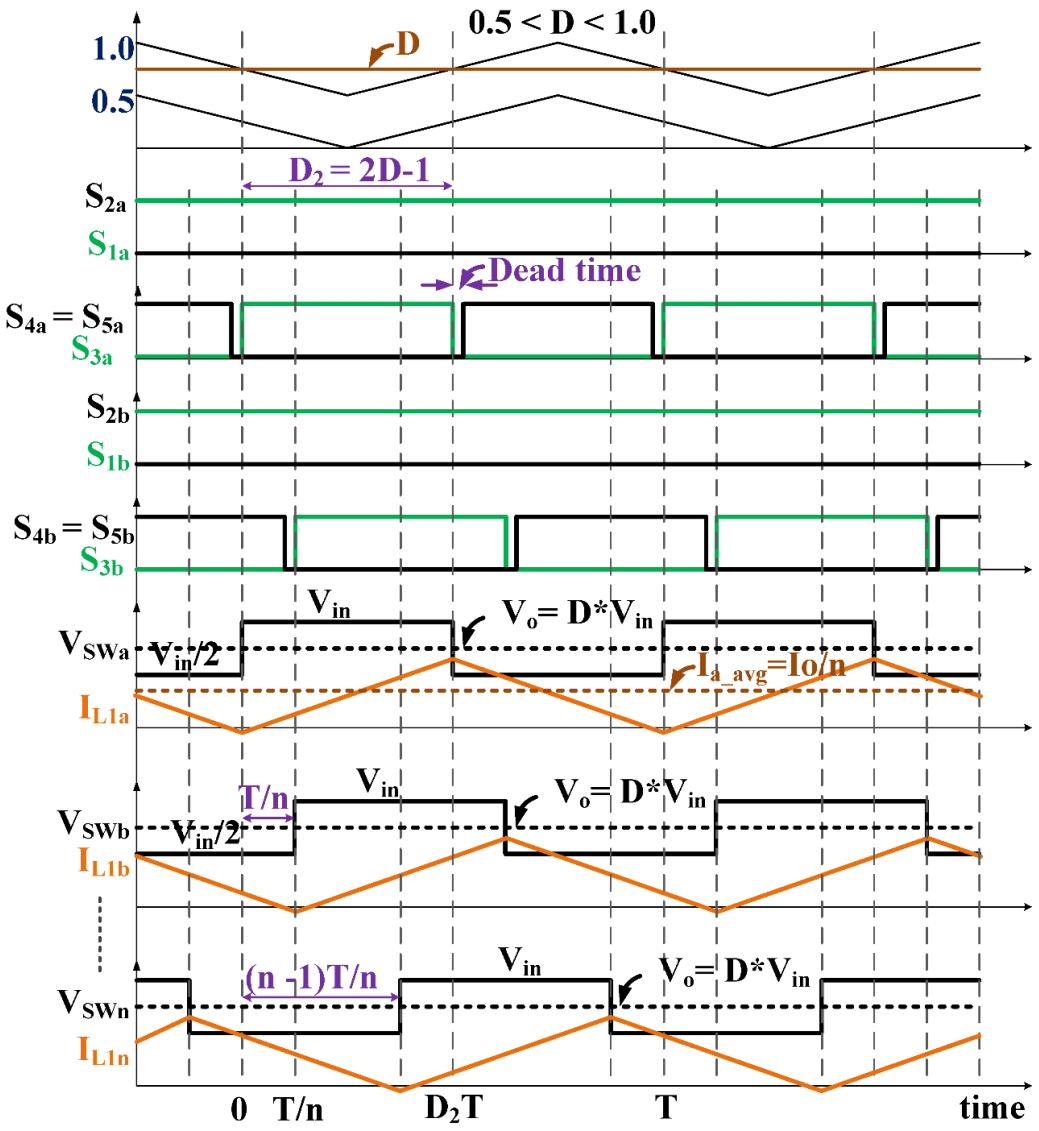


Figure 5-5: Proposed Modulation scheme and model switching waveforms for the duty cycle in the range of 0.5 < *D* < 1.0.

Mode-3 (0.5 < *D* < 1.0 and S_3 is ON): When the duty cycle *D* is above 0.5, S_2 is always off and S_1 is always in conduction. Switches S_3 and S_4 operate in a complementary manner as shown in Figure 5-3 and the switch node voltage switches between $V_{in}/2$ and V_{in} as shown in Figure 5-5. Also, switch S_5 is driven by the same gate

signal as switch S_4 through a bootstrap circuit comprised of capacitor C_{BST} and diode D_{BST}. During mode-3 of operation, S_3 and S_1 are in conduction and the load current is supplied by the series combination of switching capacitor and input voltage source as shown in Figure 5-3(a). Hence, the switch node voltage is V_{in}, which is double the input DC voltage. The switching capacitor discharges to load through S_1 and S_3 until the end of mode-3, where S_3 is turned off and S_4, S_5 are turned on.

Mode-4 ($0.5 < D < 1.0$ and S_4 and S_5 are ON): During Mode-4 of operation, S_4 and S_5 are in conduction along with S_1. The load current and the capacitor charging current are supplied by the input voltage source through S_5 as shown in Figure 5-3(b). Hence the switch node voltage is $V_{in}/2$ as shown in Figure 5-5. The converter operates in mode-3 and mode-4 for a duty cycle greater than 0.5.

5.3 **ZVS Filter Design**

A ZVS low pass output filter is designed for the proposed three-level converter to smoothly track the reference envelope signal. To achieve ZVS operation, the inductor negative peak current should be less than zero at all load currents. At $L_1 = L_{1max}$ the inductor ripple current is equal to its static current. Here, L_{1max} for a single-phase cascaded three-level buck converter is derived as

$$L_{1max} = \min\left[\frac{V_{in}(1-D)(D-1/2)}{I_{L1} f_s}\right], \text{ for } 0.5 < D < 1.0. \qquad (5.1)$$

The inductor quasi-static current I_{L1} is approximately calculated as

$$I_{L1} = \frac{DV_{in}}{R_L}, \tag{5.2}$$

where I_{L1} is inductor static current, V_{in} is the input voltage, R_L is load resistance, D is duty cycle and f_s is the switching frequency. By Substituting (5.2), (5.1) can be further simplified in to

$$L_{1max} = \min\left[\frac{R_L(1-D)(D-1/2)/D}{f_s}\right]. \tag{5.3}$$

By choosing the ZVS filter inductor value as $L_1 < L_{1max}$, the remaining filter values can be designed by following the procedure provided in section 4.5.

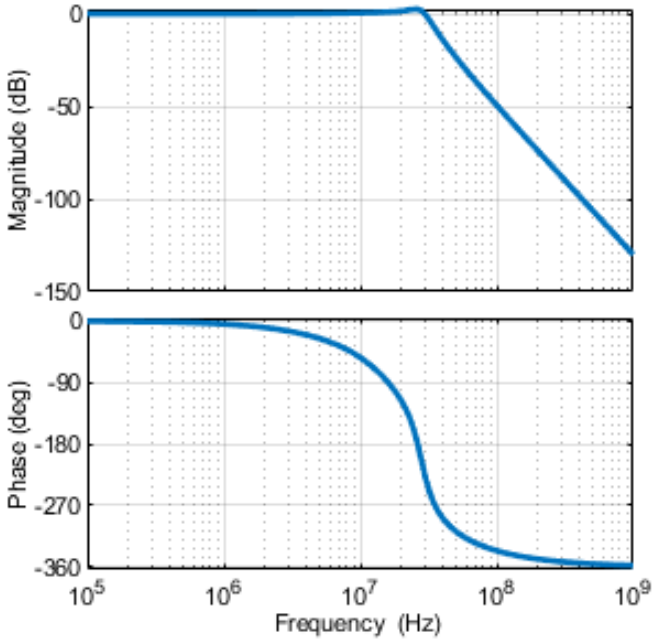


Figure 5-6: Magnitude and phase plot of fourth-order low pass ZVS output filter with 20 MHz bandwidth.

A fourth-order ZVS filter is designed for 20 MHz bandwidth and the list of filter values is provided in Table 5-1. Figure 5-6 shows the frequency response plots of the magnitude and phase of the ZVS filter. The magnitude cross-over frequency is slightly above 20 MHz and the phase delay varies up to 130° in the passband. The proposed ZVS filter also inherently balances the load current among all the phases of the converter. The ZVS turn on and current balancing mechanism are explained in Chapter 4.

Table 5-1: Filter component values.

Filter Type	R_L	L_1	C_2	L_3	C_4
ZVS	3.5 Ω	28 nH	4.6 nF	43 nH	1.5 nF

5.4 Simulation Results

The simulation of the proposed cascaded switching capacitor-based multi-phase three-level buck converter is carried out using PLECS to validate the concept. The PLECS simulation model is incorporated with the GaN FET on-state resistance ($R_{ds\text{-}on}$) and device output capacitance (C_{oss}) to account for the switching and conduction loss and voltage drop. The output voltage of the proposed cascaded switching capacitor-based four-phase three-level converter tracking 20 MHz 4G LTE envelope signal is shown in Figure 5-7. The ZVS filter inductor ensures the current balancing among the interleaved phases and ZVS turn-on of top-side switches as explained in Chapter 4. The instantaneous currents during one switching cycle are not balanced due to the various instantaneous duty cycle values of the interleaved phases. But the RMS value of the

currents throughout the tracking is balanced. The negative current flowing through the ZVS inductor L_{1a} allows the charge/discharge of the device output capacitance (C_{oss}) of each device during switching and enables ZVS turn-on of top side GaN FETs. The ZVS turn-on of the switch pairs S_1, S_2, and S_3, S_4 are shown in Figure 5-8 and Figure 5-9 respectively.

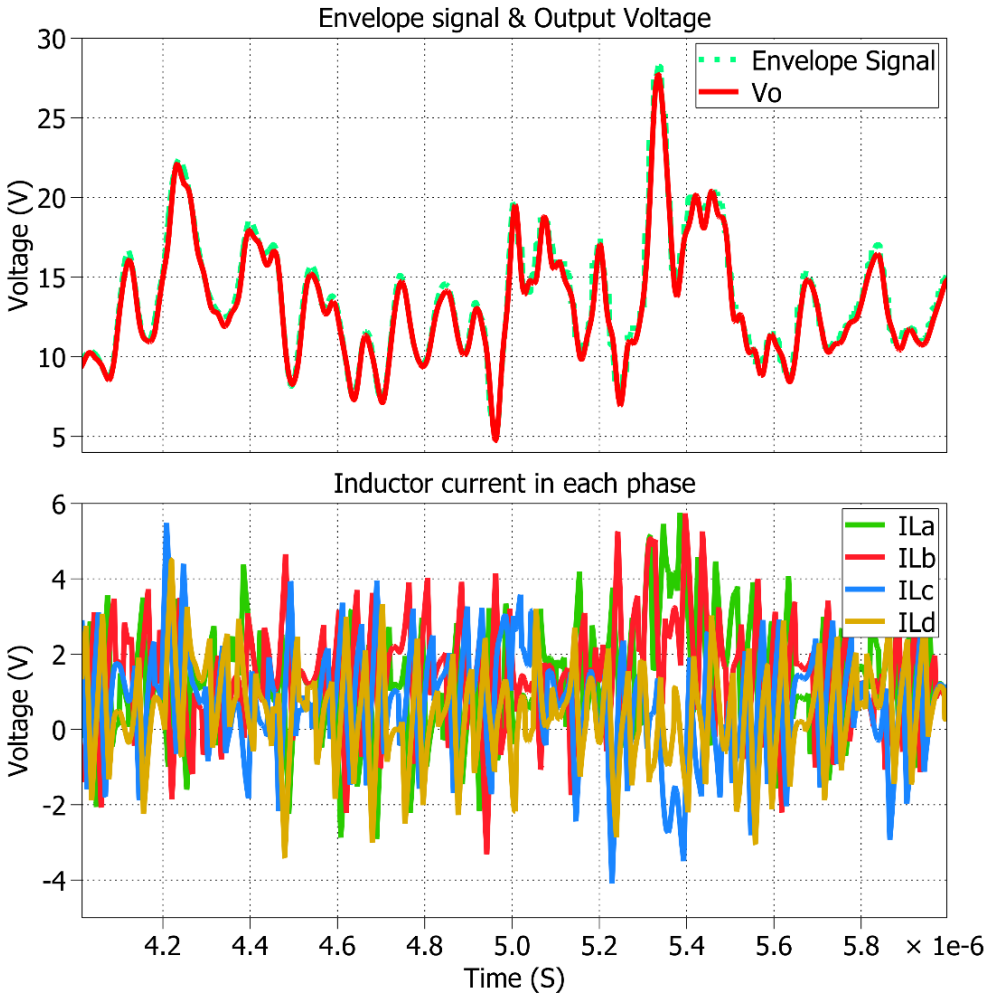


Figure 5-7: The output voltage of the proposed cascaded switching capacitor-based four-phase three-level converter tracking 20 MHz 4G LTE envelope signal.

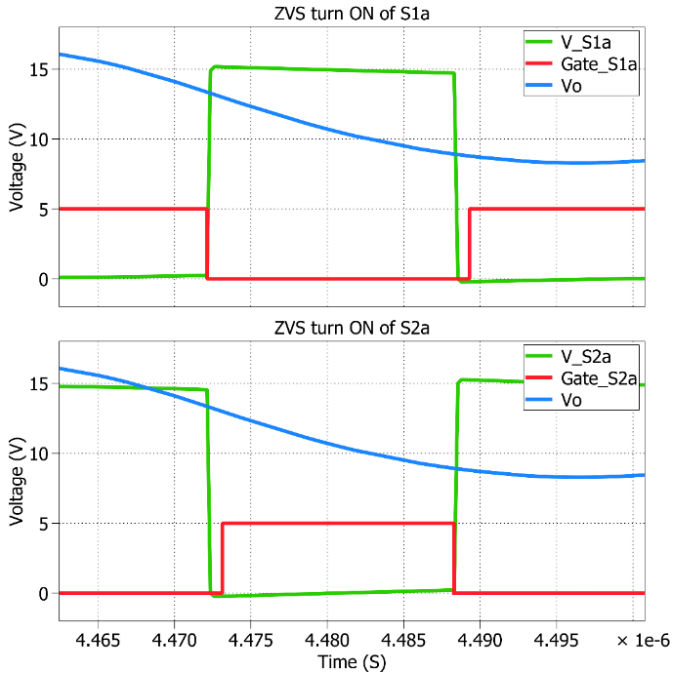


Figure 5-8: ZVS turn ON of switches S_{1a} and S_{2a} in phase-a.

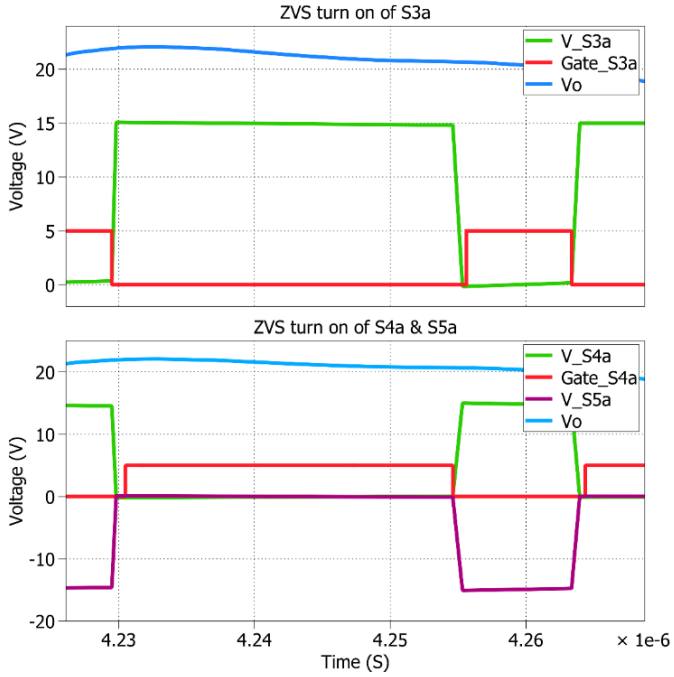


Figure 5-9: ZVS turn ON of switches S_{3a}, $S_{4a,}$ and S_{5a} in phase-a.

5.5 **Prototype and Experimental results**

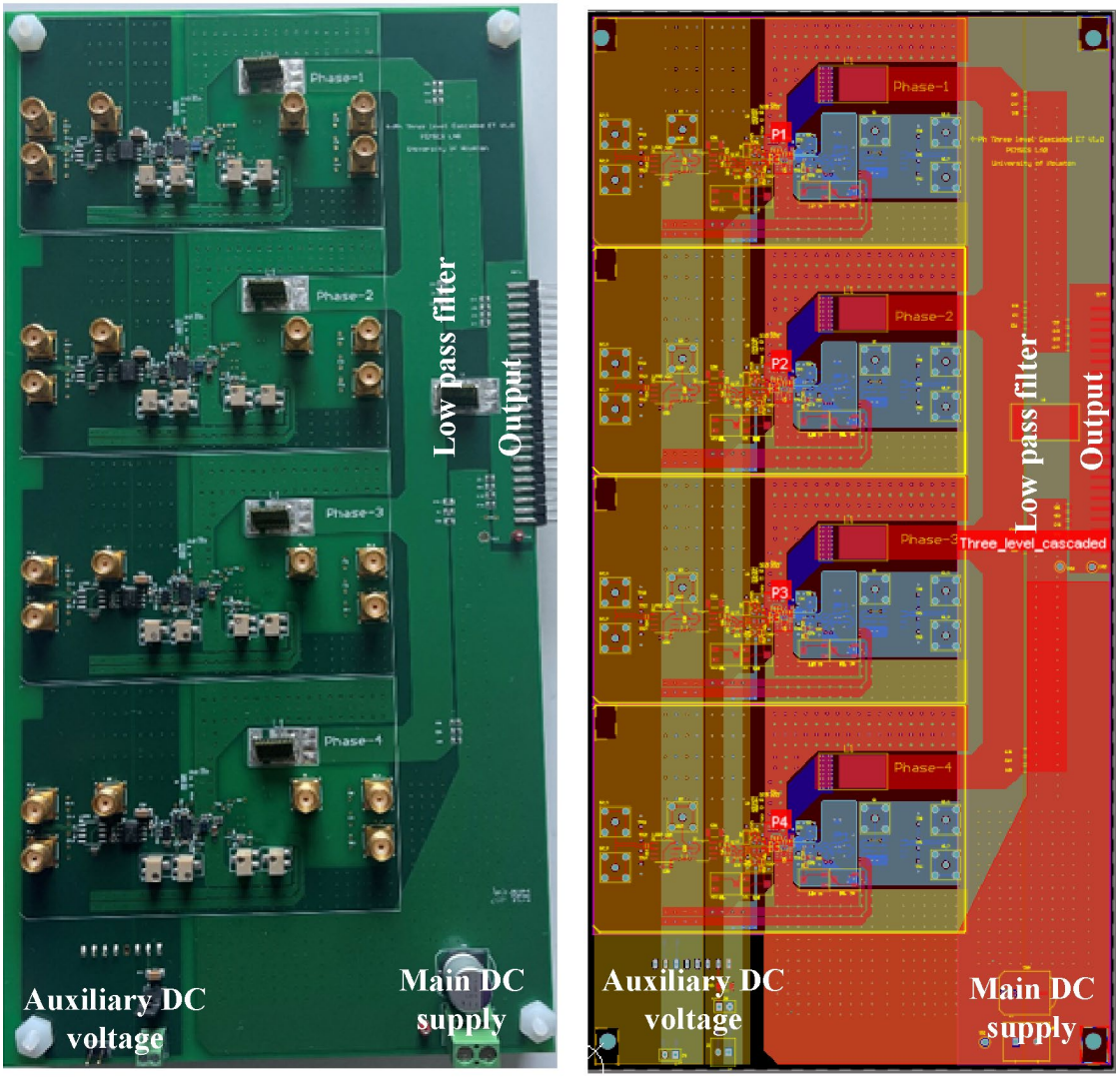
The proposed converter is designed to produce higher output voltages of up to 52 V when supplied with a DC voltage of up to 30 V. The converter is designed with a four-phase option and each phase can switch up to 25 MHz and the effective switching frequency ripple of 100 MHz in the four-phase mode of operation. The ZVS- LPF can be designed with a cross-over frequency of up to 20 MHz bandwidth to track the envelope signal.

5.5.1 Part selection

The voltage stress across all the devices is the same as that of input voltage ($V_{in}/2$) except for switch S_{2x}. The maximum voltage across the switch S_{2x} which is nothing but the switching node voltage (V_{swx}) can go up to twice the input DC voltage (V_{in}) as shown in Figure 5-5. Hence, the voltage rating of the switch S_{2x} is selected appropriately.

EPC8000 family GaN MOSFETs have a similar smaller footprint and low output capacitance. EPC8004, 40 V GaN MOSFETs [64] are used to realize the switches $S_{1x,}$ S_{3x}, $S_{4x,}$ S_{5x}, and EPC8009, 65 V, GaN MOSFETs [84] are used to realize the high voltage switches S_{2x}. All these switches are rated with 4 A continuous current and 7.5 A pulsed current ratings. The low on-state resistance and turn-on time of these devices are enabling factors of high switching frequencies and higher efficiency of the converter. Coil craft RF air-core inductors and X7R multi-layer ceramic capacitors of 0402 and 0603 sizes are used as switching capacitors and output filter capacitors.

LMG1210 high-frequency half-bridge gate driver IC with the bootstrap circuit is used to drive each half-bridge of the proposed multi-phase converter.



(a) (b)

Figure 5-10: (a) Experimental prototype and (b) PCB layout of the proposed cascaded switching converter.

The internal LDOs of LMG 1210 regulates the gate voltages at 5 V. An isolated DC voltage regulator is used to generate the 3.3 V output from the auxiliary dc supply voltage to the low voltage differential signal (LVDS) and isolator ICs.

5.5.2 PCB layout

The experimental prototype and its PCB layout of the proposed cascaded switching converter are shown in Figure 5-10. The zoomed details are marked in Figure 5-11. The MOSFETs and gate driver ICs are located on both sides of the PCB to minimize the effect of parasitic inductance on the board layout.

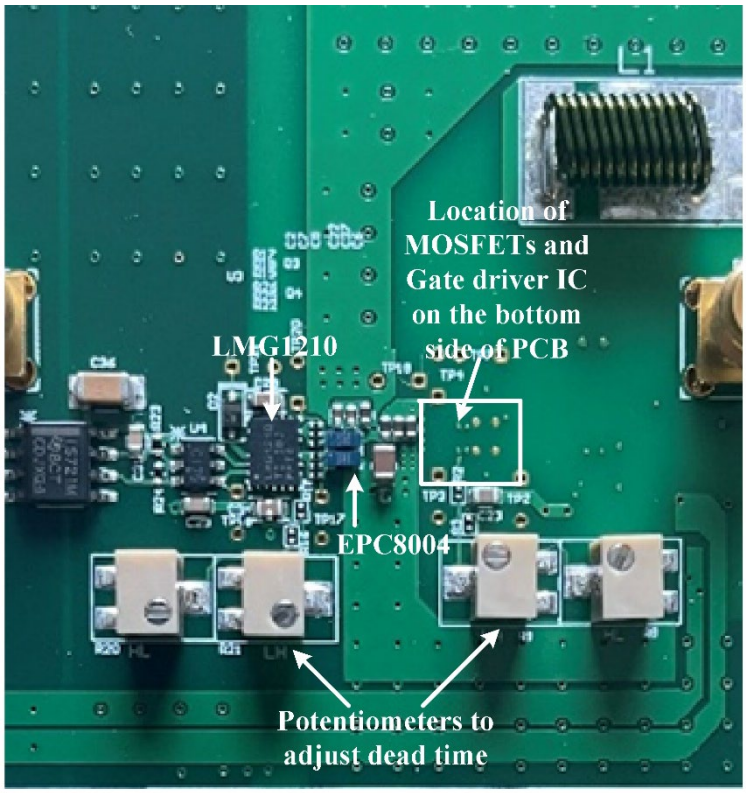


Figure 5-11: Close-up details for one phase of the proposed converter prototype.

The potentiometers are placed on the top side for easy access to adjust the turn on and turn off dead times of the MOSFETs. Figure 5-12 and Figure 5-13 show the top side of the PCB where the GaN FETs and the corresponding gate driver ICs are placed.

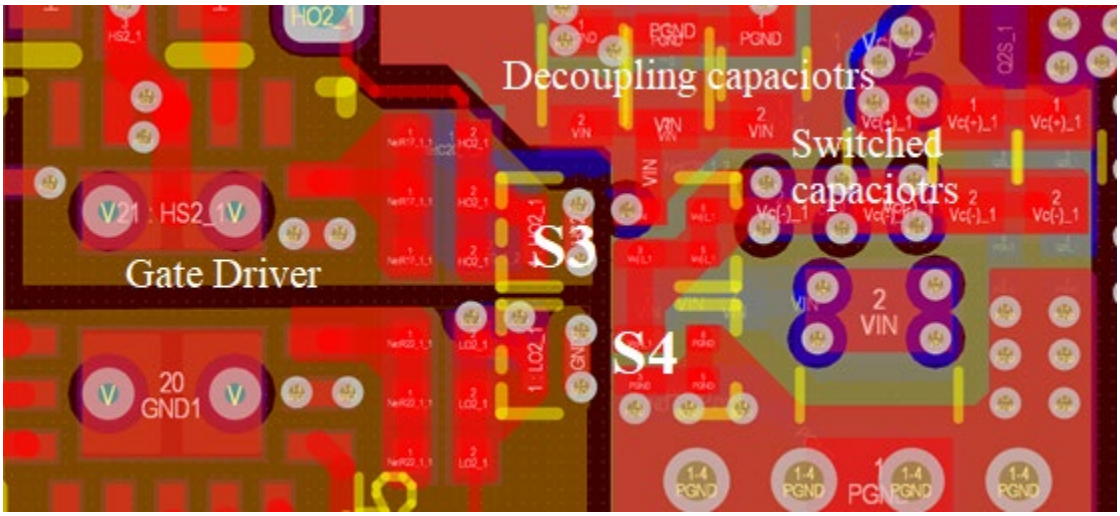


Figure 5-12: PCB routing and part placement of switches S3, S4, and their Gate driver IC along with input decoupling and cascaded switching capacitors on the top side of the PCB.

The footprint and the terminals of the EPC8000 family GaN FET are shown in Figure 5-14. The Gan FETs *S3, S4,* input DC link capacitors, and switched capacitors are placed closely on the topside of the PCB. The auxiliary switch S5 and its gate bootstrap diode $D_{BST,}$ switches *S1, S2*, and their corresponding gate driver IC are placed on the bottom side as indicated in Figure 5-13. The input DC voltage and ground return paths are routed in the adjacent layers to minimize the power loop stray inductance. The input decoupling capacitors and the cascaded switching capacitors are placed on both sides of PCB and the power ground return planes are routed in the inner two layers to minimize the commutation loop inductance for both the half-bridges. Furthermore, the

gate signal and source return paths are routed in the adjacent layers using micro-vias to minimize the influence of gate loop parasitic inductance.

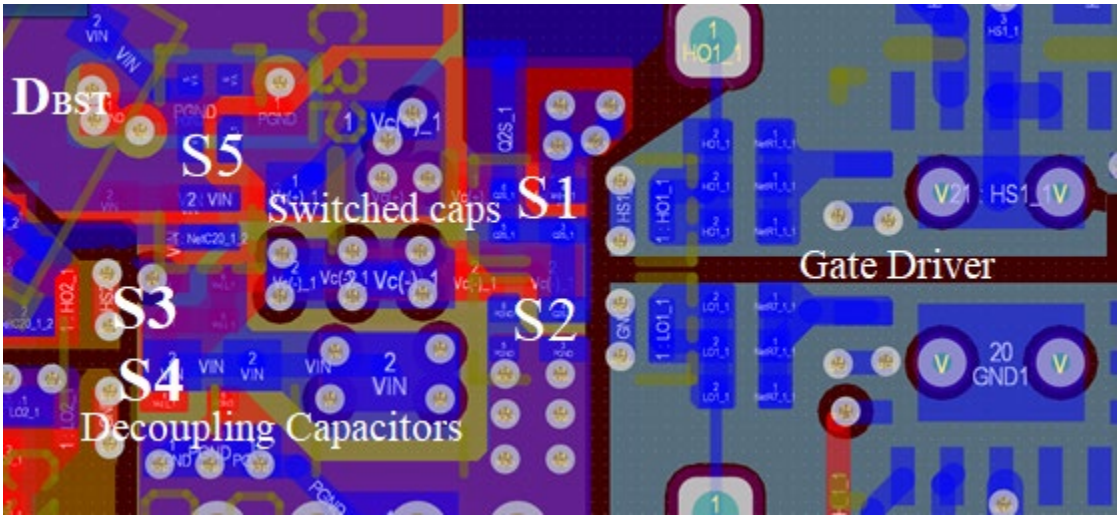


Figure 5-13: PCB routing and part placement of switch *S5* and its gate bootstrap diode $D_{BST,}$ switches *S1, S2*, and their Gate driver IC along with input decoupling and cascaded switching capacitors on the bottom side of the PCB.

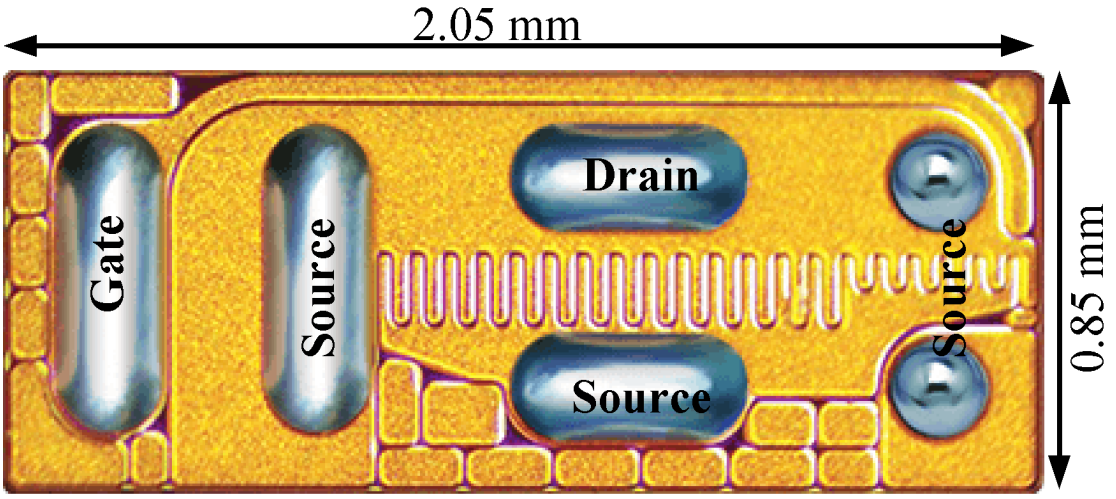


Figure 5-14: EPC8000 family of GaN MOSFET.

5.5.3 *Experimental Results*

The proposed cascaded switching converter is tested under a two-phase interleaved operating mode. Figure 5-15 and Figure 5-16 show the converter switch node voltages at duty cycle 0.3 when supplied with the input voltages of 15 V and 24 V respectively.

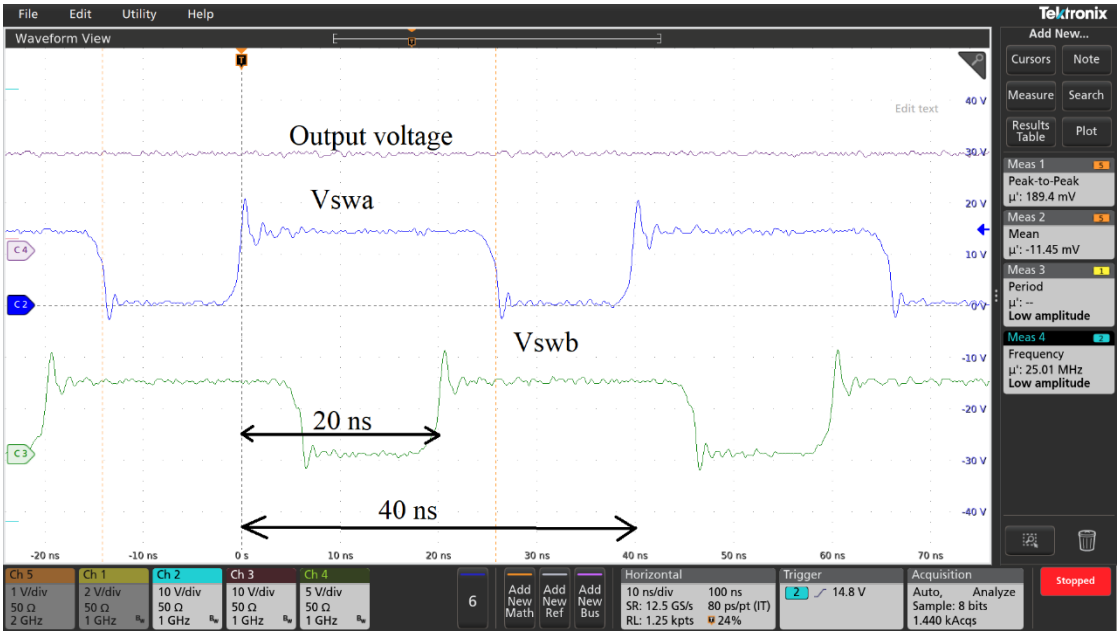


Figure 5-15: Switch node voltages and output voltage of the prototype at 25 MHz switching frequency, and at duty cycle D= 0.3 when supplied with 15 V DC input voltage. The effective duty cycle of the switch node voltage is ($D_1 = 2D$) 0.6 and switches between 0 V and 15 V.

The switch node voltages of the two phases are interleaved by an angle of 180° (20 ns) and the switching frequency is 25 MHz. For a duty cycle less than 0.5, the switch node voltage switches between 0 V and input voltage with an effective duty cycle of $D_1 = 2D$. For the converter duty cycle of 0.3, the switch node voltages shown in Figure 5-15 and Figure 5-16 have an effective duty cycle of 0.6.

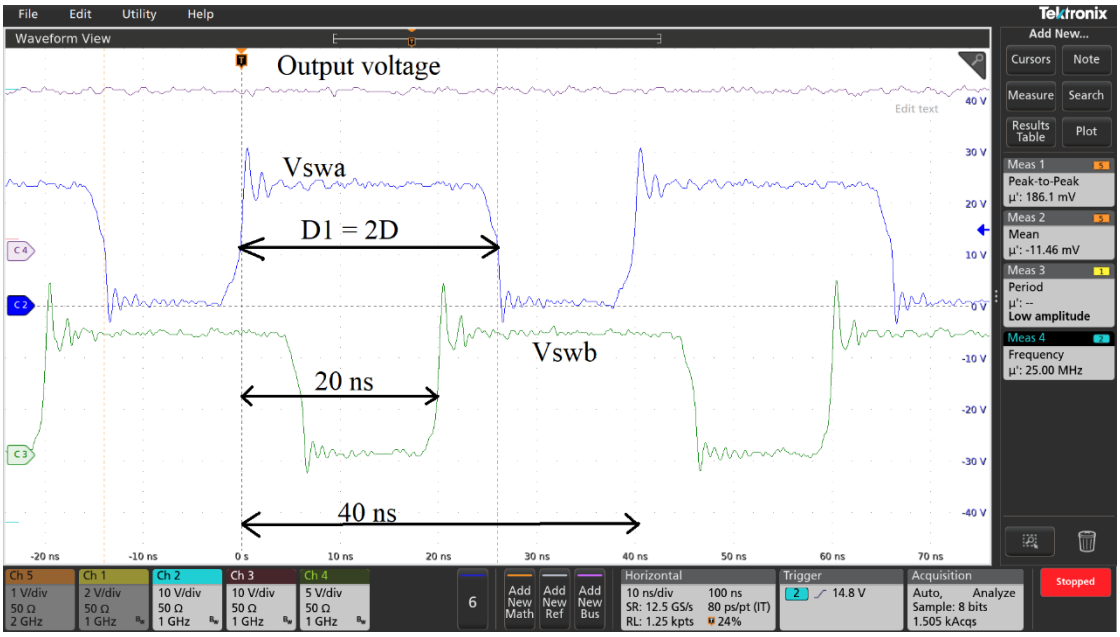


Figure 5-16: Switch node voltages and output voltage of the prototype at 25 MHz switching frequency, and at duty cycle $D = 0.3$ when supplied with 24 V DC input voltage. The effective duty cycle of the switch node voltage is ($D1 = 2D$) 0.6 and switches between 0 V and 24 V.

For a duty cycle value of above 0.5, the switch node voltages of the converter switch between the input voltage and twice the input voltage. It is possible because the cascaded switching capacitor discharges in series with the input voltage source for duty cycle values of greater than 0.5. Hence tracking of higher output voltages than the input DC voltage is possible with the proposed converter. Figure 5-17 and Figure 5-18 show the converter switch node voltages at duty cycle 0.7 when supplied with the input voltages of 15 V and 24 V respectively. The switch node voltages of the two phases are interleaved by an angle of 180° (20 ns) at the device switching frequency of 25 MHz. For a converter duty cycle value of above 0.5, the switch node voltages have an effective

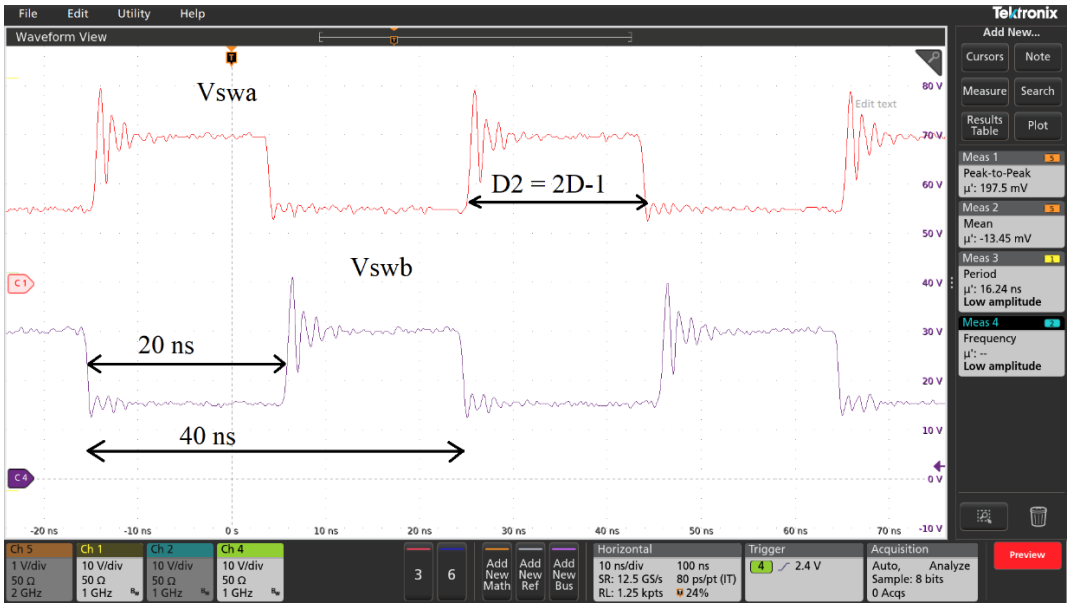


Figure 5-17: Switch node voltages at 25 MHz switching frequency, and at duty cycle D= 0.7 when supplied with 15 V DC input voltage. The effective duty cycle of the switch node voltage is ($D2 = 2D - 1$) 0.4 and switches between 15 V and 30 V.

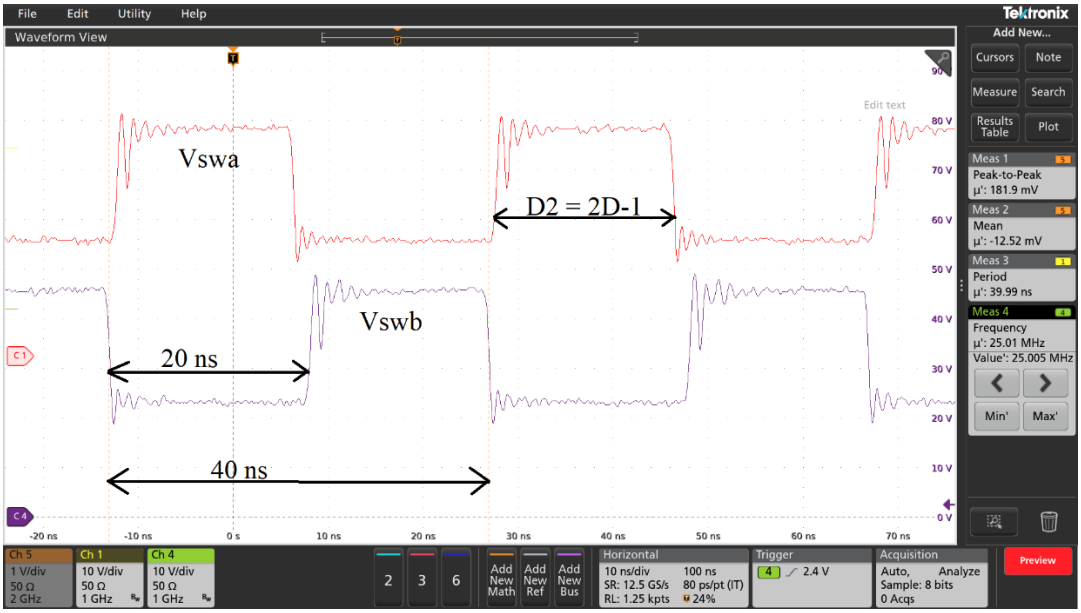


Figure 5-18: Switch node voltages at 25 MHz switching frequency, and at duty cycle D= 0.7 when supplied with 24 V DC input voltage. The effective duty cycle of the switch node voltage is ($D2 = 2D - 1$) 0.4 and switches between 24 V and 48 V.

duty cycle of $D_2 = 2D\text{-}1$. For the converter duty cycle of 0.7, the switch node voltages shown in Figure 5-17 and Figure 5-18 have an effective duty cycle of 0.4. Figure 5-19 shows the output voltage of the converter operating in one phase mode when supplied with 15 V input voltage. The highest bandwidth of the output voltage is limited at 5 MHz for the converter switching frequency of 25 MHz. The output voltage varies from 4 V to 26 V and the switch node voltage switches between either 0 and 15 V or 15 V and 30 V based on the reference envelope signal. The output voltage range can be further extended by increasing the input voltage. Figure 5-20 shows the output voltage varying from 6 V to 42 V when supplied with 24 V input voltage.

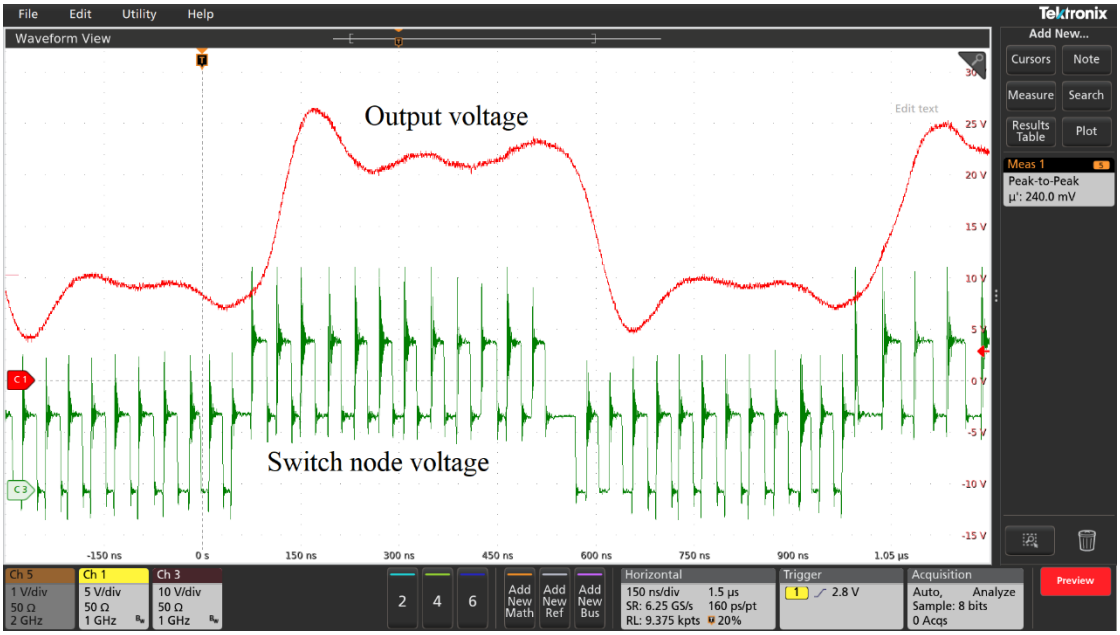


Figure 5-19: Switch node voltage and output voltage tracking 5 MHz band-limited envelope signal when supplied with 15 V input voltage.

The output voltage has the highest transient voltage change of 442 V/us when tracking a 5 MHz band-limited signal.

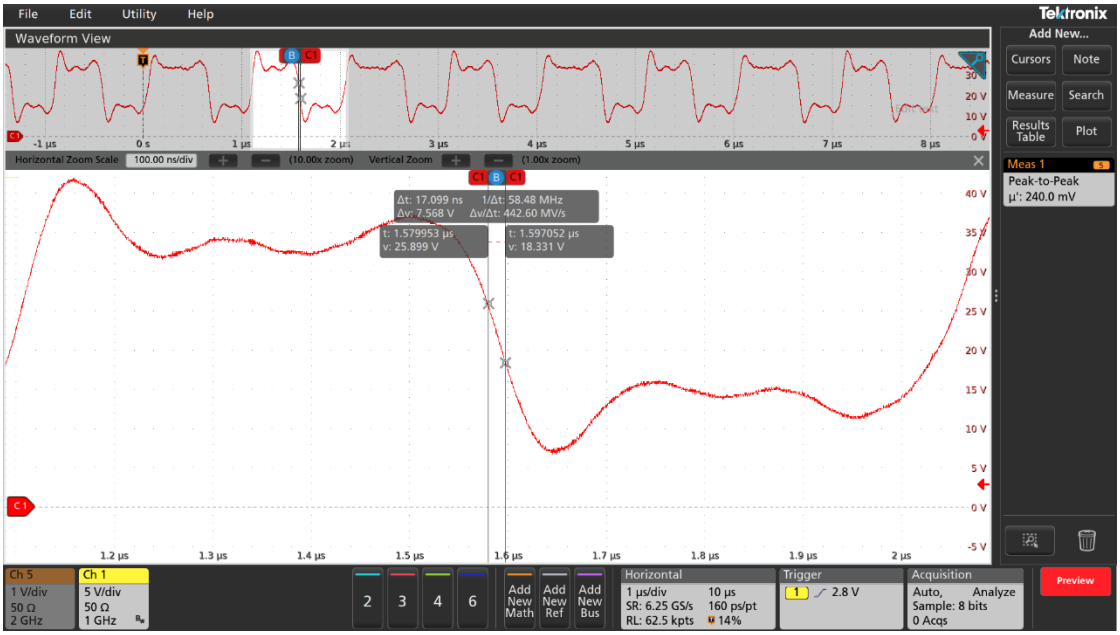


Figure 5-20: Output voltage tracking 5 MHz band-limited envelope signal when supplied with 24 V input voltage.

Figure 5-21 shows the comparison of analytical model-based efficiency curves of conventional two-level and proposed converters switching at 25 MHz to track the same envelope signal. The load resistance of both the converters is fixed at 3.5 Ω and the efficiency is plotted at various output voltages. EPC8000 family of GaN FETs are used to model the converter efficiency. The proposed converter has slightly better efficiency compared to the conventional buck converter due to the reduced switching loss associated with the former one. The proposed converter has a peak efficiency of 97.5 % and the efficiency stays flat above 90 % for most of the output voltage range, where the output voltage probability is higher.

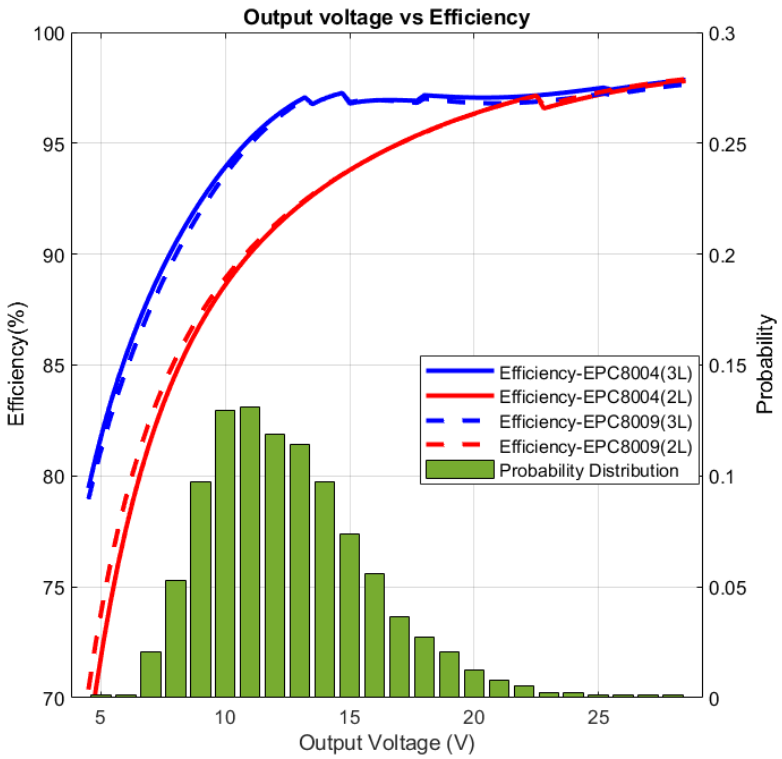


Figure 5-21: Efficiency comparison of the proposed cascaded switching capacitor-based four-phase three-level converter with the conventional four-phase two-level buck converter.

5.6 **Summary**

A cascaded switching capacitor-based multi-phase three-level converter is proposed in this chapter. The proposed cascaded switched capacitor three-level converter eliminated the need for active switched capacitor voltage control when compared with the conventional FCTL converter. The proposed modified PWM strategy provided linear input to output voltage relationship for ET. A hardware prototype was built and tested in the laboratory at 15 V and 24 V DC input voltage. Simulation and experimental results were provided to validate the proposed concept. The proposed converter has a better efficiency of above 95 % for most of the operating range when compared with

the two-level buck converter and a peak converter efficiency of 97.5 % is reported. The proposed converter concept is scalable for high voltage and high PAPR ET applications of up to 60 V by choosing appropriate voltage ratings for the GaN MOSFETs. Table 5-2 summarises various characteristics of 2-level, FCTL, and cascaded switching capacitor buck converters for high voltage ET application. Also, the 2-level buck converter is limited by the availability of higher voltage-rated GaN FETs that are capable of switching at high switching frequencies (multi-MHz).

Table 5-2: Comparision of proposed cascaded switching capacitor topology with FCTL and 2-level Buck converters for high voltage ET application.

Converter topology	**Switching loss**	**Conduction loss**	**Efficiency at higher input voltage**	**Hardware and layout complexity**	**Suitability for higher voltage ET**	**Scalability**
2-level Buck	High	Low	Good	Low	Low	Easy
FCTL Buck	Low	High	Better	High	Medium	Medium
Cascaded switching capacitor	Low	Medium	Best	Medium	High	Easy

6. SINGLE STAGE THREE-LEVEL INTERLEAVED BUCK CONVERTER WITH CURRENT SELF-BALANCING FOR IMPROVED POINT-OF-LOAD PERFORMANCE

6.1 Introduction

Breakthroughs in cyber-physical systems have created a vast demand for faster, more efficient micro-controllers and GPUs. This requires better point-of-load voltage regulators with reduced noise and faster dynamic response. Therefore, the performance of power converters needs to be improved to mitigate the issues with noise and power losses at high current values. Many researchers proposed a two-stage conversion-based topology for this purpose [62], [85]. With such an architecture, the efficiency of the conversion system is lower, especially during the light load operation. Moreover, the two-stage conversion results in lower power density.

To overcome these issues, industries are using a single-stage conversion approach [63]. A sine amplitude converter with zero voltage switching (ZVS) and zero current switchings (ZCS) is proposed in [79] which is a simple open-loop solution and the output voltage may not be well regulated under dynamic load conditions. A single-stage cascaded buck topology is introduced in [86] has design flexibility that can be scaled to the requirements of the load. But the overall efficiency of the converter is not significantly high. Since isolation is not required for POL conversion switched-capacitor converters have been studied and extensive research has been conducted in

this area [87]–[99]. It is also possible to interleave multiple buck converters [81], [82] with individual inner current loops and outer voltage control loops. To mitigate the switching losses of the two-level buck converter and reduce the magnetics size and voltage ripple, multi-level multiphase buck converters have been explored. But they typically require several current sensors, otherwise, it leads to severe inductor current unbalancing issues.

To address the above challenges, this section proposes a multi-phase three-level buck converter with an inherent phase current balancing scheme as a single-stage solution for 48 V to 5 V (or 3.3 V) voltage regulator applications. This design can be implemented by using low voltage rating discrete GaN devices. The major advantages of the proposed topology are the reduction of device voltage stress, ripple current, and inductor size and hence improved dynamic load response of the converter. Usage of the multiple current sensors to achieve phase current balancing is not economical and is a limiting factor for the multi-phase voltage regulator. Moreover accurate current sensing at high frequency has more challenges. This issue is addressed by a current self-balancing mechanism, thus eliminating the need for current sharing control loops. The current self-balancing in the phases along with the ZVS turn on is achieved by the proper design of the output filter inductor. Moreover, the issue of poor light load efficiency is addressed by proposing a variable switching frequency operation under light load conditions. The complete design is presented in the later sections of this chapter. The

proposed methods have the following benefits over conventional two-level synchronous buck converter.

- Single conversion stage from 48 V to 5 V/3.3 V leads to efficiency improvement
- The reduced voltage stress on the devices leads to less switching loss during turn-off.
- Reduced output voltage ripple and magnetics size and improved transient response
- Current self-balancing that further eliminates current sharing control loops
- Improved light load efficiency due to variable switching frequency operation

6.2 Single-stage Three-level Buck Converter

The power stage architecture of the four-phase three-level buck converter along with its ZVS second-order output filter is shown in Figure 6-1. The power stage operation of the three-level converter is described in this section. Each phase of the converter consists of four switches namely $S_{1x}, S_{2x}, S_{3x}, S_{4x}$, where $x = a, b, c,$ and d. The gate pulses to the top two devices, S_{1x}, S_{2x} are similar with a duty cycle D, and gate pulses to S_{2x} are delayed by $T/2$ (Here T is device switching period). The gate signals to switch pairs S_{1x}, S_{4x} and S_{2x}, S_{3x} is complementary to avoid the short circuit of the voltage source and flying capacitor. The switching waveforms of the single-phase three-level converter are shown in Figure 6-2. The node voltage V_{swx} switches between

the levels of 0 and $V_{in}/2$ for the duty cycle $0 < D < 0.5$, and switches between $V_{in}/2$ and V_{in} for $0.5 < D < 1.0$. Moreover, the frequency of the switch node voltage is twice the device switching frequency.

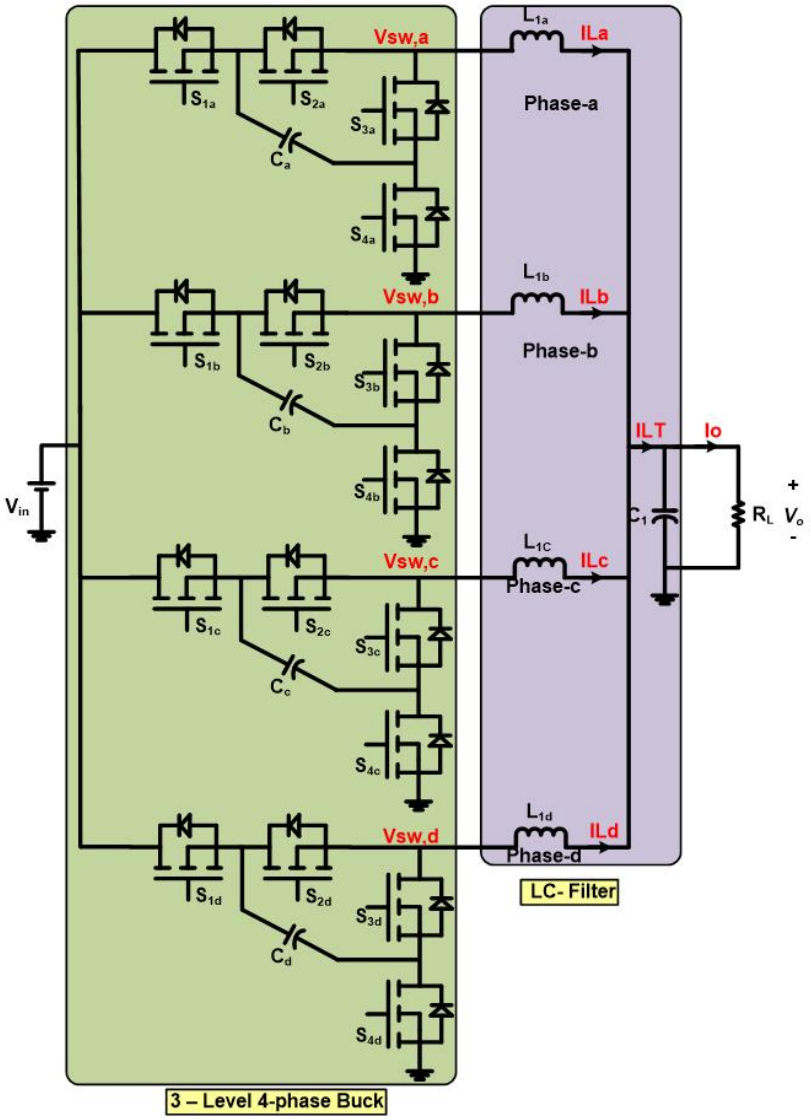


Figure 6-1: The power stage of the four-phase three-level interleaved buck converter.

This phenomenon reduces the size of the LC-filter and increases the open-loop bandwidth of the converter. The operating principle of the remaining phases is similar, switching at the same duty cycle. But the gate pulses of the corresponding switches are delayed by $T/2N$ (Where N is the number of phases) with respect to the adjacent phase for interleaved operation. The two bottom devices S_{1x}, S_{4x} operate in synchronous rectification mode, and hence continuous conduction mode of operation irrespective of the load current. The voltage across the flying capacitor is controlled at 24V and hence the device voltage stress is limited to half of the input voltage. Figure 6-3 shows the four-phase interleaved switch node voltages and inductor currents with a phase shift of $T/8$.

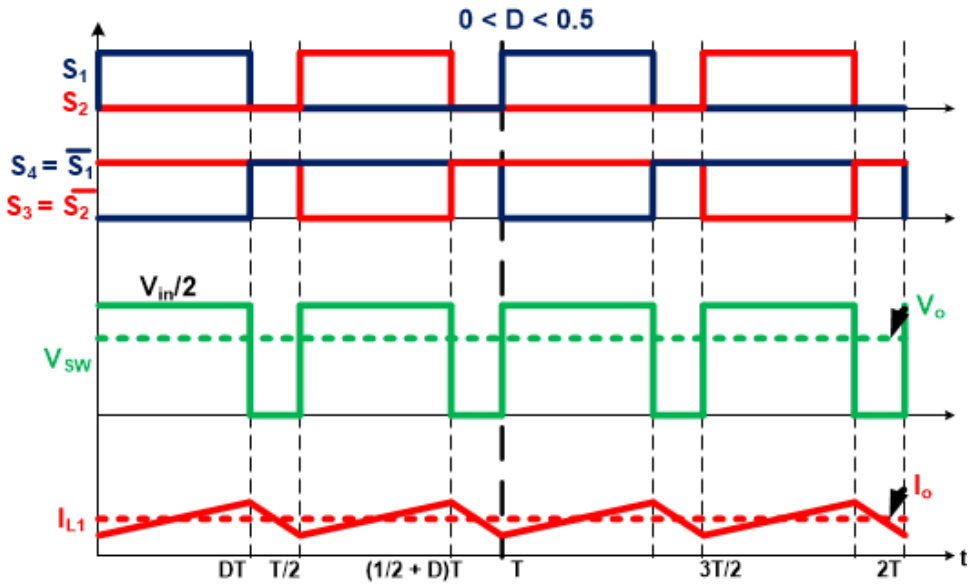


Figure 6-2: Basic switching waveforms of Single phase 3-level converter for $0 < D < 0.5$.

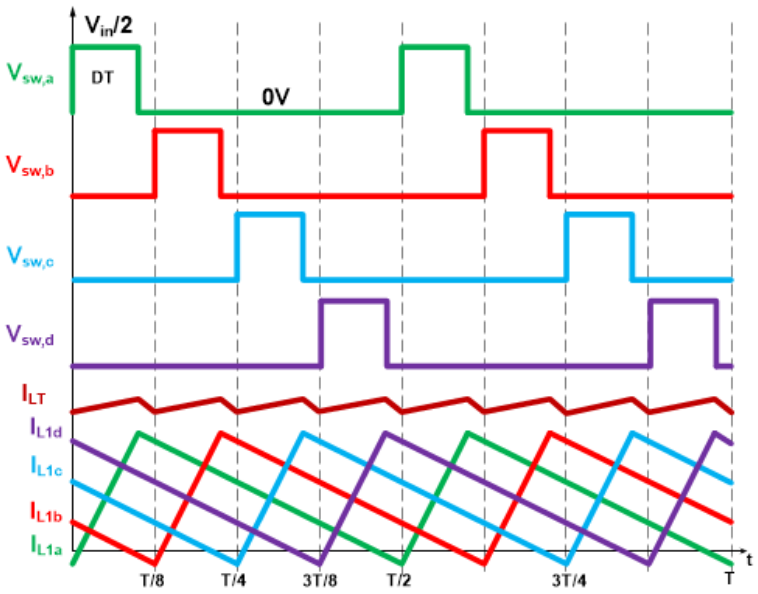


Figure 6-3: Switch node voltages and inductor currents of three-level four-phase interleaved buck converter.

6.3 **Converter Design**

The converter design, output voltage control loop, and proposed variable switching frequency operation are presented in this section.

6.3.1 Power Device Selection

The conduction losses are dominant for the converter due to the proposed inherent current balancing scheme. Therefore, a power switching device with less on-state resistance needs to be selected for better efficiency. EPC2023 30 V, 90 A GaN MOSFET has a very low on-state resistance of 1.45 $m\Omega$ is used as a power switching device [100]. EPC2024 GaN FET rated with 40 V and 90 A continuous current [101] can also be used to account for voltage overshoots. The number of phases cab be selected

based on the output power requirement and device current rating. A four-phase converter is designed for a maximum power rating of 800 W with each phase is rated for 200 W.

6.3.2 Inherent Current Balancing and Filter Inductor Design

Each three-level buck converter has two pairs of switches. The top two devices S_{1x} and S_{2x} (connects the inductor to input DC bus/capacitor positive terminal) are referred to as High Side MOSFETs (HSM) and the bottom two devices S_{3x} and S_{4x} (connects the inductor to the ground or negative terminal of the flying capacitor) are termed as Low Side MOSFETs (LSM). In general, ZVS is possible during the turn-on of the LSM by a proper delay of the gating signals to these devices, but the turn-on of the high side devices is dissipative due to the lack of negative inductor current to charge/discharge the parasitic capacitance across the devices. By proper designing of the inductor to have the inductor ripple current greater than 200 % of its average current, ZVS of HSM along with current self-balancing can be achieved. But it leads to dominant conduction losses under light load conditions. A variable switching frequency strategy is proposed in this chapter to overcome this poor light load efficiency issue. At the end of synchronous conduction mode (S_3 and S_4 are in conduction), S_3 is turned off and the inductor negative peak current charge/discharges the parasitic capacitance of S_2 and S_3 as shown in Figure 6-4. This makes the switch node voltage $V_{in}/2$ as if S_2 is turned on as shown in Figure 6-5. And the time to charge/discharge these switches to $V_{in}/2$ is inversely proportional to the instantaneous inductor current i_{neg_pk} and is given by

$$t_c = \frac{2C_{oss}}{i_{neg\_pk}} V_{in} / 2, \tag{6.1}$$

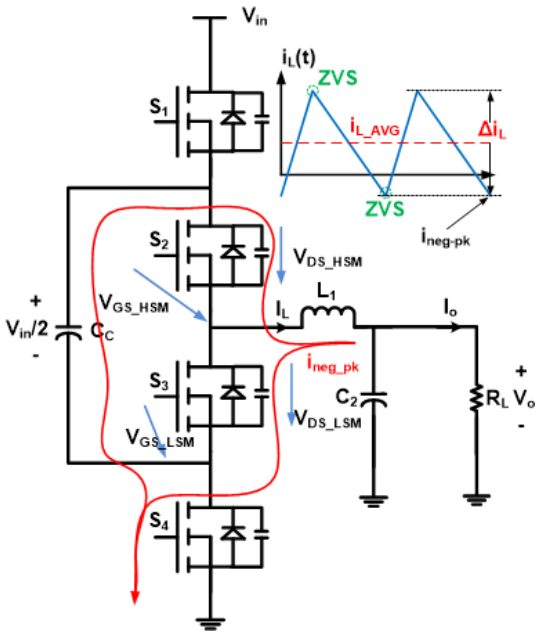


Figure 6-4: Power stage of the 3-level synchronous buck during the turn off of LSM.

where C_{oss} is the device output capacitance. The positive difference of (Deadtime - t_c), increases the effective duty cycle and leads to an increment in the average inductor current of that particular phase. The phase with less average current (higher absolute value of i_{neg_pk}) has the smaller t_c and highest effective duty cycle thus pushes up the average current carried by that particular phase. This entire process operates as a negative feedback effect and enables inherent phase current balancing.

For a given switching frequency f_s, input voltage V_{in} and the filter inductance L, the inductor current ripple is

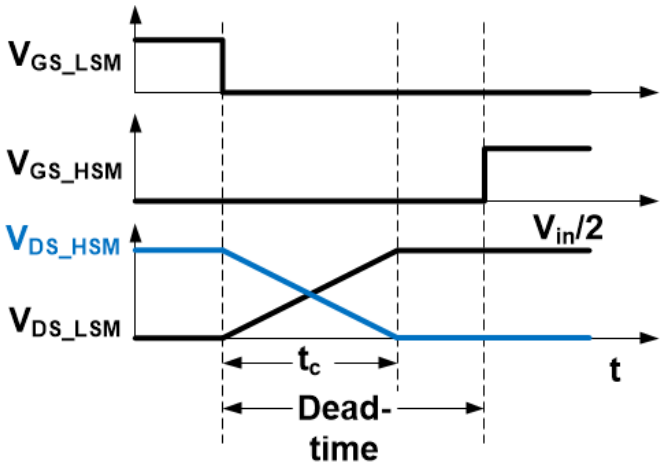


Figure 6-5: Primary waveforms of the 3-level synchronous buck during the turn-off of LSM.

$$\Delta i_L = \frac{V_{in}}{2Lf_s}[0.5 - D]D, \text{ for } 0 < D < 0.5 \tag{6.2}$$

and

$$\Delta i_L = \frac{V_{in}}{2Lf_s}[1 - D][D - 0.5], \text{ for } 0.5 < D < 1.0. \tag{6.3}$$

For this application, D is not going to exceed 0.5. Hence the design is based on (6.2). For a given switching frequency f_s, input voltage V_{in}, and the filter inductance L, the inductor current ripple for $0 < D < 0.5$ is,

$$L_{1max} = \min\left[\frac{2N^2R(0.5 - D)}{2f_{s,eq}}\right], \tag{6.4}$$

where R is load resistance at peak load condition and $f_{s,eq}$ is equivalent switch node frequency which is given by,

$$f_{s,eq} = N * 2f_s. \tag{6.5}$$

The value of the per-phase inductance L_{1x} (where $x = a,\ b,\ c,\ d$) is selected such that $L_{1x} < L_{1max}$. For the four-phase three-level converter the filter values are designed as $L_{1x} = 116\ nH$ and $C_1 = 470\ uF$.

6.4 Output Voltage Control

Figure 6-6 shows the block diagram representation of output voltage control along with flying capacitor voltage control and switching frequency selection blocks. Small-signal modeling of the converter is developed and the output voltage to duty cycle transfer function is derived.

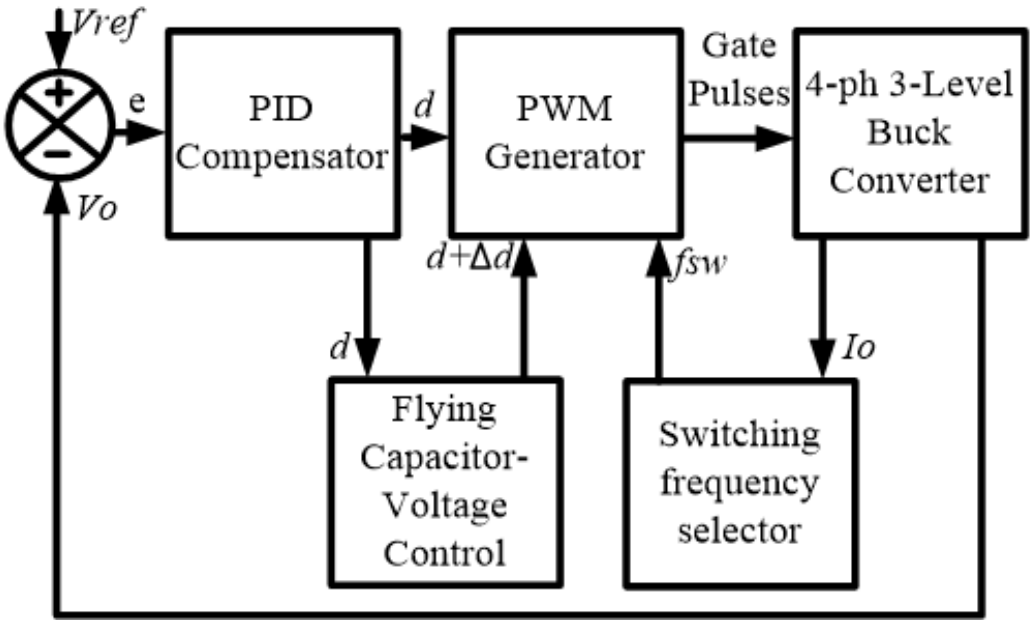


Figure 6-6: Block diagram representation of the entire control scheme.

A PID compensator is designed to regulate the output voltage, with a gain crossover frequency of 160 kHz and a phase margin of more than 90°. Figure 6-7 shows

the closed-loop frequency response of the converter with the PID compensator. The gain cross-over frequency is 160 kHz, whereas the effective switching node voltage frequency of the converter is 1.6 MHz at the minimum gate pulse frequency of 200 kHz.

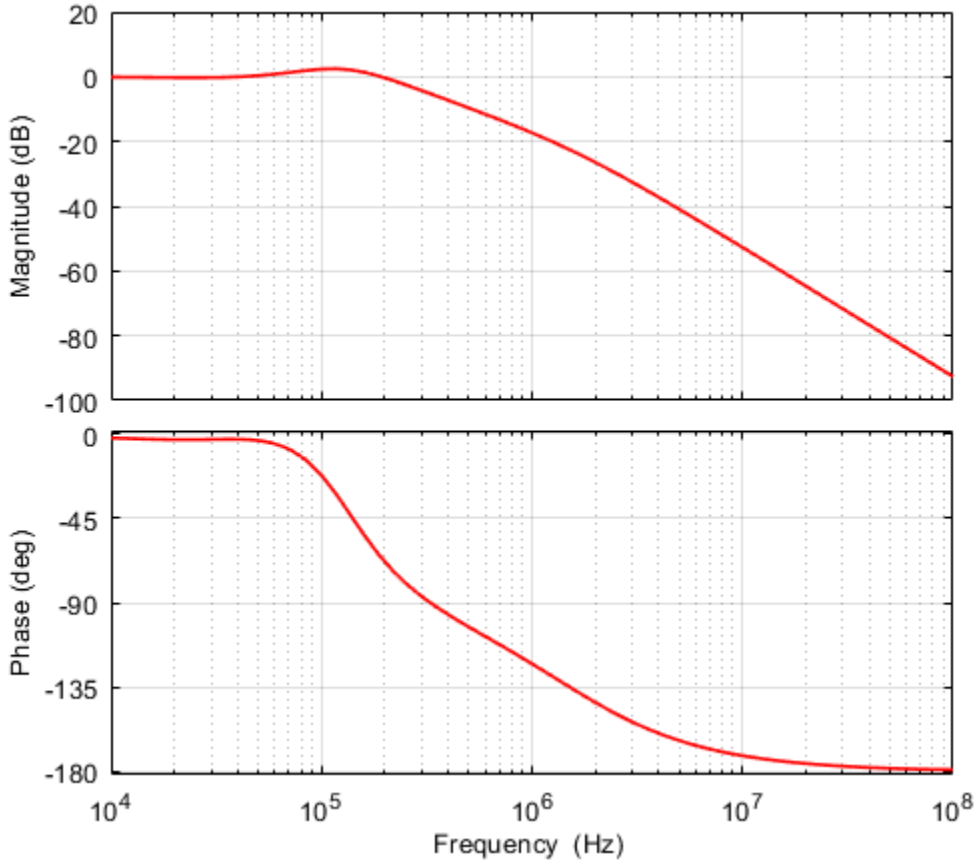


Figure 6-7: Frequency response of the closed-loop system. The gain cross-over frequency is 160 kHz, whereas the effective switching node voltage frequency of the converter is 1.6 MHz at the minimum gate pulse frequency of 200 kHz.

6.5 **Switching frequency selection**

For the designed ZVS inductor the light load RMS current of the converter is dominant and results in increased conduction losses. To improve the light load efficiency of the converter variable switching frequency concept is proposed in this

work. The switching frequency is changed in steps and selection is made by comparing the load current with preset current limits that are obtained from the efficiency curves. For the full load current rating of 160 A the converter is switched at 200 kHz and the switching frequency is increased to 300 kHz for the load current between 100 A and 60 A. At light loads of less than 60 A the switching frequency is further increased to 400 kHz. Too much increase in switching frequency may result in higher switching losses. Moreover, high switching frequency at a specific load condition may lead to a lack of negative current through the inductor which further results in loss of ZVS turn-on of HSM and phase current unbalance. Hence increase in switching frequency at specific load conditions is always a trade-off between phase current balance, switching and conduction losses. The converter efficiency can be further improved with mathematical modeling of efficiency optimization problems and solving for optimal switching frequency at various loading conditions.

6.6 **Loss modeling**

The conduction and switching losses of the multi-phase three-level buck under ZVS turn-on are modeled in this section. The total on-state resistance for each phase is given by

$$R_{par} = R_L + 2R_{on}\,. \tag{6.6}$$

Therefore, the Conduction losses of N–phase three-level buck converter are given by

$$P_{cnd} = \left(I_o^2 \frac{R_{par}}{N} + \mathrm{N} \times \frac{\Delta i_{L,p-p}^2}{12} R_{par} \right), \tag{6.7}$$

where,

$$\Delta i_{L,p-p} = \frac{\Delta V\left(1-D\right)D}{Lf_{sw}}, \tag{6.8}$$

and ΔV is the change in voltage at the switch node which is 0.5Vin for the 3-level buck.

The turn-off switching loss is given by

$$P_{sw} = 2\mathrm{N}\left[\frac{1}{2}\times 2C_{oss}\left(V_{in}/2\right)^2 f_{sw}\right], \tag{6.9}$$

and the gate drive losses are modeled as

$$P_{gd} = 2\mathrm{N}\left[\frac{1}{2}\times 2C_{iss}\left(V_{Gate}\right)^2 f_{sw}\right]. \tag{6.10}$$

The total loss is given by

$$P_{loss} = P_{cnd} + P_{sw} + P_{gd}, \tag{6.11}$$

And finally, the efficiency is obtained by

$$\eta = \frac{1}{1+\frac{P_{loss}}{P_{out}}}. \tag{6.12}$$

Here,

$\Delta i_{L,p-p}$ – Peak to peak inductor current ripple (A),

R – Output load resistance (Ω),

R_{on} – On-state resistance of MOSFET (Ω),

R_L – Inductor ESR (Ω),

R_{par} – Total on-state resistance per phase (Ω),

I_o – Load current (A),

V_o – Output voltage (V),

C_{oss} – MOSFET output capacitance (F),

C_{iss} – MOSFET input capacitance (F),

f_{sw} – Switching frequency (Hz),

V_{in} – DC input voltage (V),

and

V_{Gate} – Voltage swing in the gate pulse (V).

The above equations are used to model the switching and conduction losses. The efficiency of the converter at various output power levels operating at the output voltages of 3.3 V and 5 V are also plotted in the later sections.

6.7 **Results and Analysis**

Figure 6-8 shows the simulated inductor currents and switch node voltages of the four-phase three-level buck converter in the PLECS simulation environment. The

converter is supplied by a 48 V DC source. The total output current ripple I_{LT} is small irrespective of the large per phase inductor ripple current, due to the effect of the interleaved operation. Also, the phase currents are balanced. The flying capacitor voltage is regulated at half of the input voltage at 24 V and the switch node voltages are always switching between 0 V and 24 V.

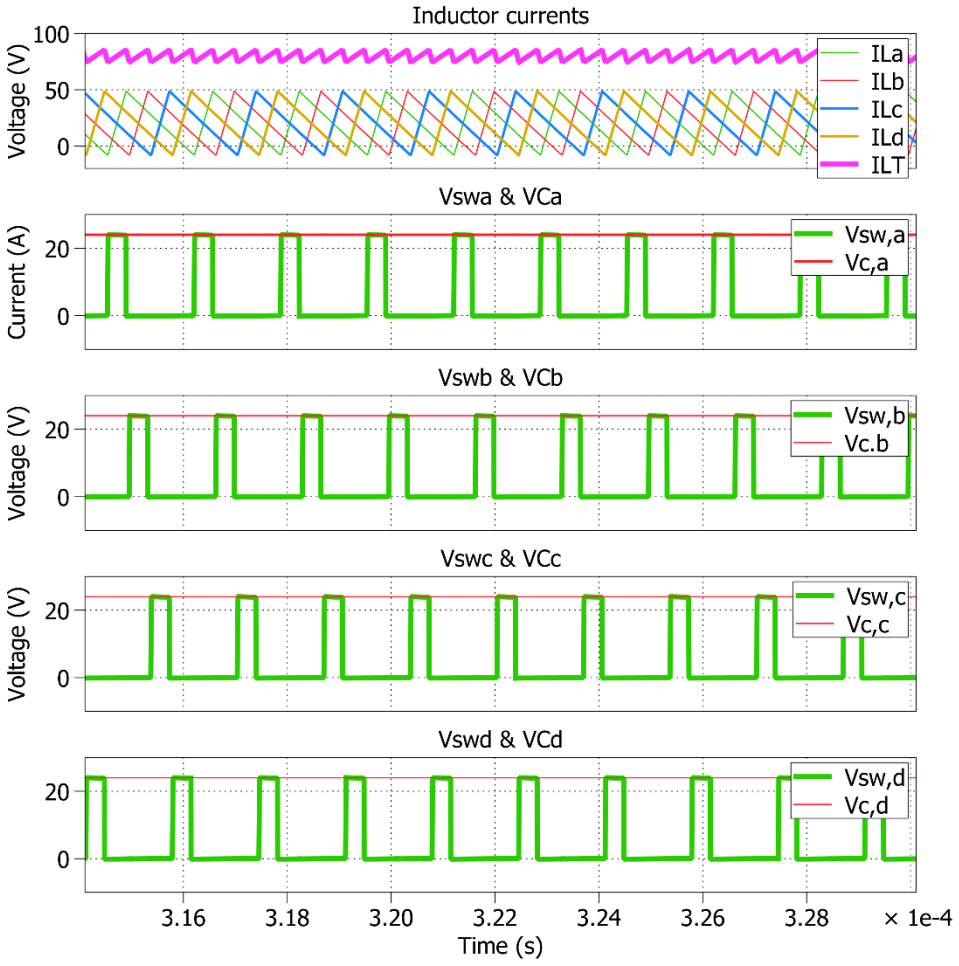


Figure 6-8: Inductor currents, flying capacitor (V_c), and switch node (V_{sw}) voltages during transient operation of load change from full load to half load.

Figure 6-9 and Figure 6-10 show the output voltage regulation during load current transients at 5 V and 3.3 V respectively. When the reference voltage is set to 5 V, the output voltage of the converter is regulated at 5 V during step changes in load current from 40 A to 120 A and vice versa. The switching frequency is changed from 400 kHz to 200 kHz for the load current change from 40 A to 120 A as shown in Figure 6-9.

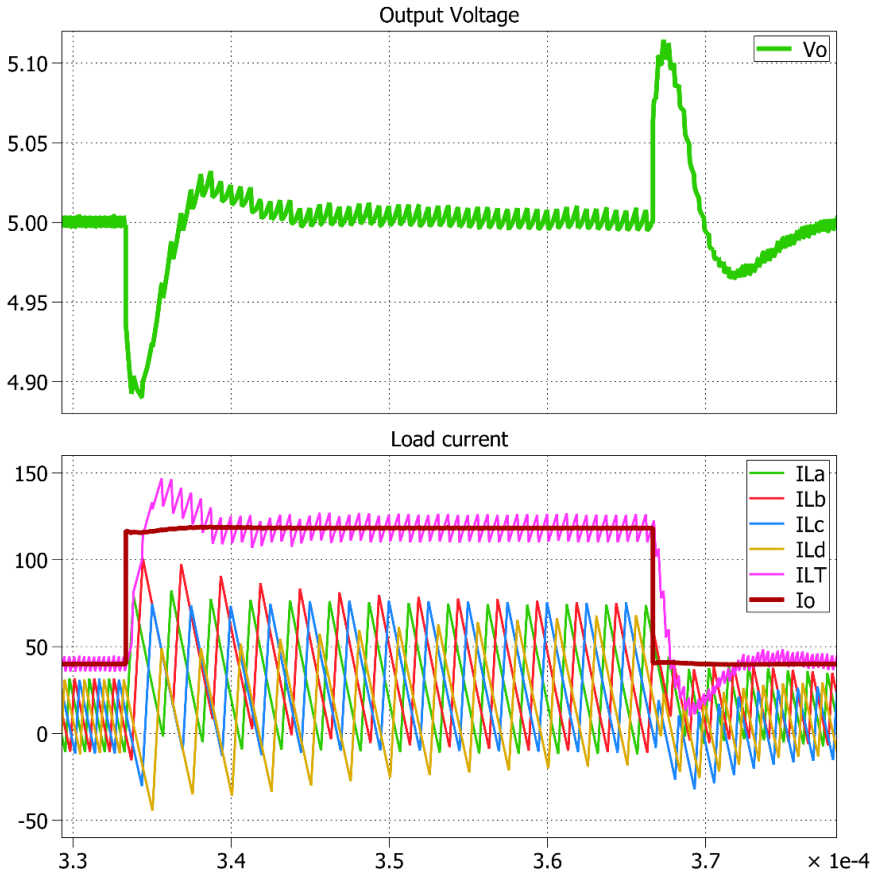


Figure 6-9: Inductor currents and output voltage regulation at 5 V during step changes in load current from 40 A to 120 A and vice versa. The voltage overshoots and/or undershoots by 100 mV.

Similarly, when the reference voltage is set to 3.3 V the output voltage is also regulated at 3.3 V during step changes in load current from 120 A to 25 A and vice versa. Also, the switching frequency increased from 200 kHz to 400 kHz to limit the inductor ripple current under light load conditions. The output voltage overshoots and/or undershoots by 100 mV and the output voltage ripple is ~ 12 mV.

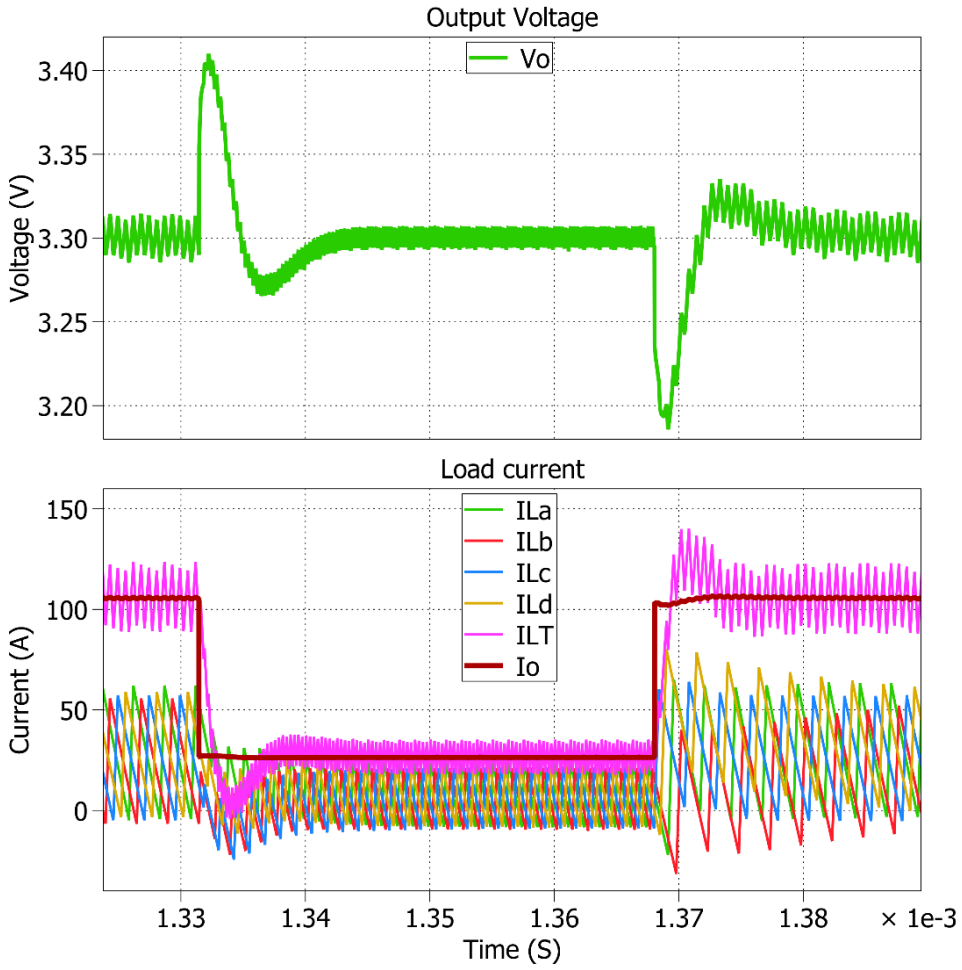


Figure 6-10: Inductor currents and output voltage regulation at 3.3 V of the proposed converter during step changes in load current from 120 A to 25 A and vice versa. The voltage overshoots and/or undershoots by 100 mV and the output voltage ripple is ~ 12 mV.

Figure 6-11 shows the step-change in load current from 160 A to 80 A and the switching frequency also changed from 200 kHz to 300 kHz during the step-change in load current from 160 A to 80 A.

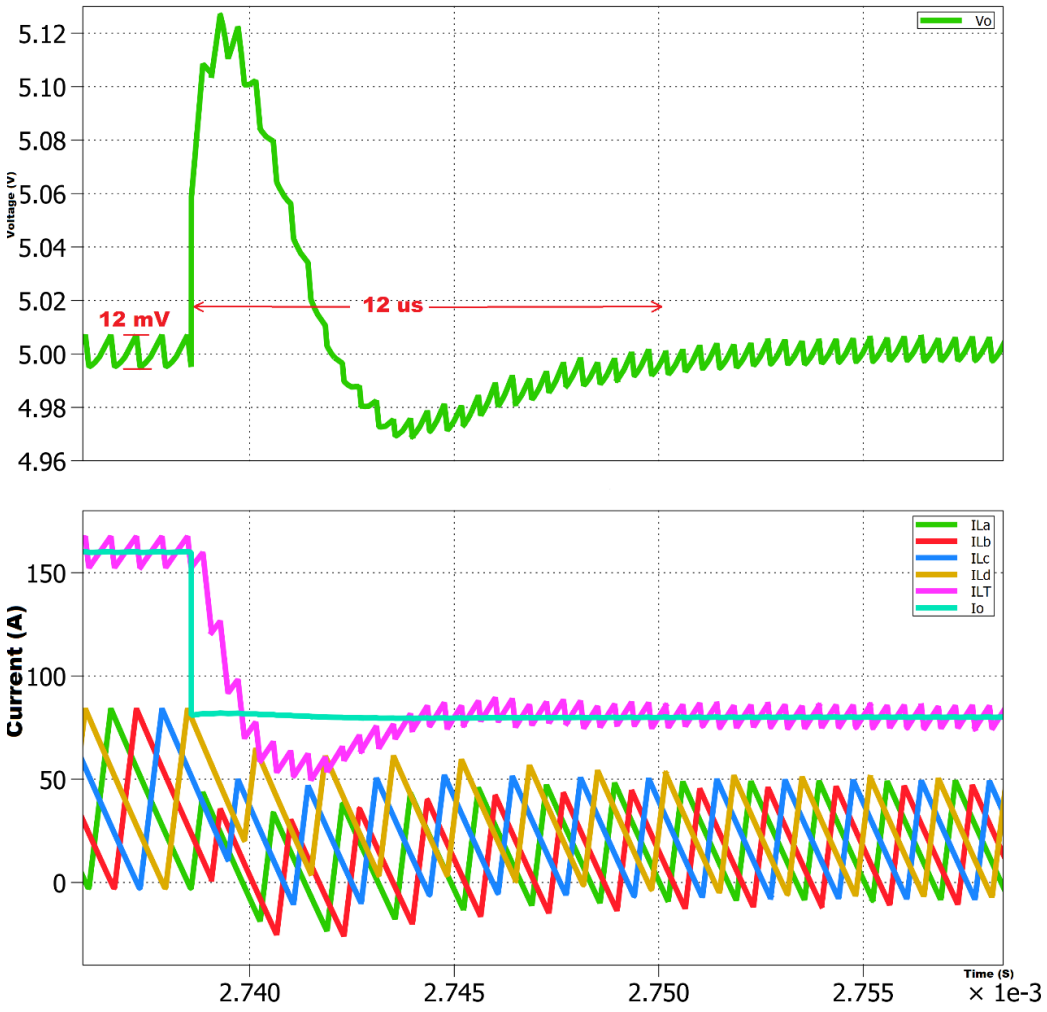


Figure 6-11: Output voltage regulation during step changes in load current from full load to half load.

The inductor currents attained a balanced state after the transient is passed. A voltage overshoot/undershoot of 120 mV is occurred during transient load current

variation and demonstrated a quick transient response time of 12 µs. Moreover, the converter has a steady-state voltage ripple of only 12 mV.

Figure 6-12 shows the ZVS turn-on of the HSM S_2. The voltage across the switch S_2 (V_{S2}) is gradually discharged from $V_{in}/2$ to 0 V and then the gate switching pulse G_2 is applied.

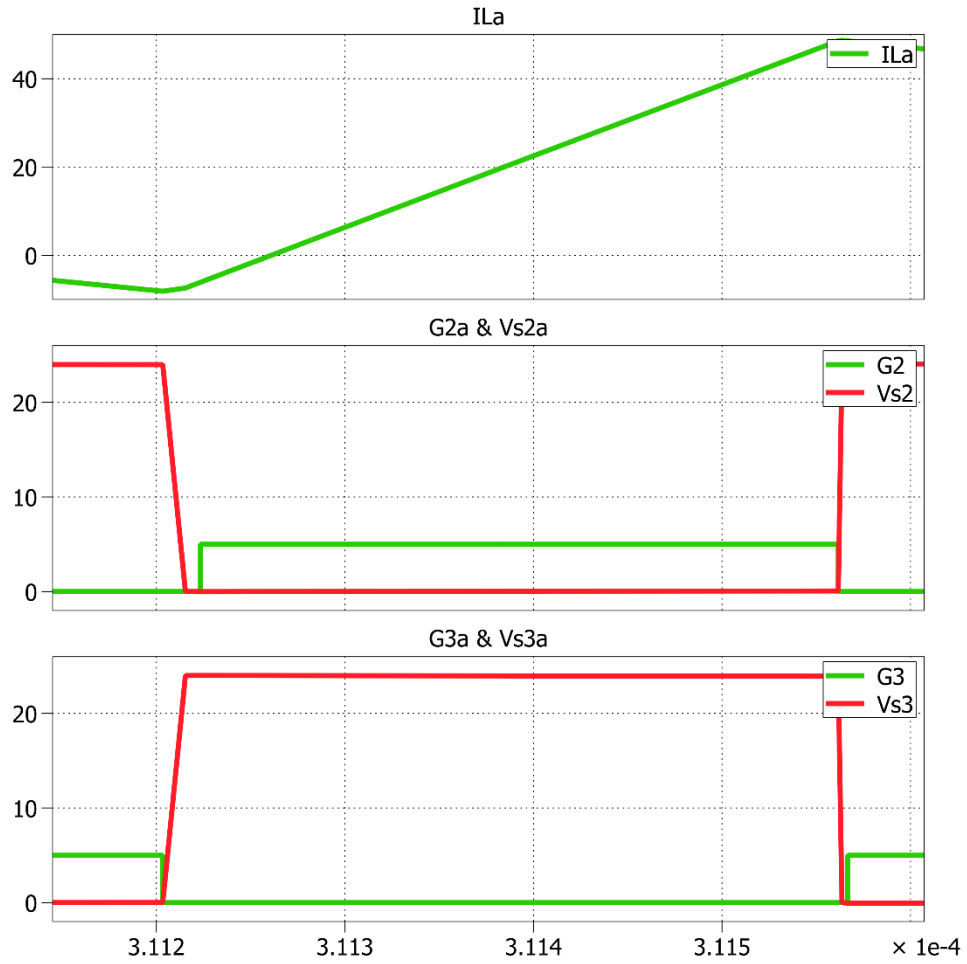


Figure 6-12: ZVS turn-on of the High Side MOSFET S2. The voltage across the switch is 24 V when supplied with 48 V input DC voltage.

ZVS turn-on of LSMs is achieved, by including proper delay in gating pulses to the corresponding switches. The turn-on delay of 20 ns and a turn-off delay of 10 ns are selected for HSM gate pulses, to achieve ZVS over the full range of converter operation.

The efficiency of the converter at various output power levels and the output voltage of 5 V and 3.3 V have been plotted in Figure 6-13 and Figure 6-14 respectively. With the fixed switching frequency of operation, the converter demonstrated poor efficiency at light load conditions. This is due to the dominant ripple current that increases the conduction losses of the converter at light load conditions.

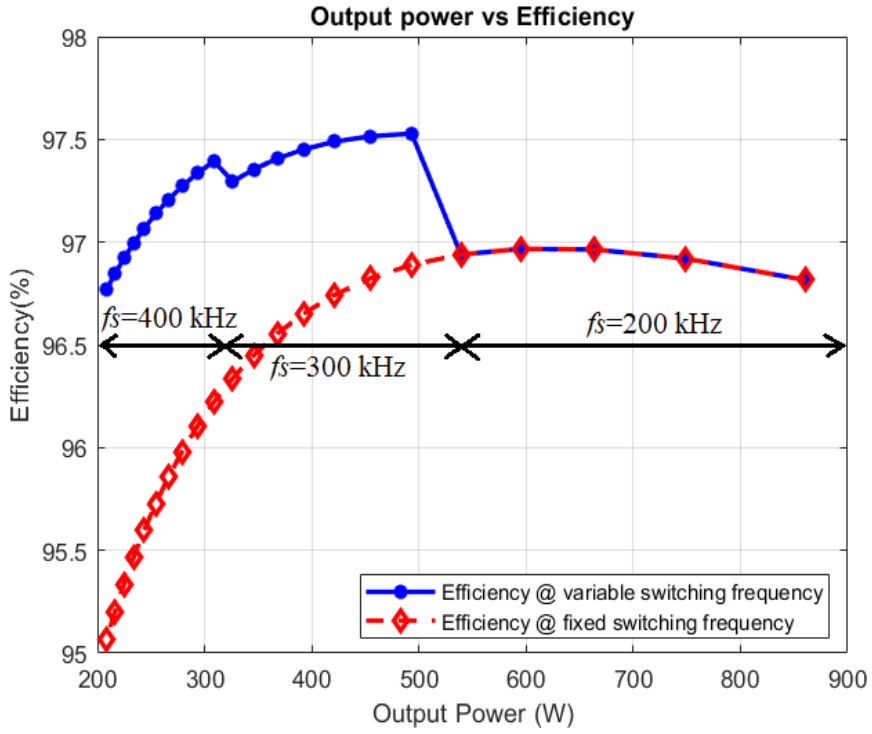


Figure 6-13: Efficiency of the converter at different output power levels and operating at 5 V output voltage. The variable switching frequency scheme improved the light load efficiency by ~1.5%.

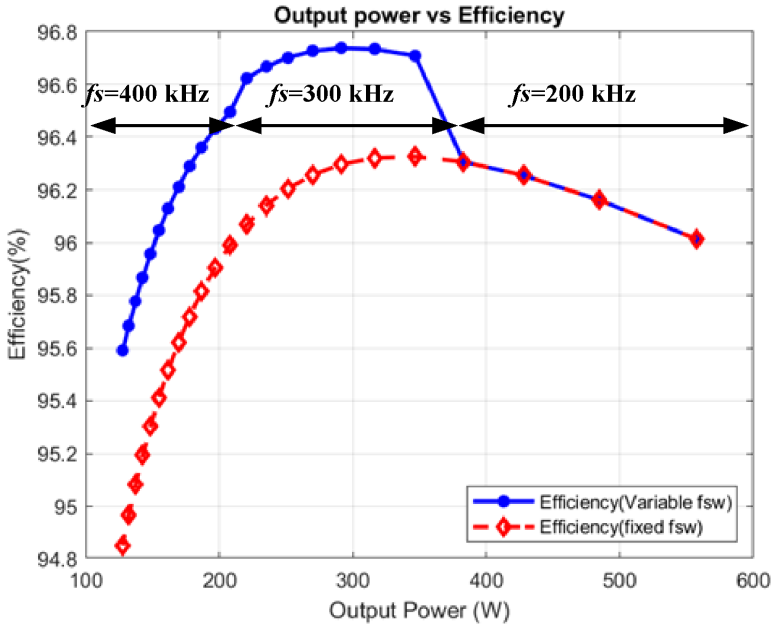


Figure 6-14: Efficiency of the converter at different output power levels and operating at 3.3 V output voltage. The variable switching frequency scheme improved the light load efficiency by ~1.5%.

With an optimal increased switching frequency of operation at light load, the overall efficiency of the converter is improved by 1.5 %. The switching frequency is changed from 200 kHz to 400 kHz in steps of 100 kHz for the load current changes from 140 A to 60 A in steps of 40 A. The higher switching frequency may result in loss of ZVS turn-on of HSM, and phase current unbalance due to lack of negative current through the inductor. Therefore, higher switching frequency increments are not recommended and are limited to 400 kHz in this design. The peak efficiency of the converter is 97.5 % at 500 W output power and the efficiency is greater than 96.5 % for 80 % of the operating range of 5 V output. The maximum efficiency of the converter

operating at 3.3 V output is 96.6 % and it is greater than 95 % for most of the output power range.

6.8 **Summary**

A four-phase three-level buck converter was designed for a 48 V input to 5 V or 3.3 V point-of-load voltage regulator application. Inherent phase current balancing and zero voltage switching of the HSM were achieved by proper designing of the inductor value, thereby eliminating multiple current sharing control loops. Variable switching frequency operation was proposed to improve the converter efficiency under light load conditions. The converter's transfer function was derived and a PID compensator was designed for output voltage regulation. The converter had a fast transient response of 12 μs and a peak overshoot of less than 120 mV during load fluctuations. The efficiency of the converter peaked at 97.6 % at 500 W output power and maintained above 96.5 % for 80 % of the operating range at 5 V. The efficiency was 95 % for the output voltage of 3.3 V. The efficiency can be further improved by solving a mathematical optimization problem formed as a multi-objective function of efficiency, inductor ripple current, and switching frequency. Also, multiple switching frequency steps can be used based on the outcome of the optimization.

7. CONCLUSION AND FUTURE WORK

7.1 Conclusion

This dissertation introduced various single and multi-phase three-level buck converter topologies for telecom and POL regulator power supply application. An FCTL buck converter was studied as a potential candidate for high voltage ET application. An experimental prototype was built and the high-frequency PCB layout guidance was provided. The subsequent chapter proposed a simple gate driving technique for the FCTL buck converter, which can be used for high switching frequency applications such as in envelope tracking, IoT, etc. A hardware prototype was built with a fewer number of active and passive components to reduce the complexity of PCB layout and cost. The gate drive technique was validated through experimental results.

Chapter 4 introduced a multi-phase FCTL buck converter with current self-balancing for high bandwidth and high PAPR ET application. A fourth-order ZVS low pass output filter was designed and a step-by-step design procedure was presented. Simulation results were presented to verify the proposed current self-balancing mechanism in the multi-phase FCTL buck converter. Efficiency and loss analysis was presented to compare the performance with conventional two-level buck equivalent.

Chapter 5 extended the ZVS filter design and current self-balancing concepts proposed in chapter 4 and applied them to the proposed cascaded switching capacitor three-level buck converter. The cascaded switching capacitor was connected in parallel to the input DC voltage and charged through an auxiliary switch and discharged through

the load in series with the input voltage source. The proposed topology eliminated the need for a complex control circuitry to balance the switched capacitor voltage. A modified PWM strategy was proposed to maintain the linear input to output voltage relationship for envelope tracking application. This concept enabled the higher voltage envelope signal tracking for the limited input voltage supply at reduced switching loss. Detailed simulation results were present. An experimental prototype was built and experimental results were shown. The proposed concept is scalable for high power and high voltage ET applications with appropriate voltage-rated devices from the EPC8000 family of GaN FETs.

Chapter 6 concentrated on the design of a single-stage POL regulator. The current self-balancing concept proposed in the previous chapter was used for current sharing and ZVS switching. A variable switching frequency concept was introduced to improve the light load converter efficiency. The voltage regulation and current sharing capability were tested under dynamic loading conditions. Loss modeling and detailed simulation results were presented. The variable switching frequency effect on the improved efficiency of the converter under light load conditions was noted and analyzed.

To conclude this dissertation studied the FCTL buck converter for ET and POL regulator applications and a switched capacitor topology was proposed to avoid the complex control circuitry of switched capacitor voltage balancing. A simple MHz switching frequency gate driving technique is proposed for a high-frequency FCTL

buck converter that can switch up to 40 MHz. It was identified that for high switching frequency converter applications that require fast output transient response, multi-level converters designed with high-frequency GaN MOSFETs and commercially available half-bridge gate driver ICs could improve the efficiency and output response speed. The proposed ZVS filter designs, variable switching frequency, and current self-balancing concepts improved the efficiency and power-sharing capability of the multi-phase designs. The scalability of the proposed designs could significantly improve the PAPR and highest trackable output voltage to 60 V. Multi-phase interleaved converters can improve the output voltage bandwidth without a significant increase in the device switching frequency.

7.2 **Future Work**

The work presented in this dissertation can be extended in various possible ways. A few are listed below.

- The number of switching levels of the cascaded switching converter topology can be improved and modified PWM strategies can be proposed for envelope tracking applications.
- And the switching performance of GaN FETs with negative gate volatges during turn-off would be an interesting topic for future work.
- Though the RFPA behavior is modeled as resistive load an actual RFPA can be used to conduct the system-level study of the proposed converter designs. And, the effect

of variation in the RF input signal frequency on the ET supply voltage and RFPA performance can be studied.

- Since only a basic analysis of PCB is carried using ANSYS Q3D, the PCB layout and part placement can be further optimized with more detailed analysis using a finite element analysis software.
- Since the single-stage POL regulator was programmed with predefined values of switching frequencies, the efficiency can be further improved by solving a multi-objective function for the number of optimal switching frequency levels.

7.3 **Papers Based on This Work**

7.3.1 Published/accepted:

[1] S. Yerra, H. S. Krishnamoorthy and G. S. Kulothungan, "Design and Analysis of Fourth Order ZVS Output Filter for Three-Level Buck Envelope Tracking Power Supply," *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2020, pp. 1-6**.**

[2] S. Yerra and H. S. Krishnamoorthy, "Multi-Phase Three-Level Buck Converter with Current Self-Balancing for High Bandwidth Envelope Tracking Power Supply," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 1872-1877

[3] S. Yerra, H. Krishnamoorthy and Y. Yao, "Single Stage Three-Level Interleaved Buck Converter with Current Self-Balancing for Improved Point-of-Load Performance," *2020 IEEE International Conference on Power Electronics,*

Smart Grid and Renewable Energy (PESGRE2020), Cochin, India, 2020, pp. 1-6.

[4] S. Yerra, H. Krishnamoorthy and J. Hawke, "Three-Level DC-DC Converter using eGaN FETs for Wide Bandwidth Envelope Tracking Applications with Extended Output Voltage Range," *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Genova, Italy, 2019, pp. P.1-P.9.

[5] S. Yerra, H. S. Krishnamoorthy and G. S. Kulothungan, " Simplified Gate Driving Strategy for GaN-Based Multi-level Buck Converters Operating at Multi-MHz Switching Frequencies," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021 – Accepted.

[6] S. Yerra and H. Krishnamoorthy, " Cascaded Switching Capacitor based Multi-phase Three-Level Buck Converter for Communication Envelope Tracking," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021 – Accepted.

7.3.2 To be submitted:

[7] S. Yerra and H. Krishnamoorthy, “High-frequency Flying Capacitor Three-level Buck Converter with Simplified Gate Driving for Fast Varying Voltage Applications,” *IEEE Transactions on Industrial Electronics – To be submitted.*

REFERENCES

[1] GlobeNewsWire, "Bitumen Market to Reach USD 112.01 Billion by 2026: Reports and Data," 2019. https://www.globenewswire.com/news-release/2019/04/11/1802979/0/en/Bitumen-Market-To-Reach-USD-112-01-Billion-By-2026-Reports-And-Data.html (accessed Aug. 19, 2020).

[2] E.C.W. de Jong & P.T.M. Vaessen, "DC power distribution for server farms." [Online]. Available: https://directpowertech.com/docs/LEONARDO ENERGY.pdf.

[3] S. C. Cripps, "RF power amplifiers for wireless communications," *IEEE Microwave Magazine*, vol. 1, no. 1, 2000, doi: 10.1109/mmw.2000.823830.

[4] Johan Strydom, "Using eGaN FETs for Envelope Tracking," https://epc-co.com/epc/Portals/0/epc/documents/papers/eGaN FETs for Envelope Tracking Applications.pdf.

[5] R. Caverly, F. Raab, and J. Staudinger, "High-efficiency power amplifiers," *IEEE Microwave Magazine*, vol. 13, no. 7, 2012, doi: 10.1109/MMM.2012.2216716.

[6] A. S. Tehrani, H. M. Nemati, H. Cao, T. Eriksson, and C. Fager, "Dynamic load modulation of high power amplifiers with varactor-based matching networks," 2009, doi: 10.1109/MWSYM.2009.5166002.

[7] T. M. Hone, S. Bensmida, K. A. Morris, M. A. Beach, and J. P. McGeehan, "Controlling active load-pull in a dual-input inverse load modulated doherty

architecture," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6 PART 2, 2012, doi: 10.1109/TMTT.2012.2190748.

[8] A. F. Aref, T. M. Hone, and R. Negra, "A study of the impact of delay mismatch on linearity of outphasing transmitters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, 2015, doi: 10.1109/TCSI.2014.2349573.

[9] J. Groe, "Polar transmitters for wireless communications," *IEEE Communications Magazine*, vol. 45, no. 9. 2007, doi: 10.1109/MCOM.2007.4342857.

[10] G. T. Watkins and K. Mimis, "A 65% efficient envelope tracking radiofrequency power amplifier for orthogonal frequency division multiplex," *IET Microwaves, Antennas and Propagation*, vol. 9, no. 7, 2015, doi: 10.1049/iet-map.2014.0253.

[11] E. McCune, "Envelope Tracking or Polar—Which Is It? [Microwave Bytes]," *IEEE Microwave Magazine*, vol. 13, no. 4, pp. 34–56, May 2012, doi: 10.1109/MMM.2012.2189506.

[12] F. H. Raab and D. J. Rupp, "High-efficiency single-sideband HF/VHF transmitter based upon envelope elimination and restoration," in *IEE Conference Publication*, 1994, no. 392, doi: 10.1049/cp:19940458.

[13] K. Mimis, S. Wang, and G. T. Watkins, "A load-modulated low-power amplifier with average power tracking," 2015, doi: 10.1109/EuMC.2015.7345706.

[14] Jinsung Choi, Daehyun Kang, Dongsu Kim, and Bumman Kim, "Optimized envelope tracking operation of doherty power amplifier for high efficiency over an extended dynamic range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 6, 2009, doi: 10.1109/tmtt.2009.2020674.

[15] X. Ruan, Y. Wang, and Q. Jin, "A review of envelope tracking power supply for mobile communication systems," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 277–291, Dec. 2017, doi: 10.24295/CPSSTPEA.2017.00026.

[16] A. Williams, "Envelope tracking feature spreads in Android phones," *Electron. Wkly.*, 2014.

[17] "Thomson Broadcast unveils Futhura Plus TV transmitter suitable for HDTV and 3D services," *3D Roundabout*, 2011. .

[18] Z. Wang, "Demystifying envelope tracking: use for high-efficiency power amplifiers for 4g and beyond," *IEEE Microwave Magazine*, vol. 16, no. 3, 2015, doi: 10.1109/MMM.2014.2385351.

[19] K. Moon, J. Kim, S. Jin, B. Park, and Y. Cho, "Highly linear envelope tracking power amplifier with simple correction circuit," in *2015 IEEE Radio Frequency Integrated Circuits Symposium*, 2015, pp. 127–130, doi: 10.1109/RFIC.2015.7337721.

[20] S. Jin, K. Moon, B. Park, J. Kim, and D. Kim, "Dynamic feedback and biasing for a linear CMOS power amplifier with envelope tracking," in *IEEE MTT-S*

International Microwave Symposium (IMS2014), 2014, pp. 1–4, doi: 10.1109/MWSYM.2014.6848264.

[21] J. Hoversten, S. Schafer, M. Roberg, M. Norris, D. Maksimović, and Z. Popović, "Codesign of PA, supply, and signal processing for linear supply-modulated RF transmitters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6 PART 2, 2012, doi: 10.1109/TMTT.2012.2187920.

[22] J. Choi, D. Kim, D. Kang, M. Jun, and B. Jin, "A 45/46/34% PAE linear polar transmitter for EDGE/WCDMA/Mobile-WiMax," 2009, doi: 10.1109/MWSYM.2009.5165721.

[23] M. Rodriguez, Y. Zhang, and D. Maksimovic, "High-frequency PWM buck converters using GaN-on-SiC HEMTs," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2462–2473, 2014, doi: 10.1109/TPEL.2013.2279212.

[24] Y. Zhang, J. Strydom, M. de Rooij, and D. Maksimović, "Envelope tracking GaN power supply for 4G cell phone base stations," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2292–2297, doi: 10.1109/APEC.2016.7468185.

[25] H. Huang, J. Bao, and L. Zhang, "A MASH-controlled multilevel power converter for high-efficiency RF transmitters," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1205–1214, 2011, doi: 10.1109/TPEL.2010.2073721.

[26] C. Florian, T. Cappello, R. P. Paganelli, D. Niessen, and F. Filicori, “Envelope Tracking of an RF High Power Amplifier With an 8-Level Digitally Controlled GaN-on-Si Supply Modulator,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 8, pp. 2589–2602, 2015, doi: 10.1109/TMTT.2015.2447552.

[27] J. Sebastian, P. Fernandez-Miaja, F. J. Ortega-Gonzalez, M. Patino, and M. Rodriguez, “Design of a two-phase buck converter with fourth-order output filter for envelope amplifiers of limited bandwidth,” *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5933–5948, 2014, doi: 10.1109/TPEL.2013.2295035.

[28] C. Wang, P. Xing, L. Zhang, K. Wang, and Y. Li, “A Modular Cascaded Multilevel Buck Converter Based on GaN Devices Designed for High Power Envelope Elimination and Restoration Applications,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 4851–4857, doi: 10.1109/ECCE.2018.8558052.

[29] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, “Three-level buck converter for envelope tracking in RF power amplifiers,” in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2005.*, Mar. 2005, vol. 3, pp. 1588-1594 Vol. 3, doi: 10.1109/APEC.2005.1453248.

[30] V. Yousefzadeh, E. Alarcón, and D. Maksimovíc, “Three-level buck converter for envelope tracking applications,” *IEEE Transactions on Power Electronics*, vol. 21, no. 2, 2006, doi: 10.1109/TPEL.2005.869728.

[31] V. Mehrotra, A. Arias, J. Bergman, C. Neft, M. Urteaga, and B. Brar, “865 MHz switching-speed step-down DC-DC power converter for envelope tracking,” in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2016, vol. 2016-May, doi: 10.1109/APEC.2016.7467855.

[32] V. Mehrotra, A. Arias, C. Neft, J. Bergman, M. Urteaga, and B. Brar, “GaN HEMT-Based >1-GHz Speed Low-Side Gate Driver and Switch Monolithic Process for 865-MHz Power Conversion Applications,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, 2016, doi: 10.1109/JESTPE.2016.2564946.

[33] Y. P. Hong, K. Mukai, H. Gheidi, S. Shinjo, and P. M. Asbeck, “High efficiency GaN switching converter IC with bootstrap driver for envelope tracking applications,” 2013, doi: 10.1109/RFIC.2013.6569602.

[34] S. Shinjo, Y. P. Hong, H. Gheidi, D. F. Kimball, and P. M. Asbeck, “High speed, high analog bandwidth buck converter using GaN HEMTs for envelope tracking power amplifier applications,” 2013, doi: 10.1109/WiSNet.2013.6488618.

[35] P. F. Miaja, A. Rodríguez, and J. Sebastián, “Buck-derived converters based on gallium nitride devices for envelope tracking applications,” *IEEE Transactions on Power Electronics*, vol. 30, no. 4, 2015, doi: 10.1109/TPEL.2014.2326046.

[36] M. Rodríguez, P. Fernández-Miaja, A. Rodríguez, and J. Sebastián, "A multiple-input digitally controlled buck converter for envelope tracking applications in radiofrequency power amplifiers," *IEEE Transactions on Power Electronics*, vol. 25, no. 2, 2010, doi: 10.1109/TPEL.2009.2028732.

[37] J. Sankman, M. K. Song, and D. Ma, "Switching-converter-only multiphase envelope modulator with slew rate enhancer for LTE power amplifier applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, 2016, doi: 10.1109/TPEL.2015.2406710.

[38] Y. Zhang, M. Rodríguez, and D. Maksimović, "Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages With Integrated Gate Drivers," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, 2016, doi: 10.1109/TPEL.2015.2513058.

[39] Y. Zhang, M. Rodríguez, and D. Maksimović, "100 MHz, 20 V, 90% efficient synchronous buck converter with integrated gate driver," 2014, doi: 10.1109/ECCE.2014.6953899.

[40] Y. Zhang, M. Rodriguez, and D. Maksimovic, "High frequency synchronous Buck converter using GaN-on-SiC HEMTs," 2013, doi: 10.1109/ECCE.2013.6646741.

[41] A. Sepahvand, P. Momenroodaki, Y. Zhang, Z. Popovic, and D. Maksimovic, "Monolithic multilevel GaN converter for envelope tracking in RF power

amplifiers," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7, doi: 10.1109/ECCE.2016.7855275.

[42] M. Vasić, P. Cheng, O. García, J. A. Oliver, and P. Alou, "The Design of a Multilevel Envelope Tracking Amplifier Based on a Multiphase Buck Converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4611–4627, 2016, doi: 10.1109/TPEL.2015.2476517.

[43] V. Yousefzadeh, E. Alarcón, and D. Maksimović, "Band separation and efficiency optimization in linear-assisted switching power amplifiers," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–7, doi: 10.1109/PESC.2006.1712188.

[44] P. F. Miaja, M. Rodríguez, A. Rodríguez, and J. Sebastián, "A linear assisted DC/DC converter for envelope tracking and envelope elimination and restoration applications," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3302–3309, 2012, doi: 10.1109/TPEL.2011.2181869.

[45] Q. Jin and M. Vasic, "Optimized Design of GaN Switched-Capacitor-Converter-Based Envelope Tracker for Satellite Application," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1346–1355, 2017, doi: 10.1109/JESTPE.2017.2697719.

[46] Q. Jin, X. Ruan, X. Ren, and H. Xi, "High-Efficiency Switch-Linear-Hybrid Envelope-Tracking Power Supply With Step-Wave Approach," *IEEE*

Transactions on Industrial Electronics, vol. 62, no. 9, pp. 5411–5421, 2015, doi: 10.1109/TIE.2015.2416690.

[47] D. Díaz, M. Vasic, Ó. García, J. A. Oliver, and P. Alou, "Three-level cell topology for a multilevel power supply to achieve high efficiency envelope amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 9, 2012, doi: 10.1109/TCSI.2012.2185307.

[48] D. F. Kimball, J. Jeong, C. Hsia, P. Draxler, and S. Lanfranco, "High-Efficiency Envelope-Tracking W-CDMA Base-Station Amplifier Using GaN HFETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 11, pp. 3848–3856, Nov. 2006, doi: 10.1109/TMTT.2006.884685.

[49] D. Kimball, T. Nakatani, J. Yan, P. T. Theilmann, and I. Telleiz, "High efficiency envelope tracking power amplifiers for wide modulation bandwidth signals (invited)," 2014.

[50] Q. Jin, X. Ruan, X. Ren, Y. Wang, Y. Leng, and C. K. Tse, "Series-parallel-form switch-linear hybrid envelope-tracking power supply to achieve high efficiency," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, 2017, doi: 10.1109/TIE.2016.2595479.

[51] Y. Wang, Q. Jin, and X. Ruan, "Optimized Design of the Multilevel Converter in Series-Form Switch-Linear Hybrid Envelope-Tracking Power Supply," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, 2016, doi: 10.1109/TIE.2016.2565459.

[52] P. Y. Wu and P. K. T. Mok, “A two-phase switching hybrid supply modulator for RF power amplifiers with 9% efficiency improvement,” in *IEEE Journal of Solid-State Circuits*, 2010, vol. 45, no. 12, doi: 10.1109/JSSC.2010.2076510.

[53] M. Tan and W. H. Ki, “An Efficiency-Enhanced Hybrid Supply Modulator With Single-Capacitor Current-Integration Control,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, 2016, doi: 10.1109/JSSC.2015.2490224.

[54] J. Sebastián, P. Fernández-Miaja, A. Rodríguez, and M. Rodríguez, “Analysis and design of the output filter for buck envelope amplifiers,” *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 213–233, 2014, doi: 10.1109/TPEL.2013.2248752.

[55] Y. Zhang, M. Rodriguez, and D. Maksimovic, “Output filter design in high-efficiency wide-bandwidth multi-phase buck envelope amplifiers,” in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2026–2032, doi: 10.1109/APEC.2015.7104627.

[56] R. Pierson, “How to Exceed 98% Efficiency in a Compact 48 V to 6 V, 900 W LLC Resonant Converter Using eGaN FETs,” *Efficient Power Conversion*, 2019. https://epc-co.com/epc/GaNTalk/Post/15230/How-to-Exceed-98-Efficiency-in-a-Compact-48-V-to-6-V-900-W-LLC-Resonant-Converter-Using-eGaN-FETs.

[57] A. Sannino, G. Postiglione, and M. H. J. Bollen, “Feasibility of a DC network for commercial facilities,” *IEEE Transactions on Industry Applications*, vol. 39, no. 5, 2003, doi: 10.1109/TIA.2003.816517.

[58] “Guidelines for energy-effi cient datacenters,” *The green grid*. http://www.thegreengrid.org.

[59] D. Nilsson and A. Sannino, “Efficiency analysis of low- and medium-voltage dc distribution systems,” in *2004 IEEE Power Engineering Society General Meeting*, 2004, vol. 2, doi: 10.1109/pes.2004.1373299.

[60] K. Engelen, E. L. Shun, P. Vermeyen, I. Pardon, and R. D’hulst, “The feasibility of small-scale residential DC distribution systems,” 2006, doi: 10.1109/IECON.2006.347246.

[61] P. Greenland, “Trends in distributed-power architecture,” *The national edge*. http://www.national.com.

[62] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, “High efficiency two-stage 48V VRM with PCB winding matrix transformer,” in *ECCE 2016 - IEEE Energy Conversion Congress and Exposition, Proceedings*, 2016, pp. 1–8, doi: 10.1109/ECCE.2016.7855150.

[63] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, “A 98.55% Efficiency Switched-Tank Converter for Data Center Application,” *IEEE Transactions on Industry Applications*, vol. 54, no. 6, pp. 6205–6222, 2018, doi: 10.1109/TIA.2018.2858741.

[64] Efficient Power Conversion, “EPC8004 – Enhancement Mode Power Transistor,” 2019. http://epc-

co.com/epc/Portals/0/epc/documents/datasheets/EPC8004_datasheet.pdf (accessed Aug. 19, 2020).

[65] B. Kim, J. Moon, and J. Kim, "A multimode/multiband envelope tracking transmitter with broadband saturated amplifier," 2011, doi: 10.1109/TELSKS.2011.6112036.

[66] S. Yerra, H. Krishnamoorthy, and Y. Yao, "Single Stage Three-Level Interleaved Buck Converter with Current Self-Balancing for Improved Point-of-Load Performance," in *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy, PESGRE 2020*, 2020, pp. 1–6, doi: 10.1109/PESGRE45664.2020.9070580.

[67] S. Yerra and H. Krishnamoorthy, "Multi-Phase Three-Level Buck Converter with Current Self-Balancing for High Bandwidth Envelope Tracking Power Supply," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1872–1877, doi: 10.1109/APEC39645.2020.9124075.

[68] S. Yerra, H. Krishnamoorthy, and G. S. Kulothungan, "Design and Analysis of Fourth Order ZVS Output Filter for Three-Level Buck Envelope Tracking Power Supply," in *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2020, pp. 1–6.

[69] C. Barth, J. Colmenares, T. Foulkes, K. Coulson, and J. Sotelo, "Experimental evaluation of a 1 kW, single-phase, 3-level gallium nitride inverter in extreme

cold environment," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 717–723, doi: 10.1109/APEC.2017.7930773.

[70] T. Modeer, C. B. Barth, N. Pallo, W. H. Chung, T. Foulkes, and R. C. N. Pilawa-Podgurski, "Design of a GaN-based, 9-level flying capacitor multilevel inverter with low inductance layout," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2582–2589, doi: 10.1109/APEC.2017.7931062.

[71] A. Stillwell, C. N. Robert, and Pilawa-Podgurski, "A 5-level flying capacitor multi-level converter with integrated auxiliary power supply and start-up," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2932–2938, doi: 10.1109/APEC.2017.7931113.

[72] I. Moon, C. F. Haken, E. K. Saathoff, E. Bian, and R. C. N. Pilawa-Podgurski, "Design and implementation of a 1.3 kW, 7-level flying capacitor multilevel AC-DC converter with power factor correction," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2017, pp. 67–73, doi: 10.1109/APEC.2017.7930674.

[73] Z. Ye, Y. Lei, W. C. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2020, doi: 10.1109/TPEL.2019.2951116.

[74] Z. Ye and R. C. N. Pilawa-Podgurski, “A power supply circuit for gate driver of GaN-based flying capacitor multi-level converters,” in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 53–58, doi: 10.1109/WiPDA.2016.7799909.

[75] Z. Ye, Y. Lei, W. C. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, “Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters,” in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2925–2931, doi: 10.1109/APEC.2017.7931112.

[76] S. Biswas, D. Reusch, and M. de Rooij, “Design of GaN-based multilevel switched capacitor converters - Benefits and challenges,” *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 979–988, 2020, doi: 10.1109/TIA.2020.2965902.

[77] S. Biswas and D. Reusch, “GaN Based Switched Capacitor Three-Level Buck Converter with Cascaded Synchronous Bootstrap Gate Drive Scheme,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 3490–3496, doi: 10.1109/ECCE.2018.8557595.

[78] Texas Instruments, “LMG1210 200-V, 1.5-A, 3-A half-bridge MOSFET and GaN FET driver with adjustable deadtime for applications up to 50 MHz,” 2019. https://www.ti.com/product/LMG1210 (accessed Aug. 08, 2020).

[79] Vicor, “Vicor’s sine amplitude converter topology.” https://vimeo.com/2428429 (accessed Jul. 19, 2019).

[80] and A. M. K. K. Leong, G. Deboy, K. Krischan, “A single stage 54 V to 1.8 V multi-phase cascaded buck voltage regulator module,” in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1966–1973.

[81] A. M. Damerdash, M. Aly, and E. M. Ahmed, “Design and Analysis of Multi-Phase Buck DC-DC Converters for Li-Fi Attocell Drivers,” in *2019 International Conference on Innovative Trends in Computer Engineering, ITCE 2019*, 2019, pp. 515–520, doi: 10.1109/ITCE.2019.8646687.

[82] A. Castro de, P. Alou, and J. A. Cobos, “Current Self-Balance Mechanism in Multiphase Buck Converter,” *IEEE Transactions on Power Electronics*, 2009, doi: 10.1109/TPEL.2009.2013859.

[83] A. Abdulslam, S. H. Amer, A. S. Emara, and Y. Ismail, “Evaluation of multi-level buck converters for low-power applications,” 2016, doi: 10.1109/ISCAS.2016.7527360.

[84] Efficient Power Conversion, “EPC8009 – Enhancement Mode Power Transistor,” 2019. http://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC8009_datasheet.pdf (accessed Dec. 14, 2018).

[85] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, “High-efficiency high-power-density 48/1V sigma converter voltage regulator module,” 2017, doi: 10.1109/APEC.2017.7931005.

[86] K. K. Leong, G. Deboy, K. Krischan, and A. Muetze, “A single stage 54V to 1.8V multi-phase cascaded buck voltage regulator module,” in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2015, vol. 2015-May, no. May, doi: 10.1109/APEC.2015.7104617.

[87] H. S. H. Chung, S. Y. Hui, and S. C. Tang, “Development of a multistage current-controlled switched-capacitor step-down DC/DC converter with continuous input current,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 7, 2000, doi: 10.1109/81.855457.

[88] B. B. Macy, Y. Lei, and R. C. N. Pilawa-Podgurski, “A 1.2 MHz, 25 v to 100 v GaN-based resonant Dickson switched-capacitor converter with 1011 W/in3 (61.7 kW/L) power density,” in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2015, vol. 2015, pp. 1472-1478 doi: 10.1109/APEC.2015.7104542.

[89] X. Zhang, C. Yao, and J. Wang, “A Quasi-Switched-Capacitor Resonant Converter,” *IEEE Transactions on Power Electronics*, vol. 31, no. 11, 2016, doi: 10.1109/TPEL.2015.2490554.

[90] X. Zhang, C. Yao, C. Li, L. Fu, F. Guo, and J. Wang, “A wide bandgap device-based isolated quasi-switched-capacitor DC/DC converter,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, 2014, doi: 10.1109/TPEL.2013.2287501.

[91] R. C. N. Pilawa-Podgurski and D. J. Perreault, “Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, 2012, doi: 10.1109/JSSC.2012.2191325.

[92] H. P. Le, J. Crossley, S. R. Sanders, and E. Alon, “A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm2 at 73% efficiency,” in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2013, vol. 56, doi: 10.1109/ISSCC.2013.6487775.

[93] S. R. Sanders, E. Alon, H. P. Le, M. D. Seeman, M. John, and V. W. Ng, “The road to fully integrated DC-DC conversion via the switched-capacitor approach,” *IEEE Transactions on Power Electronics*, vol. 28, no. 9, 2013, doi: 10.1109/TPEL.2012.2235084.

[94] C. Schaef and J. T. Stauth, “A 12-volt-input hybrid switched capacitor voltage regulator based on a modified series-parallel topology,” 2017, doi: 10.1109/APEC.2017.7931043.

[95] C. Schaef and J. T. Stauth, “A 3-Phase Resonant Switched Capacitor Converter Delivering 7.7 W at 85% Efficiency Using 1.1 nH PCB Trace Inductors,” *IEEE*

Journal of Solid-State Circuits, vol. 50, no. 12, 2015, doi: 10.1109/JSSC.2015.2462351.

[96] C. Li, R. D. Zamora, C. Yao, L. Fu, and A. Lang, "A family of high gain hybrid switched capacitor-inductor dc-dc circuits for renewable energy applications," 2014, doi: 10.1109/ITEC-AP.2014.6941073.

[97] M. Alsolami, K. A. Potty, and J. Wang, "A Gallium-Nitride-Device-Based Switched Capacitor Multiport Multilevel Converter for UPS Applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, 2017, doi: 10.1109/TPEL.2016.2629283.

[98] H. P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, 2011, doi: 10.1109/JSSC.2011.2159054.

[99] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, 2008, doi: 10.1109/TPEL.2007.915182.

[100] Efficient Power Conversion, "EPC2023–enhancement mode power transistor," 2019. https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2023 (accessed Jun. 13, 2019).

[101] Efficient Power Conversion, "EPC2024 - Enhancement Mode Power Transistor." https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2024.aspx.