CONTROL STRATEGIES FOR MINIMIZING THE DC-LINK CAPACITANCE IN POWER ELECTRONICS CONVERTERS FOR AIRCRAFT ELECTRICAL POWER SYSTEMS

by

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ABSTRACT

In more electric aircraft (MEA), the electrical power system (EPS) consists of AC and DC power distribution systems to deliver power to various aircraft loads. In main power generation, variable frequency generators (VFGs) generate VF AC supply (380-800Hz 115/230V) to feed frequency insensitive loads. The VF AC is also converted into DC (+/-270V or 540V) by using transformers and power electronics converters (PECs) to feed DC loads. The DC is further converted into 115V 400Hz AC, and 28V DC using PECs to feed legacy loads. In MEA, the usage of PECs has increased significantly over the last few decades. These PECs have DC-link and use DC-link capacitors that are space-consuming, and heavy. In order to reduce the fuel consumption of aircraft, weight-saving and volume reduction are the critical challenges faced by engineers. Hence, reducing the DC-link capacitance value in the PECs is very crucial in MEA. In this dissertation, novel control algorithms and improvements are proposed for different configurations of VF brushless synchronous generator (BSG) based DC and AC power systems to minimize the DC-link capacitance in the PECs.

First, a BSG based 270V DC system using a diode rectifier is investigated in which the DC-link voltage regulation is obtained through the excitation control of the exciter SG using a two-quadrant DC chopper. A steady-state feedforward duty ratio and output power-based feedforward exciter field current reference are proposed to improve the transient response of the DC system to meet the military standard (MIL-STD-704F) transient voltage specifications with minimized DC-link capacitance. Next, BSG based diode rectifier inverter (DRI) regulated 115V, 400Hz AC variable speed constant frequency system (VSCF) is investigated. In the VSCF system, the control improvement from the BSG based

DC system is used along with a novel adaptive inverter voltage reference (AIVR) algorithm in the four-leg inverter side and to reduce the effects of inverter side fast dynamics. The combined control improvements help to meet the stringent MIL-STD-704F transient voltage specifications at the inverter output with minimum DC-link capacitance required in the VSCF system.

Further, the BSG based DC system is investigated with an active rectifier in place of a diode rectifier. An improved DC-link voltage regulation based on field oriented control (FOC) of the BSG along with a feedforward excitation control for fast transient operation is proposed to further improve the transient response of the DC-link voltage and reduce the DC-link capacitance when compared to the diode rectifier based DC system. A steady-state rotor flux optimization algorithm based on BSG steady-state equations is proposed to maintain unity power factor (UPF) operation at the BSG terminals during steady-state operating conditions. Finally, the Electro-magnetic interference (EMI) filter design for the BSG based DC and AC systems are studied. The EMI filters are designed for different PECs such as two-quadrant DC chopper, diode rectifier, active rectifier, and four-leg inverter in the BSG based DC and AC systems. The effects of EMI filters in the control of BSG based DC and AC systems are investigated. All the proposed control algorithms are validated through extensive modeling and simulations in PLECS and the effectiveness of the control algorithms are verified through controller hardware in loop (C-HIL) testing results.

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CHAPTER 1

INTRODUCTION

The electrical power system (EPS) in the aerospace industry has gone through major evolution over the past several decades, as shown in Fig. 1.1. In 1950s and 1960s, the twin 28V DC and 115V 400Hz constant frequency (CF) AC were used as standard power supply in the aircraft. In 1990s, the VF AC 115V, 360Hz-720Hz system was introduced and subsequently used in more electric aircraft (MEA) Airbus A380. In the early 2000s, the VF 230V, 320Hz-800Hz AC is used along with DC +/- 270V (540V) in MEA Boeing 787 aircraft [1]–[4]. The trend is moving towards high voltage DC (HVDC) systems (Starc-abl-NASA) to increase the efficiency of the EPS in the aircraft [5].

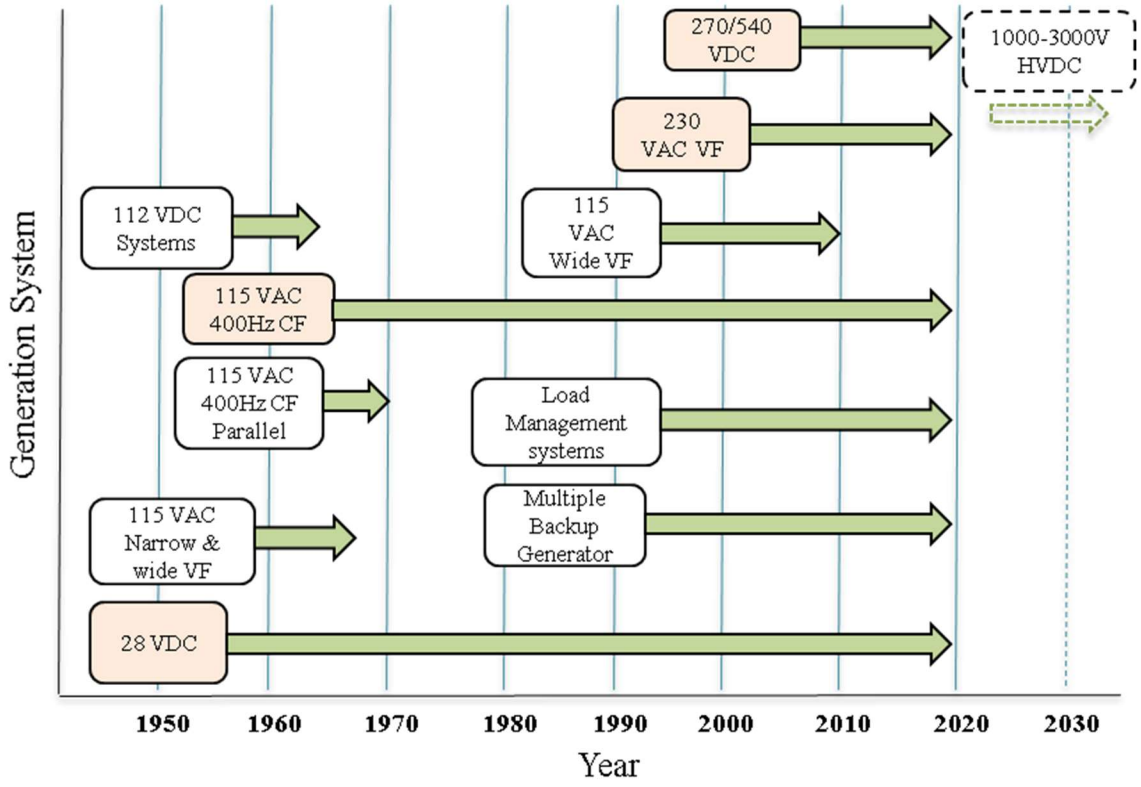

Fig. 1.1: Evolution of aircraft EPS over the past several decades [1].

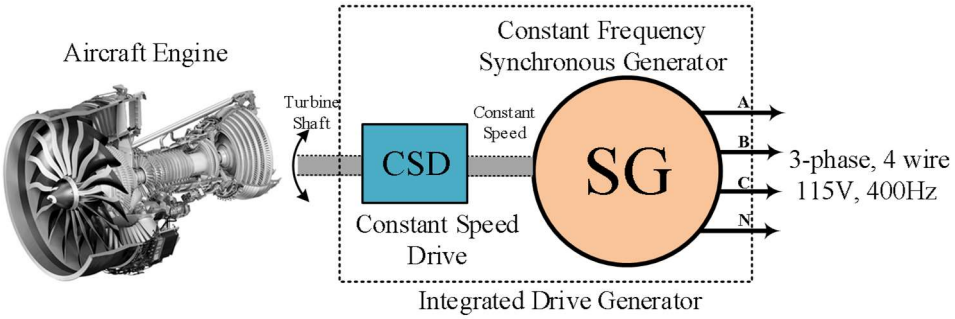

Fig. 1.2: Integrated Drive Generator (IDG) based 115V 400Hz AC system.

Though different DC and AC voltage systems are used in the aircraft EPS in the past several decades, the majority of the electrical equipment in the modern MEA such as A380 and B787 are still largely rated for the legacy 115V, 400Hz AC and the 28V DC and relatively smaller portions of the electrical loads are rated for +/- 270V DC and 230/115V VF AC [6].

1.1 Review of electrical power generation in aircraft EPS

Traditionally, the 115V, 400Hz supply in the aircraft is generated by using three phase AC generator. In order to generate CF AC supply, the AC generators are driven by the engine turbine shaft through a hydro mechanical gear system, also known as constant speed drives (CSD). These CSDs have mechanical couplings and gears arrangement that convert the variable speed operation of the engine turbine shaft to a constant speed operation to generate a CF AC voltage [1], [3], [7]. These CSDs have moving mechanical parts that make the system bulky and have high losses and are prone to mechanical failures that make the aircraft EPS less reliable and less efficient. In order to reduce the space consumption of the CSD and to increase the power density of the power generating system, the CSD and the AC generator are later integrated together as a single unit, called Integrated Drive Generator (IDG) [8]. Fig 1.2 shows the IDG in the aircraft EPS.

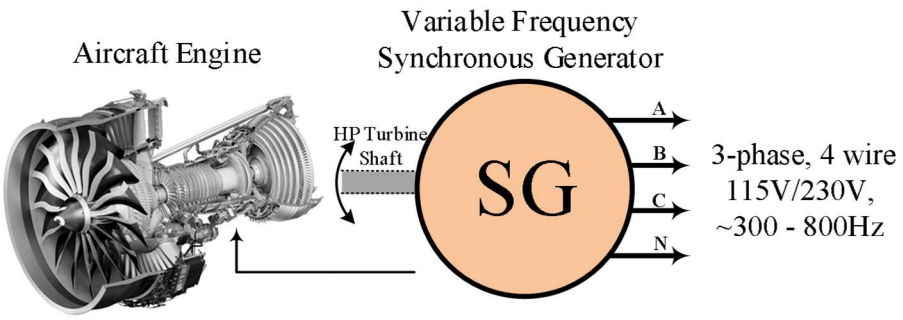

Fig. 1.3: Variable Frequency AC power generation system in MEA.

Though IDG replaces the CSD in the aircraft to save space consumption, it still holds all the demerits from the CSD because the IDG still contains the CSD which includes the less reliable mechanical couplings and gears that make the system less reliable and needs extra maintenance. These IDGs were primarily used for both main and backup power generation in the aircraft. However, due to the increased demand for electrical power in the aircraft and the trend towards MEA to reduce fuel consumption, and to increase efficiency and power density of the electrical system, most of the IDGs used in main power generation were replaced by the Variable frequency Generators (VFG) in MEA. These VFGs are smaller in size, weight and more efficient than the IDGs due to their VF operation which waives the requirement of additional mechanical gears and couplings needed in the IDGs.

Fig. 1.3 shows the VF 300-800Hz, 115/230V AC power generation system in MEA using VFG. In MEA, the non-propulsive loads such as mechanical, hydraulic, and pneumatic are replaced by the electrical loads and these high power electrical loads are frequency insensitive, so are directly fed by the VF AC main supply from the VFGs [6], [9]. Fig. 1.4 shows EPS architecture of the MEA Boeing 787. It can be seen from Fig. 1.3 that the VF 230V AC supply from VFG is used as the primary power distribution. It also feeds the frequency insensitive large loads directly from the VF 230V AC supply. It can

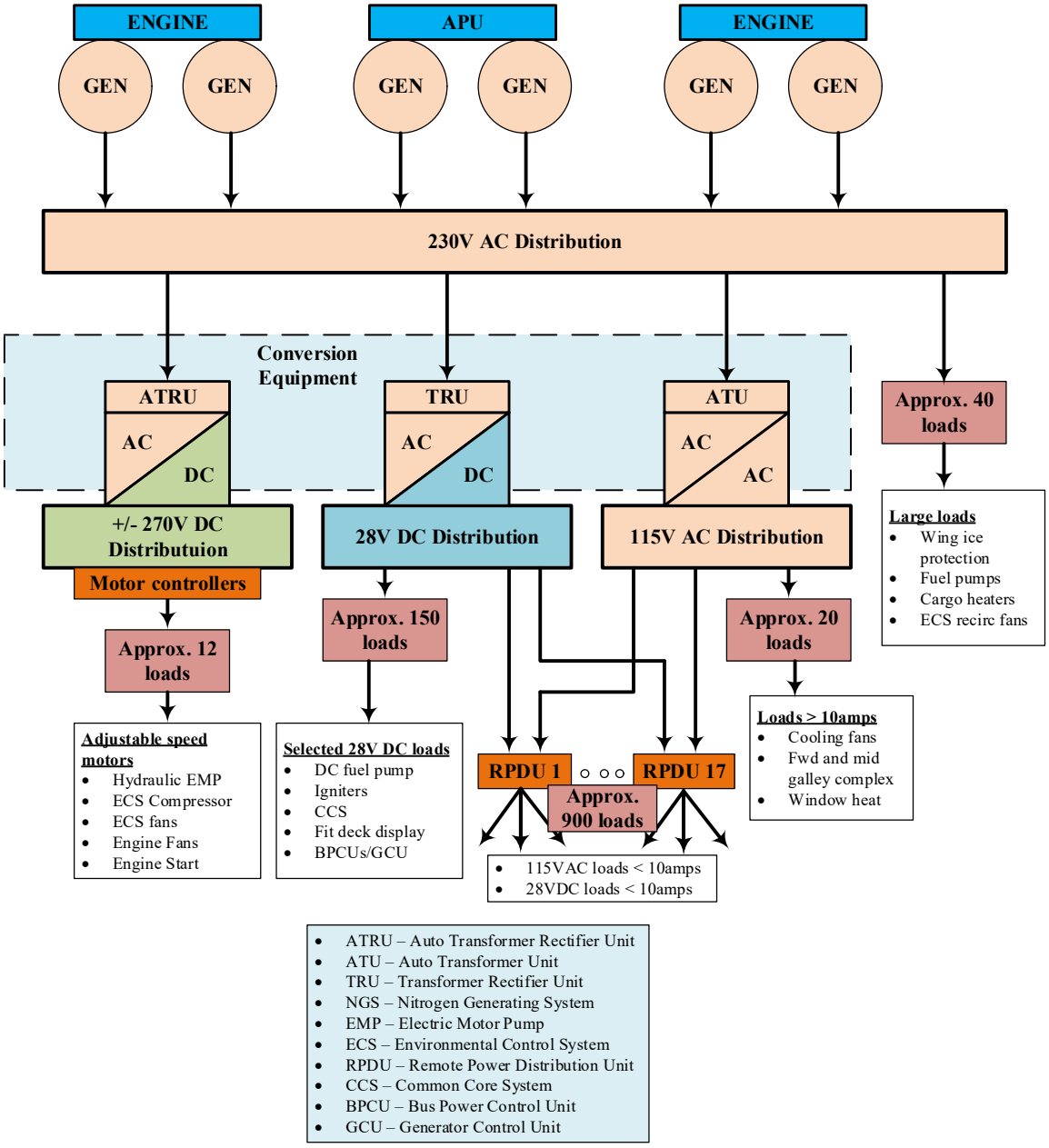

Fig. 1.4: EPS architecture of Boeing 787 [6].

also be noted from Fig 1.4 that the other frequency sensitive AC loads and DC loads are powered from the main 230V VF AC through Auto Transformer Unit (ATU), Auto Transformer Rectifier Unit (ATRU), Transformer Rectifier Unit (TRU), Remote Power Distribution Unit (RPDU), and Power Electronics Converters (PEC).

Though IDGs are replaced by VFGs in aircraft main power generation, they are still used in few modern aircraft (B737NG, B777x, and A330) [10] to provide 115V 400Hz AC backup power to the aircraft loads. Since the IDGs are less reliable and less efficient, the VFGs were used along with PECs to provide 115V, 400Hz AC backup power to the aircraft loads. These systems are called variable speed constant frequency (VSCF) systems and are used by some aircraft (B777, some versions of B777-500) with very little success in the past [1]. However, with the latest advancements in power electronics such as reliable power switches, fault tolerant converter architectures and advanced control methods to reduce the space consumption of the converters, the PEC based backup power systems are still very attractive options to provide backup power to the aircraft loads. In this dissertation, PEC based backup power systems with different topologies and control methods are investigated and control improvements are proposed to help reduce the space consumption of the PEC by reducing the DC-link capacitance required in the PEC.

1.1.1 VFG based PEC controlled AC power system

One of the main advantages of using PEC based VSCF backup power system, when compared to the IDG system is that the PEC can be mounted anywhere in the aircraft which not only helps in reducing the size of the backup power generator but also gives flexibility in the aircraft weight distribution. There are different PEC topologies for VSCF system that are currently being used or in consideration in both civil and military aircraft, they are,

1. The DC-link based Diode Rectifier Inverter (DRI) system (AC-DC-AC).
2. The Cyclo-converter or Matrix converters based system (AC-AC).
3. The DC-link based Active Rectifier Inverter (ARI) system (AC-DC-AC).

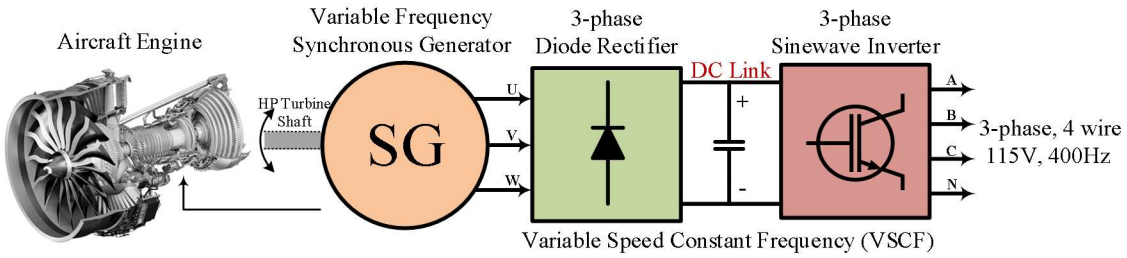

Fig. 1.5: VFG based DRI regulated 115V, 400Hz VSCF system with DC-link.

Fig. 1.5 shows the VFG based DRI regulated 115V, 400Hz VSCF system with DC-link. In DC-link based DRI systems, the VF AC voltage from the VFG is first converted into a DC voltage using a three phase diode rectifier to form a DC-link, then the DC voltage is converted into a CF 400Hz, 3 phase, 115V AC by using a three phase inverter. The state of the art DC-link based DRI system is a highly matured and proven technology in several power electronics applications for the last several decades. The main drawback in using the DC-link based VSCF system is the usage of bulky energy storage DC capacitors at the DC-link [11]–[13]. The presence of bulky DC-link capacitors increases the total volume of the PEC and poses increased difficulties in realizing high power density.

Fig. 1.6 shows the VFG based matrix converter regulated 115V, 400Hz VSCF system. In Cycloconverter or Matrix converter based VSCF systems, the VF AC is directly converted into CF AC without the need for DC-link and thereby eliminates the space consuming DC-link capacitors in the PEC[14]. The cycloconverter based VSCF systems are widely used in US military aircraft (F/A18-C/D, F/A18-E/F, F117A, U2 and V-22) [15], [16].

Though cycloconverters and matrix converters eliminate the bulky DC-link capacitors, these systems need AC filters at the input and output side of the PEC and require additional number of semiconductor switches and consequently require more gate drivers

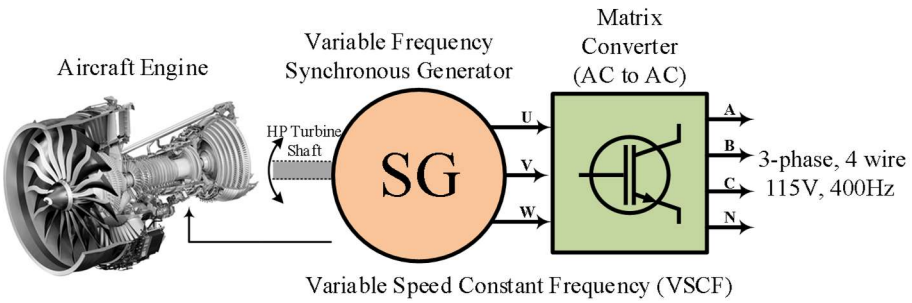

Fig. 1.6: VFG based cycloconverter or matrix converter regulated 115V, 400Hz VSCF system without DC-link.

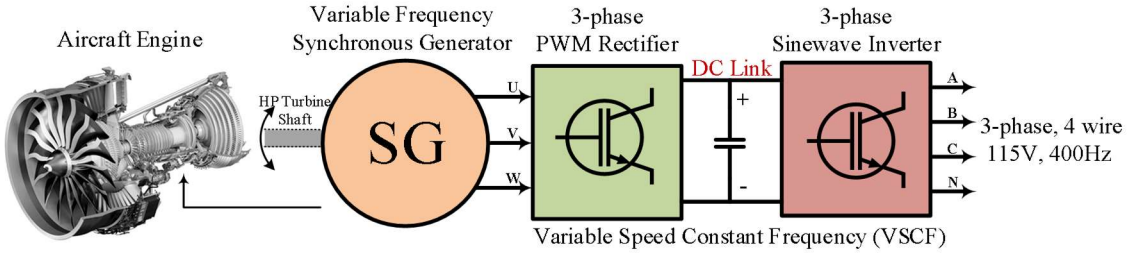

Fig. 1.7: VFG based active rectifier regulated 115V, 400Hz VSCF system with DC-link.

in the PEC. Moreover, these systems produce less output voltage and high conduction loss due to the increased number of semiconductor switches in the PEC [17], [18]. As a result, there is no significant reduction in size and weight of the PEC and no substantial improvement in the performance when compared to the DC-link based DRI system. Hence, DC-link based VSCF DRI systems are more commonly used in civil aircraft, such as MD90 till 1990 (2 x 75kVA converter), B717, B737, and B777 (2 x 20kVA in older models and 2 x 43.3kVA in newer models) [1], [3], [19]–[21]. Besides, the demand for minimizing DC-link capacitance in the DC-link based VSCF system increases day by day and becomes more significant in the civil aircraft to increase the power density of the EPS and at the same time to keep the volume and space consumption lower than other backup power systems. The pioneering advancements in power electronics and the development of ultra-high speed Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA)

play a vital role in reducing the bulky DC-link capacitance through fast digital control strategies.

One another VSCF topology, which is gaining more interest in the aircraft EPS is the active rectifier inverter regulated VSCF system. The usage of active rectifier enables number of advantages in the EPS such as, starter/generator operation when compared to only generation mode with diode rectifier based VSCF systems, fast transient control helps to enable DC loads and energy storage in the DC-link along with the AC loads. Fig. 1.7 shows the VFG based active rectifier regulated 115V, 400Hz VSCF system with DC-link. In this VSCF system, the diode rectifier is replaced with an active rectifier to improve the power quality and efficiency of the VFG and at the same time to improve the transient response at the DC-link to meet the transient voltage specifications at the DC-link and allows local DC loads and energy storage at the DC-link. Though active rectifier based system improves the power quality and efficiency of the VFG, the presence of active rectifier increases the space consumption due to the presence of additional gate drivers and controllers in the PEC, along with the DC-link capacitors. However, with suitable control improvements and high switching frequency operation, the presence of switching converter helps to reduce the sizing of the PEC.

1.1.2 VFG based PEC controlled DC power system

In modern MEA, DC power distribution is becoming more popular and increasingly being considered in aircraft EPS in recent years due to its reduced power loss and weight-saving qualities. In Boeing 787, +/-270 Volt DC is used as one of the primary power distribution along with the 230V VF AC supply [6], [22].

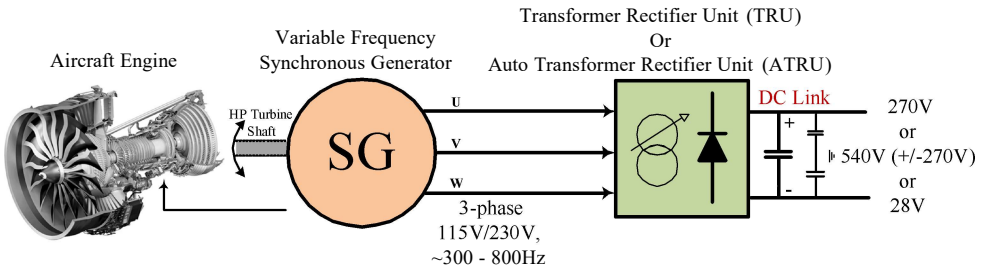

Fig. 1.8: VFG based ATRU/TRU regulated +/-270V DC power system.

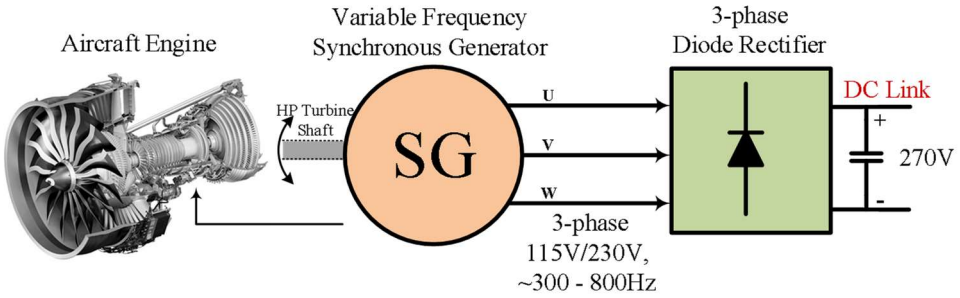

Fig. 1.9: VFG based diode rectifier regulated 270V DC power system.

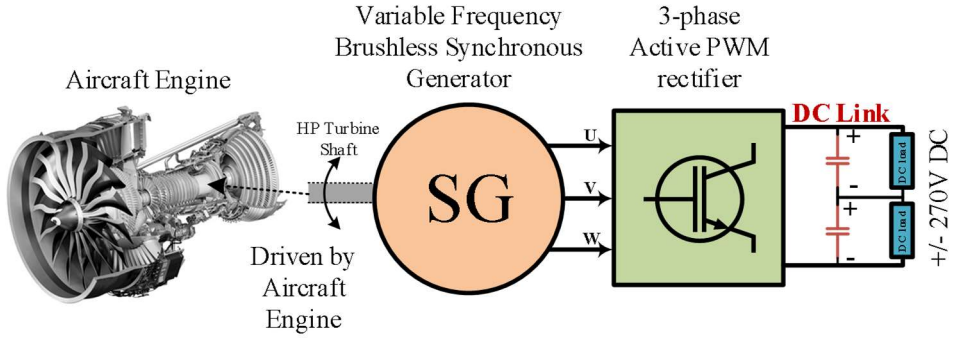

Fig. 1.10: VFG based active rectifier regulated +/-270V DC power system.

As per Fig 1.1, the aircraft EPS trend is moving towards the HVDC systems so that the DC backup power systems also need to be optimized for better efficiency and less fuel consumption in the aircraft. The +/-270 Volt DC is obtained by converting the VF AC into DC by using ATRU and TRU as shown in Fig. 1.8. Though the VFG is used along with the PEC (diode rectifier), the usage of ATRU and TRU, makes the system extra bulky. One possibility in the standalone DC power system is that the diode rectifier can be directly

connected to the VFG without ATRU and TRU, and DC-link voltage regulation is obtained by controlling the excitation of the VFG. Fig 1.9 shows the VFG based diode rectifier regulated DC system without ATRU/TRU. However, the power quality at the output of VFG is still poor.

Fig 1.10 shows the VFG based active rectifier regulated +/- 270V DC power system. In this system, similar to Fig. 1.7, the diode rectifier is replaced with an active rectifier to improve the power quality and efficiency of the VFG and at the same time to improve the transient response at the DC-link. It also helps to reduce the amount of DC-link capacitance required in the system with its fast switching and accurate torque control strategy.

In this dissertation, control improvements are proposed for different AC and DC backup power system architectures, to improve the transient step load response at the POR to help reduce the DC-link capacitance required in the PECs and at the same time to meet the aircraft MIL-STD transient voltage specifications at the POR with the reduced DC-link capacitance.

1.2 Summary of the contributions

This dissertation is focused on the following research objectives,

1. Minimization of DC-link capacitance in a VF Brushless Synchronous Generator (BSG) based diode rectifier regulated 270V DC power system.
2. Minimization of DC-link capacitance in a VF BSG based Diode Rectifier Inverter (DRI) regulated VSCF 115V, 400Hz AC system.

3. Minimization of DC-link capacitance in a VF BSG based active rectifier regulated DC system and active rectifier inverter regulated VSCF AC system.

4. EMI filter design for the PECs in AC and DC EPS and the investigation of the effects of EMI filters on the control algorithm for minimization of DC-link capacitance.

5. Modeling and simulation of the AC and DC aircraft EPS in PLECS and validating the effectiveness of the control algorithms in real-time controller Hardware in loop testing.

1.3 Organization of the dissertation

This dissertation is organized in the following manner,

In chapter 2, a VF BSG based diode rectifier regulated 50kW DC power system is studied. The DC-link voltage regulation is employed by controlling the field current of the exciter SG using two-quadrant DC chopper. Feedforward control improvements are proposed for the two-quadrant DC chopper control. The feedforward control improvements help to improve the transient step load response of the DC-link voltage regulation and to meet the MIL-STD704F transient voltage specification with minimized the DC-link capacitance. The control improvements are verified using PLECS simulation and Controller hardware in the loop (C-HIL) testing.

In chapter 3, a VF BSG based DRI regulated 80kVA VSCF AC system is investigated. The objective is to reduce the DC-link capacitance value and at the same time to meet the strict MIL standard transient voltage specifications at the 115V 400Hz AC

inverter output. In this chapter the control improvements from the BSG side DC chopper control is adapted with a novel adaptive inverter voltage reference (AIVR) algorithm in the inverter side control. The combined control improvements help to reduce the rate of change of DC-link voltage during transient step load at the inverter output and thereby reduces the DC-link capacitance required in the VSCF system. An 80 KVA VSCF system is modeled and simulated in PLECS with control improvements and the effectiveness of the control improvements are validated in C-HIL testing with 100uF DC-link capacitance.

In chapter 4, control improvements are proposed for a VF BSG based active rectifier regulated DC system to further improve the transient response of the DC-link voltage and to minimize the DC-link capacitance when compared to DRI based DC system. The proposed control algorithm also optimizes the field current of the exciter SG and the direct axis field current component of the BSG during steady state operating condition to maintain unity power factor operation at the BSG output terminals. The proposed control algorithm is also adapted into the active rectifier inverter regulated VSCF system along with inverter side AIVR algorithm from chapter 3. The control improvements are validated in real time C-HIL testing.

In chapter 5, the EMI filter design for VF BSG based PEC regulated DC and AC systems are studied for aircraft EPS by following DO-STD-160. The EMI filters are designed for different PECs in a 50kW active rectifier regulated DC systems such as two-quadrant DC chopper, and the active rectifier. The transient performance of the DC system control with minimized DC-link capacitance is compared for cases with and without EMI filters and the interaction of EMI filters with the fast transient control algorithms are studied and presented with real-time C-HIL testing results.

Chapter 6 concludes the dissertation by summarizing the key research contribution and discusses the future scope of the research in the areas such as: (1) Aircraft EPS with control improvements for the PEC based DC and AC systems with EMI filters; (2) The control improvements for the backup power system with loads in both 115V, 400Hz AC and 270V DC with strict AC and DC transient voltage limits; (3) The VF BSG machine model based exciter SG field current estimation to replace the look up table approach; and (4) Induction Generator (IG) based AC and DC systems with control improvements for minimization of DC-link capacitance.

CHAPTER 2

MINIMIZATION OF DC-LINK CAPACITANCE FOR BRUSHLESS SYNCHRONOUS GENERATOR (BSG) BASED DC POWER SYSTEM FOR DC LOADS

In this chapter, feedforward control improvements for minimizing the DC-link capacitance in a brushless Synchronous Generator (SG) based aircraft DC power system are proposed. The proposed techniques involve an output power based feedforward compensation for the DC-link voltage regulation control and a feedforward steady-state duty cycle compensation for the exciter SG field current control. This control scheme helps to meet the tight MIL-STD-704F transient voltage requirements for 270V aircraft DC power system with minimum DC-link capacitance. The proposed controller is validated through simulation and Controller Hardware-in-Loop (C-HIL) experiments for a 50KVA three-stage brushless SG system model with 600μF DC-link capacitance and results are provided at different speeds of the machine.

2.1 Introduction

In More Electric Aircraft (MEAs), DC power distribution is being increasingly considered for aircraft electrical power system (EPS) due to its reduced power loss and weight-saving aspects.

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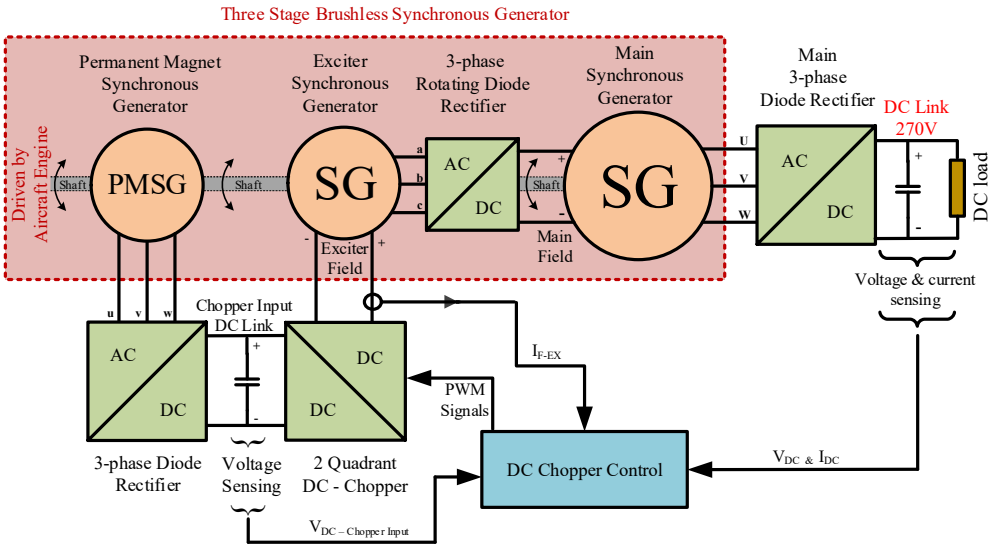


Fig. 2.1: Block diagram of the BSG based 270V DC power system.

The MEA such as Boeing 787 uses 270V DC distribution in addition to 115V AC at 400 Hz, and 28 V DC. The 270V DC supply is generated from 230V/115V, 300-800Hz AC output from variable frequency (VF) synchronous generators [2]–[4]. The aircraft DC loads are locally connected to the 270V DC bus using DC-link capacitor banks. These DC-link capacitors are space-consuming, heavy, and high in capacitance value due to the very tight transient voltage requirements from MIL-STD-704 [23]. Hence, efforts to minimize the DC-link capacitance value through suitable control techniques in a VF brushless synchronous generator (BSG) based DC power system as shown in Fig. 2.1 are presented in this chapter. Several control methods to reduce the DC-link capacitance for Pulse Width Modulation (PWM) active rectifier based DC power systems have been investigated in [24]–[26]. However, in most of the world's airplanes, passive diode bridge rectifiers are still being used. In [27], BSG based diode rectifier based active DC load with traditional buck converter control is used with 10mF DC-link capacitance is used for a 120kVA system. A deadbeat control for a 270V aircraft DC power system based on a three-stage BSG along with a diode rectifier is presented in [28].

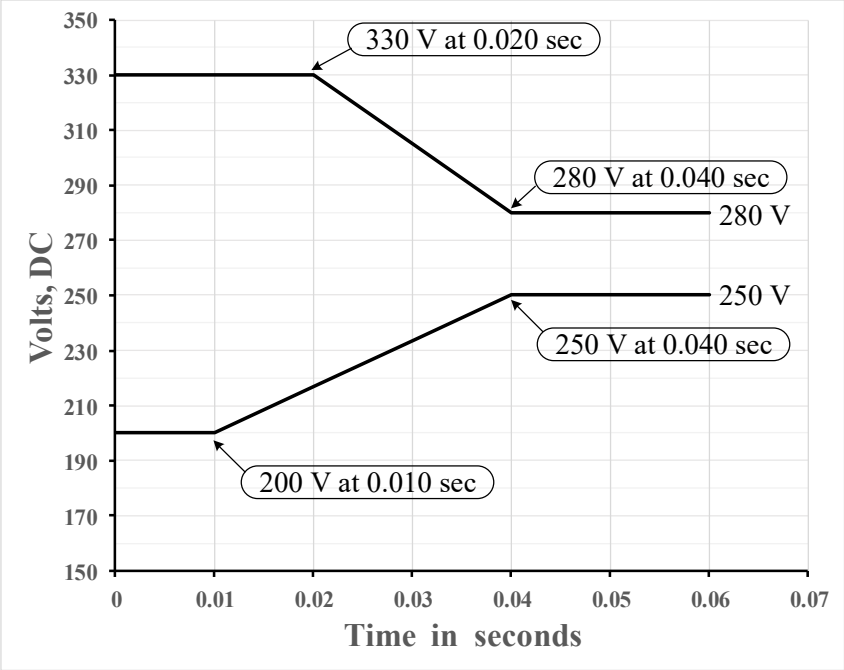


Fig. 2.2: MIL-STD-704 transient voltage specifications for 270V DC system [23].

This method demonstrates that the control is able to meet the MIL-STD-704F transient voltage specification as shown in Fig 2.2, for the 270V DC system at low and high-speed operations. Although the presented control method in [28] is able to meet the MIL transient voltage limits, this method does not address the issue of the high DC-link capacitance value required in the system. Moreover, not much research has been reported in the literature on the methodologies to achieve lower DC-link capacitance value in such applications. In this chapter, new feedforward control techniques are proposed to minimize the DC-link capacitance value required in the aircraft DC power systems. The two feedforward techniques for the three-stage SG system proposed in this chapter are 1) an output power based field current reference for the exciter SG field current control; 2) a steady-state duty ratio calculation to the DC chopper for field current control of exciter SG. The proposed control techniques help to achieve a better transient response for DC-link voltage regulation control and exciter SG field current control. This helps to minimize the

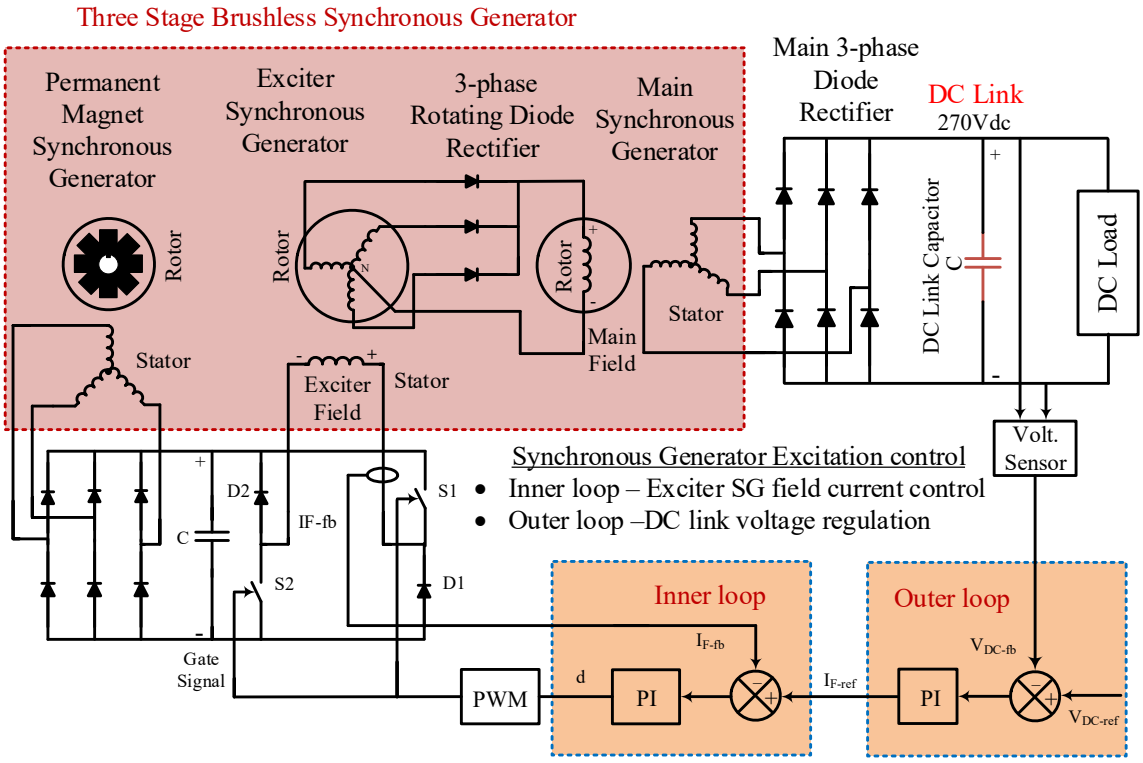


Fig. 2.3: Control block diagram of the DC-link voltage regulation and exciter SG field current control using two-quadrant DC chopper.

DC-link capacitance value required in the system and at the same time to meet MIL-STD-704F transient voltage limits for the 270V aircraft DC power system. The proposed controller is implemented for a BSG based 50kW DC power system modeled in PLECS and validated through PLECS and real-time simulations. The effectiveness of the control is verified in real-time using controller Hardware-In-Loop (C-HIL) emulator. The results prove that the control is able to meet MIL-STD-704F transient voltage limits with reduced DC-link capacitance of 600µF as compared to 2500µF, for both low and high-speed operations.

2.2 Controller for BSG based DC power system

Fig. 2.3 shows the control block diagram of the DC-link voltage regulation of the three-stage VF BSG based 270V aircraft DC power system. The three-stage BSG consists of a main SG, an exciter SG, a three-phase rotating diode rectifier, and a PMSG mounted

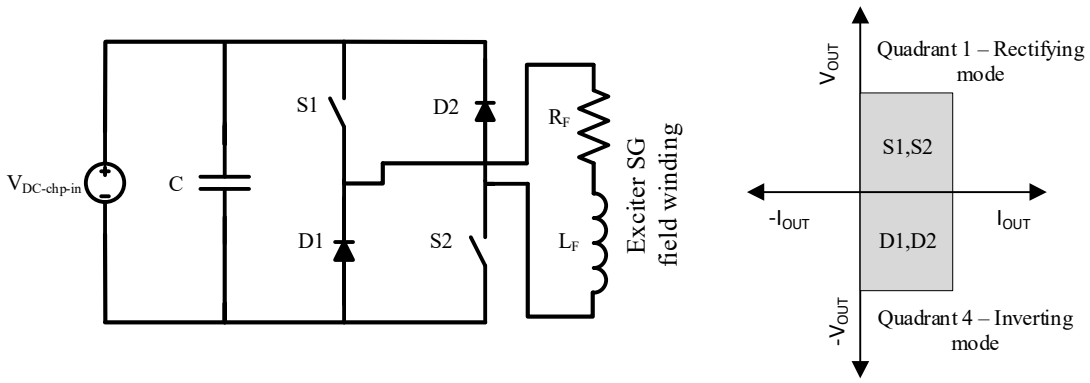


Fig. 2.4: Class D two-quadrant DC chopper.

on an extended single shaft which is coupled to the shaft of the High Pressure (HP) spool turbine of the aircraft main engine. The main SG generates three-phase variable frequency AC voltage which is then converted into DC voltage by using the main 3phase diode rectifier to form the DC-link of the VSCF power system. The DC-link voltage regulation is achieved by regulating the output voltage of the main SG through field excitation control of the exciter SG using a two-quadrant DC chopper. In order to design the exciter field current controller of the DC chopper, the steady state and averaged small-signal models of the DC chopper connected exciter SG field winding are studied.

Fig. 2.4 shows a class D two-quadrant DC chopper connected to the field winding of the exciter SG. The state space steady state model of the DC chopper connected exciter SG field winding is used to derive the steady state duty cycle of the DC chopper. At steady state condition, $AX + BU = 0$ so the state space equation becomes

$$\left[\frac{-R_F}{L_F}\right] I_F \ + \left[\frac{2D-1}{L_F}\right] V_{DC-chp \ \ in} = 0. \tag{2.1}$$

From (2.1), the duty cycle D can be derived as

$$D = \left[\frac{V_{DC-chp-\,in} \ + (I_F \, R_F)}{2V_{DC-chp-\,in}}\right], \tag{2.2}$$

where $V_{DC-chp-\,in}$ is the DC input voltage to DC chopper, I_F is the field winding current. If $V_{DC-chp-\,in}$ and the exciter field winding resistance R_F are known, the equation (2.2) can be used to calculate the steady state duty cycle D for a required amount of field winding current I_F. This steady state duty cycle D can be used in the exciter field current control as a feedforward compensation to improve the controller performance and to get faster transient response. Additionally, the averaged small signal model of the two-quadrant DC chopper is derived for the purpose of controller design. The state space equations for the DC chopper input and output currents are

$$\left[\ \dot{\hat{i}}_{L_F}\right] = \left[\frac{-R_F}{L_F}\right] \hat{i}_{L_F} + \left[\frac{2D-1}{L_F} \quad \frac{2V_{DC-chp \ \ in}}{L_F}\right] \begin{bmatrix} \hat{v}_{DC-chp \ \ in} \\ \hat{d} \end{bmatrix}, \tag{2.3}$$

and

$$[i_{in}] = [2D \ - 1] \ \hat{i}_{L_F}, \tag{2.4}$$

where $\hat{i}_{L_F}$ is the small signal inductor current, $\dot{\hat{i}}_{L_F}$ is the derivative form of the small signal inductor current, i_{in} is the input current of DC chopper, $\hat{v}_{DC-chp-\,in}$ is the small signal DC input voltage to DC chopper, and $\hat{d}$ is the small signal duty cycle. From equations (2.3) and (2.4), the small-signal duty to field current transfer function $\frac{\hat{i}_{L_F}(s)}{\hat{d}}$ is derived as

$$\frac{\hat{\imath}_{L_F}(s)}{\hat{d}} = \left[\frac{2V_{DC-chp\ \ in}}{R_F+SL_F}\right]. \tag{2.5}$$

It can be seen from the equation (2.5) that the two-quadrant DC chopper with exciter field winding is a first-order system and has a pole at $S = \frac{-R_F}{L_F}$, with the time constant $\tau = \frac{L_F}{R_F}$.

Table 2.1: System Parameters.

DESCRIPTION	VALUES		
THREE STAGE BSG			
	MAIN SG	EXCITER SG	PMSG
Normal speed range (N)	7 – 14 krpm	7 – 14 krpm	7 – 14 krpm
Number of pole pairs (PP)	8 (16 poles)	4 (8 poles)	8 (16 poles)
Output frequency (F_{SG})	933 – 1866 Hz	466 – 933 Hz	933 – 1866 Hz
Stator phase resistance (R_S)	0.13 Ω	0.07 Ω	1.17 Ω
Stator phase inductance (L_S) = (L_D + L_Q)/2 $L_D = L_{LS} + 3/2\ L_{MD}$; $L_Q = L_{LS} + 3/2\ L_{MQ}$	510 µH	317 µH	600 µH
Stator phase leakage inductance (L_{LS})	60 µH	44 µH	
Magnetizing inductance in D-axis (L_{MD})	250 µH	175 µH	
Magnetizing inductance in Q-axis (L_{MQ})	350 µH	190 µH	
Turns ratio between stator winding and field winding; used for referring field winding variables to the stator	0.1531	0.04284	
Field winding resistance (R_F); value referred to the stator	(1.144 * (0.1531)^2) Ω	(10 * (0.04284)^2) Ω	
Field winding leakage inductance in q-axis (L_{LFD}); value referred to the stator	4.3 mH * (0.1531)^2	22 mH * (0.04284)^2	
D-axis damper winding resistance (R_{KD}) referred to the stator	0.2034 Ω		
Q-axis damper winding resistance (R_{KQ}) referred to the stator	0.0746 Ω		
Damper phase winding leakage inductance in d-axis (L_{LKD}) referred to the stator	50 µH		
Damper phase winding leakage inductance in q-axis (L_{LKQ}) referred to the stator	20 µH		
MAIN DIODE RECTIFIER			
DC output voltage (DC-link)	270 V		
DC-link capacitance (designed value for 50kW)	2500 µF based on transient operation results from simulation		

A cascaded loop voltage control strategy is used for DC-link voltage regulation, as shown in Fig. 2.3. The outer loop DC-link voltage regulation is based on a Proportional and Integral (PI) controller which generates the excitation field current reference to the

inner current loop. The PI controller gains selected for rated 50kW operation at 14000rpm are Kp = 0.0001 and Ki = 0.3. The inner current loop PI controller regulates the excitation field current of the exciter SG. The inner current loop PI controller is designed based on

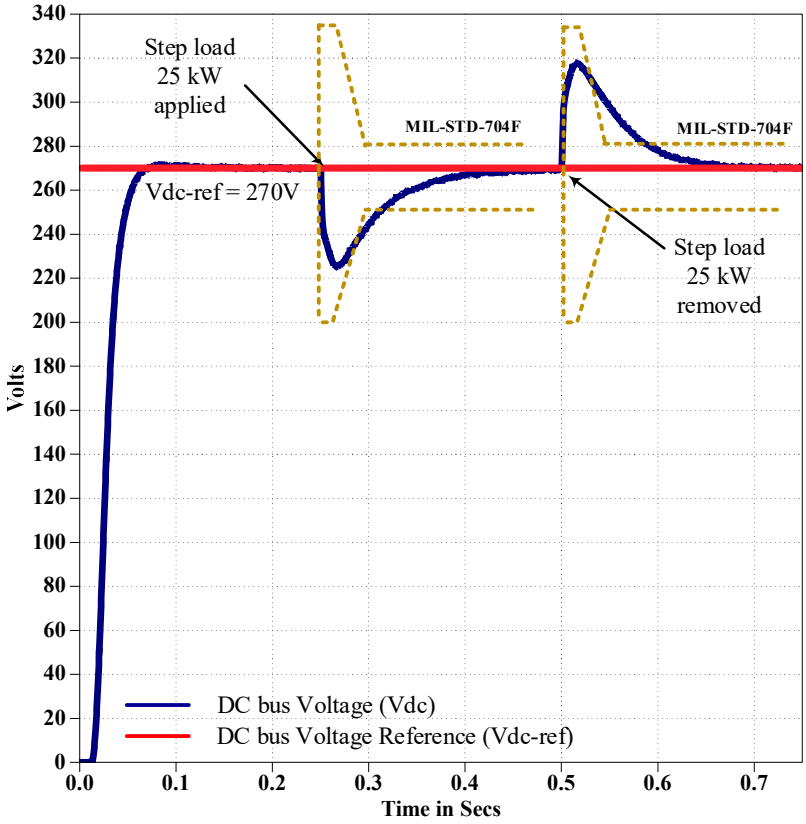


Fig. 2.5: DC-link voltage regulation waveform for 2500μF DC-link capacitance without any control improvements for 25kW step load at 7000rpm.

pole placement technique. The PI controller gains selected for rated 50kW operation at 14000rpm are Kp = $L_F * gain$ = 22, Ki = $\frac{R_F}{L_F}$. = 454. Table 2.1 shows the machine parameters of the system under study. The simulation results of DC bus voltage regulation with 2500μF DC-link capacitor are shown in Fig. 2.5 and 2.6 for 7000rpm and 14000 rpm with a rated power of 25kW and 50kW step load respectively. It can be seen from Fig. 2.5 and 2.6 that the DC-link voltage is regulated at 270V for both 7000rpm and 14000rpm.

Furthermore, the transient response shows that the DC chopper controller is able to successfully recover the DC-link voltage back to 270V during the step load application and removal. Though the DC chopper controller provides stable operation at the DC-link during transient and steady-state conditions for both low and high speed operation, the rate of

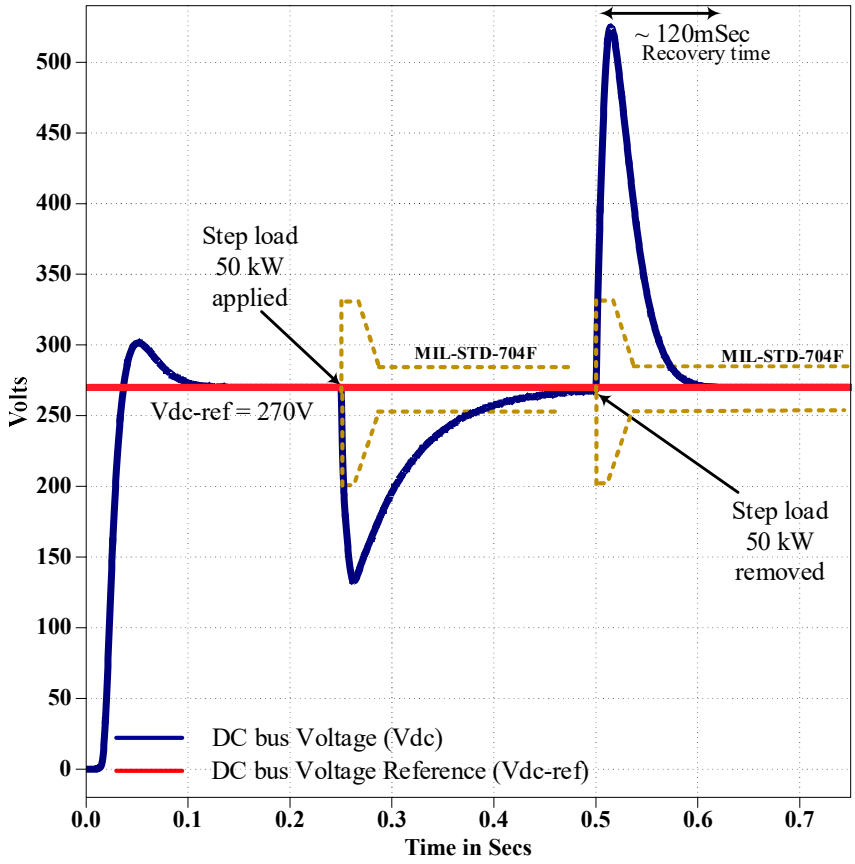


Fig. 2.6: DC-link voltage regulation waveform for 2500μF DC-link capacitance without any control improvements for 50kW step load at 14000rpm.

change of DC-link voltage during transient step load is very high. As a result, the 270V DC system is not able to meet MIL-STD-704F transient voltage limits for rated power 50kW step load during high-speed operation (14000rpm), as shown in Fig. 2.6. It can also be seen from Fig. 2.6 that, the DC-link voltage overshoots more than 500V (which is beyond the limits suggested in MIL-STD-704F), during high-speed operation for 50kW step load

removal. This is mainly because the excitation current required during high-speed operation is very low when compared to the low-speed operation. This limits the PI controller gain margin for DC-link voltage regulation during step load at high-speed operation [28]. Hence, it is evident that the conventional DC chopper controller for the BSG based DC power system does not work effectively at high speed operation and thus the 270V DC power system is not able to meet the MIL-STD-704F transient voltage requirements even with 2500μF DC-link capacitance.

2.3 Feedforward control techniques for BSG based DC power system

One of the main requirements of the 270V aircraft DC power system is to meet the MIl-STD-704F transient voltage limits at the DC-link. In order to achieve tight transient voltage specifications, the DC-link capacitors need to be sized with very high value. Moreover, the conventional DC-link voltage regulation control of the BSG based DC system is limited by poor transient response time. To overcome these limitations, two feedforward compensation techniques are introduced to the two-quadrant DC chopper control:

1) Steady-state duty cycle based feedforward compensation for inner current loop controller.

2) Lookup table based feedforward exciter field current reference for outer voltage loop controller based on output power.

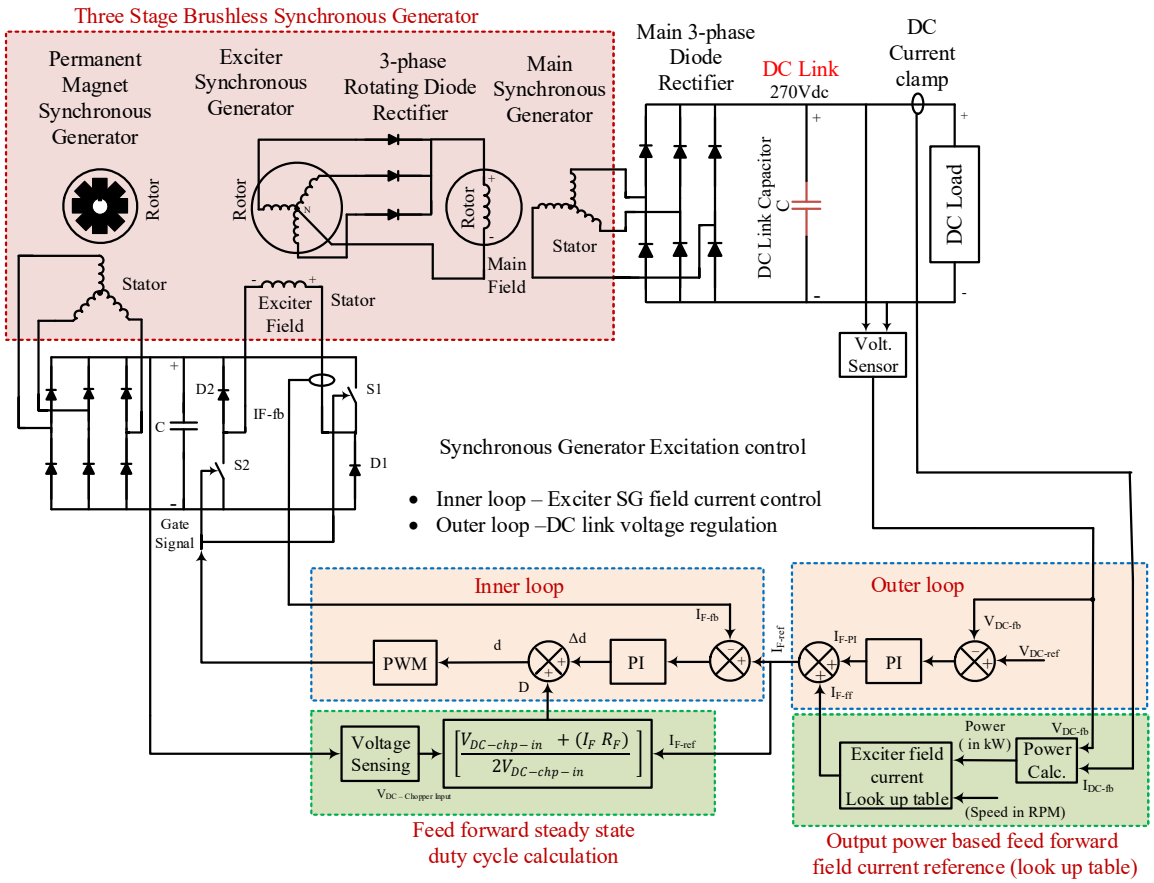


Fig. 2.7: Control block diagram of the exciter field current control and DC-link voltage regulation with feedforward compensation.

Fig. 2.7 shows the control block diagram of the DC-link voltage regulation of the three-stage VF BSG based DC power system with feedforward compensations added to the DC chopper control. As shown in Fig. 2.7, the steady-state duty cycle for a two-quadrant DC chopper from equation (2.2) is added as a feedforward compensation to the output of the inner current loop PI controller. During transient operations such as heavy step load application or step load removal at the DC-link, the steady-state duty cycle 'D' provides an instantaneous change required in the DC chopper duty cycle to regulate the exciter SG field current.

Table 2.2: Feedforward field current reference Look up table (in Amps) for Exciter SG.

		Load in kW					
		0	10	20	30	40	50
Speed in RPM	7000	1.5	2.3	3	3.7	4.3	4.9
	8000	1.3	1.9	2.45	3.1	3.6	4.1
	9000	1.1	1.55	1.98	2.48	2.95	3.45
	10000	0.9	1.3	1.68	2.03	2.41	2.8
	11000	0.82	1.15	1.53	1.89	2.15	2.48
	12000	0.73	1.03	1.31	1.59	1.88	2.22
	13000	0.64	0.9	1.22	1.47	1.7	1.9
	14000	0.5	0.8	1.1	1.31	1.52	1.6

Generally, the inner loop field current control response is faster than the outer voltage loop since it only involves the exciter field winding time constant. On the other hand, the DC-link voltage regulation and its transient response heavily depend on the performance of the outer loop voltage controller of the DC chopper. In the outer voltage loop, a lookup table based feedforward compensation is added to the PI controller output to provide a combined field current reference to the inner current loop control, as shown in Fig. 2.7.

Table 2.2 shows the feedforward exciter field current reference lookup table which is obtained through the simulation of brushless SG for different DC load power at different speed conditions. During the load transient operations, the steady-state field current reference from the lookup table is added to the output of the voltage loop PI controller to provide the instantaneous change in the field current reference required at the input of the inner control loop. This helps in faster recovery of the DC-link voltage during heavy step load. Moreover, the rate of change of DC-link voltage during step load can also be reduced since the feedforward compensation provides instantaneous change required at the input of the exciter SG field current control for any instantaneous change in the output power.

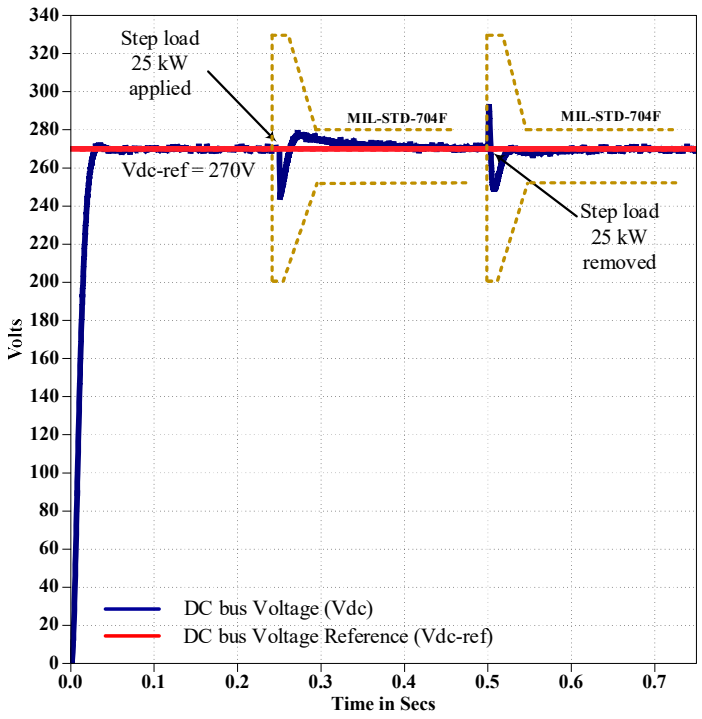


Fig. 2.8: DC-link voltage regulation waveform for 600µF DC-link capacitance when feedforward compensation is enabled for 25kW step load at 7000rpm.

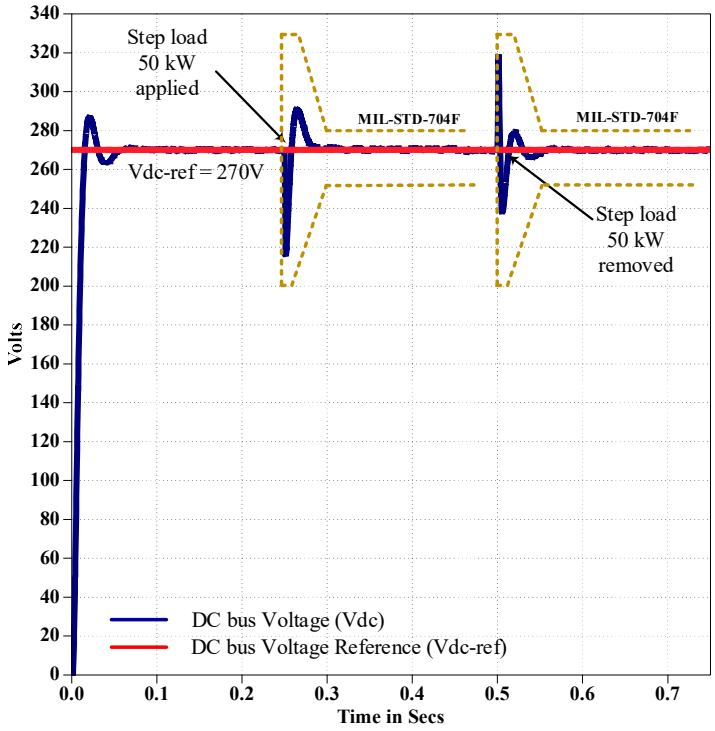


Fig. 2.9: DC-link voltage regulation waveform for 600µF DC-link capacitance when feedforward compensation is enabled for 50kW step load at 14000rpm.

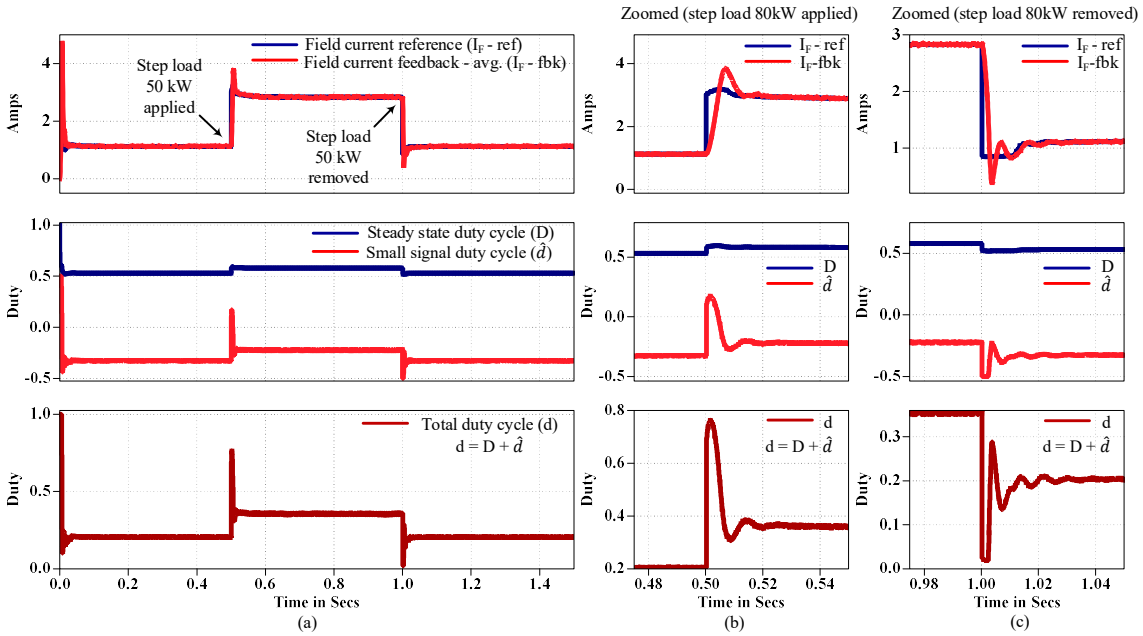


Fig. 2.10: (a) Exciter field current control transient response for 50kW step load during 14000rpm when feedforward compensation is enabled; (b) During step load 50kW is applied; (c) During step load 50kW is removed.

The simulation results of DC bus voltage regulation using 600µF DC-link capacitor using the feedforward compensation techniques at various speeds - 7000rpm and 14000 rpm and under rated power of 25kW and 50kW step load respectively, are shown in Fig. 2.8 and 2.9. When the feedforward compensation is enabled for both inner and outer loop controllers of the DC chopper, significant improvement can be observed in the transient response of the DC-link voltage when compared to the transient response without feedforward compensation.

It can be seen from Fig. 2.8 and 2.9 that the DC-link voltage recovery time during transients operation has reduced significantly to less than "~40mSec" which is only ~1/5th of the recovery time observed without feedforward compensation. Moreover, the DC-link capacitance value has been reduced significantly to a lower value of 600µF, and more

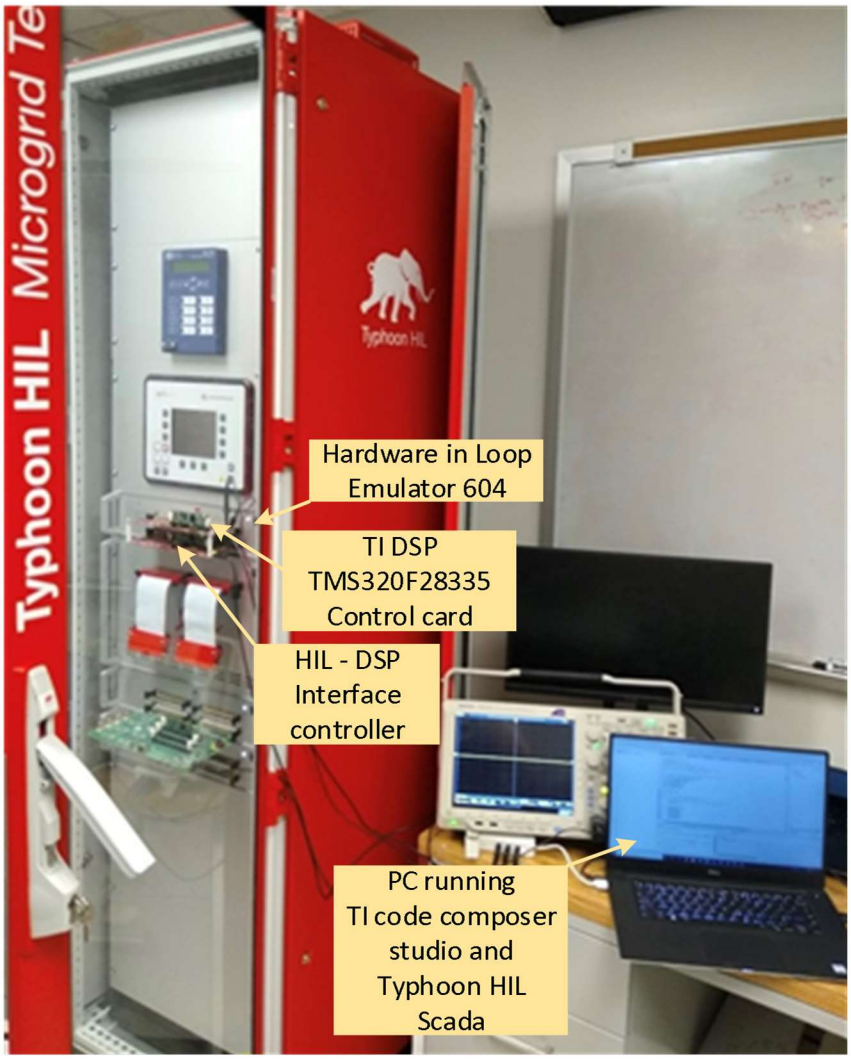


Fig. 2.11: Controller Hardware-In-Loop (C-HIL) real-time simulation testbed.

importantly, the 270V aircraft DC power system is able to meet MIL-STD-704F transient voltage limits with minimum DC-link capacitance. Fig. 2.10 (a), (b) and (c) show the exciter field current control transient response for 50kW step load during 14000rpm when feedforward compensation is enabled.

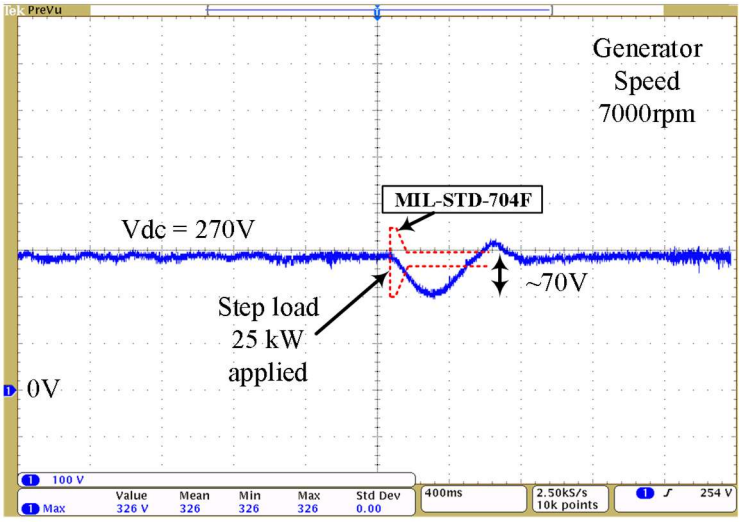
2.4 Real-time C-HIL testing and results

The proposed feedforward control improvements for DC-link voltage regulation of a BSG based DC aircraft power system using two-quadrant DC chopper is verified in real-

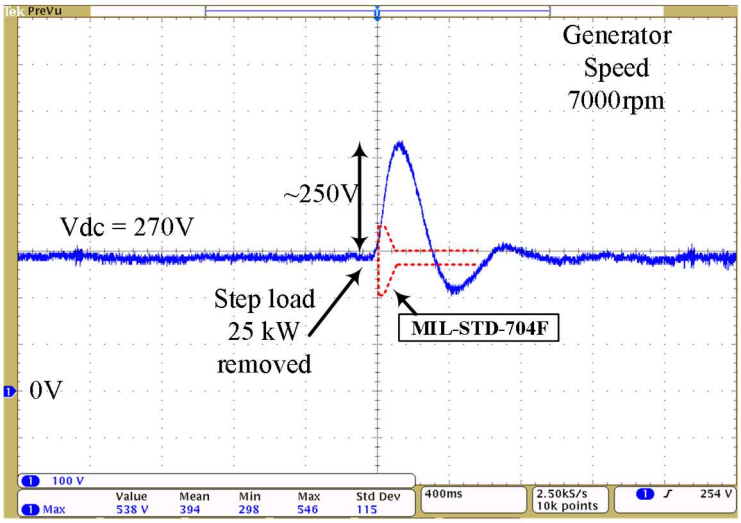
time C-HIL simulation. Fig. 2.11 shows the C-HIL real-time simulation testbed based on Typhoon HIL 604 emulator and Texas Instruments (TI) Digital signal processor (DSP) TMS320F28335 based controller. The three-stage BSG, two-quadrant DC chopper, and three phase diode rectifier are modelled in Typhoon HIL emulator using the system parameters from table 2.1.

The two-quadrant DC chopper control is implemented in TI DSP. The switching PWM carrier frequency is selected as 40 kHz. The exciter SG field current controller is processed at 40kHz in the inner loop same as the PWM frequency and the DC bus voltage controller in the outer loop is processed at 8kHz which is 1/5 the processing speed of the current controller. The processor bandwidth utilization is about 80%. Typhoon HIL SCADA environment is used to apply and remove step load to the system, and also to monitor the generator and DC bus voltages and currents. TI code composer studio is used to debug, monitor, and control the real-time control parameters such as PID tuning of controllers.

The DC chopper control is implemented in the per-unit system. The PI values chosen in the DSP for the current controller are Kp_current = 0.01 and Ki_current = 0.2. The PI values chosen for voltage controller are Kp_voltage = 0.0015 and Kp_voltage = 0.04. The feedforward steady-state duty ratio ‘D’ is calculated based on equation (2.2) and the feedforward exciter field current reference is provided from table 2.2.



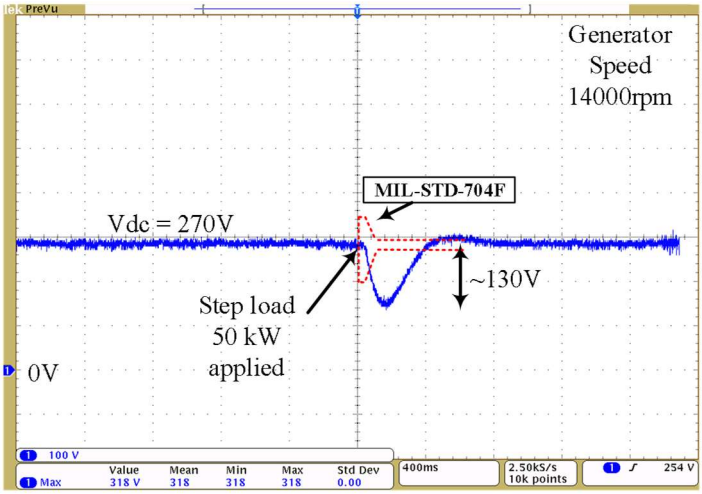
(a)



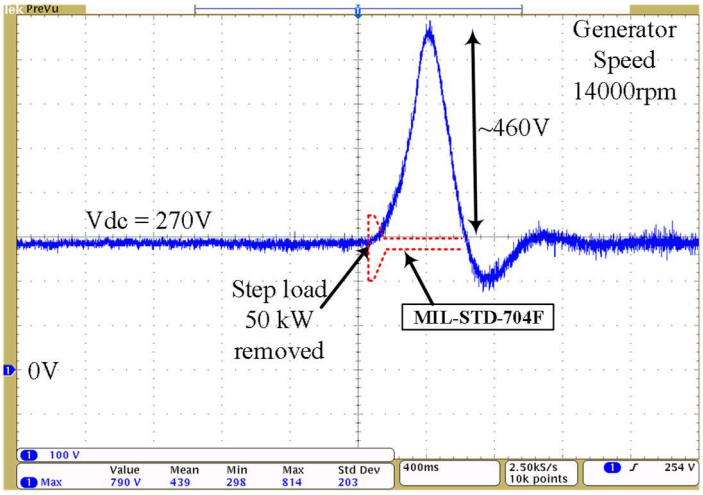
(b)

Fig. 2.12: DC-link voltage regulation waveform from HIL for 2500µF DC-link capacitance without any control improvements for speed 7000rpm: (a) 25kW step load applied; (b) 25kW step load removed.

The C-HIL simulation results for the BSG based DC power system using two-quadrant DC chopper are shown in Fig.2.12 to 2.15. Fig. 2.12 (a) and (b) and Fig. 2.13 (a) and (b) show the real-time C-HIL simulation results for DC-link voltage regulation using 2500µF DC capacitor with conventional DC chopper control without feedforward control improvements for speed 7000rpm and 14000rpm, and with 25kW and 50kW step load



(a)



(b)

Fig. 2.13: DC-link voltage regulation waveform from HIL for 2500µF DC-link capacitance without any control improvements for speed 14000rpm: (a) 50kW step load applied; (b) 50kW step load removed.

changes, respectively. It can be seen from Fig. 2.12 and 2.13 that the C-HIL results match closely with the PLECS simulation results shown in Fig. 2.5 and 2.6.

Fig. 2.14 (a) and (b), and fig. 2.15 (a) and (b) show the DC-link voltage regulation waveforms from C-HIL testing for 600µF DC-link capacitor with feedforward control improvements enabled for speeds 7000rpm and 14000rpm, and with 25kW and 50kW step load changes, respectively.

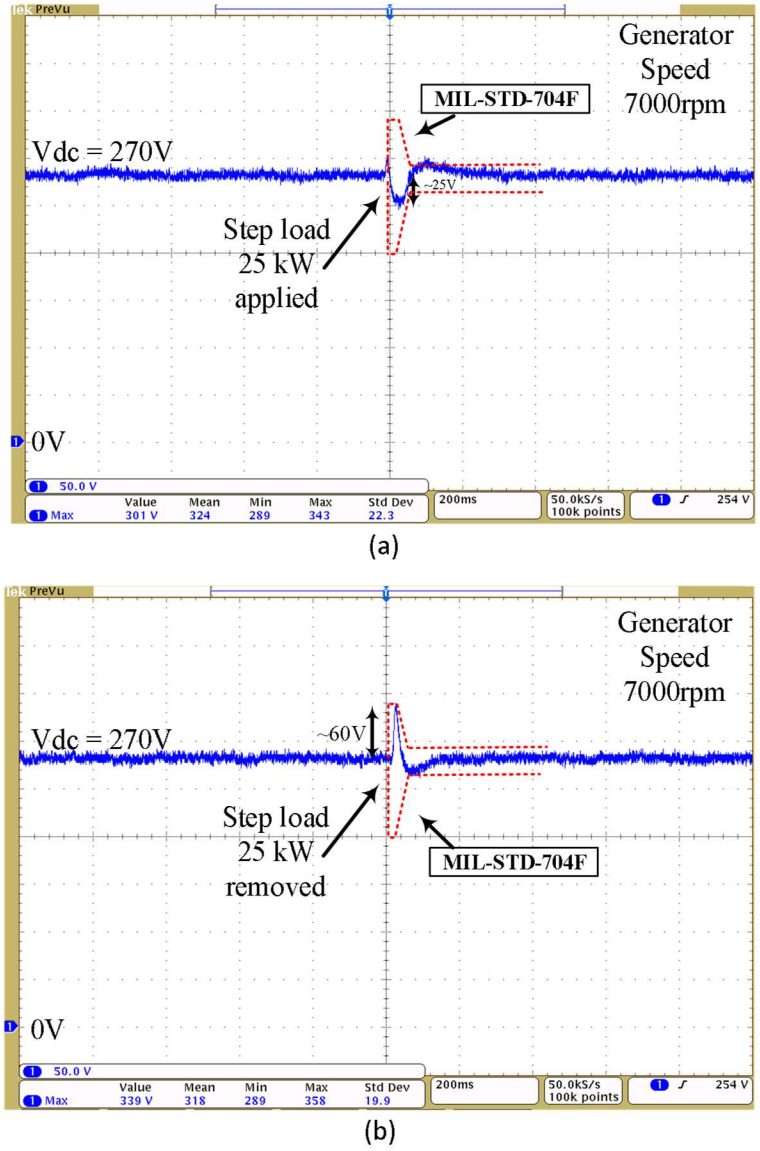
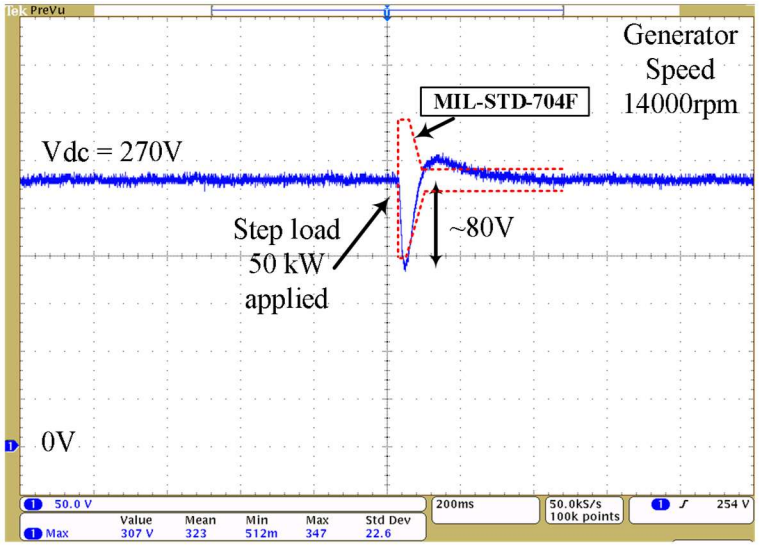
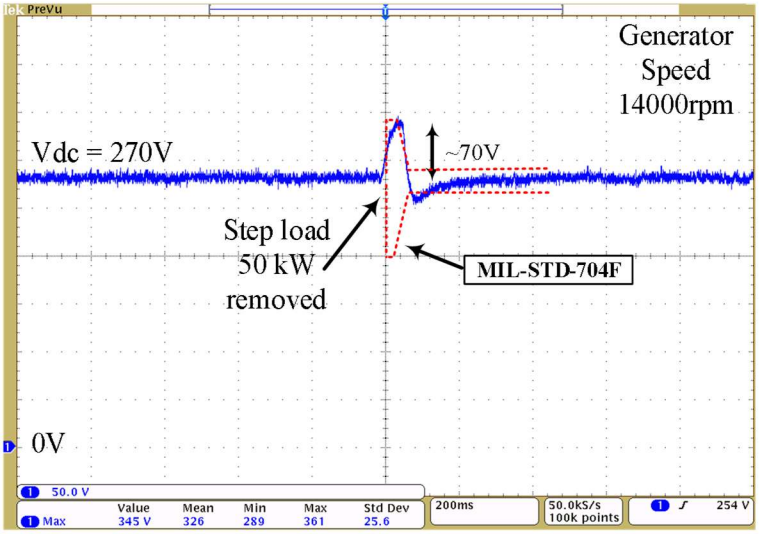


Fig. 2.14: DC-link voltage regulation waveform from HIL for 600µF DC-link capacitance with feedforward compensation enabled for speed 7000rpm: (a) 25kW step load applied; (b) 25kW step load removed.

The C-HIL real-time simulation results of the feedforward control matches closely with the PLECS simulation results and hence the controller is able to meet the MIL-STD-704F for DC system with a minimum DC capacitance of 600µF.



(a)



(b)

Fig. 2.15: DC-link voltage regulation waveform from HIL for 600µF DC-link capacitance with feedforward compensation enabled for speed 14000rpm: (a) 50kW step load applied; (b) 50kW step load removed.

2.5 Summary

In this chapter, feedforward control improvements for a three-stage BSG based 270V 50kW aircraft DC power system to minimize the DC-link capacitance are proposed. The proposed control techniques, namely, an output power based feedforward compensation for DC-link voltage regulation and a feedforward steady-state duty cycle

compensation for the exciter SG field current control can be easily integrated into conventional brushless SG control without any additional hardware requirements. The DC-link capacitance value of as low as 600μF could be achieved as compared to larger values above 2500μF present in the existing DC power system with conventional control method, by still meeting the transient output voltage requirements as per MIL standards. The concept is validated through aircraft power system modeling and extensive simulation using PLECS and C-HIL with satisfactory results at different operating speeds and load transient conditions as per MIL-STD-704F requirements.

2.6 Publications

1. G. Selvaraj, K. R. Ramachandran Potti, K. Rajashekara, "An Improved Feedforward Controller for Minimizing the DC-link Capacitance in a Brushless Synchronous Generator based Aircraft DC Power System*," in Proc. IEEE ITEC*, June 2021.

CHAPTER 3

MINIMIZATION OF DC-LINK CAPACITANCE FOR BRUSHLESS SYNCHRONOUS GENERATOR (BSG) BASED VSCF SYSTEM

3.1 Introduction

The Electrical Power System (EPS) in the aviation industry has gone through major transformations over the past several decades. Various DC and AC architectures have been used in the aircraft such as 28V DC, 115V AC at 400Hz Constant Voltage Constant Frequency (CVCF), and Constant Voltage Variable Frequency (CVVF) of 230V,300-800Hz and then converting it into 115V, 400Hz and 270V DC (in aircraft such as A380 and B787) [1]–[3]. Though many modern aircraft including More Electric Aircraft (MEA) are currently using CVVF AC architecture, majority of the aircraft electrical equipment are legacy loads that have to be supplied with 115V, 400Hz AC and 28V DC [2], [3], [6], [22], [29]. For main power generation in MEA systems, the CVVF AC is mainly used and is generated by using Variable Frequency Generators (VFGs) [9], [30]. Though VFGs have replaced the CVCF Integrated Drive Generators (IDGs) in MEAs for main power generation, IDGs are still used in a few modern aircraft for backup power generation [31]. Since the IDGs are less reliable and less efficient due to their mechanical gear arrangements, power electronic converter (PEC) based VSCF systems are gradually replacing the IDGs in backup power generation [2], [3], [24]. One of the main advantages of VSCF system as compared to IDG is that the PEC can be mounted anywhere in the aircraft. This helps in reducing the size of the backup generator and also gives flexibility in the aircraft weight distribution.

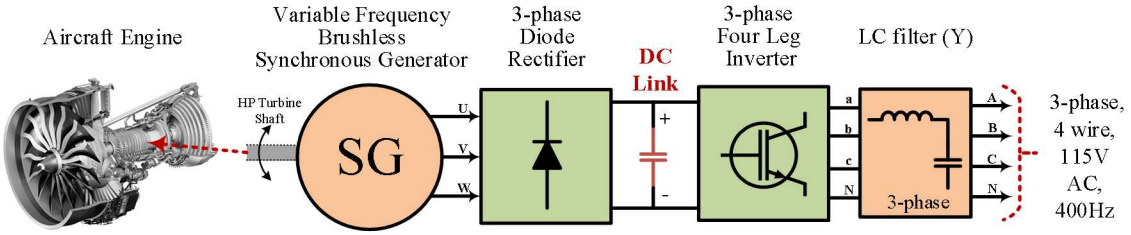


Fig. 3.1: Block diagram of the BSG based DC power system.

The DC-link based VSCF systems as shown in Fig. 3.1 are more commonly used in civil aircraft, such as MD90, and B777 backup power generation [1], [3], [31]. In this type of Diode Rectifier-Inverter (DRI) based system, it is estimated that the DC-link capacitors consume about 20 to 25% of the total volume of the PEC, which is quite high. This chapter focuses on proposing conceptual strategies to minimize the DC-link capacitance in the DRI based VSCF system in aircraft.

A number of techniques have been proposed in the literature to minimize the DC-link capacitance in PECs [24], [32], [33]. VSCF based on PWM converter-inverter configuration in [24] uses a DC-link capacitor current control on the PWM rectifier side along with a feedforward compensation. A feedforward control of PWM rectifier based on inverter output power variation is proposed in [32]. These feedforward compensation techniques based on output power can improve the stability of the PWM rectifier-inverter system with reduced capacitance. However, such methods have not been addressed to meet the output transient specifications for the inverter while switching heavy loads. Although these control methods could significantly reduce the DC-link capacitance value in the PEC, they are not suitable for DRI systems because the diode rectifiers are not controllable. Various control methods that use inverter side control of DRI systems are proposed in [34]–[38].

Since the reduction in DC-link capacitance increases the voltage fluctuations, which can lead to instability challenges, the methods used in [34]–[38] are mainly focused on DC-link voltage stabilization and ripple reduction. An active damping strategy to stabilize the DC-link voltage is proposed in [36]–[38]. In [36], the DC-link voltage fluctuation during step load change is suppressed by adjusting the d-axis voltage tolerance range in the inverter control. This method demonstrates a significant amount of reduction in DC-link capacitance (4.5μF/kW) for DRI systems. It involves estimation of source current, which needs source impedance and input filter parameters that are not readily and accurately available. Moreover, the methods in [36]–[38] consider only for fixed frequency grid source applications and are not easily adaptable for variable frequency generating systems. One of the major challenges in the aircraft EPS is to meet the MIL-STD-704F transient voltage specifications which need further control improvements to minimize the DC-link capacitance.

In this chapter, a novel output power based Adaptive Inverter Voltage Reference (AIVR) algorithm is proposed for the inverter side control to minimize the DC-link capacitance of the DRI based VSCF aircraft power systems. In addition, the paper proposes a DC-link voltage regulation control on the VFG side with feedforward compensations to improve the transient response of the DC-link voltage regulation. The proposed AIVR algorithm adopts the control of four-leg inverter to adaptively match with the generator side dynamics, which helps to meet the inverter output requirements for different transient load operating conditions over the entire speed range, with reduced capacitance. Moreover, both VFG side and inverter side controllers are independent to each other so that a decentralized control scheme for VSCF systems can be realized to achieve better weight

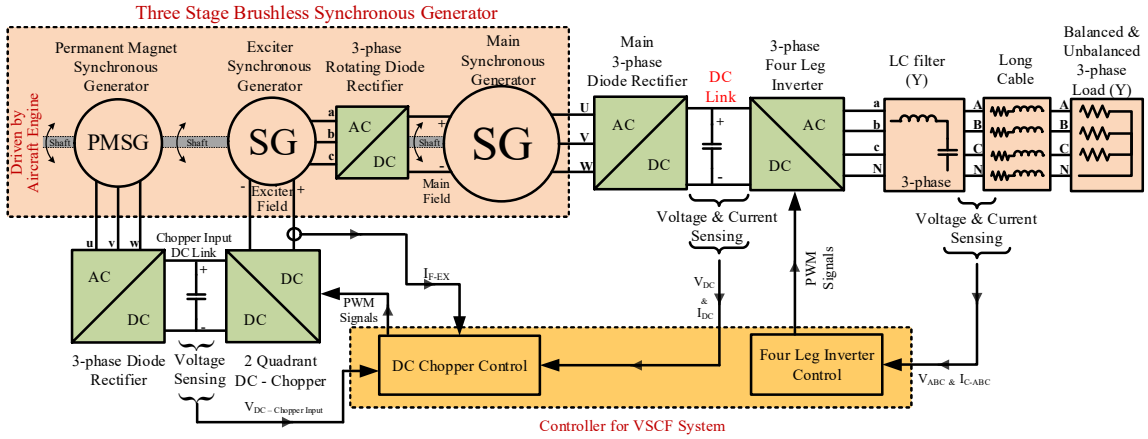


Fig. 3.2: Block diagram of a BSG based VSCF aircraft AC power system.

distribution in the aircraft. In this chapter, the proposed control improvements are validated through extensive simulation and controller hardware in loop testing (C-HIL).The VSCF operation with reduced DC-link capacitance (by 95% of the value when compared to conventional control method and still satisfying the MIL-STD-704F AC voltage transient requirements at the Point of Regulation (POR) is also successfully demonstrated.

3.2 System overview

Fig. 3.2 shows the block diagram of a brushless Synchronous Generator (BSG) based DC-link DRI VSCF aircraft AC power system. The VFG used in this system is a three-stage BSG. It consists of a main SG, an exciter SG, a three-phase rotating diode rectifier, and a PMSG. They are mounted on an extended single shaft which is coupled to the shaft of the High Pressure (HP) spool turbine of the aircraft main engine. The field winding of the main SG is excited with a DC voltage that comes from a 3phase rotating diode rectifier which converts the AC output voltage from the exciter SG into DC voltage. The exciter SG has stationary field and rotating armature; and the stationary field winding of the exciter SG is excited using a two-quadrant DC to DC converter, also known as two-

quadrant DC chopper. The AC output voltage generated by the PMSG is converted into DC voltage and given as the input to this two-quadrant DC chopper. The operating speed of the HP spool turbine in the modern aircraft main engine is typically in between 7000 and 14,000 rpm [3], [31]. For this speed range, a 16 pole main SG generates a three-phase AC voltage with variable frequency in the range of 933.3 to 1866.6 Hz. This variable frequency AC voltage is then converted to DC voltage by using the main 3phase diode rectifier to form the DC-link of the VSCF power system. The DC-link voltage regulation is achieved through an excitation control of the BSG using the two-quadrant DC chopper. A three-phase four-leg inverter along with an output LC filter is used to convert the DC voltage from DC-link to a three-phase, four-wire, sinusoidal, 400Hz fixed frequency, 115V AC voltage at the POR. A long feeder cable delivers the inverter output from POR to the aircraft AC loads. The control schemes for two-quadrant DC chopper and four-leg inverter are discussed in Section 3.4.

3.3 Selection criteria for choosing minimum DC-link capacitance for VSCF system

To make the VSCF system suitable and attractive for aircraft applications, higher power density is one of the major requirements. DC-link capacitance in a VSCF system is one of the critical components which needs to be reduced to achieve higher power and volume densities. In aerospace applications, film capacitors are more commonly used as DC-link capacitors in PECs due to their ability to handle high-temperature operation, high ripple current capacity [39], [40], and most importantly smaller in size when compared to

the bulky electrolyte capacitors. For such critical systems, the minimum value of DC-link capacitance chosen should meet three main criteria, they are,

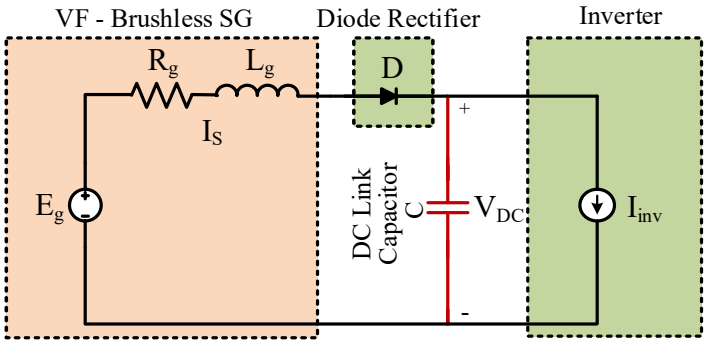


Fig. 3.3: Simplified equivalent circuit model of the VFG connected DRI system with DC-link capacitance.

1. To maintain stable operation during steady-state and transient conditions.
2. To meet DC-link voltage ripple requirements.
3. To meet transient output voltage requirements during step load conditions.

The theoretical minimum DC-link capacitance for DRI systems to meet system stability (Criteria 1) is derived in [34]–[38]. In this method, a simplified equivalent circuit is modeled with input source, diode rectifier, and inverter as shown in Fig. 3.3, and the minimum DC-link capacitance ($C_{DC\text{-}min}$) value is calculated as

$$C_{DC-m} \geq \left[\frac{P_{DC} * L_g}{V_{DC}^2 * R_g}\right], \tag{3.1}$$

where P_{DC} is the output power at DC-link, L_g is the equivalent input source inductance ($L_g = 2L_S$), R_g is the equivalent input source resistance ($R_g = 2R_S + \frac{3\omega_S * L_S}{\pi}$), L_S and R_S are the source inductance and resistance, ω_S is the input source frequency in radians/sec, and V_{DC} is the DC-link voltage.

Table 3.1: Minimum DC-link capacitance and ripple calculation

	For 7krpm, P_{DC} = 40kW	For 14krpm, P_{DC} = 80kW
$C_{DC\text{-}min}$ (based on eqn. 1)	45.04µF	46.93 µF
% $ripple_{pk\text{-}pk}$ (based on eqn. 2) (C_{DC} from eqn. 1)	3.33%	3.19%

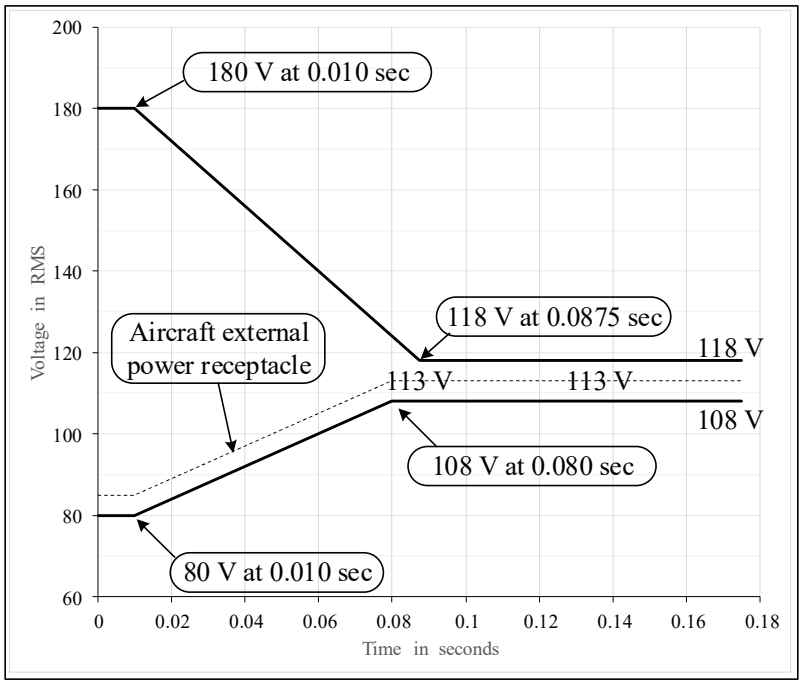


Fig. 3.4: MIL-STD-704F AC voltage transient limits [23].

In order to meet the voltage ripple requirement (Criteria 2) at the DC-link for film capacitors, the method used in [39] should be considered, which is given as

$$C_{DC} = \left[\frac{P_{DC}}{240 * V_{ripple} * V_{S-r} \quad * f_S}\right], \tag{3.2}$$

where V_{S-rms} is the phase rms voltage at the input of the diode rectifier, V_{ripple} is the peak to peak (pk-pk) ripple voltage at the DC-link, and f_S is the input source frequency in Hz. Though criteria 2 is one of the main requirements for selecting minimum DC-link capacitance, the design for steady-state and transient operation could still meet satisfactory ripple voltage for the DC-link of the VSCF system as calculated per criteria 1.

The equations (3.1) and (3.2) guarantee the stability and DC-link voltage ripple of the DRI system during steady-state and transient conditions. However, to meet the inverter output voltage transient requirements (Criteria 3) during step load conditions, the minimum DC-link capacitance required is determined based on factors such as; maximum allowed rate of change of DC-link voltage during step load at the inverter output, maximum allowed rate of change of AC output voltage and transient recovery time based on MIL-STD-741F as shown in Fig. 3.4, rated DC-link voltage and the required AC output voltage that determine the modulation index of the inverter control during step load, stiffness of the input source, control methods, etc. Hence, the minimum DC-link capacitance value required to meet criteria 3 differs from system to system and generally, the value chosen is multiple times the value calculated based on criteria 1 and 2 to meet criteria 3.

For the VSCF system studied in this paper, the input source is a VF BSG with the output AC frequency range from 933.3Hz to 1866.6Hz for the speed range 7000rpm to 14000rpm. The rated power at the DC-link are 40kW and 80kW for the speed 7000rpm and 14000rpm respectively. Hence, the minimum DC-link capacitance values are calculated for both lower and upper limit frequencies at rated DC-link power using (3.1) and the corresponding DC-link ripple percentage (%) are calculated using (3.2) as shown in Table 3.1. The value calculated based on (3.1) is used as a theoretical minimum DC-link capacitance for the simulation of the 80kVA VSCF system. The equations (3.1) and (3.2) are used to calculate the minimum DC capacitance for the VSCF system to meet the stability criteria and voltage ripple requirements. However, the calculated DC-link capacitance value may not be enough for the VSCF system to meet the strict MIL-STD-704F transient voltage specifications at the 115V 400Hz AC output as shown in Fig. 3.4.

Therefore, in order to meet the inverter output voltage limits during transient conditions, a minimum value of DC-link voltage has to be maintained and the minimum DC-link capacitance value has to be chosen such that the rate of change of DC-link voltage is minimum during step load and the DC-link voltage stays above the minimum required voltage to meet the required minimum inverter AC output voltage as required by MIL-STD-704F.

The minimum DC-link voltage required to meet the minimum inverter output voltage limit during transient load condition is calculated as

$$V_{DC-} = (V_{out-ph-rms-mi} + V_{fil-drp-ph-r}) * \sqrt{6}, \quad (3.3)$$

where $V_{out-ph-rms-m}$ is the minimum AC output voltage required during transient condition based on MIL-STD-704F and $V_{fil-drp-ph-}$ is the voltage drop across the output filter. For the VSCF system considered in this paper, the initial DC-link capacitance value chosen for the simulation is 50μF based on (3.1).

3.4 Control of VSCF system and simulation results

Fig. 3.5 shows the control block diagram of the DC-link based DRI VSCF system. A brief description on the BSG side control, four-leg inverter side control, and the combined VSCF system control are discussed in the following subsections. The simulation results for 50μF DC-link capacitance in the 80kVA VSCF system operated under steady-state and transient step load conditions are provided.

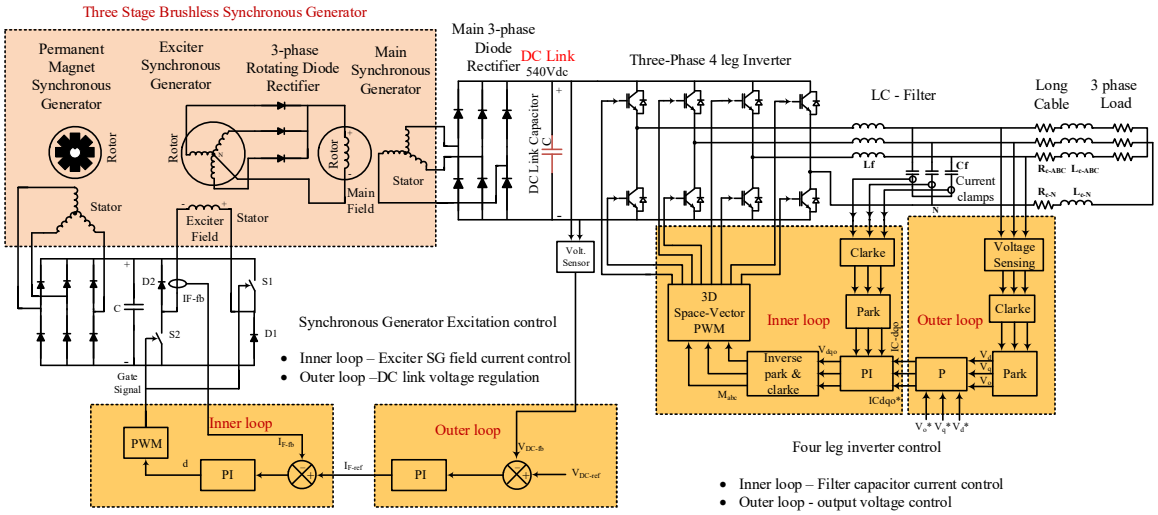


Fig. 3.5: Control block diagram of the DC-link based DRI VSCF system.

3.4.1 DC-link voltage regulation based on exciter SG field current control using two-quadrant DC chopper

The BSG side DC-link voltage regulation of 540V is achieved through the exciter SG field current control using two-quadrant DC chopper. The control of BSG side DC-link voltage regulation is adapted from chapter 2 section 2.3 and [27], [41]. Fig. 3.6 (a), (b), and (c) show the DC-link voltage regulation and the exciter field current control waveforms for step changes in DC loads. It can be seen from Fig. 3.6 (a) that the DC-link voltage is regulated at 540V during steady-state operation. In addition, the transient response shows that the DC chopper controller is able to successfully recover the DC-link voltage back to 540V during transient switching load conditions.

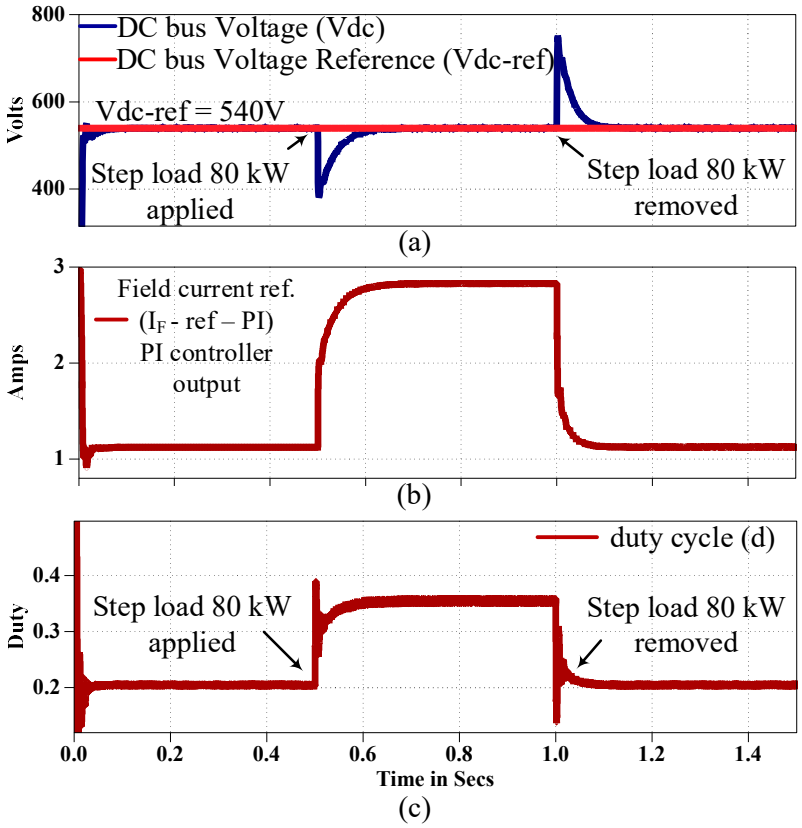


Fig. 3.6: Transient response of the DC chopper control during step change in DC load (80kW): (a) DC-link voltage; (b) Exciter field current; (c) Duty cycle.

3.4.2 Voltage mode control for four-leg inverter:

A four-leg inverter topology, shown in Fig. 3.7, is considered in this VSCF system to generate CVCF 115V, 400Hz AC supply to aircraft loads. This scheme is also a better replacement for the inverter with output transformer. An output filter is used to filter the switching harmonics from the inverter output to obtain a sinusoidal AC output voltage at the POR. The inverter output voltage from POR is supplied to the aircraft loads through long feeder cables. The inverter output voltage regulation is obtained by controlling the output filter capacitor current [42]. The control is implemented in synchronous reference frame (SynRF) and it has cascaded inner current loop and outer voltage loop controllers in DQ0 axes.

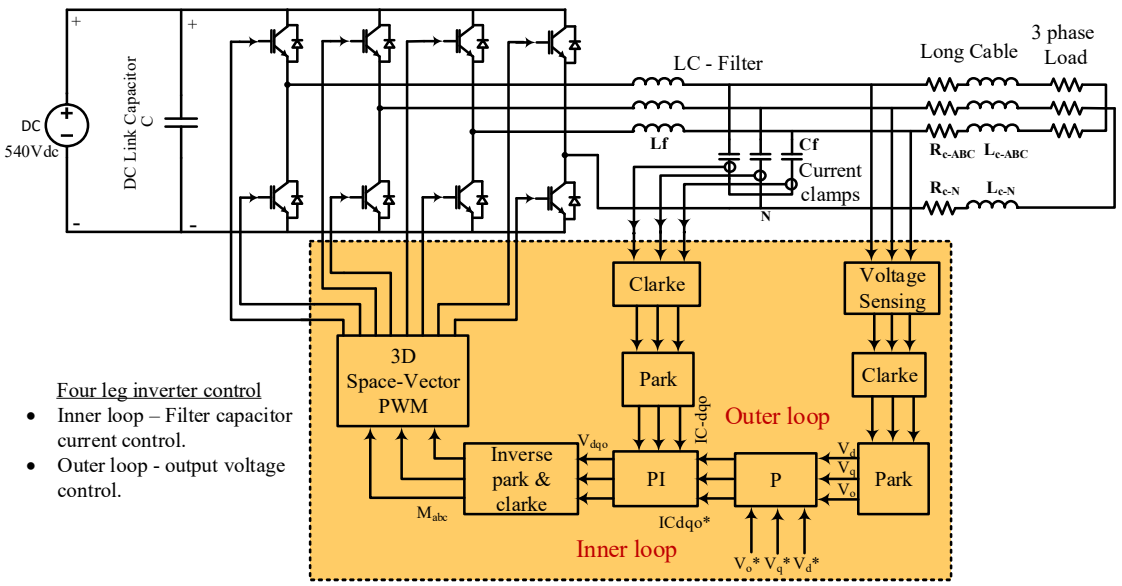


Fig. 3.7: Block diagram of the four-leg inverter and its voltage mode control.

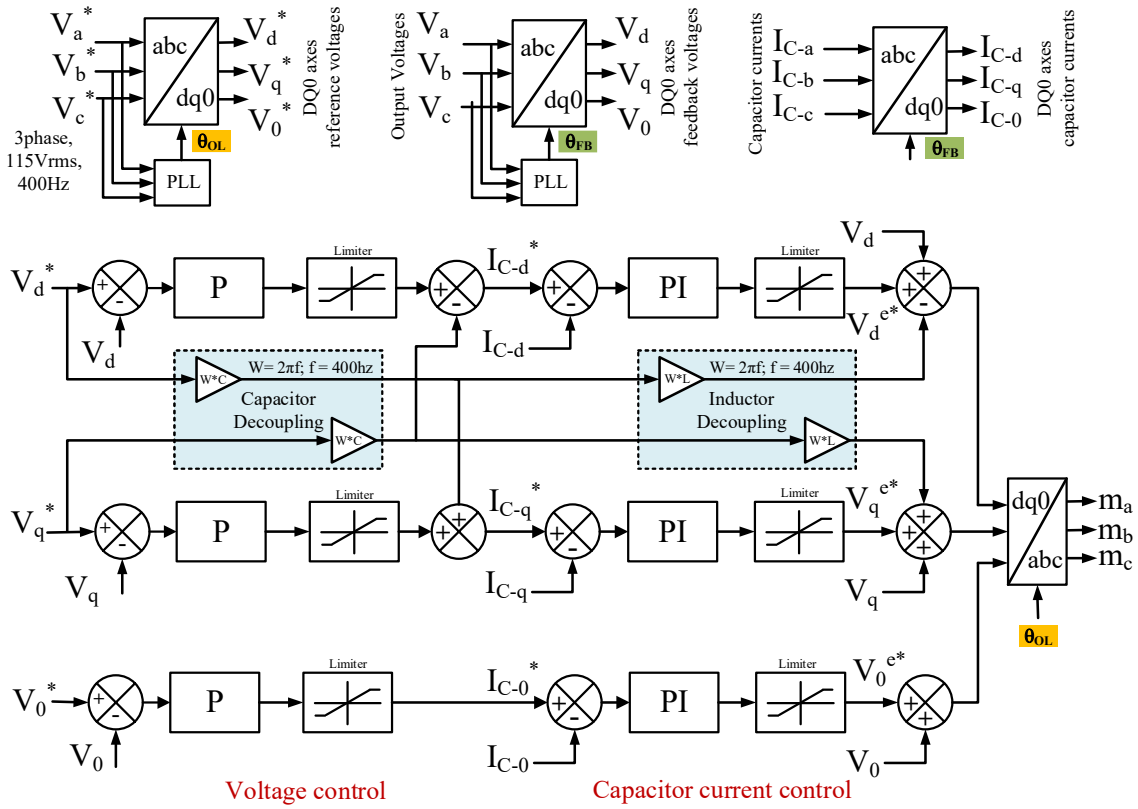


Fig. 3.8: Output voltage control and capacitor current control of four-leg inverter.

In this method, a dual phase angle control is adapted to improve the tracking accuracy of the DQ0 axis controllers [43]. The detailed block diagram of the dual phase

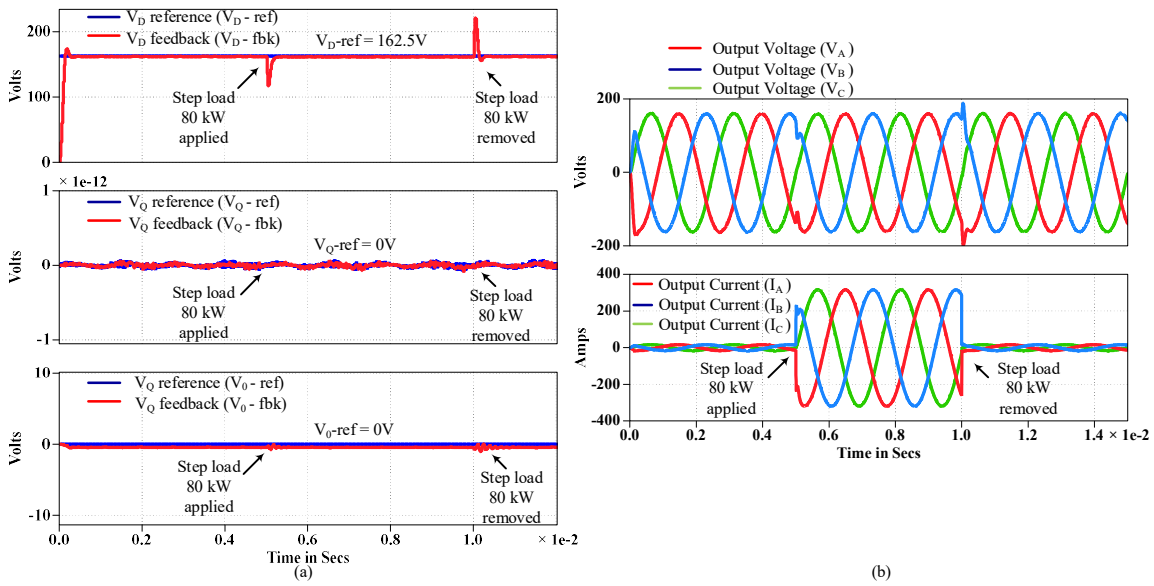


Fig. 3.9: Transient step load response of the four-leg inverter: (a) DQ0 axes voltages; (b) Inverter output voltages and currents.

angle control of the four-leg inverter is shown in Fig. 3.8. The outer loop capacitor voltage control is implemented using proportional (P) controllers and the inner loop filter capacitor current control is implemented using PI controllers. The neutral wire inductance in the output filter is not included to avoid the zero sequence cross coupling effects in the D and Q axes. Hence, the inductor current decoupling for the 0 axis need not be considered. In addition, the output voltage is added as feedforward to the capacitor current control output to improve the transient response of the inverter.

The simulation results of the standalone four-leg inverter are shown in Fig. 3.9 (a) and (b). The DQ0 axes controllers are able to successfully track the DQ0 axes reference voltages during transient step load operation. It can be seen from Fig. 3.9 (b) that the inverter output voltage is a sinusoidal 400Hz, 115V AC voltage. Moreover, the four-leg inverter output voltage meets the MIL-STD-704F transient AC voltage limits.

3.4.3 Complete VSCF system simulation

The combined VSCF system is verified for transient step load operations with different DC-link capacitance values to determine the minimum DC-link capacitance required to meet the MIL-STD-704F transient voltage specifications. Fig. 3.10 (a) and (b) show the simulation results for the DC-link based VSCF system with DC-link capacitance value of 50μF based on (1). It can be seen from Fig. 3.10 (a) that the DC-link voltage has a significant drop in DC voltage during transient step load of 80kW applied at time 0.2sec. It may also be noted from Fig. 3.10 (a) that the rate of change of DC-link voltage is relatively high and the DC-link voltage dropped well below the minimum DC-link voltage required to meet the transient AC output voltage limits. As per MIL-STD-704F as shown in Fig. 3.4, the minimum DC-link voltage required to provide 115V AC output voltage at the POR is ~285V based on equation (3.3). However, during transient step load conditions, the minimum DC-link voltage required to meet the output AC transient voltage limits vary from ~196V to ~282V calculated based on Fig. 3.4.

Though only ~196V is required from the DC-link at the instant when step load is applied, it can be seen from Fig. 3.10 (a) that the DC-link voltage has fallen to 110V. Since the DC-link voltage is lower than the minimum DC-link voltage required to meet the transient AC voltage limits, the inverter does not meet the MIL-STD-704F. This is mainly because the inverter side dynamics are faster than the generator side dynamics, which affects the DC-link voltage regulation during transient operating conditions. Fig. 3.10 (b) shows the transient response of the DC-link voltage regulation of the VSCF system for 80kW step load with 2000μF DC-link capacitance. It can be seen from Fig. 3.10 (b) that the minimum DC-link capacitance required to meet the transient voltage limits at the

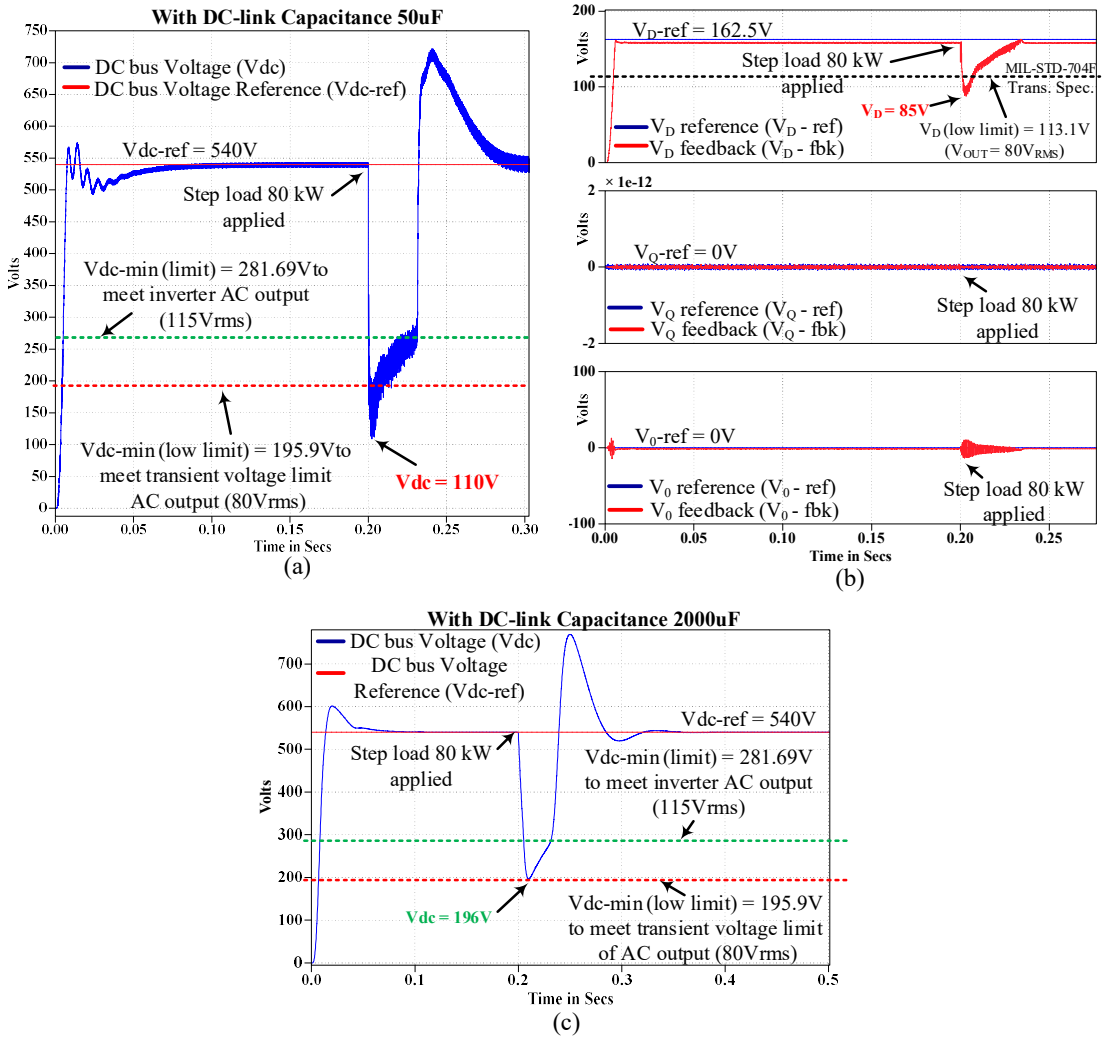


Fig. 3.10: Transient step load response of the VSCF system: (a) DC-link voltage regulation for 50µF DC-link capacitance; (b) Inverter - DQ0 axes voltages for 50µF DC-link capacitance; (c) DC-link voltage regulation for 2000µF DC-link capacitance.

inverter output is 2000µF. The minimum DC-link capacitance value chosen based on theoretical calculation from (3.1) is not able to meet the transient voltage limit requirements at the inverter output. Hence, the selection criteria for minimum DC-link capacitance for the VSCF system mainly depends on the transient performance of the generator side control which has relatively slower dynamics when compared to inverter side control. In this paper, feedforward control improvements are proposed for the generator side DC-link voltage regulation control and output power based adaptive inverter voltage reference for four-leg

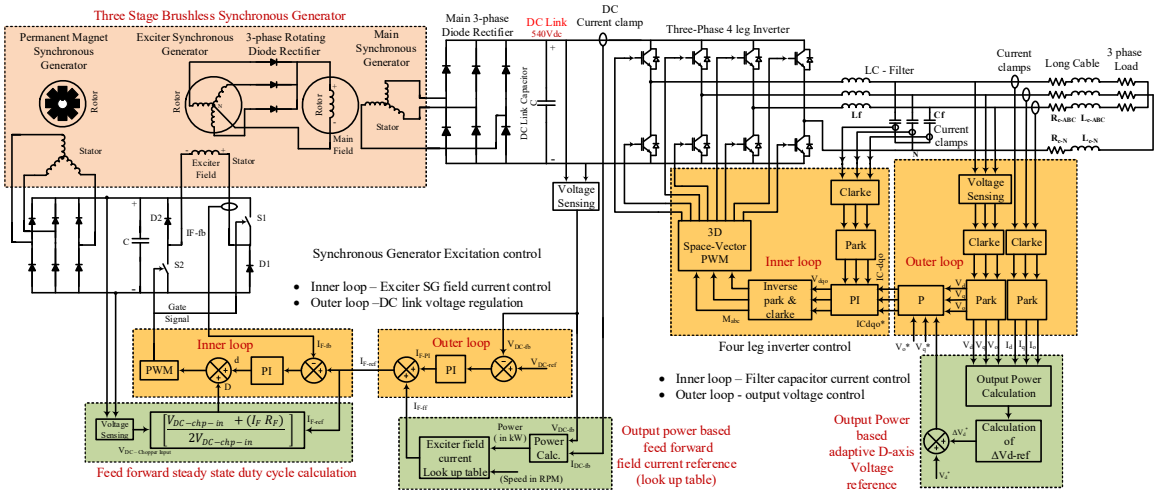


Fig. 3.11: Block diagram of the proposed controller for the DC-link based VSCF system.

inverter control to improve the transient response at the DC-link for step loads at the inverter output. The proposed control methods are explained in detail in Section 3.5.

3.5 Proposed control improvements for minimizing DC-link capacitance in VSCF system

In order to minimize the DC-link capacitance of the VSCF system and at the same time to meet the stability and MIL standard requirements, two independent decentralized control improvements are proposed in this section for both generator side and inverter side controls of the VSCF system.

3.5.1 Feedforward compensation techniques for BGS side DC-link voltage regulation control

In order to improve the transient response of the DC-link voltage regulation, a lookup table based feedforward compensation for generator side voltage control is adapted from Chapter 2 section 2.3 and [41], as shown in Fig. 3.11. In this method, the feedforward

Table 3.2: Feedforward exciter field current reference.

		Load in kW								
		0	10	20	30	40	50	60	70	80
Speed in RPM	7000	1.5	2.3	3	3.7	4.3	4.9	5.6	6.3	7
	8000	1.3	1.9	2.5	3.1	3.6	4.1	4.8	5.5	6.2
	9000	1.1	1.6	2	2.5	3	3.5	4.2	4.9	5.5
	10000	0.9	1.3	1.7	2	2.4	2.8	3.5	4.2	4.9
	11000	0.8	1.2	1.5	1.9	2.2	2.5	3.2	3.9	4.5
	12000	0.7	1	1.3	1.6	1.9	2.2	3	3.7	4.2
	13000	0.6	0.9	1.2	1.5	1.7	1.9	2.6	3.2	3.8
	14000	0.5	0.8	1.1	1.3	1.5	1.6	2.3	2.9	3.5

field current reference from the lookup table is added to the output of the outer voltage loop to generate the required field current reference to the inner current loop.

Table 3.2 shows the feedforward exciter field current reference lookup table obtained from the field test for different DC load power at different speeds of the main SG. In addition, the steady-state duty cycle for the two-quadrant DC chopper is also added as a feedforward compensation to the output of the inner current loop PI controller. These feedforward improvements help in faster recovery of the DC-link voltage for larger step loads. Hence, the rate of change of DC-link voltage during a step load change can be significantly reduced since the feedforward compensations provide instantaneous change required for step increase in the DC power.

The simulation results with feedforward compensation is enabled on the generator side DC-link voltage regulation of the VSCF system control are shown in Fig. 3.12 (a) and (b). The DC-link capacitance value used in the simulation is 400μF. When the feedforward compensation is enabled on the generator side outer loop voltage controller, significant improvement can be observed in the transient response at the DC-link voltage. It can be seen from Fig. 3.12 (a) that when 80kW step load is applied, the DC-link voltage reaches

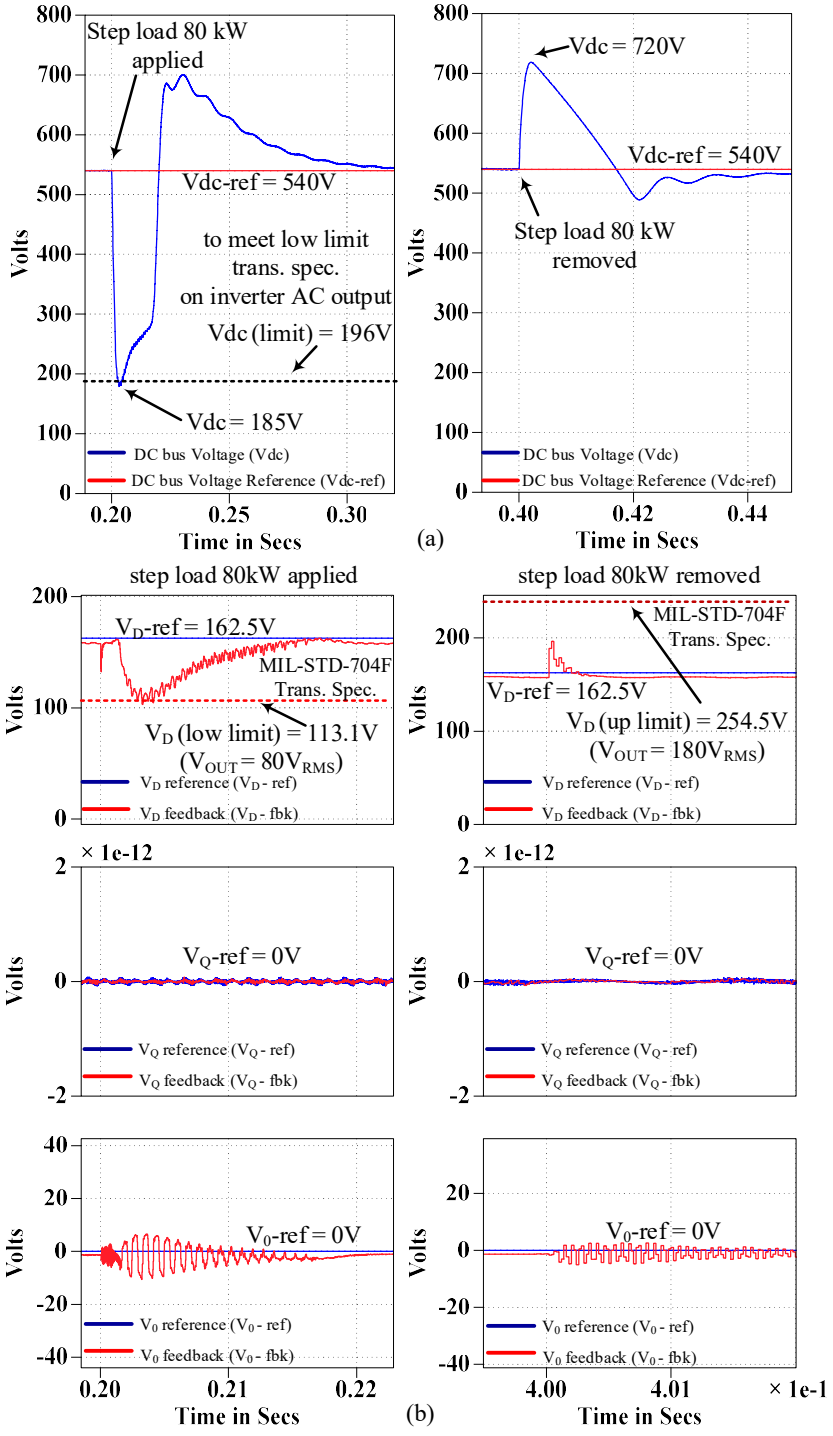


Fig. 3.12: 80kW step load response of the VSCF system with BSG side improvements with 400µF DC-link capacitance: (a) DC-link voltage; (b) Inverter DQO axes voltages.

185V momentarily. However, the DC voltage quickly recovers above 196V which is the minimum DC-link voltage required during transient condition. Since the DC-link voltage regulation is able to maintain the voltage above the minimum required DC-link voltage, the VSCF system is able to meet the MIL-STD-704F AC voltage transient limits and recovery time as shown in Fig. 3.12 (b). As per Fig. 3.10(c), for a 80kVA VSCF system, a DC-link capacitance value of 400 uF (five times lower than actual value of 2000uF) is only required, however, it is relatively much higher (approx. 8 times) compared to DC-link capacitance to satisfy stability requirements. Moreover, the rate of change of DC-link voltage during transient step load operation is still very high and it may trigger the over voltage and under voltage protection of the PEC. Thus, the 400μF DC-link capacitance for an 80kVA VSCF system is still not an attractive size reduction and hence the objective is to further reduce the DC-link capacitance by using the proposed control improvement on the four-leg inverter control.

3.5.2 Proposed AIVR algorithm for four-leg inverter control

In this proposed Adaptive Inverter Voltage Reference (AIVR) algorithm, the output voltage reference to the inverter control is adaptively adjusted based on rate of change of instantaneous inverter output power and the required transient AC output voltage limits based on MIL-STD-704F. During transient step load conditions, the rate of change of inverter output power is measured to determine the amount of voltage change (ΔV) needed at the inverter output voltage as

$$V_{out-ref-total} = V_{out-ref} + \Delta V. \quad (3.4)$$

The change in inverter output voltage reference helps to reduce or increase the inverter output voltage during transient step load conditions to limit the rate of change of power at the DC-link. As a result, it limits the magnitude of the rate of change of DC-link voltage during transient conditions and thereby reduces the amount of capacitance required at the DC-link. The amount of voltage change (ΔV) calculated by the AIVR is based on the transient output voltage specification of the inverter. For DC-link based VSCF system used in aerospace applications, the transient AC output voltage limits are based on MIL-STD-704F as shown in Fig. 3.4. For four-leg inverter with DQ0 axes control as shown in Fig. 3.11, the inverter output voltage reference is calculated in d-axis reference as

$$V_{d-ref-tota} = V_{d-ref} + \Delta V_{d-ref}, \tag{3.5}$$

where $V_{d\text{-}ref}$ is calculated based on the rated output voltage of the inverter ($V_{d\text{-}ref} = \sqrt{2} * V_{out\text{-}ph\text{-}rm)}$ and $\Delta V_{d\text{-}ref}$ is calculated based on transient AC output voltage limits from MIL-STD704F and the rate of change of inverter output power, given as

$$\Delta V_{d-ref} = \begin{cases} -\left[\frac{\Delta P_o + P_{min}}{P_{max}}\right] * \left(V_{out-r} - V_{out-min}\right) * \sqrt{2} & : \quad for\ P_{max} > \Delta P_o > P_{min} \\ 0 & : \quad for\ P_{min} > \Delta P_o > -P_{min}, \\ +\left[\frac{\Delta P_o - P_{min}}{P_{max}}\right] * \left(V_{out-max} - V_{out-r}\right) * \sqrt{2} & : \quad for\ -P_{max} < \Delta P_o < -P_{min} \end{cases} \tag{3.6}$$

where $V_{out-max}$ and V_{out-m} are the rms value of the maximum and minimum limits of the inverter output voltage during transient operation which are extracted from MIL-STD-704F. P_{max} is the maximum output power rating of the inverter. ΔP_{min} is the minimum rate of change of output power required to enable the $\Delta V_{d\text{-}ref}$ calculation. A typical value of ΔP_{min} is 10% of the P_{max}.

Fig. 3.13 (a) shows the flowchart of the AIVR algorithm. It can be seen from the flowchart that once the $\Delta V_{d\text{-}ref}$ is calculated and added to the $V_{d\text{-}ref}$, the current value of $\Delta V_{d\text{-}ref}$ is reduced or increased to zero with the ramp rate that matches with the recovery time of AC voltage transient limits from MIL-STD704F (80mS).

Table 3.3: Calculation of ΔVd-ref for 80KVA VSCF system at different step loads.

ΔP_o	$V_{d\text{-}ref}$	$\Delta V_{d\text{-}ref}$	$V_{d\text{-}ref\text{-}total}$	**Constant values**
< 5kW	162.6V	0V	162.6V	$P_{min} = 5kW$ $P_{max} = 80kW$ $V_{out\text{-}max} = 180V_{rms}$ $V_{out\text{-}min} = 80V_{rms}$ $V_{out\text{-}ref} = 115V_{rms}$
-35kW	162.6V	45.96V	208.5V	
35kW	162.6V	-24.24V	137.8V	
75kW	162.6V	-49.49V	113.1V	
-75kW	162.6V	91.92V	254.5V	

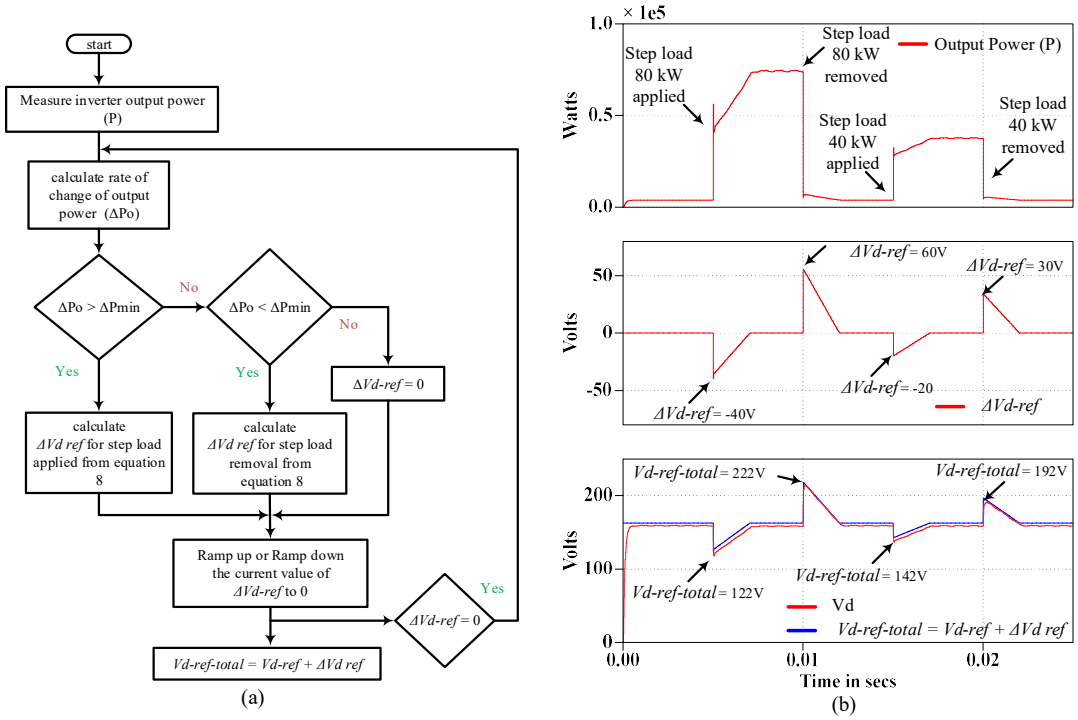


Fig. 3.13: AIVR algorithm for four-leg inverter control: (a) Flowchart of the AIVR algorithm; (b) Four-leg inverter control DQ0 axes voltages during 80kW & 40kW step load.

For the 80kVA VSCF system under study, the calculation of $\Delta V_{d\text{-}ref}$, and $V_{d\text{-}ref\text{-}total}$ for different ΔP_o during transient step load conditions are listed in Table 3.3. Fig. 3.13 (b)

shows the d-axis controller response of the four-leg inverter side control of the VSCF system with the proposed AIVR algorithm. It can be seen that the $\Delta V_{d\text{-}ref}$ for different step loads are calculated and reduced or increased back to zero with the recovery time of ~80ms which is extracted from transient voltage limits. It also shows that the inverter d-axis voltage meets the MIL-STD-704F transient specification.

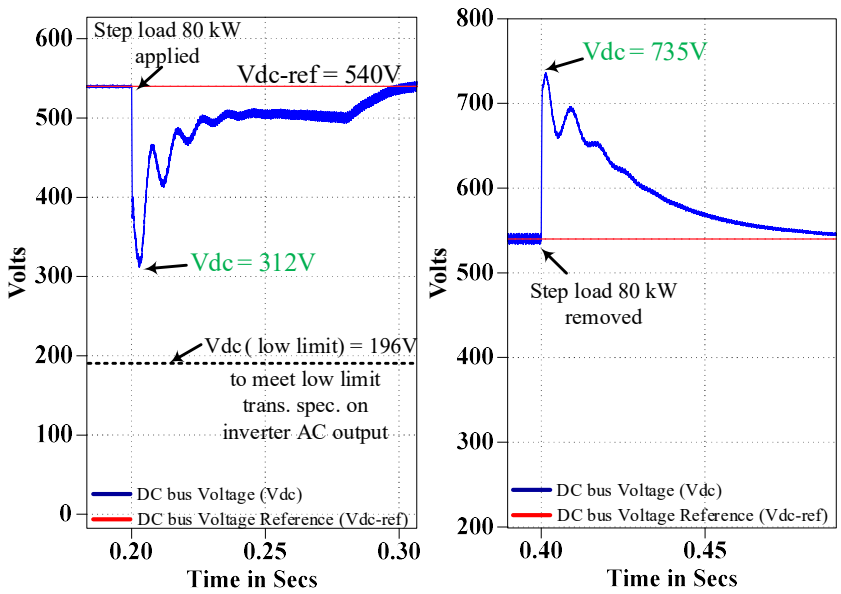


Fig. 3.14: (a) DC-link voltage of the VSCF system during step load 80kW with proposed control improvements on both four-leg inverter and BSG side with 100µF DC-link capacitance.

3.6 Simulation and verification of the VSCF system with proposed control improvements

The simulation results in Fig. 3.14 (a) and (b) show that the 80kVA VSCF system is able to meet the MIL-STD-704F output transient specifications with a minimum DC-link capacitance value of 100µF, using the proposed improvements in generator side and four-leg converter controls. It can be noted from Fig. 3.14 (a) that the rate of change of DC-link voltage has reduced significantly for 80kW step load. Moreover, the minimum

DC-link voltage value during transient step load is well above the minimum DC-link voltage required to meet the transient specifications.

Similarly, the minimum d-axis voltage during transient step load is also above the minimum d-axis voltage limit to meet the transient requirements, as shown in Fig 3.14 (b). Hence, the proposed control improvements help to reduce the DC-link capacitance value

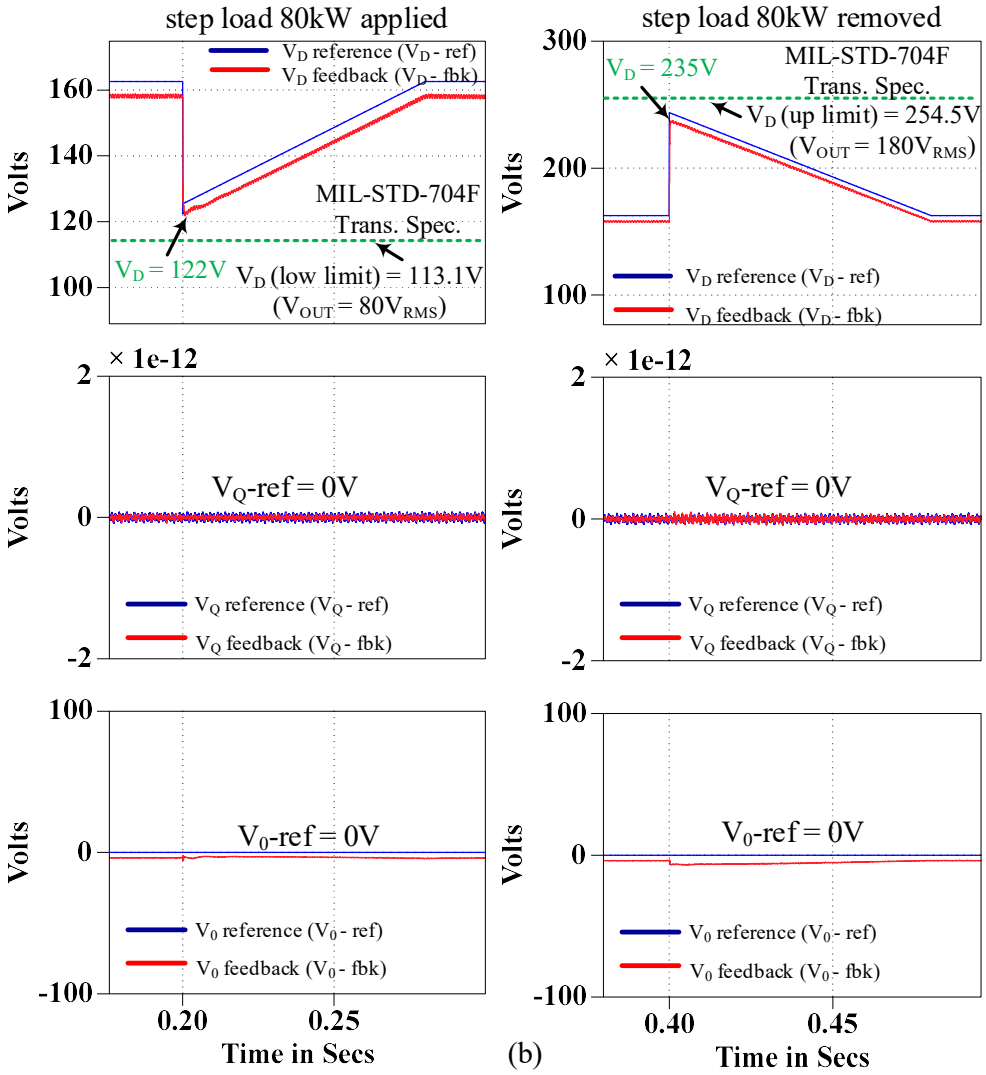


Fig. 3.14: (b) Four-leg inverter DQO axes voltages of the VSCF system during step load 80kW with proposed control improvements on both four-leg inverter and BSG side with 100µF DC-link capacitance.

in the VSCF system from 2000µF to 100µF at rated speed and power condition and still be able to meet the MIL-STD-704F transient specification.

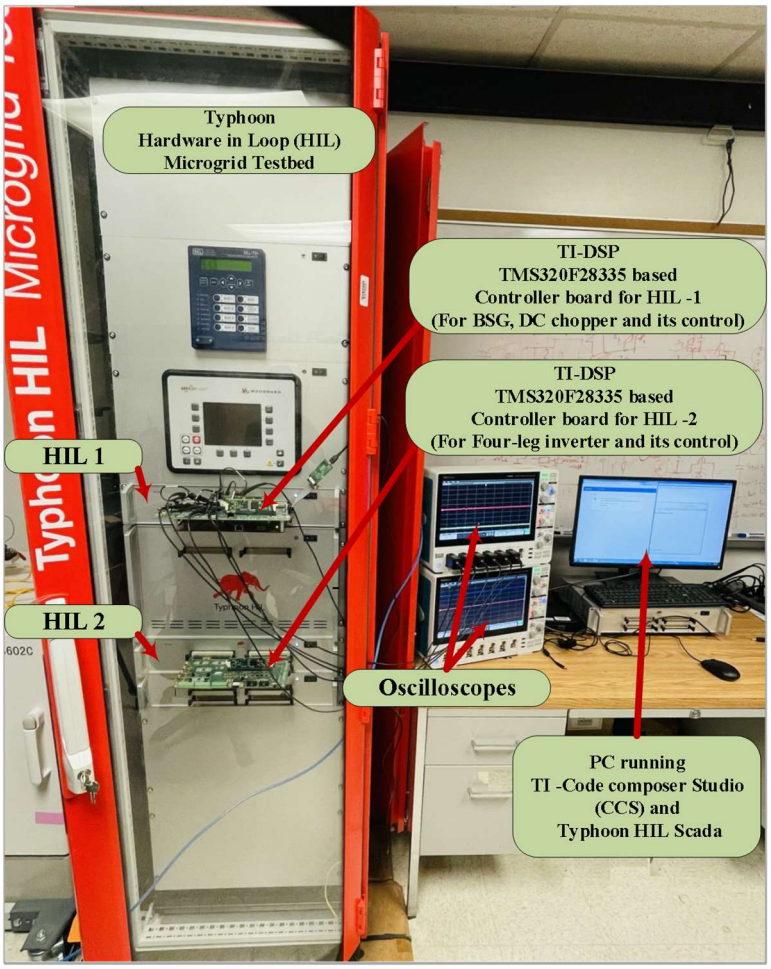


Fig. 3.15: C-HIL test set up.

3.7 Controller hardware-in-loop (C-HIL) real-time testing of an 80kVA VSCF system

Fig. 3.15 shows the experimental test set up of the real-time C-HIL testing of the 80kVA VF BSG based DRI-VSCF system. The C-HIL test setup consists of Typhoon-HIL Microgrid testbed and Texas Instruments (TI) TMS320F28335 Digital Signal Processor (DSP) based control boards. In Typhoon HIL Microgrid testbed, two HIL-604 emulators

such as HIL1 and HIL2 are used and they are paralleled using high-speed serial communication. The BSG side circuits of the VSCF system such as BSG (PMG, Exciter SG, and Main SG), two-quadrant DC chopper, main 3phase diode rectifier, and DC-link capacitance are modeled in HIL1. The AC output side circuits such as four-leg inverter, sinewave LC filer, long cable, and the loads are modeled in HIL2.

The specification of the 80kVA VSCF system studied in this paper is based on BSG parameters from Table 2.1 in chapter 2 and four-leg inverter specification from Table 3.4. The electrical machines such as exciter SG and main SG are chosen as non-linear machines and used with DQ-axis currents vs magnetizing inductance values obtained from an 80kVA

Table 3.4: Specifications of the PECs.

Description	Values
DC-link capacitance	2000µF for without control improvements
DC-link Voltage	540V
AC Output Voltage (Phase RMS)	115V
Output frequency	400Hz
Switching carrier frequency	40kHz
Output Power	80kVA (0.8 to 1.0 pf)
Output filter type (star connected C)	LC (cut-off 4kHz)
Load side cable - phase resistance (R_c)	10 mΩ
Load side cable - phase inductance (L_c)	3.5 µH
Load side cable - neutral wire resistance (R_cN)	7.8 mΩ
Load side cable - neutral wire inductance (L_cN)	2.5 µH
Load (Balanced & Unbalanced)	Max: 80kW
Output connection type	3phase, 4 wire

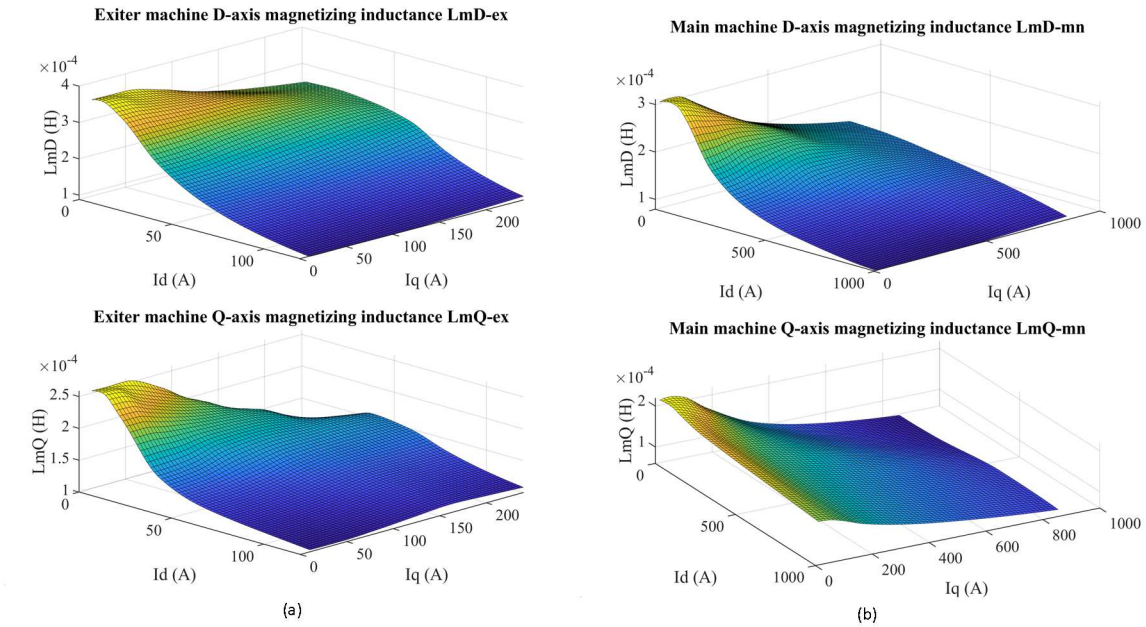


Fig. 3.16: DQ-axis currents vs magnetizing inductance: (a) Exciter SG; (b) Main SG.

BSG used in aircraft VSCF backup power generation as shown in Fig. 3.16 (a) and (b). Each HIL-604 is connected to its dedicated DSP control board (DSP1 & DSP2).

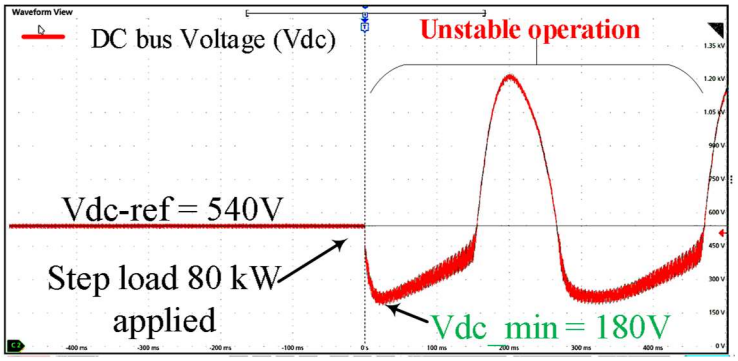
The control of DC-link voltage regulation, the exciter SG field current control based on two-quadrant DC chopper, and the proposed feedforward DC chopper control improvements are implemented in DSP1. The control of the four-leg inverter and the proposed AIVR control improvement are implemented in DSP2.Each DSP is independently controlled without any intercommunication to maintain decentralized control strategy for the VSCF system. In both DSPs, the control algorithms are implemented with a maximum frequency of 25 kHz is used for feedback signal sampling, current control processing, PWM generation, and switching carrier frequency. The voltage controls, feedforward compensation, and AIVR algorithm are implemented with a maximum processing frequency of 5 kHz. The total DSP bandwidth utilization is less than 75% for both DSPs.

Fig. 3.17 (a) and (b) show the C-HIL test results of the 80kVA VSCF system during 80kW step load with 50µF DC-link capacitance with the conventional control method. Without any control improvements for the VSCF system, it can be seen from Fig. 3.17 (a) that the DC-link voltage becomes unstable due to the effects of four-leg inverter side faster dynamics. Hence the DC-link voltage is not able to reach the steady-state when 80kW step load is applied. As a result, the inverter output voltage becomes unstable and not able to meet the MIL standard voltage specifications.

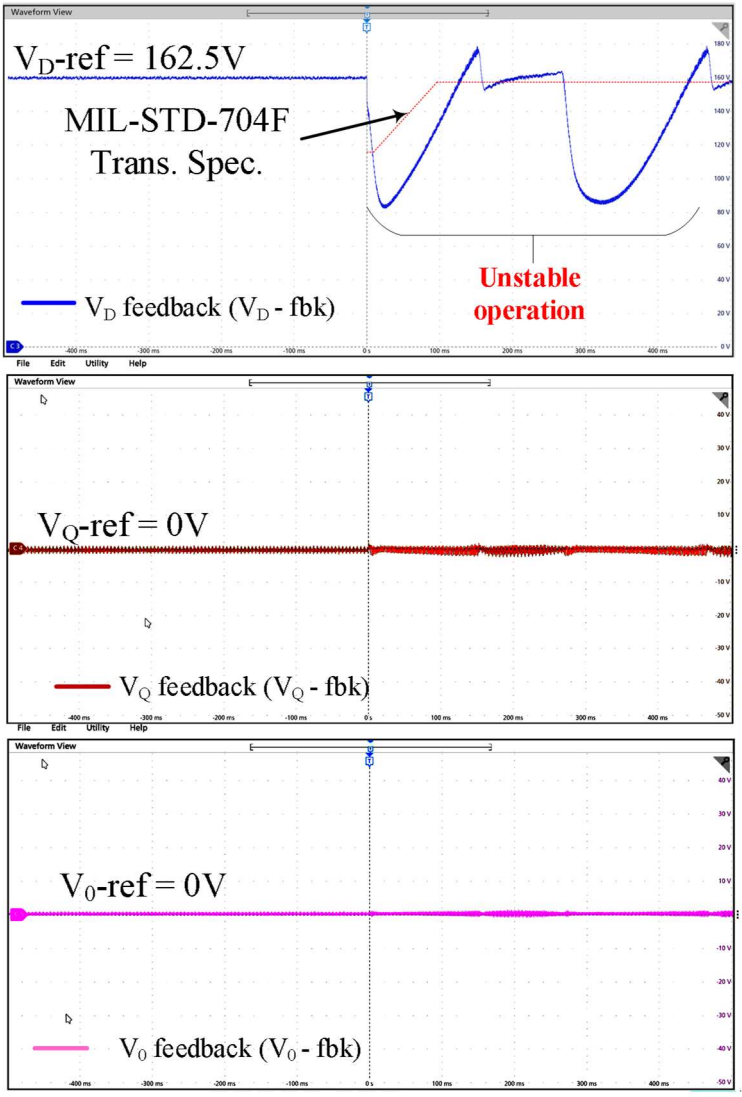
Fig. 3.18 (a) and (b) show that the VSCF system is able to meet the MIL-STD-704F inverter output voltage magnitude limits using a higher DC-link capacitance value of 2000 µF. For 2000uF DC-link capacitance, the DC-link voltage still has a very high rate of change of voltage during the 80kW step load. Furthermore, the settling time of the inverter D-axis output voltage takes around 400µS due to the high value of DC-link capacitance and slow dynamics of the three-stage BSG and its control.

Table 3.5: DC-link capacitance value for an 80kVA VSCF system with and without control improvements.

VSCF control methods	DC-link capacitance required to meet MIL-STD-704F	Reduction from conventional control method
Conventional control method without any improvements	**2000µF**	**N/A**
Proposed BSG side feedforward control improvements	**400µF**	**80%**
Proposed BSG side feedforward control and four-leg inverter AIVR	**100µF**	**95%**

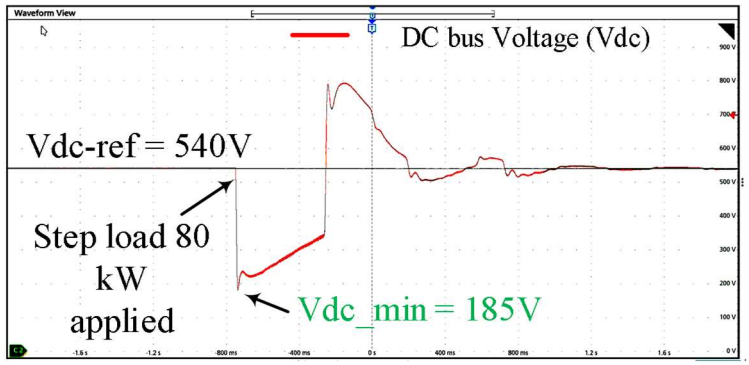


(a)

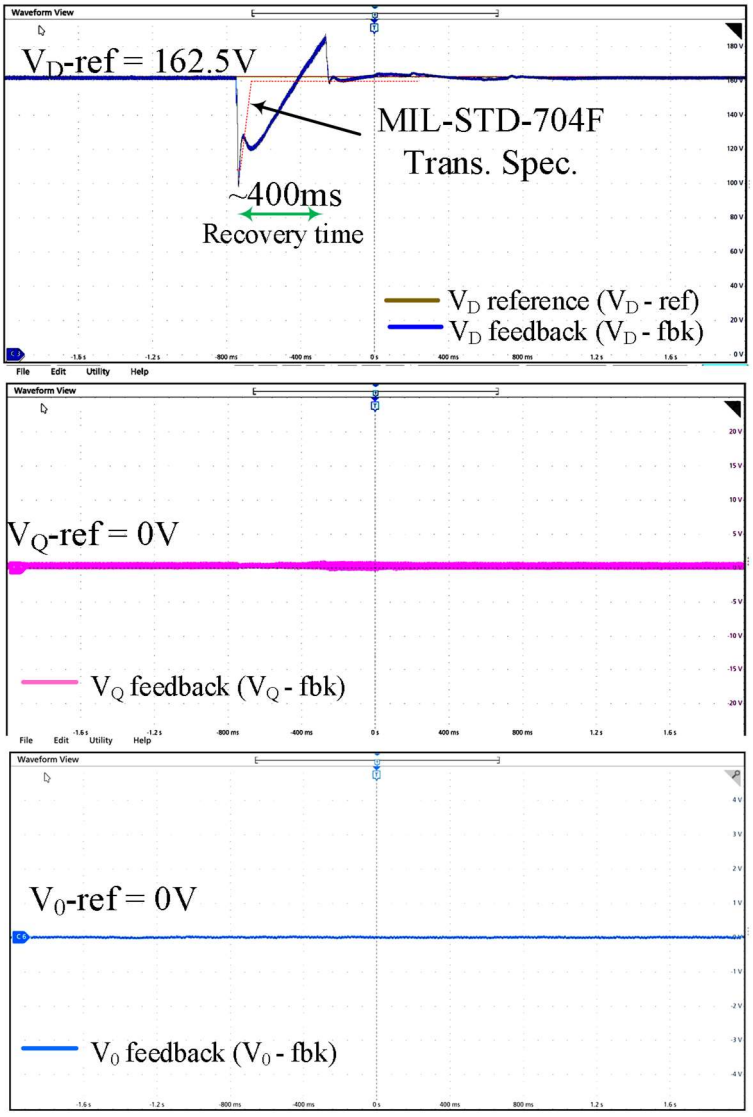


(b)

Fig. 3.17: Transient response of the VSCF system with 50µF DC-link capacitance for step load 80kW without control improvements: (a) DC-link voltage; (b) Four-leg inverter DQO axes voltages.



(a)

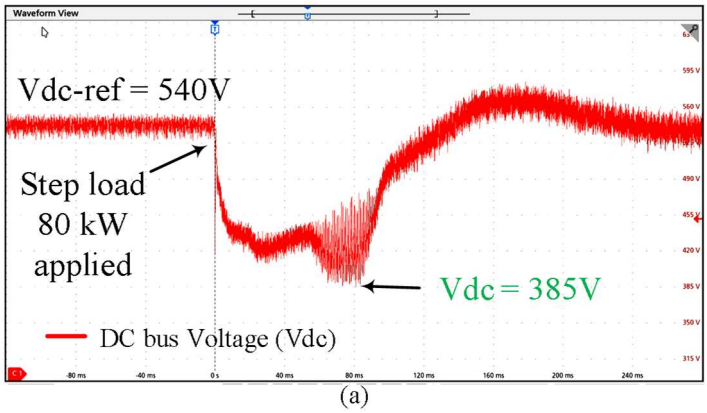


(b)

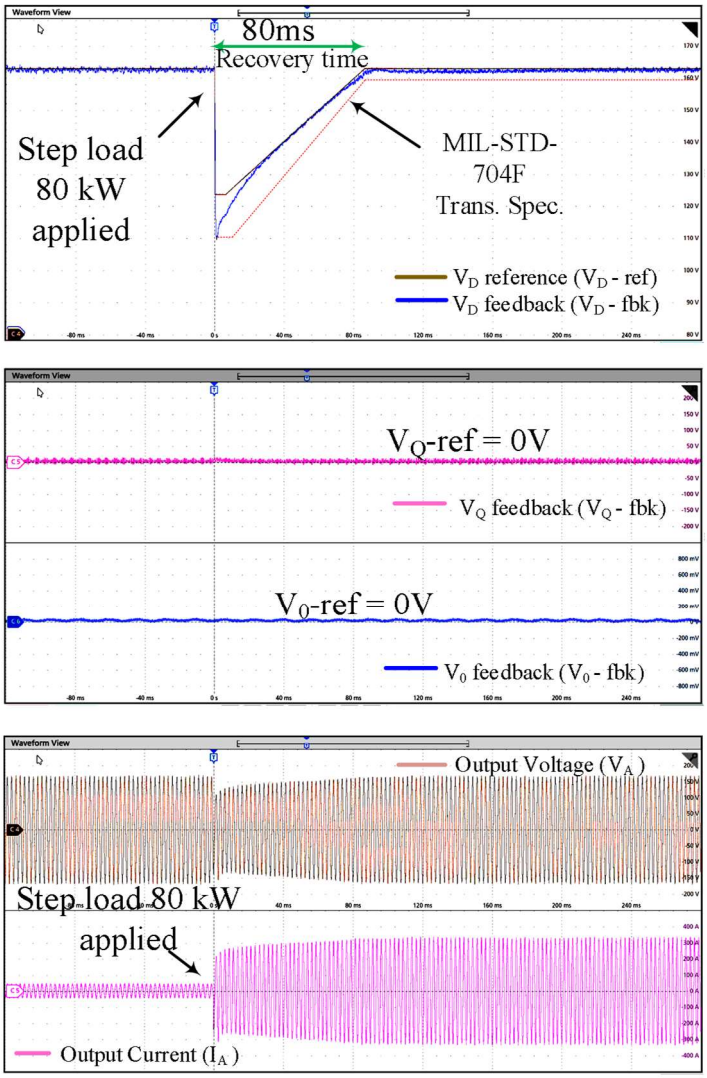
Fig. 3.18: Transient response of the VSCF system with 2000µF DC-link capacitance for 80kW step load without control improvements: (a) DC-link voltage; (b) Four-leg inverter DQO axes voltages.

Fig. 3.19 and 3.20 show the C-HIL test results of the 80kVA VSCF system during 80kW with only 100μF DC-link capacitance and with proposed control improvements such as BSG side feedforward control improvements and the AIVR algorithm for the four-leg inverter control, respectively. It can be seen form Fig. 3.19 (a) and 3.20 (a) that the DC-link voltage is very stable during both 80kW step load applied and removed.

Moreover, the rate of change of DC-link voltage during step load has reduced significantly. Hence, it verifies that the four-leg inverter output voltage is able to meet MIL-STD-704F transient voltage specification as shown in Fig 3.19 (b) and 3.20 (b). It also verifies that the proposed control improvements help to reduce the DC-link capacitance in the VSCF system by 95% when compared to the conventional control method as tabulated in Table 3.5.

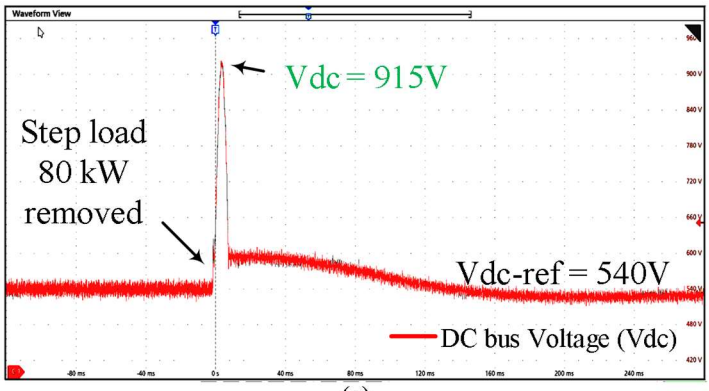


(a)

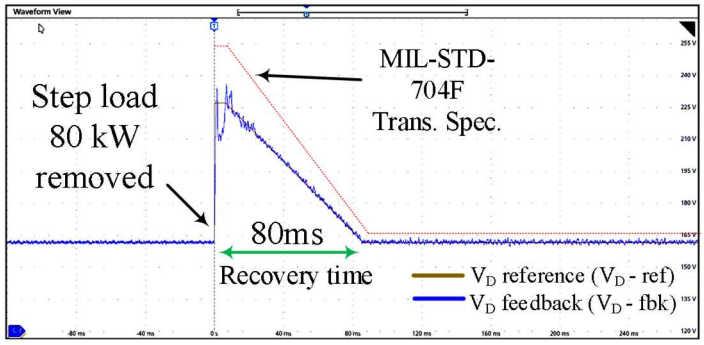


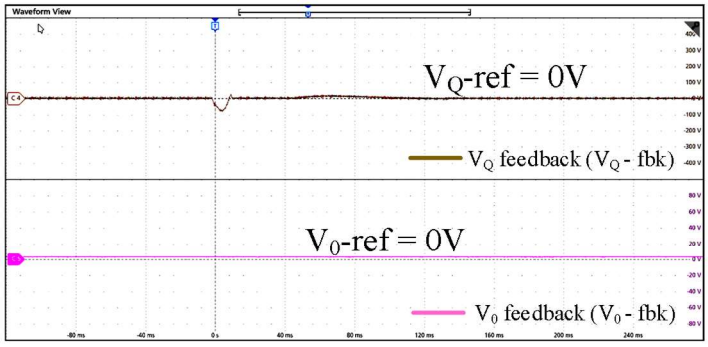
(b)

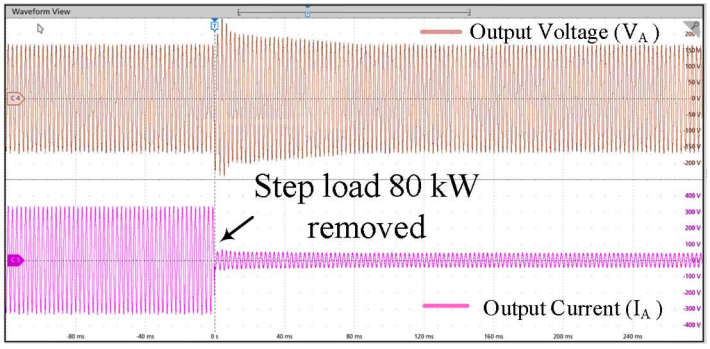
Fig. 3.19: Transient response of the VSCF system for 100μF DC-link capacitance with proposed improvements on both four-leg inverter and BSG side controls when 80kW step load is applied : (a) DC-link voltage; (b) Four-leg inverter DQO axes voltages, output voltage, and current.



(a)







(b)

Fig. 3.20: Transient response of the VSCF system for 100μF DC-link capacitance with proposed improvements on both four-leg inverter and BSG side controls when 80kW step load is removed : (a) DC-link voltage; (b) Four-leg inverter DQO axes voltages, output voltage, and current.

3.8 Summary

In this chapter, novel control strategies to minimize the DC-link capacitance in a BSG based diode rectifier-inverter VSCF system are proposed for MEA applications. An output power based feedforward field current reference for BSG is proposed to improve the transient response of the DC-link voltage regulation. In order to meet the transient switching load specifications at the inverter output as per MIL standards, the output voltage reference of the four-leg inverter control is adaptively modified based on the rate of change of inverter output power during step load conditions. In order to match the fast dynamic voltage control of inverter with the slow inertial dynamics of the BSG, the inverter output voltage reference is modified within the permissible limits specified in the MIL-STD-704F to limit the amount of energy required from or observed to the DC-link during step load conditions. As a result, the amount of DC-link capacitance required in the VSCF system is reduced. The proposed control strategies enable to significantly reduce (about 95%) the DC-link capacitance value of the VSCF system used in the aircraft. The output of the four-leg inverter in the VSCF system is able to meet the MIL-STD-704F transient voltage specifications for step load conditions at rated power.

3.9 Publications

1. G. Selvaraj, K. R. Ramachandran Potti, K. Rajashekara, "An Enhanced Controller for Four Leg Inverter-Fed Loads in an Aircraft Power System," *in Proc. IEEE APEC*, June 2021.

2. G. Selvaraj, K. Rajashekara, K. R. Ramachandran Potti, "Minimization of DC-link Capacitance for a DC-link Based Variable Speed Constant Frequency Aircraft Power System," *in Proc. IEEE ECCE*, Oct 2021.
3. G. Selvaraj, K. Rajashekara, K. R. Ramachandran Potti, "Minimization of DC-link Capacitance for a DC-link Based Variable Speed Constant Frequency Aircraft Power System," *IEEE Trans. on Ind. Appl.,* 2021 [under review].

CHAPTER 4

CONTROL STRATEGY FOR A BRUSHLESS SYNCHRONOUS GENERATOR BASED ACTIVE RECTIFIER REGULATED DC POWER SYSTEM WITH MINIMAL DC-LINK CAPACITANCE

In this chapter, control improvements to minimize the DC-link capacitance in a BSG based active rectifier regulated aircraft DC power system are proposed. The active rectifier regulates the DC-link voltage, achieves unity power factor (UPF), and low Total Harmonic Distortion (THD) current at the BSG output. The improved excitation control of BSG aids during transient load conditions to meet MIL-STD-704F transient specifications at the active rectifier output of +/-270V DC with reduced DC-link capacitance. The field optimization technique helps to maintain UPF operation at the BSG output during steady-state operation. The proposed strategy is modeled and verified for a 25kW DC power system using Controller Hardware-in-loop (C-HIL) testing and results show that the proposed strategy helps to achieve a fast transient response to meet MIL-STD-704F with minimal DC-link capacitance.

4.1 Introduction

In MEA such as Boeing 787, the EPS follows two primary power distribution methods: 1) Variable Frequency (VF) 360-800Hz 115/230V AC, and 2) +/-270V DC.

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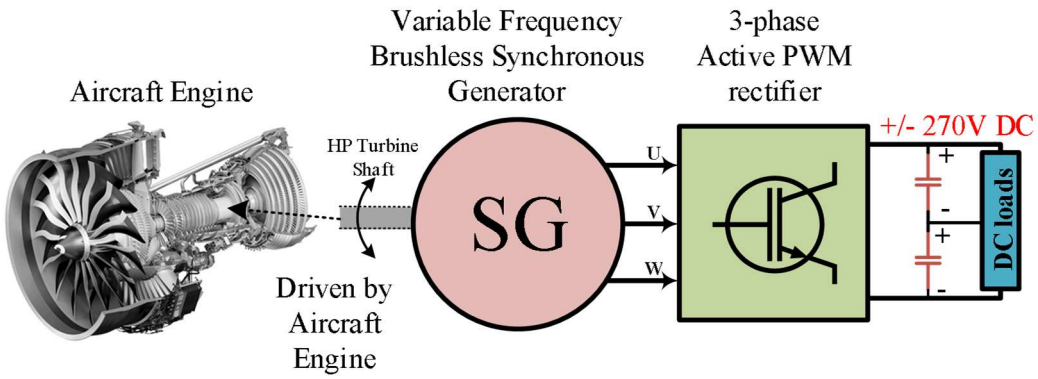


Fig. 4.1: Block diagram of a Brushless SG based Active rectifier regulated aircraft DC power system.

In recent years, the DC power distribution (+/-270V) is becoming more popular and increasingly considered due to its reduced losses and weight reduction as compared to traditional AC power distribution. The +/-270V DC is obtained by converting the VF AC from the generator into DC using Transformer Rectifier Unit (TRU) and Auto Transformer Rectifier Unit (ATRU) [2]–[4], [9], [20], [44]. The main disadvantages of TRU and ATRU are, high THD in current for low input frequency, inability to achieve unity power factor (UPF), and extra space/weight consumption by the transformers [45], [46]. To overcome the power quality challenges such as high THD in current and UPF operation, an active power filter (APF) is considered along with TRU or ATRU to meet 5% THD in current and to achieve UPF operation [47], [48]. However, the APF comes as an additional unit and increases the weight and space consumption in the aircraft.

The recent advancements in power electronics and the increased reliability of power switches make the active rectifier a more reliable and an excellent option to handle power quality issues. Moreover, the active rectifier replaces the TRU or ATRU and connects directly to the VF BSG to regulate the DC-link voltage during generator mode and acts as an inverter during starter mode [2]. Though the active rectifier helps to solve the power

quality issues, the weight and space consumption of the active rectifier is higher when compared to the diode bridge rectifier (DBR) unit, due to the usage of switching transistors, gate drivers, controller, capacitors,etc. In addition, the DC loads are connected to the +/-270V DC bus using bulky DC-link capacitor banks. These DC-link capacitors along with the active rectifier increases the total volume of the PEC. Hence, in this chapter, control improvements for reducing the DC-link capacitance and to improve power quality in a VF BSG based active rectifier regulated DC power system as shown in Fig. 4.1 are investigated.

For an active rectifier based DC power system, several control methods are presented in the literature to minimize the DC-link capacitance [24]–[26]. In [24], a DC-link capacitor current control is proposed to reduce the capacitor current during load change to reduce the DC-link capacitance requirement. In [25], an output power based feedforward controller for the DC-link voltage control loop is proposed. A feedback linearizing control for PWM rectifier- inverter motor drive system is proposed in [26]. These methods are generally effective for Utility applications where the grid is sufficiently a stiff source and supports faster dynamics at the output. However, these methods are not effective for aircraft applications, where the source is a generator and the dynamics are dependent on the transient response of the generator control. In [41], an output power based feedforward exciter current controller for a BSG based DC system using DBR is proposed to minimize the DC-link capacitance to 600μF for a 50kW DC power system for BSG speed of 14000rpm.

In this chapter, a lookup table based feedforward controller for VF BSG side exciter control along with the field oriented control (FOC) based DC-link voltage regulation is

proposed for the BSG based active rectifier regulated DC power system. In addition, a field optimization technique is proposed to maintain UPF during steady-state operation. In the proposed method, the feed-forward control improvements help the active rectifier side control during step load conditions to achieve faster transient response at the DC-link to meet the MIL-STD-704F transient voltage limits with a minimal DC-link capacitance value [23]. The proposed control is modeled and implemented for a 25kW DC power system and validated through real-time Controller Hardware-in-loop (C-HIL) testing using Typhoon HIL system. The results show that the control improvements help to achieve fast transient response at the DC-link for step load changes, to meet MIL-STD-704F transient voltage specification with only 200μF DC-link capacitance.

4.2 Control of VF BSG based active rectifier regulated DC power system

Fig. 4.2 shows the control block diagram of the BSG based active rectifier regulated aircraft DC power system. The BSG exciter field current control is employed through a two-quadrant DC chopper [41]. The exciter field current reference is given based on the speed of the BSG. In the active rectifier side control, the DC-link voltage regulation is achieved by using dual-loop cascaded direct (D) and quadrature (Q) axis field oriented control (FOC) of the BSG in the synchronously rotating reference frame (Syn-RF) [49]–[52]. In the inner current loops, the D-axis and Q-axis current controllers regulate the flux and torque of the BSG respectively. In the outer voltage loop, the DC-link voltage control provides Q-axis current reference (a proportional torque reference) to the inner loop Q-axis current control. The speed of the BSG is sensed using a speed encoder to find the angle for the Syn-RF transformations. The control methods for BSG and active rectifier are

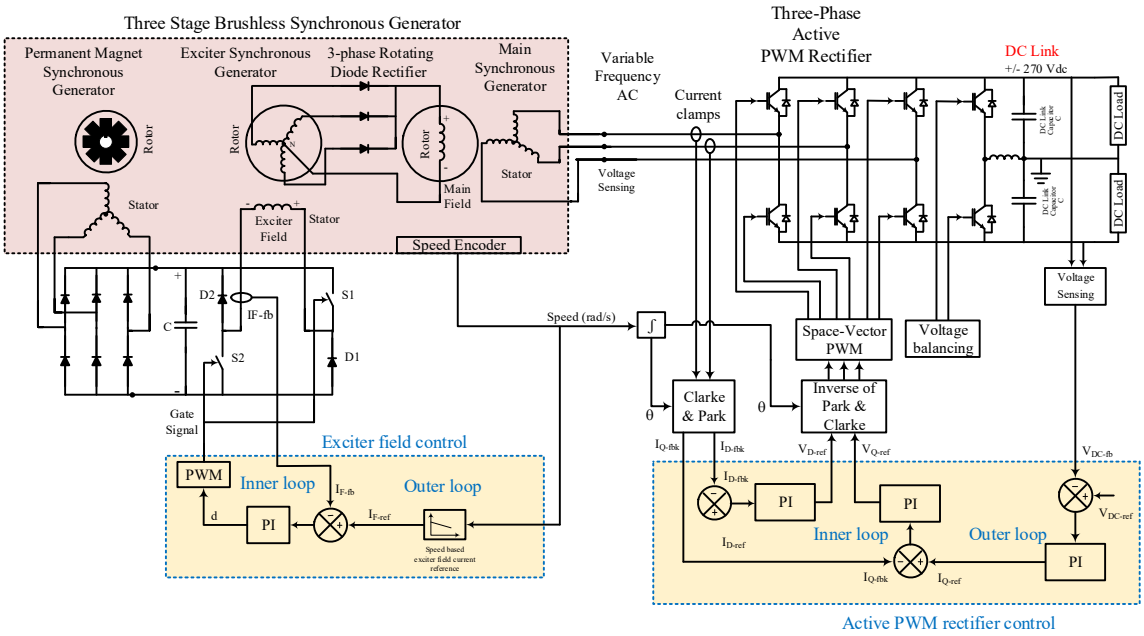


Fig. 4.2: Control block diagram of BSG based active rectifier regulated aircraft DC power system.

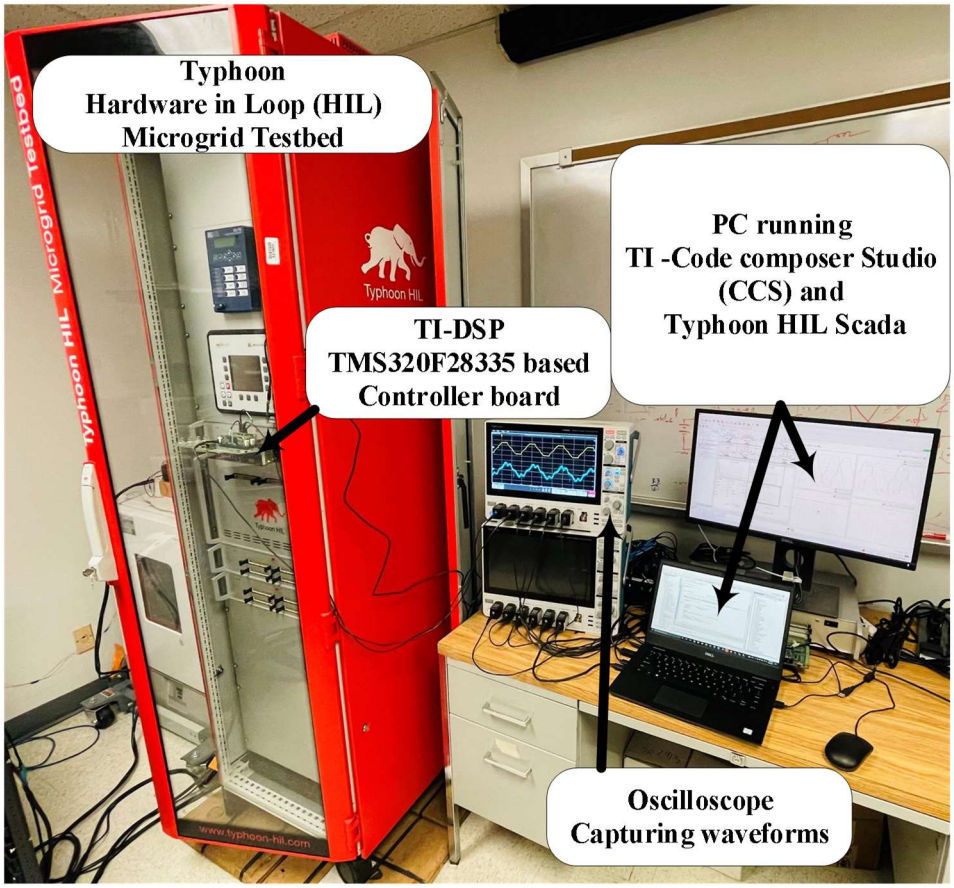
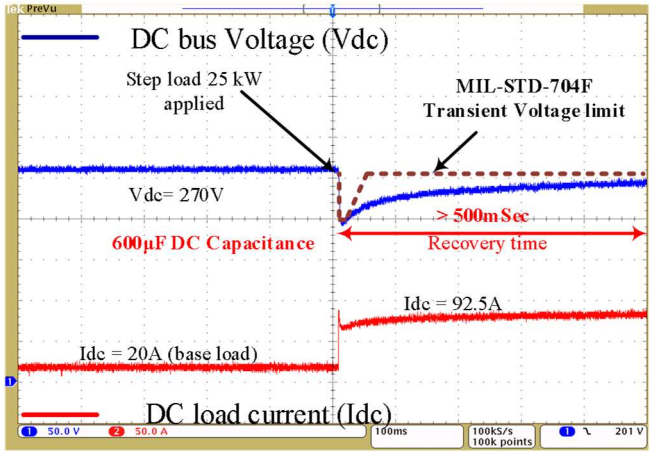


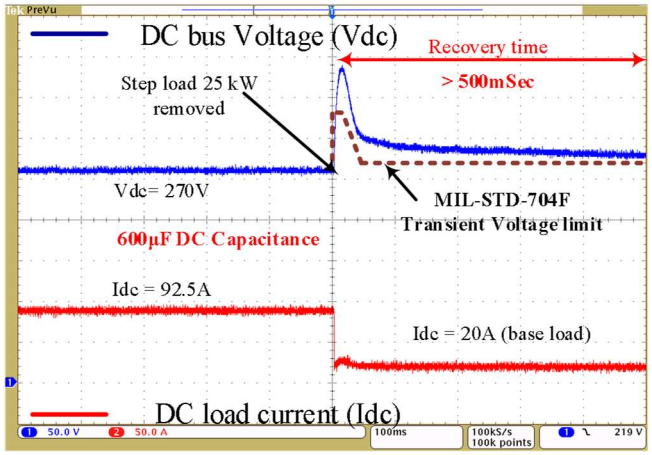
Fig. 4.3: C-HIL test set up.

independently implemented in two Texas Instruments DSP TMS320F28335 for a 25kW DC system and performed C-HIL simulations as shown in Fig. 4.3. The PI controller gains selected for the active rectifier and excitation control are: a) In outer voltage loop of active rectifier: Kp = 2, and Ki = 0.5; b) In inner current loop (DQ) of active rectifier: Kp =10, and Ki = 450 (based on BSG time constant); c) In exciter field current control: Kp = 20 and Ki = 455. The DC-link capacitance value chosen for the 25kW DC system is 600μF for BSG speed 7000rpm, which is based on a BSG based DC system using DBR with control improvements for reduced DC-link capacitance [41]. The BSG parameters used in C-HIL testing are adapted from chapter 2, table 2.1. The C-HIL test results for the BSG based active rectifier regulated DC power system with 600μF DC-link capacitor are shown in Fig. 4.4 (a) and (b) for the speed 7000rpm with a rated power of 25kW step load. Fig. 4.4 (c) shows the steady-state generated EMF, terminal voltage, and output current of the BSG during 25kW rated load at 7000rpm. It can be seen from Fig. 4.4 (a) and (b) that the DC-link voltage is regulated at 270V and the transient response shows that the DC-link voltage is able to successfully recover back to 270V during the step load conditions.

The results also show that, during transient step load conditions, the rate of change of DC-link voltage during transient step load is higher and the recovery time is slower than the required MIL-STD-704F [23]. As a result, the 270V DC system is not able to meet MIL-STD-704F transient voltage specifications. Hence, the control of the BSG based active rectifier regulated DC power system does not work effectively in meeting the transient voltage limits with 600μF DC-link capacitance. Fig. 4.4 (c) shows that the BSG is operating in a leading PF when the BSG is controlled in rotor FOC. This is mainly



(a)



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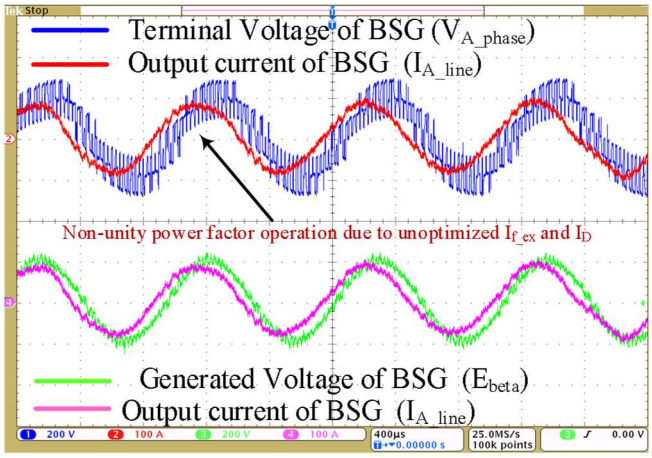


(c)

Fig. 4.4: C-HIL simulation results for speed 7000rpm without control improvements: a) DC-link voltage regulation when 25kW step load is applied; b) DC-link voltage regulation when 25kW step load is removed; c) Generated EMF, terminal voltage, and current of BSG during steady-state operation with 25kW load.

4.2.1 Phasor analysis of the BSG during steady state operation

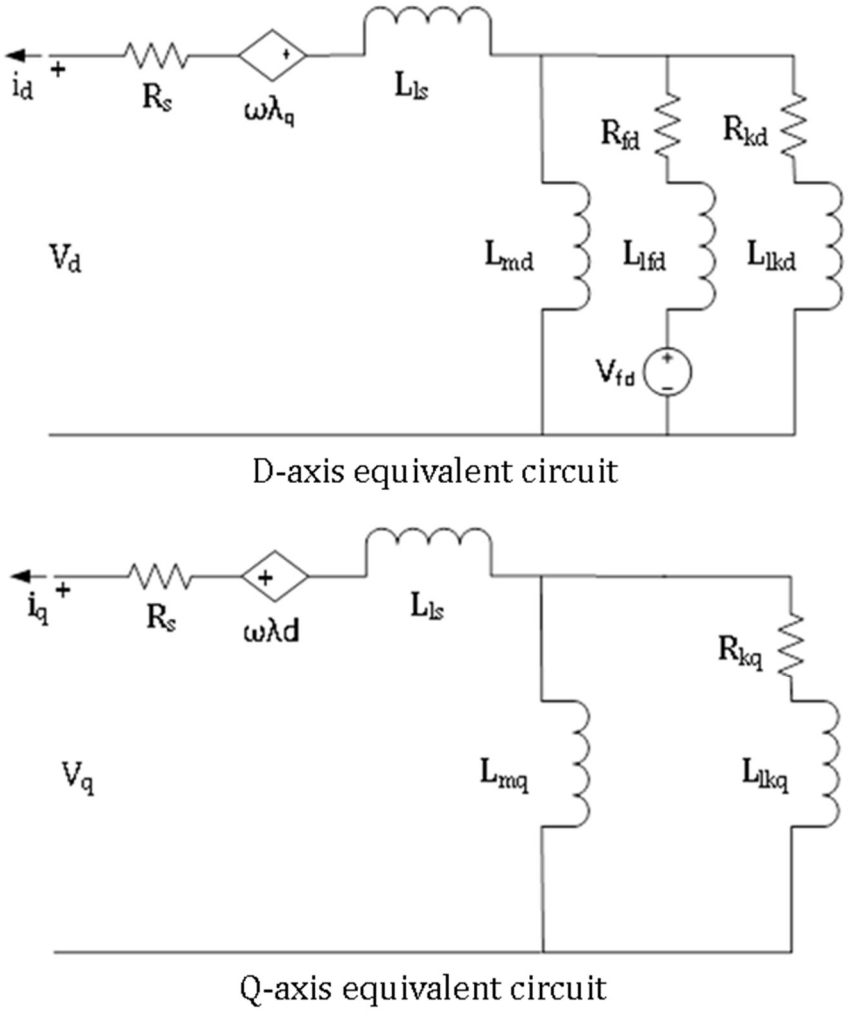


Fig. 4.5: DQ-axis equivalent circuit model of the SG.

because the active rectifier controls the Q-axis current of the BSG to supply DC power to the loads at the DC-link and maintains zero D-axis current due to the availability of a seperately excited field in the BSG.

The steady state phasor analysis of the BSG when controlled in FOC mode and the leading PF operation of the BSG are discussed in this subsection. Fig. 4.5 shows the DQ-axis equivalent circuit model of the SG. Based on the DQ-axis equivalent circuit model, the steady state DQ-axis terminal voltages of the SG are derived as [53]

$$V_D = -E_D - R_S I_D, \tag{4.1}$$

$$V_Q = \ E_Q - R_S I_Q, \tag{4.2}$$

$$E_D \ = \ \omega \lambda_Q, \tag{4.3}$$

$$E_Q \ = \ \omega \lambda_D, \tag{4.4}$$

$$\lambda_D = -L_{SD} I_D + L_{MD} I_{FD}, \tag{4.5}$$

and

$$\lambda_Q = -L_{SQ} i_Q, \tag{4.6}$$

where $I_D \ and \ I_Q$ are the DQ axis currents; $E_D \ and \ E_Q$ are the DQ axis generated voltages; I_{FD} is the field winding current; $\lambda_D \ and \ \lambda_Q$ are the DQ axis fluxes; $L_{SD} \ and \ L_{SQ}$ are the DQ axis stator inductances; ω is the angular velocity of the SG.

Based on equations (4.5) and (4.6), the steady state phasor diagram of the BSG is drawn for the case when BSG is operated in FOC mode, which is shown in Fig. 4.6. It can be seen from the phasor diagram, in FOC of BSG, I_D is maintained zero ($I_D = 0$) due to the presence of the seperately excited I_{FD} in the BSG. As a result, the output current (I_S) becomes inphase with I_Q and E_Q and consequently, the output current (I_S) leads its output terminal voltage (V_S). Hence it verifies that the BSG is operated in leading power factor when $I_D = 0$, as observed in Fig 4.4 (c).

In order to achieve UPF during steady state operation, the I_D and I_{FD} of the BSG need to be optimized. Hence, based on the steady state response shown in Fig. 4.4 and the steady state phasor diagram of the BSG shown in Fig. 4.6, it is very clear that the control

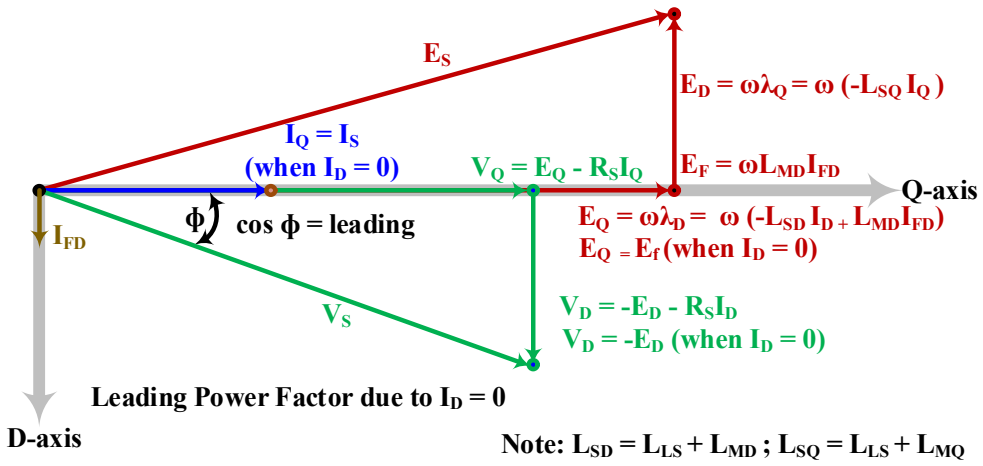


Fig. 4.6: Steady-state phasor diagram during FOC of Main SG when I_D is maintained zero.

of BSG based active rectifier regulated DC system needs control improvements to be able to achieve the objectives of this chapter such as:

1) Meet MIL-STD-704F transient voltage specifications;
2) Minimize the DC-link capacitance value;
3) Achieve UPF operation.

In this chapter, feedforward control improvements and a field optimization technique are proposed to overcome these slow transient response and power quality issues, and at the same time to reduce the DC-link capacitance required in the system. The proposed control improvements are explained in section 4.3.

4.3 Proposed control improvements for BSG based active rectifier regulated DC power system

Fig. 4.7 shows the control block diagram of the proposed feedforward control improvements and field optimization for the BSG based active rectifier regulated aircraft DC system. In order to meet the MIL-STD-704F transient voltage specifications at the DC-link with minimal DC-link capacitance and to maintain UPF operation, the BSG exciter

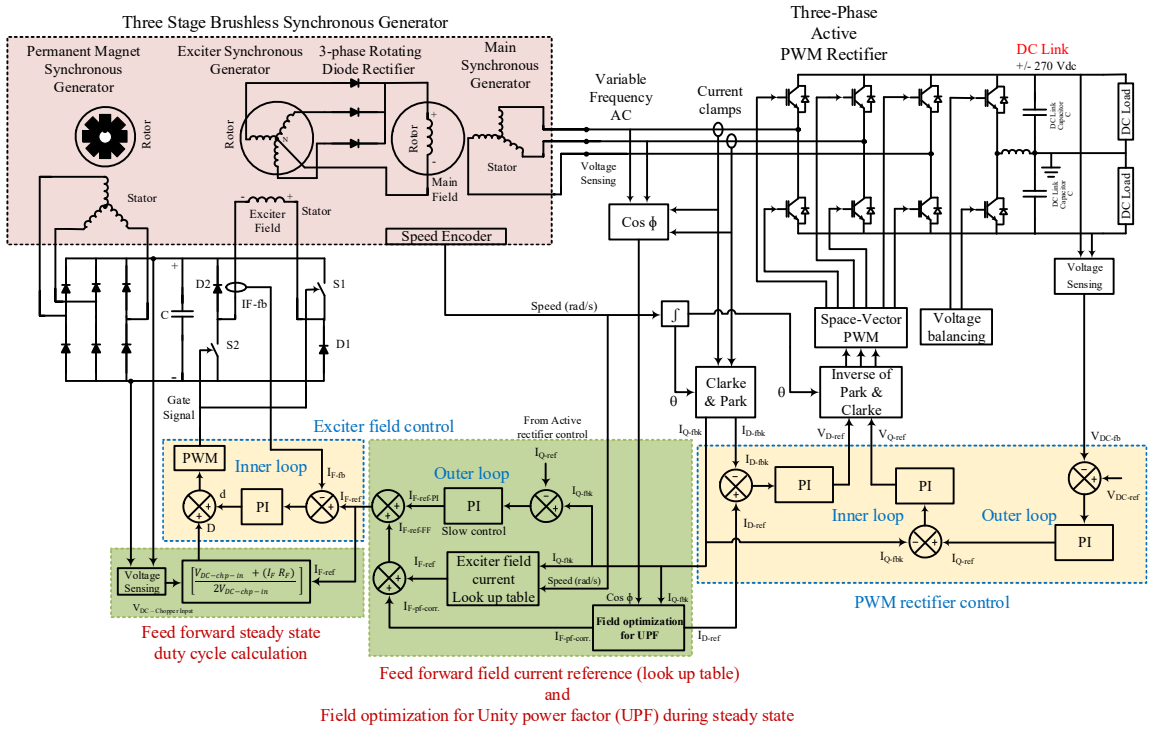


Fig. 4.7: Steady-state phasor diagram during FOC of Main SG when I_D is maintained zero ($I_D = 0$).

field control is introduced with the proposed control method which is a combination of three techniques:

1) Feedforward field current reference (lookup table) to the exciter SG field current control based on the Q-axis current of the main SG.

2) Feedforward steady-state duty cycle to the DC chopper.

3) Optimization of exciter field current and D-axis current of the BSG based on power factor and Q-axis current requirement.

Table 4.1 shows the feedforward exciter field current reference lookup table of the BSG. The lookup table values are obtained from the field/lab test data of the BSG during steady-state operation under different loads and speed conditions. During transient step load conditions at the DC-link, the field current reference value from the lookup table is

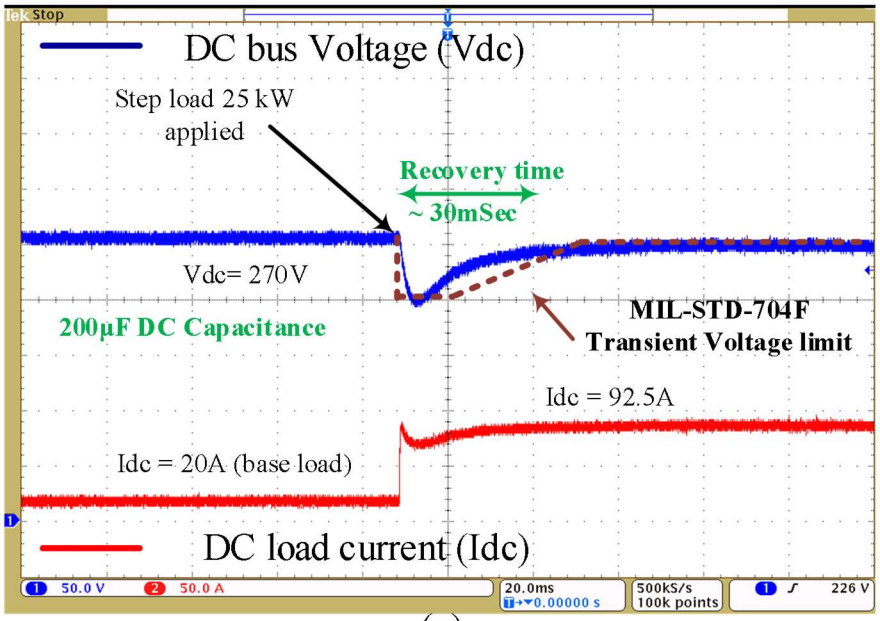
used in conjunction with a slow acting PI controller to provide a combined filed current reference to the exciter field current control of the DC chopper.

The feedforward lookup table provides an instantaneous field current reference required to improve the transient response at the DC-link. Moreover, the feedforward steady-state duty cycle of the two-quadrant DC chopper is adapted from chapter 2, equation (2.2) to provide duty cycle compensation needed for the DC chopper for the change in the input voltage of the two-quadrant DC chopper [41].

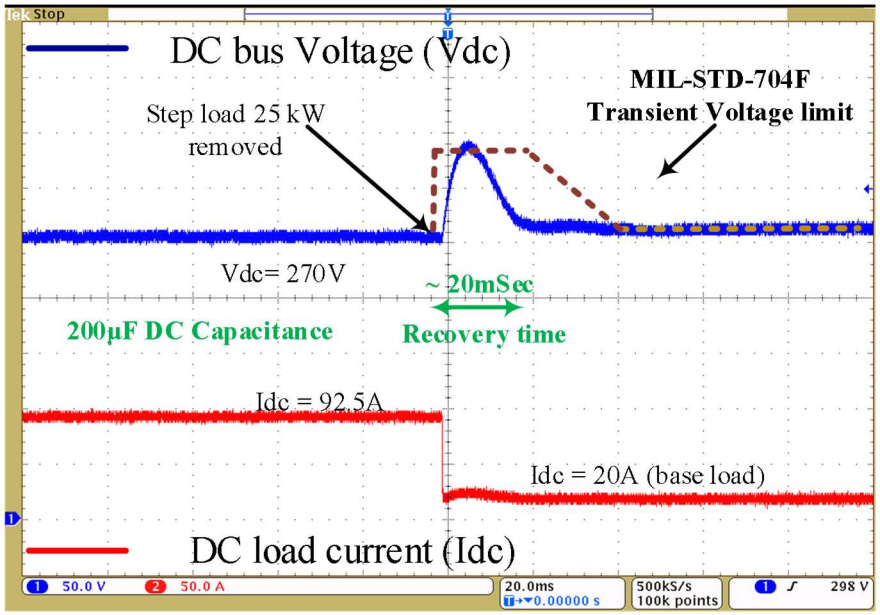
Table 4.1: Feedforward field current reference Lookup table of Exciter SG (in per-unit).

		Q axis current in P.U					
		0	0.2	0.4	0.6	0.8	1
Speed in RPM	7000	2.1	2.4	2.7	3	3.3	3.6
	8000	1.9	2.2	2.5	2.8	3.1	3.4
	9000	1.7	2	2.3	2.6	2.9	3.2
	10000	1.5	1.8	2.1	2.4	2.7	3
	11000	1.3	1.6	1.9	2.2	2.5	2.8
	12000	1.1	1.4	1.7	2	2.3	2.6
	13000	0.9	1.2	1.5	1.8	2.1	2.4
	14000	0.7	1	1.3	1.6	1.9	2.2

To achieve UPF operation during steady-state operating conditions (for load power above 10% of the rated load power at the DC-link), the D-axis current reference to the active rectifier FOC and the exciter SG field current reference are optimized based on power factor. Fig. 4.8 (a) and (b) show the C-HIL test results of the DC-link voltage regulation of BSG based active rectifier regulated DC system during 25kW step load at 7000rpm, with only 200µF DC-link capacitance with proposed control improvements. It can be seen from Fig. 4.8 (a) and (b) that the proposed control improvements enable faster transient response at the DC-link. The DC-link voltage recovery time during transients step load has reduced significantly to less than "~30mSec" which is more than 15 times faster than the transient step load response without any control improvements.



(a)



(b)

Fig. 4.8: C-HIL simulation results for speed 7000rpm with proposed improvements: a) DC-link voltage regulation when 25kW step load is applied; b) DC-link voltage regulation when 25kW step load is removed.

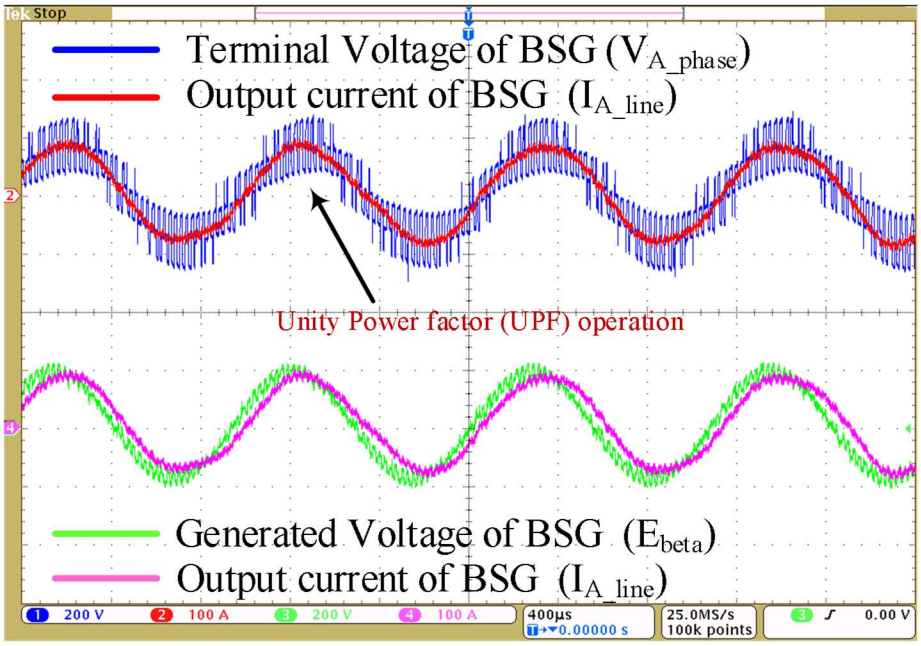


Fig. 4.9: Generated EMF, terminal voltage, and output current of BSG during steady-state operation with UPF for 25kW load at speed 7000rpm with proposed control improvements.

Fig. 4.9 shows the steady-state terminal voltage, generated EMF, and output current of the BSG with the proposed D-axis current and exciter field current reference optimization, maintaining UPF operation for 25kW rated load at 7000rpm. As per the steady-state phasor diagram of the BSG in active rectifier FOC, as shown in Fig. 4.10, a positive value of D-axis current is optimized based on I_Q and I_{FD} to achieve UPF operation. In summary, based on C-HIL test results shown in Fig. 4.8 and 4.9, it can be seen that the proposed control improvements have significantly reduced the DC-link capacitance value from 600µF to 200µF. The most significant result is that the BSG based active rectifier regulated +/-270V DC power system is able to meet MIL-STD-704F transient voltage specifications at the DC-link during transient step load (25kW) conditions with the minimized 200µF DC-link capacitance and maintaining UPF at the BSG output terminals during steady-state operating conditions.

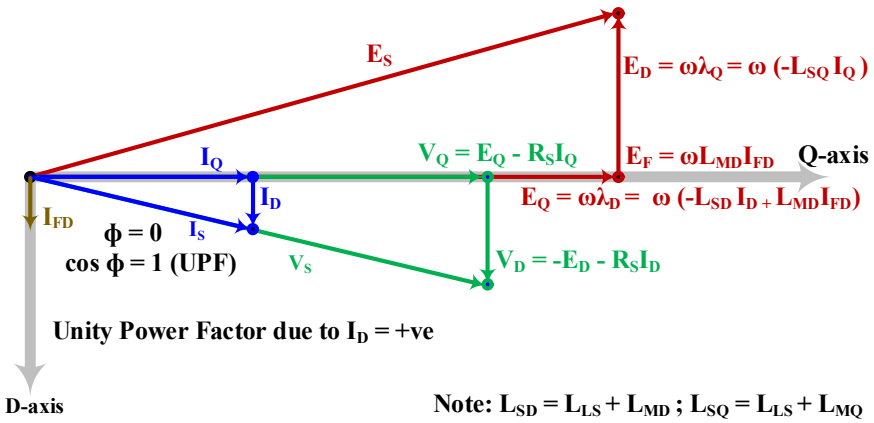


Fig. 4.10: Steady-state phasor diagram during FOC of Main SG when I_D is positive.

4.4 Summary

In this chapter, control improvements for BSG based active rectifier regulated aircraft DC power systems to minimize the DC-link capacitance required in the system and to improve transient response at the DC-link are proposed and validated through modeling and real-time C-HIL simulation. A field optimization technique is introduced to achieve UPF operation at the BSG output terminals. The C-HIL test results with the proposed control improvements at a speed of 7000rpm with 25kW step load, with only 200µF DC-link capacitance, are presented in this chapter. The real time simulation results obtained verify that the controller meets the MIL-STD-704F transient voltage specifications at the DC-link and at the same time maintains UPF at the BSG output terminals.

4.5 Publications

1. G. Selvaraj, K. R. Ramachandran Potti, S. R. P. Reddy, K. Rajashekara, "Control Strategy for a Brushless Synchronous Generator based Active Rectifier regulated DC Power System with minimal DC-link capacitance for More Electric Aircraft," *in Proc. IEEE COMPEL*, Nov 2021.

CHAPTER 5

EMI FILTER DESIGN FOR POWER ELECTRONICS CONVERTERS IN AIRCRAFT AC AND DC POWER SYSTEMS

5.1 Introduction

In aircraft EPS, the conducted Electro-Magnetic Interference (EMI) suppression is one of the critical requirements to keep the aircraft electrical and electronic equipment from malfunctioning due to the unwanted EMI from the surrounding equipment through conduction wires. The conducted EMI noises are high frequency signals generated in the electrical equipment such as switching PECs, electronic circuits, transformers , inductors, capacitors, etc. and create magnetic field that can interfere with the operation of surrounding electrical and electronic equipment in the EPS [54]. These conducted EMI noises have to be attenuated with in the permissible limits in the aircraft EPS using EMI filters. The main function of the EMI filter is to attenuate the EMI noise signals that flow from or to the line supply or load of the aircraft electrical and electronic equipment. In aircraft applications, the EMI and Electromagnetic compatibility (EMC) standards such as MIL-461G, and Radio Technical Commission for Aeronautics (RTCA) DO-160G are the most widely followed standards internationally to meet the unique requirements for military and civil aircraft respectively [54]. Fig. 5.1 shows the RTCA/DO-160G permitted EMI noise level for different categories of the aircraft system. As shown in Fig. 5.1, the DO-160G requires the Radio Frequency (RF) conducted EMI to be attenuated in the frequency range from 150kHz to 152MHz [55].

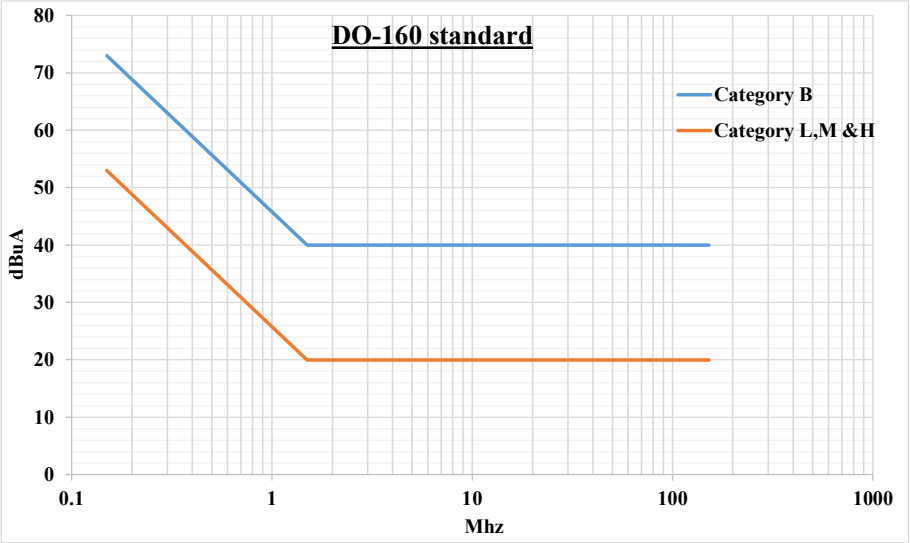


Fig. 5.1: RTCA/DO-160G: Standard test conditions for avionics electronic hardware in airborne systems.

In modern aircraft EPS, due to the increased usage of high power switching PECs with PWM and high switching frequency operation, the conducted EMI suppression becomes more challenging. Particularly, when the PECs are designed with high frequency digital control with tightly designed passive components such as DC-link capacitance to reduce the size of the PECs, the inclusion of EMI filters need to effectively attenuate the EMI without causing any negative effects in the normal operation of the PECs. Hence, when EMI filters are designed to attenuate the conducted EMI for PECs that use minimized DC-link capacitance, the effects of EMI filter in the control performance of the PECs need to be studied. Since the inclusion of EMI filter can modify the system equivalent circuit, the control performance of the PECs will be affected.

In this chapter, the EMI filter design for meeting the EMI/EMC requirements of the RTCA/DO-160G in civil aircraft for different PEC based AC and DC systems are studied. In addition, the performance of BSG based DRI regulated VSCF system using minimized DC-link capacitor that was introduced in chapter 3 is evaluated with and without the

inclusion of EMI filter. The effects of EMI filter on the control performance of the VSCF system are validated using C-HIL testing and the results show that the inclusion of EMI filter significantly affects the VSCF system stability during transient step load conditions.

5.2 Conducted EMI

In aircraft EPS, one of the ways the conducted EMI noises generate is due to the presence of switching PECs. The switching action in the PEC creates high frequency discontinuous currents at the input & output side of the PEC which creates voltage ripples and these voltage ripples conducted to other systems through physical contact of the conductors. The conducted EMI noise can be categorized in to two, they are:

1. Common mode (CM) noise
2. Differential mode (DM) noise

5.2.1 Common mode (CM) noise

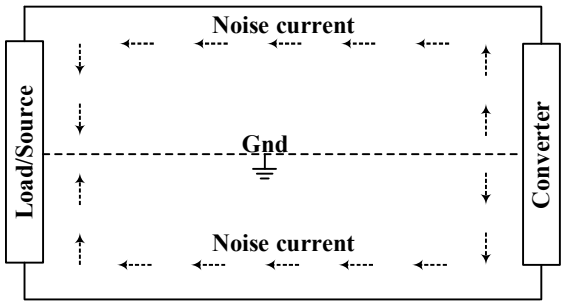


Fig. 5.2: Common mode noise in the PEC system that flows from converter to load/source.

The CM noise in the system is typically seen as the voltage difference between line and ground and it is mainly due to capacitive coupling in the system. The CM noise is common to all the lines with respect to ground and the noise current flows from the line to

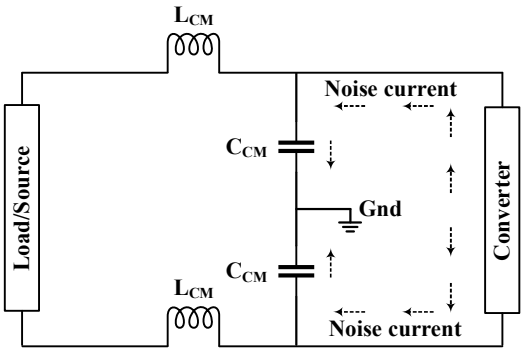


Fig. 5.3: LC common mode noise filter configuration.

ground in the same direction as shown in Fig. 5.2. The average value of CM noise voltage magnitude can be expressed as

$$V_{CM} = \frac{(V_{LINE1} + V_{LINE2})}{2}, \tag{5.1}$$

where V_{LINE1} and V_{LINE2} are the noise voltage magnitude of two lines with respect to ground. The CM noise in the system can be attenuated by using CM EMI filter [56]. Fig. 5.3 shows the LC CM noise filter configuration with CM inductance (L_{CM}) and capacitance (C_{CM} or Y capacitor). The Y capacitor (C_{CM}) value is limited to 4700Pf to limit the current flow to be less than 0.5mA to avoid the risk of electric shock. The L_{CM} is connected in series with the equipment so the value has to be chosen such that it carries the line/load current of the equipment. The typical design involves merging the two line L_{CM} into one to reduce the sizing of the filter. The L_{CM} and C_{CM} values are calculated from filter corner frequency as

$$L_{CM} = \frac{1}{(2\pi f_c)^2 \, C_{CM}}, \tag{5.2}$$

where f_c is the filter corner frequency which is calculated based on the order of the filter.

5.2.3 Differential mode noise

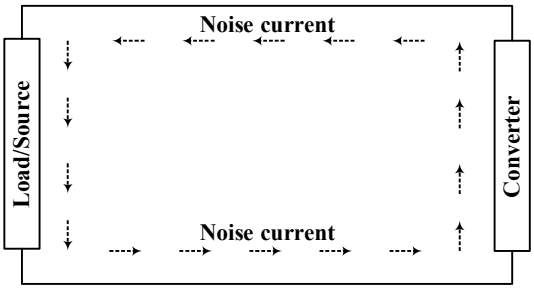


Fig. 5.4: Differential mode noise in the PEC system that flows from converter to load/source.

The DM noise in the system is typically seen as the voltage difference between two power lines or between line to return line or neutral. The DM noise is differential with respect to its return line or neutral. The DM noise current flows from the noise source through a line and returns back through the return line or neutral as shown in Fig. 5.4. The average value of DM noise voltage magnitude can be expressed as

$$V_{DM} = \frac{(V_{LINE1} - V_{LINE})}{2}. \tag{5.3}$$

The DM noise in the system can be attenuated by using DM EMI filter. Fig. 5.5 shows the LC DM noise filter configuration with DM inductance (L_{DM}) and capacitance (C_{DM} or X capacitor). The typical design of DM filter involves merging the DM filter into CM to reduce the size and at the same time to use the leakage inductance of the combined CM DM inductance as the equivalent value of L_{DM} [56]. Once the L_{DM} value and the f_c are known, the value of X capacitor (C_{DM}) can be calculated from

$$L_{DM} = \frac{1}{(2\pi f_c)^2 C_{DM}}. \tag{5.4}$$

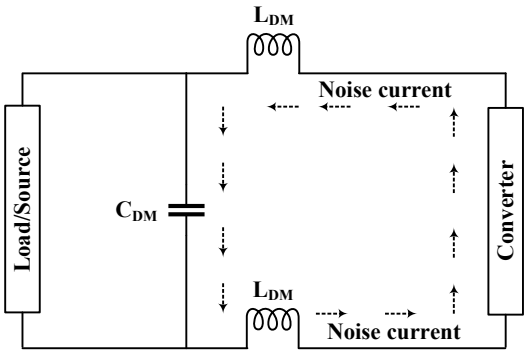


Fig. 5.5: LC differential mode noise filter configuration.

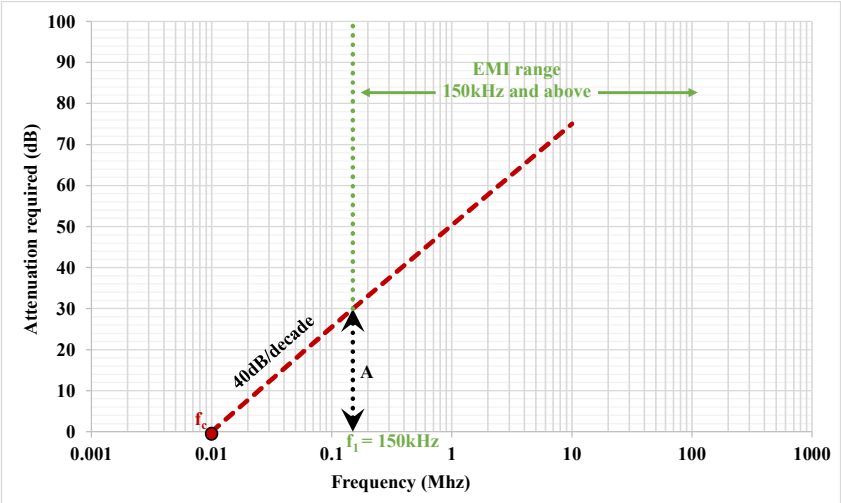


Fig. 5.6: Corner (fc) and cut-off (f1) frequency for a first order CM and DM filter with attenuation rate 40dB/decade for the required attenuation of A_{REQ}.

The corner frequency of the CM and DM filter for a 40dB/decade attenuation can be calculated as

$$f_{c\_CM\ or DM} = f_1 * 10^{\frac{-A_{REQ}}{40N}}, \tag{5.5}$$

where f_1 is the filter cut-off frequency, A_{REQ} is the required attenuation in dB and N is the order of the filter as shown in Fig. 5.6. The required attenuation A_{REQ} of the EMI filter can be expressed as

$$A_{REQ\_CM/DM}\ (dB) = V_{CM/DM}\ (dB) - V_{LIMIT\_CM/DM}\ (dB) + 3dB. \tag{5.6}$$

For example, if the $V_{CM/DM}$ is 100dB, in order to meet DO-160G standard, the V_{LIMIT} is 73dB at 150kHz so that the required attenuation A_{REQ} of the EMI filter is 33dB which is calculated based on 5.6.

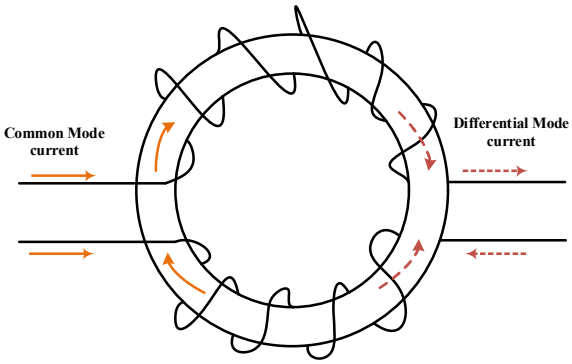


Fig. 5.7: Toroidal inductor core for both CM and DM Filter.

5.3 Combined CM and DM EMI filter

In order to reduce the size of the CM and DM EMI filter, a typical design method is to use the hybrid EMI filter which is a combination of both CM and DM EMI filter together. To realize a combined CM and DM filter, toroidal inductor core as shown in Fig. 5.7 is preferred. It can be seen from Fig. 5.7 that the CM and DM noise currents both flow in the same toroid. The equivalent L_{CM} of the toroid becomes $1/4^{th}$ the total inductance of the toroid (L_{TOTAL}). This is mainly because the CM noise signal flows in the same direction in both the lines in toroid winding as shown in Fig. 5.7, which makes the inductance value squared in both lines. On the other hand, the equivalent L_{DM} of the toroid becomes twice the total leakage inductance of the toroid (L_{LEAK}). This is mainly due to the flow of DM noise in opposite direction in the toroid windings as shown in Fig. 5.7, which makes the total differential inductance cancel each other and left with only leakage inductances in the two lines. Fig. 5.8 (a) and (b) shows the equivalent circuit of the EMI filter using toroidal core.

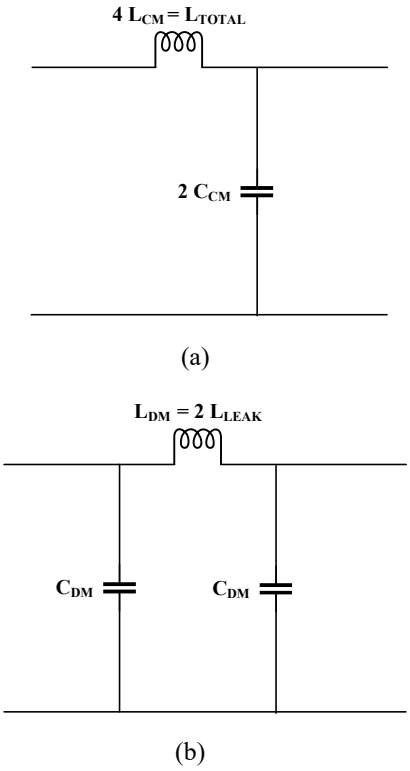


Fig. 5.8: Equivalent circuit of the toroidal core EMI: (a) CM filter; (b) DM filter.

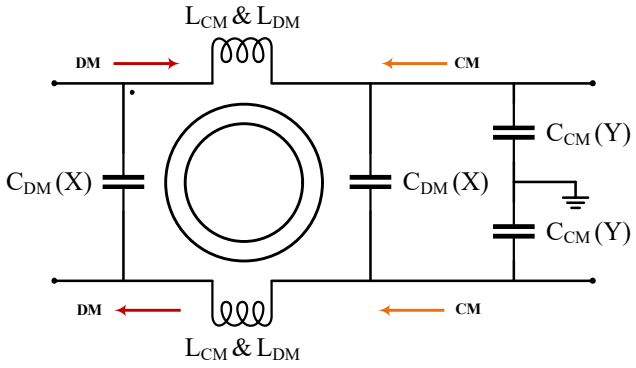


Fig. 5.9: Complete CM and DM EMI filter using toroidal core and XY capacitors.

Based on the equivalent circuit from Fig. 5.8, the L_{TOTAL} and L_{CM} can be expressed as

$$L_{TOTAL} = \frac{1}{(2\pi f_c)^2\ 2*C_{DM}}, \tag{5.7}$$

and

$$L_{CM} = \frac{L_{TOTAL}}{4}. \tag{5.8}$$

In toroid core, L_{LEAK} is approximately 1% of the L_{TOTAL}. Hence L_{DM} can be expressed as

$$L_{DM} = 2 * L_{LEAK}. \tag{5.9}$$

5.4 EMI filter design for PECs in BSG based aircraft EPS

In this section, the EMI filter design for BSG based PEC regulated AC and DC systems are explained. The CM and DM EMI filters are designed for switching PECs such as two-quadrant DC chopper, diode rectifier, active rectifier and four-leg inverter.

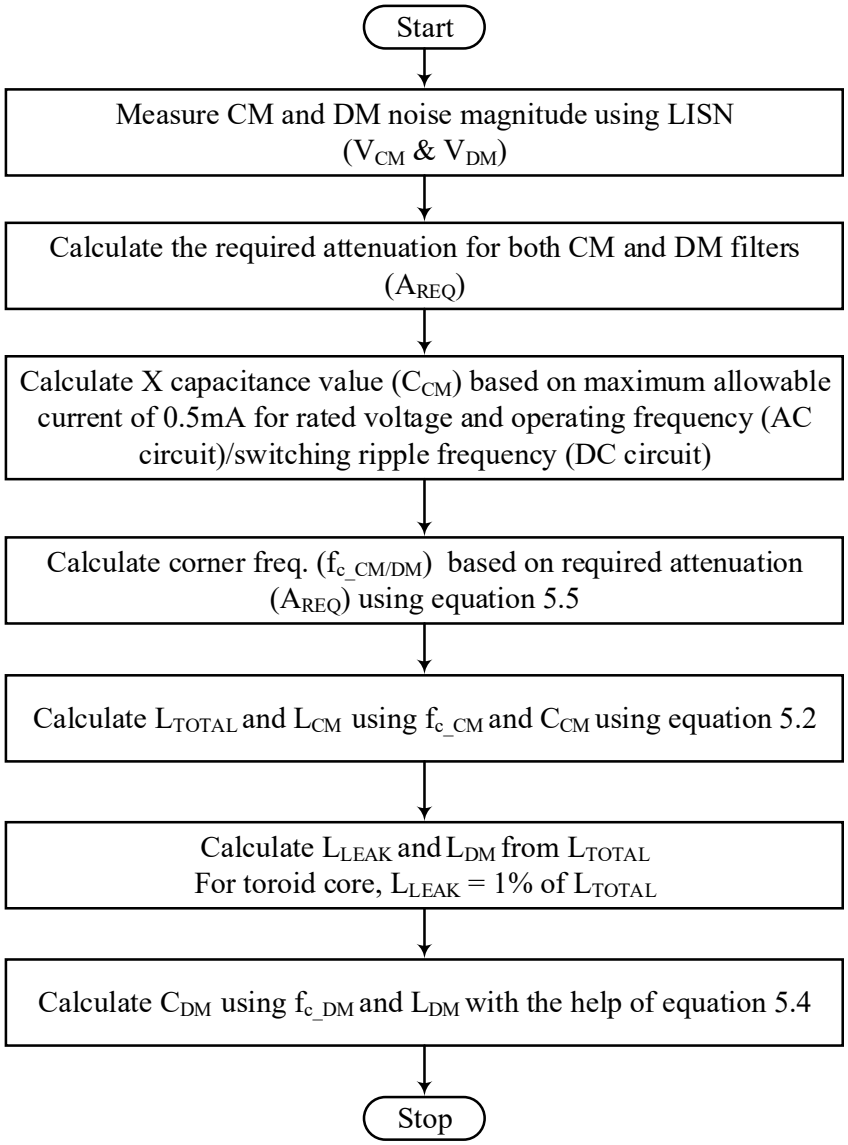


Fig. 5.10: EMI filter design procedure.

Table 5.1: EMI filter values for different PECs in the BSG based AC and DC systems

SI.NO	Description	EMI filter design values			
		for two-quadrant DC chopper at DC output: for converter in chapter 2, 3 & 4	for main diode rectifier at DC-link: for converter in chapter 2 & 3	for active rectifier at DC-link: for converter in chapter 4	for four-leg inverter output: for converter in chapter 3
1	Fundamental frequency	N/A	N/A	N/A	400Hz
2	Rated voltage	N/A	540 V_{DC}	+/- 270V_{DC}	115V_{AC}
3	f_l	150kHz	150kHz	150kHz	150kHz
4	V_{CM}	92dB (Assumed)	85dB (Assumed)	95dB (Assumed)	90dB (Assumed)
5	V_{DM}	90dB (Assumed)	65dB (Assumed)	75dB (Assumed)	85dB (Assumed)
6	A_{REQ} for CM	25dB	18dB	28dB	23dB
7	A_{REQ} for DM	23dB	13dB	8dB	18dB
8	f_{c_CM}	35.57kHz	53.22kHz	29.92kHz	39.91kHz
9	**C_{CM}**	**1.98nF**	**1.47nF**	**1.17nF**	**1.72nF**
10	L_{TOTAL}	5mH	3.03mH	11mH	4.5mH
11	**$L_{CM} = L_{TOTAL}/4$**	**1.2mH**	**0.75mH**	**0.29mH**	**1.1mH**
12	$L_{LEAK} = 1\%$ of L_{TOTAL}	50µH	30µH	120µH	46µH
13	**$L_{DM} = 2 * L_{LEAK}$**	**101µH**	**30µH**	**120µH**	**46µH**
14	f_{c_DM}	39.9kHz	70.9kHz	96.6kHz	53.2kHz
15	**C_{DM}**	**0.15µF**	**82nF**	**11nF**	**97nF**

Fig. 5.10 shows the flow chart of the EMI filter design procedure. It can be seen from Fig. 5.10 that the CM and DM noise for the PECs are measured using Line Impedance Simulation Network (LISN). Once the actual noise level is measured using LISN, the required attenuation (A_{REQ}) and the EMI filter parameters such as $f_{c\_CM/DM}$, L_{TOTAL}, L_{LEAK}, L_{CM}, C_{CM}, L_{DM}, and C_{DM} can be calculated based on the procedure from flowchart in Fig. 5.10. Table 5.1 shows the designed CM and DM filter values for different PECs in the BSG based DC and AC systems from chapter 2, 3 and 4. The V_{CM} and V_{DM} values used in this study are assumed values as shown in Table 5.1.

5.5 The effects of EMI filter on the control performance of the BSG based aircraft EPS

In aircraft EPS, EMI filters are used along with PECs to suppress the EMI with in the permissible limits required by the EMI/EMC standards such as RTCA/DO-160G and MIL-461G. In this chapter, the EMI filter design for different PECs in BSG based DC and AC systems are discussed in the previous sections. In this section, the effects of EMI filters on the control performance is discussed. For the purpose of this study, the BSG based DRI regulated VSCF system is tested with and without the inclusion of EMI filters. The control of VSCF system is adapted from chapter 3 which includes the BSG side DC-link voltage regulation using two-quadrant DC chopper control and four-leg inverter side AC output voltage control along with the combined control improvements from DC chopper and four-leg inverter to achieve reduction in DC-link capacitance (100μF) and meeting the MIL-STD-704F transient voltage specifications. The EMI filters are designed for DC chopper output and four-leg inverter output as shown in Fig. 5.11. The values of EMI filter components are tabulated in Table 5.1.

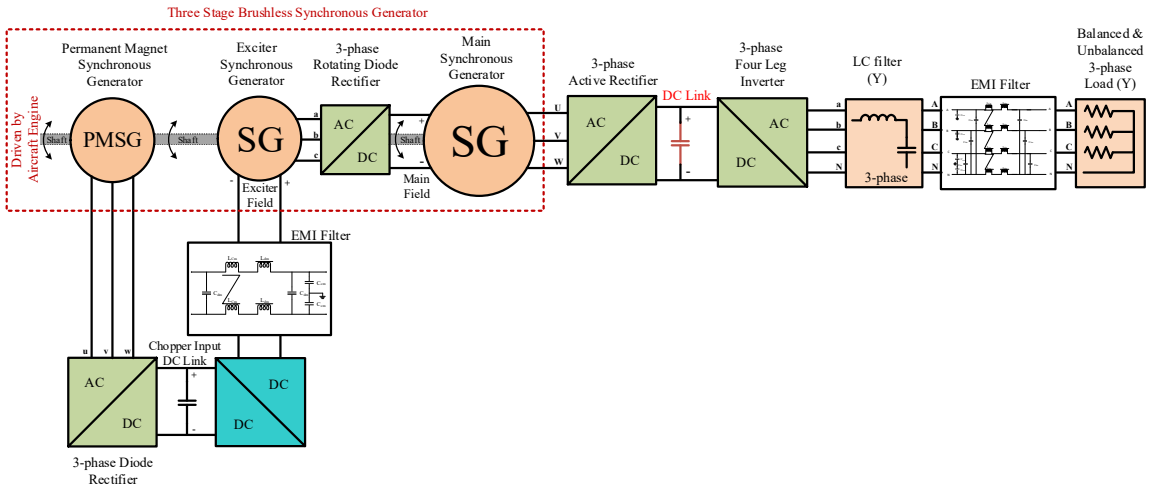


Fig. 5.11: BSG based DRI regulated AC VSCF system along with EMI filters.

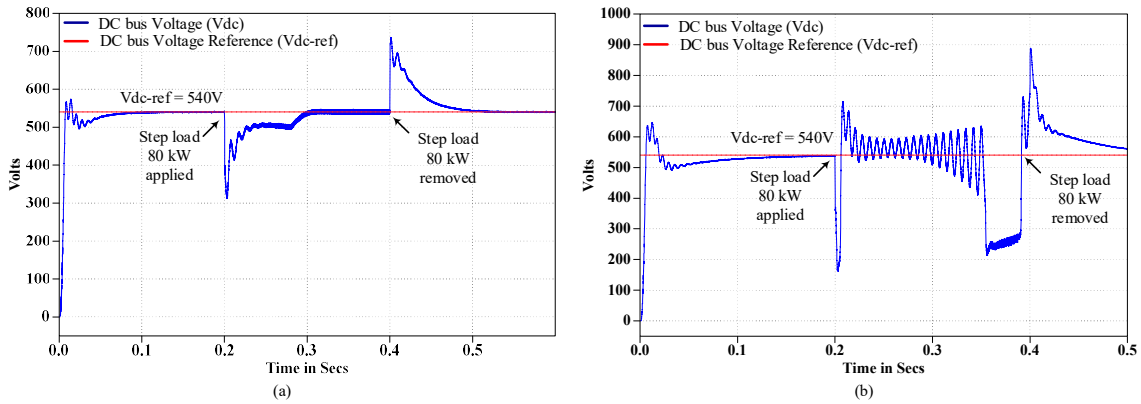


Fig. 5.12: DC-link voltage regulation of BSG based DRI regulated AC VSCF system during 80kW step load: (a) With EMI filters; (b) Without EMI filters.

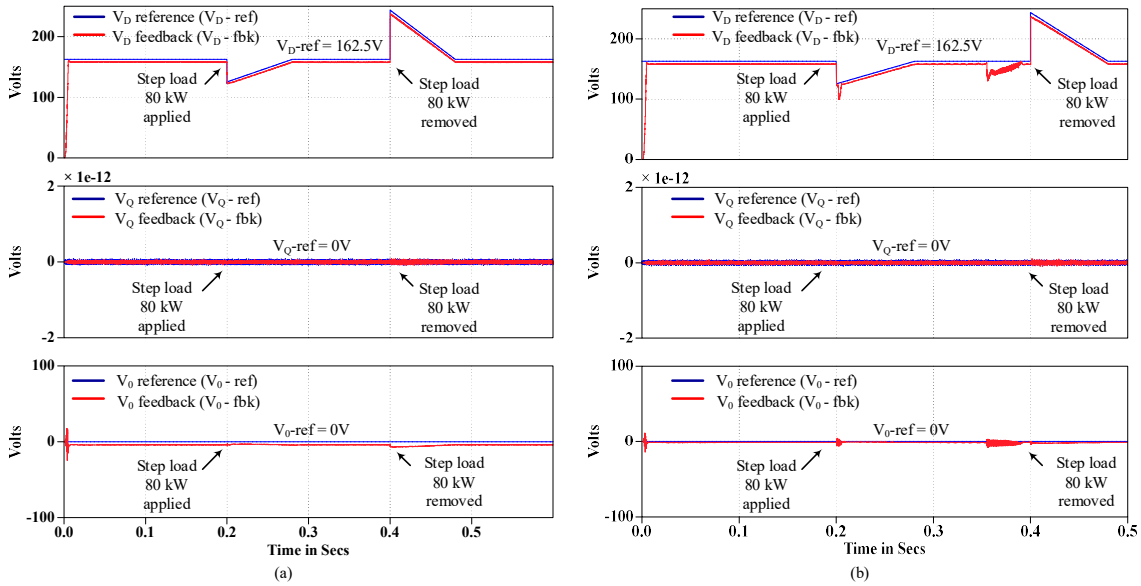


Fig. 5.13: DQO axes four-leg inverter output regulation of BSG based DRI regulated AC VSCF system during 80kW step load: (a) With EMI filters; (b) Without EMI filters.

Fig. 5.12 (a) and (b) show the comparison of transient response of the DC-link voltage regulation for 80kW step load with and without EMI filters. Similarly, Fig. 5.13 (a) and (b) show the comparison of transient response of the DQO axes inverter output voltage regulation for 80kW step load with and without EMI filters. It can be seen from Fig. 5.12 and 5.13 that the inclusion of EMI filters in the VSCF system alters the control

performance and make the DC-link voltage unstable when the step load is applied. In addition, the rate of change of DC-link voltage becomes very high and as a result the DC-link voltage no longer maintains the minimum required DC voltage to meet the MIL-STD-704F transient voltage specifications at the four-leg inverter output. Since the DC-link voltage becomes unstable and does not maintain the minimum required voltage during transient step load operation, the four-leg inverter output voltage does not meet the MIL-STD-704F transient voltage specification which can be seen in Fig. 5.13 (b). The effects of EMI filter is very prominent in the DC-link voltage regulation of the two-quadrant DC chopper. This is mainly because the inclusion of EMI filter at the DC chopper output modifies the output circuit from a simple first order system (Exciter SG field winding) to a multi order system and thus the steady state duty cycle feedforward calculation from chapter 2, subsection 2.2 becomes invalid.

Furthermore, the DC-link voltage regulation in the outer loop control of DC chopper becomes unstable and the minimized DC-link capacitance value of 100μF is not able to maintain stability at the DC-link. Hence, it can be inferred from this study that, while selecting the minimum DC-link capacitance and designing the control for a BSG based VSCF system, the effects of EMI filters on the system dynamics need to be considered and the control algorithm for BSG side DC-link voltage regulation need to be improved with faster and robust control techniques to overcome the effects of EMI filter in the system.

5.6 Summary

In this chapter, the Electromagnetic Interference (EMI) filter design and its effects on the control performance of the PECs in VF BSG based DC and AC aircraft EPS are

investigated. The conducted EMI noises such as Common mode (CM) and differential mode (DM) noises generated in PECs are suppressed within the permissible noise level based on Boeing DO-160 standard. The filter design using toroidal core is considered to combine both CM and DM noise filter reactor into one. The EMI filter design for the two-quadrant DC chopper, the active rectifier, and the four-leg inverter are explained in detail. The performance comparison between BSG based DRI regulated VSCF AC power system using minimized DC-link capacitance with and without the presence of EMI filter is analyzed and the effects of EMI filter on the control of DRI regulated VSCF system is verified with the help of real-time C-HIL and the results show that the inclusion of EMI filter significantly affects the control performance of the DC chopper control and makes the system unstable.

5.7 Publications

1. G. Selvaraj, S. R. P. Reddy, K. R. Ramachandran Potti, K. Rajashekara, "Stability analysis of Brushless Synchronous Generator based Active Rectifier Inverter regulated Variable Speed Constant Frequency AC Power System with minimal DC-link capacitance and EMI filter," *in IEEE Open J. on Power Electron., 2021 (To be submitted)*

CHAPTER 6

CONCLUSION

In this dissertation, control strategies for minimizing the DC-link capacitance in the PECs for aircraft AC and DC backup power system are investigated.

The minimization of DC-link capacitance for a VF BSG based 50kW 270V DC system using diode rectifier is investigated in which the DC-link voltage regulation is obtained through the excitation control of the exciter SG using two-quadrant DC chopper. A steady state feedforward duty ratio and output power based feedforward exciter field current reference are proposed to improve the transient response of the DC system to meet the military standard (MIL-STD-704F) transient voltage specifications with minimized DC-link capacitance.

An 80kVA VF BSG based diode rectifier inverter (DRI) regulated 115V, 400Hz AC variable speed constant frequency system (VSCF) is investigated. In VSCF system, the control improvements from BSG based DC system is used along with a novel adaptive inverter voltage reference (AIVR) algorithm in the four-leg inverter side to reduce the effects of four-leg inverter side fast dynamics. The combined control improvements helps to meet the stringent MIL-STD-704F transient voltage specifications at the inverter output with minimum the DC-link capacitance required in the VSCF system.

Further, the VF BSG based DC system is investigated with active rectifier in place of diode rectifier. An improved DC-link voltage regulation based on field oriented control (FOC) of the VF BSG along with a feedforward excitation control for fast transient operation is proposed to further improve the transient response of the DC-link voltage and

reduce the DC-link capacitance when compared to diode rectifier based DC system. A steady state rotor flux optimization algorithm derived based on steady state equations of VF BSG is proposed to maintain unity power factor (UPF) operation at the BSG terminals during steady state operating conditions.

Finally, the EMI filter design for VF BSG based PEC regulated DC and AC systems are studied for aircraft EPS by following DO-STD-160. The EMI filters are designed for different PECs in AC and DC systems such as two-quadrant DC chopper, active rectifier, and four-leg inverter. The transient performance of the VSCF AC system control with minimized DC-link capacitance is compared for cases with and without EMI filters and the interaction of EMI filters with the fast transient control algorithms are studied and presented with real-time C-HIL testing results..

6.1 Future work

The future scope of this research in the areas such as:

- Aircraft EPS with control improvements for the PEC based DC and AC systems with EMI filters and minimized DC-link capacitance.
- Control improvements for BSG backup power system with loads in both 115V, 400Hz AC and 270V DC with strict AC and DC transient voltage limits.
- The VF BSG machine model based exciter SG field current estimation to replace the look up table approach.
- Induction Generator based AC and DC Systems with control improvements for minimization of DC-link capacitance.

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