PULSE HEIGHT ANALYSIS
USING ATHENA COMPUTER

An Abstract of a Thesis

Presented to

the Faculty of the Department of Electrical Engineering

University of Houston

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

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ABSTRACT

A pulse height analyzer which sorts and converts pulses according to their height with the remote operation mode has been designed and constructed. The analyzer system consists of a pulse height-to-digital converter, the Athena Computer, and two digital-to-analog converters. The pulse height-to-digital converter converts input data pulses (0.2V~2V height, 2μs~10μs width) to 7-digit binary outputs which are proportional to the pulse height. The digitized input data pulses are stored in the 127 different core addresses of the Athena Computer determined by their height. The digital-to-analog converters displays a plot of the number of pulses versus pulse height of the stored data on an oscilloscope. The remote operation which performs clearing of the magnetic core storage, data-loading, and readout-data is accomplished by using several of the special features of the Athena Computer.

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CHAPTER I

INTRODUCTION

In nuclear spectroscopy, data is often obtained from a detector in the form of electrical pulses whose height is proportional to the energy of the particle being detected. The physicist many times would like to sort these pulses into increments of pulse height and count the number of each increment of height. If the number of pulses is plotted versus pulse height then an energy distribution is obtained for the radiation being detected.

It is also often desirable to plot the number of occurrences of events versus the time of the event after some known occurrences. This time can be converted to a pulse whose height is proportional to the time and these pulse heights can then be sorted.

An instrument which sorts and converts pulses according to their height is called a pulse height analyzer. A system was built which would allow the Athena Computer to be used as a pulse height analyzer. The system is a self-contained controller-digitizer which allows remote operation of the computer. The system block diagram is shown in Fig. 1-1.

The counter type pulse height-to-digital converter

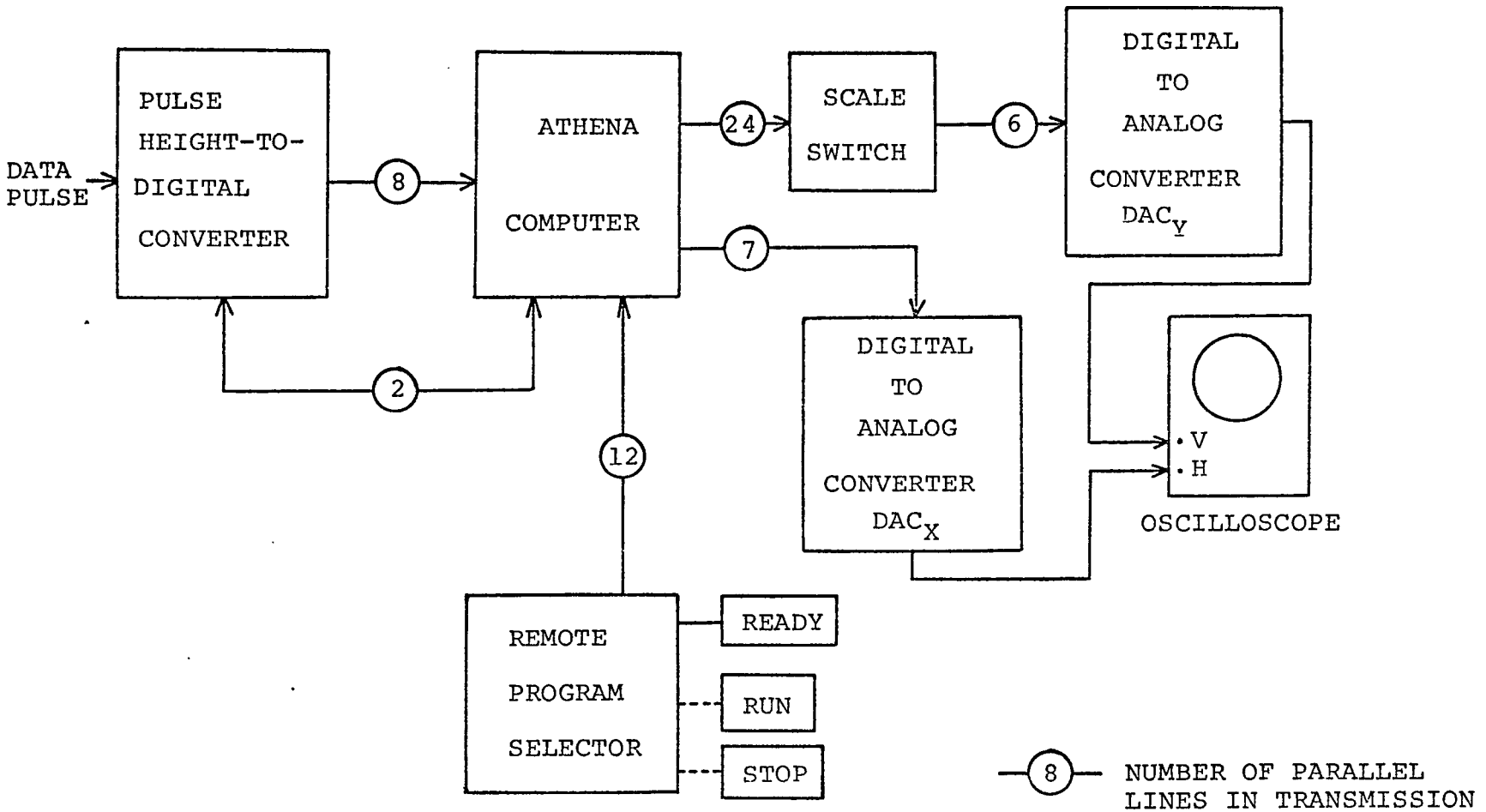


Fig. 1-1 BLOCK DIAGRAM OF SYSTEM

(PHDC) provides 7-bit binary output for input pulses from +0.2V to 2.0V. The digital outputs are loaded in the 127 magnetic core addresses of the Athena by a data-loading program which performs the following functions:

(1) Read the digitized pulse height from the pulse height-to-digital converter.

(2) Add one to the contents of the core address given by the digitized data from the PHDC.

(3) Send a timing pulse to the PHDC and receive a timing pulse from the PHDC.

For readout data from the computer to an oscilloscope, two digital-to-analog converters (DAC_X and DAC_Y) are used. The 7 digital outputs of the Index Register (pulse height) go to the DAC_X input stage and the analog output of the DAC_X is used as a horizontal input signal of the oscilloscope. A selected 6-bits group of the display register outputs (number of pulses) is applied to the DAC_Y to drive the vertical display on the oscilloscope. For the remote data-process there are three pre-loaded programs on the drum storage of the computer. These programs perform the following:

(1) Clear the counter block of the magnetic core storage.

(2) Load data.

(3) Readout data.

The Athena was a special purpose digital computer which interpreted missile position data by the radar system. It operates in the parallel mode of data transmission. One of the advantages of using Athena is the remote program-choice. The choice of a program among the pre-loaded ten programs can be done simply by depressing a specified program pushbutton. Also, the current Athena has several modified features which include expanded word length (18 bits) of the drum storage, index register (8 bits), and more available operational codes. The major disadvantage is low speed of the drum (200 KC). More detailed specifications of the system are shown in Table 1-1, 1-2, and 1-3.

PULSE HEIGHT/DIGITAL CONVERTER

Input pulse height	positive 0.2~2.0V
Input pulse width	2μs~10μs
Quantization	7 bits, 127 levels of 20mV each
Linearity	± 1.6%
Clock-rate	4.755 MHZ
Analysis Time	38μs (max.)
External timing pulse input	0 to -2V (2μs) pulse from the Athena
Power supply	built-in +10V, +5V, -4V, -10V, -15V 3 W (max.) dissipation
Complexity	6 I. C. packs 100 discrete semi-conductors (approx.)

Table 1-1 SPECIFICATION OF SYSTEM

ATHENA COMPUTER

Magnetic drum speed	200KC (12000 rpm)
Magnetic drum storage	8192 words 8 groups (1024 words/gr) 18 bits/word
Magnetic core storage	256 words 24 bits/word
Minimum execute time of an instruction	40μs
Maximum number of program sectors for remote selection	10 (256 drum words/sector)
Number of current instruction	45

Table 1-2 SPECIFICATION OF SYSTEM

DIGITAL/ANALOG CONVERTER

Decoder type	Resistor ladder R = 10K 1% 2R = 20K 1%
Op. Amp.	μA709 X2 (Fairchild)
Reference Voltage	-4V
Input stage	DAC_X : 7-bit Logic 1 0V Logic 0 -2V DAC_Y : 6-bit Logic 1 -10V Logic 0 0V
Full scale output	+4V
Scale switch for DAC_Y	7 positions for 24 bits (1) $2^0 - 2^5$ (2) $2^2 - 2^7$ (3) $2^4 - 2^9$ (4) $2^6 - 2^{11}$ (5) $2^8 - 2^{13}$ (6) $2^{10} - 2^{15}$ (7) $2^{12} - 2^{17}$

Table 1-3 SPECIFICATION OF SYSTEM

CHAPTER II

SYSTEM AND CIRCUIT DESIGN

Pulse Height-to-Digital Converter

The PHDC, shown schematically in Fig. 2-1, is of the capacitor-discharge,counter type. The input data pulses pass through the Linear Gate and generate pulses from the PHWC (Pulse Height-to-Width Converter) which are proportional to the amplitude of data pulses. These pulses gate the clock pulses with a logic and gate. The gated clock pulses are counted by 7-bit Binary Counter and the digital information is applied to the computer for data-loading through the Data Driver stage. The eight pilot lamps of Monitor Driver indicate the digital output of data pulses. The Trigger Pulse Generator is a monostable-multivibrator. The output gate of PHWC generates a trigger pulse which closes the Linear Gate to inhibit next coming pulses until the first data is stored in the computer memory. The Sync. Pulse Generator monostable-multivibrator is also triggered by the output gate of PHWC at the leading-edge (Fig. 2-2I). The sync. pulses go to the computer to synchronize the data-loading process. The Reset Pulse Generator monostable-multivibrator receives a trigger pulse from the computer immediately after finishing data-loading of an input data

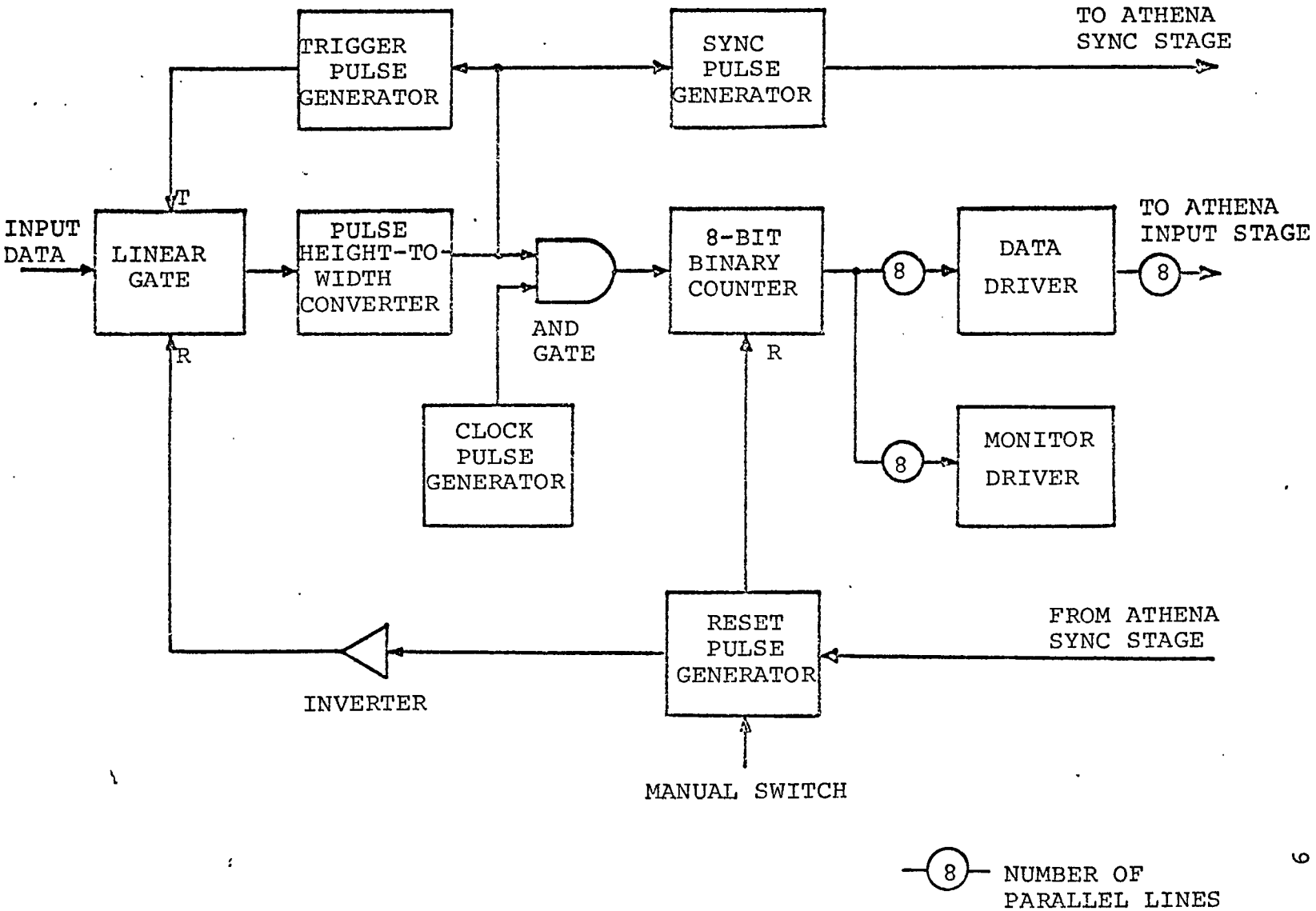


Fig. 2-1 BLOCK DIAGRAM OF PHDC

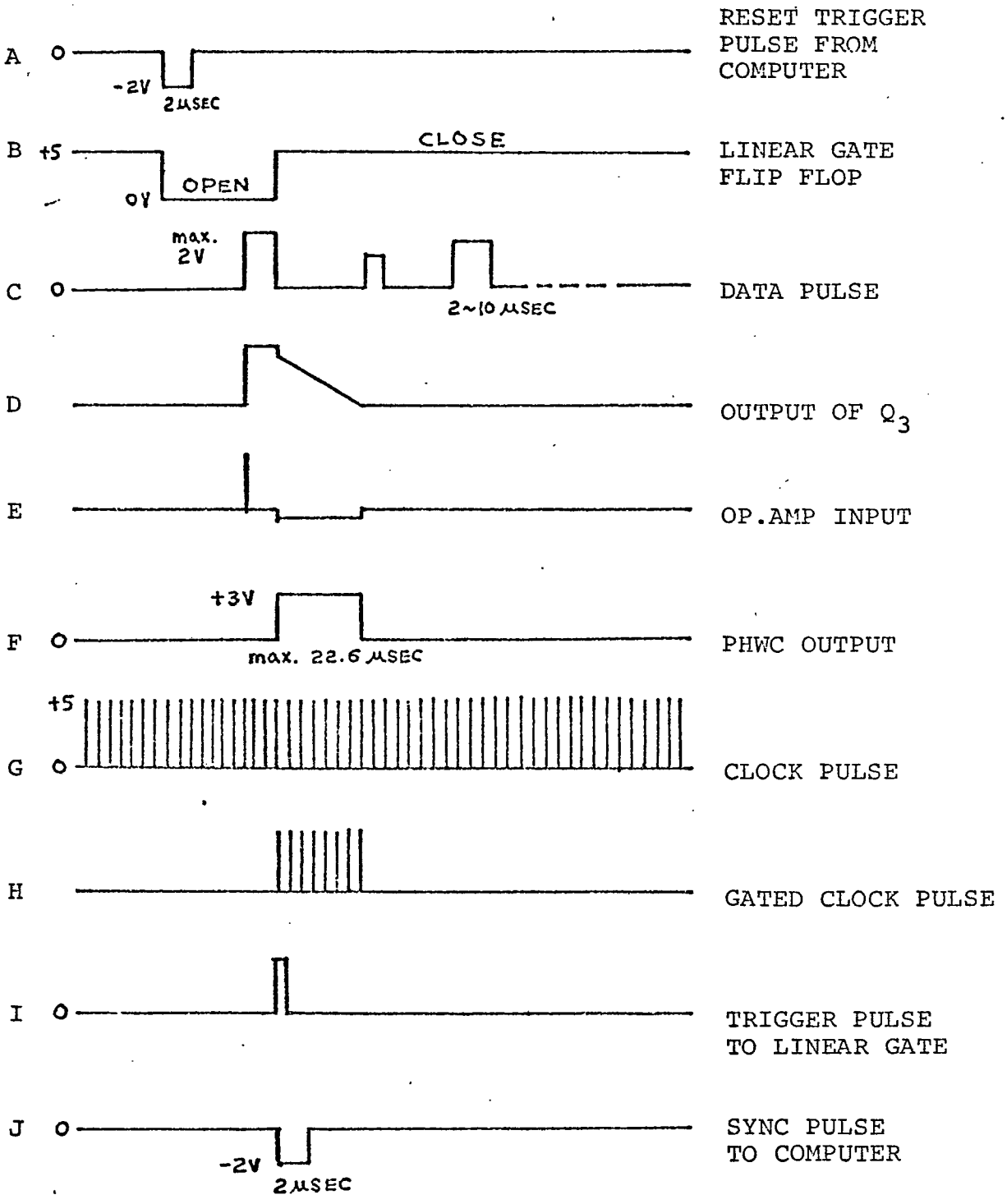


Fig. 2-2 TIMING DIAGRAM OF SYSTEM

pulse (Fig. 2-2A). The reset pulse clears the Binary Counter and open the Linear Gate so that another pulse can be processed (Fig. 2-2B). The manual reset switch is provided for initiating the system process.

The Linear Gate

The Linear Gate, shown in Fig. 2-3, uses a N-Channel Field Effect Transistor Q_1 and a J-K FF for gating Q_1. The high level output (+5v) of FF provides OFF gating bias (-15v) through the gate driver Q_2. The high impedance of drain-source junctions of Q_1 (OFF state) prevents passing any pulses. Reset pulse from Reset Pulse Generator change the high level output of FF into low level (0v). The low level output turns on Q_1 and the drain-source junctions have low impedance (200 ohms) allowing a data pulse to the PHWC stage. A trigger pulse by the output gate of PHWC changes the low level to the high level of FF, then turns OFF Q_1. (Fig. 2-2B)

Pulse Height-to-Width Converter

Conversion of the +0.2 to 2-volt input pulse to a gate whose width is proportional to the height is accomplished by the PHWC, shown in Fig. 2-4. Action of the gate is dependent on a constant-current generator discharging capacitor C_1 which is charged to the pulse height. Since

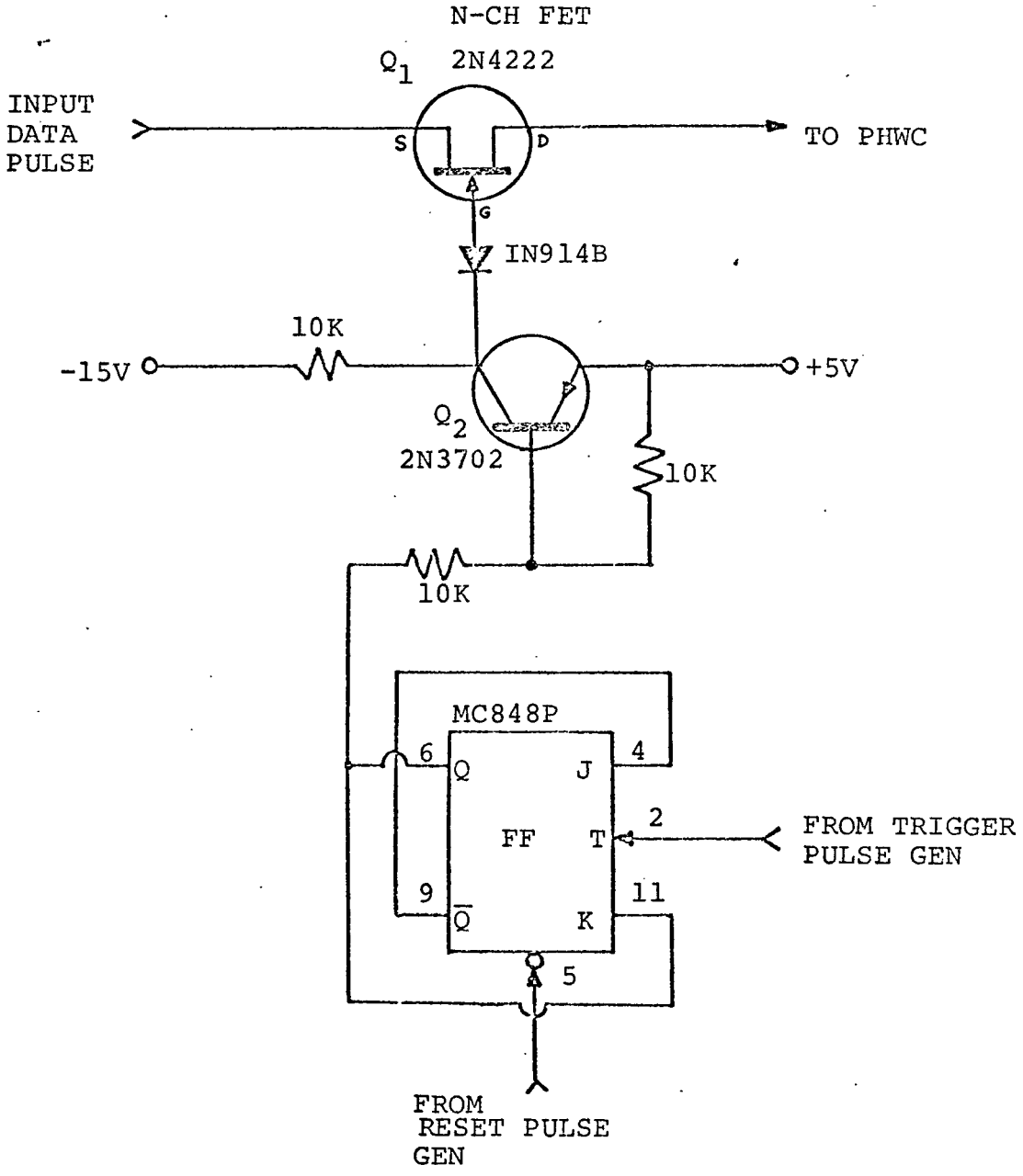


Fig. 2-3 LINEAR GATE

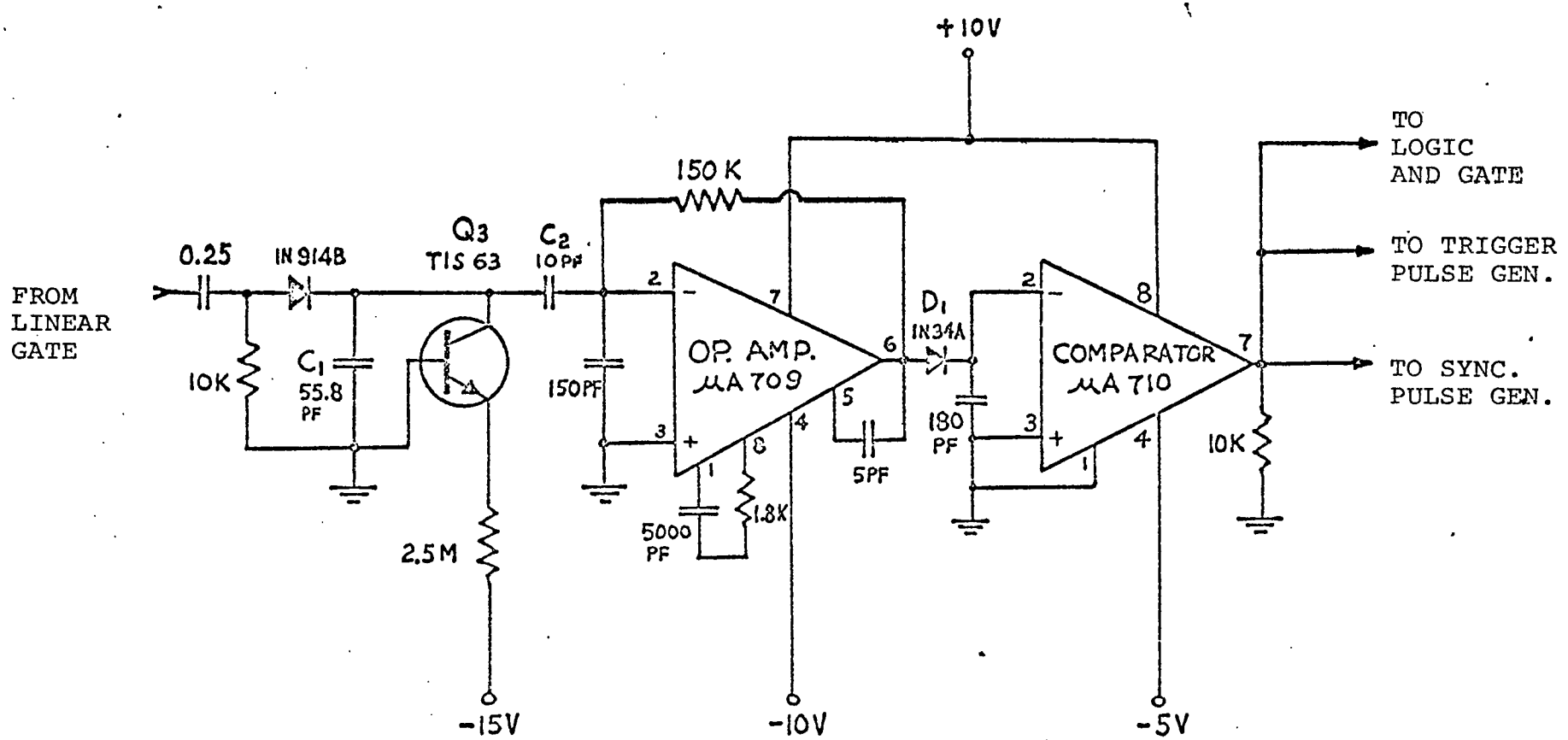


Fig. 2-4 PHWC (PULSE HEIGHT-TO-WIDTH CONVERTER)

the capacitor C_1 is connected to the collector of the NPN grounded-base transistor Q_3, it starts to discharge after the input pulse has dropped to zero. The high impedance in the emitter of the transistor Q_3 limits the emitter to a low current. The I_c vs E_c characteristics of this configuration show that the collector current is constant for wide variation of the collector voltage. The charge on the capacitor C_1 is removed at a constant rate; therefore the voltage is reduced linearly (Fig. 2-2D). The constant-current generator run-down is set at 22.6 μsec for a 2-v input pulse. The output pulse of Q_3 is differentiated by the capacitor C_2, resulting in a leading-edge spike and a gate whose width is proportional to the height of the pulse (Fig. 2-2E). The operational amplifier (integrated circuit) amplifies the gate and inverts the polarity. The diode D_1 clips the unwanted spike and the comparator (integrated circuit) produces a positive level gate (+3v) comparing with ground level (Fig. 2-2F). Then, the gate is applied to the logic AND gate with the clock pulses (4.755 MHz) for counting proportional to the data pulse height. The linearity of PHWC vs data pulse height and width is shown in Fig. 2-5A,B.

Clock Pulse Generator

The Clock Pulse Generator, shown in Fig. 2-6, is

Input Pulse HEIGHT \ Input Pulse Width	2μs	3μs	4μs	5μs	6μs	7μs	8μs	9μs	10μs
0.2V	10	12	12	12	12	12	12	12	11
0.25V	14	14	14	14	14	14	14	14	14
0.50V	27	28	28	28	28	28	28	28	28
0.75V	40	41	42	42	42	42	42	42	42
1.00V	52	56	56	56	56	56	56	56	56
1.25V	64	66	67	68	68	68	68	68	68
1.50V	76	80	82	82	82	82	82	82	81
1.75V	88	92	93	93	93	93	93	93	93
2.00V	100	106	108	108	108	108	108	108	108

Fig. 2-5A THE LINEARITY OF PHDC

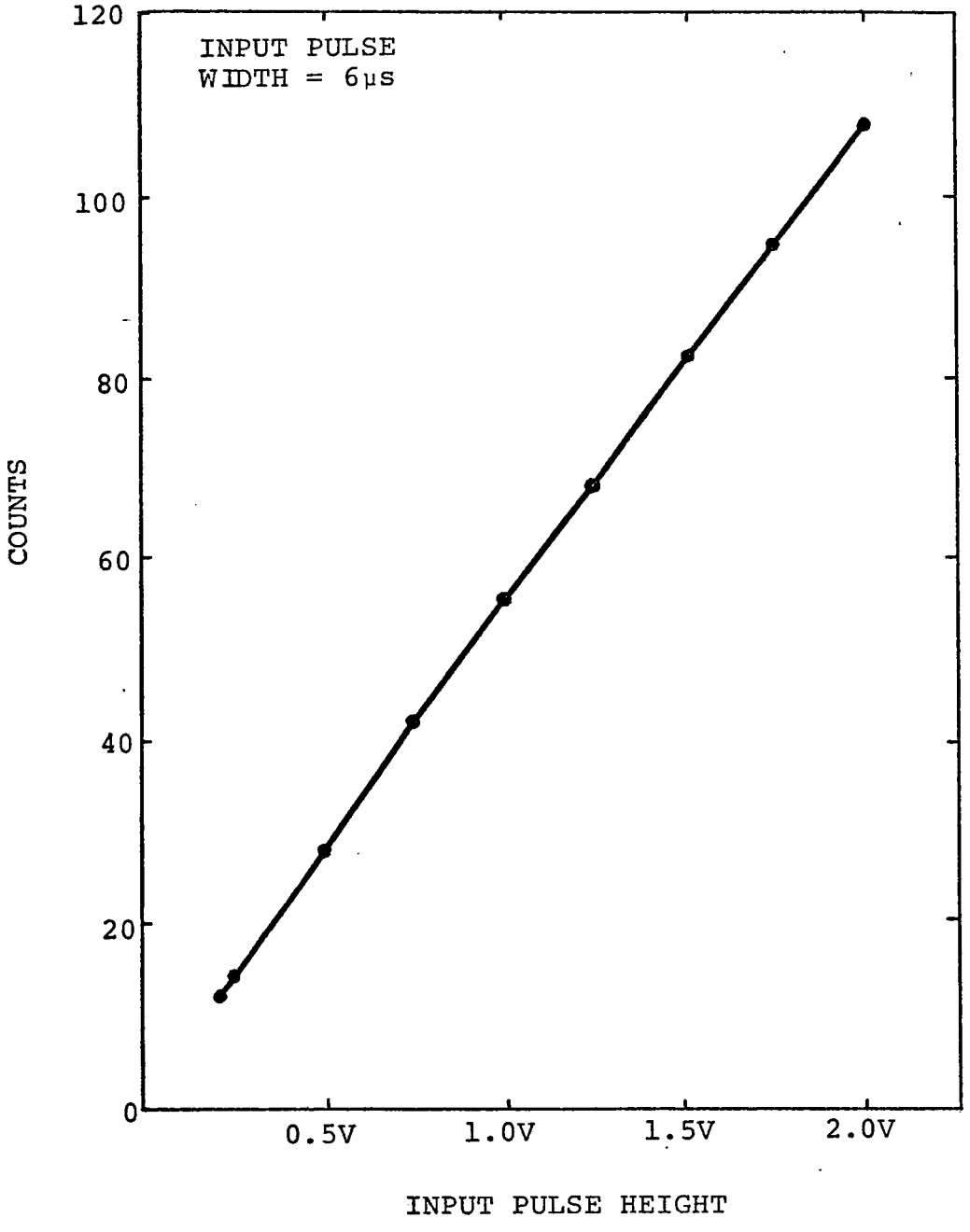


Fig. 2-5B THE LINEARITY OF PHDC

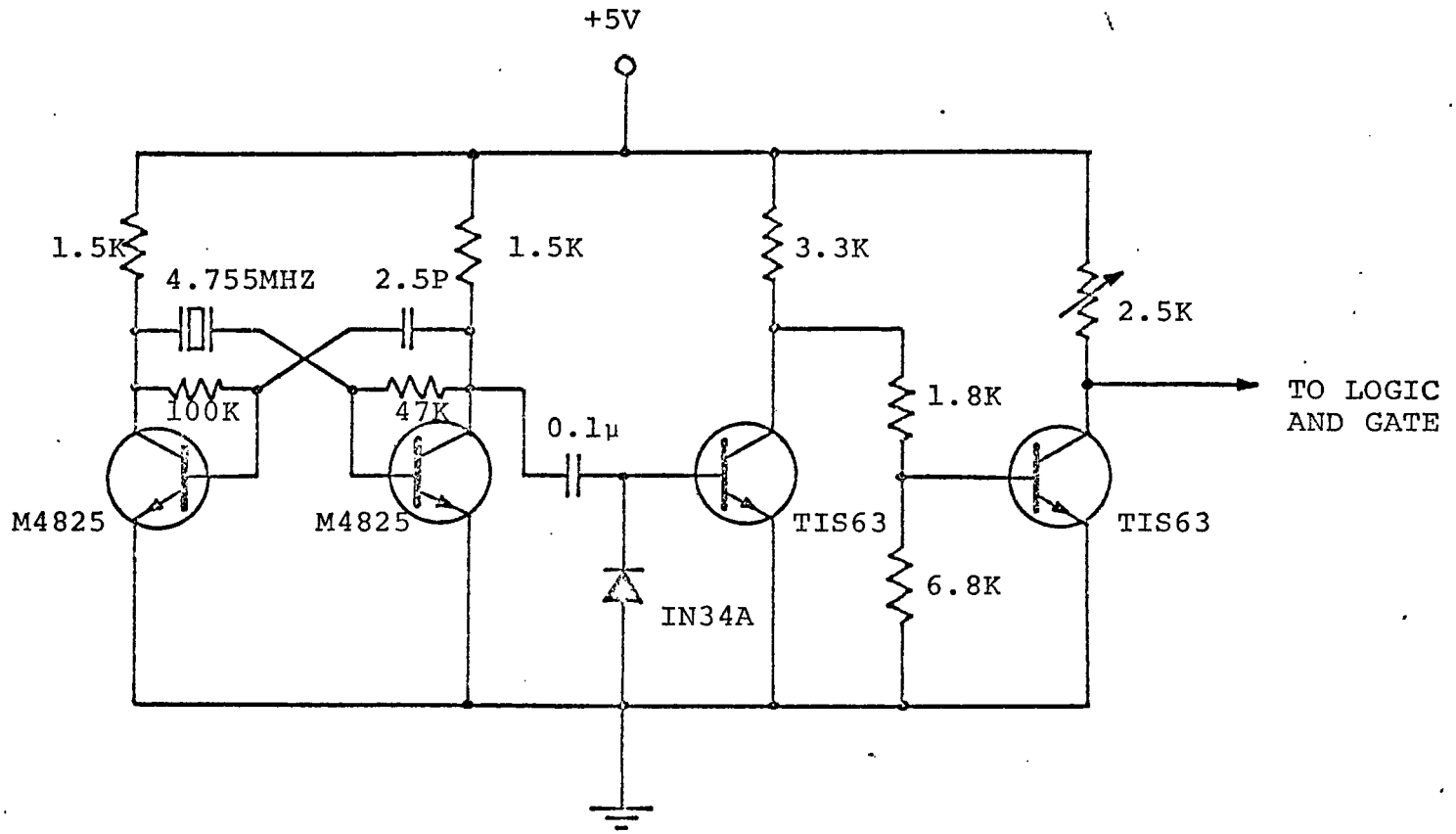


Fig. 2-6 CLOCK PULSE GENERATOR

crystal-control multivibrator whose frequency is 4.755 MHz. To improve the clock pulse a squaring Schmitt trigger circuit is used.

Counter, Data and Monitor Driver (Fig. 2-7)

The output gate of PHWC enables the logic AND gates G_1 and G_2, and allows the clock pulses (Fig. 2-2H) to be applied to an 7-bit binary counter composed of two integrated circuit 4-bit counters (A_1 and A_2). The digital information stored in the binary counter is transferred via the Data Driver stage to the computer input stage. The Data Driver circuits translate the digital levels of the PHDC (Logic 1 = +5v, Logic 0 = 0v) to those of the computer input stage (Logic 1 = -4v, Logic 0 = 0v). The Monitor Driver provides visual indication of data pulse by 8 pilot lamps with one pilot lamp indicating overflow of the 7-bit counter.

Pulse Generators

Three monostable-multivibrators (Fig. 2-8A, B, and C) generate trigger pulses for the Linear Gate FF, sync. pulses for the computer Data-loading process, and reset pulses for Binary Counter and Linear Gate FF. Reset pulses are obtained by triggering the Reset Pulse Generator with a manual switch or external pulses from the computer. Reset pulses to the Linear Gate FF which requires negative-going pulses are

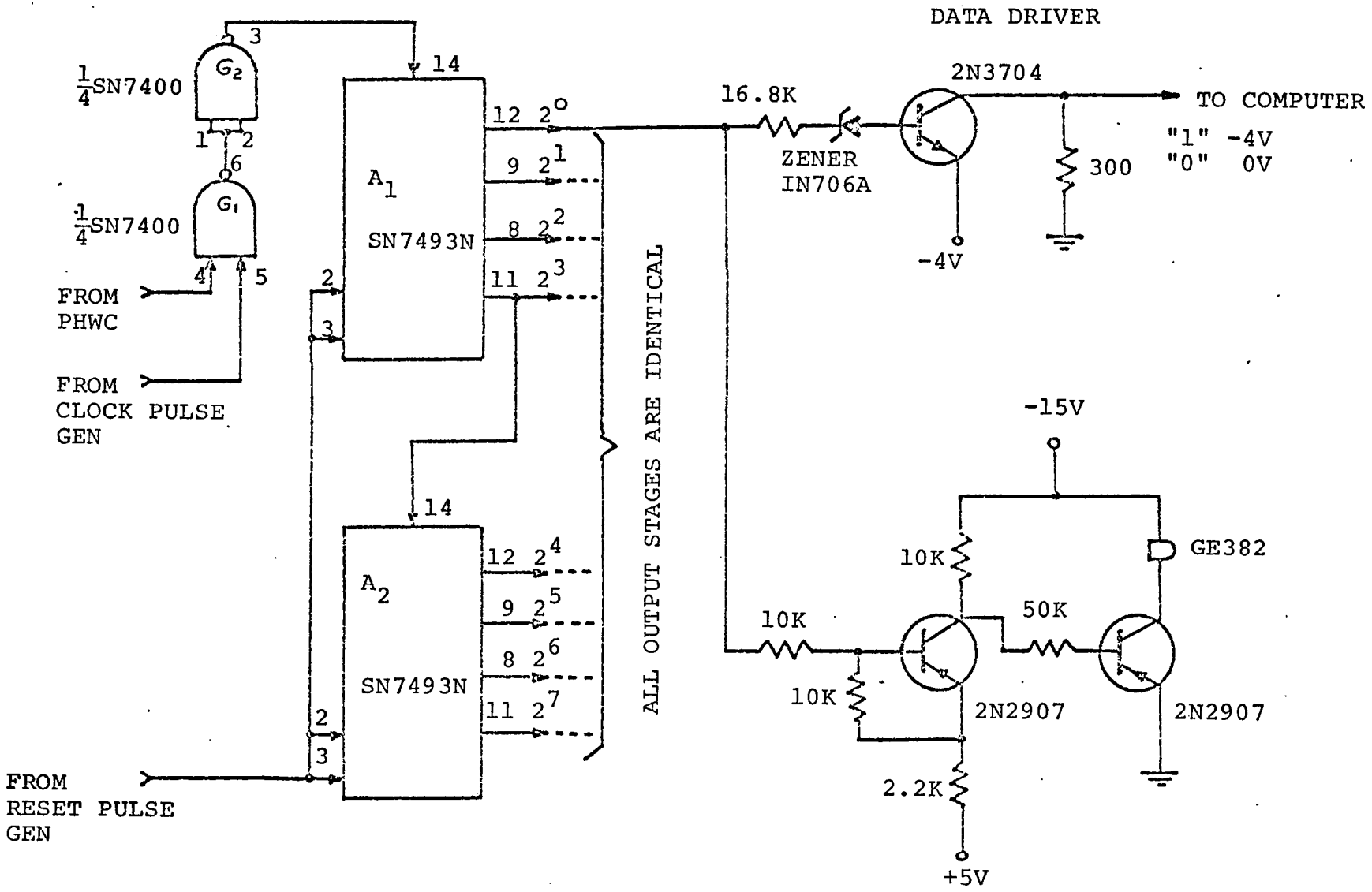


Fig. 2-7 LOGIC AND GATE, COUNTER, DATA AND MONITOR DRIVER

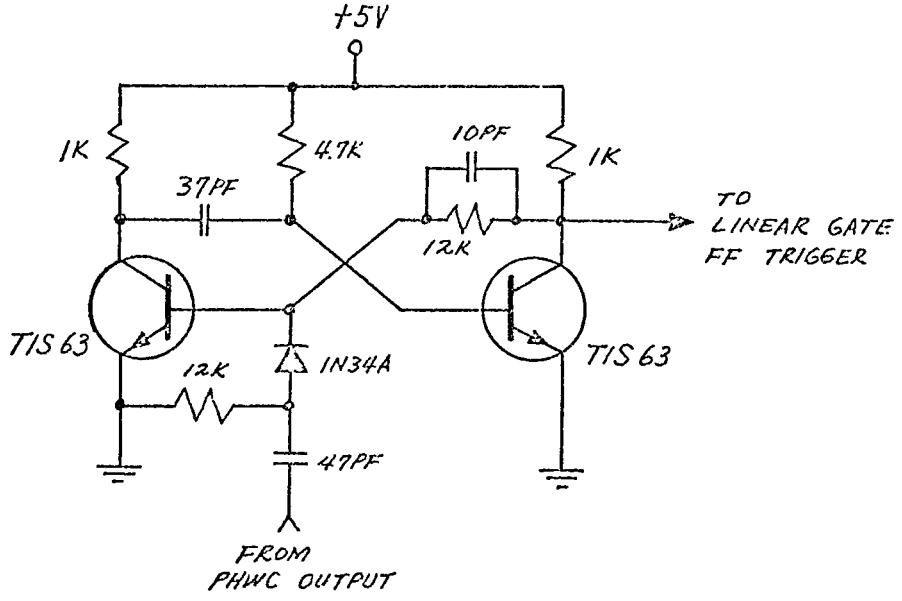


Fig. 2-8A TRIGGER PULSE GENERATOR

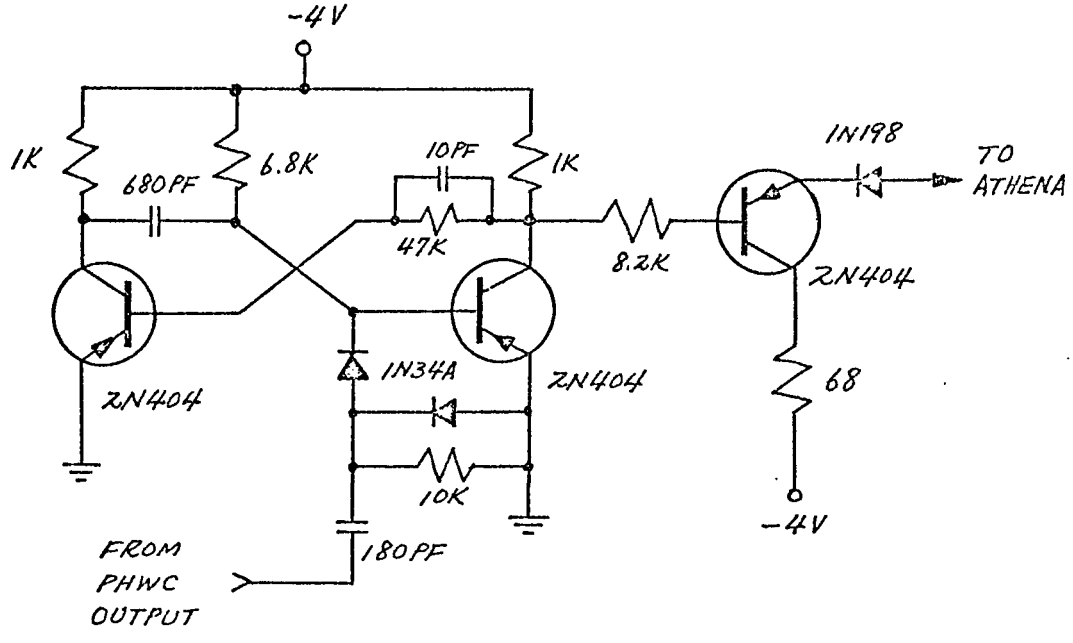


Fig. 2-8B SYNC PULSE GENERATOR

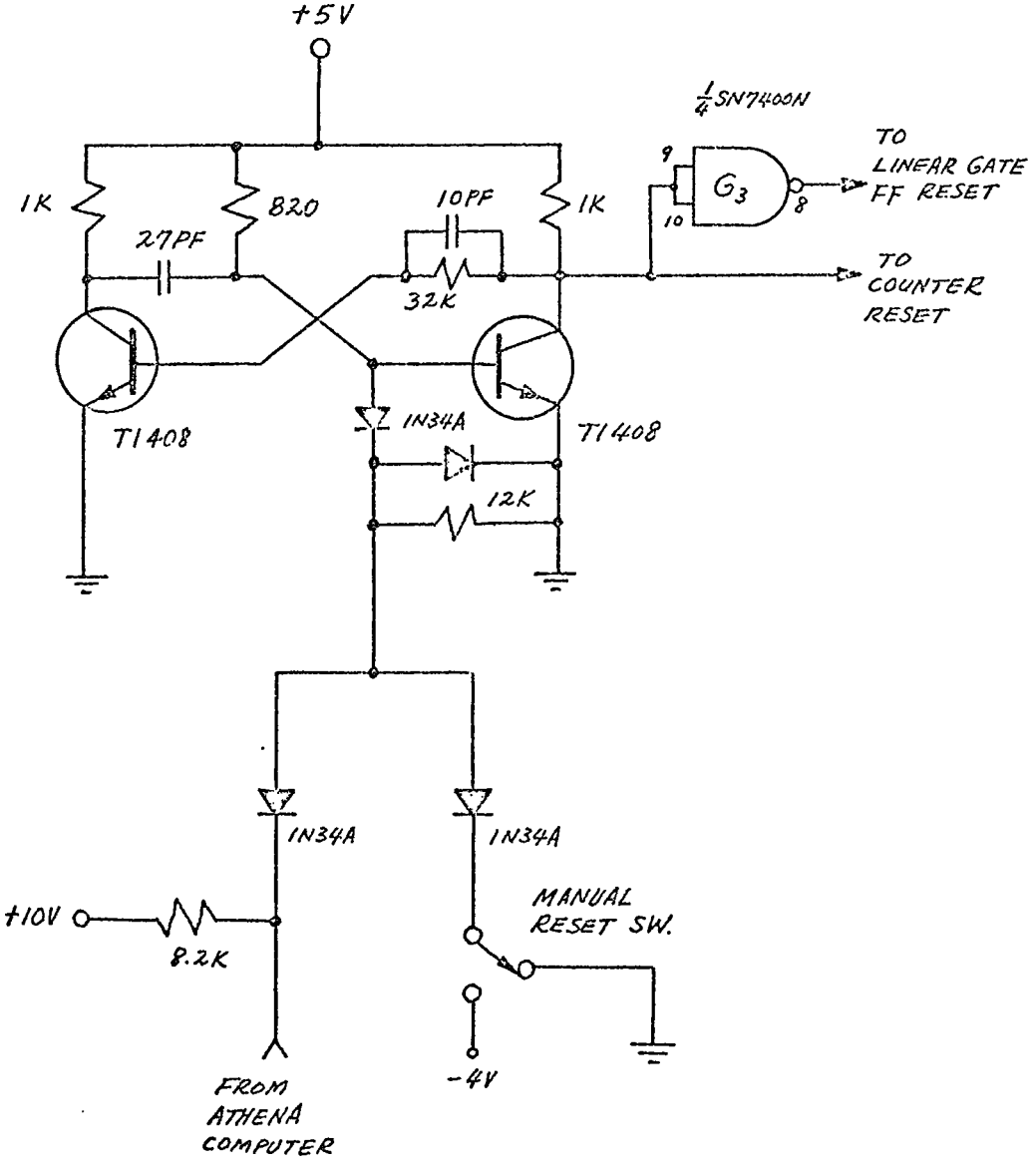


Fig. 2-8C RESET PULSE GENERATOR

inverted by a NAND gate (Fig. 2-8C).

Digital-to-Analog Converter

A digital-to-analog converter (DAC) consists essentially of two parts: the actual decoding unit which is usually a high-output-impedance low current device and a high-gain summing amplifier with a low-output-impedance. The resistor-ladder type decoder was chosen because of the simplicity of the circuit. An IC operational amplifier (μA709) is used as the summing amplifier (Fig. 2-9, 10). The relationship between output and input of the circuit of Fig. 2-9 is given by

$$V_{0A} = -\frac{R_f}{R}\left[\frac{V_R(2^5)}{2} + \frac{V_R(2^4)}{4} + \frac{V_R(2^3)}{8} + \frac{V_R(2^2)}{16} + \frac{V_R(2^1)}{32} + \frac{V_R(2^0)}{64}\right]$$

for 6-bit decoder where R_f is the feedback resistor of Op.Amp. and R is the decoder resistor. For data read-out two DAC's are provided; DAC_Y (Fig. 2-9) for the accumulated digital information in the magnetic core storage and DAC_X (Fig. 2-10) for the addressing digital information in the index register. The input stage of DAC_Y consists of 6-bit decoder instead of 24-bit since 6 bits yield sufficient accuracy for display on the oscilloscope. Therefore a

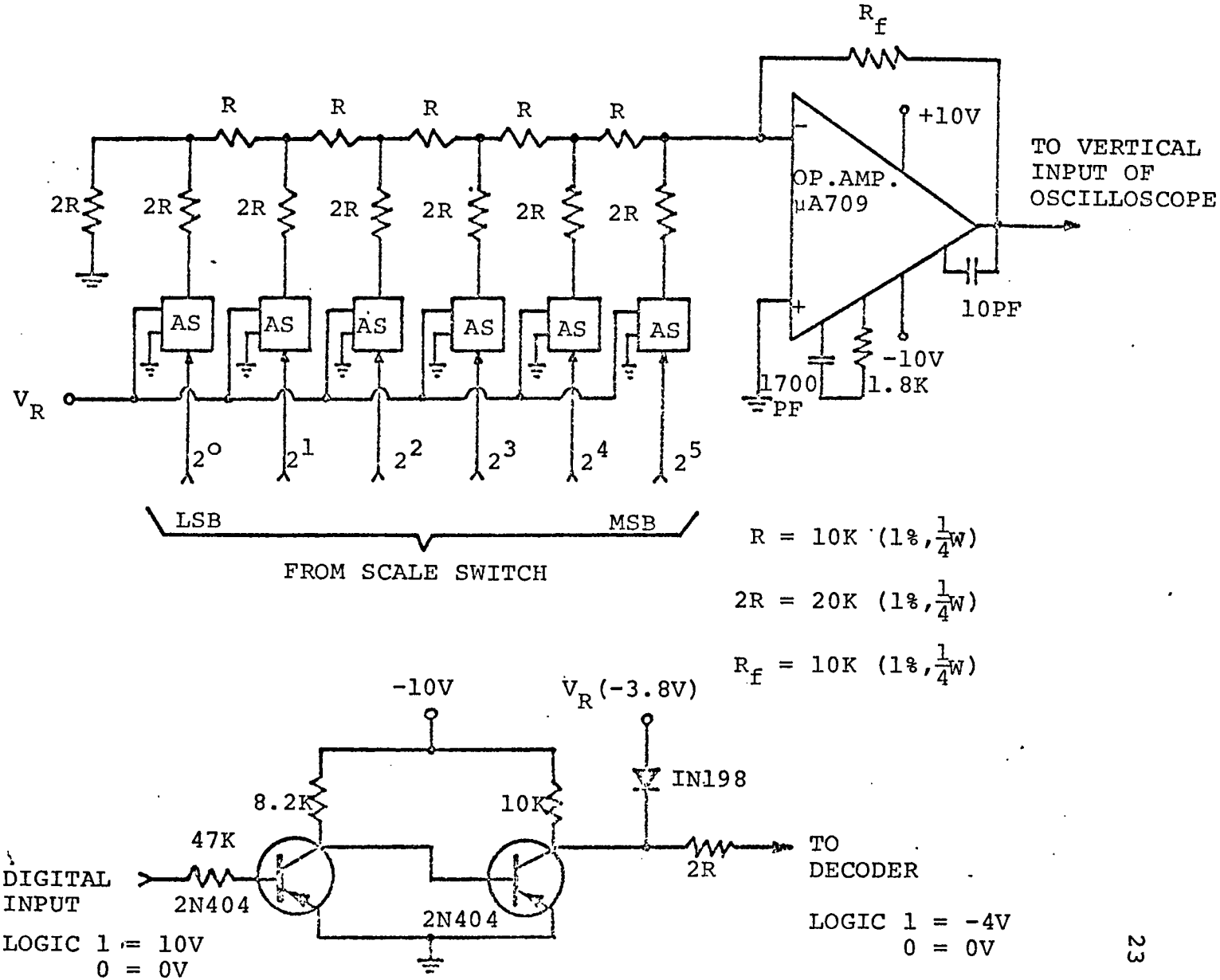


Fig. 2-9 DAC_Y (DIGITAL-TO-ANALOG CONVERTER)

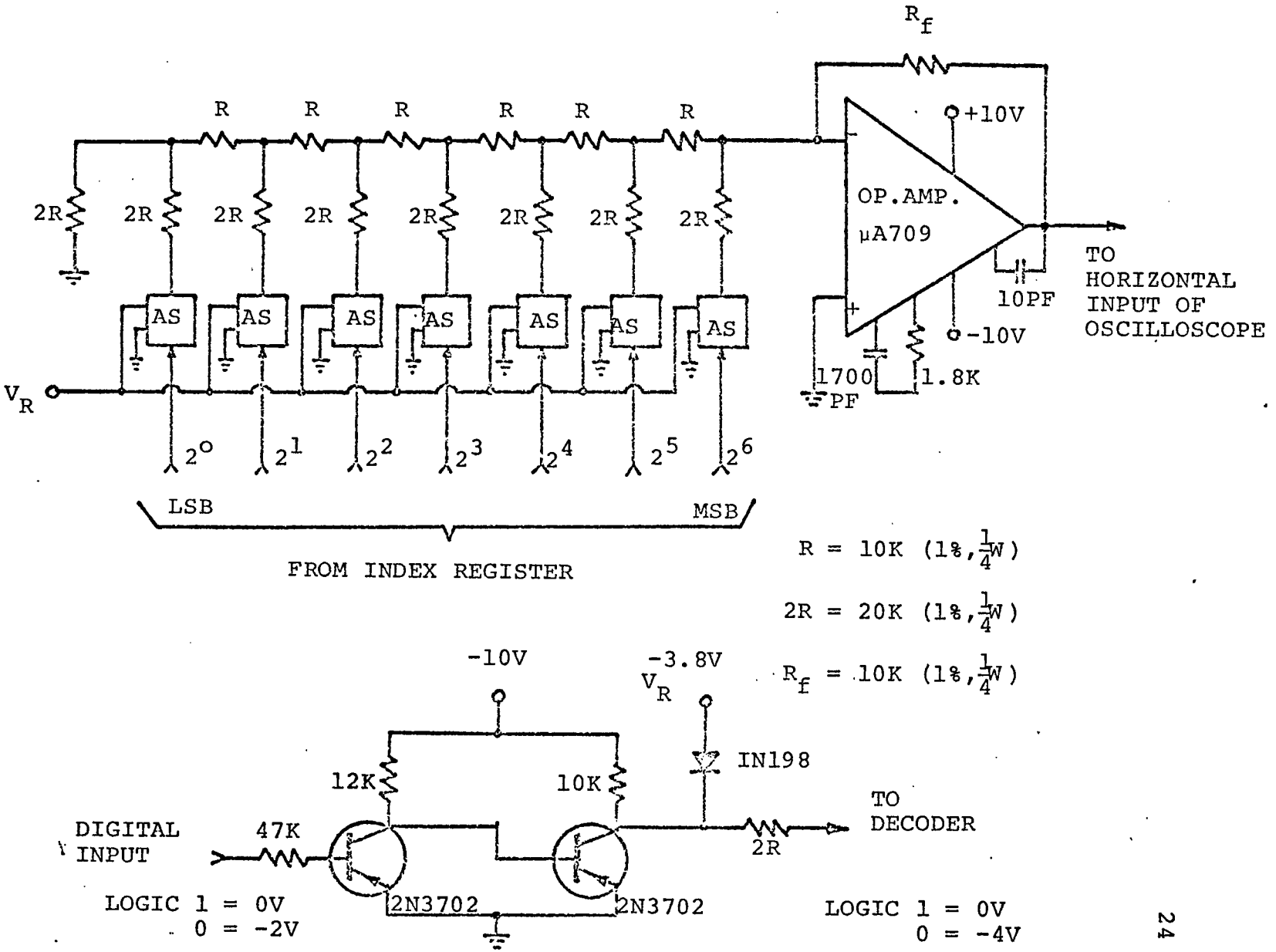
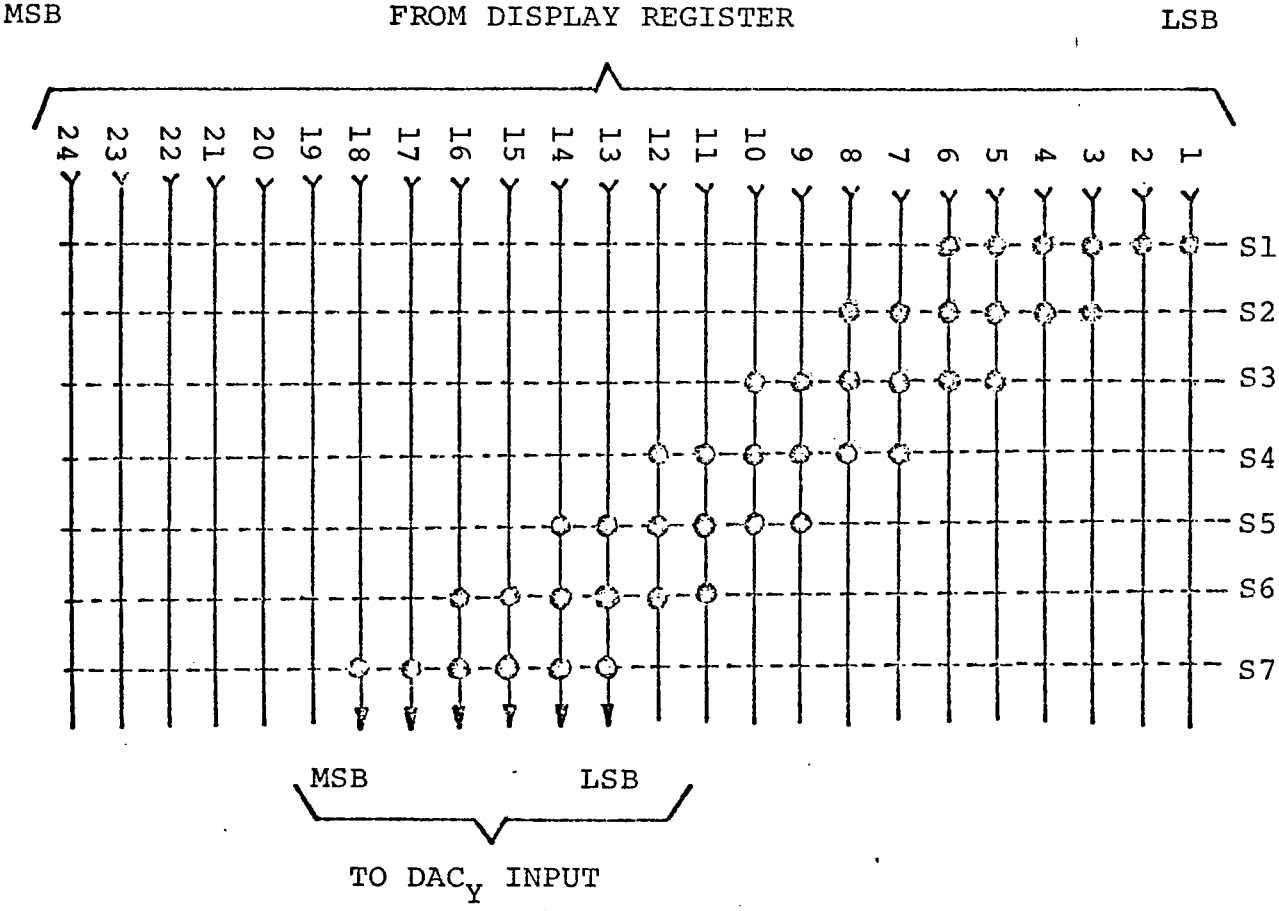


Fig. 2-10 DAC_x (DIGITAL-TO-ANALOG CONVERTER)

scale switch is arranged, which selects a 6-bit group and thus the scale of the vertical axis. As the analog switch two silicon PNP transistors are used for each bit. The scale switch is shown in Fig. 2-11.



SWITCH POSITION	SCALE LSB	RANGE MSB	FULL SCALE (+4V)
S1	1	32	63
S2	4	128	252
S3	16	512	1008
S4	64	2048	4032
S5	256	8192	16128
S6	1024	32768	64512
S7	4096	131072	258048

Fig. 2-11 SCALE SWITCH

CHAPTER III

MODIFICATION TO ATHENA AND PROGRAMMING

The functional diagram of the Athena Computer[1] is shown in Fig. 3-1. The Athena Computer has a special operational code, Coefficient Jump (CJ), which provides means of selecting particular programs stored on the drum storage. A specific program stored in a given sector of drum groups four, five, and six (Fig. 3-2) can be selected by the Program Selecting pushbutton with this instruction. Each sector address is a 2-bit binary number while each magnetic drum group address is a 3-bit binary number. The program selecting pushbuttons introduce into the Program Address Register (PAR) a 4-bit binary number which selects the drum group and sector address of a given sector. The most significant bit of the 5-bit binary number drum addresses for drum groups four, five, and six is always a "1". This bit is entered into the PAR from the CJ instruction during program operation. The remote data-process diagram is shown in Fig. 3-3.

There are three data-process programs which are pre-loaded in the given sectors of magnetic drum storage. Those are as follows:

(1) Clear magnetic core storage where data

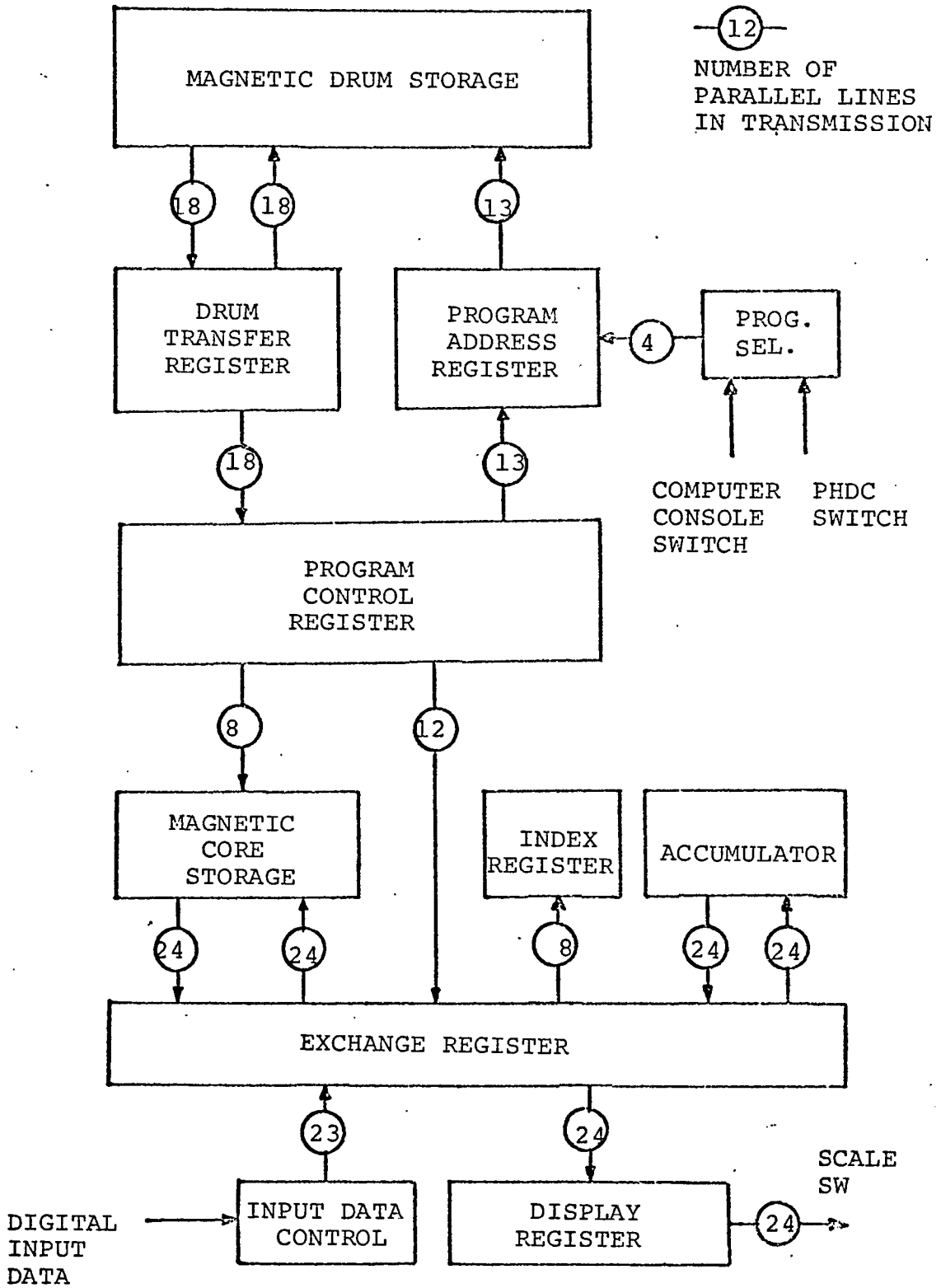


Fig. 3-1 BLOCK DIAGRAM OF ATHENA

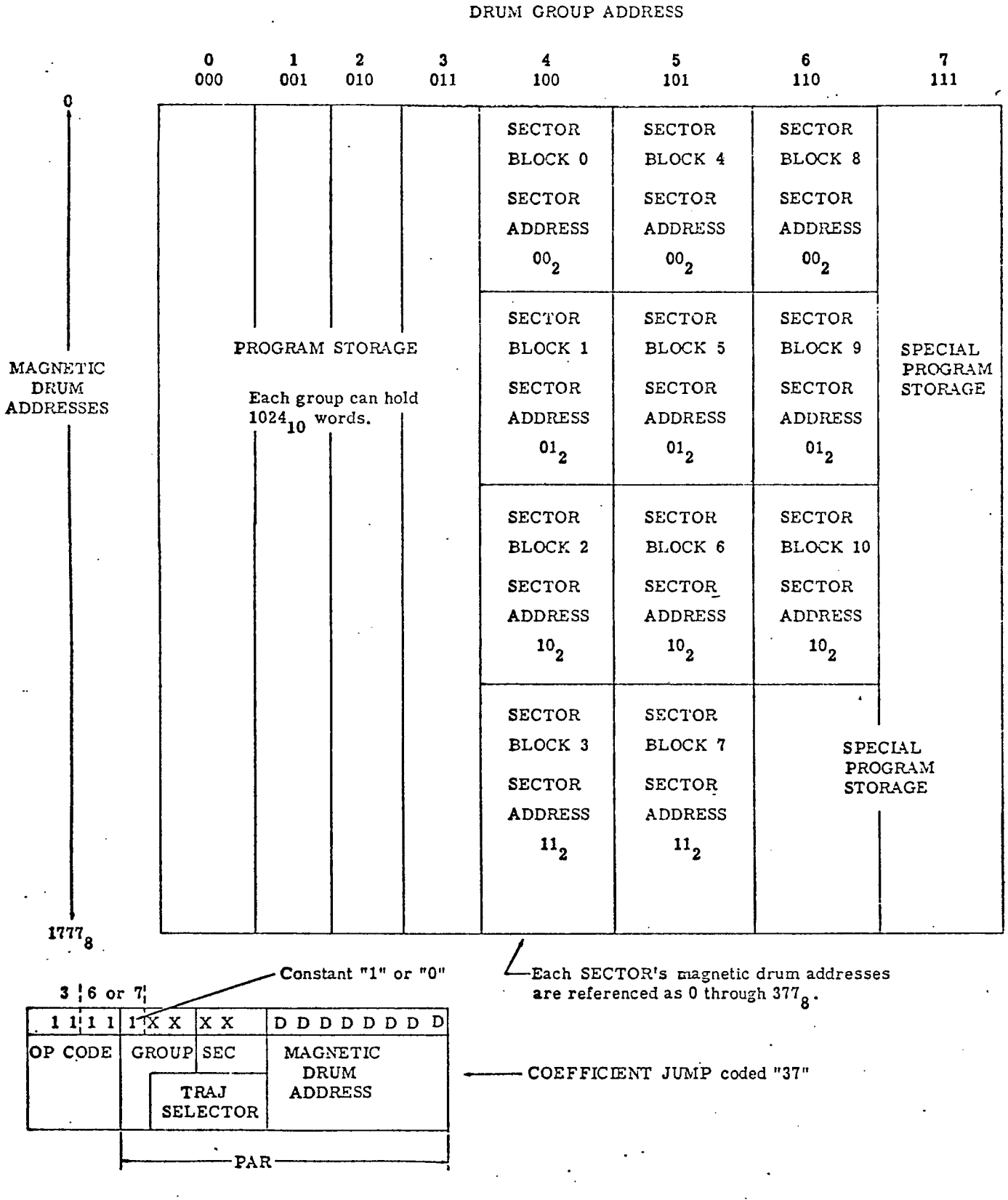


Fig. 3-2 MAP OF MAGNETIC DRUM STORAGE

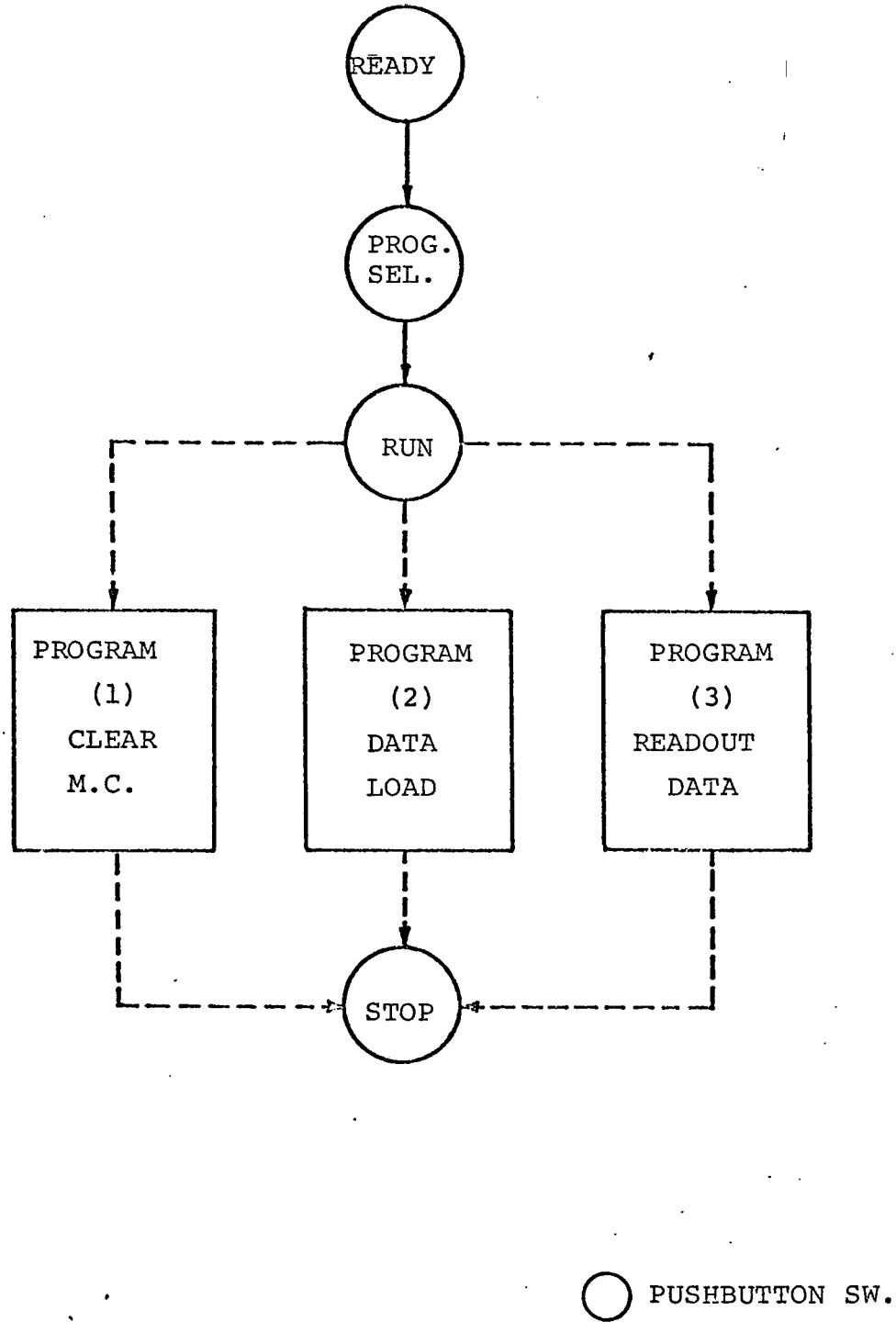


Fig. 3-3 REMOTE CONTROL MODE

to be stored. (Flow diagram in Fig. 3-4A)

(2) Add 1 to the core address given by the digitized pulse height information from the PHDC. (Flow diagram in Fig. 3-4B)

(3) Cycle through the core address and read the contents of each address. (Flow diagram in Fig. 3-4C)

During the data-loading program (2) operation the Wait Partial (WP) instruction is used to slave the computer to the PHDC. When this instruction is decoded, the computer will be stopped by inhibiting the Main Pulse Distributor (MPD). When a Partial Sync Pulse is received from the PHDC, the MPD is enabled again to issue main pulses, and the computer continues. During the first cycle of the data-loading program, operation the WP instruction will be decoded. This applies the output of the WP logic circuits (Fig. 2-2A) to the Reset Pulse Generator (RPG) of the PHDC. Then the reset pulse from the RPG clears the Binary Counter, and opens the Linear Gate to receive an input data pulse. At the trailing-edge of the data pulse a partial sync pulse (Fig. 2-2J) is generated by the Sync Pulse Generator of the PHDC which releases the computer from the stop state. This

*;INDEXING

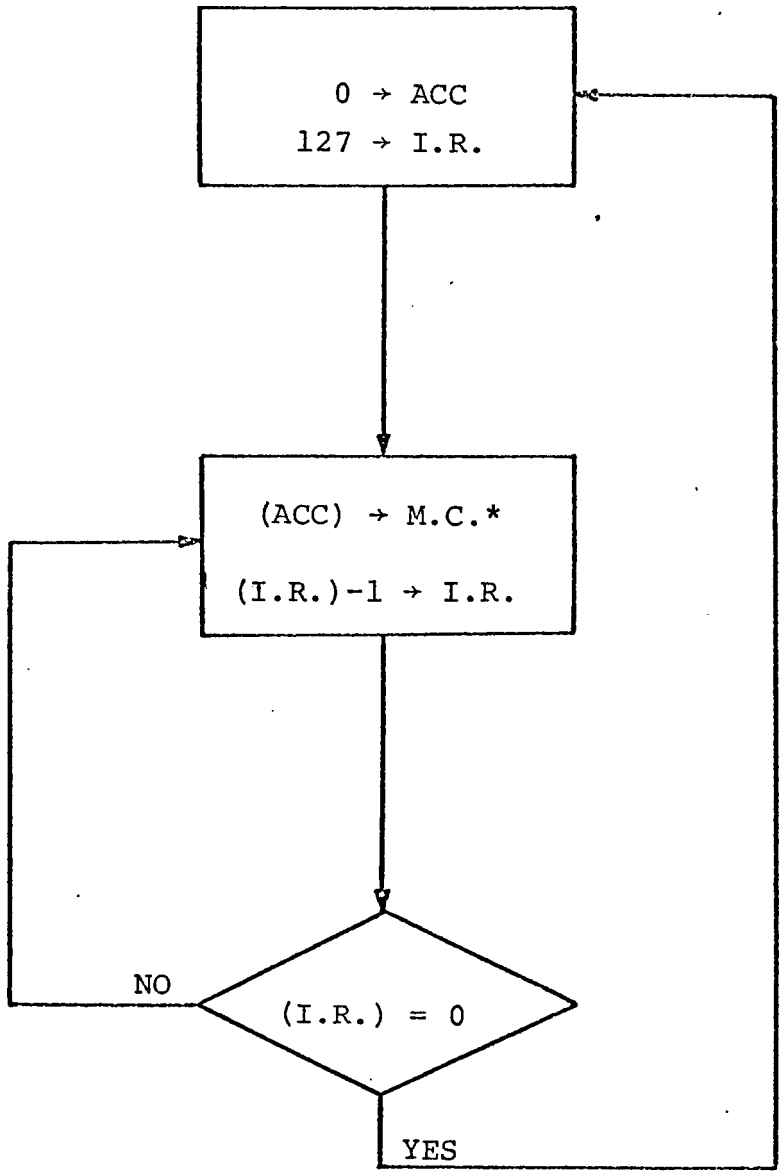


Fig. 3-4A FLOW DIAGRAM OF CLEAR M.C.

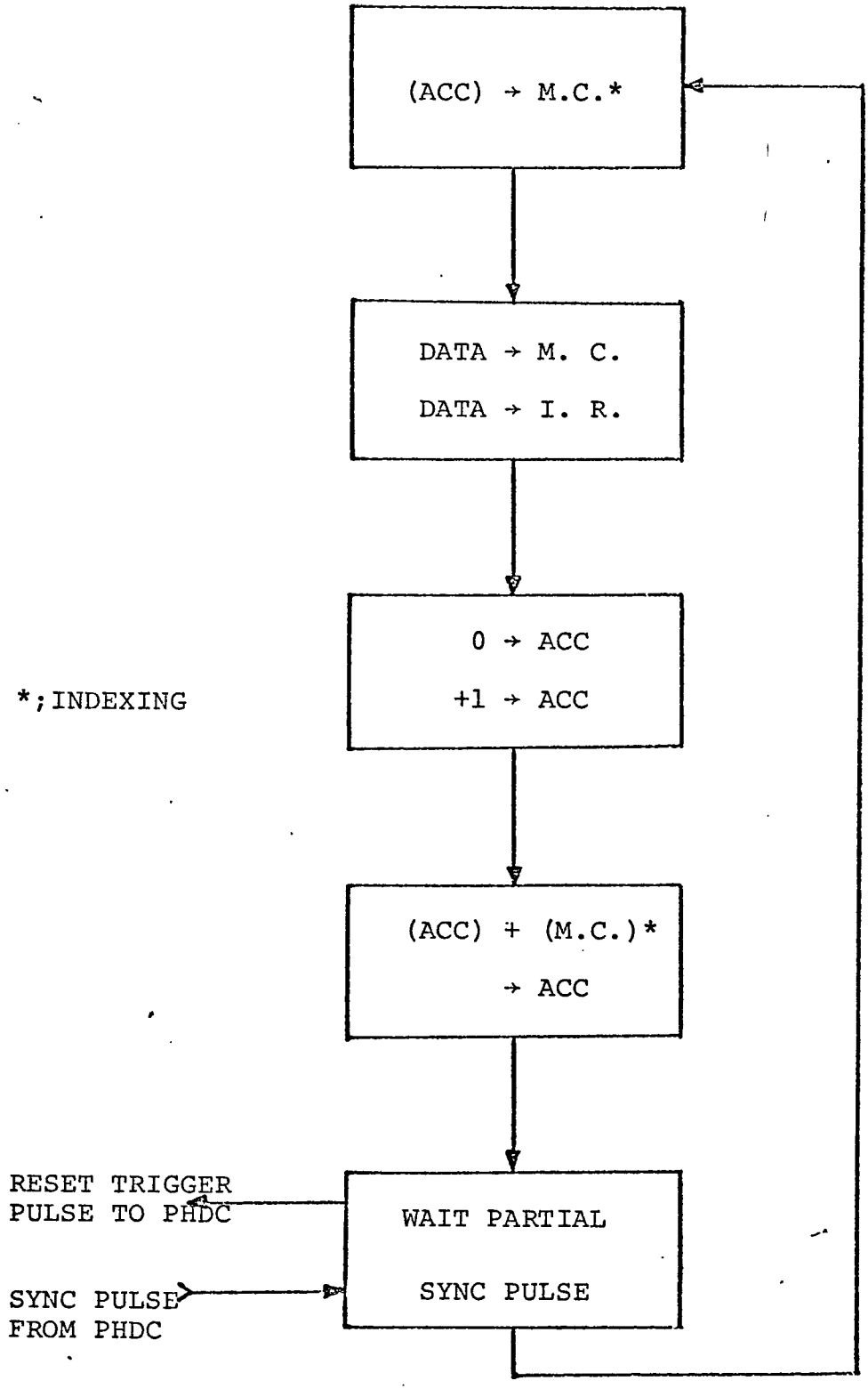


Fig. 3-4B FLOW DIAGRAM OF DATA LOAD

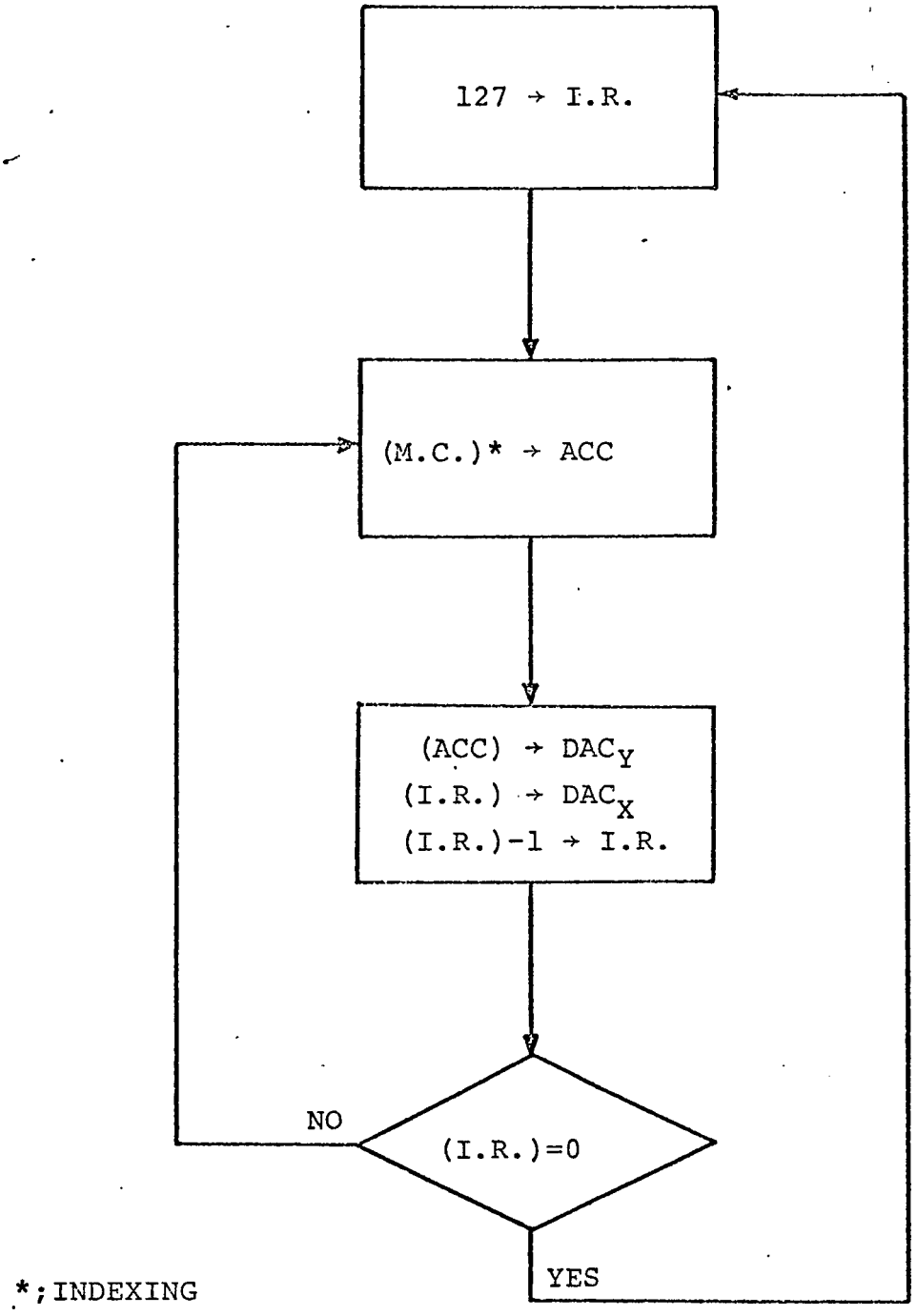


Fig. 3-4C FLOW DIAGRAM OF READOUT DATA

allows the data to be stored in a magnetic core address. The operation of data-loading program (Fig. 3-4B) is as follows:

(1) Transfer the contents of the Acc. (former input data information) to the core address given by the contents of Index Register.

(2) Transfer the digitized input data from the PHDC to a certain core address except the reserved ones. (for temporary storage) Load the certain address data into the Index Register.

(3) Clear the contents of Acc. and load +1 into the Acc.

(4) Add the contents of Acc. (+1) to the contents of the core address given by the contents of Index Register and place the results in the Acc.

(5) WP instruction code is decoded. A reset trigger pulse is supplied to the PHDC and receive a sync pulse from the PHDC while an input data pulse is processing in the PHDC.

Only one data pulse can be processed during one cycle of the data-loading program.

The operation of clearing the magnetic core storage program (Fig. 3-4A) is as follows:

(1) Load zero into the Accumulator.

(2) Load 127 (the number of reserved core addresses) into the Index Register.

(3) Transfer the contents (zero) of the Acc. to the magnetic core address given by the contents of Index Register. Decrement the contents of Index Register by one.

(4) If the contents of Index Register becomes zero, jump to the Step (1). If it is not, jump to the Step (3).

But the next cycles after the first one are redundant.

The operation of readout data program (Fig. 3-4C) is as follows:

(1) Load 127 (the number of reserved core addresses) into the Index Register.

(2) Transfer the contents of the core address given by the contents of the Index Register to the Acc.

(3) Transfer the contents of Acc. to the scale switch via the Display Register, and also the contents of Index Register to the DAC_X input stage. Decrement the contents of Index Register by one.

(4) If the contents of Index Register is zero, jump to the Step (1). If it is not, jump to the Step (2).

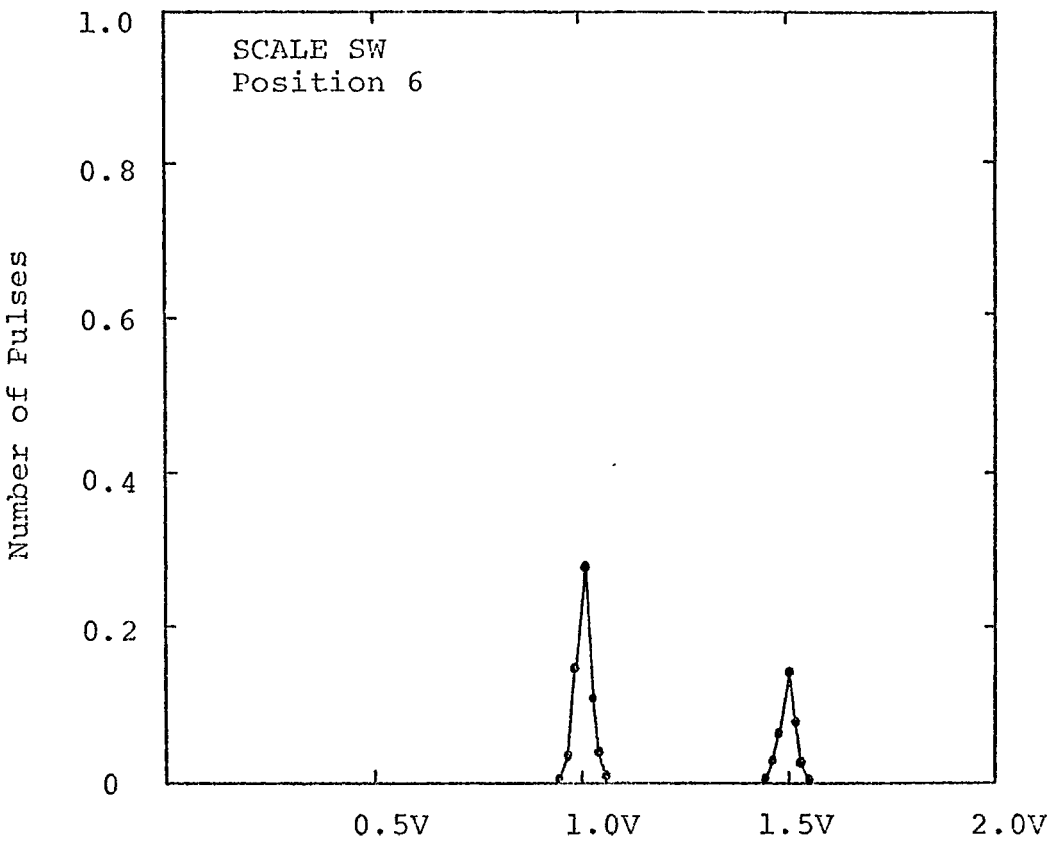
CHAPTER IV

RESULTS

The system was built and tested using a pulse generator with variable output as a source. Fig. 4-1 shows the pulse height distribution which is obtained by storing 1.0V data pulses for 100 seconds and 1.5V data pulses for 50 seconds with a pulse width of 10μs and pulse rate of 1000 PPS.

The maximum processing rate of the Athena Computer is about 500 PPS since the seven necessary data-loading instructions have a minimum execution time of 40μs each and the Wait Partial instruction has an execution time of 0 to 5ms depending on the occurrence of an input data pulse.

During the data processing it is possible for the turn on of the linear gate to coincide with the occurrence of an input pulse thus producing a pulse whose width is less than 2μs. In this case the pulse height is incorrectly digitized. However, the probability of this event is very small for random input data pulses at low rates.



Input Data Pulse

Height	1.0V, 1.5V
Width	10 μs
Rate	1000 PPS

Fig. 4-1 Number of Pulses vs Input Data Pulse Height

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APPENDIX A

Circuit Diagrams

For

The Pulse Height Analyzer

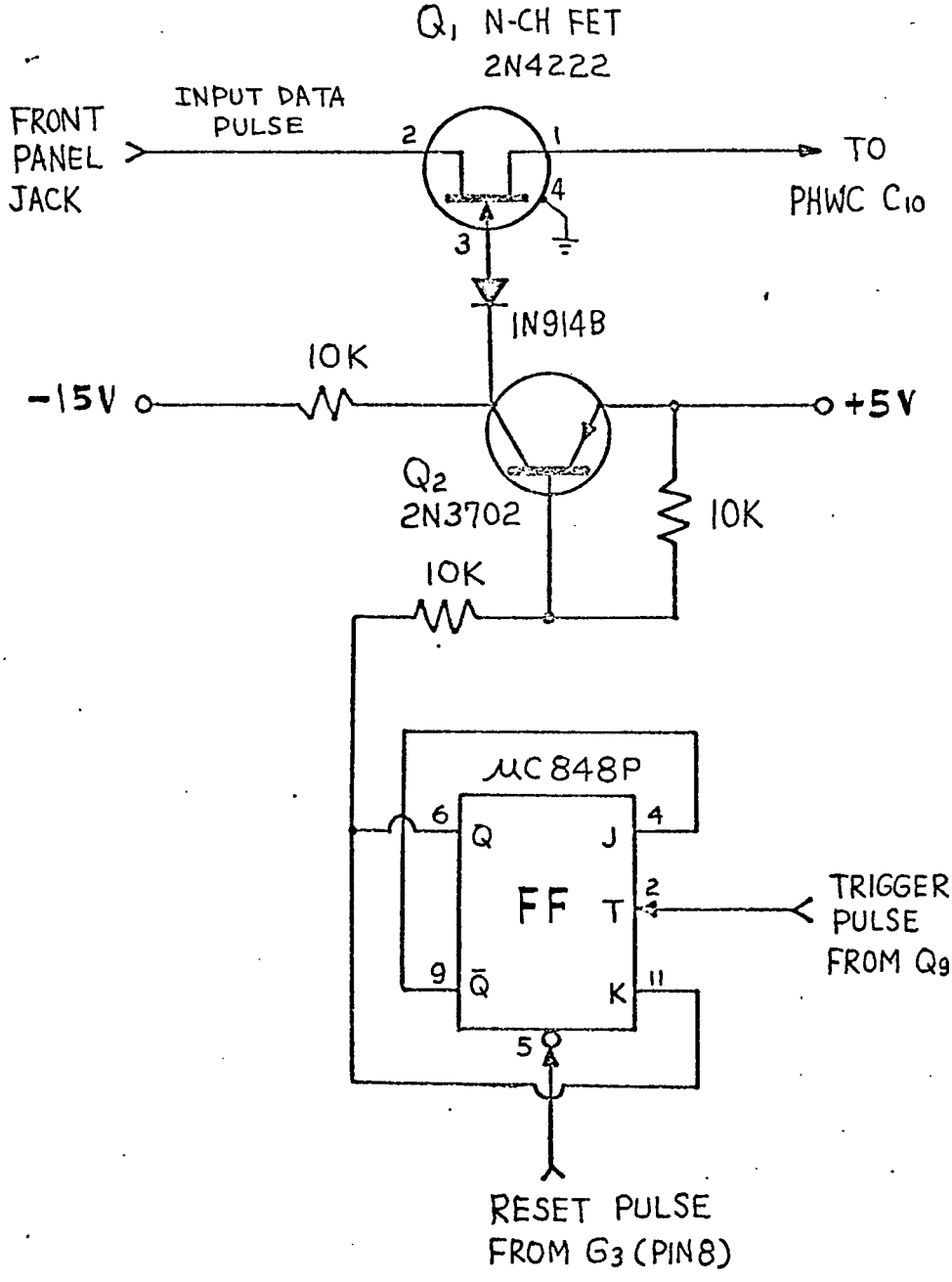


Fig. A-1 LINEAR GATE

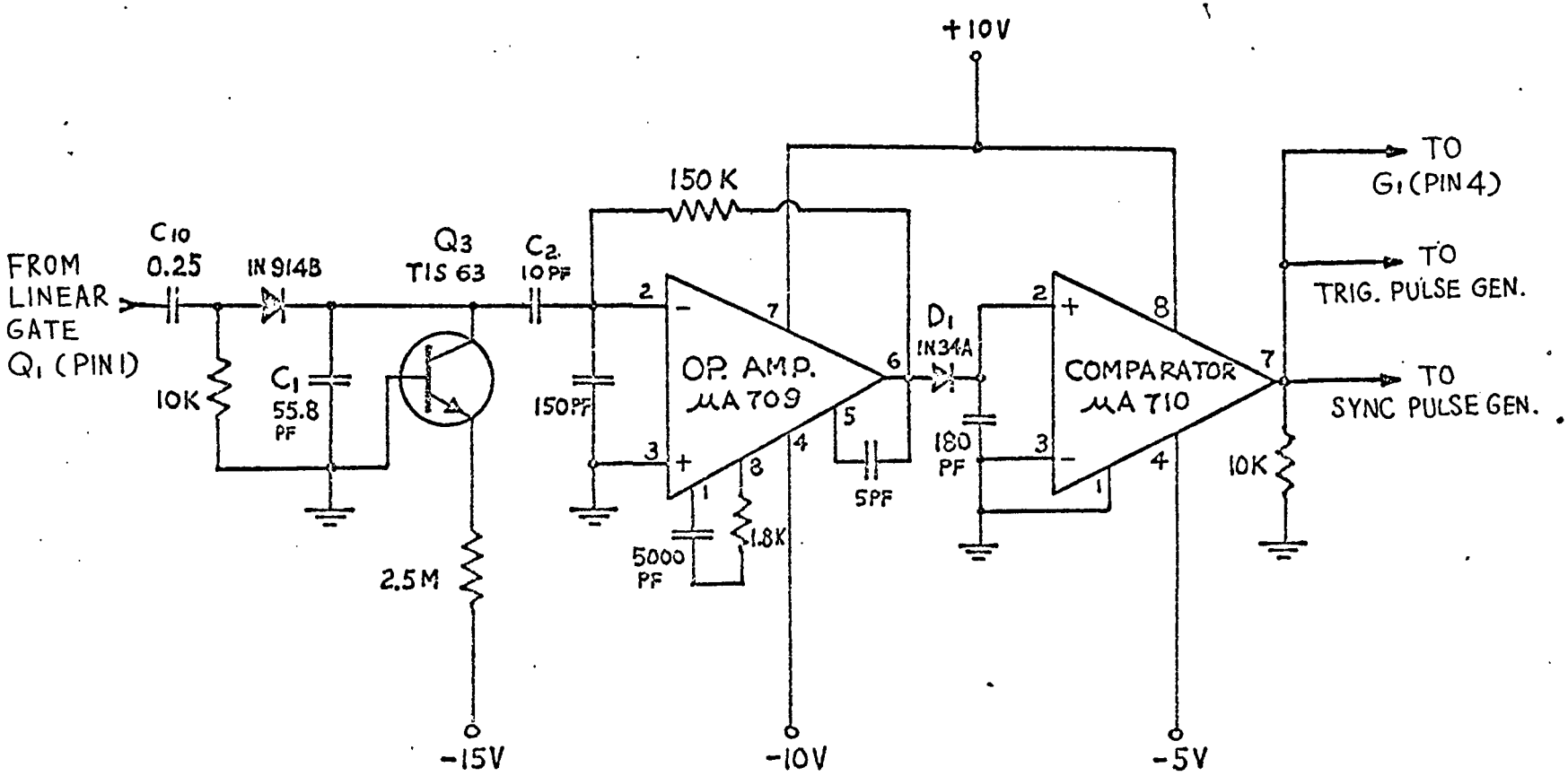

+10V
150 K
TO
G1 (PIN 4)
TO
TRIG. PULSE GEN.
TO
SYNC PULSE GEN.
FROM
LINEAR
GATE
Q1 (PIN 1)
C10
0.25
IN 914B
Q3
TIS 63
C2
10 PF
C1
55.8
PF
10K
2.5 M
150PF
OP. AMP.
μA 709
5PF
5000
PF
1.8K
D1
IN34A
180
PF
COMPARATOR
μA 710
10K
-15V
-10V
-5V

Fig. A-2 PHWC

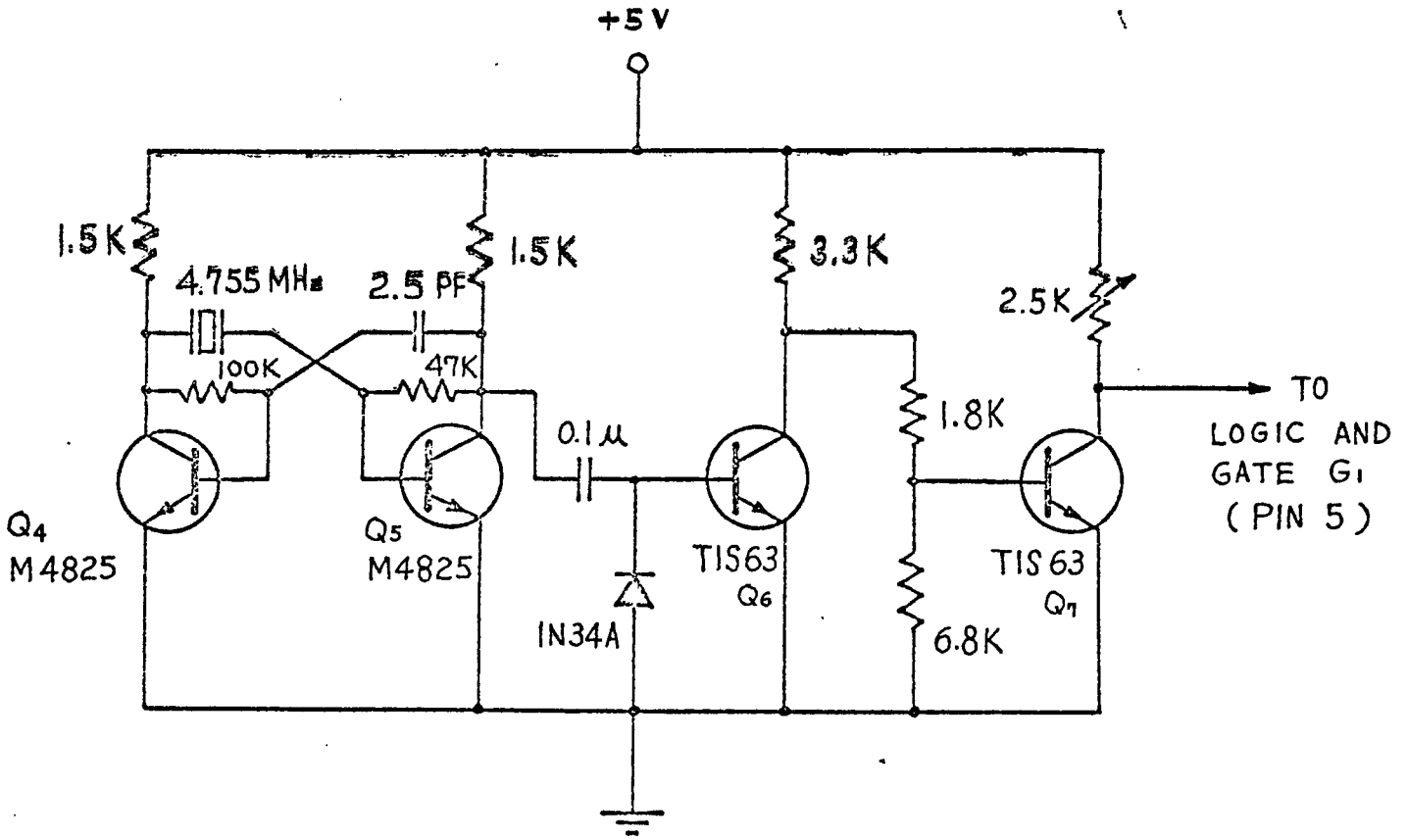


Fig. A-3 CLOCK PULSE GENERATOR

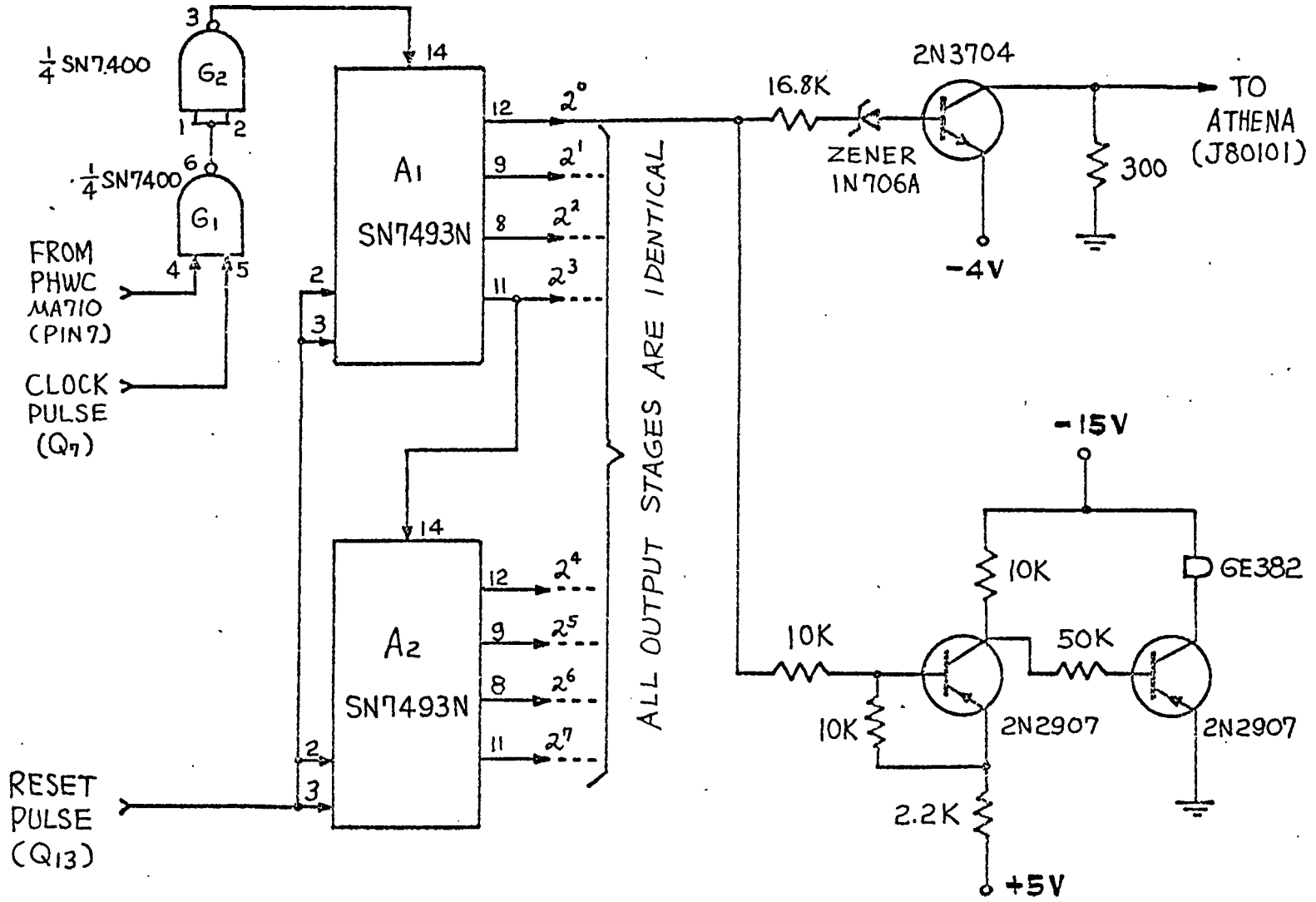


Fig. A-4 LOGIC AND GATE, COUNTER, DATA AND MONITOR DRIVER

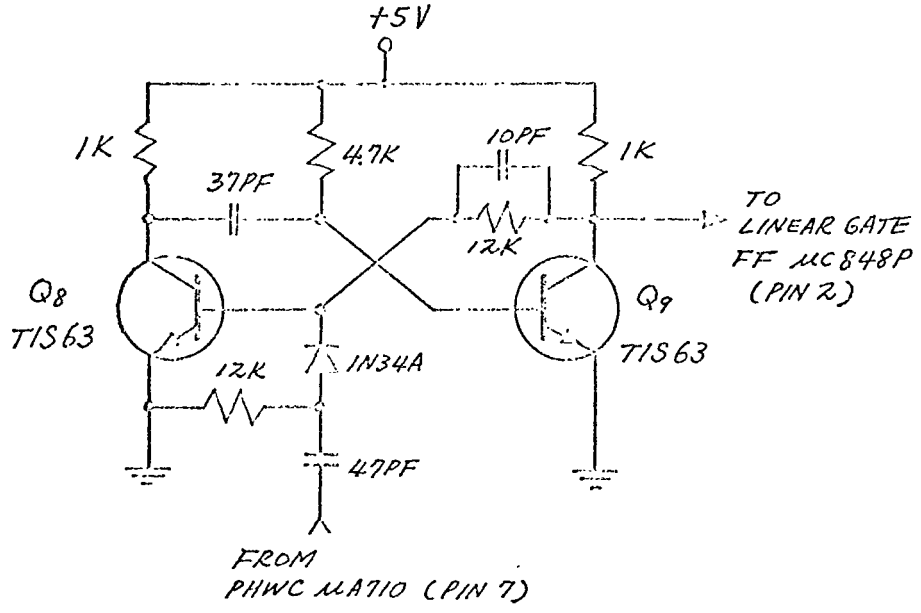


Fig. A-5A TRIGGER PULSE GENERATOR

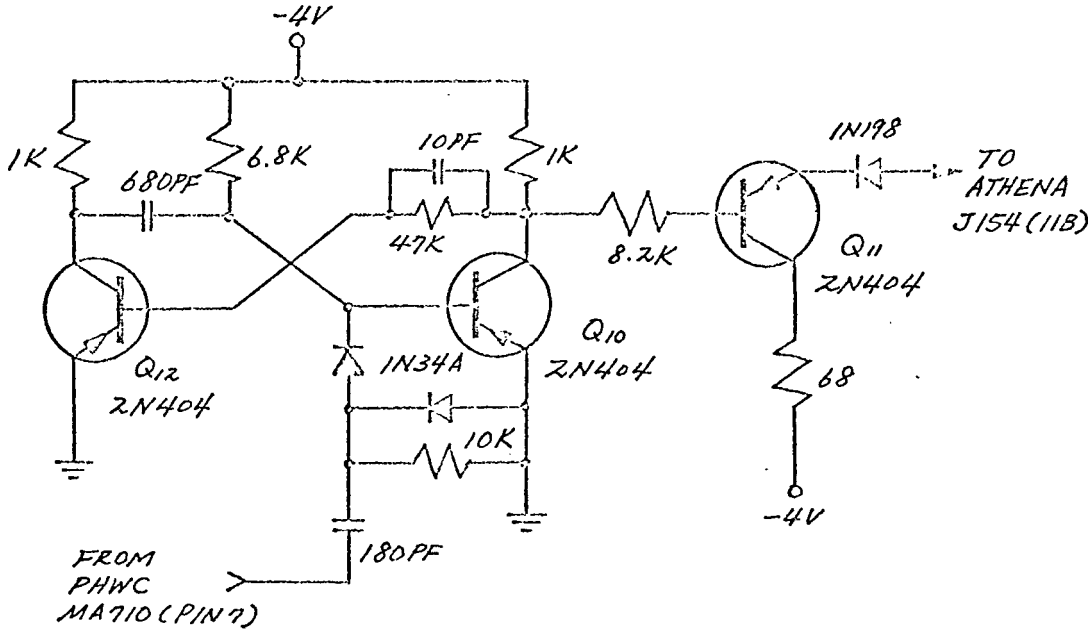


Fig. A-5B SYNC PULSE GENERATOR

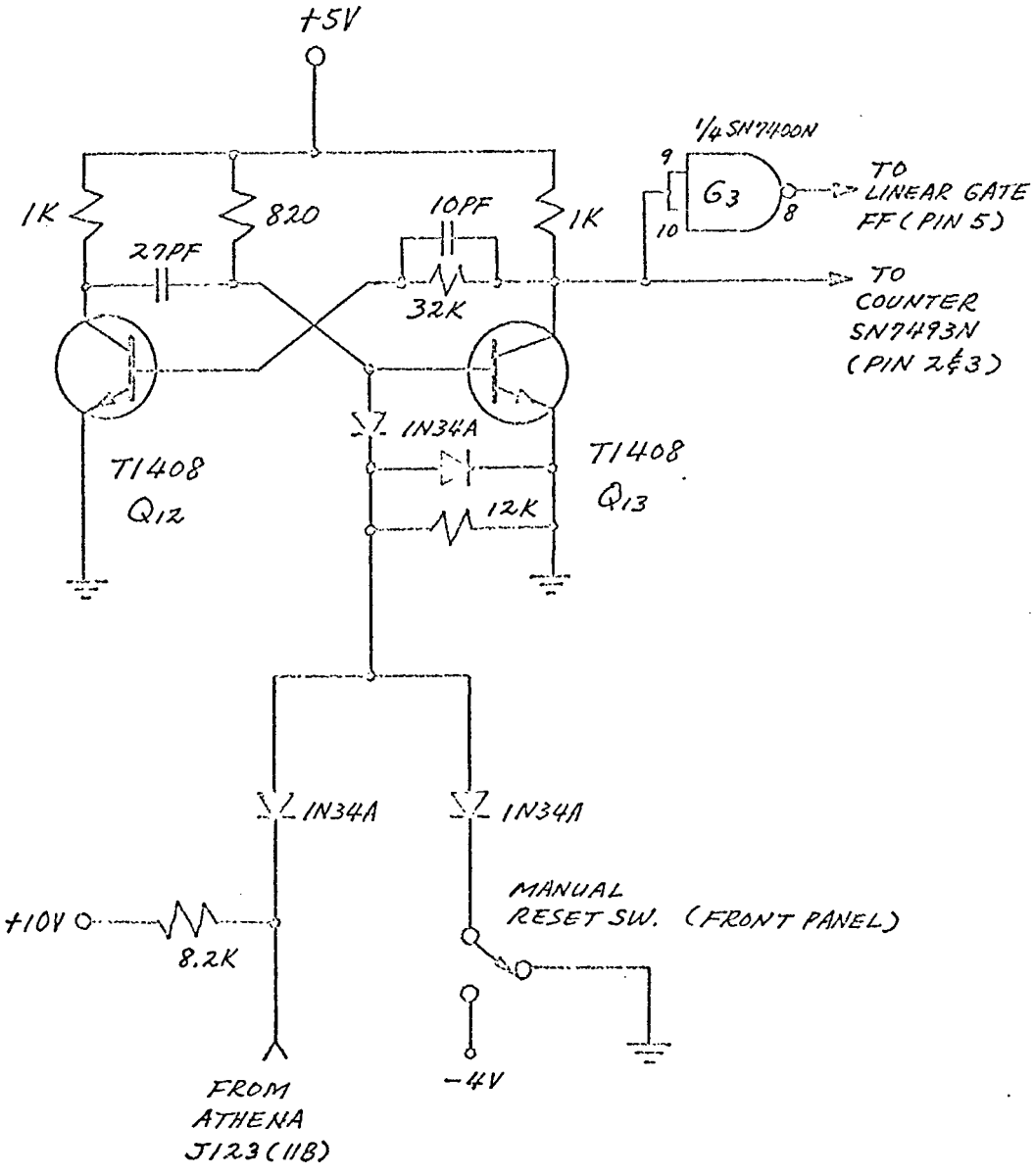
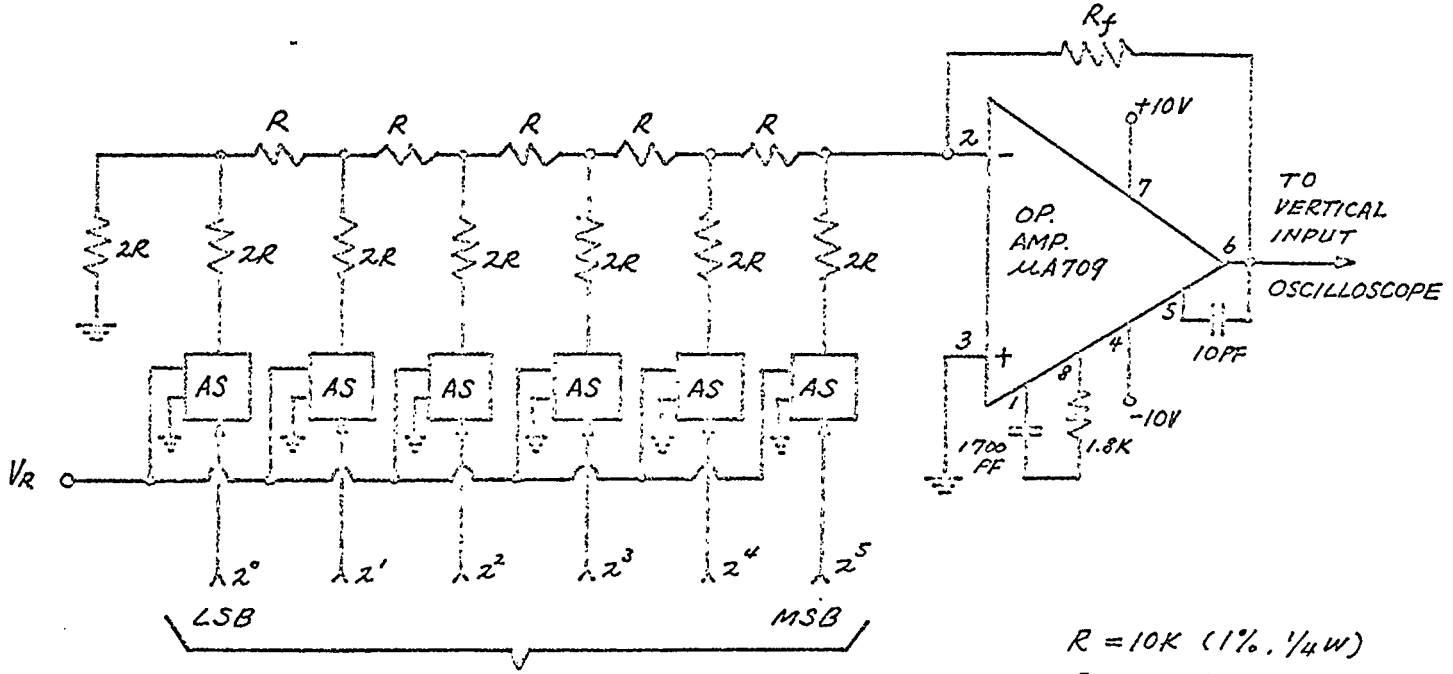


Fig. A-5C RESET PULSE GENERATOR


Rf
+10V
R
2R
AS
OP. AMP. μA709
TO VERTICAL INPUT
OSCILLOSCOPE
10PF
-10V
1700 PF
1.8K
VR
z°
z'
z²
z³
z⁴
z⁵
LSB
MSB
FROM SCALE SWITCH
R = 10K (1%, 1/4 W)
2R = 20K (1%, 1/4 W)
Rf = 10K (1%, 1/4 W)

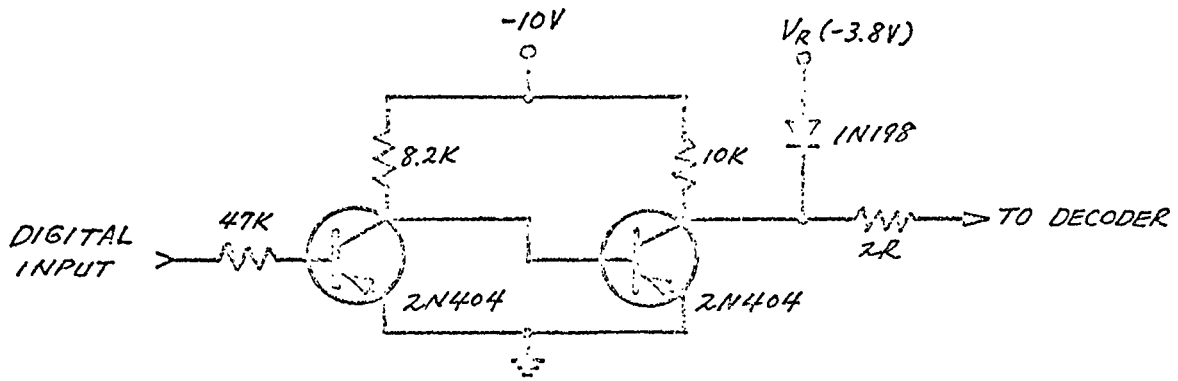
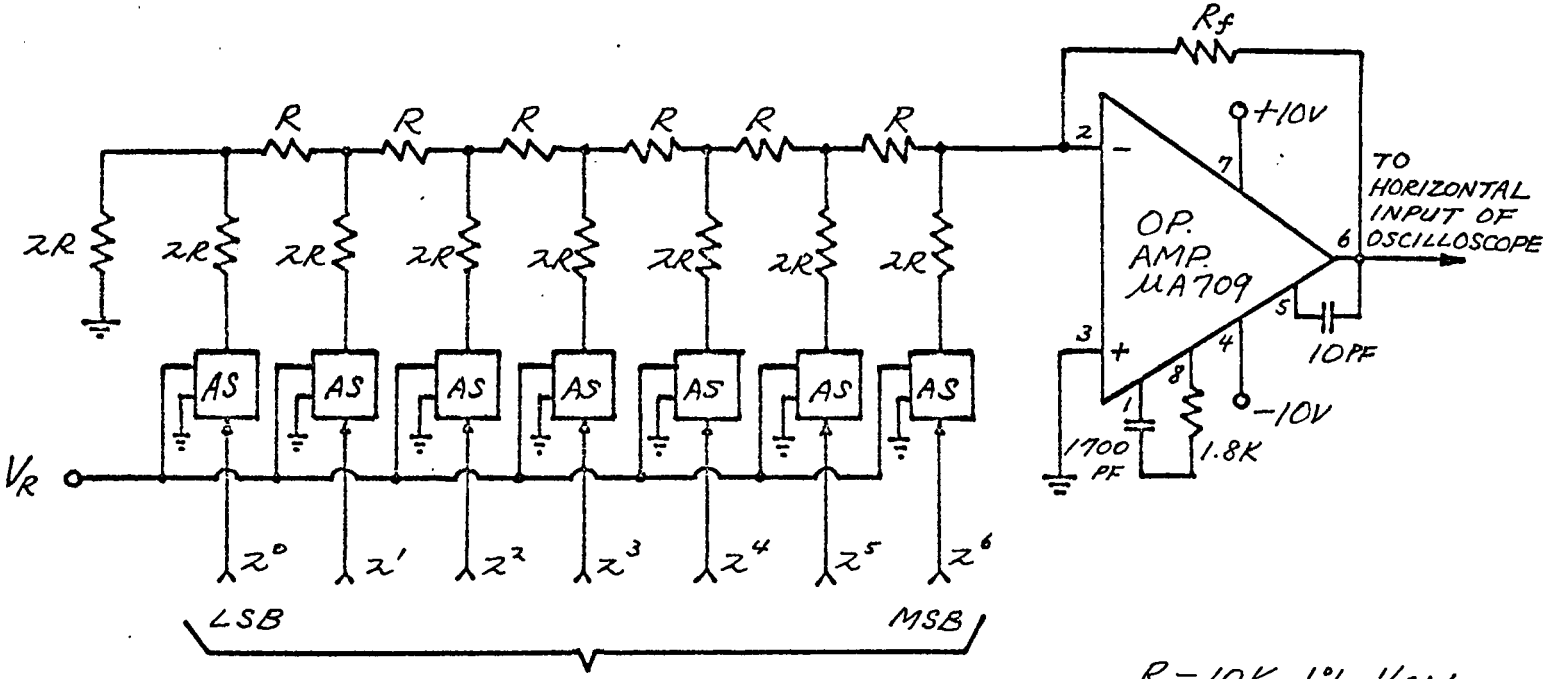

-10V
VR (-3.8V)
8.2K
10K
IN198
DIGITAL INPUT
47K
2N404
2N404
2R
TO DECODER
ANALOG SWITCH (AS)

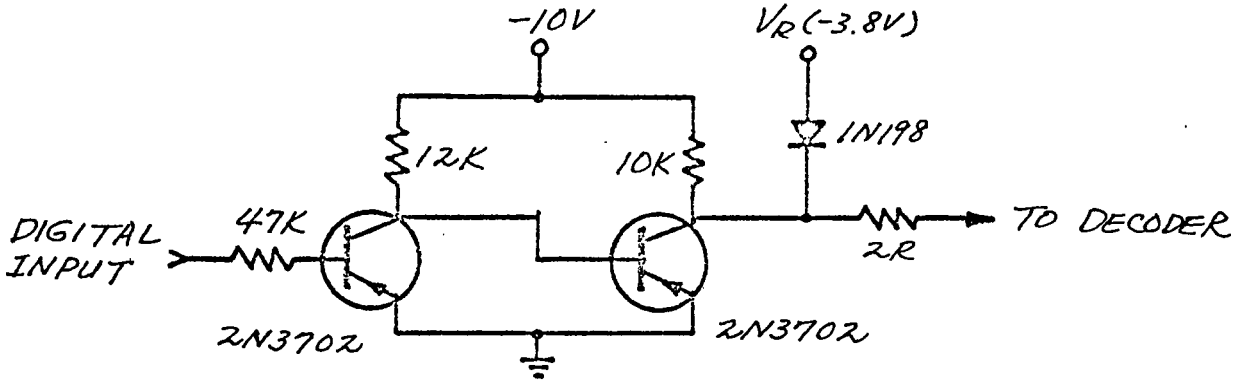
Fig. A-6 DACy



$R = 10K, 1\%, 1/4W$

$2R = 20K, 1\%, 1/4W$

$R_f = 10K, 1\%, 1/4W$



ANALOG SWITCH (AS)

Fig. A-7 DAC_X

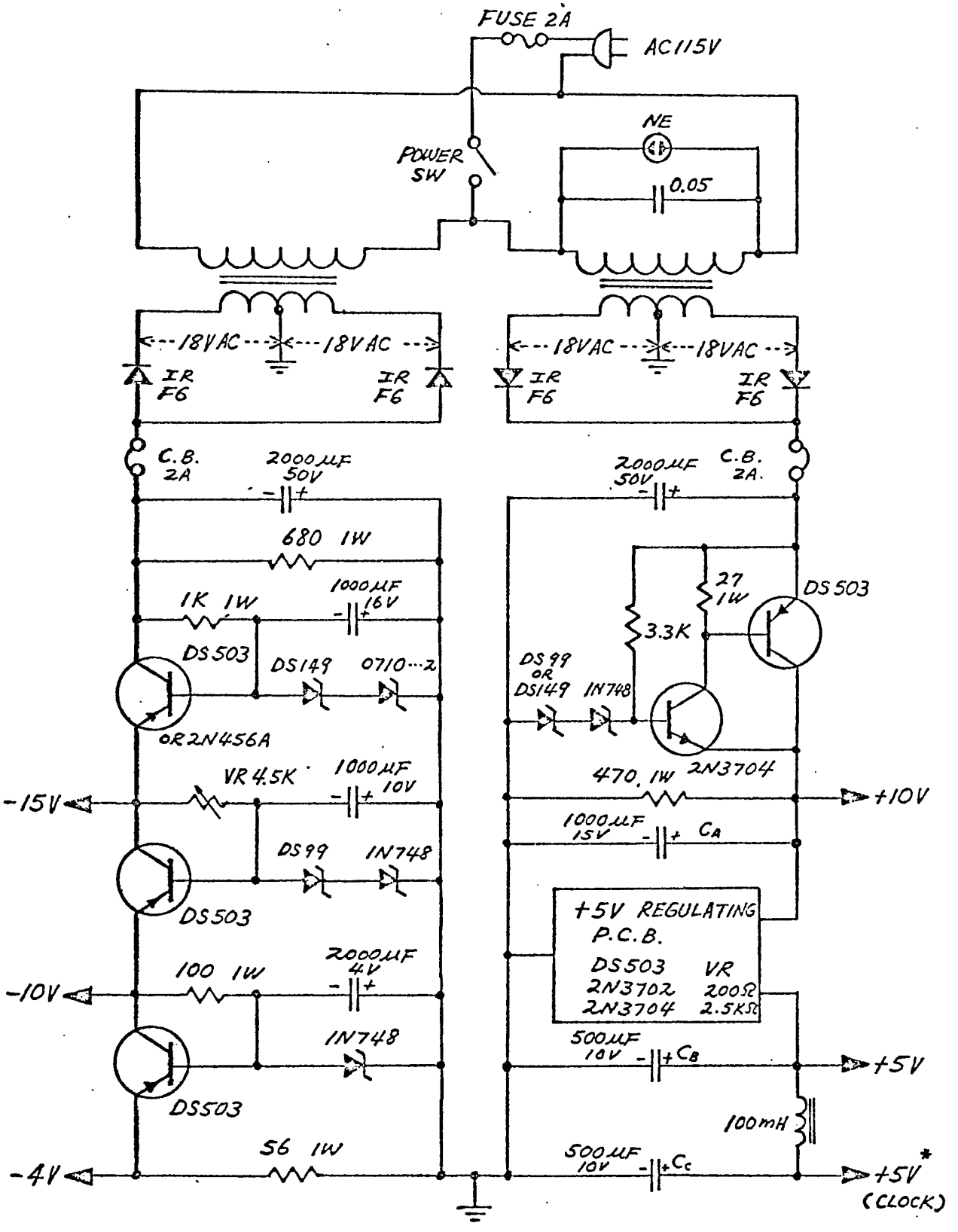


Fig. A-8 POWER SUPPLY

PULSE HEIGHT ANALYZER	PIN NO. & JACK	TERMINAL BOARD	ATHENA COMPUTER
WAIT SYNC →	5A	BA34	J154(11B)
OPEN GATE ←	7A	BB34	J123(11B)
DIGITAL OUTPUT 0	10A	AA1	J80101
1	11A	AA2	J80102
2	12A	AA3	J80103
3	13A	AA4	J80104
4	14A	AA5	J80105
5	15A	AA6	J80106
6	16A	AA7	J80107
7	17A	AA8	J80108
CLEAR M.C. SW	20A	BB26	TARGET SW4
DATA LOAD SW	22A	BB27	TARGET SW2
READOUT DATA SW	24A	BB28	TARGET SW6
SW COMMON	1A	BB29	TARGET SW COM
CLEAR M.C. LAMP	21A	BC26	TARGET LAMP 4
DATA LOAD LAMP	23A	BC27	TARGET LAMP 2
READOUT DATA LAMP	25A	BC28	TARGET LAMP 6
LAMP COMMON	27A	BC29	TARGET LAMP COM
READY SW (C)	3A	BB32	READY SW (C)
READY SW (N.O.)	4A	BB31	READY SW (N.O.)
READY LAMP	6A	BC31	READY LAMP
READY LAMP (COM)	26A	BC32	READY LAMP (COM)
GROUND	2A	BC34	GROUND

Fig. A-9 ATHENA-PULSE HEIGHT ANALYZER CABLE INTERCONNECTION

PULSE HEIGHT ANALYZER	PIN NO. & JACK	TERMINAL BOARD	ATHENA COMPUTER
DAC_Y DIGITAL INPUT			DISPLAY REGISTER
1	1B	BA5	J80205
2	2B	BA6	206
3	3B	BA7	207
4	4B	BA9	209
5	5B	BA10	210
6	6B	BA11	211
7	7B	BA13	213
8	8B	BA14	214
9	9B	BA15	215
10	10B	BA17	217
11	11B	BA18	218
12	12B	BA19	219
13	13B	BA21	221
14	14B	BA22	222
15	15B	BB1	224
16	16B	BB3	226
17	17B	BB4	227
18	18B	BB5	228
19	19B	BB7	230
20	20B	BB8	231
21	21B	BB9	232
22	22B	BB11	J80234
23	23B	BC14	DR-29
24	24B	BC16	DR-30

PULSE HEIGHT ANALYZER	PIN NO. & JACK	TERMINAL BOARD	ATHENA COMPUTER
DAC_X			
DIGITAL INPUT			INDEX REGISTER
1	30B	BA26	J242B (7B)
2	31B	BA27	J242A (7A)
3	32B	BA28	J252B (7B)
4	33B	BA29	J252A (7A)
5	34B	BA30	J253A (7A)
6	35B	BA31	J250A (7A)
7	36B	BA32	J272B (5B)

Fig. A-10 ATHENA-PULSE HEIGHT ANALYZER CABLE INTERCONNECTION

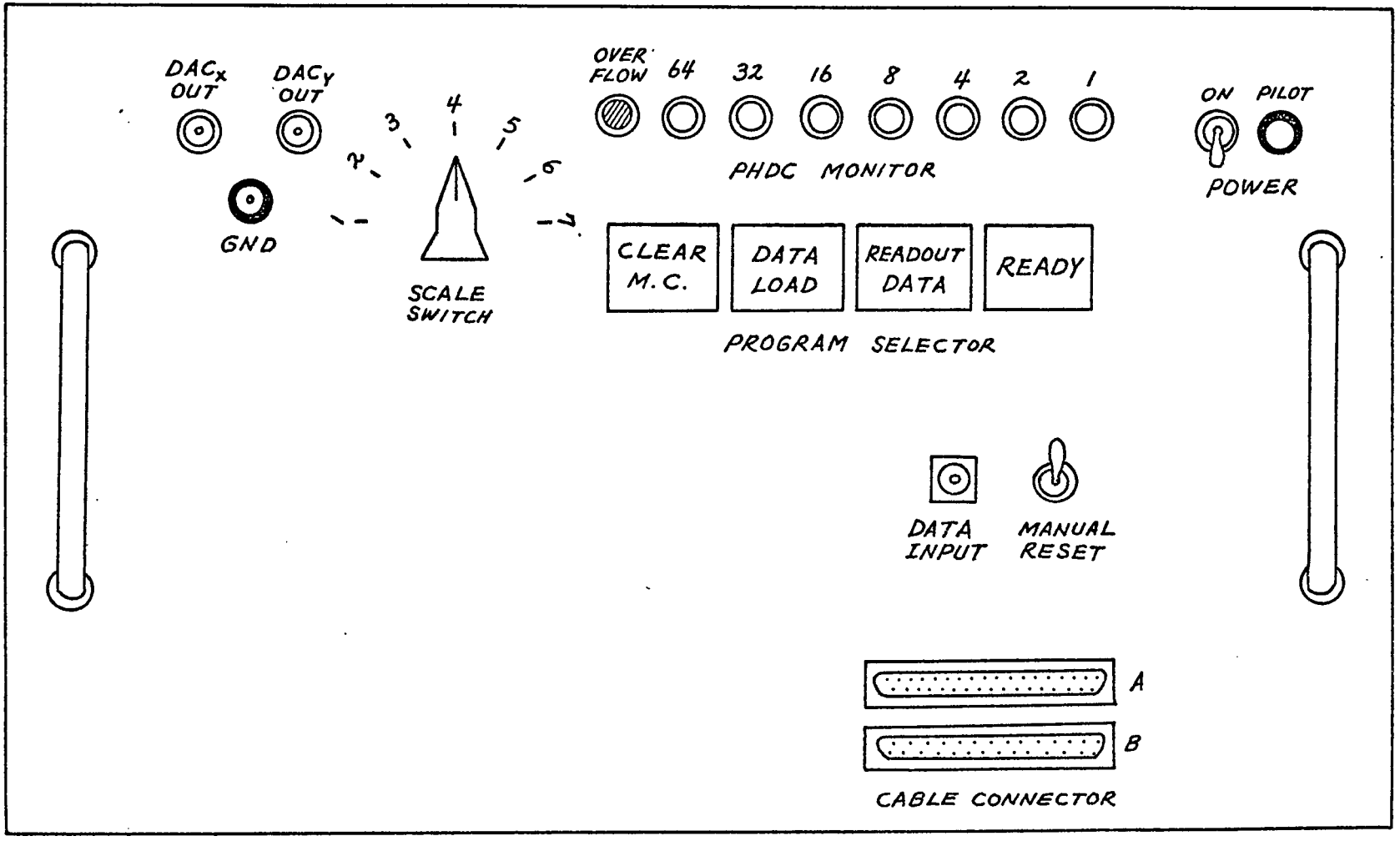


Fig. A-11 FRONT PANEL OF THE PULSE HEIGHT ANALYZER

APPENDIX B

Program Listings

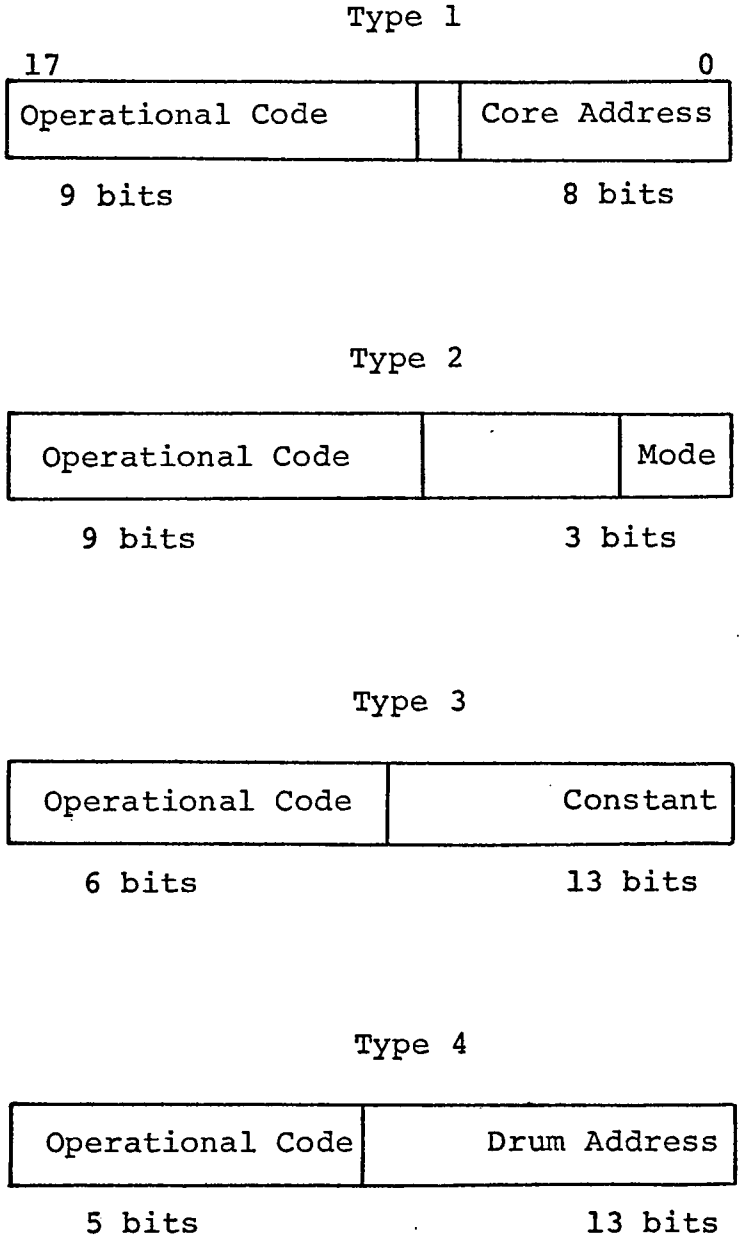


Fig. B-1 TYPES OF PROGRAM WORDS OF ATHENA

Instruction	Octal Code	Type of Instruction	Instruction Description
CX	12-	3	Transmit the rightmost 12 bits of instruction word to the x register at bit positions X_{00-11}.
CA	14-	3	Transmit the rightmost 12 bits of instruction word to the x register at bit positions x_{12-23}. Clear the accumulator and add the quantity in x to the accumulator.
SA	004	1	Store the contents of the accumulator in magnetic core storage.
LI	52-	3	Transmit the rightmost 8 bits of instruction word to the index register.
TD	024(001)	2	Cause the following instruction to be indexed.
TD	024(003)	2	Cause the following instruction to be indexed and then the index register to be decremented.
TJ	30-	4	Jump to the 13-bit drum address specified in the instruction word if the contents of index register are zero.

Fig. B-2 INSTRUCTION REPERTOIRE OF ATHENA (1)

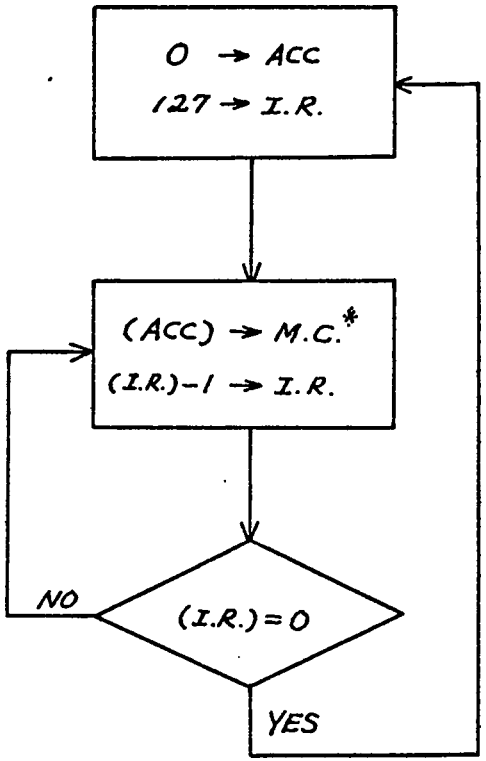
Instruction	Octal Code	Type of Instruction	Instruction Description
UJ	20-	4	Unconditional Jump
SI	006	1	Store the input data in magnetic core storage.
LV	426	2	Transmit 8 bits in x_{00-07} to the index register.
TP	060	1	Clear accumulator and add the quantity in magnetic core storage.
AD	064	1	Add to contents of accumulator the quantity in magnetic core storage and place results in accumulator.
WP	34-	4	Wait for Partial Sync Pulse
DD	417(003)	2	Transmit data from the accumulator to the output jack-panel via the display register (24-bit binary, no print cycle).
CJ	37-	4	Co-efficient Jump. Jump to a drum group sector in drum groups four, five, and six; the specific sector being determined by the PROG-SEL push-button selected.

Fig. B-3 INSTRUCTION REPERTOIRE OF ATHENA (2)

PROGRAM	PROGRAM ADDRESS (OCTAL)	OP CODE	INSTRUCTION (OCTAL)
Store +1 in the core address, 310_8		CX CA SA	120001 140000 004310
Remote Program Selecting	00040*	CJ	370000

*When READY pushbutton is depressed during operation the computer always returns to this address.

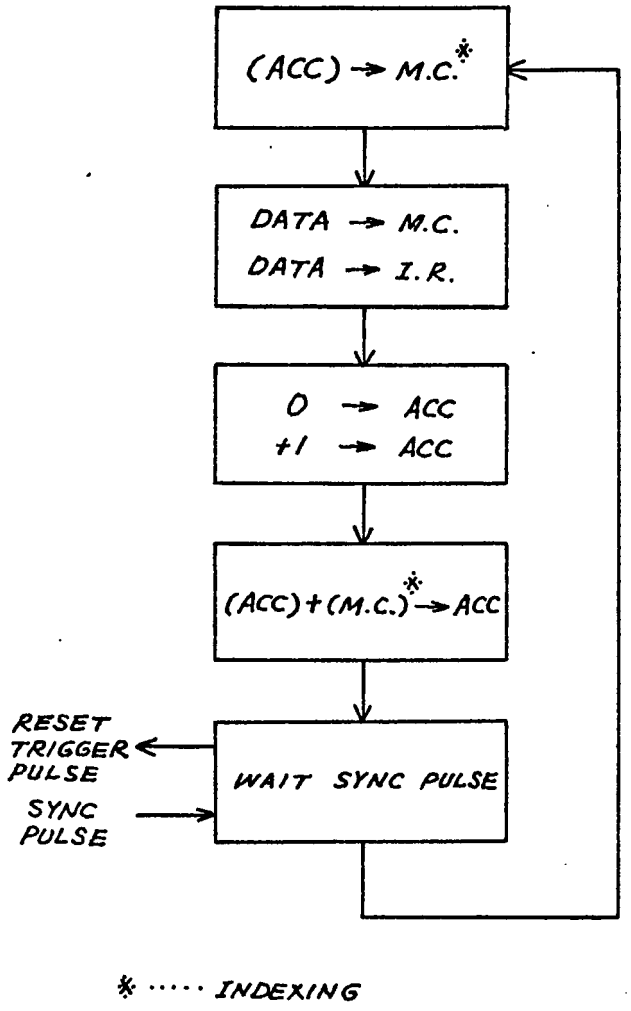
Fig. B-4 SUB-PROGRAM



Program Address (Octal)	OP Code	Instruction (Octal)
12000	CX	120000
12001	CA	140000
12002	LI	520177
12003	TD	024003
12004	SA	004000
12005	TJ	312000
12006	UJ	212003

*Program Location --- Drum Group 5
Sector Block 4

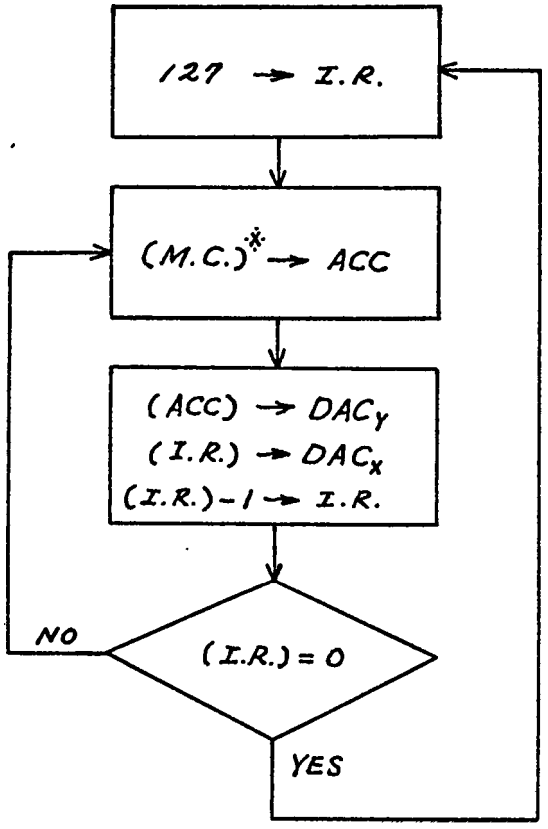
Fig. B-5 CLEAR M. C. PROGRAM



Program Address (Octal)	OP Code	Instruction (Octal)
11000	TD	024001
11001	SA	004000
11002	SI	006300
11003	LV	426000
11004	TP	060310
11005	TD	024001
11006	AD	064001
11007	WP	351000

*Program Location ----- Drum Group 4
Sector Block 2

Fig. B-6 DATA LOAD PROGRAM



Program Address (Octal)	OP Code	Instruction (Octal)
13000	LI	520177
13001	TD	024003
13002	TP	060000
13003	DD	417003
13004	TJ	313000
13005	UJ	213001

*Program Location --- Drum Group 5
Sector Block 6

Fig. B-7 READOUT DATA PROGRAM

(1) STANDBY the computer in NORMAL RATE
(2) depress READY
(3) depress CLEAR M.C.
(4) depress RUN
check the zero display on the oscilloscope
with the 7 scale switch positions.
(5) depress STOP
(6) depress READY
(7) depress LOAD DATA
(8) depress RUN
(9) depress STOP by the given schedule
(10) depress READY
(11) depress READOUT DATA
(12) depress RUN
study results on the oscilloscope
with changing the scale switch position
(13) depress STOP

It is also possible to continue the LOAD DATA after a READ-OUT DATA without a CLEAR M.C.

Fig. B-8 SYSTEM OPERATION