THE NOISE PERFORMANCE
OF
A SQUARING LOOP PSK DEMODULATOR

A Thesis

Presented to

the Faculty of the Department of Electrical Engineering

University of Houston

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

---

by

Wai-Leung Hon

May 1969

ACKNOWLEDGEMENTS

The author wishes to acknowledge the encouragement, guidance and counsel received from Dr. R. D. Shelton throughout the research. To S. Riter, the author expresses his appreciation for the use of his analytical calculations. Appreciation is also extended to Mrs. Alice Roach and Mr. John Hennessy for typing and assembling the thesis.

The author also wishes to acknowledge the sponsorship of this research through NASA Grant NGR-44-005-039.

Wai-Leung Hon

May 1969

THE NOISE PERFORMANCE
OF
A SQUARING LOOP PSK DEMODULATOR

An Abstract

of

A Thesis

Presented to

the Faculty of the Department of Electrical Engineering

University of Houston

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

---

by

Wai-Leung Hon

May 1969

ABSTRACT

In this research, a receiver was developed and built for the acquisition of pulse signals from Phase-Shift-Keyed (PSK) modulated signals transmitted over a noisy channel. To demodulate a PSK modulated signal, a phase-coherent signal of the carrier frequency is needed. This is quite often obtained from a synchronized pilot tone (in practice, this signal is usually referred to as the sync-subcarrier) transmitted along with the PSK signal. However, there are several disadvantages associated with this method that render it impractical for space communications.

A better method is the use of a squaring loop to derive the carrier frequency and phase from the received PSK signal. This method was used in the receiver.

A low frequency model of the receiver (at 225 kHz) was built and tested with PSK signal contaminated by white Gaussian additive noise. The performance of the receiver was indicated by the bit-error-rate at different signal-to-noise ratios. These experimental results were then compared with theoretical results obtained elsewhere.

TABLE OF CONTENTS

LIST OF FIGURES

FIGURE PAGE

LIST OF TABLES

CHAPTER I

INTRODUCTION

The Theory of Demodulation of PSK Signal

A phase shift key (PSK) modulation scheme uses

$$S_1(t) = K_1 \cos(2\pi f_c t + 90^0 + \theta)$$

to represent a binary "one" and

$$S_2(t) = K_1 \cos(2\pi f_c t - 90^0 + \theta)$$

to represent a binary "zero". The parameter f_c is the carrier frequency, θ is the phase angle with respect to an arbitrary reference and K_1 is the amplitude of the signal.

The bit rate f_b is less than the carrier frequency f_c by a factor n. Thus each bit is represented by a sequence of n cycles of either $S_1(t)$ or $S_2(t)$. Also, the length of each bit (T) is

$$T = 1/f_b = n/f_c.$$

A typical PSK signal is shown in Fig. 1. with n=4.

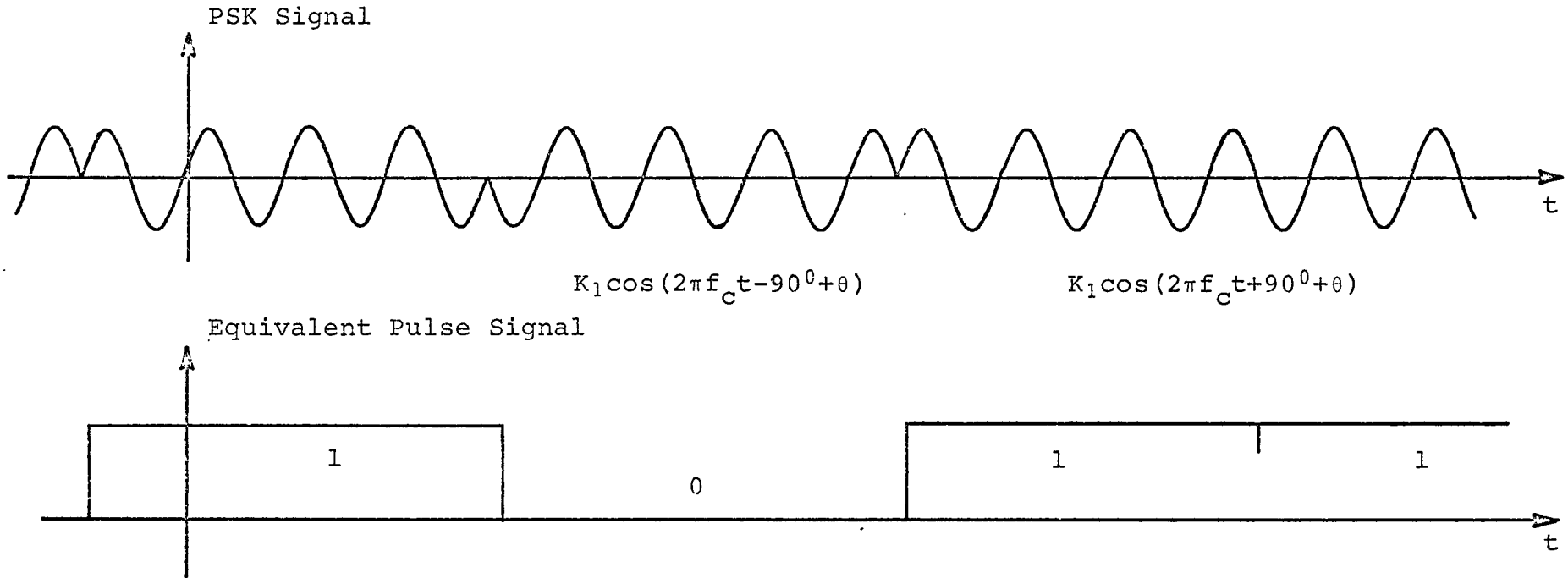


Figure 1. PSK Signal

The demodulation operation is performed by a multiplier-integrator combination. A carrier reference $R(t) = K_2\cos(2\pi f_c + 90^0 + \theta)$ of the same frequency f_c and phase θ is multiplied by the PSK signal. The result is

$$S(t)\cdot R(t) = \begin{cases} K_1K_2\cos^2(2\pi f_c t + 90^0 + \theta) & \text{if } S(t)=S_1(t), \\ -K_1K_2\cos^2(2\pi f_c t + 90^0 + \theta) & \text{if } S(t)=S_2(t). \end{cases}$$

Integrating the product over the period T results in the following:

$$\int_0^T S(t)\cdot R(t)dt = \begin{cases} \int_0^T S_1(t)\cdot R(t)dt \\ \int_0^T S_2(t)\cdot R(t)dt \end{cases}$$

$$= \begin{cases} K_1K_2/2 & \text{if } S(t) = S_1(t), \\ -K_1K_2/2 & \text{if } S(t) = S_2(t). \end{cases}$$

These two resulting values, $K_1K_2/2$ and $-K_1K_2/2$ represent the "1" and "0" of the original signal respectively.

This operation may be mechanized as indicated in Fig. 2.

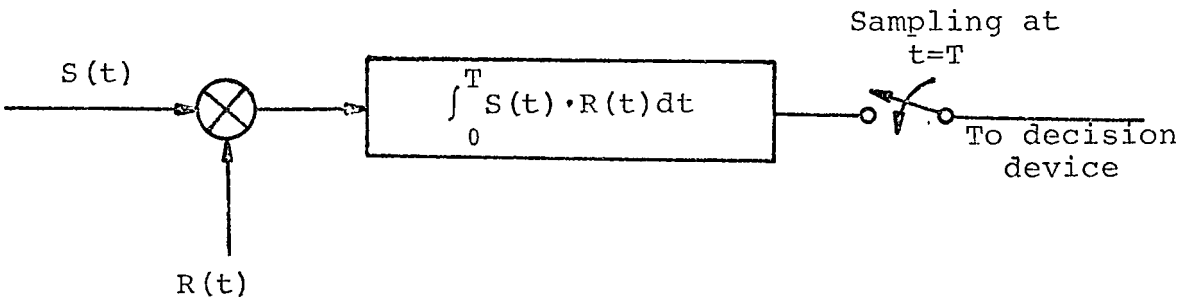


Figure 2. Demodulation Operation

Derivation of the Carrier Reference

Two methods are generally used for the derivation of the carrier reference. One method requires the transmission of an auxiliary carrier (usually referred to as the sync-subcarrier). This carrier is tracked at the receiver by means of a phase-locked-loop. The output of the loop is used as a reference signal for performing demodulation. The other method is to obtain the synchronization directly from the PSK modulated signal. There are several ways to do this, but only the squaring loop method is being considered in this study.

The basic operation performed by a squaring loop is illustrated in Fig. 3. The received PSK signal

$$S(t) = K_1 \cos(2\pi f_c t \pm 90^0 + \theta)$$

is squared. The result is

$$S^2(t) = K_1^2 \cos^2(2\pi f_c t \pm 90^0 + \theta)$$

$$= K_1^2 \left\{ \tfrac{1}{2} + \tfrac{1}{2} \cos 2(2\pi f_c t \pm 90^0 + \theta) \right\}$$

$$= K_1^2 \left\{ \tfrac{1}{2} + \tfrac{1}{2} \cos(4\pi f_c t \pm 180^0 + 2\theta) \right\} \quad .$$

Since $\cos(A+180^0) = \cos(A-180^0)$, the square of the PSK signal becomes

$$S^2(t) = K_1^2 \left\{ \tfrac{1}{2} + \tfrac{1}{2} \cos(4\pi f_c t + 180^0 + 2\theta) \right\} \quad .$$

Thus, the information modulated in the phase is eliminated. The double frequency component of $S^2(t)$ is then tracked by means of a phase-locked-loop whose voltage-controlled oscillator (VCO) output is frequency divided by two and is used as the carrier reference.

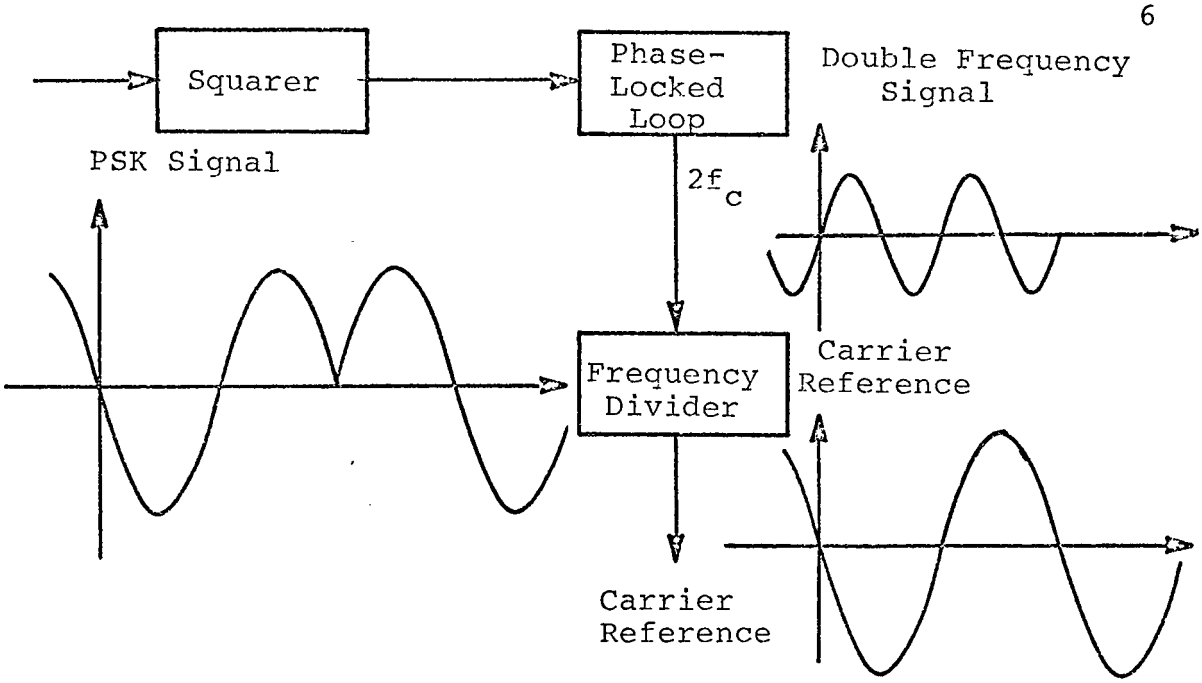


Figure 3. Squaring Loop

Performance of PSK Demodulator in the Presence of Noise

Communication channels are usually somewhat noisy. The presence of noise in the channel affects the demodulator in two ways. First, it contaminates the transmitted signal and causes error in detection. Secondly, the presence of noise creates phase-jitter at the output of the squaring loop. The phase-jitter, also called phase-noise, is the random variation of phase about the carrier reference phase. This also affects the demodulator and is considered as one kind of timing noise. There is another kind of timing noise which is directly related to the phase-jitter. This has to do with the instances at which the integrator outputs are

sampled. Such timing information is usually referred to as bit synchronization. Since the sampling time is synchronized to the output of the squaring loop, this kind of timing noise is directly related to the phase-jitter.

The performance of the PSK demodulator has been thoroughly investigated. Such investigations, using assumption that perfect carrier reference may be obtained, are well-known and documented[1]. Recently, work has been done to investigate the effect of phase-jitter (and therefore timing noise) on the performance of self-synchronized demodulators[2,3,4]. There appears to be very little experimental results to verify some of the more recent analytical work. The purpose of this thesis is to provide such verification for a complete squaring loop PSK demodulator.

The results of such studies are usually in terms of the input signal-to-noise ratio and the bit-error-rate. The bit-error-rate is the probability of an error occurring and can be obtained experimentally as the ratio of the number of errors occurred to the number of bits transmitted over a sufficiently long period of time.

Experimental Verification of Analytical Results

In this research, a low-frequency model of a squaring loop PSK demodulator was built and its performance tested with white Gaussian additive noise. Results were obtained for both cases where phase-jitter was present and not present. These were then compared with the analytical results.

Aside from the demodulator built, three other pieces of necessary equipment were also designed and built. They were a PSK signal generator, a simulated channel and an error detector. The PSK signal generator is capable of producing PSK signals equivalent to alternate "1's" and "0's". The simulated channel provides a point at which noise may be added to the signal. Errors occurring are detected by comparing the original pulse signal with the demodulated pulse signal. The error detector serves such a purpose. At the occurrence of an error, the error detector produces a pulse output and the number of these pulses is recorded by a digital counter.

The building of the demodulator and the equipment involved the use of numerous types of transistor circuits, including linear, non-linear, switching and logic circuits. In all, a total of about 100 transistors were used.

CHAPTER II

SYSTEM DESIGN

Design of the PSK Signal Generator:

In order to test the receiver, it was necessary to build a PSK signal generator to provide the PSK signal. For simplicity it was designed and built to produce PSK signals representing alternate "1's" and "0's". A block diagram of the PSK generator and the waveforms at different points is shown in Figure 4.

The generator is triggered by a 450 kHz reference signal. Using a flip-flop as a frequency divider, and a band pass filter, a square wave and a sine wave of 225 kHz are obtained. The square wave is used to trigger a series of three (3) flip-flops which divides the frequency by eight (8). The last flip-flop of the series is used to control two sampling gates, turning them on alternately. The outputs of the sampling gates are, therefore, bursts of 225 kHz signal with four cycles in each burst. One of the outputs is inverted and added to the other one producing a PSK signal whose bit rate (f_b) is $f_c/4$.

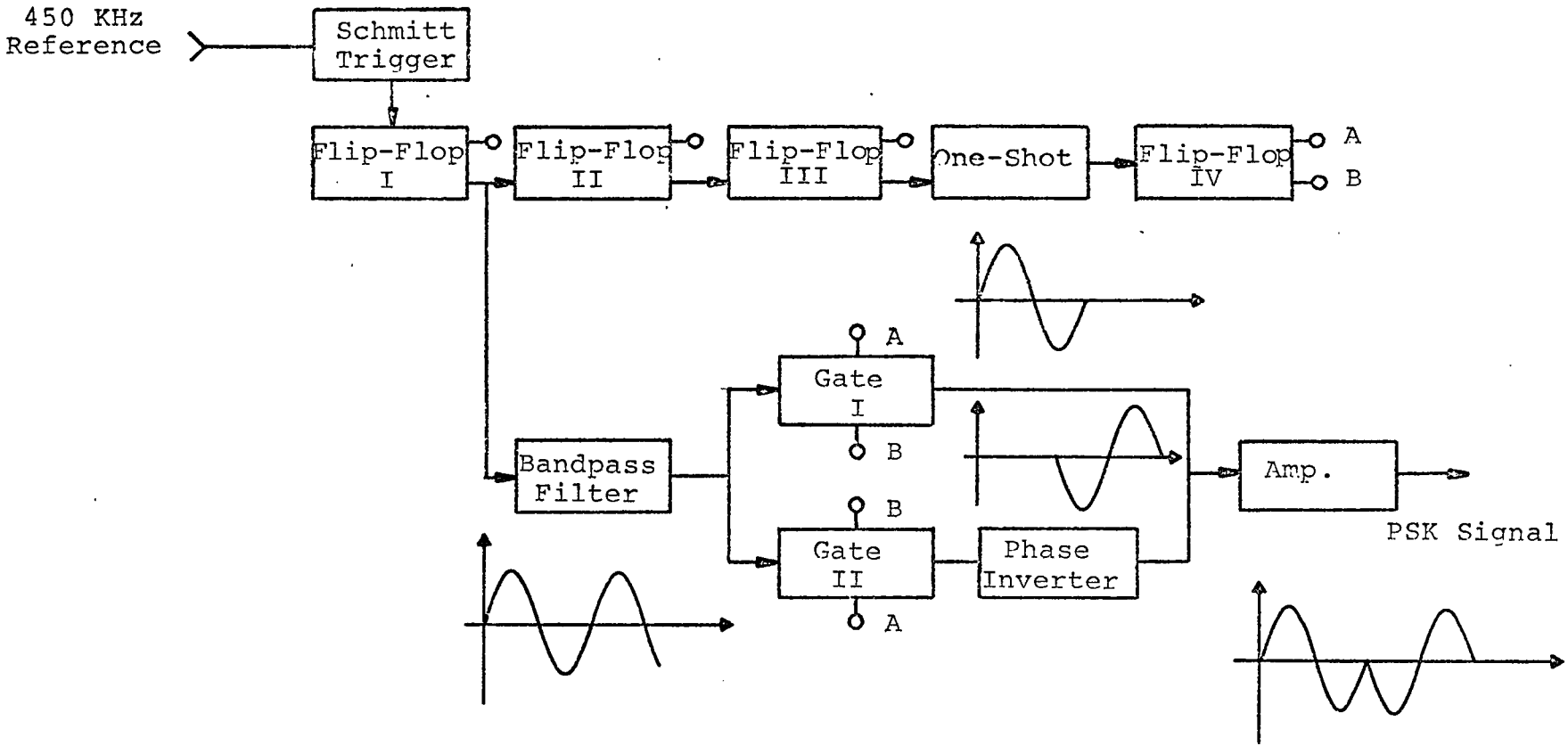


Figure 4. PSK Signal Generator

Design of the Simulated Channel

The simulated channel acts as a summing point at which noise may be added to the signal. It is desirable to have the input impedances to both signal and noise both equal and high. The equal impedances simplify calculation of signal-to-noise ratio. With the input impedances equal, the input signal-to-noise ratio, which is the ratio of input signal power to the input noise power, reduces to the square of the ratio of input signal voltage to the input noise voltage. The two impedances, being equal, cancel out in the ratio. The high input impedances protect both the PSK signal generator and the noise generator from being over-loaded.

The channel supplies signal and noise to both the squaring loop and the phase detector. The experiment calls for both measurement of performance of the demodulator with a steady carrier reference (i.e. no phase-noise) and then with a noisy reference. A selector switch is therefore built into the channel so that the input to the squaring loop can either be noise-free or noise contaminated. If the input is noise-free, the carrier reference has no phase-jitter. Fig. 5. is the block diagram of the simulated channel.

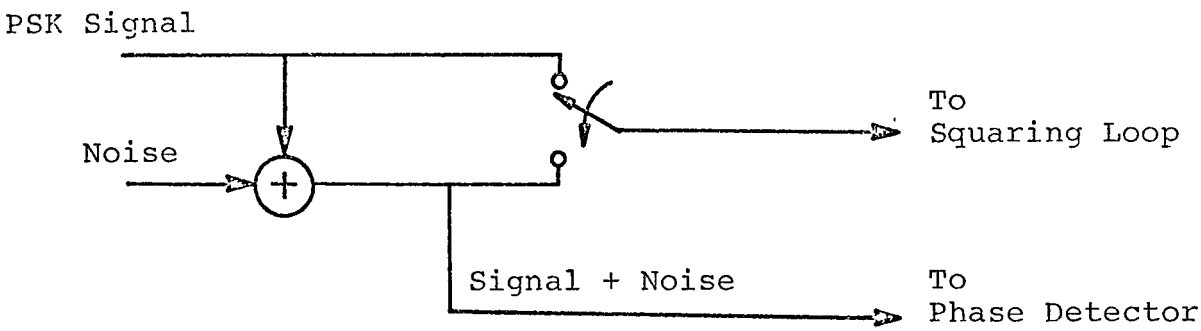


Figure 5. Simulated Channel Block Diagram

Design of the Error Detector

The error detector detects any error in demodulation by comparing the original pulse signal (a train of pulses of alternate "1's" and "0's") with the demodulated pulses. A block diagram of the detector is shown in Fig. 6.

The two inputs to the detector are the original pulse signal and the demodulated signal. The original pulse signal triggers a flip-flop. The outputs of the flip-flop are of half of the bit rate (f_b) and are 180^0 in phase with each other. Each output drives a narrow pulse-width one-shot circuit. These pulses are used to turn on two sampling gates.

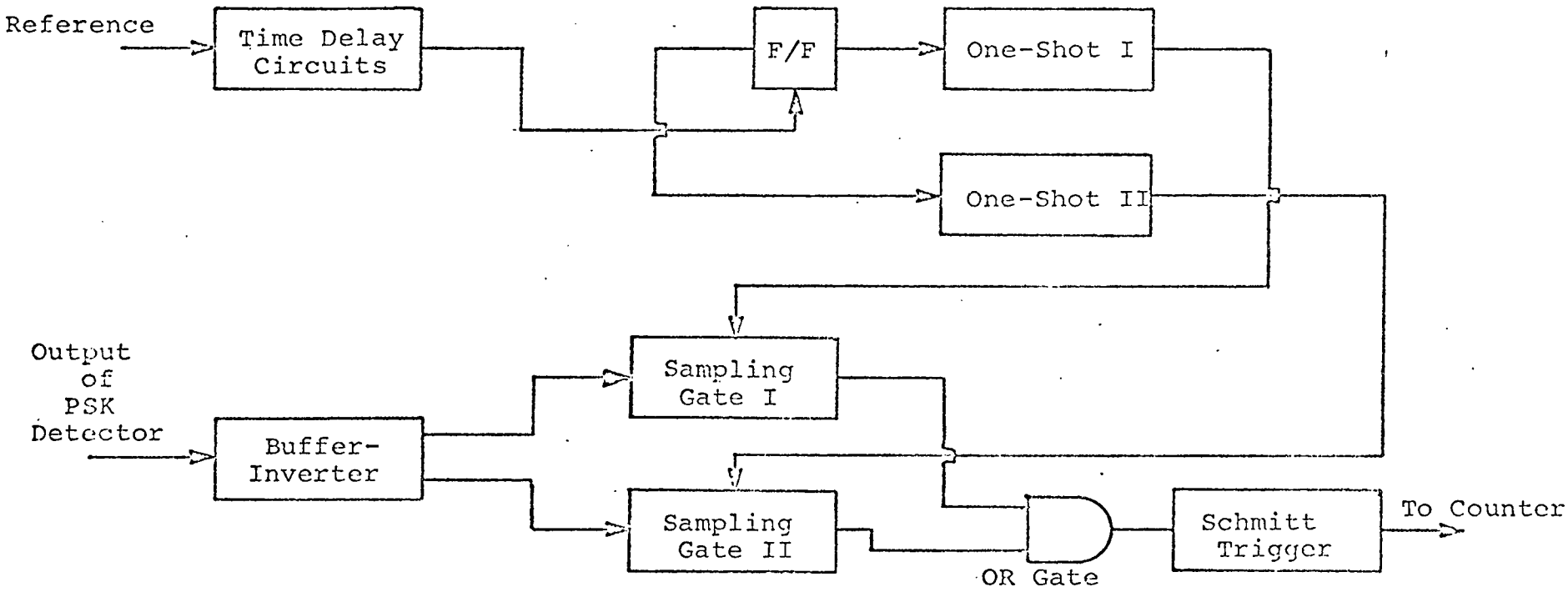


Figure 6. Error Detector

These gates are constructed such that the output is zero if the gate is turned off or if the input is a "0" when the gate is turned on; the output is a narrow pulse if the input is a "1" when the gate is turned on.

The demodulated pulses pass through a buffer-inverter circuit. The two outputs are the original and the inversion of the input signal (i.e. a "1" becomes a "0" and vice versa).

When the timing of the delay circuit is correctly adjusted and no error is occurring, one of the gates (gate I) is turned on only when the input is a "0". Thus no pulse is generated. The other gate (gate II) is turned on when the demodulated pulse is a "1". This gate is connected to the inverted output of the buffer-inverter circuit. Thus no pulse is generated either. This indicates the presence of no error.

If an "0" is missed and a "1" is resulted, the error will be detected by gate I. Similarly, gate II detects the missing of "1's".

The outputs of the two gates are added using an OR-gate. A Schmitt Trigger is then used to produce pulses of greater amplitude to drive the digital counter. It also acts

as a threshold circuit to discriminate between the error indicating pulses and any noise which might be present.

Design of the Squaring Loop PSK Demodulator

The combination of the detector of the synchronizer of Fig.2 and Fig.3 results in a simplified block diagram of the demodulator. This is shown in Fig.7.

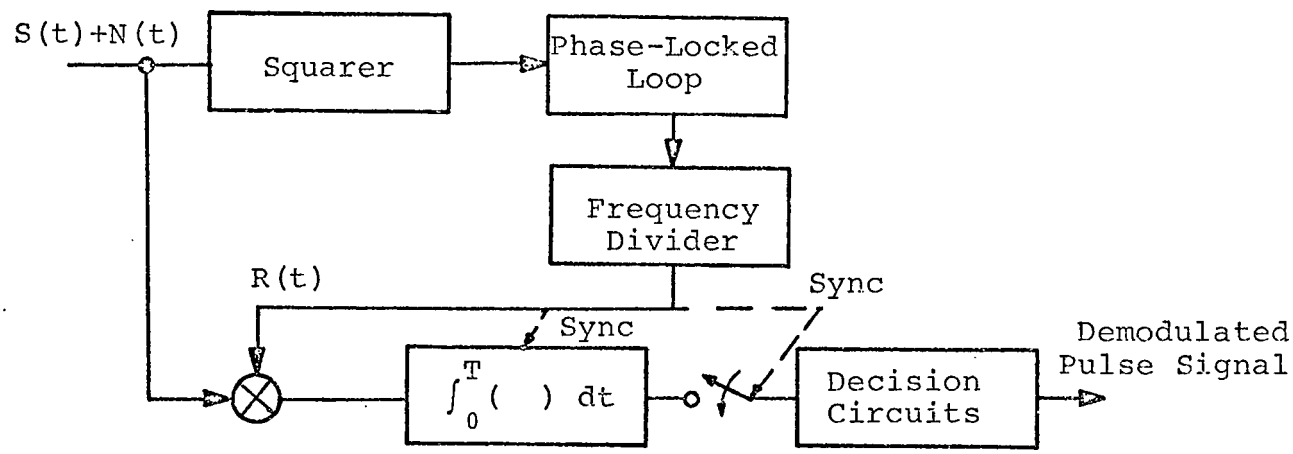


Figure 7. Squaring Loop PSK Demodulator

The squaring operation is first done by full-wave rectifying the receiving PSK signal. This removes or eliminates the phase-shift-keyed modulation. Then the double frequency component is filtered by a band pass filter cen-

tered at $2f_c$ as shown in Fig.8. Since the output frequency is double that of the input, the squarer is also referred to as frequency doubler.

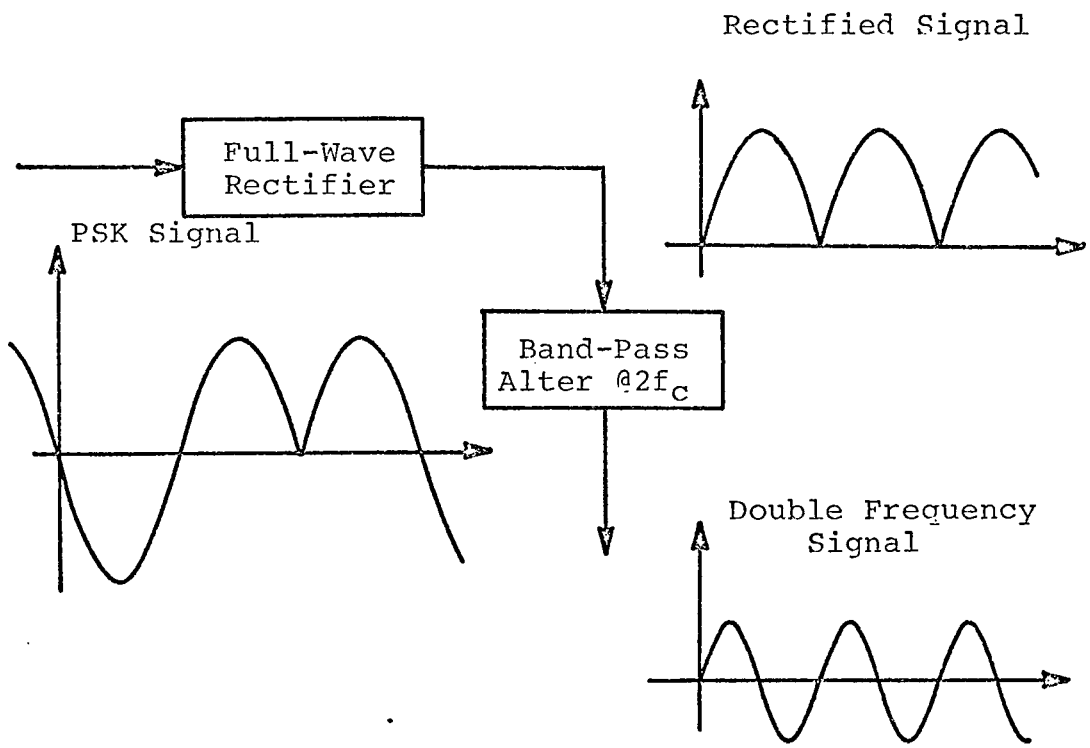


Figure 8. Squarer

A great deal of analytical and experimental work on phase-locked-loop has been done. It is essentially a feedback frequency control system as shown in Fig. 9. It consists of a phase detector, a low-pass filter (referred to as the loop filter) and a voltage-controlled oscillator (VCO).

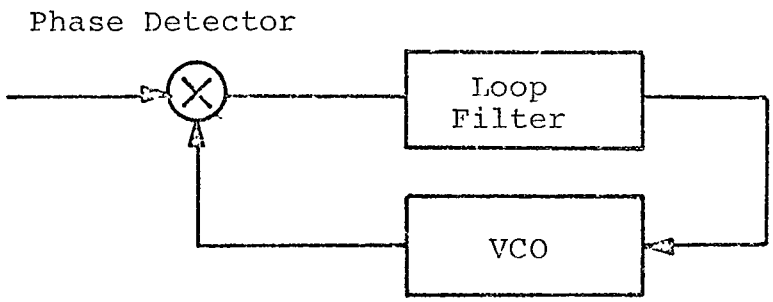


Figure 9. Phase-Locked-Loop

The problem of design and optimization of phase-locked-loops was studied as early as 1956 by R. Jaffe and E. Rechtin[5]. A brief description of the operating principles can be found in a paper they published.

The frequency divider can be a simple flip-flop, a regenerative frequency divider, or a tuned-oscillator frequency divider. The tuned-oscillator frequency divider was chosen.

In actual systems, a carrier reference generated using a squaring loop is either in-phase or 180^0 out of phase with the received signal. To eliminate this phase ambiguity, it is either possible to use differential PSK modulation or to transmit a phase reference prior to each message. This "1-0

ambiguity" can also be eliminated by special codes[6].

The other circuits of the demodulator are simple linear, nonlinear or switching circuits. They will be briefly described. The phase detector is a switching-type detector[7]. The integrator is a simple R-C integrator using a transistor as a discharging device. The sampler and the decision circuit are merely a sampling gate and a Schmitt's Trigger, respectively.

The bit rate of the system is one-fourth of the carrier frequency (i.e. n=4). Therefore, the bit synchronization is obtained through frequency dividing the carrier reference by four (using two flip-flops). Two series of narrow pulses are generated by two one-shots to control the integrator and the sampling gate. These pulses occur at bit-rate frequency (f_b), and the pulse that controls the sampling gate is slightly ahead of that which controls the integrator. The block diagram of the bit-synchronization circuits is shown in Fig. 10. Fig. 11, is a detailed diagram of the complete squaring loop PSK demodulator.

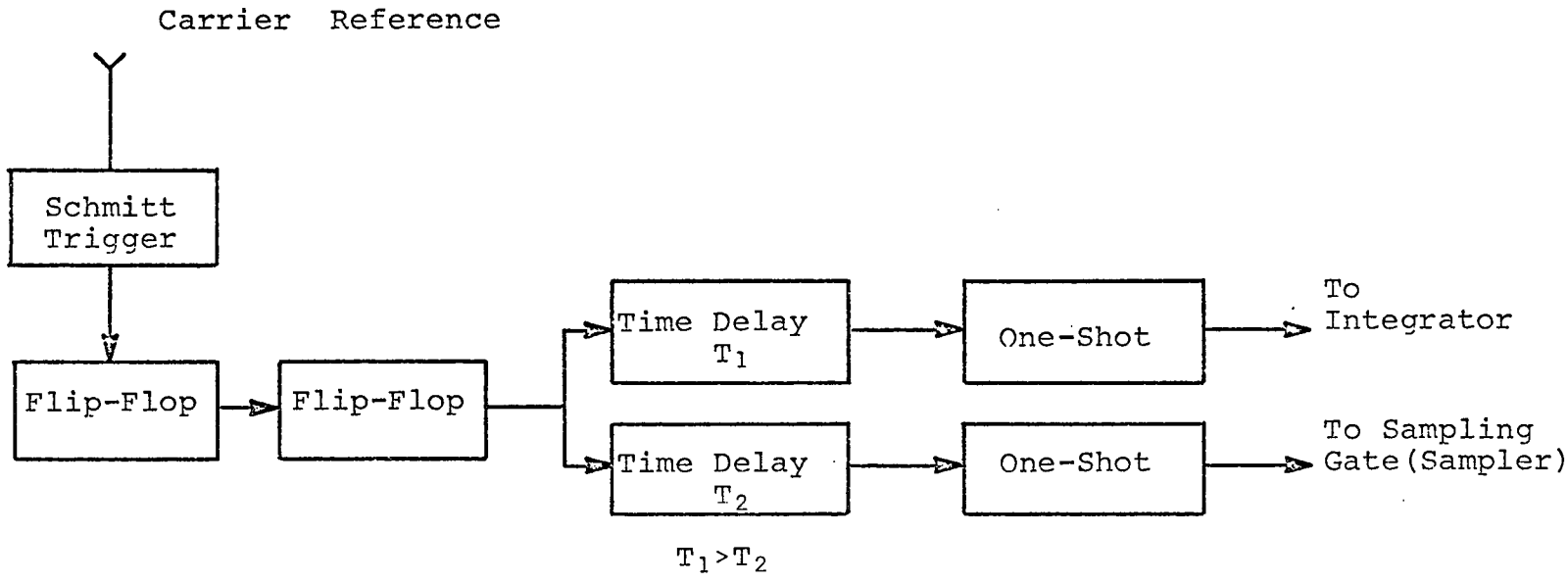


Figure 10. Bit Synchronization Circuit

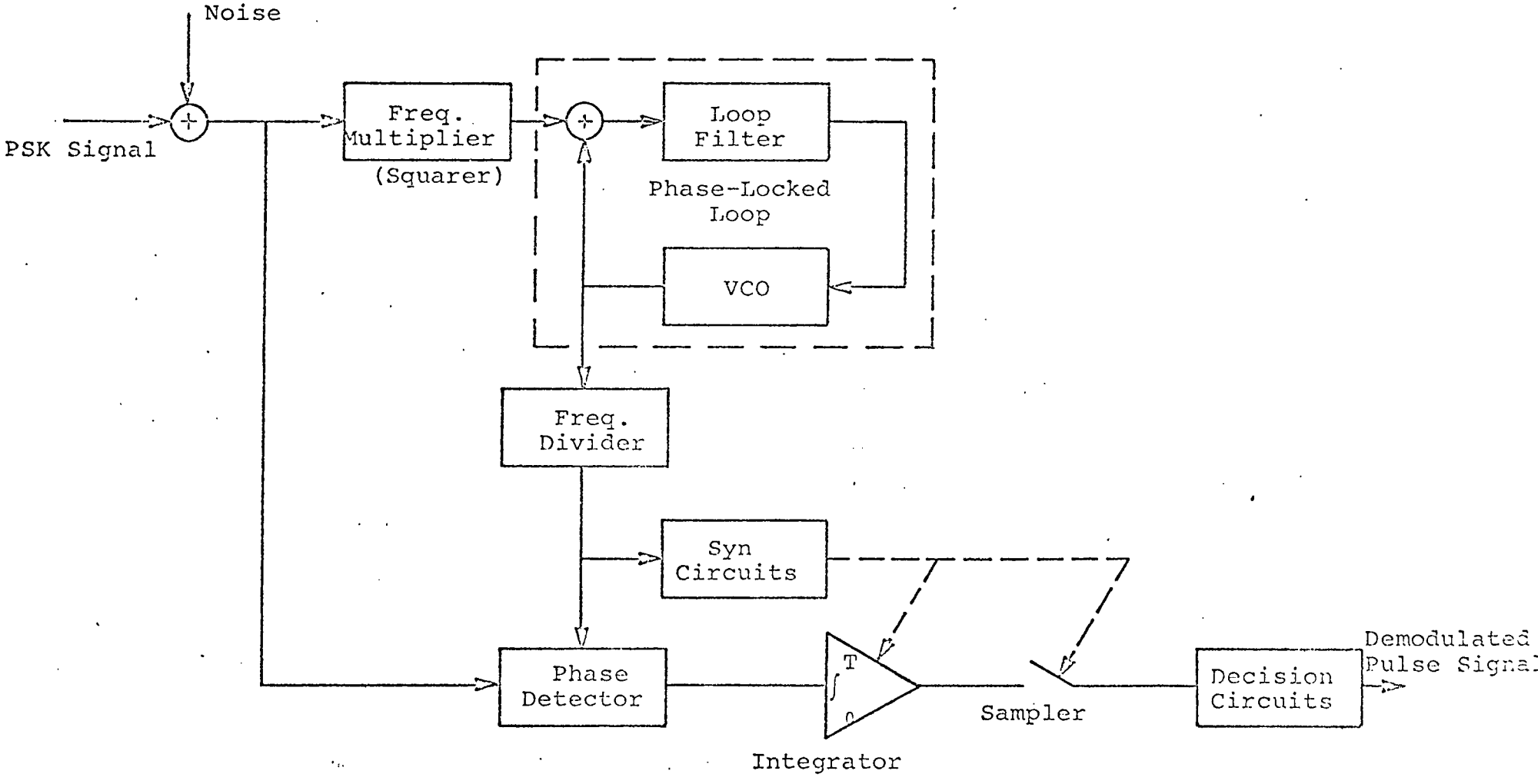


Figure 11. Squaring Loop PSK Demodulator

CHAPTER III

THE PHASE-LOCKED-LOOP

The accuracy of the demodulator depends largely on the phase-locked-loop which derives the carrier reference. At low signal-to-noise ratios, the performance of the phase-locked-loop is especially important. Becuase of large phase-jitter at low signal-to-noise ratios, the phase-locked-loop slips cycles. This causes error in the bit synchronization and results in complete failure of the demodulator. Therefore, the phase-locked-loop is specially treated in this chapter.

A phase-locked-loop can be viewed as a narrow bandwidth filter whose band-pass frequency is automatically controlled to be the input frequency. This special property enables the phase-locked-loop to be used to track frequency varying signals. In systems this variation is due to Doppler effect or instability of the various transmitter and receiver oscillators. As a result, a phase-locked-loop is quite often referred to as a narrow-band tracking filter.

The range of frequencies the phase-locked-loop is able to track is called the pull-in range and is dependent on the bandwidth of the loop filter. The wider the bandwidth, the wider the pull-in range. Obviously, it is desirable to have

a wide pull-in range. However, widening the loop filter bandwidth to increase the pull-in range increases the noise-bandwidth (i.e. phase-jitter increases). Another factor to be considered is the lockup time. For a certain pull-in range, noise bandwidth cannot be reduced without sacrificing the lockup time. A trade off must be made to optimize the performance of the phase-locked-loop.

The optimum loop filter was determined by F. J. Charles and W. C. Lindsey[8]. The loop filter is of the proportional-plus-integral control type which is generally used for carrier tracking purposes in phase-coherent communication systems. One realization of the loop filter is shown in Figure 12. This circuit is used in the demodulator.

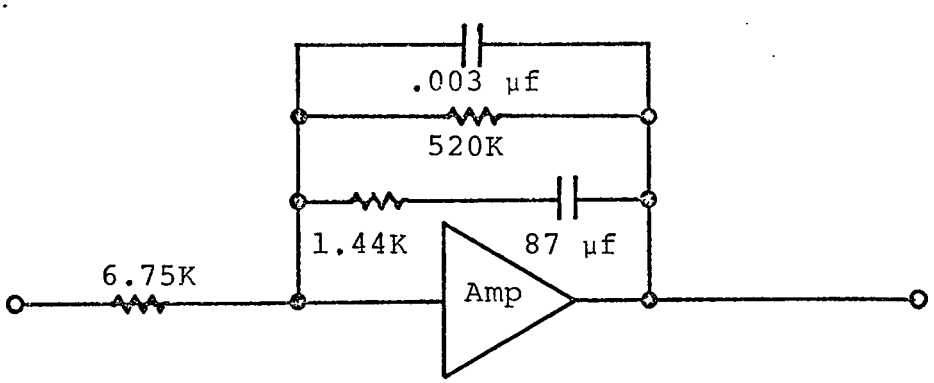


Figure 12. Loop Filter

CHAPTER IV

PROBABILITY OF ERROR AND SIGNAL-TO-NOISE RATIO

The performance of the optimum PSK demodulator in white Gaussian noise has been studied by many with the assumption that perfect carrier reference might be obtained[9]. For the equally likely transmission of "1's" and "0's", the probability of error was calculated to be

$$P(E) = \tfrac{1}{2}(1-\mathrm{erf}(\sqrt{E_s/N_o}))$$

where E_s is the signal energy per bit, N_o the one-sided noise power density and $\mathrm{erf}(\alpha)$ is the error function. Thus the performance of the system is solely a function of the signal-to-noise ratio (SNR).

The same result was obtained by different authors using different approaches. The signal-to-noise ratio in some cases are defined to be ST/N_o, where S is the signal power and T the bit length. The two are actually equivalent, therefore

$$SNR = E_s/N_o = ST/N_o.$$

In actual systems, a perfect carrier reference cannot be obtained because of noise at the tracking filter (phase-

locked-loop). The carrier reference signal contains phase-jitter (or phase-noise) and as a result degrades the performance.

Recently, work was done by W. C. Lindsey[10] and S. Riter[11], among others, to study the effect of noisy carrier reference on synchronous detection systems. Special attention was put into the investigation of systems using a squaring loop to derive the necessary carrier reference. Apparently, according to the investigation of H. L. Van Trees[12] and J. J. Stiffler[13], the squaring loop is the optimum method of derivation of carrier reference. The primary reason is that the power saved by not transmitting a sync-subcarrier can be put into the transmission of the information modulated signal and consequently increasing the signal-to-noise ratio.

Lindsey derived his result by assuming that the phase-jitter, although random, is constant within the period T during which a bit is being demodulated. Riter, on the other hand, assumed that the phase-jitter is totally random and it varies within the period T. Actually the phase-jitter is a continuous variation of phase and the rate of variation is comparatively slower than the bit-rate. Assuming that the phase-jitter is constant, as done by Lindsey, tends to under-

estimate the effect of the phase-jitter. Riter, on the contrary, overestimated the effect. The actual effect is therefore between the results obtained by the two. One of the objectives of this research is to verify the effect of noisy reference on the performance of the squaring loop demodulator.

CHAPTER V

EXPERIMENTAL RESULTS AND CONCLUSION

The complete performance test set is shown in Figure 13. The PSK signal generator is driven by an oscillator (Hewlett-Packard 200 CD) which provides a stable 450 kHz signal. This signal, which is two times the carrier frequency, is frequency divided to produce the necessary 225 kHz carrier frequency.

White Gaussian noise is obtained from a noise generator (Elginco, Model 602A). The bandwidth of the noise is set at 500 kHz. The power spectrum is fairly uniformly distributed within the band from 120 Hz to 500 kHz. The spectral density is approximately 1.1×10^{-3} volts/$\sqrt{\text{Hz}}$ at 1 volt rms (p.2-1 instruction manual). In the usual spectral density unit (V^2/Hz), the spectral density of the noise (N_0) at K volts rms is the square of the product of 1.1×10^{-3} and K. Therefore,

$$N_0 = (1.1 \times 10^{-3} \times K)^2 V^2/Hz \quad .$$

A band-pass filter is usually used for preliminary filtering of noise before the demodulation. The pass band of the filter has to be wide enough to pass the signal without

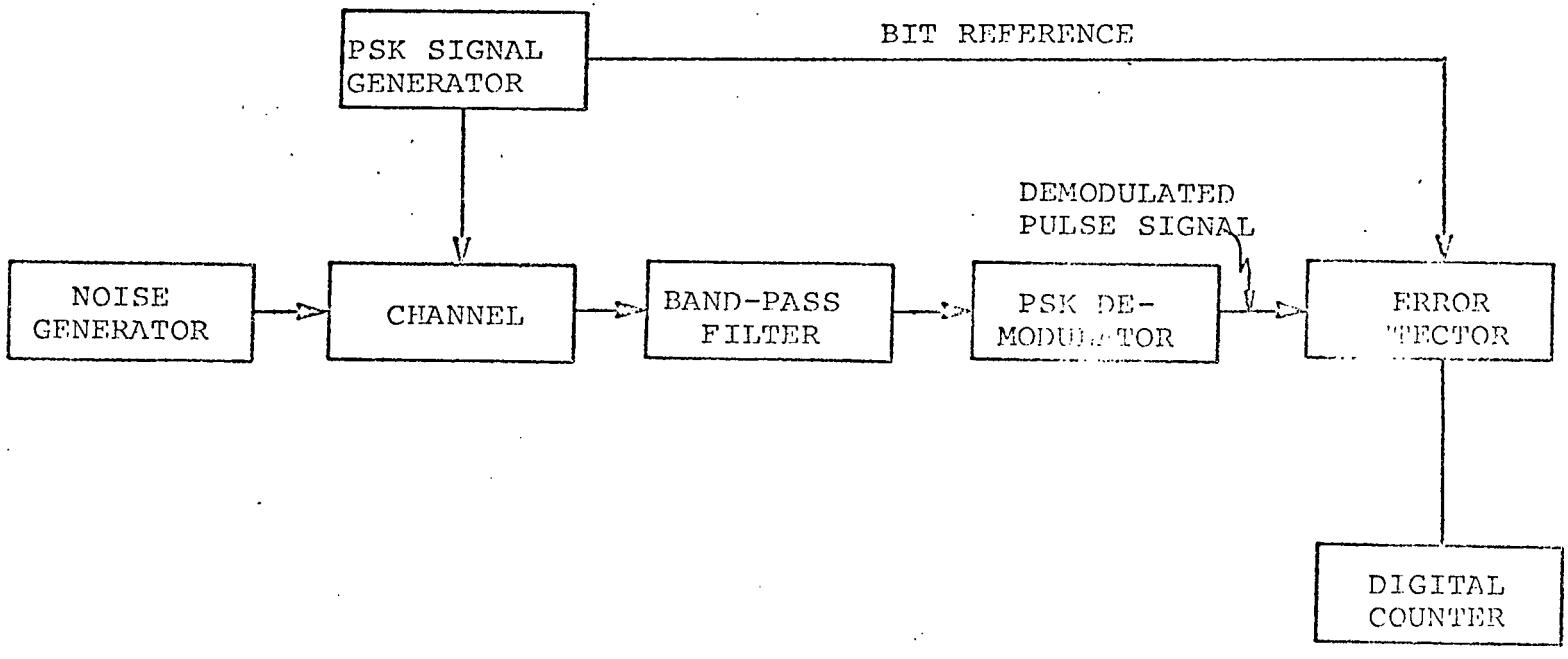


Figure 13. Performance Test Set

too much distortion. Because of the frequency limitation of the transistors used, the roll-off frequency of the channel is about 350 kHz. This coincides with the upper roll-off frequency of the necessary band-pass filter. Therefore, only a high-pass filter is needed. A simple high-pass filter with the lower roll-off frequency at about 20 kHz was used. Figure 13 is the high-pass filter used and the frequency response.

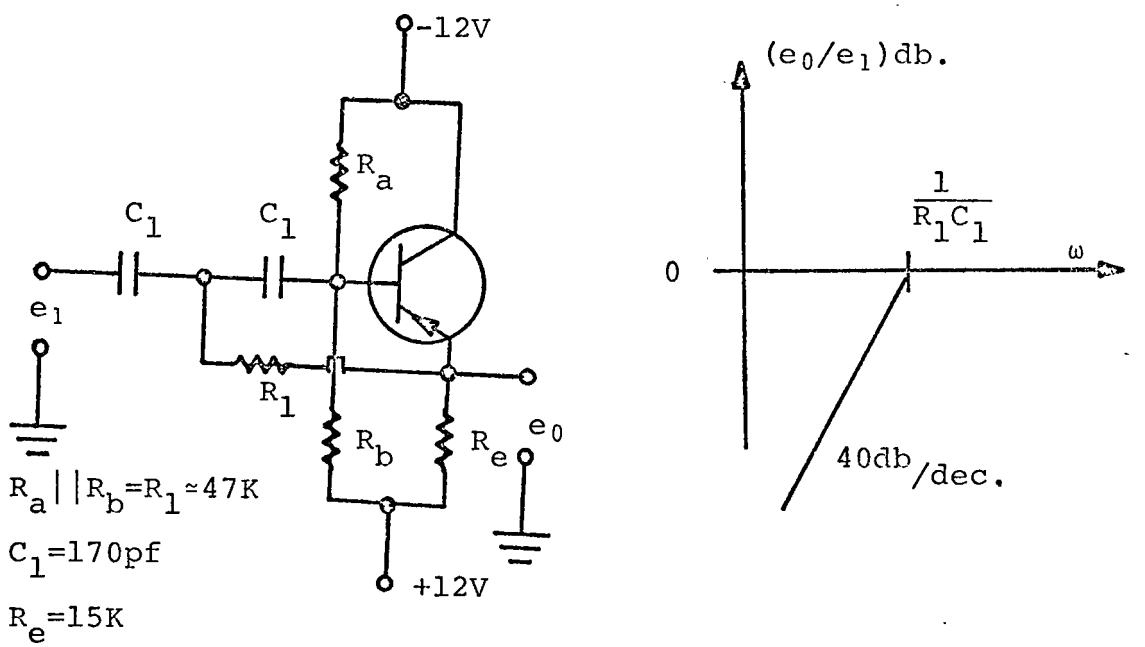


Figure 14. High-Pass Filter

The digital counter (Hewlett-Packard 521A) used for recording errors is capable of counting up to 10000 errors. A special feature of this counter is that it has an automatic gate which resets and switches on the counting for either 1/10 second or 1 second at a preset rate. This is especially useful for obtaining data at high bit-error-rate. The manual mode is also available for low bit-error-rate data recording.

At low bit-error-rate, it is essential to record data for a long period of time. However, with some preset measurement accuracy tolerance, the minimum time for data recording can be calculated. Appendix A shows the necessary time of data recording for different ranges of bit-error-rate.

Results of the performance of the squaring loop demodulator was obtained and plotted on Figure 15. The theoretically derived performance curves from the previously mentioned references were also plotted for the purpose of comparison.

The theoretical performance curve for noise-free reference detection was obtained from published literature[15]. Comparing this curve with the one obtained experimentally shows that the two curves are less than 1 dB apart. The normal operation region is where the bit-error-rate is about 10^{-3}. The curves indicate that an extra 0.6 dB of signal-to-noise

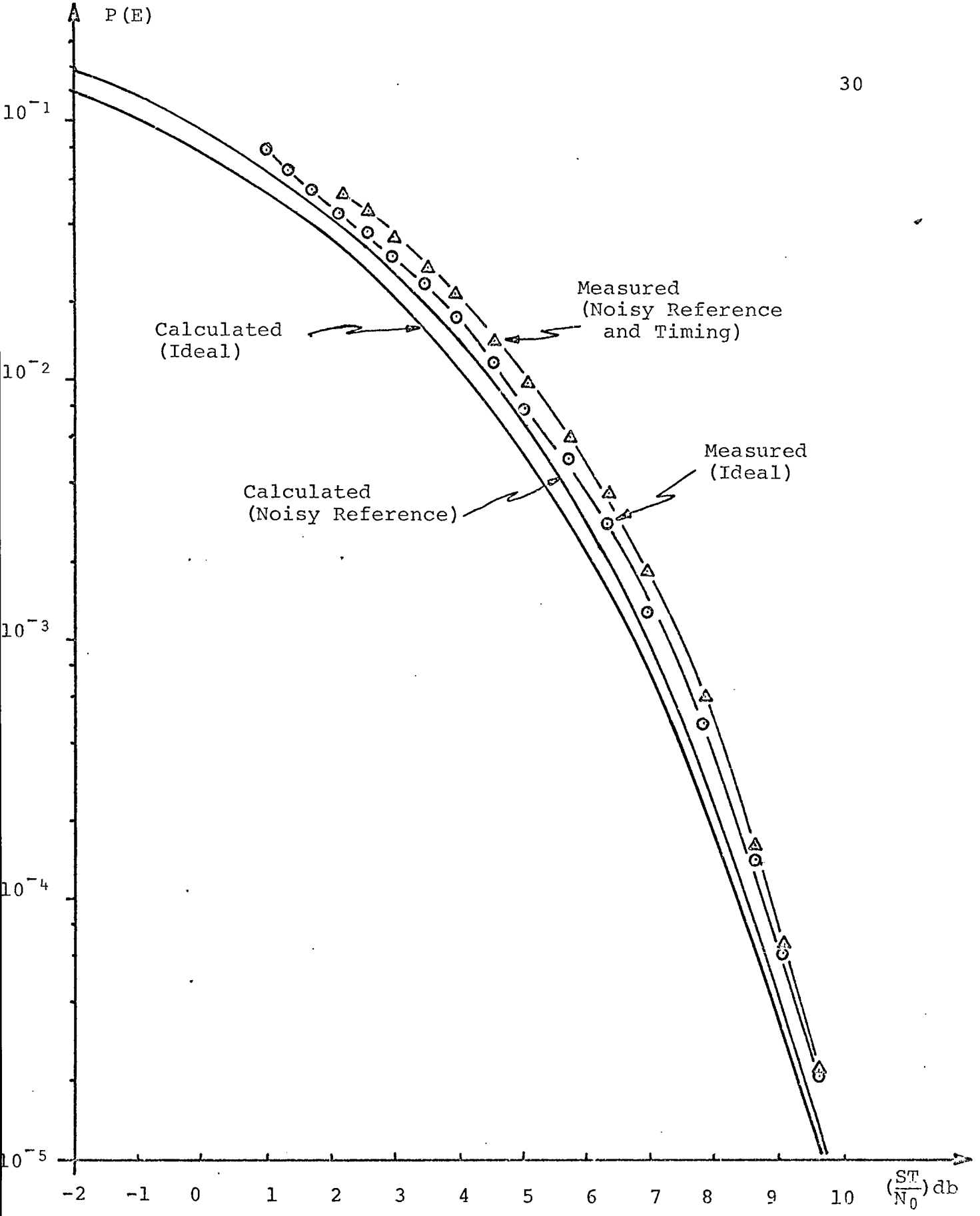


Figure 15. Probability of Bit Error versus Signal-to-Noise Ratio With a Squaring Loop

ratio is needed for the experimental detector to perform as well as the theoretical prediction at the normal operation region. This performance level is typical of commercial PSK demodulators.

A theoretical performance curve, taking consideration of the timing noise, was obtained from S. Riter[16]. The experimental results shows that the degradation of performance due to timing noise is very small. This agrees well with Riter's prediction.

The experimental results also indicate that the two curves, with timing noise and without timing noise, converges at high signal-to-noise ratios as expected. The reason being that the probability of bit-error approaches zero for both cases at high signal-to-noise ratios.

At signal-to-noise ratio below 2.2 dB, the phase-lock-loop starts to lose lock. Since bit-synchronization information is not obtainable beyond this point, data obtained beyond this point is useless.

Tests were also performed using phase-locked-loops of comparatively wider noise-bandwidth. This was accomplished by replacing the 87 μf capacitor of the loop filter by a smaller capacitor. The degradation of performance of the PSK demodulator was almost undetectable for a small increase of

the noise-bandwidth.

From the results of the performance tests, it is concluded that the calculated performance curves, for both cases (timing noise present and not present) are accurate for all practical purposes. Furthermore, the degradation of performance due to timing noise is small. Therefore, the assumption that the effect of timing noise is negligible is valid. Thus in the design of PSK communication systems, the ideal case serves a good approximation especially if a safety factor is used.

CITED REFERENCES

1. J. M. Wozencraft, I. M. Jacobs, Principles of Communication Engineering, John Wiley & Sons, New York, 1965, p. 250.

2. W. C. Lindsey, "Phase-Shift-Keyed Signal Detection With Noisy Reference Signals", IEEE Trans. on Aerospace and Electronic Systems, Vol. AES-2, No. 4, July 1966, pp. 393-401.

3. P. R. Karr, "The Effect of Phase Noise on the Performance of Bi-Phase Communication Systems", SWIEEECO Record, April 1967.

4. S. Riter, "Signal Design for a Coded Communication System", Doctoral Dissertation, University of Houston, Houston, Texas, June 1968.

5. R. Jaffe, E. Rechtin, "Design and Performance of Phase-Locked Circuits Capable of Near-Optimum Performance Over a Wide Range of Input Signal and Noise Levels", IRE Trans. - Information Theory, IT-1. March 1955, pp. 66-76.

6. R. C. Martin, M. E. Mitchell, L. D. Rudold, "Phase-Inversion Tolerant Coding for PSK Data Links," IEEE Trans. on Communication Technology, CS-12, No. 2, June 1964, p. 206.

7. F. M. Gardner, S. Kent, Theory of Phase Lock Techniques, Prentice-Hall, 1967, pp. 6-10.

8. F. J. Charles, W. C. Lindsey, "Some Analytical and Experimental Phase-Locked-Loop Results for Low Signal-to-Noise Ratios", Proc. of the IEEE, Vol. 54, No. 9, Sept. 1966, pp. 1152-1166.

9. J. M. Wozencraft, I. M. Jacobs, op.cit. pp. 250-252.

10. W. C. Lindsey, loc. cit.

11. S. Riter, loc. cit.

12. S. W. Golomb, J. R. Davey, I. S. Reed, H. L. Van Trees, J. J. Stiffler, "Synchronization", IEEE Trans. on Communication Systems, Vol. CS-11, Dec. 1963, pp. 481-491.

13. J. J. Stiffler, "On the Allocation of Power in a Synchronous Binary Communication System", Proc. of National Tele. Conf., June 1964.

14. S. W. Golomb, L. D. Baumert, M. F. Easterling, J. J. Stiffler, A. J. Viterbi, Digital Communication With Space Application, Prentice-Hall, 1964, p. 125.

15. S. Riter, loc. cit.

16. A. Papoulis, Probability, Random Variable and Stochastic Processes, McGraw-Hill Book Co., New YOrk, 1965, p.67.

BIBLIOGRAPHY

Charles, F. J., W. C. Lindsey, "Some Analytical and Experimental Phase-Locked Loop Results for Low Signal-to-Noise Ratios", Proceedings of the IEEE, Vol. 54, No. 9, Sept. 1966, pp. 1152-1166.

Golomb, S. W., L. D. Baumert, M. F. Easterling, J. J. Stiffler, and A. J. Viterbi, Digital Communication With Space Application, Prentice-Hall, 1964.

Golomb, S. W., J. R. Davey, I. S. Reed, H. L. Van Trees and J. J. Stiffler, "Synchronization", IEEE Trans. on Communication Systems, Vol. CS-11, Dec. 1963, pp. 481-491.

Jaffe, R., E. Rechtin, "Design and Performance of Phase-Lock Circuits Capable of Near-Optimum Performance Over a Wide Range of Input Signal and Noise Levels", IRE Transactions-Information Theory, IT-1, pp. 66-76, March 1955.

Karr, P. R., "The Effect of Phase Noise on the Performance of Bi-Phase Communications Systems", SWIEEECO Record, April, 1967.

Lindsey, W. C., "Phase-Shift-Keyed Signal Detection With Noisy Reference Signals", IEEE Trans. on Aerospace and Electronic Systems, Vol. AES-2, No. 4, July 1966, pp. 393-401.

Martin, R. C., M. E. Mitchell, and L. D. Rudold, "Phase-Inversion Tolerant Coding for PSK Data Links", IEEE Trans. on Communication Technology, Vol. CS-12, No. 2, June 1964, p. 206.

Papoulis, A., Probability, Random Variable and Stochastic Processes, McGraw-Hill Book Co., New York 1965.

Riter, S., "A Study of the Synchronization Problem for Coherent Phase Shift Keyed Signal", Doctoral Dissertation University of Houston, Houston, Texas, June 1968.

Stiffler, J. J., "On the Allocation of Power in a Synchronous Binary PSK Communication System", Proc. National Telemetering Conference, June 1964.

Wozencraft, J. M., I. M. Jacobs, Principles of Communication Engineering, John Wiley & Sons, New York, 1965.

APPENDIX A

MINIMUM DATA RECORDING TIME AT DIFFERENT BIT-ERROR-RATES

Accurate bit-error-rate can be obtained by recording the data for a long period of time. However, this is not feasible because it is time consuming. A minimum recording time can be calculated given the tolerance.

Let p be the bit-error-rate and n be the number of bits to be sampled (for detection of errors). It can be shown that, if n bits were sampled, the most probable number of errors detected would be np. It is desired to find the minimum value of n such that for n bits sampled, the actual number of bit errors detected K is different from np by less than 2 percent, the tolerance.

The probability that K lies within np (1±.02) is

$$P\{K\} = P\{np(.98) \leq K \leq np(1.02)\}$$

$$= \sum_{i=np(.98)}^{np(1.02)} \binom{n}{i} p^i (1-p)^{n-i}.$$

Using approximations[16],

$$P\{K\} = 2\,\mathrm{erf}\left(\frac{np(.02)}{\sqrt{np(1-p)}}\right).$$

Assuming that $P\{K\} = 0.95$ is high enough to be considered as a certain event. Then solving the inequality

$$2\text{erf}\left(\frac{np(.02)}{\sqrt{np(1-p)}}\right) \geq .95$$

gives the minimum value of n.

From the error function table, the solution is

$$\left(\frac{np(.02)}{\sqrt{np(1-p)}}\right) \geq 2.$$

Simplifying,

$$n \geq (10^4)(1-p)/p.$$

At low bit-error rates,

$$(1-p) \approx 1.$$

Therefore,

$$n \geq (10^4)/p.$$

The minimum value of n and the minimum data recording time (n/f_b) is listed in Table 1. for different bit-error-rates.

p	n (bits)	n/f_b (sec.)
$1(10^{-4})$	$1(10^{8})$	1780
$5(10^{-4})$	$2(10^{7})$	356
$1(10^{-3})$	$1(10^{7})$	178
$5(10^{-3})$	$2(10^{6})$	36
$1(10^{-2})$	$1(10^{6})$	18
$5(10^{-2})$	$2(10^{5})$	4
$1(10^{-1})$	$1(10^{5})$	2

Table 1. Minimum Data Recording Time at Different Bit-Error-Rates (tolerance = ± 2%).

APPENDIX B

PSK SIGNAL GENERATOR CIRCUIT DIAGRAMS

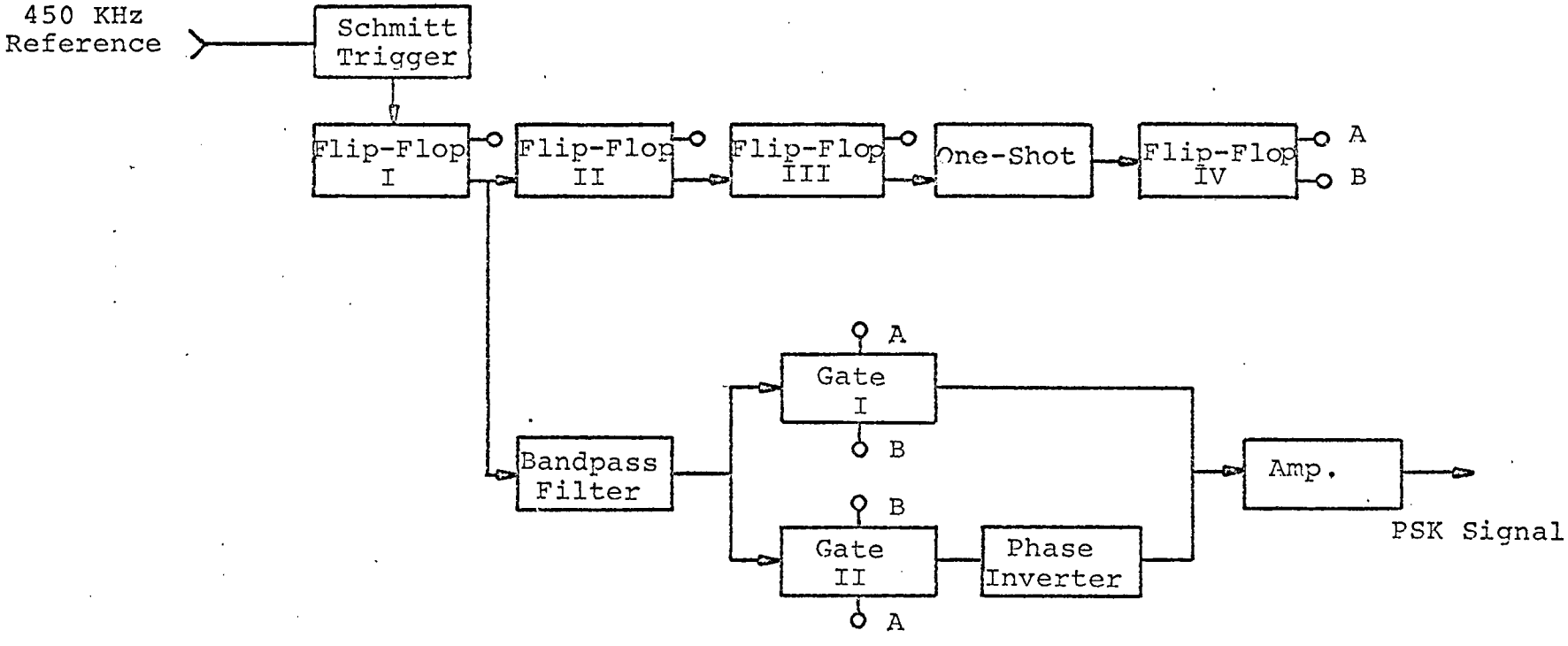


Figure 16. PSK Signal Generator Block Diagram

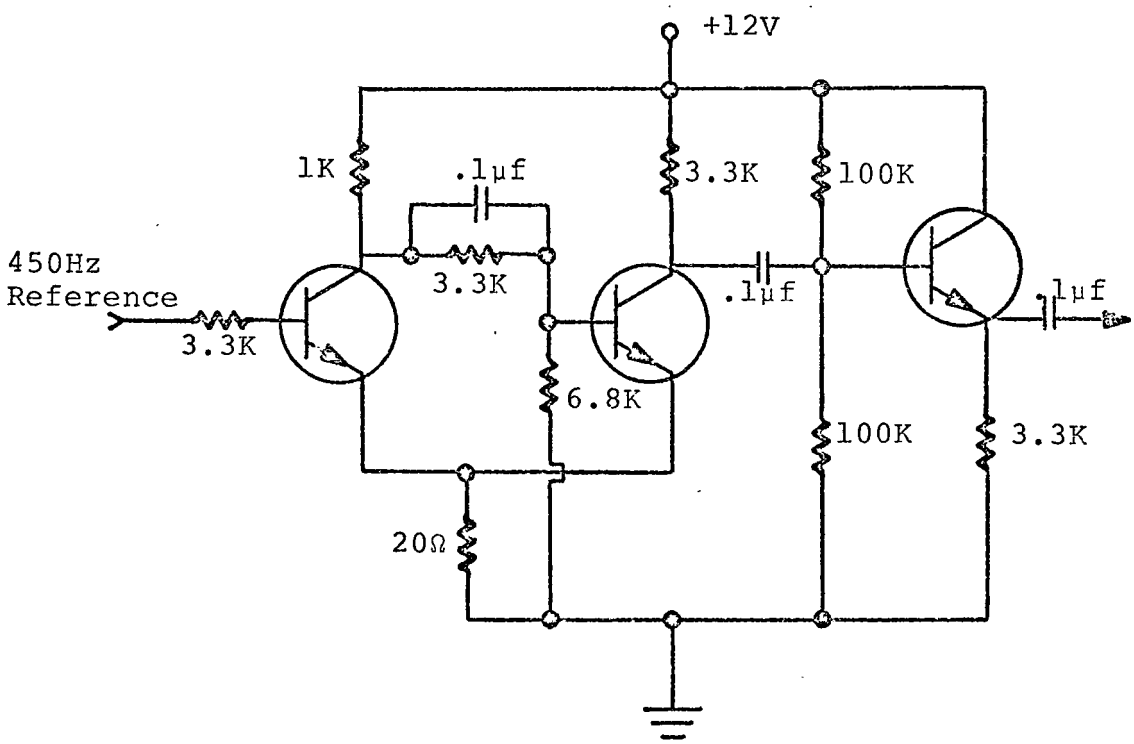


Figure 17. Schmitt Trigger

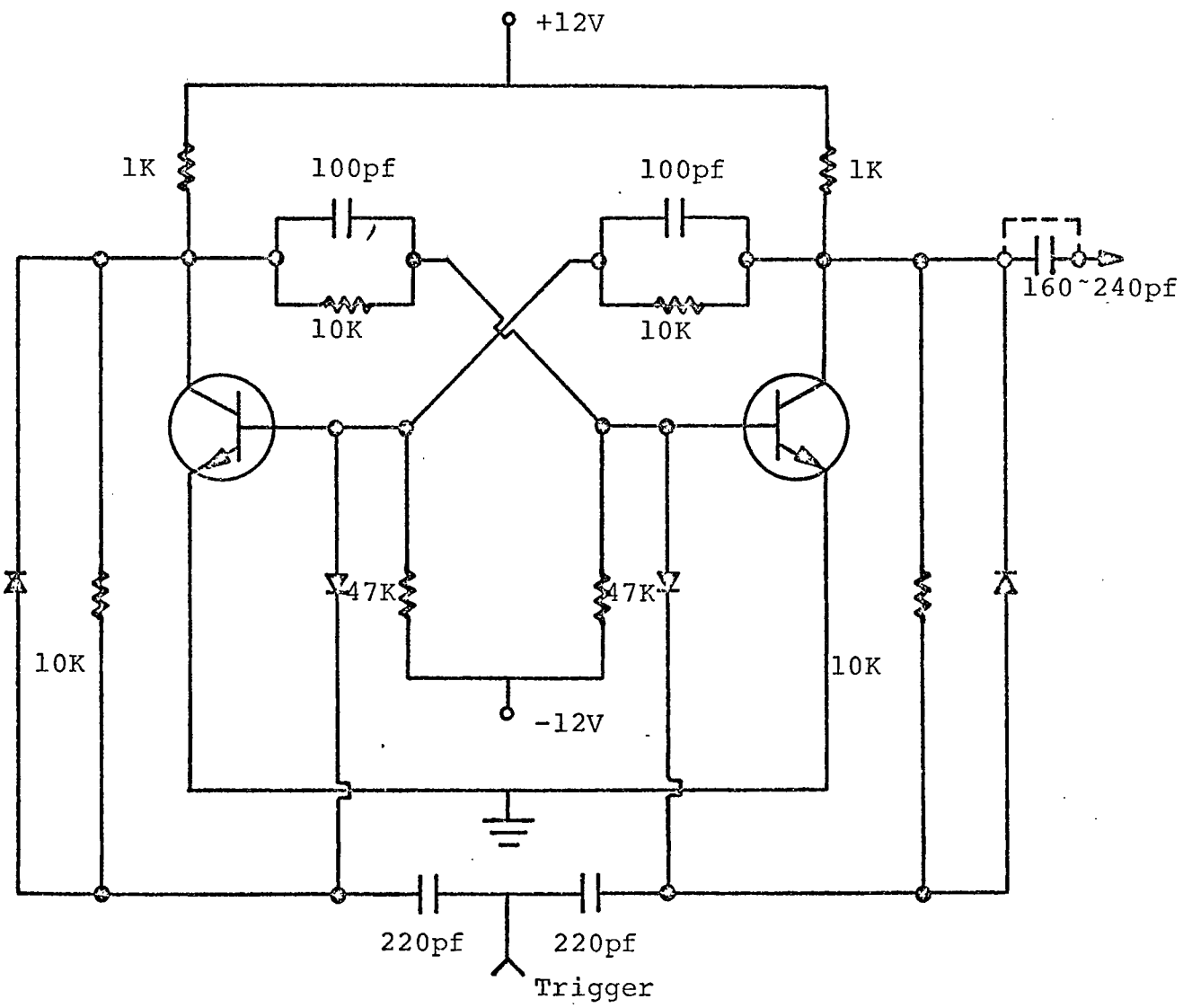


Figure 18. Flip-Flop I, II and III

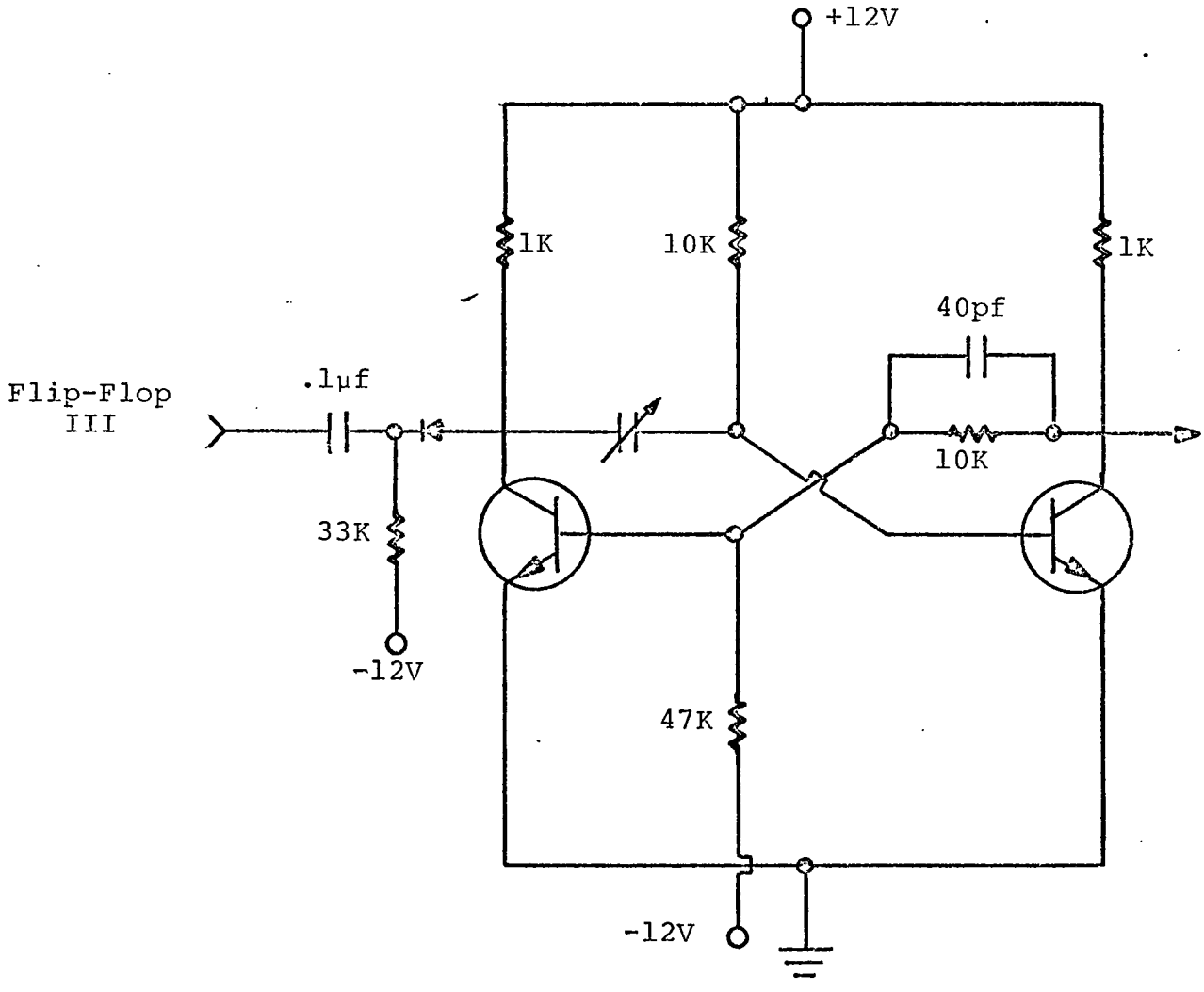


Figure 19. One-Shot Time Delay Circuit

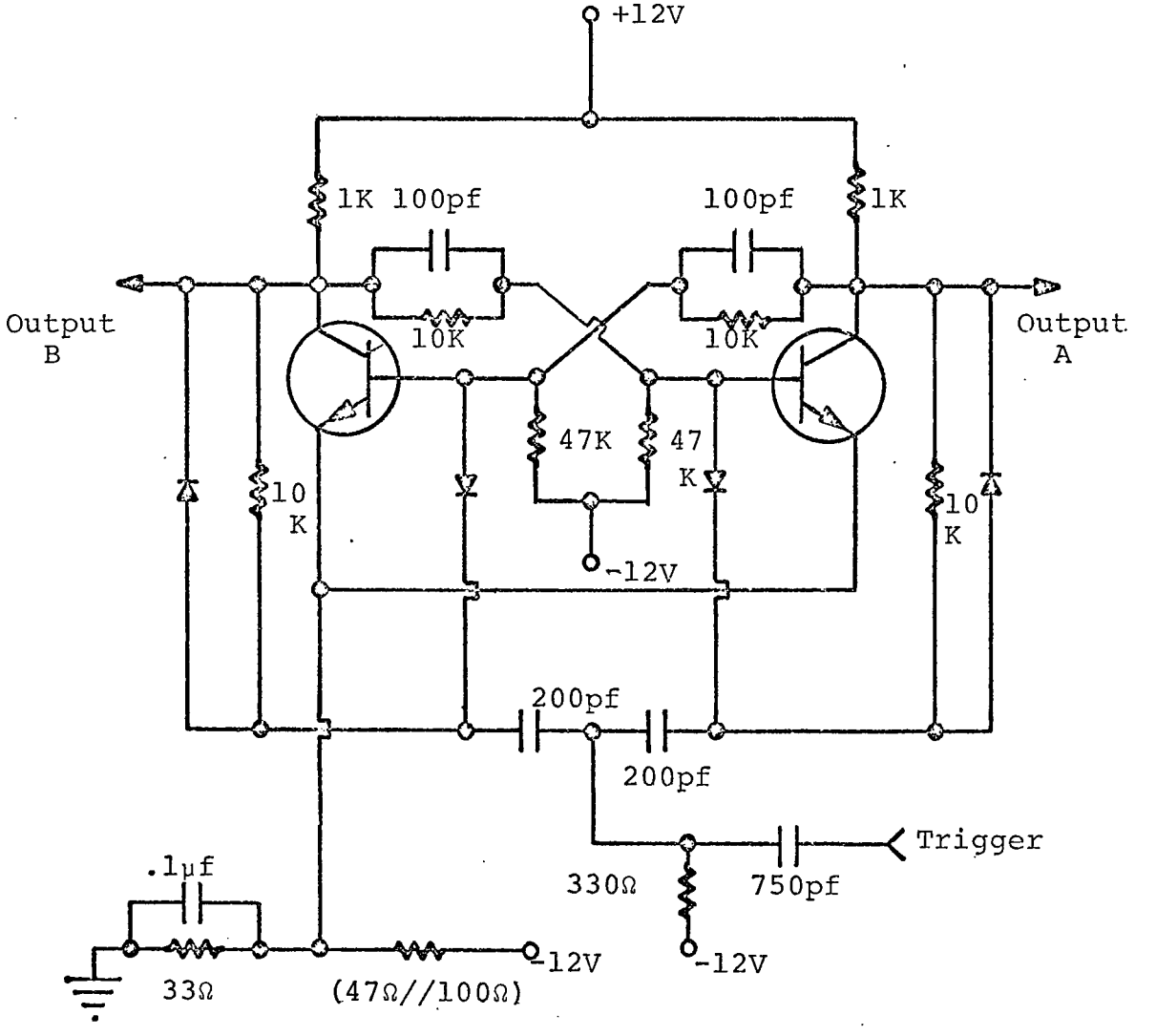
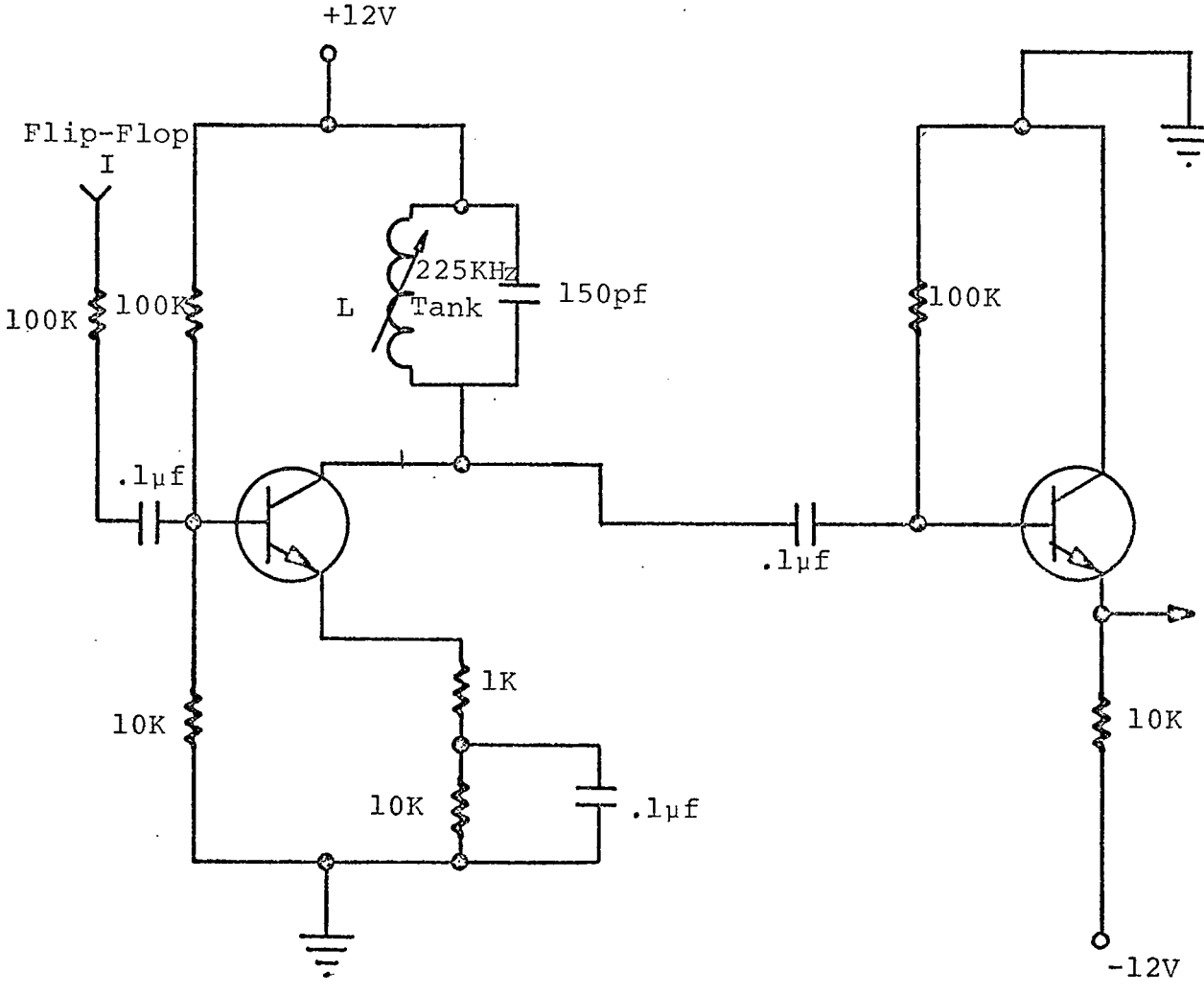


Figure 20. Flip-Flop IV



L = Miller 9003 -
.57~2.8

Figure 21. 225 kHz Band-Pass Filter

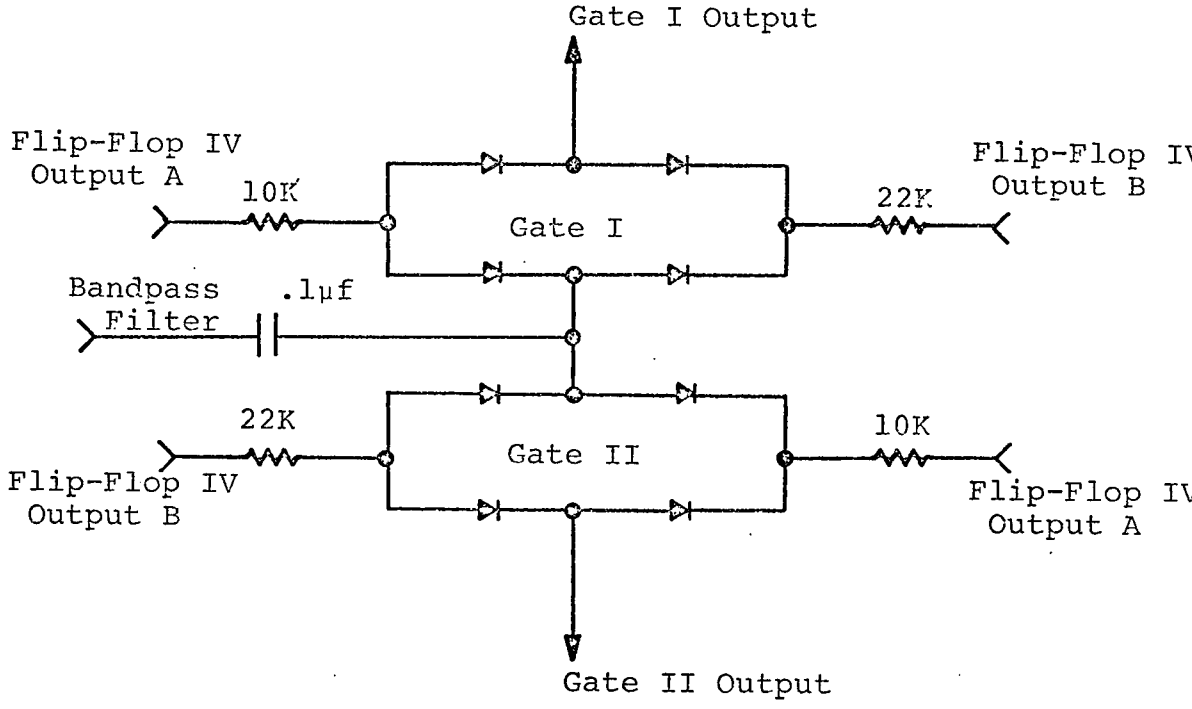


Figure 22. Sampling Gates

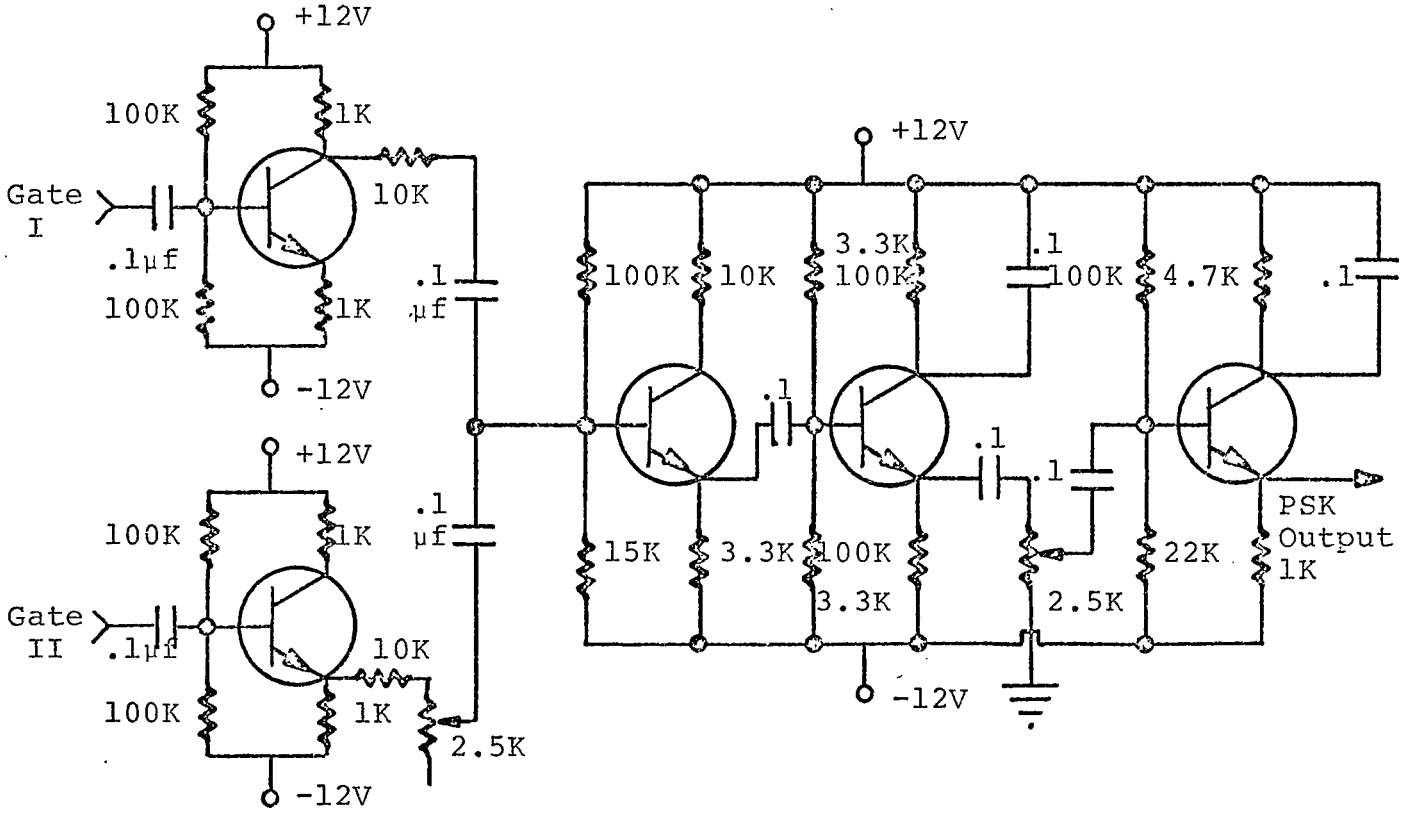


Figure 23. Inverter and Buffer Amplifier

APPENDIX C

SIMULATED CHANNEL CIRCUIT DIAGRAM

Figure 24. Simulated Channel Circuit Diagram.

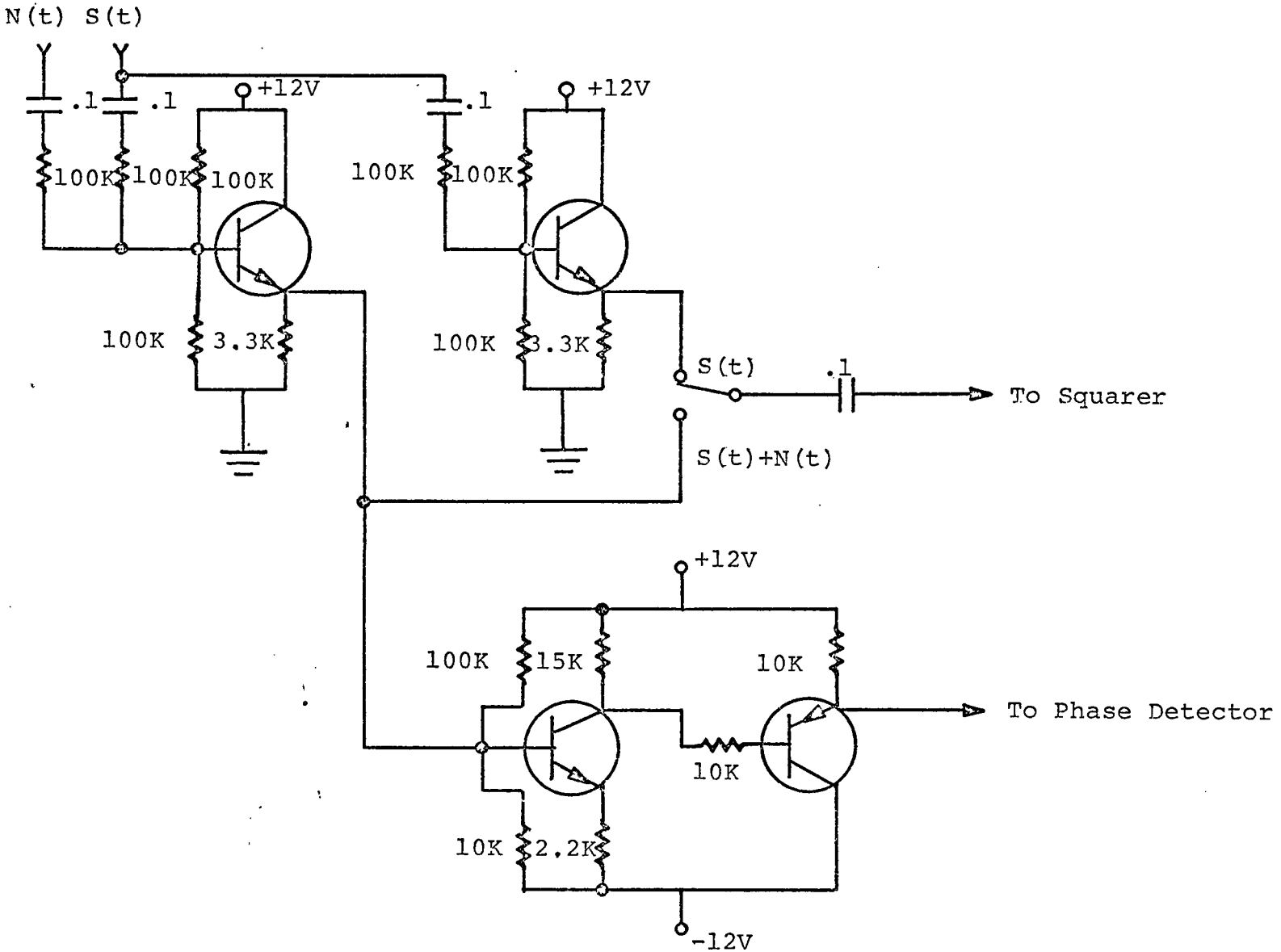


Figure 24. Simulated Channel Circuit Diagram

APPENDIX D

SQUARING LOOP PSK DEMODULATOR CIRCUIT DIAGRAMS

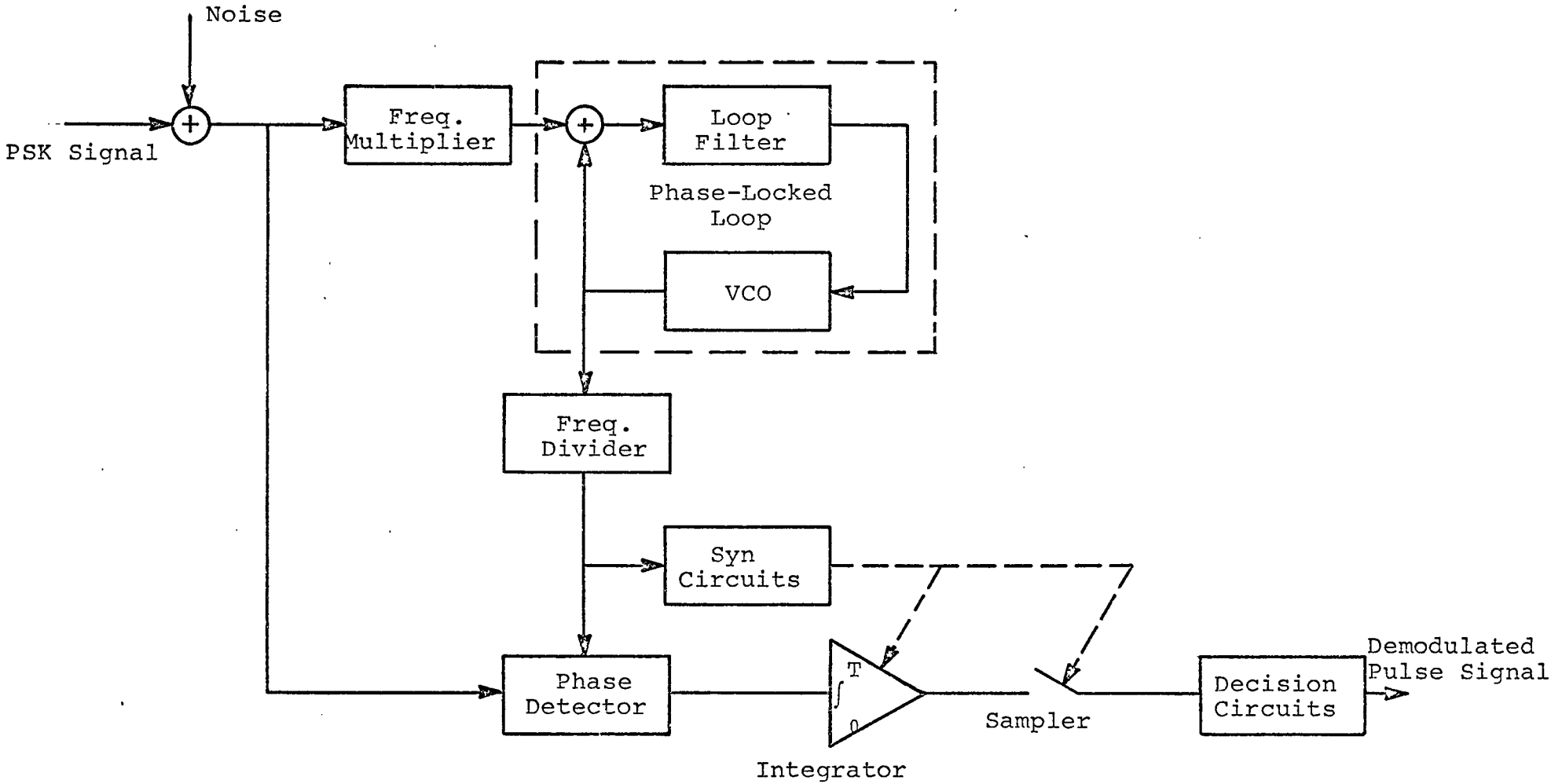


Figure 25. Squaring Loop PSK Demodulator Block Diagram

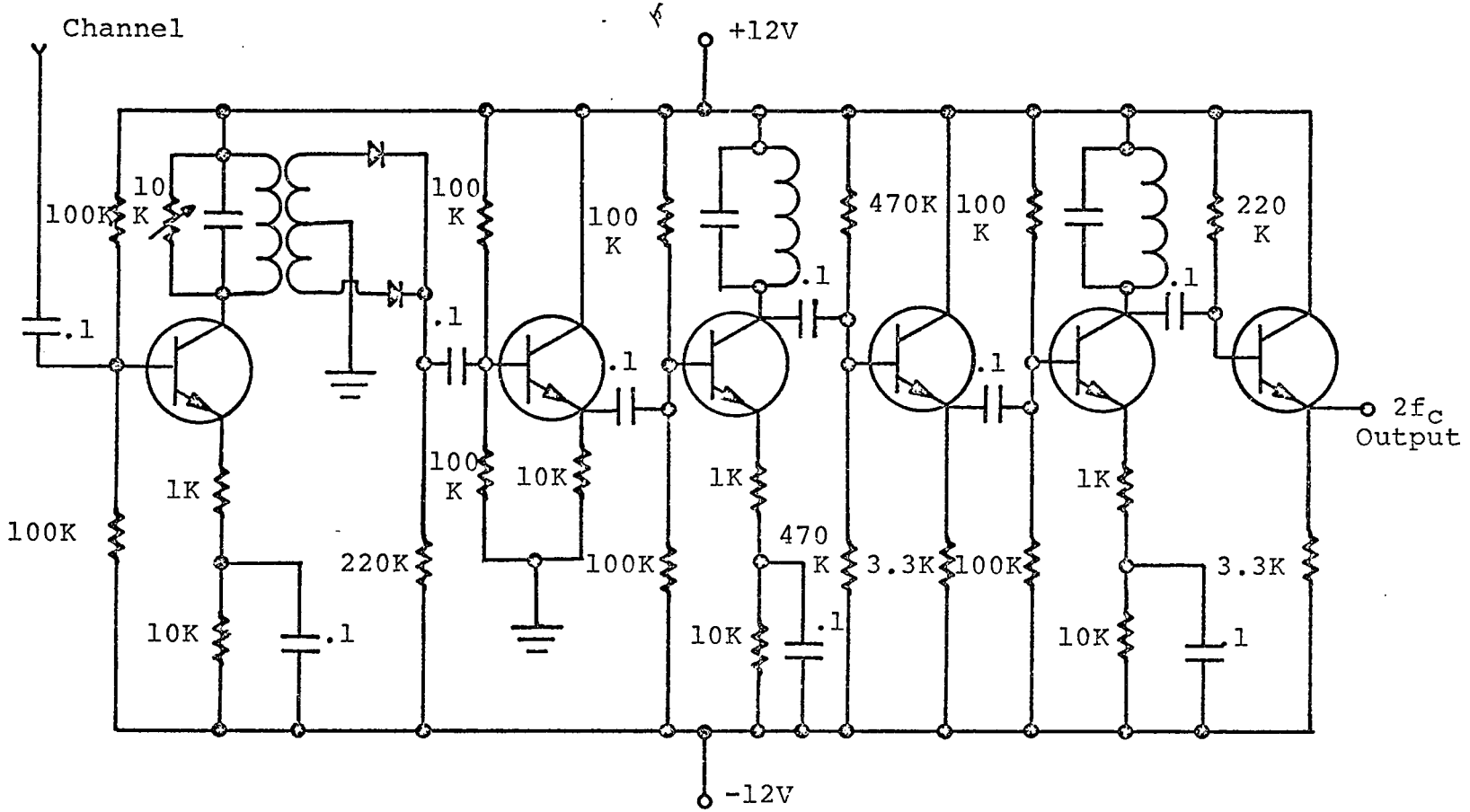


Figure 26. Squarer (Frequency Doubler)

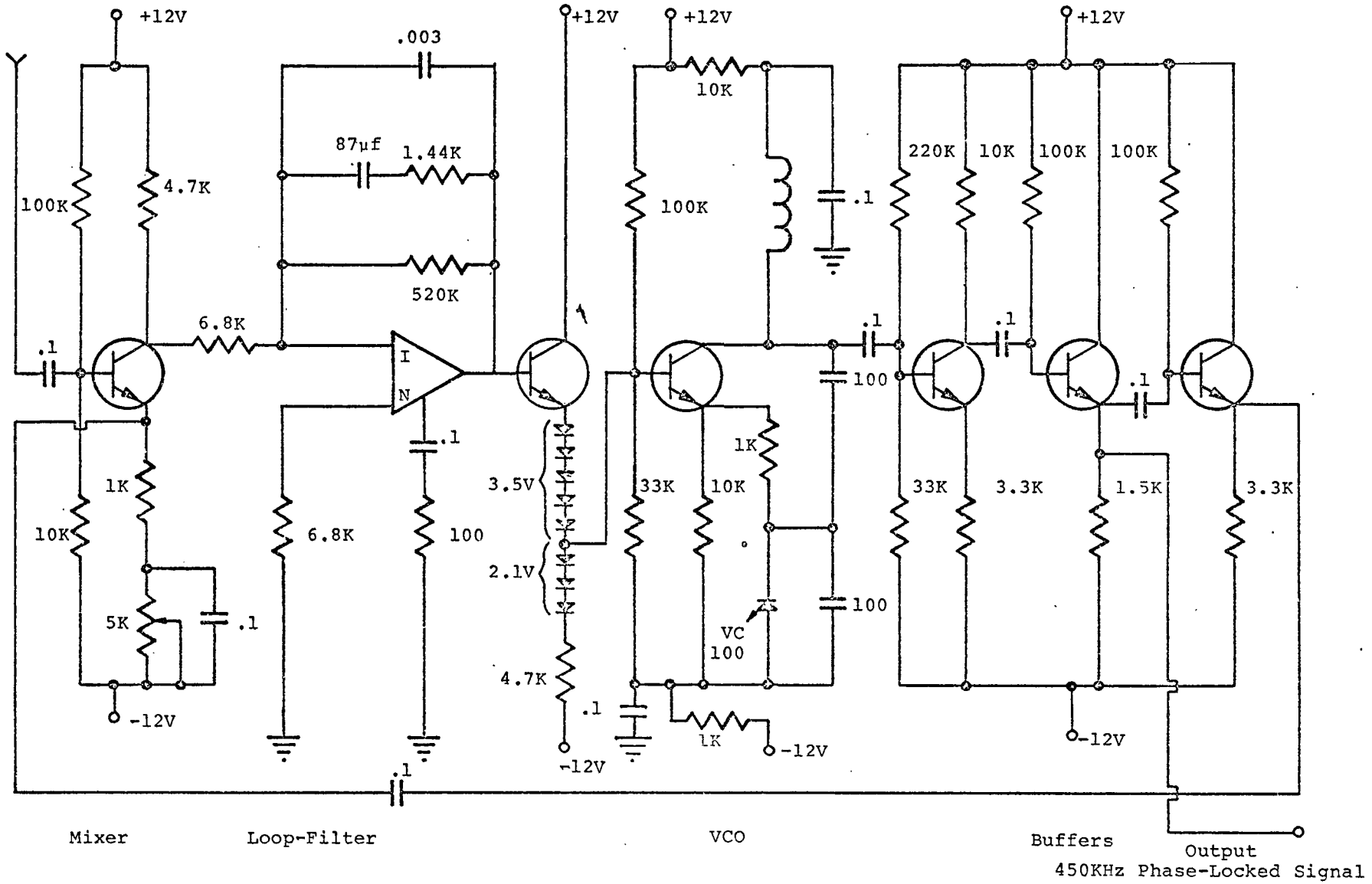


Figure 27. Phase-Locked Loop

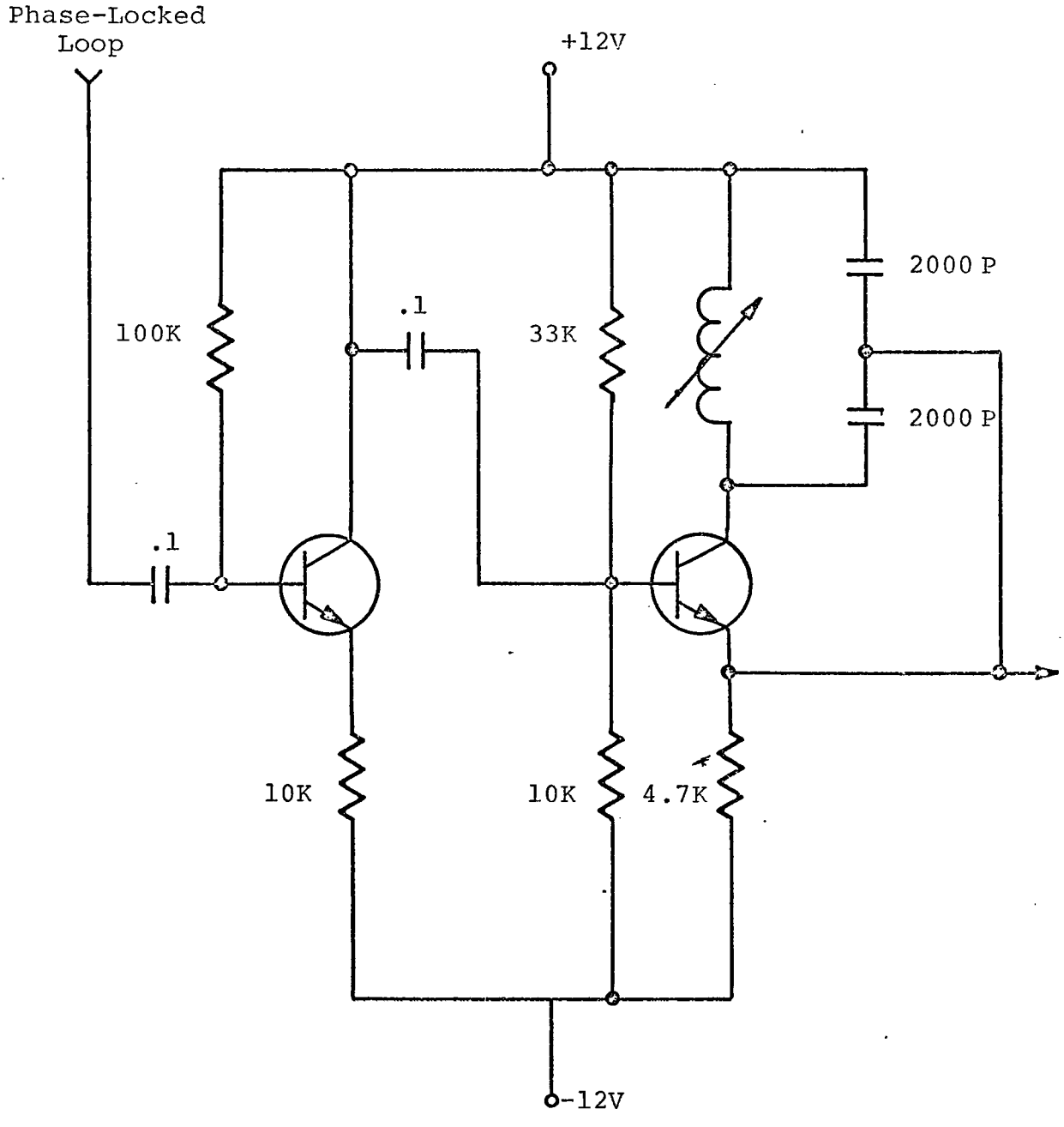


Figure 28. Tuned Oscillator Frequency Divider

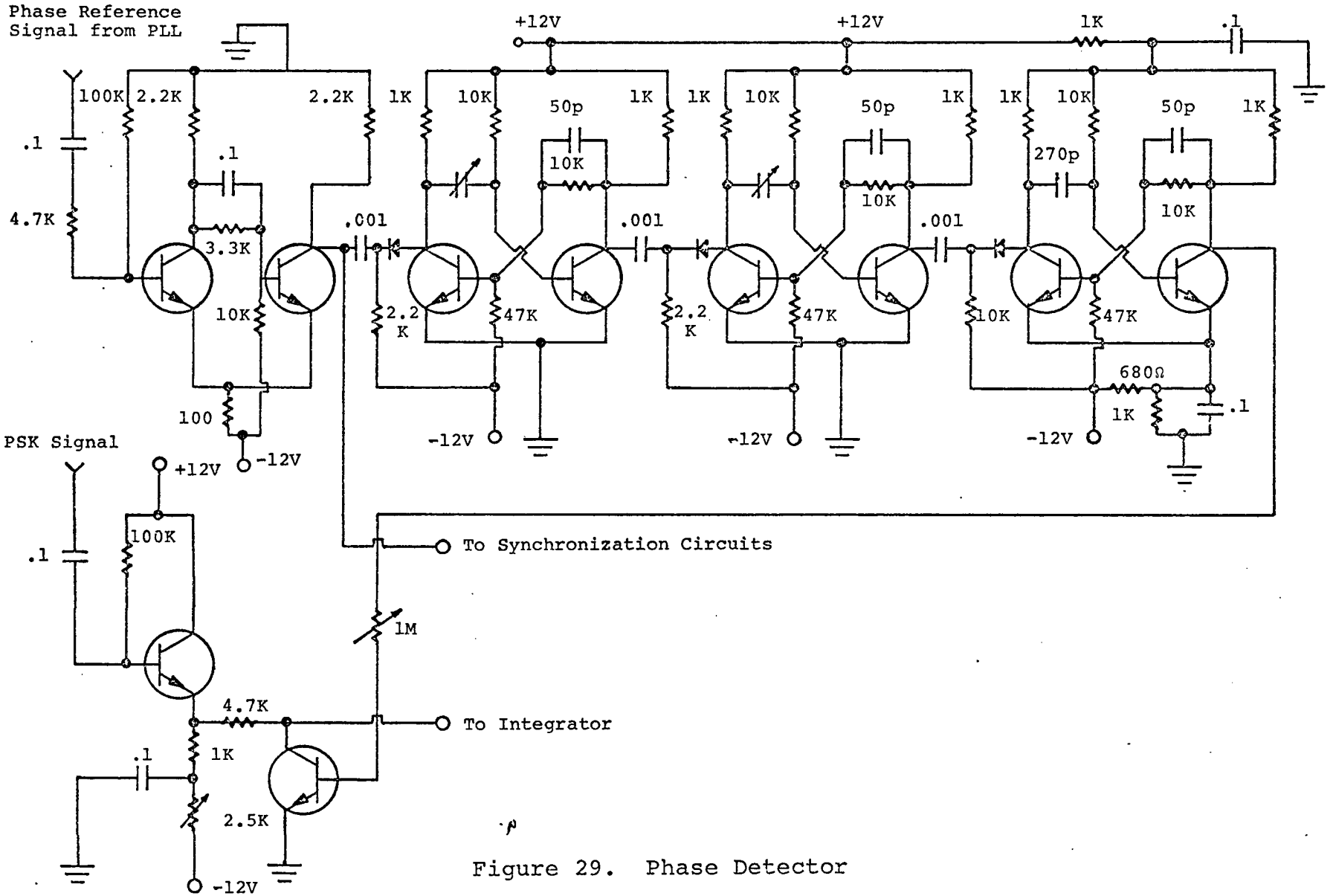


Figure 29. Phase Detector

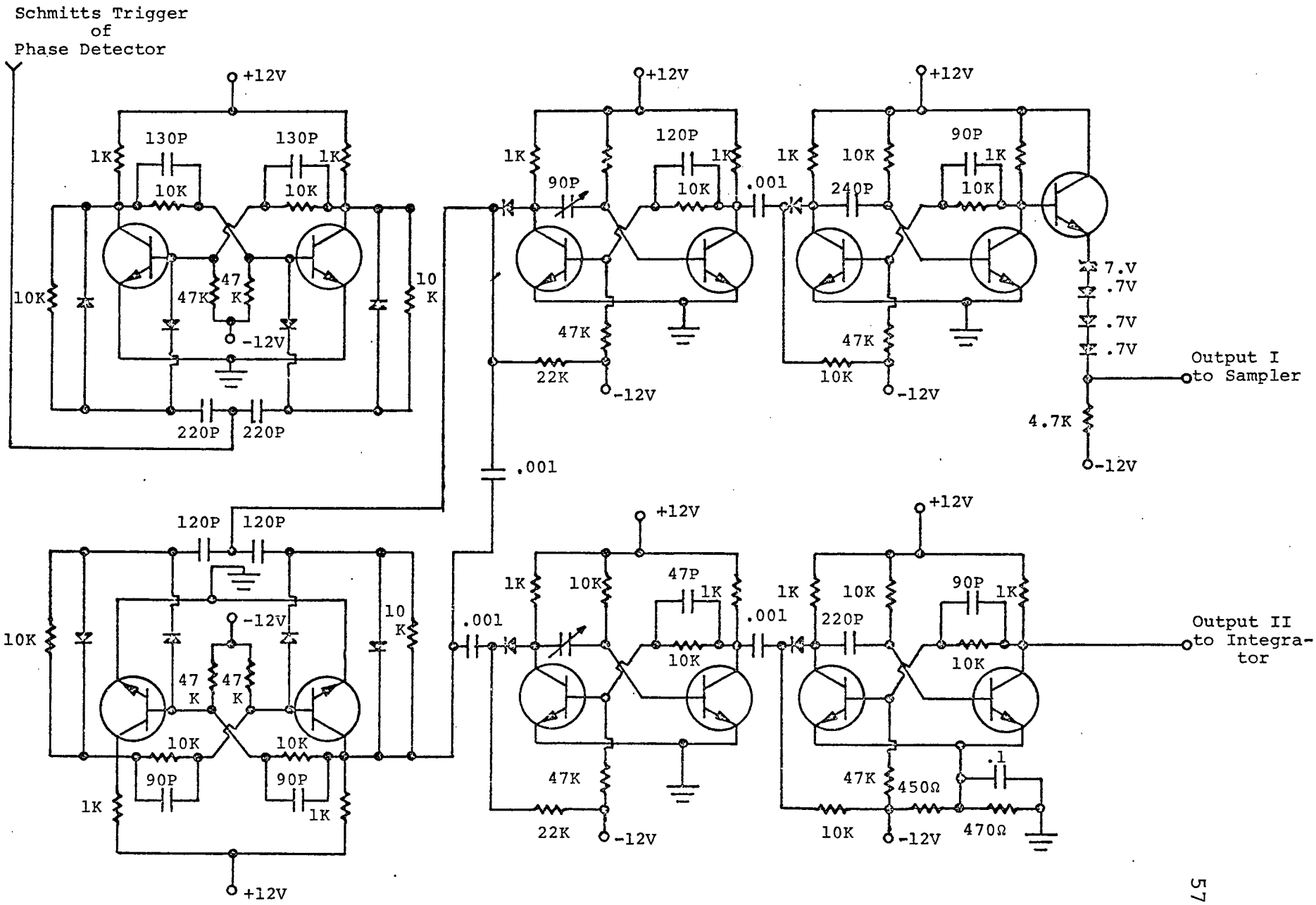


Figure 30. Bit Synchronization Circuit

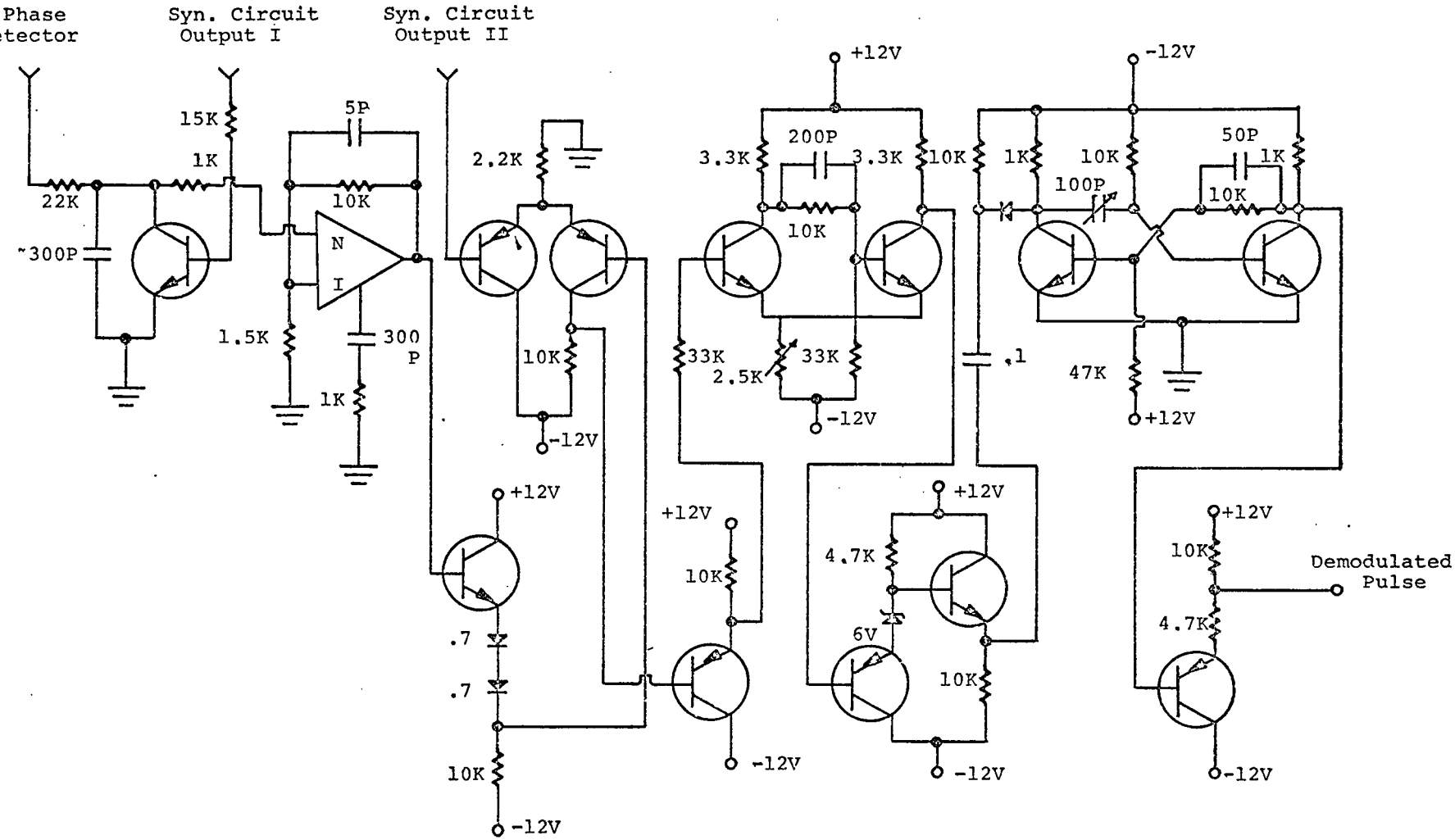


Figure 31. Integrator, Samples and Decision Circuits

APPENDIX E

ERROR DETECTOR CIRCUIT DIAGRAMS

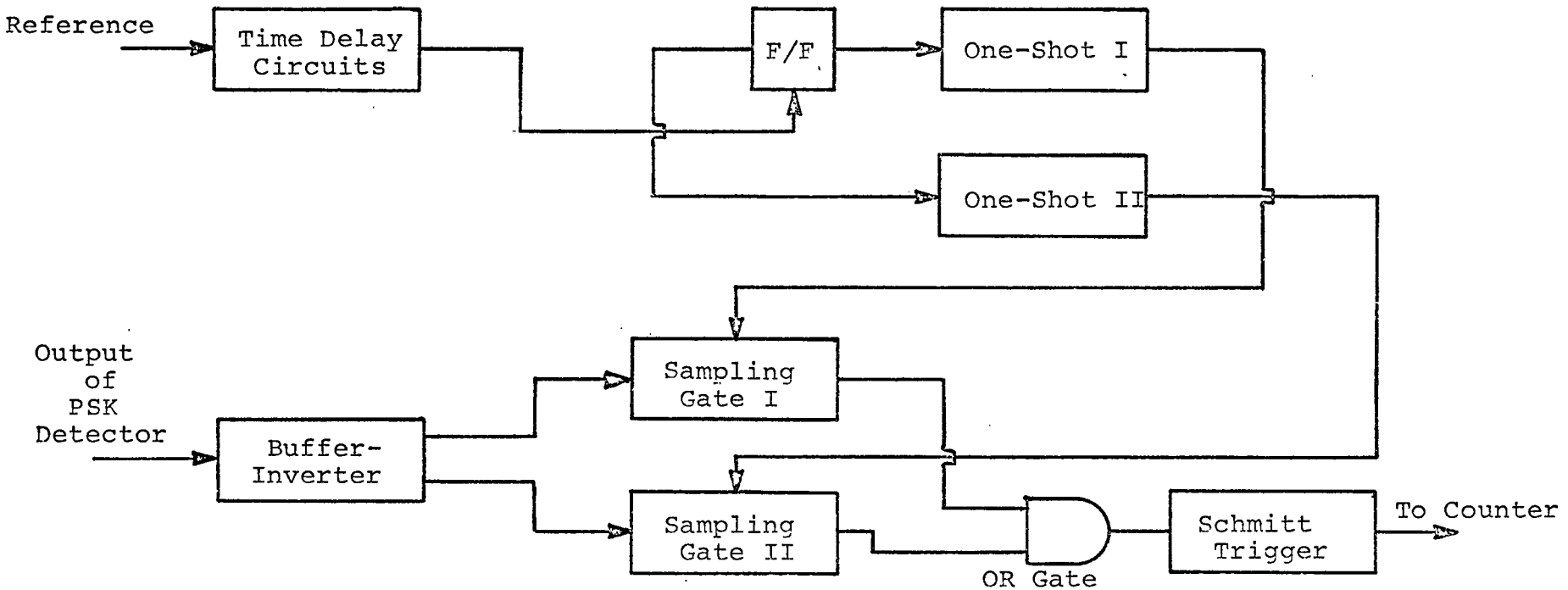


Figure 32. Error Detector Block Diagram

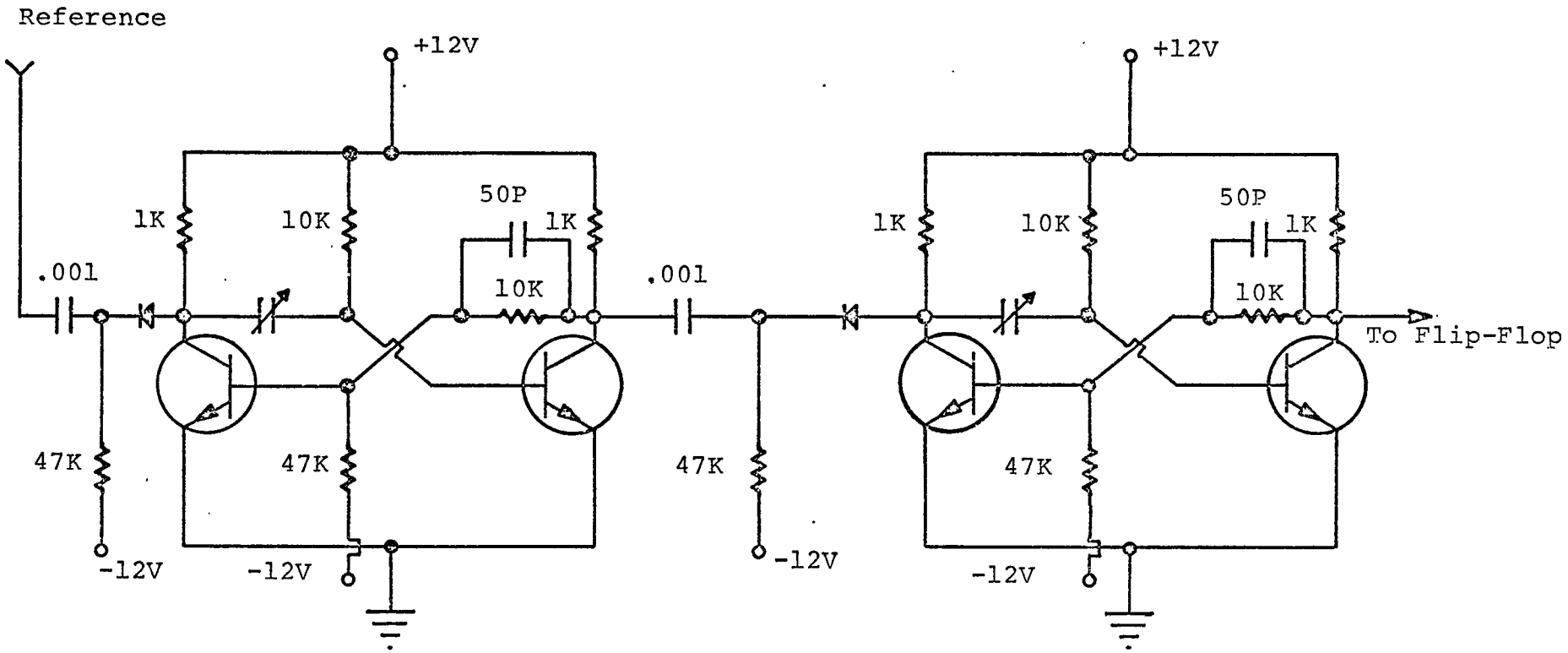


Figure 33. Adjustable Time Delay Circuit

Time Delay Circuit

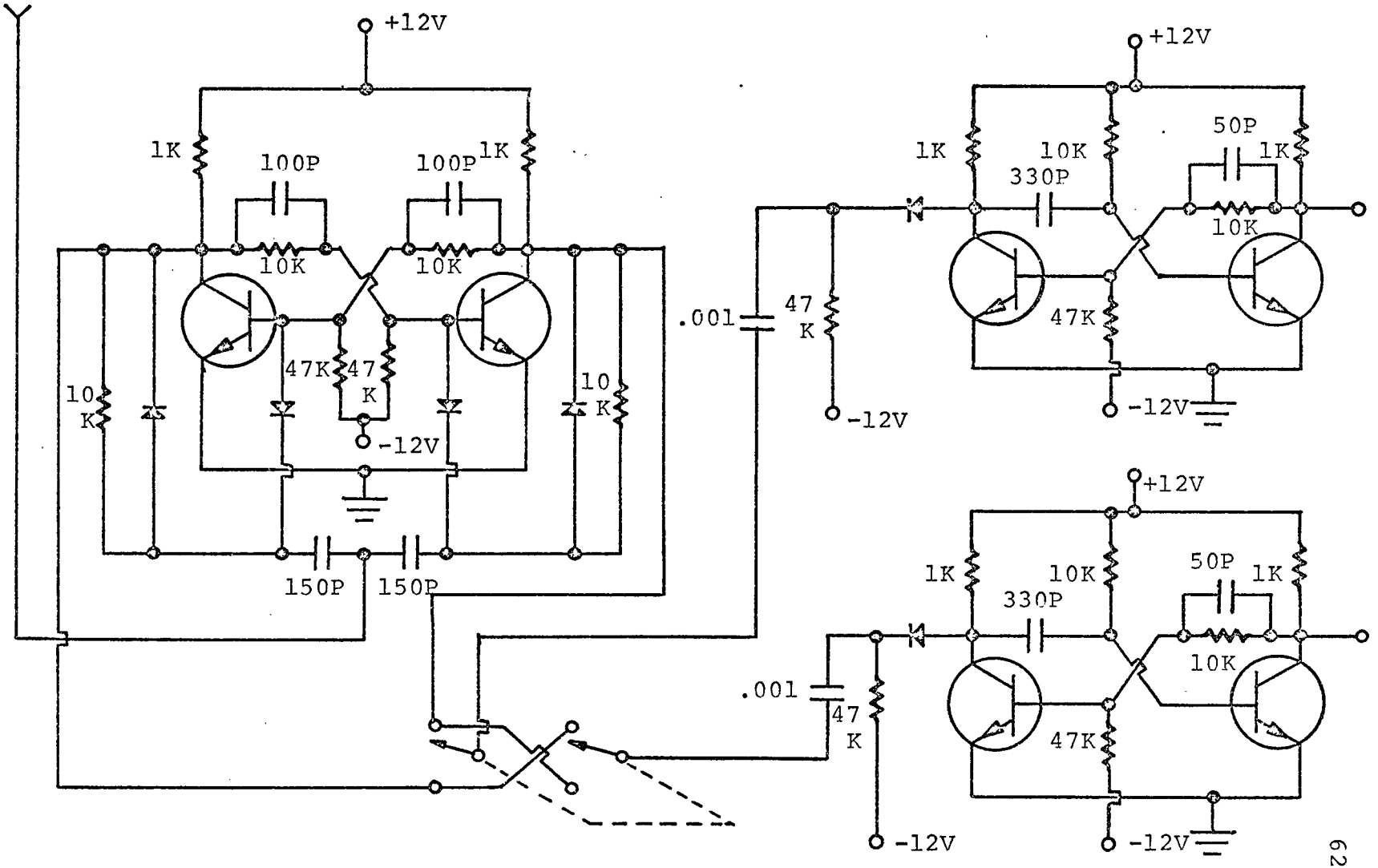


Figure 34. Flip-Flop and One-Shot Circuits

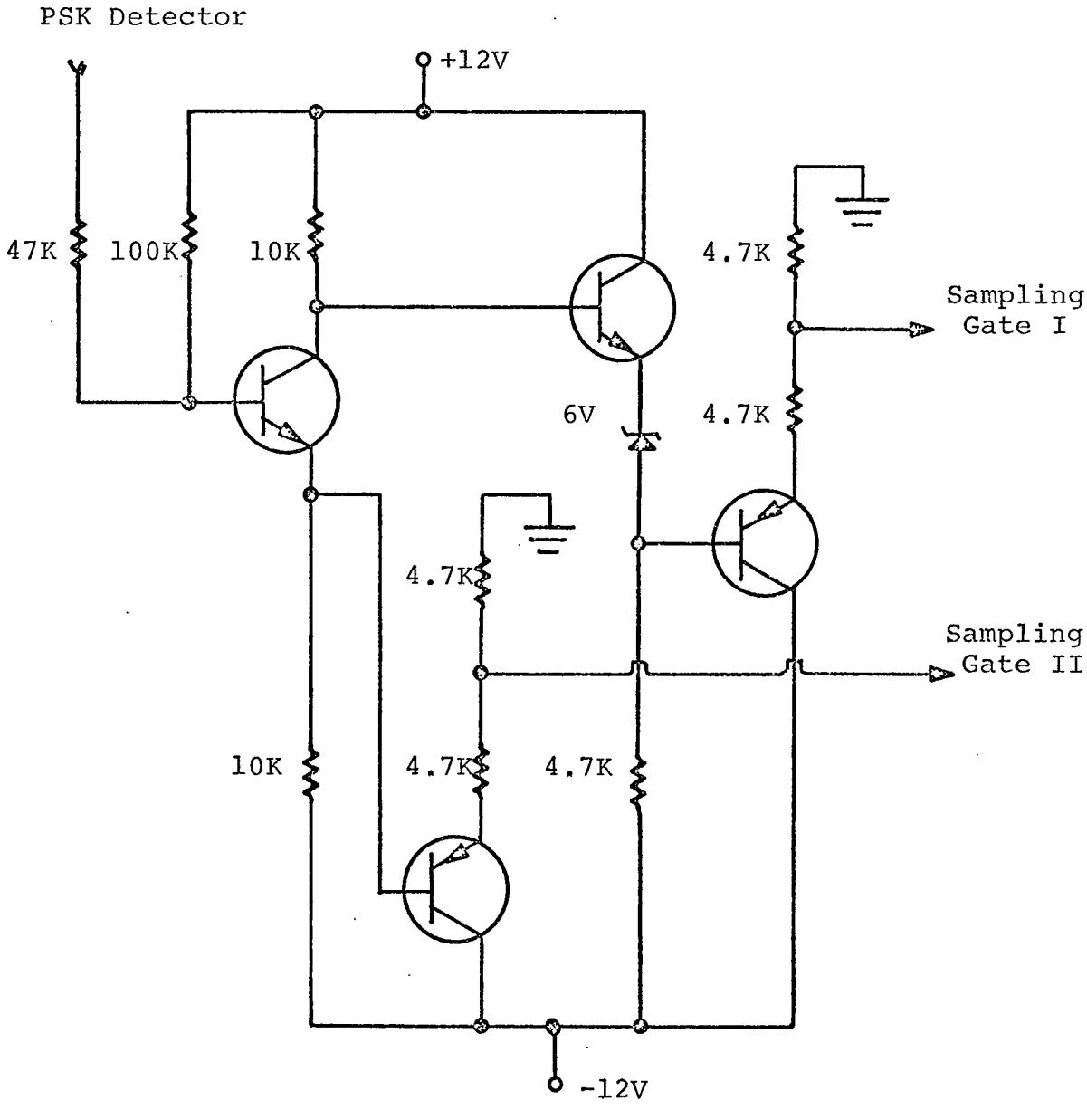


Figure 35. Buffer-Inverter Circuit

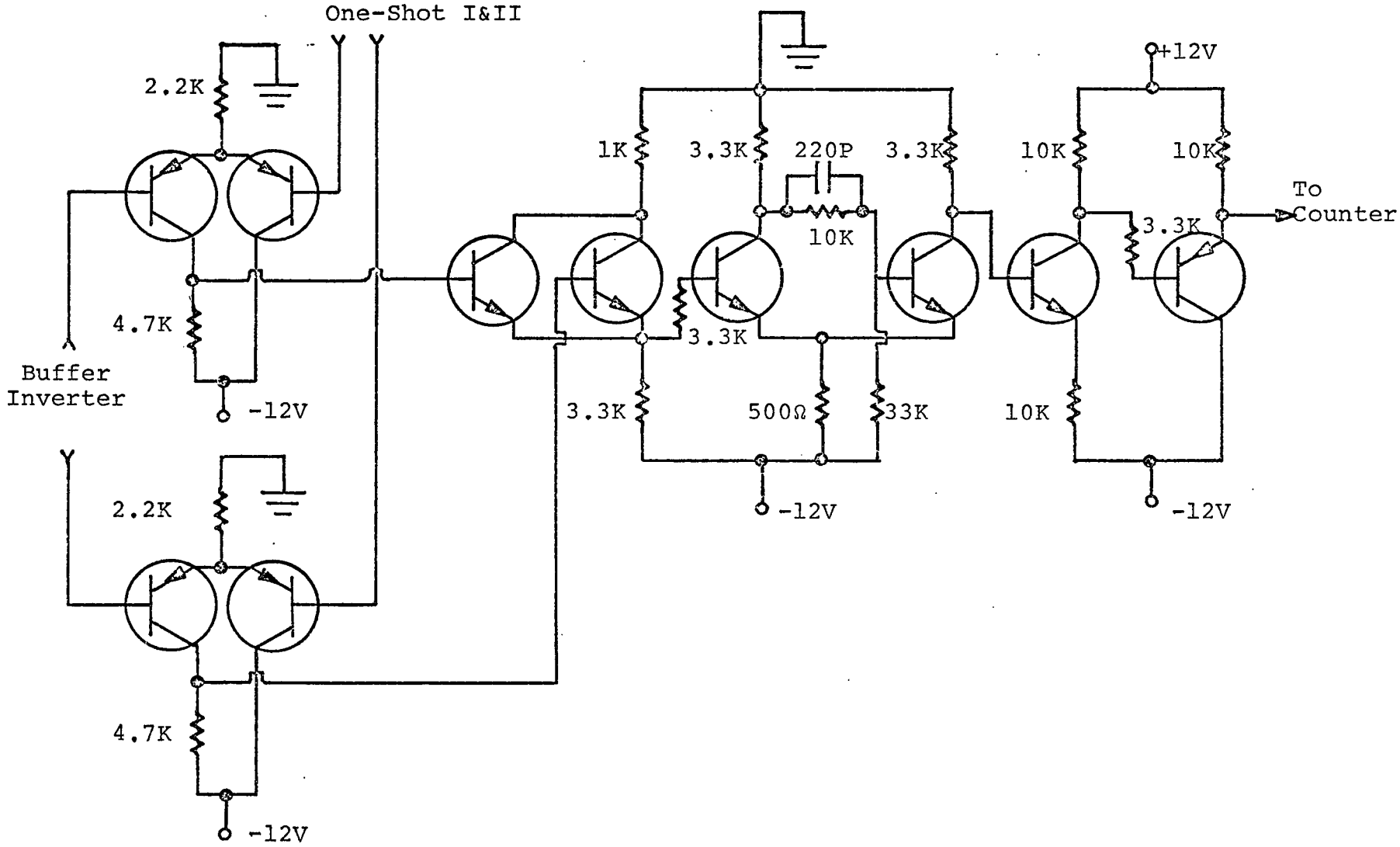


Figure 36. Sampling Gates, Or-Gate and Schmitt Trigger