DC/DC Converters with High Power Density and Fast Response for Pulsed Load Applications

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ABSTRACT

As a special kind of load that requires periodic high power bursts, pulsed loads are widely being powered using solid state converters in various modern applications, such as radar, nuclear magnetic resonance imaging (NMR), light detection and ranging (Lidar), etc. The related power converters need to handle the following three conditions: 1) high peak to average power ratio (PAPR); 2) small duty ratios under peak power; and 3) fast pulse rise and fall times. With the additional requirement of high power density in modern space-constrained applications, these bring several challenges in the design of such 'pulsed power supplies' or PPSs.

In applications involving voltages up to 900 V, Gallium Nitride (GaN) devices are increasingly being preferred due to their advantages over Silicon Carbide (SiC) and Silicon (Si) devices. For example, GaN devices' lowest switching loss helps the PPSs to operate in higher switching frequencies, which increases converters' response speeds and reduces the size of the passive components. This dissertation bridges the use of GaN devices with new converter architectures and control techniques to improve the power density and response speed of PPSs.

First, design and development of a high power density 375 V input, 50 V output, two stage GaN based DC/DC converter prototype for 4 kW/800 W (peak/average) pulsed load application is discussed, along with its hardware, in this dissertation. By the benefits of lower switching loss, the first stage isolated converter can operate in a higher frequency to reduce transformer size. Higher switching frequency of 1 MHz also contributes to a high bandwidth of the second non-isolated converter stage, which

improves the transient performance. A novel average current control strategy has been proposed and applied in this PPS, which reduces the input current noise at pulse repetition frequency (PRF), and, therefore, reduces the input filter size and power rating. Some practical issues, such as the failure of zero voltage switching (ZVS) during light load, voltage ringing caused by GaN devices with small C_{oss}, and the limit of DSPs' processing speed, have also been discussed in this two stage converter. Solutions to these problems have been proposed and verified via experiment results.

A novel power converter architecture that can be applied in pulsed NMR applications such as in subsea or downhole formation evaluation has been proposed and verified in this dissertation. The proposed topology reduces the volume of the transformer, input filter, and midpoint capacitor due to a unique average power control strategy. A 150 V to 400 V, 20 kW peak power converter is designed. Simulation results, scaled-down experimental results, and design analysis are also provided in this dissertation to prove the validity of the proposed architecture.

Finally, a linear assisted DC/DC converter for PPSs to improve the response speed is also proposed in this dissertation. The main power is transferred by a highly efficient LLC resonant converter and the linear amplifier is responsible to compensate for the current difference during the load transients. The otherwise large output capacitor size gets reduced due to this converter's fast response speed. A 'band separation' solution is proposed and verified by simulation to deal with the practical issues arising from the parallel output connection between the LLC resonant converter and the linear amplifier.

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CHAPTER 1. INTRODUCTION

1.1. Introduction

Pulsed power applications widely appear in various fields of modern industry, such as particle accelerator, nuclear magnetic resonance (NMR) spectroscopy, radar, and 4G/5G communication system [1]-[4]. For example, radar transmitters are designed to periodically send short bursts of energy out at radio frequencies (RFs) so that the receivers can detect the targets by analyzing the echoes. The pulse repetition frequencies (PRFs) are typically in kilohertz level but the pulse durations are generally in microseconds [5]-[8]. This means that the peak power only occurs in a very small portion of the whole transmitting period. NMR spectroscopy also adopts pulsed power to periodically excite the magnetic field. The pulsed power rise and fall times are required to be tens or hundreds of nanoseconds [9]-[13]. Modern communication modulations, such as orthogonal frequency-division multiplexing (OFDM), also lead to a high peak to average power ratio (PAPR), which makes the transmitter operate in pulsed modes [14][15].

Based on the above-mentioned examples, it can be noticed that pulsed power applications have three main characteristics as follows: 1) high PAPR; 2) small duty ratios under peak power; and 3) fast pulse rise and fall times, which are very different from common power applications with relatively stable power demand. Therefore, the power supplies of these pulsed power applications are classified as a specific kind and popularly referred to as pulsed power supplies (PPSs). Unfortunately, the above three

characteristics bring several issues to the PPS designs, such as low efficiency and low power density.

1.2. Practical issues faced in the designs of the pulsed power supplies

As one of the main loads in the earlier discussed pulsed power applications, power amplifiers (PAs) must operate under very well-regulated supply voltages to ensure their performances of linearity and low noise, which proposes high requirements on the output voltage regulation of the PPSs.

The detailed output voltage regulation requirements of PPS are elaborated in Figure 1-1. The V_{ripple} is the inherent switching ripple of the switching power supply and $V_{undershoot}$/$V_{overshoot}$ is caused by the transient pulsed load on/off. Both parameters will insert noise to the PAs at power supply switching frequencies and PRFs respectively. V_{droop} is the voltage difference of average output voltage between the start and the end of a single pulse. Large V_{droop} harms the linearity of a PA as its voltage gain changes with the instantaneous supply voltage (also assumed as biasing voltage). Typically, -0.5 dB is the maximum acceptable voltage droop to avoid large signal distortion [16].

Figure 1-1 Ideal PPS output voltage waveform.

Two main methods can improve a switching power converter's voltage regulation performance. These are, i) increasing the switching frequency and ii) increasing the output filter size. However, simply increasing switching frequency or

output filter size results in serious power loss and low power density, which cannot meet the requirement of high efficiency and miniaturization in modern power converter designs. Therefore, a lot of research focused on the innovations of the power converter's structures and control methods to improve the output voltage regulations. The main existing techniques will be summarized in section 1.3.

On the other hand, since the peak power is only needed in very short duty ratios, these PPSs' power ratings are seriously over-designed, which causes massive cost loss and bulky converter sizes, especially for the switches, inductor, and transformer sizes. In addition, PRFs at such a high PAPR results in large amplitudes of PRF harmonics on the input side, which brings PRF noise to the other systems connected in the same DC bus. Since PRFs are generally in low frequencies (kilohertz level), they make the noise impact even worse and hard to filter out. A conducted emissions test standard (CE101) has been proposed to quantitatively limit the low frequency (LF) noise as shown in Figure 1-2 [17].

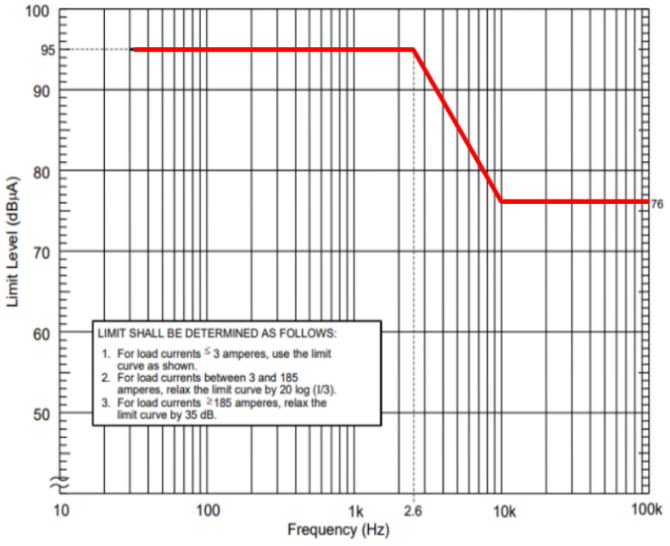


Figure 1-2 Conducted emissions test standard (CE101) for low frequency (LF) noise.

To meet the requirement of CE101, low pass filters with large capacitance and inductance values have to be used to filter out these LF harmonics. Besides, a PPS's input side is commonly a high voltage side, which means the components of the input filter need high voltage ratings. Therefore, total power density gets reduced further. In consideration that these pulsed power systems are typically applied in narrowly spaced environments, such as ships, underground logging tools, and base stations, the high power density is a very high priority demand on the PPSs designs. Section 1.3 will also introduce some converter topology designs that can improve the utilization rate of converters' power rating and reduce the input side LF harmonics to increase the power densities.

1.3. Converter architectures used in pulsed power supplies (PPSs)

Based on section 1.2, it can be concluded that the three main objectives in the PPSs design are: increasing the power densities, increasing power efficiencies and increasing the response speeds to the load transients. A significant amount of research has been done to achieve these objectives, based on the different architectures of power converters. The existing architectures can mainly be classified into four kinds as follow: 1) single stage PPS, 2) series connected two stage PPS, 3) parallel connected two stage PPS, and 4) active-controlled storage components PPS.

1.3.1. Single stage PPSs

The block diagram of single stage PPSs is shown in Figure 1-3. The types of the power conversion block in the diagram can be classified as linear power supply and switching power supply.

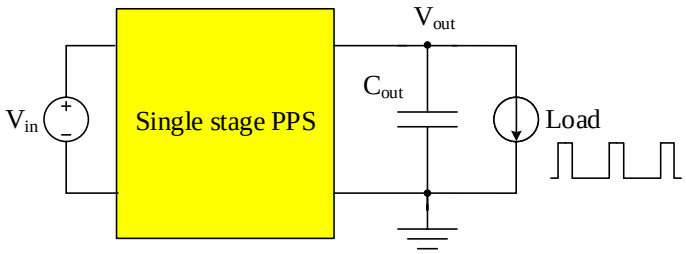


Figure 1-3 Block diagram of single stage PPSs.

Linear power supplies force the power FETs operating in the saturation region to continuously conduct the power. Since there is no switching behavior, the linear power supplies can achieve extremely low noise and excellent output voltage regulations. However, due to the operation in the saturation region, all the voltage difference between V_{in} and V_{out} is added to the power FETs which produces massive power loss and limits the output power range. A lot of low-dropout regulators (LDOs) have been investigated to improve the efficiency [18][19], but their output current and voltage level still cannot fit the high power high voltage pulse power applications.

Switching power supplies adopted in the block diagram of Figure 1-3 can be a buck converter, boost converter, LLC resonant converter, phase shift full bridge (PSFB) converter, or any other types of switching power converter (If not specified mentioned, power converter stands for switching power converter in the remaining part of this dissertation). A certain type of power converter is chosen depending on the specific functional requirements of the PPS, such as voltage stepping down/up and isolated/non-isolated. However, since there is only one stage, all these power converters have to switch in high frequencies or adopt bulky output filters to achieve great voltage regulations, which causes low efficiency and low power density as discussed in section 1.2. Another problem is that the single stage doesn't have any ability of energy

buffering, which means almost all pulsed load power will be reflected to the input side in real-time. Then, the large LF harmonics will appear on the input side and bulky input filters have to be adopted to reduce the harmonics.

1.3.2. Series connected two stage PPSs

The block diagram of series connected two stage PPSs is shown in Figure 1-4. The benefit of using a two-stage structure is that stage I can step down the high input voltage to an intermediate level so that stage II can adopt lower voltage rating devices with less parasitic capacitances (C_{oss}) to reduce the switching loss at high switching frequency. Since the output voltage regulation is mainly dependent on stage II, stage I can switch in lower frequency, which sacrifices the first stage's voltage regulation for higher power efficiency. Then, the high switching frequency in stage II improves the output voltage regulation performance. The lower voltage devices used in stage II also have smaller on state resistance (R_{dson}) to reduce the conducting loss, therefore the total power efficiency can still be maintained at the desired level.

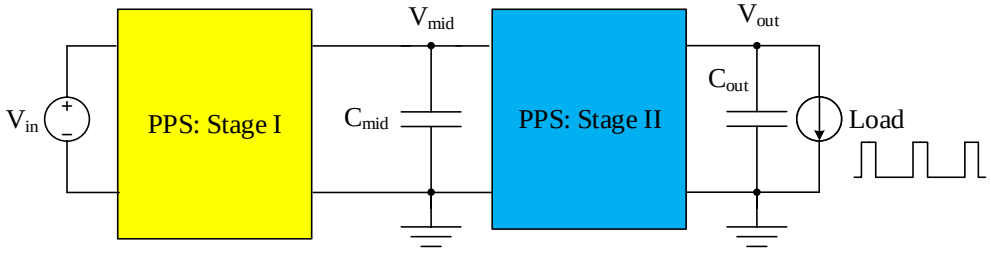


Figure 1-4 Block diagram of series connected two stage PPSs.

An unregulated LLC resonant converter (stage I) plus buck converter (stage II) topology is proposed in [20] to realize this series connected two-stage structure, where the unregulated LLC resonant converter always switches in resonant frequency to minimize switching loss due to the zero voltage switching (ZVS) benefits. However,

the unregulated first stage cannot buffer the pulsed load at the intermediate voltage V_{mid}, so a large input filter is still necessary. In [21], a slow response first stage is proposed to allow flexible V_{mid} to reduce the LF harmonics on the input side. However, the slow response voltage loop controller cannot average the pulsed load current precisely at different average power levels (caused by variable pulse duty ratios or different pulse peak voltages). Thus, the input filter size cannot be reduced greatly. In addition, the varying intermediate voltage also causes an obvious voltage droop on stage II output voltage due to its poor line regulation, which harms the PA's linearity.

1.3.3. Parallel connected two stage PPSs

The block diagram of parallel connected two stage PPSs is shown in Figure 1-5.

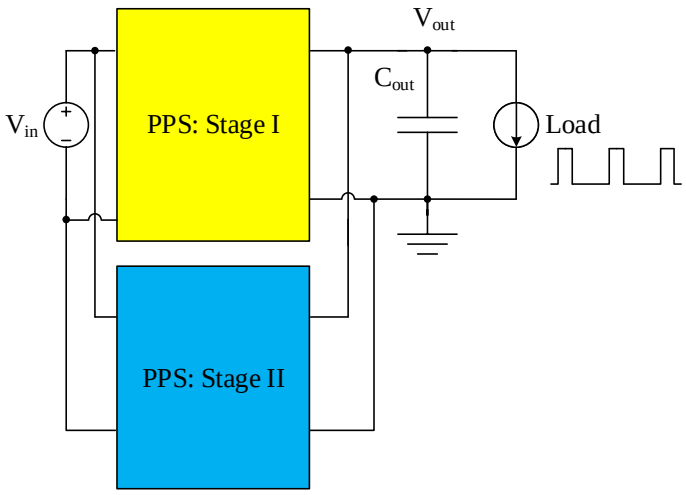


Figure 1-5 Block diagram of parallel connected two stage PPSs.

Based on the discussion in previous sections, it can be noticed that there is always a trade-off between fast response speed and high efficiency. Therefore, the main ideal of parallel connected two stage PPSs is adopting a highly efficient stage I to supply main power to the load and a fast response stage II to improve the overall output voltage

regulation. Since stage II only compensates for the power difference between the output of stage I and the pulsed load during the on/off transient, the overall high efficiency can still be maintained.

In consideration of the low power rating feature and fast response speed requirement of stage II, linear power supplies are reutilized to realize the parallel connected two stage PPSs structure, the experimental results in [22][23] prove that parallel connected two stage PPSs can achieve excellent regulation performance and high efficiency simultaneously. However, the linear amplifier needs an extra DC voltage level for biasing and a special circuit design for the parallel connection, which increases the complexity and size of the whole system.

A dual parallel buck converter is proposed in [24], in which one buck converter operates in lower switching frequency for normal voltage regulation and the other one in higher switching frequency for compensating the current difference between the slow buck converter and the pulsed load transients. However, this topology's rating is redundant since both buck converters are designed to handle the pulses' peak power.

Moreover, compared with series connected two stage PPSs, all above-mentioned parallel connected two stage PPSs can't buffer the pulsed load power so that large input filter and excessive device ratings (peak pulse power) are still needed.

1.3.4. Actively-controlled storage components PPSs

PPS block diagram involving actively-controlled storage components is shown in Figure 1-6. The difference from parallel connected two stage PPSs is that the stage II is replaced with an energy storage component with active control. When pulse load is

off, the power converter will intentionally transfer excessive power to the energy storage component. Then, the stored energy will be released by the energy storage component when the pulse is on. By this behavior, two benefits can be achieved as follow: 1) input side will only see the average power of pulsed load, which reduces the PRF harmonics and the input filter size; 2) the extra energy in the energy storage component helps the power converter to compensate the power difference during pulse on/off transient, which improves the output voltage regulation.

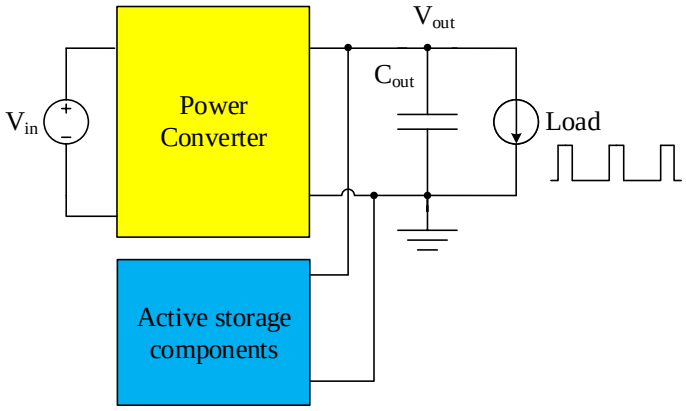
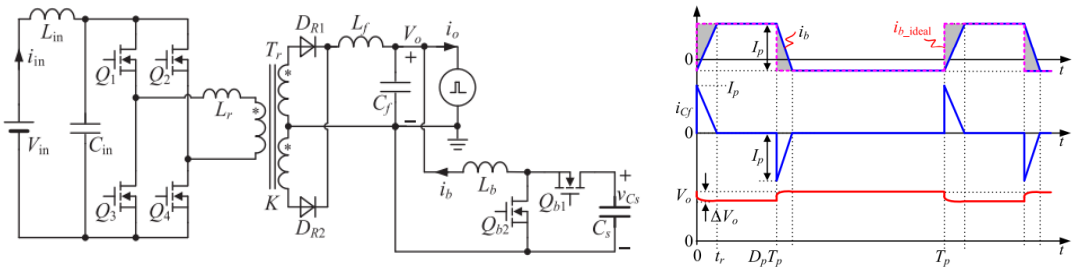


Figure 1-6 Block diagram of active-controlled storage components PPSs.

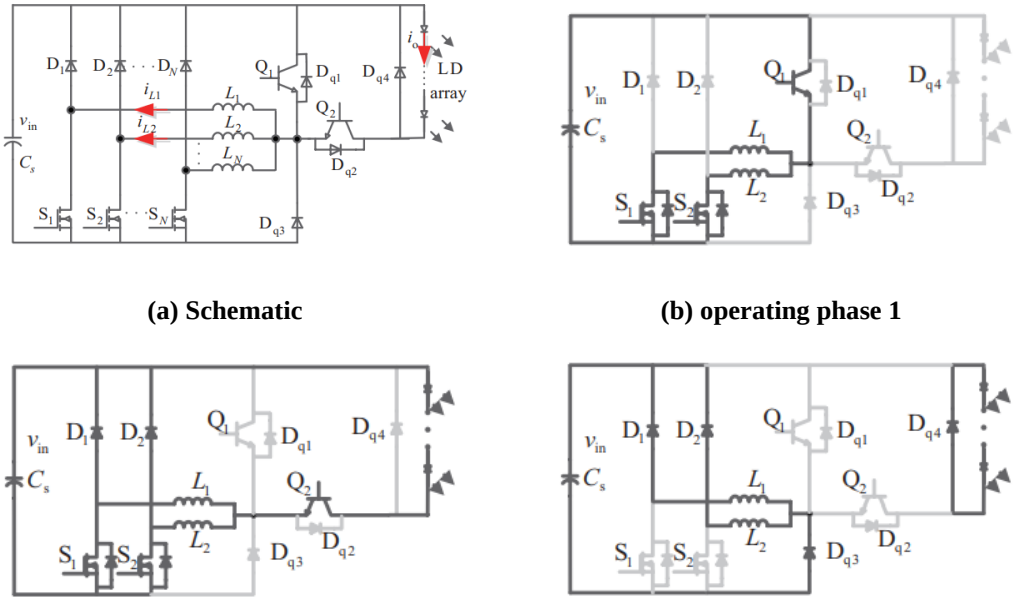
An active capacitor converter is proposed in [26] to realize this active-controlled storage components PPS. The schematic and main operating waveforms are shown in Figure 1-7. By adopting a large storage capacitor with a bidirectional interface converter connected in parallel with the pulsed load, the equivalent load will be the average power during a whole pulse period. However, this structure will consume more power since most energy goes through the bidirectional converter twice in one pulse period and the load information is needed to control the storage capacitor circuit.



(a) Schematic **(b) main operating waveforms**

Figure 1-7 Schematic and main operating waveforms of active capacitor converter.

An active inductor topology is also proposed in [27], and the schematic and different operating phases are shown in Figure 1-8. The converter charges the output inductor in advance to reduce the rise time of the output current. However, the pre-charging inductor circuit increases the loop conducting losses, further, load information is still needed.



(a) Schematic **(b) operating phase 1**

(c) operating phase 2 **(d) operating phase 3**

Figure 1-8 Schematic and main operating phases of active inductor converter.

1.4. Performance overview of GaN FETs

To build the hardware of PPSs, the choice of power switching devices is important to achieve low losses and high power density. The power loss is mainly composed of two parts: conduction loss and switching loss, which can be presented as

$$Couduction\ loss = \frac{1}{2} {I_{ds}}^2 R_{dson}, \tag{1.1}$$

$$and\ Switching\ loss = \frac{1}{2} C_{oss} V_{ds}^2 f_{SW}, \tag{1.2}$$

where R_{dson} is the equivalent conducting resistance of the power FET, I_{ds} is power FET's conducting current, V_{ds} is the voltage across the power FET when turning on, C_{oss} is the equivalent output capacitance of the power FET and f_{SW} is the switching frequency. From (1.1)(1.2), it can be noticed that the conduction loss is proportional to the R_{dson} and the switching loss is proportional to the C_{oss} of the device.

Therefore, the R_{dson} and C_{oss} of three widely used power switching devices technologies, Silicon, Gallium Nitride (GaN), and Silicon Carbide (SiC), will be compared in this section. In consideration that the supply voltages of PPSs are typically from the rectifiers after the AC source and the input voltages for common pulsed loads are less than 500 V, the blocking voltage (U_B) of power switching devices are focused in the range from 100 V to 1000 V.

1.4.1. Benefits of GaN FETs over SiC and Si FETs

The U_B related R_{dson} can be presented as [28]

$$R_{dson}(U_B) = \frac{k_R U_B^{\alpha_R}}{A_{die}}, \tag{1.3}$$

where A_{die} is the die area, k_R is the technology-specific constant and α_R is the voltage-scaling factor. Figure 1-9 shows a survey of commercially available state-of-the-art devices and Table 1.1 gives the empirically-fit exponential coefficients and constants for each technology. From Figure 1-9, it can be noticed that GaN devices have the smallest theoretical value of R_{dson} at the range of 100 V to 1000 V and the available commercial devices survey also proves this conclusion.

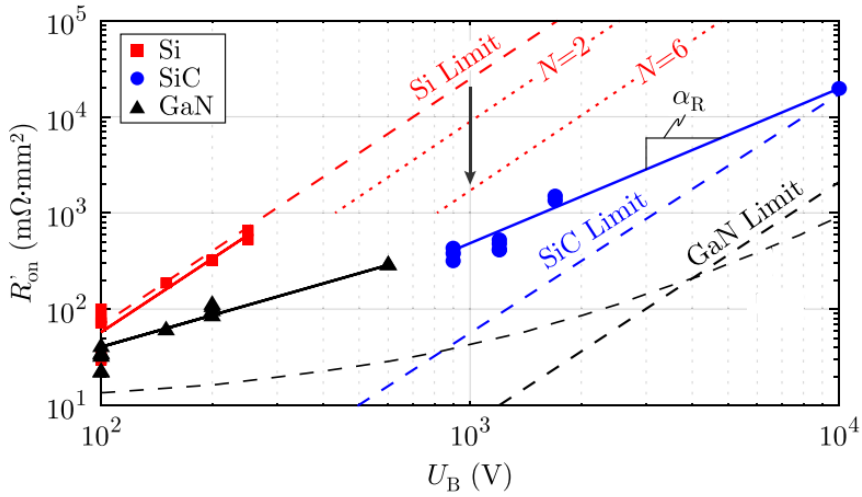


Figure 1-9 Specific R_{dson} at 25 °C junction temperature (T_j) for a selection of commercial power semiconductors. The Si, SiC and GaN theoretical limits from [29]–[31] are shown (dashed) together with the power function fits ($k_R \cdot U_B^{\alpha R}$) given in Table 1.1.

Table 1.1 Scaling factors α_R and k_R for R_{dson}, k_R is given such that R_{dson} is in mΩ·mm² and is fit at T_j = 25°C

	Si	SiC	GaN
k_R	$4.8*10^{-4}$	$7.2*10^{-3}$	0.26
α_R	2.5	1.6	1.1

The U_B related C_{oss} can also be presented as [28]

$$C_{oss}(U_B) = k_C U_B^{\alpha_C} A_{die}, \tag{1.4}$$

where k_C is the technology-specific constant and α_C is the voltage-scaling factor. Figure 1-10 shows a survey of commercially available state-of-the-art devices and Table 1.2 gives the empirically-fit exponential coefficients and constants for each technology. It can be noticed from Figure 1-10 that GaN devices have the smallest C_{oss} except the one at 200 V and 250 V and SiC is much more suitable for the application over 900 V.

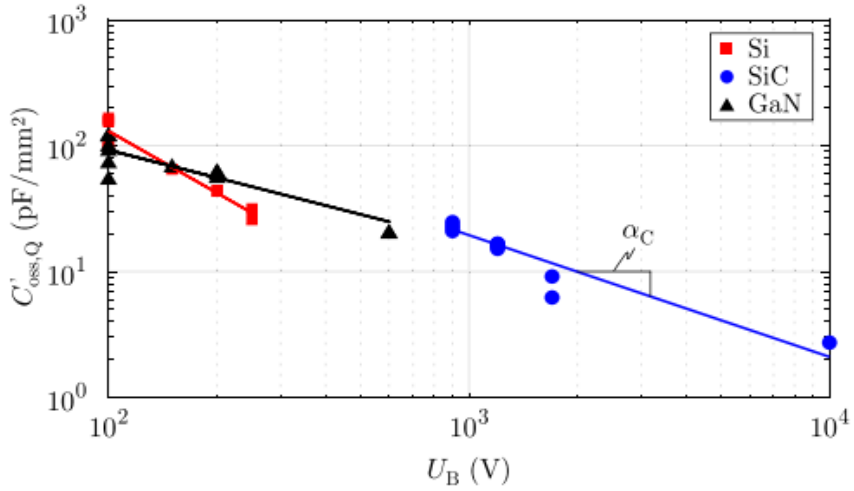


Figure 1-10 Specific charge-equivalent output capacitance C_{oss} for a selection of commercially-available power devices. The power function fits ($k_C \cdot U_B^{\alpha C}$) are given in Table 2.

Table 1.2. Scaling factor α_C and k_C for C_{oss}. k_C is given such that C_{oss} is in pF · mm^{-2}

	Si	SiC	GaN
k_C	$2.4*10^5$	$1.6*10^4$	$2.7*10^3$
α_C	-1.6	-1.0	-0.7

Based on the comparisons of the R_{dson} and C_{oss}, it can be concluded that GaN devices contribute to smaller conducting and switching losses. Besides, the turning on/off speed of the devices is also compared in [32]. All similarly rated commercial devices are chosen and operate under the same switching conditions. The results shown

in Figure 1-11 prove that the GaN devices have the fastest switching speed, which is most suitable for the power converters switching at high switching frequencies.

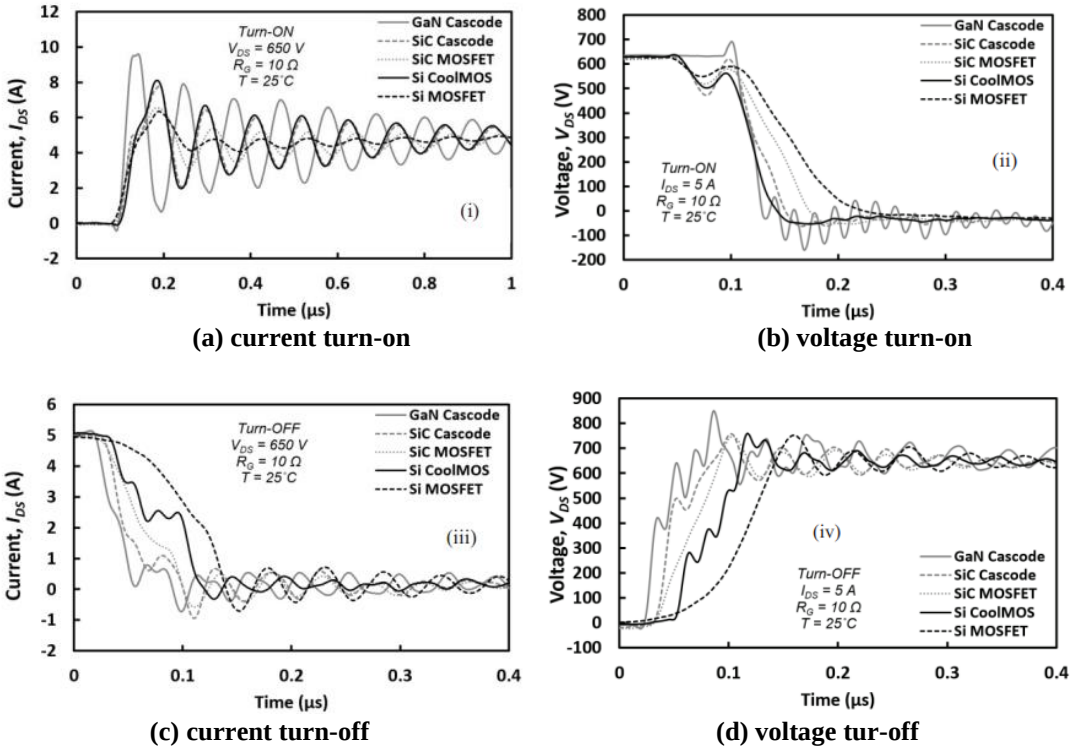


Figure 1-11 The transients of the silicon, SiC & GaN devices. It can be seen that the GaN device is the fastest in all switching.

1.4.2. Challenges involved with using GaN FETs in PPSs

The major reasons for the GaN devices' advantages can also be explained by its inherent materials properties shown in Table 1.3 [33].

Table 1.3 Different properties of Si, SiC, and GaN devices

Materials Property	Si	SiC	GaN
Band Gap (eV)	1.1	3.2	3.4
Critical Field 106 V/cm	0.3	3	3.5
Electron Mobility (cm^2 /V-sec)	1450	900	2000
Electron Saturation Velocity (10^6 cm/sec)	10	22	25
Thermal Conductivity (Watts/cm^2 K)	1.5	5	1.3

The high critical fields of both GaN and SiC compared to Si allow these devices to operate at higher voltages and lower leakage currents. Higher electron mobility and electron saturation velocity allow GaN devices for a higher frequency of operation and smaller equivalent on-resistance. However, GaN devices also have an inherent problem of the smallest thermal conductivity. This drawback causes the GaN devices to increase the maximum junction temperature in these three devices when conducting the same load current. And the maximum junction temperature will in turn dramatically increase the R_{dson} of the GaN devices. Therefore, the heat management for GaN devices brings more challenges for system designers to contend with.

1.5. Research objective

Because of the shortcomings of original PPSs, this dissertation will re-assess the requirements of the power supplies for three pulsed power applications and propose improved solutions using GaN devices to advance the PPSs' efficiencies, power densities, and response speeds. The circuit and controller designs will be included and the main non-ideal conditions in practical applications will be taken into consideration. Simulations and/or hardware results will be provided to justify the effectiveness of proposed solutions.

1.6. Dissertation outline

This dissertation is organized into seven sections. Chapter 1 introduces the main characteristics of the pulsed loads and summarizes the benefits and drawbacks of

existing techniques of PPSs. GaN devices' advantages and disadvantages compared to Si and SiC devices are also been analyzed.

A novel two stage high power density fast response PPS for pulsed power amplifiers is designed in chapter 2 to increase the power density and response speed. A special average current control strategy is proposed and verified. By using the unique control strategy, first stage power rating and size of input filter and midpoint capacitors get reduced, and therefore power density increase dramatically. Some hardware practical application issues, such as hard switching during light load, ringing caused by small C_{oss}, limited DSP calculating ability in high switching frequency are discussed in chapter 3 and chapter 4. Related improving methods on circuits and controllers are also proposed and verified.

Chapter 5 designs a novel power converter architecture applied in pulsed NMR applications. Proposed topology reduces the volume of the transformer, input filter and midpoint capacitor due to the average power control strategy. A 150 V to 400 V, 20 kW peak power converter is designed and the simulation results, scaled-down experimental results and design analysis are described to prove the validity of the proposed topology.

Chapter 6 proposed a linear assisted DC/DC converter design for the pulsed load to dramatically improve the response speed. The main power is transferred by a high efficient LLC converter and the linear amplifier is responsible to compensate for the current difference during the transient. Large output capacitor gets reduced by this converter's fast response. A band separation solution is also proposed to deal with the output parallel connection issue.

Chapter 7 is the conclusion for this dissertation and the outlook of the future work.

CHAPTER 2. PPS FOR POWER AMPLIFIERS IN RADAR APPLICATIONS

Pulsed PAs are widely used in radio frequency applications. Since these pulsed loads usually operate in short duty ratios with high peak current, there are traditionally two main challenges in the converter design: high power density and response to fast load transients.

2.1. Existing DC/DC converters for pulsed power amplifier applications

To address these challenges, a lot of existing techniques has been discussed in chapter 1 but all the above-mentioned converters can only partially solve the problems and still have relatively large size caused by the input filter or excessive device ratings.

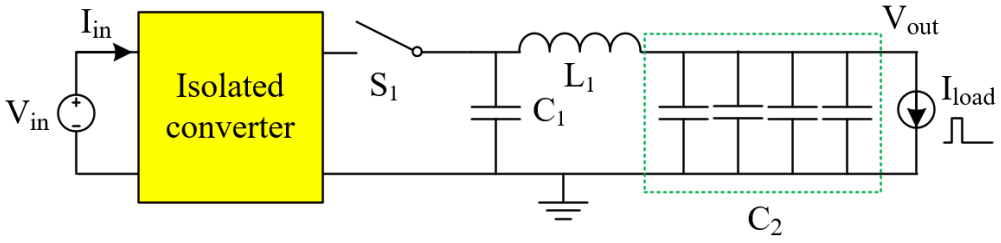


Figure 2-1 Block diagram of the conventional converter.

An isolated converter with a large capacitor bank C_2 (>> 10 mF) is still widely used as the conventional method (shown in Figure 2-1) to supply power for pulsed mode PAs [34]. When the pulse is on, S_1 turns off. C_2 supplies the power needed by the pulsed load. When the pulse is off, S_1 turns on and the isolated converter charges C_2 in a relatively smaller current compared with a pulse on load current. It can be understood that S_1 changes the high PAPR low duty ratio real pulsed load to an equivalent low PAPR high duty ratio pulsed load. Therefore, the isolated converter can be designed in

a lower current rating and the input filter can get reduced partially. However, since all the power is supplied by C_2 during pulse on, an extremely large capacitance value is needed to maintain the PA's requirement on output voltage droop and under/overshoot.

2.2. Proposed two stage structure for higher power density

This chapter presents a GaN-based two-stage converter as the power supply for pulsed load PA to address the above-mentioned issues and the possibility of achieving the design target as given in Table 2.1.

Table 2.1: Design Specifications

Symbol	Description	Values
V_{in}	Input voltage	325 V to 400 V
V_{out}	Output voltage	50 V
V_{droop}	Output voltage droop during pulse	< 0.5 V (1% V_{out})
$V_{under/overshoot}$	Output voltage under/overshoot at pulse on/off	< 0.75 V (1.5% V_{out})
I_{load_on}	Pulse on load current	2 × 40 A
I_{load_off}	Pulse off load current	~ 0 A
$T_{rise/fall}$	Load current rising/falling time	<< 1 us
D_{load}	Pulse duty ratio	5% to 20%
f_{load}	Pulse repeat frequency	1 kHz
I_{in_noise}	Input current harmonics	95 dBuA@ < 2.6 kHz
	Converter power density	> 150 W/in^3
	Total power density with cooling	> 75 W/in^3

The major contributions and advantages of the proposed converter are as follows:

- Two-stage architecture with flexible intermediate DC bus can reduce the size of storage (energy transfer) capacitor to < one-twentieth, in comparison with conventional methods.
- Average current control on the first stage (isolated converter) can reduce the size of low-PRF input filter by over 80% of the one without average current control.
- With the proposed input feed forward compensator, the second stage (fast converter, buck) achieves better line regulation performance which overcomes the load-side issues caused by wide-ranging flexible intermediate DC bus.
- GaN-based converter design achieves high average efficiency (>> 90%) and power density (>150 W/in^3), despite the pulsed nature of the applications.

The benefit of using a two-stage structure is that the converter functionalities are split between the stages to meet the specification. The first isolated stage steps down the high input voltage to an intermediate level with high efficiency. Whereas the second 'buck' stage uses a lower voltage rating device with less parasitic capacitance (C_{oss}) to achieve reduced switching loss at high switching frequency (~1 MHz) operation. The second stage is controlled at high bandwidth to respond fast to handle pulsed load transients.

Proper selection of topologies and control technique of the two stages plays a vital role to achieve the desired specification. An unregulated LLC can be used as the first stage to achieve high efficiency [3]. However, the unregulated first stage cannot buffer the load pulse at an intermediate level, so a large input filter is still necessary. In [4], a slow response first stage is proposed to allow flexible intermediate voltage (output voltage of the first stage) to reduce the current harmonics on the input side. However,

the slow response voltage loop controller cannot average the pulsed load current precisely at different average power levels (caused by variable pulse duty ratios). Thus, the input filter size cannot be reduced greatly using two-stage in [4], for a wide pulse duty ratio range (5% to 20%). In addition, the varying intermediate voltage also causes an obvious voltage droop on second stage output voltage due to its poor line regulation, which is not suitable for a PA application since it has an extremely high requirement on its supply voltage droop (-0.5 dB maximum) to avoid signal distortion [35].

This chapter discusses an average current control on the first stage and an input feed forward compensator on the second stage to fix the issues of the earlier mentioned two-stage converter. The functional block diagram is shown in Figure 2-2.

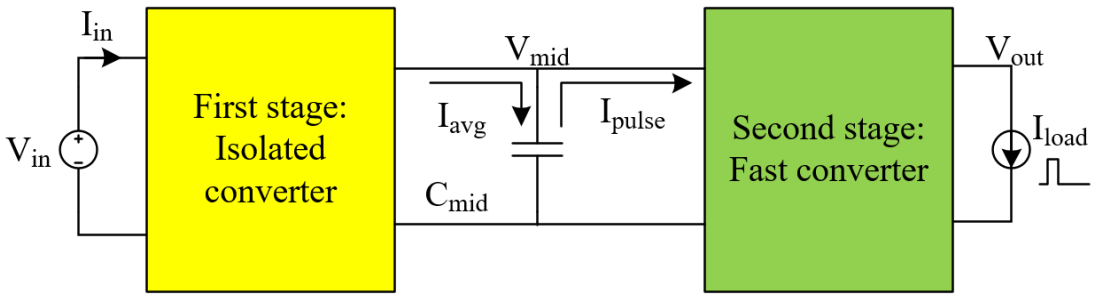


Figure 2-2 Block diagram of proposed converter.

Since the first stage isolated converter is limited to only transfer average power, lower current rating components (transformer and switches) can be utilized. Low PRF current harmonics also shrink dramatically on the input side. A high bandwidth buck converter is designed as second stage fast converter to meet the pulsed load transient requirement. To compensate for the current difference between continuous average current I_{avg} and pulsed peak current I_{pulse}, a midpoint capacitor C_{mid} is adopted.

The operating principle will be elaborated in Section 2.3. Section 2.4 and Section 2.5 discuss the first and second stage design respectively. A 375 V input 50 V output converter prototype for 4 kW/800 W(peak/average) pulsed load has been built and tested. The simulation and experimental results are discussed in Section 2.6 to verify the validity of the proposed topology. Section 2.7 is the summary.

2.3. Operating principle

The schematic and ideal operating waveforms of the proposed converter are shown in Figure 2-3 and Figure 2-4. It adopts a zero-voltage switching (ZVS) phase shifted full bridge (PSFB) topology as the first stage. Series capacitor C_b is designed to avoid transformer saturation. Diodes D_1 and D_2 are designed for clamping purposes. Midpoint voltage V_{mid} is the flexible intermediate voltage. The second-stage fast converter adopts buck converter topology. A single isolated converter is designed to supply power for two fast converters with pulsed PA loads.

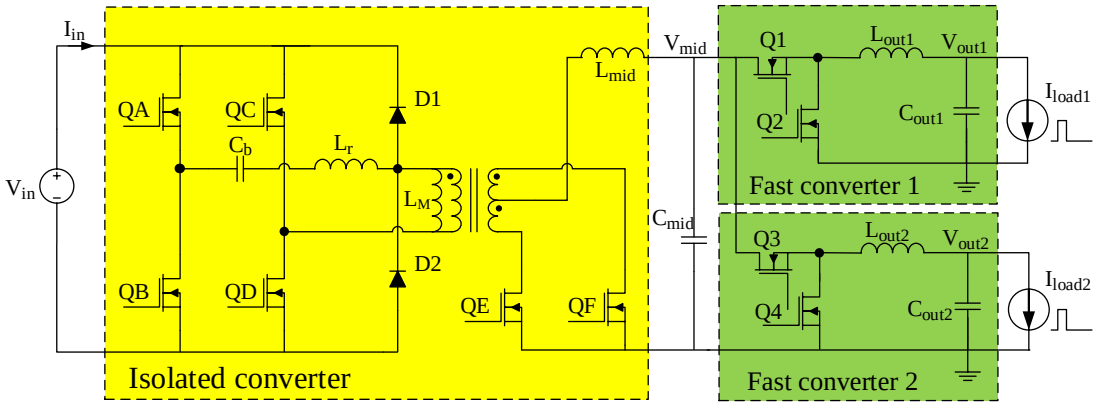


Figure 2-3 Schematic of proposed converter.

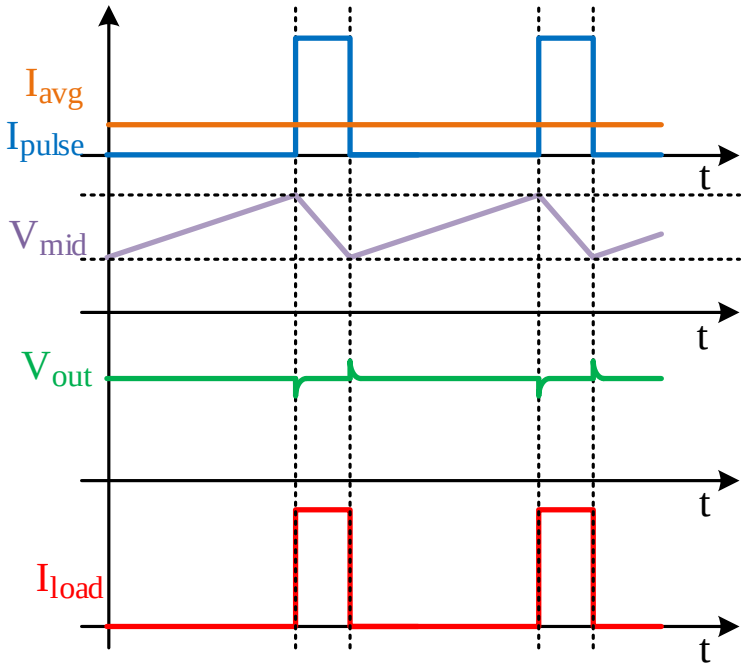


Figure 2-4 Ideal main operating waveforms of proposed converter.

An average current control strategy has been designed for the isolated converter to ensure that only average power is drawn from the voltage source V_{in}. It is noteworthy that transmitting average current is not equal to transmitting constant current. For a certain application, peak load current may be constant, but its pulse width can change between pulse periods. Average current control automatically modifies its output current to follow the average current changes between pulse periods but doesn't affect the current transients that vary inside a single pulse period. Besides, since the first stage only transfers average current, device ratings decrease dramatically to support the high peak to average power ratio (e.g., 4 kW vs. 800 W).

A fast response voltage mode control is adopted in the buck converter to meet the load transient requirements. Due to the lower switching loss of Gallium Nitride (GaN) devices and lower V_{mid} voltage compared to V_{in}, the fast converter can switch at

high frequency to achieve high bandwidth. The midpoint capacitor C_{mid} compensates for the instantaneous power difference between the two stages. The energy needed from C_{mid} during each period can be expressed by

$$E = \left(P_{peak} - P_{avg}\right) \times Pulsewidth \leq \frac{1}{2} C_{mid}\left(V_{mid\_max}^2 - V_{mid\_min}^2\right), \quad (2.1)$$

where, P_{peak} = 4 kW and P_{avg} = 800 W and maximum pulse width is 0.2 ms. To ensure that there is enough energy storage capacity with minimum capacitance value, V_{mid} is designed to be flexible in a wide range. Its minimum value V_{mid_min} (55 V) can be the minimum input voltage of the second stage for normal operation and the maximum value V_{mid_max} (70 V) should be decided based on second-stage devices voltage rating. Thus, C_{mid} needs to be larger 682 µF based on (2.1).

The storage capacitor C_2 value in conventional topology can also be calculated by (1), where P_{peak} = 4 kW, P_{avg} = 0 W, maximum pulse width = 0.2 ms, V_{mid_max} = 50 V and V_{mid_min} = 49.6 V (V_{droop} = 0.4 V). Here, C_2 needs to be larger than 32 mF. The hardware figure of C_2 capacitor can be found in [34], which occupies an extremely large space of the converter.

To eliminate the adverse effects of flexible V_{mid}, an input (V_{mid}) feed forward compensator has been designed in the 2nd stage to improve its line regulation. Details are discussed in section 2.5.

2.4. Isolated converter design

A PSFB topology has been chosen as the isolated converter topology. Compared with LLC resonant converter, PSFB has lower complexity on current control and its

fixed switching frequency benefit is more friendly for multiple power converters' synchronization at a system level. For example, if PA loads are applied in a radar array, their corresponding power converters will also form a power supply array. The minor difference between LLC converters switching frequencies will cause LF noise issues at common ground.

The first stage isolated converter schematic is shown in Figure 2-5. L_r is the transformer leakage inductance which is used for achieving ZVS and C_b is adopted to block DC current to avoid the transformer saturation. The diodes D_1 and D_2 clamp the current ringing caused due to resonance between leakage inductance and parasitic capacitances (C_{oss}) of QE and QF. The operating waveforms are shown in Figure 2-6. Gate signals of QA and QB are complementary with dead time, so are gate signals of QC and QD. By phase shifting between two legs, a bipolar square wave (V_{PRI}) with an adjustable duty cycle can be applied to the transformer. After synchronous rectification of QE and QF, unipolar square waveform (V_{SEC}) is applied to output LC (L_{mid} and C_{mid}) to regulate the mid-point voltage V_{mid}.

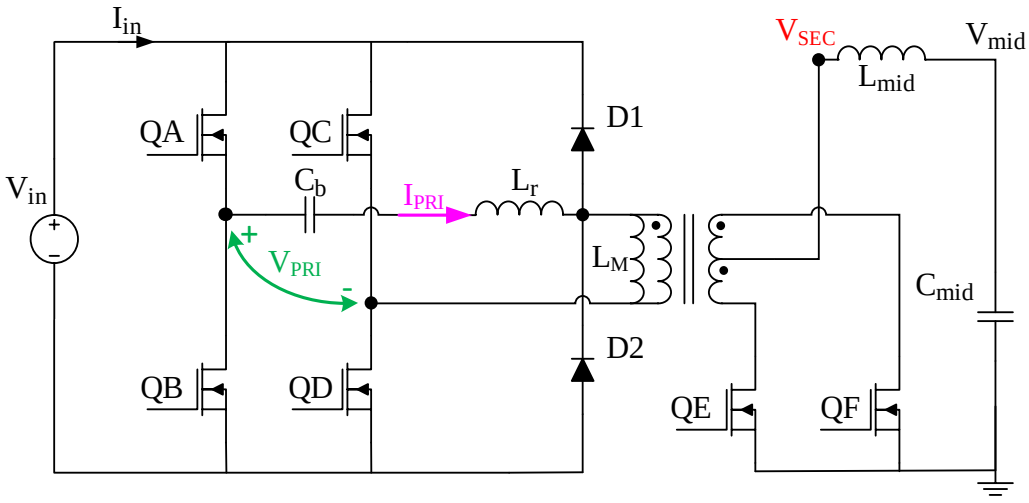


Figure 2-5 Proposed isolated converter schematic.

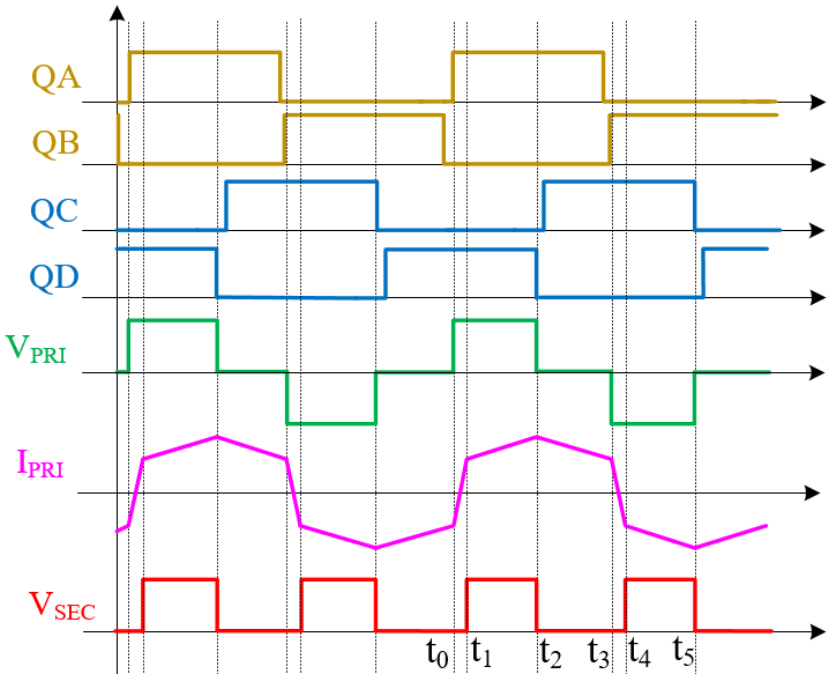


Figure 2-6 Isolated converter main operating waveforms.

2.4.1. Leakage inductor L_r design

For better efficiency, ZVS is needed during the converter operation. The basic principle for PSFB to achieve ZVS is using the energy stored in the leakage inductor to discharge the C_{oss} of switches before switches turn on. Thus, the minimum leakage inductance value to meet the ZVS requirement is given by [36]

$$\frac{1}{2}L_{r\_min}\cdot I_{PRI_{t3}}^2 \geq \frac{1}{2}(C_{ossA}+C_{ossB})V_{in\_max}^2, \tag{2.2}$$

where, $I_{PRI_{t3}}$ is the primary side transformer current I_{PRI} at time t_3 as shown in Figure 2-6. At different load conditions (i.e., average power due to different pulse duty ratios), L_r should be as large as possible to have sufficient energy for ZVS. However, with large L_r, it takes a longer time for the transformer to change current direction during t_0~t_1 and t_3~t_4 time slot which brings serious duty loss issues from primary side (V_{PRI}) to the

secondary side (V_{SEC}), especially at the higher switching frequency. Maximum acceptable duty loss D_{loss} can be calculated by (2.3)

$$D_{loss\_max} = 0.5 - \frac{N \cdot V_{o,max}}{2 \cdot V_{in,min}}, \tag{2.3}$$

where, N is the turns ratio of the transformer. Thus, L_r has a maximum limit in [36]

$$L_{r\_max} = \frac{N \cdot V_{in,max} \cdot D_{loss\_max}}{2 \cdot I_o \cdot f_s}. \tag{2.4}$$

Therefore, L_r can be limited in the range of (2.2) and (2.4). In this design, L_r range for achieving ZVS is calculated as 1.6 µH to 7.7 µH. The inductance value of 4.1 µH (a 3.3 µH external inductor in addition to the 0.8 µH leakage inductance from the transformer) has been chosen to achieve the least leakage inductor power loss. Based on the leakage inductance, DC blocking C_b is set as 2 µF in consideration of 300 kHz switching frequency to prevent transformer saturation.

2.4.2. Average current control design

The proposed average current control loop of the PSFB converter is shown in Figure 2-7.

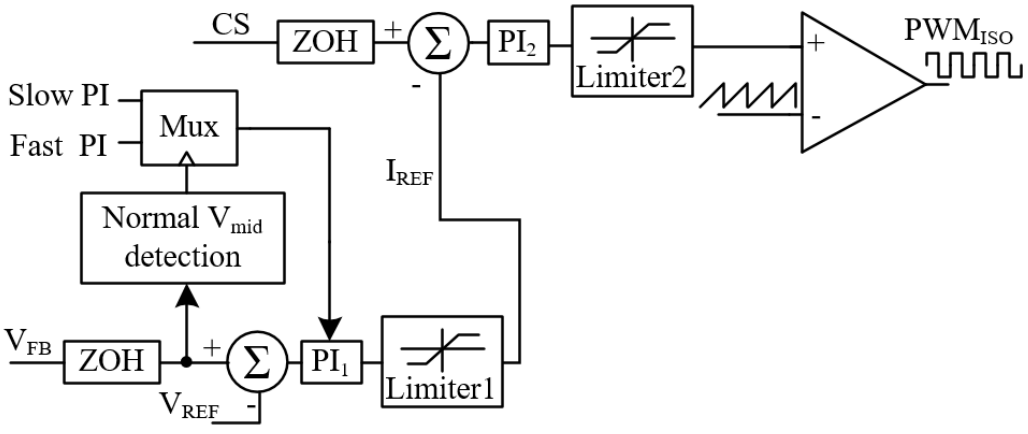


Figure 2-7 Average current control loop in isolated converter.

V_{FB} is the isolated converter output voltage feedback and CS is the output current feedback. This controller includes an outer voltage loop and an inner current loop. The voltage loop responds very slow to ignore the load changes within a pulse period and produces an average current reference I_{REF} for the inner current loop. The inner loop responds fast enough to ensure that the output current follows the change of I_{REF}.

For constant pulse duty ratio, voltage loop bandwidth can be as small as possible, such as designed in [4], since average current will be constant and current reference only has very minor modification.

However, in many applications, pulse duty ratios can vary widely after a few hundred pulse periods. If the voltage loop responds too slow, it won't bring the average current to desired levels within the required time. Then, V_{mid} cannot stay in the normal operating range, which may damage second-stage devices or cause the failure of voltage regulation by the second stage.

Therefore, a fast/slow PI switch block is designed in this control loop. When the control loop responds too slow and V_{mid} moves out of the normal operating range, fast PI will be used to make V_{mid} go back to normal operating range as soon as possible. The voltage loop will be indifferent to V_{mid} as long as it is within the normal operating range and provides the precise average current reference to the inner current loop. If V_{mid} is out of operating range for any reason (such as sudden unexpected load transients), the voltage loop will respond fast to recover V_{mid} back to normal operating range.

However, PI_1 switching frequently between fast and slow values will bring back the LF current harmonics issue. As shown in Figure 2-8, when PI1 responds too slow to cause V_{mid} increases over 70 V at every period, fast PI_1 needs to be active every pulse

period to modify isolated output current I_{Lmid}. Then, 1 kHz harmonics can be observed on the input current I_{in}.

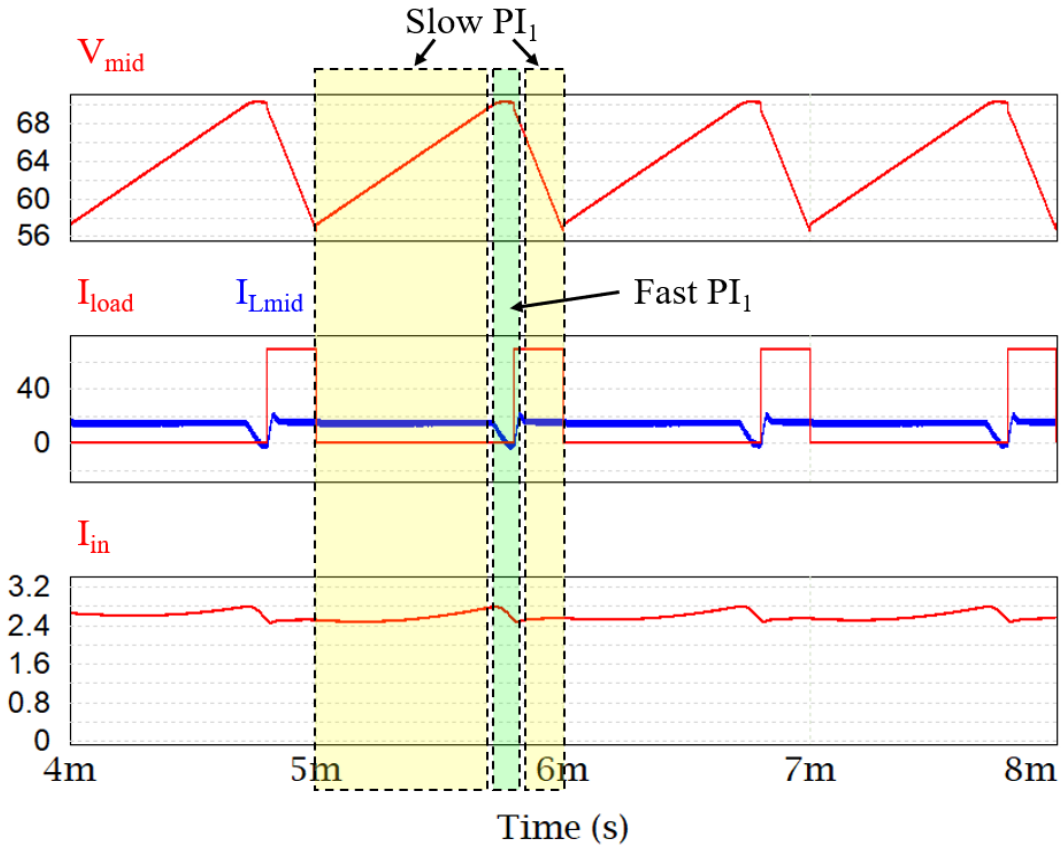


Figure 2-8 Simulation waveforms of fast/slow PI_1 switching.

Thus, a fast PI switch is designed only for some sudden unexpected load transients in this design. Typically, the maximum load transient is a step change from 5% pulse duty ratio (minimum average current scenario) to 20% pulse duty ratio (maximum average current scenario). Slow PI's response time for this step change should be less than 2 pulse periods so that even if fast PI is triggered at the first period, the control loop can revert to the slow PI in the second period. In other words, the fast PI avoids being active in two periods continuously, which ensures that the LF harmonics are small.

The voltage loop can be modeled as a first order transfer function. The relationship between step response time t and bandwidth f_{BW} in 1st order transfer function is given by [37]

$$t = \frac{0.34}{f_{BW}}. \tag{2.5}$$

The voltage loop bandwidth should be 170 Hz since t = 2 ms.

2.4.3. LC input filter design

The load current can be simplified as a square waveform as shown in Figure 2-9 and expressed in (2.6).

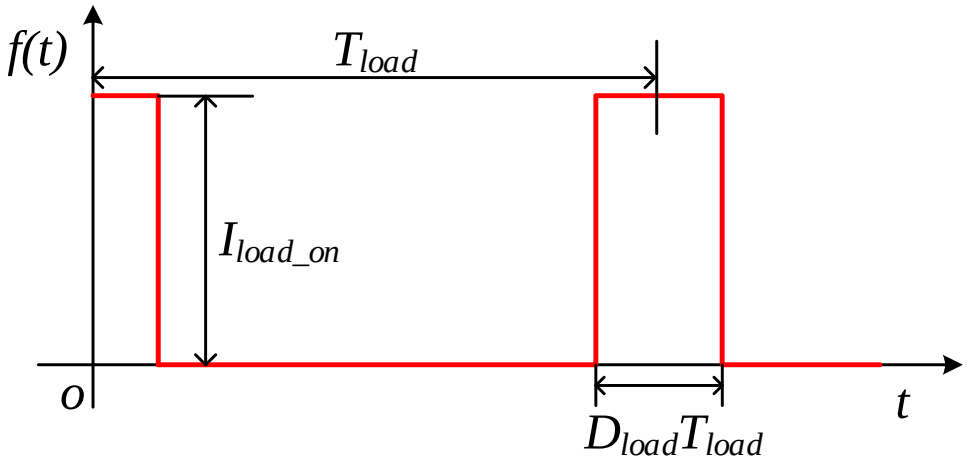


Figure 2-9 Load current simplified waveform.

$$f(t) = \begin{cases} I_{load_{on}}, |t| < \dfrac{D_{load}T_{load}}{2} \\ 0, \quad |t| > \dfrac{D_{load}T_{load}}{2} \end{cases}, -\frac{T_{load}}{2} \le t \le \frac{T_{load}}{2}. \tag{2.6}$$

Converting the function in (2.6) to Fourier series:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(\frac{2\pi nt}{T_{load}}\right), \tag{2.7}$$

$$a_n = \begin{cases} \dfrac{2}{T_{load}} \displaystyle\int_{-\frac{T_{load}}{2}}^{\frac{T_{load}}{2}} f(t)\, dt, & n = 0 \\ \dfrac{2}{T_{load}} \displaystyle\int_{-\frac{T_{load}}{2}}^{\frac{T_{load}}{2}} f(t) \cos\left(\dfrac{2\pi nt}{T_{load}}\right) dt, & n = 1,2,3 \ldots \end{cases}, \tag{2.8}$$

$$a_0 = 2D_{load} I_{load_{on}}, \tag{2.9}$$

and

$$\begin{aligned} a_n &= \frac{2}{T_{load}} \int_{-\frac{D_{load}T_{load}}{2}}^{\frac{D_{load}T_{load}}{2}} I_{load_{on}} \cos\left(\frac{2\pi nt}{T_{load}}\right) dt \\ &= \frac{4}{T_{load}} \int_{0}^{\frac{D_{load}T_{load}}{2}} I_{load_{on}} \cos\left(\frac{2\pi nt}{T_{load}}\right) dt \\ &= \frac{4}{T_{load}} \frac{I_{load_{on}} T_{load}}{2\pi n} \sin\left(\frac{2\pi nt}{T_{load}}\right)\Big|_{0}^{\frac{D_{load}T_{load}}{2}} \\ &= \frac{2I_{load_{on}}}{\pi n} \sin(D_{load} n\pi), \quad n = 1,2,3 \ldots . \end{aligned} \tag{2.10}$$

Based on (2.10), it can be concluded that maximum a1 appears with maximum load pulse duty ratio D_{load} (20%) and maximum load on current I_{load_on} (2*40 A). Thus, the maximum load current harmonics value at 1 kHz is 22.4 A. At steady state, the current harmonics can be reflected to the input side by

$$I_{in} = \frac{V_{out} I_{out}}{V_{in}}. \tag{2.11}$$

Thus, the 1 kHz current harmonics caused by the pulsed load can be calculated as 3.99 A. The objective is to achieve 95 dBuA (56 mA) as per CE101 standard. Thus, 1/71.3 attenuation (-37.1 dB) should be attained by the average current control loop, plus LC filter at 1 kHz. Since voltage loop bandwidth is 170 Hz and the inner current

loop also contributes a pole at the origin, the isolated converter can provide -18.7 dB attenuation at 1 kHz by

$$\mathrm{A}_{iso@1\,kHz} = 20\log\frac{(170\ Hz)^2}{(1000\ Hz)^2} = -30.8\ \mathrm{dB}. \tag{2.12}$$

Therefore, the attenuation needed by LC input filter is -37.1dB - (-30.8dB) = -6.3 dB. Since LC filter is a second order filter, its attenuation at 1 kHz can be expressed as

$$\mathrm{A}_{LC@1\,kHz} = 20\log\frac{\left(f_{o_{LC}}\right)^2}{(1000\ Hz)^2} = -6.3\ \mathrm{dB}. \tag{2.13}$$

Based on (2.13), LC filter's cutoff frequency can be calculated as $f_{o_{LC}} = 695$ Hz. If the average current control is not adopted in the isolated converter, all -37.1dB attenuation should be provided by LC filter alone. Then, such a small cutoff frequency has to be achieved via much larger inductors and capacitors.

2.5. Fast converter design

A buck converter has been designed as the second stage 'fast converter' to achieve high bandwidth for pulsed load transient. The schematic is shown in Figure 2-10, where R_L and R_C are the parasitic resistors of L_{out} and C_{out} respectively.

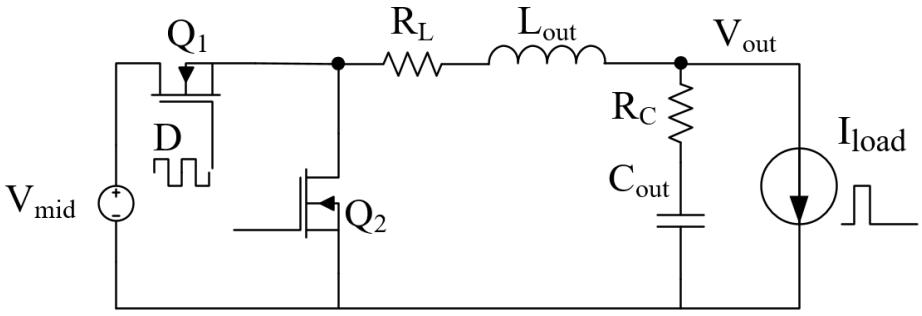


Figure 2-10 Second stage fast converter schematic.

In ideal condition, control loop's bandwidth can reach high values by properly tuning the loop compensator. However, the bandwidth of the buck converter is generally limited by the switching frequency. To avoid the adverse effects from converter noise, control loop cutoff frequency is typically designed to be less than 1/5th of switching frequency. Thus, to achieve a higher bandwidth, switching frequency has to be higher. However, high switching frequency also causes high switching losses, since $P_{loss_{switching}} \propto V_{in} C_{oss} f_{sw}$.

First stage isolated converter helps to step down the input voltage to a lower intermediate level and GaN devices provide a much smaller C_{oss} than Si devices. Thus, for a limited switching loss budget, fast converter can switch at a high frequency to achieve sufficient bandwidth. In this paper, the switching frequency is set as 1 MHz. Buck converters operating at MHz frequencies have been widely applied in point of load and envelope tracking applications [38]-[40], which are relatively low voltage and low power applications. However, for a 50 V output, 2 kW peak, pulsed power application, switching frequency of 1 MHz is much higher than what have been used by conventional approaches.

A practical digital control issue has been addressed in [41], when operating at such high switching frequencies. Fast switching operation requires high-speed controllers, which is increasingly becoming difficult to be achieved using the digital microcontrollers due to the hardware limitations such as signal latency and sampling rates. The numerical type of all digital signal processor (DSP) values used in this fast converter's control code are set as 'integer' to reduce DSP calculation time (<1 us).

Hence, the DSP is able to sample and update PWM signals every cycle and reduce the digital control delay.

With the proposed approach, a single voltage control loop is able to meet the undershoot/overshoot requirement during pulsed load transients. However, it has a line regulation issue because of wide varying range of V_{mid}.

Based on Figure 2-10, fast converter transfer function can be represented as [42]

$$G_{vd}(s) = \frac{\triangle V_{out}}{\triangle D} = R_{load}V_{mid}(1 + sR_cC_{out})/[s^2\big((R_{load} + R_c)L_{out}C_{out}\big) + s(L_{out} + (R_{load} + R_c)R_LC_{out} + R_cR_{load}C_{out}) + R_{load} + R_L]. \quad (2.14)$$

It can be noticed that V_{mid} directly affects the loop gain, which causes the poor line regulation of the fast converter.

To improve the line regulation performance, the impact of V_{mid} should be compensated by the control loop. Thus, an input feed forward compensator is designed in this controller, as shown in Figure 2-11. Since division calculation is extremely time consuming in DSP, an integer type second order *F(x)* and a 11-bit right shift operation are used to imitate the division of $1/V_{mid}$ with minimal computing resources. This 2nd order approximation ($F(V_{mid})/2048$) is compared with $1/V_{mid}$ in Figure 2-12.

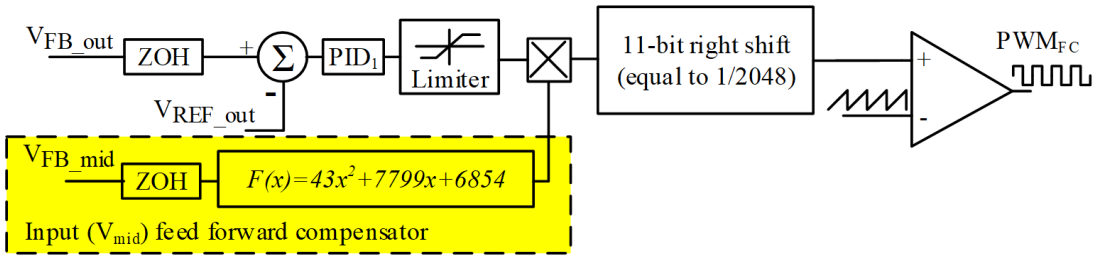


Figure 2-11 Fast converter control loop.

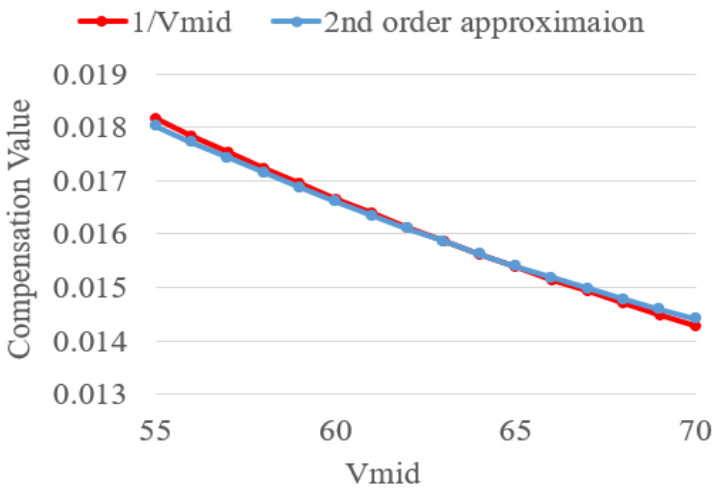
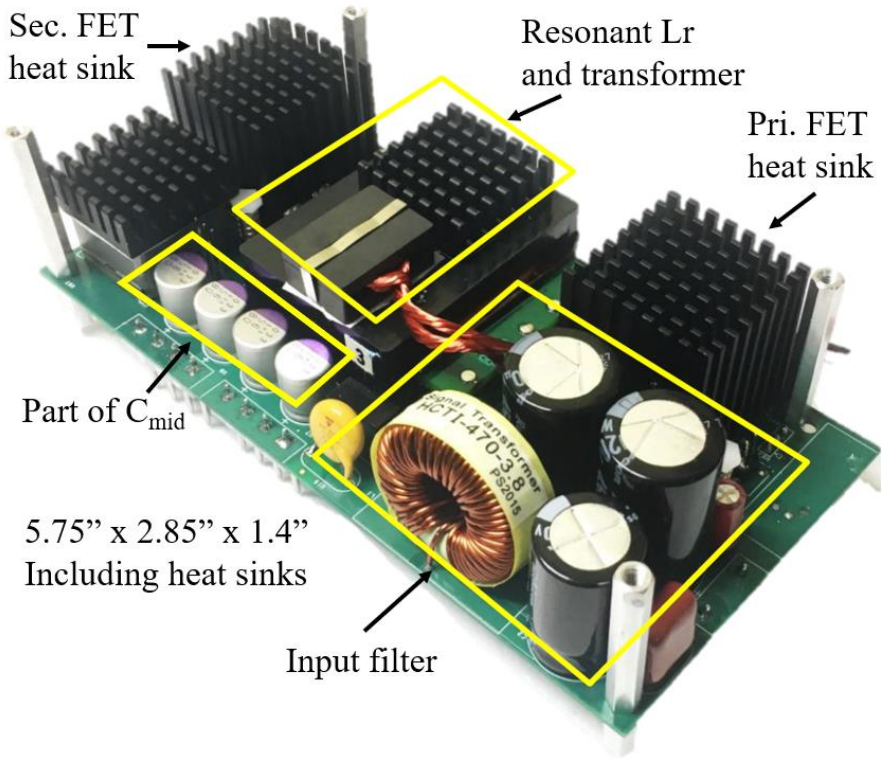


Figure 2-12 $1/V_{mid}$ and 2nd order approximation comparison.

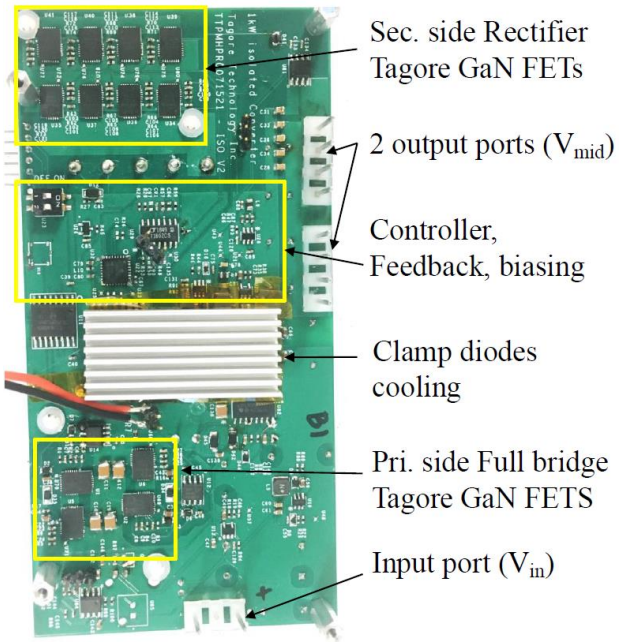
2.6. Simulation and test result

To verify the effectiveness of the proposed GaN devices-based two-stage topology and control methods, full scale prototype of an 800 W (average) / 4 kW (peak) power converter has been built and tested. The whole test setup includes a single isolated converter supplying power to two fast converters with two power amplifiers (PA) as pulsed loads.

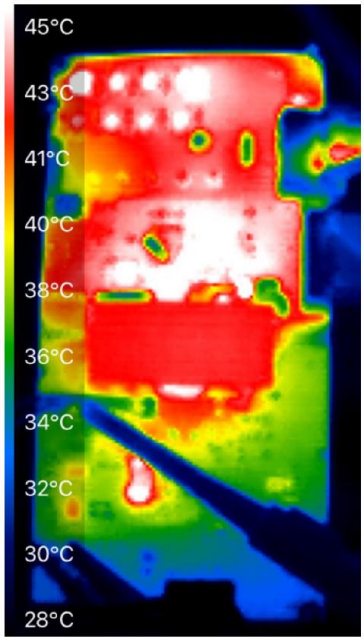
First stage isolated converter is shown in Figure 2-13. It steps down high voltage DC to an intermediate level, V_{mid}. All the switches are using Tagore Tech 650 V, 7.5 A GaN devices (TP44200NM). Based on the benefits of GaN devices and average current control, the temperature of isolated converter at full load is kept below 45 ℃ with fan cooling system. Its operating waveform is shown in Figure 2-14. Isolated converter only transfers average current to second stage with varying midpoint voltage V_{mid}. The input current harmonics is analyzed in Figure 2-15. Current harmonics at pulse frequency has largest amplitude and still meets the CE101 requirement, which proves the effectiveness of average current control with smaller input filter.



(a) isolated converter top view

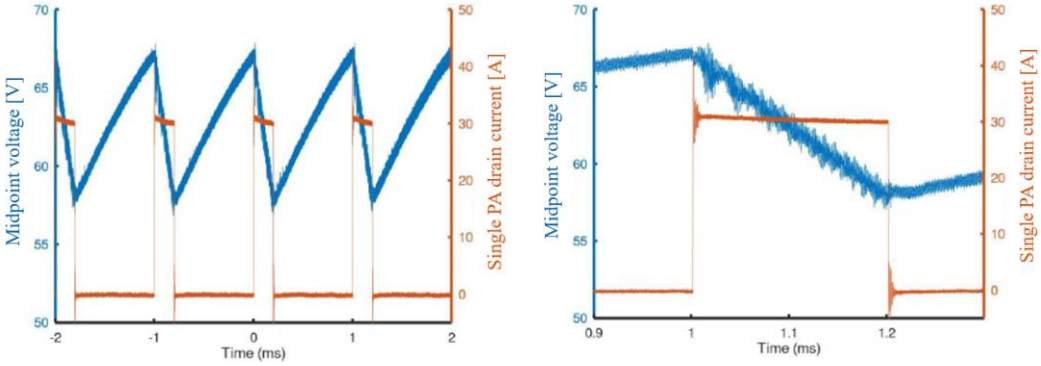


(b) isolated converter bottom view



(c) full load thermal photo

Figure 2-13 Hardware of first stage isolated converter.



(a) isolated converter output voltage with single pulsed load

(b) zoom in operating waveform

Figure 2-14. Isolated converter experimental operating waveform.

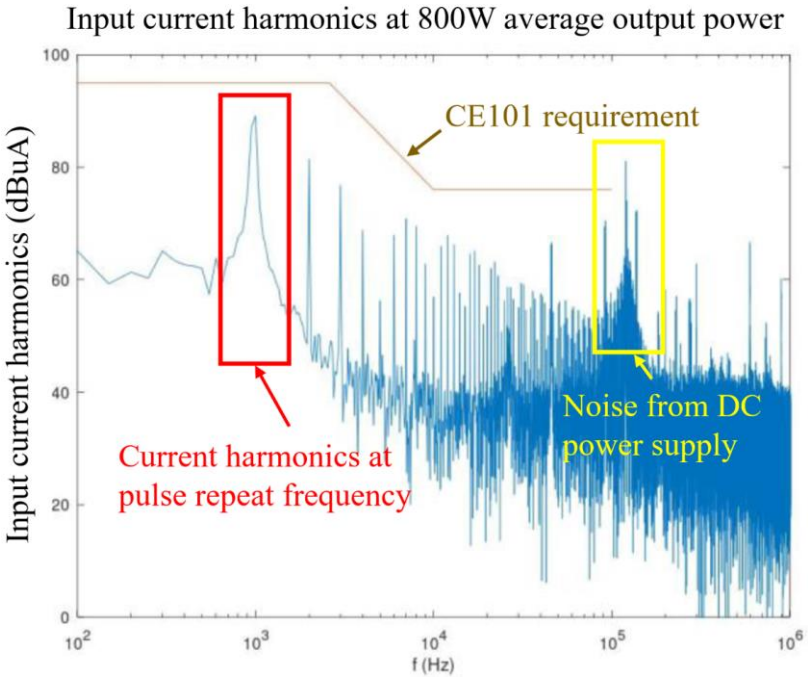


Figure 2-15 Input current FFT under full load condition.

The input filter cutoff frequency should be set as 695 Hz as calculated in section IV. In consideration of ± 30% component variation and value degrading at high temperatures, an LC filter with 424 Hz cutoff frequency using 470 µH inductor and 3×100 µF capacitors are designed for redundant design purposes. As discussed in section IV, if average current control is not adopted, input filter will be almost 6 times

larger than the one shown in Figure 2-13 (a). Therefore, the average current control dramatically increases power density. Average efficiency of the isolated converter under pulsed loads is shown in Figure 2-16. The efficiency is well over 90% for the entire specification of duty ratios.

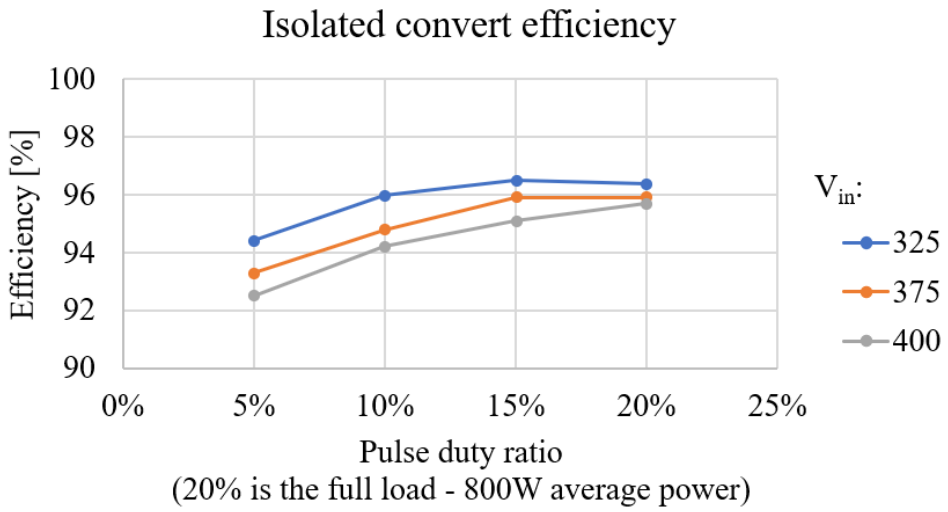
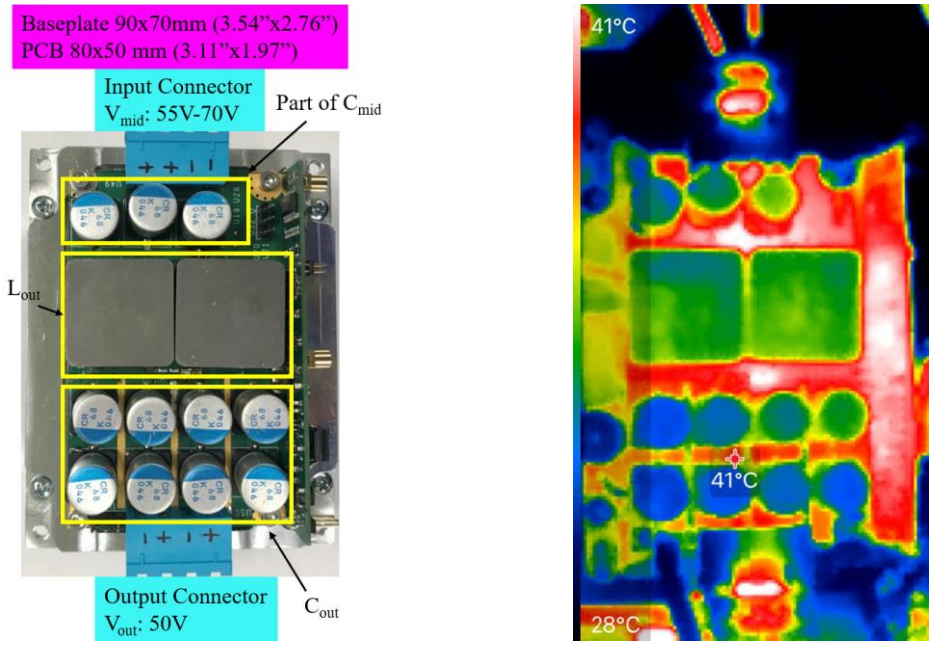


Figure 2-16 Isolated converter efficiency with different input voltage.

Second stage fast converter is shown in Figure 2-17. It regulates the varying V_{mid} to a constant output voltage V_{out}. Two output inductors Lout (2.2 µH each) are connected in parallel to handle 40 A peak current rating for a single PA load. C_{out} of each fast converter includes 8 × 68 µF. Fast converter is mounted close to the PA to minimize the voltage drop and it shares the water cooling system with the PA. Fast converter's hottest point at full load (2 kW) is 41℃, which shows the feasibility of such a high switching frequency (1 MHz). Its load transient waveform is shown in Figure 2-18 with 640 mV undershoot, 340 mV overshoot and almost zero droop voltage. All meet the requirement in Table 2.1, which proves the effectiveness of single voltage control in high switching frequency.



(a) fast converter top view **(b) full load thermal photo**

Figure 2-17 Hardware of second stage fast converter.

Fast converter's line regulation with/without input (V_{mid}) feed forward compensator is compared in Figure 2-19. Simulation and experimental result both prove that input (V_{mid}) feed forward can fix the line regulation issue caused by flexible V_{mid} and the 2nd order approximation is an effective method to imitate division operation in the DSP controller. In this protype, the C_{mid} consists of 4 × 82 µF from isolated converter plus 3 × 68 µF on each fast converter board. C_{mid} has a total value of 736 µF, which matches with the calculation in section II that C_{mid} should be at least 682 µF.

Fast converter efficiency is summarized in Figure 2-20. It can be seen that the maximum values of the average efficiency in pulse load conditions hover above 97%.

Based on Figure 2-13 (a) and Figure 2-17 (a), the proposed two-stage converter's total board area can be calculated as 28.6 in^2. The total height of the board is 0.83 inches. Therefore, the two-stage converter's power density (without heat sink) can be estimated at a high value of 168.5 W/in^3. The total converter volume with a fairly conservative

heat sink design can be calculated as 50 in^3. Therefore, the total power density with heatsink is 80 W/in^3.

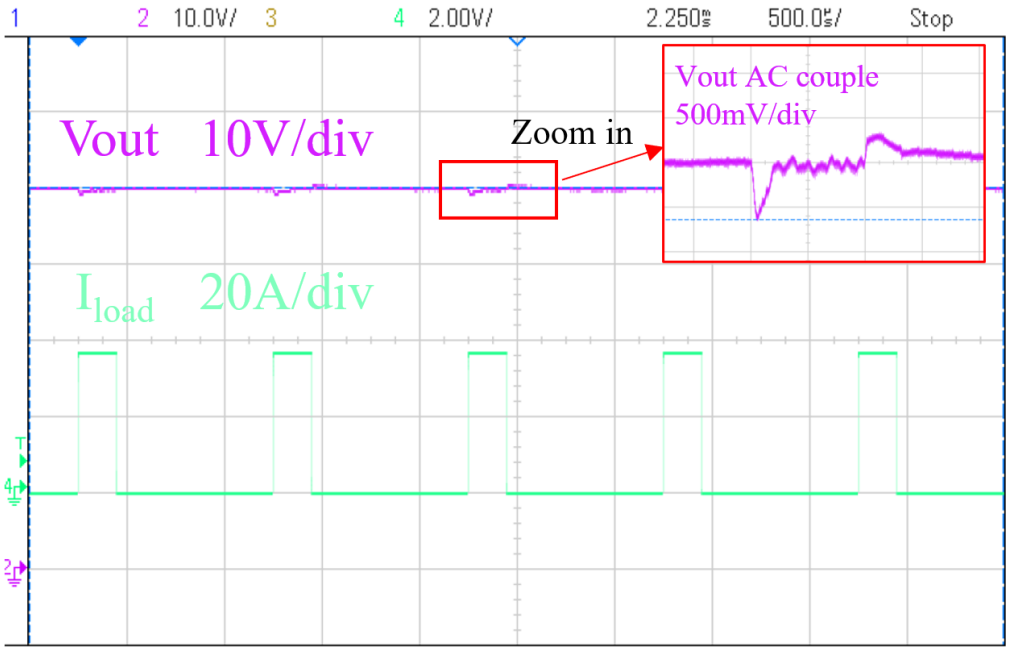


Figure 2-18 Fast converter experimental waveforms of transient response with pulsed load.

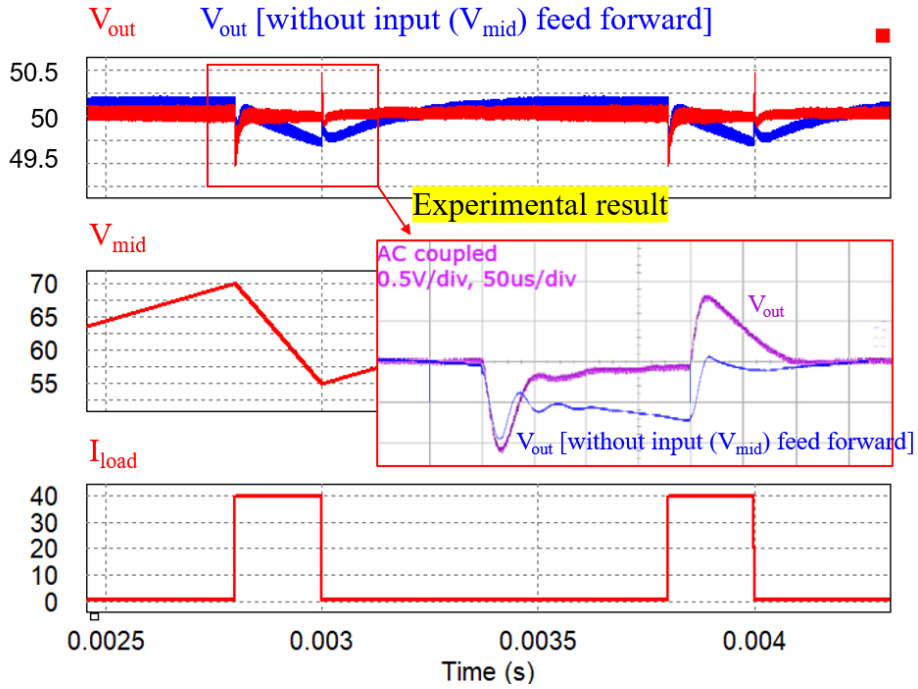


Figure 2-19 Simulation and experimental waveforms of line regulation comparison with/without input (Vmid) feed forward.

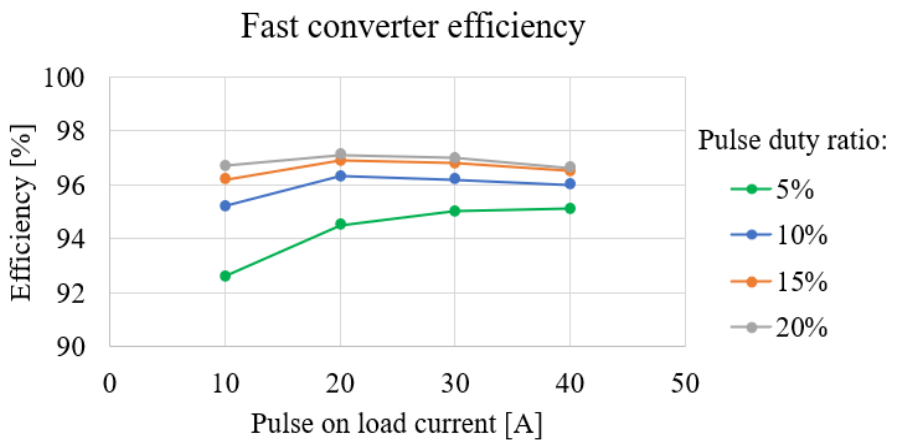


Figure 2-20 Fast converter efficiency with different pulse on current and different pulse duty ratio.

The performance of the proposed topology is summarized and compared with some of the prominent existing methods (shown in Table 2.2). The parameters in the existing literature are extrapolated to the practical specifications (375 V input, 50 V output and 80 A peak pulse current with 20% duty ratio and PRF = 1 kHz) given in Table I. From the comparison, it can be concluded that the proposed topology has been able to match or exceed the performance of the major existing approaches.

Table 2.2 Result Comparison with Different Topologies

Reference	**[20]**	**Conventional [34]**	**[43]**	**This paper (Proposed)**
Structure	ISO+buck	ISO+bank capacitor	ISO+buck	ISO+buck
ISO control	Fix ratio	Equivalent Low PAPR	Current pre-regulated	Average current control
Input filter f_{o_LC}	70.8 Hz	143 Hz	178 Hz	424 Hz
Input filter LC	470 µH+ 10.8 mF	470 µH+ 2.6 mF	470 µH+ 1.7 mF	470 µH+ 300 µF
ISO power rating	4000 W	1000 W	800 W	800 W
Buck control	Voltage mode	N/A	Current mode	Voltage mode + input feed forward
V_{droop}	400 mV	400 mV	348 mV	~ 0 mV
$C_{mid} + C_{out}$	4.1 mF	32 mF	11 mF	1.8 mF

2.7. Summary

This paper proposed a GaN-based two-stage power converter with novel control methods for low frequency pulsed load applications. With average current control, first stage isolated converter transfers consistent average current to the second stage, which helps in reducing the input filter size to < 17% of the one without average current control. A flexible intermediate voltage is applied to reduce the volume of midpoint energy storage capacitor. Using the proposed digital input feed forward compensator in the second stage fast converter, poor line regulation issues caused by varying midpoint voltage V_{mid} was avoided. Hence, V_{mid} range can be as large as possible without affecting V_{droop} on the output voltage. A 375 V input 50 V output 800 W (average) / 4 kW (peak) converter protype was built and tested. The experimental results validated the proposed topology and the control strategy. The converter's power densities are 168.5 W/in^3 and 80 W/in3, without and with the heatsink, respectively. Table 2.2 summarizes the benefits of the proposed topology over other topologies. The effectiveness of the proposed concepts make them attractive for pulse load applications requiring fast response and high power density, such as radar systems.

Paper publication:

Y. Yao, G. Kulothungan, H. Krishnamoorthy, H. Soni and A. Das "GaN based two-stage converter with high power density and fast response for pulsed load applications", *IEEE Transactions on Industrial Electronics* (under review)

CHAPTER 3. IMPROVED PPS DESIGNS FOR PULSED POWER AMPLIFIERS I

To practically realize the first stage isolated converter discussed in chapter 2, this chapter presents the advanced improvement designs of GaN based phase shifted full bridge (PSFB) converter along with a new adaptive burst mode control strategy, to achieve high efficiency over a wide power range, including light loads. The main challenges of PSFB converters addressed in this chapter are: load-dependent zero-voltage switching (ZVS), transformer saturation, and secondary side ringing. Since switching losses of GaN FETs are dominant at light loads, adaptive burst mode control can be employed to improve the efficiency at lower output power. By periodically switching output current between 0 A and minimum ZVS current, adaptive burst mode control can enable both smaller effective switching frequency and lower switching losses. A correction factor 'k' is adopted in the adaptive burst mode control's current loop PI calculation so that the output current can switch fast without any overshoot that increases switches' current stress. To verify the effectiveness of the proposed circuit and controller design, a 375 V input, 70 V output, 800 W PSIM simulation model as well as an experimental prototype are developed and tested. The experimental results demonstrate the practical benefits of the proposed adaptive burst mode control.

3.1. Drawbacks of PSFB converter and existing improvement designs

Due to the benefits of ZVS, PSFB isolated converters are widely used in many modern industrial applications, such as renewable energy conversion [44], electric vehicle charging [45][46], and telecommunication systems' power supplies [47][48].

PSFB converter has the benefits of wide gain range and fixed switching frequency over LLC resonant converter [49], has lower switch voltage rating compared to active clamp converter [50], and lower complexity than dual active bridge (DAB) converter [51], for unidirectional power flow.

Using GaN devices, the PSFB converter can operate at higher frequencies, which increases power density and response speed [52][53]. However, a higher switching frequency also makes the PSFB converter's inherent drawback, load-dependent ZVS, more prominent [54]. At high switching frequencies, a smaller transformer leakage inductance is needed to reduce the duty loss issue for maintaining sufficient voltage gain, but this will lead to ZVS failure at light loads. When using GaN devices at relatively higher voltages and frequencies, since switching losses are dominant under light load operation due to the C_{oss} capacitance [55], the total light load efficiency becomes very poor under ZVS failure. Several techniques have been proposed to improve the light load efficiency of PSFB converters and they can be overall classified into two types: (i) extending the PSFB converter's ZVS range and (ii) reducing equivalent switching frequency at light loads.

Under the first classification, many auxiliary circuits have been proposed in [56]-[60], but they increase the current stress of the device and cause extra auxiliary circuit loss. Meanwhile, several topology variants are proposed to overcome PSFB's load-dependent ZVS issue, such as triple converter with shared leading legs [61], converter adopting two series-connected transformers[62][63], and the combination of two different PSFB converters[64][65]. These variants generally have limitations of

application scenarios and are not widely used in consideration of system complexity and reliability.

For the second classification, burst mode control is utilized in [66][67]. By forcing the converter to switch in a few large duty cycles by default and then skip some switching cycles, the burst mode control can effectively reduce the overall equivalent switching frequency, thereby reducing the switching losses at light loads. However, this burst mode can only be applied to very light load conditions, since the output current is not actively controlled and continuous large duty cycles may produce high peak currents, damaging the devices.

This chapter proposes an adaptive burst mode control strategy that combines the benefits of the above-mentioned approaches. The proposed strategy forces the converter to periodically switch output current between 0 A and the minimum ZVS current, but at the same time, the average output current still matches with the load requirement. The equivalent switching frequency decreases due to the presence of converter disabled time slots (0 A current) and the converter maintains the minimum ZVS output current in most switching cycles. It is noteworthy that not all switching cycles can achieve ZVS due to the rising time needed by the output current. To reduce the output current rising time as much as possible, an adaptive current loop PI calculation is also adopted in this paper. It can also ensure that no current overshoot occurs during the output current transients (0 A to minimum ZVS), which helps to protect the devices from damage due to over-currents.

The main advantages of the proposed concepts can be summarized as follows:

- The proposed adaptive burst mode control strategy can extend PSFB converter's ZVS range and reduce the effective switching frequency concurrently at light load; thereby increasing the light load efficiency drastically.
- The new proposed correction factor 'k' can help adaptive burst mode controller to switch output current between 0 A and minimum ZVS current, quickly and smoothly.
- The developed methods can be extended to other types of DC-DC converters with current control as well, such as buck, boost, etc.

This chapter is organized as follows. In section 3.2, the circuits and operating principle of PSFB will be firstly described and the related reason for light load ZVS failure will be explained. Then, other practical concerns (such as transformer saturation and secondary side ringing) aggravated by GaN-based high switching frequency and their corresponding solutions are discussed. In section 3.3, the proposed adaptive burst mode control and the internal current loop PI calculation are designed. Section 3.4 provides the experiment results to confirm the mathematical analysis and verify the effectiveness of the proposed adaptive burst mode control. Section 3.5 will be the summary.

3.2. First stage isolated converter circuits improvement designs

The schematic of the PSFB converter is shown in Figure 3-1. L_k is the leakage inductance of the transformer, designed to achieve an extended ZVS range; this can be a separate inductor as well if the transformer leakage inductance is not sufficient. C_b is the blocking capacitor to prevent DC current saturating the transformer. It is noteworthy that GaN device does not have the parasitic reverse body diode, but itself can operate

similar to a diode when the reverse voltage is applied [68]. This property is indicated as 'equivalent' reverse diodes in Figure 3-1. C_{oss} represent FET output capacitance.

The operating principle of PSFB can be explained with the main waveforms shown in Figure 3-2. Q_1 and Q_2 in the leading leg turn on alternately with fixed 50% pulse width. The lagging leg operates the same as the leading leg, but a specific phase shift is applied between the two legs. By adjusting the phase shift value, the duty cycle of bipolar square wave V_{PRI} can be modified. After the synchronous rectification of secondary side devices Q_5 and Q_6, *Vsec* with a specific duty cycle can be applied to achieve the appropriate output voltage regulation.

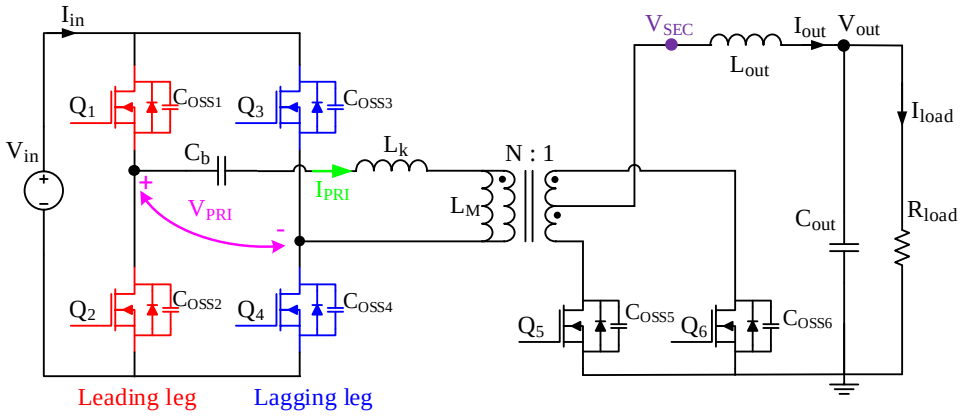


Figure 3-1 Phase shifted full bridge (PSFB) converter schematic.

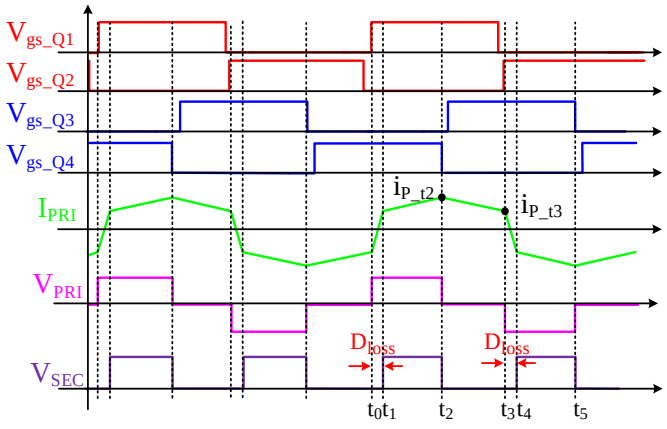


Figure 3-2 PSFB converter's main operational waveforms.

3.2.1. Leakage inductance (L_k) design

Once a certain device turns off, the current stored in the inductor L_k needs to fully discharge two C_{oss} in the same leg within the deadtime, so that the other device can turn on with ZVS. For leading and lagging legs, the leakage inductor currents at switching time can be represented as i_{P_t2} and i_{P_t3}, respectively. As shown in Figure 3-2, the leading leg utilizes a smaller current to achieve ZVS ($i_{P\_t3} < i_{P\_t2}$). Therefore, L_k should meet the requirement as in

$$\frac{1}{2}L_k i_{P_{t3}}^2 \geq \frac{1}{2}(C_{oss1} + C_{oss2})V_{in}^2. \tag{3.1}$$

After simplification,

$$L_k \geq \frac{(C_{oss1} + C_{oss2})V_{in}^2}{i_{P_{t3}}^2} \approx \frac{N^2(C_{oss1} + C_{oss2})V_{in}^2}{i_{out}^2}, \tag{3.2}$$

where, V_{in} is the input voltage, i_{out} is the output current and N is the transformer turns ratio. In the consideration of a wide load range, L_k should be as large as possible to meet the requirement of (3.2) for ZVS. However, large L_k will bring an obvious duty loss issue to the secondary side since it will take a longer time for L_k to change the current to the opposite direction as shown in t_0~t_1 and t_3~t_4 time slots of Figure 3-2. The duty loss can be defined approximately as in [50]

$$D_{loss} \approx \frac{4I_{out}L_k f_s}{N \cdot V_{in}}, \tag{3.3}$$

where, f_s is the converter switching frequency.

To obtain sufficient converter voltage gain, the maximum acceptable duty loss D_{loss} can be defined as in

$$D_{loss\_max} = D_{ctrl\_max} - \frac{N \cdot V_{out}}{V_{in}}, \tag{3.4}$$

where, D_{ctrl_max} is the maximum duty cycle that can be achieved by a practical controller, which is related to the controller's processing speed. In this paper, D_{ctrl_max} is set as 0.9 to be compatible with various performance processors. Then, by combining (3.3) and (3.4), (3.5) and (3.6) can be deduced as

$$0.9 - \frac{N \cdot V_{out}}{V_{in}} \geq \frac{4 I_{out} L_k f_s}{N \cdot V_{in}}, \tag{3.5}$$

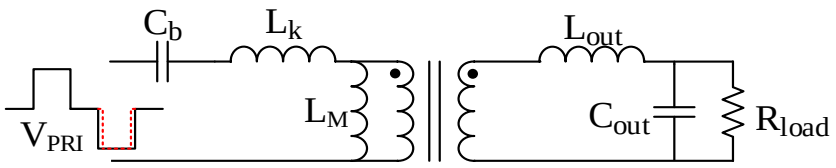
and after simplification,

$$L_k \leq \frac{N \cdot V_{in}}{4 I_{out} f_s} \cdot \left(0.9 - \frac{N \cdot V_{out}}{V_{in}}\right). \tag{3.6}$$

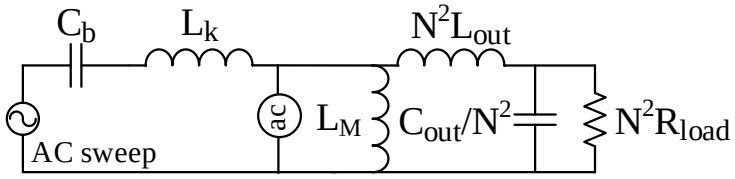
Therefore, the L_k range can be identified by (3.2) and (3.6). Since GaN based PSFB converters are switching at high frequencies, the L_k range is becoming increasingly smaller, limited by (3.2) and (3.6). Even if there are multiple L_k values possible, there will still be a trade-off on choosing relatively larger or smaller L_k, in which a smaller L_k value leads to a narrower ZVS load range and a larger L_k value results in more inductor AC core losses. In this paper, a relatively smaller L_k value is preferred, and an adaptive burst mode control is employed to increase the efficiency for the overall load range.

3.2.2. Blocking capacitor (C_b) design

The simplified PSFB convert circuit and the corresponding AC signal model are shown in Figure 3-3.



(a) Simplified PSFB converter



(b) AC signal model

Figure 3-3 Simplified PSFB converter circuit with AC signal model.

If switches are ideally the same, the bipolar square wave V_{PRI} will be symmetrical and there won't be any DC component. However, in practice, the on/off time of every switch can be different due to the mismatch of the gate driver, gate resistance, and switch input capacitance. Thus, the waveform may be asymmetrical as shown in Figure 3-3 (a), with a minor DC component that can saturate the transformer over time. This saturation issue is more serious in GaN-based PSFB converter due to its higher switching frequency. Therefore, a blocking capacitor C_b is added in series with the transformer to form a high pass filter that can block the DC components.

Based on Figure 3-3 (b), the transfer function from V_{PRI} to the transformer can be represented as

$$H(s) = \frac{sL_M||Z_{SEC}}{\frac{1}{sC_b} + sL_k + sL_M||Z_{SEC}}, \tag{3.7}$$

where, Z_{SEC} is the secondary side impedance and can be defined as

$$Z_{SEC} = sN^2L_{out} + \frac{\frac{N^2}{sC_{out}} \cdot N^2R_{load}}{\frac{N^2}{sC_{out}} + N^2R_{load}}. \tag{3.8}$$

Then, it can be approximately simplified as

$$Z_{SEC} = sN^2L_{out} + \frac{N^2}{sC_{out}}. \tag{3.9}$$

After substituting (3.9) in to (3.7) and simplifying (3.7) by ignoring a 'large' L_M, the transfer function can be approximated as

$$\begin{aligned} H(s) &= \frac{sN^2L_{out} + \frac{N^2}{sC_{out}}}{\frac{1}{sC_b} + sL_k + sN^2L_{out} + \frac{N^2}{sC_{out}}} \\ &= \frac{s^2N^2L_{out}C_bC_{out} + N^2C_b}{N^2C_b + C_{out} + s^2(L_k + N^2L_{out})C_bC_{out}} \\ &= \frac{N^2C_b}{N^2C_b + C_{out}} \cdot \frac{1 + s^2L_{out}C_{out}}{1 + \frac{s^2(L_k + N^2L_{out})C_bC_{out}}{N^2C_b + C_{out}}}. \end{aligned} \tag{3.10}$$

Based on (3.10), the high pass filter can be represented as

$$\begin{cases} H(0) = \frac{N^2C_b}{N^2C_b + C_{out}} \\ f_{zero} = \pm\frac{1}{2\pi\sqrt{L_{out}C_{out}}} \\ f_{pole} = \pm\frac{1}{2\pi}\sqrt{\frac{N^2C_b + C_{out}}{(L_k + N^2L_{out})C_bC_{out}}} \end{cases}. \tag{3.11}$$

Thus, to achieve enough attenuation for the DC component, C_b should be as small as possible. However, small C_b will simplify f_{pole} as

$$f_{pole} = \pm\frac{1}{2\pi}\sqrt{\frac{1}{(L_k + N^2L_{out})C_b}}. \tag{3.12}$$

Based on (3.12), it can be concluded that too small a value for C_b will increase pole frequency. When this value gets close to the switching frequency, it will distort the

normal V_{PRI} signal. Therefore, C_b should be designed such that pole frequency is 1/5th of switching frequency to avoid V_{PRI} distortion.

The AC sweep results with different C_b values shown in Figure 3-4 verifies the effectiveness of (3.11) and (3.12) as frequency of the 'zero' remains the same with different C_b values. Smaller values of C_b lead to lower DC attenuation but lead to higher pole frequencies.

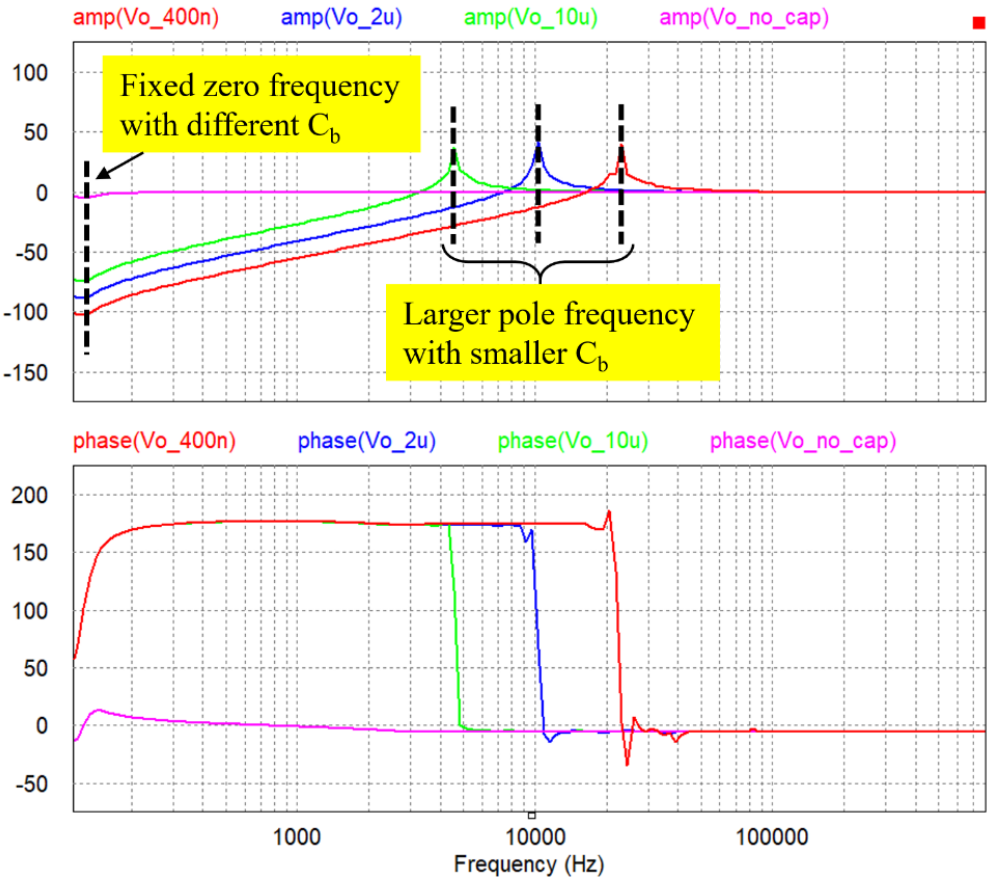


Figure 3-4 AC sweep results with different C_b (red- C_b=400nF, Blue-C_b=2 µF, Green-C_b=10 µF and Pink-C_b=0 µF).

3.2.3. Clamping circuit design for reduced ringing

In PSFB converters, it is common to observe high frequency ringing and peak overshoot across the FET devices. However, the ringing issue becomes worse in GaN

FET-based PSFB converters due to the devices' small C_{oss} and fast *di/dt*. As shown in Figure 3-5, when Q_6 turns off, the sudden voltage step change across the drain-source of Q_6 (V_{ds_Q6}) causes the leakage inductance *'L_k/N_2'* to resonate with C_{oss6}, which causes ringing/overshoots at the drain of Q_6 (V_{d_Q6}). This will also appear on V_{d_Q5} when Q_5 turns off. The ringing frequency and overvoltage peak are given by [51]

$$f_{ringing} = \frac{1}{2\pi\sqrt{\frac{L_k C_{oss}}{N^2}}}, \tag{3.13}$$

$$\text{and } V_{ov} = \frac{L_k}{N^2} \cdot \frac{di}{dt}. \tag{3.14}$$

It can be noticed that compared with Si devices, GaN devices' smaller C_{oss} and faster *di/dt* cause more frequent over-voltage peaks, that too with higher magnitudes.

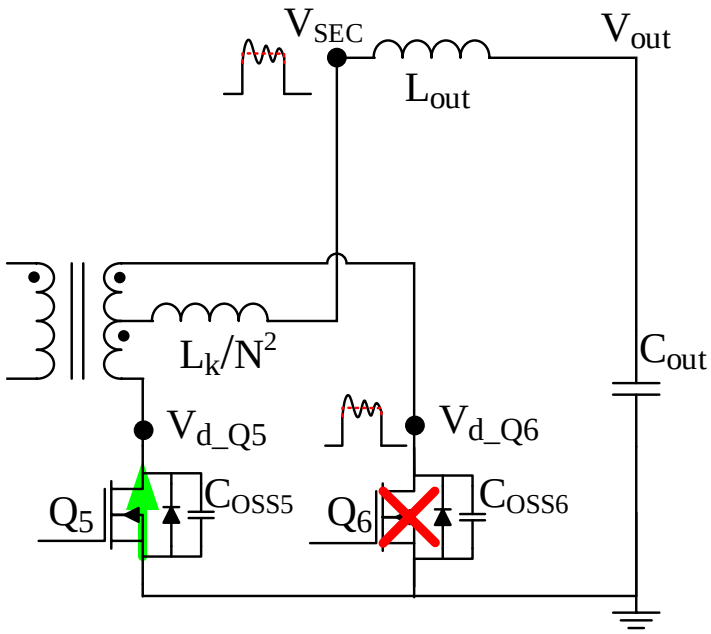


Figure 3-5 The ringing equivalent circuit referred to the secondary side.

To reduce the ringing issue, three clamping circuits are summarized in Figure 3-6, and their performances based on a 375 V input, 70 V output GaN-based PSFB

converter are compared in Figure 3-7. Operating waveforms without clamping circuits are also included in Figure 3-7 (a) as a reference.

The ringing starts at the drain voltages of Q_5 and Q_6 and can be reflected to the primary side by the transformer. Thus, introducing D_1 and D_2 shown in Figure 3-6 (a) to clamp the voltage V_T, can reduce the ringing issue. However, based on the waveforms shown in Figure 3-7 (b), it can be noticed that since diodes D_1 and D_2 can only clamp the voltage after external leakage inductor L_{ke}, the transformer's integrated leakage inductance L_{ki} still causes minor ringing. Since all the ringing energy is transferred back to the input source, the main power loss is due to the conduction loss of D_1 and D_2.

To further reduce the ringing, RCD clamping can be applied as shown in Figure 3-6 (b). On the secondary side, the maximum voltage of V_{SEC} is clamped to V_{C1} by D_3. C_1 is adopted to absorb ringing energy and R_1 is adopted to discharge C_1 so that V_{C1} can be consistent in every cycle. The relationship between C_1, R_1 and clamping voltage V_{C1} can be determined by [69]

$$R_1 = \frac{T_S(V_{C1} - V_{out})(V_{C1} - V_d)}{C_1 V_{C1}(2V_d - V_{C1})}, \tag{3.15}$$

where, T_S is the switching period and V_d is the ideal (without ringing) maximum voltage of the clamping point. In the Figure 3-6 (b) condition, the maximum V_{SEC} voltage is V_{in}/N.

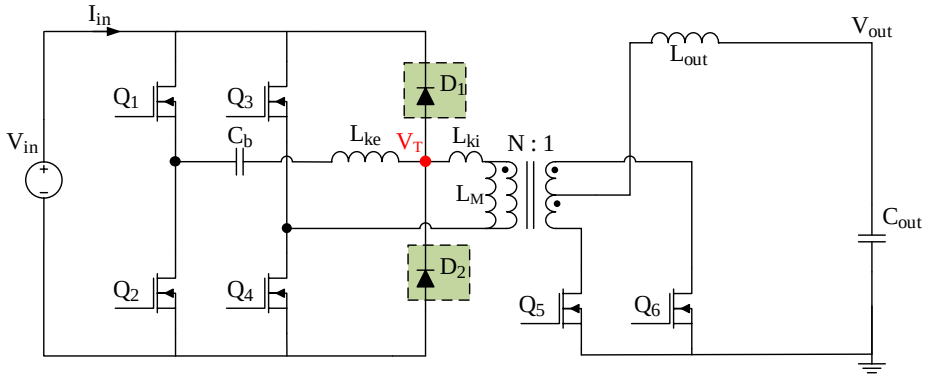
The power loss on the discharging resistor R_1 can be approximately represented as

$$P_{R1} = \frac{(V_{C1} - V_{out})^2}{R_1}, \tag{3.16}$$

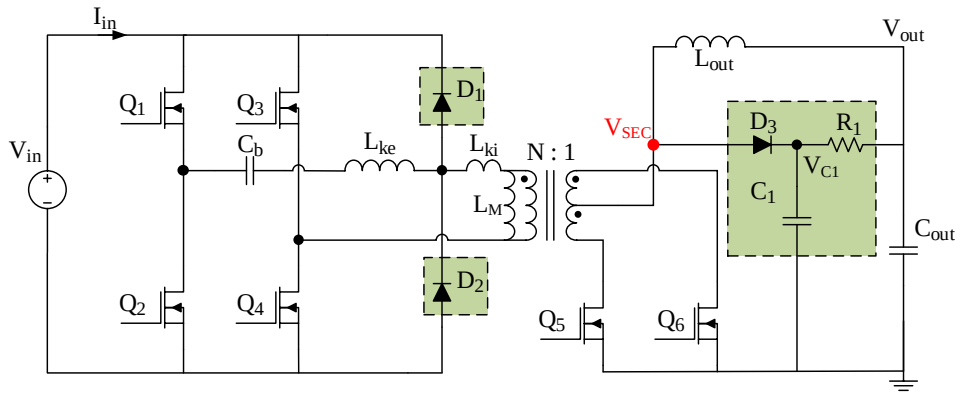
where, V_{C1} is typically set as 10% higher than V_d for practical applications. Then, combined with (3.15), (3.16) can be transformed to get

$$P_{R1} = \frac{(1.1V_d - V_{out})^2}{\frac{T_S(1.1V_d - V_{out})(1.1V_d - V_d)}{C_1 \cdot 1.1V_d \cdot (2V_d - 1.1V_d)}} = \frac{9.9C_1V_d(1.1V_d - V_{out})}{T_S}. \quad (3.17)$$

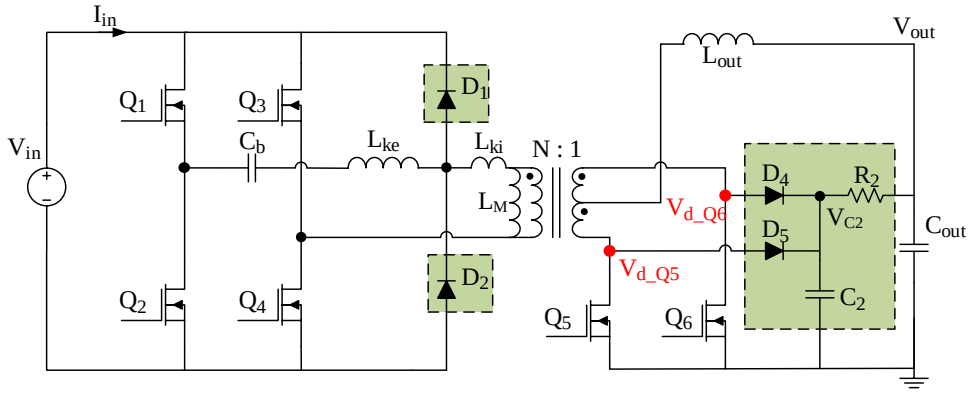
From the comparison of Figure 3-7 (b) and Figure 3-7 (c), it can be concluded that RCD clamping dramatically reduces the ringing at V_{SEC} and the performance is better than just employing diode clamping, but at a cost of slightly lower efficiency due to the power loss explained by (3.17). Figure 3-6 (c) shows a dual RCD clamping circuit that can directly clamp V_{d_Q5} and V_{d_Q6} for the best performance, which is shown in Figure 3-7 (d). Its discharging resistor power loss can still be calculated by (3.17). The only difference is that V_d becomes the ideal maximum voltage of V_{d_Q5} and V_{d_Q6}, which is twice as large as V_{SEC} due to the secondary side center-tap winding. Therefore, it has more power loss on the discharging resistor as shown in Figure 3-7 (d).



(a) PSFB converter with diode clamping

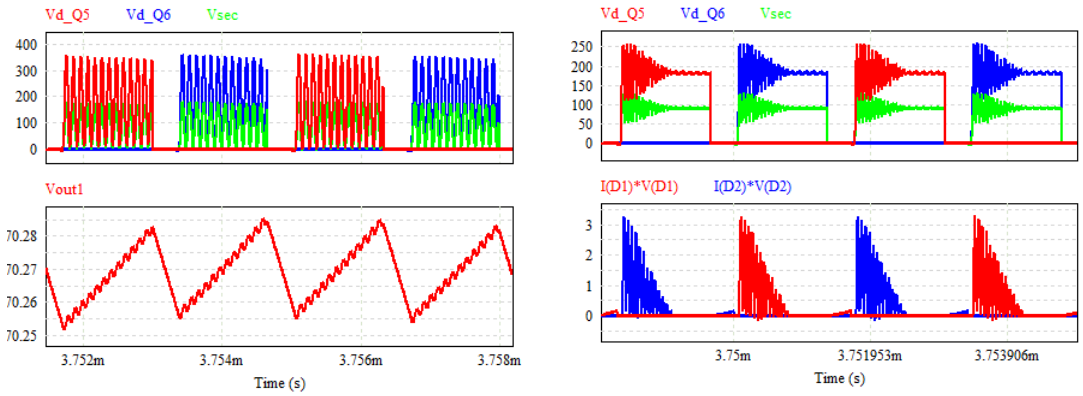


(b) PSFB converter with diode clamping + RCD clamping

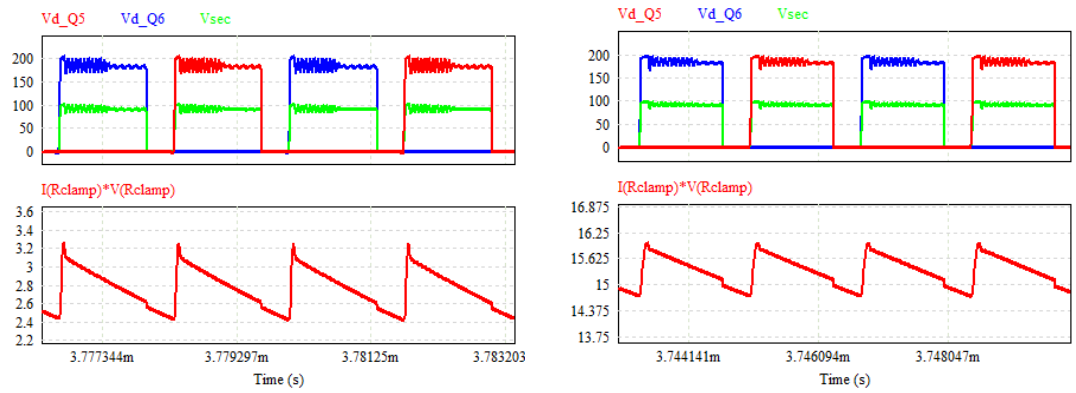


(c) PSFB converter with diode clamping + dual RCD clamping

Figure 3-6 Clamping circuits for reducing the ringing issue.



(a) without clamping **(b) with diode clamping**



(c) with RCD clamping **(d) with dual RCD clamping**

Figure 3-7 Secondary side main operating waveforms under different clamping circuits and related main power loss.

3.3. First stage isolated converter controller improvement designs

With load decreasing from full load to no load, the GaN FET switching loss becomes increasingly dominant in the total power loss. However, based on the analysis on section 3.2.1, L_k can only achieve ZVS up to certain loads, such as 50%, which causes increasingly poor efficiency at lower power. The principle of traditional burst mode is forcing a larger than desired duty cycle at the first N switching cycle and skipping the next M-N (M>N) cycles so that the average output current over M cycles still matches with the load. Therefore, switching loss can reduce to N/M. But it can only be applied at no load or very light load (typically 0% to 20% load [67]), otherwise, its uncontrolled default duty ratio will cause over-currents that can damage the devices. An adaptive burst mode control is designed in this section to overcome this issue, so that burst mode can be enabled for a wider load range.

3.3.1. Control loop design

The proposed adaptive burst mode control diagram and its detailed flowchart are shown in Figure 3-8 and Figure 3-9, respectively. V_{out_FB} and I_{out_FB} are the feedback from output voltage and current, respectively. *Burst_count* in Figure 3-9 is a counter to indicate which number of the cycle is the current cycle in the single burst mode period.

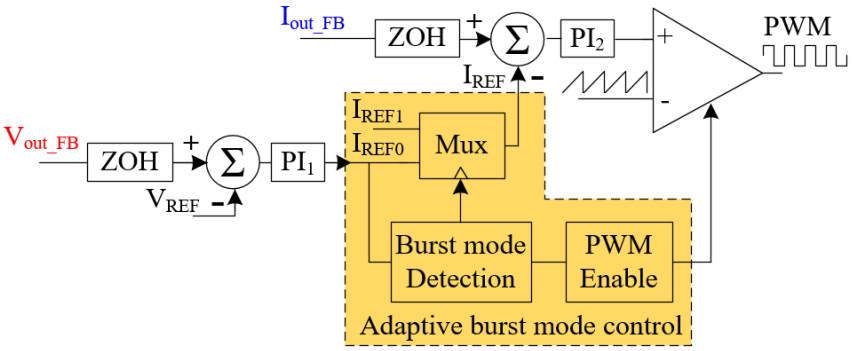


Figure 3-8 Adaptive burst mode control loop.

At the beginning of each cycle, based on the error between V_{out_FB} and voltage reference, V_{REF}, the outer voltage loop produces a current reference, IREF0 that indicates the real required output current. Then, N (the number of PWM enable cycles in a single burst mode period), is calculated by

$$N \cdot I_{REF1} = M \cdot I_{REF0}, \tag{3.18}$$

where, M is the total number of the cycles in a single burst mode period and I_{REF1} is the minimum current reference that can achieve ZVS.

If I_{REF0} is larger than I_{REF1}, N will be larger than M. Then *Burst_count* will always be smaller than N since *Burst_count* is smaller than M. Therefore, the controller will operate in continuous mode and the inner current loop will modify the PWM signal to control the output current to follow the current reference, I_{REF0}. If I_{REF0} is less than

I_{REF1}, N will be less than M. Then, for the first N cycles, burst mode will be active and will force the inner current loop to control the output current as I_{REF1} indicates. During the rest of the 'M-N' cycles, the current loop PI calculation will be skipped, PWM will be disabled, and the converter will stop switching.

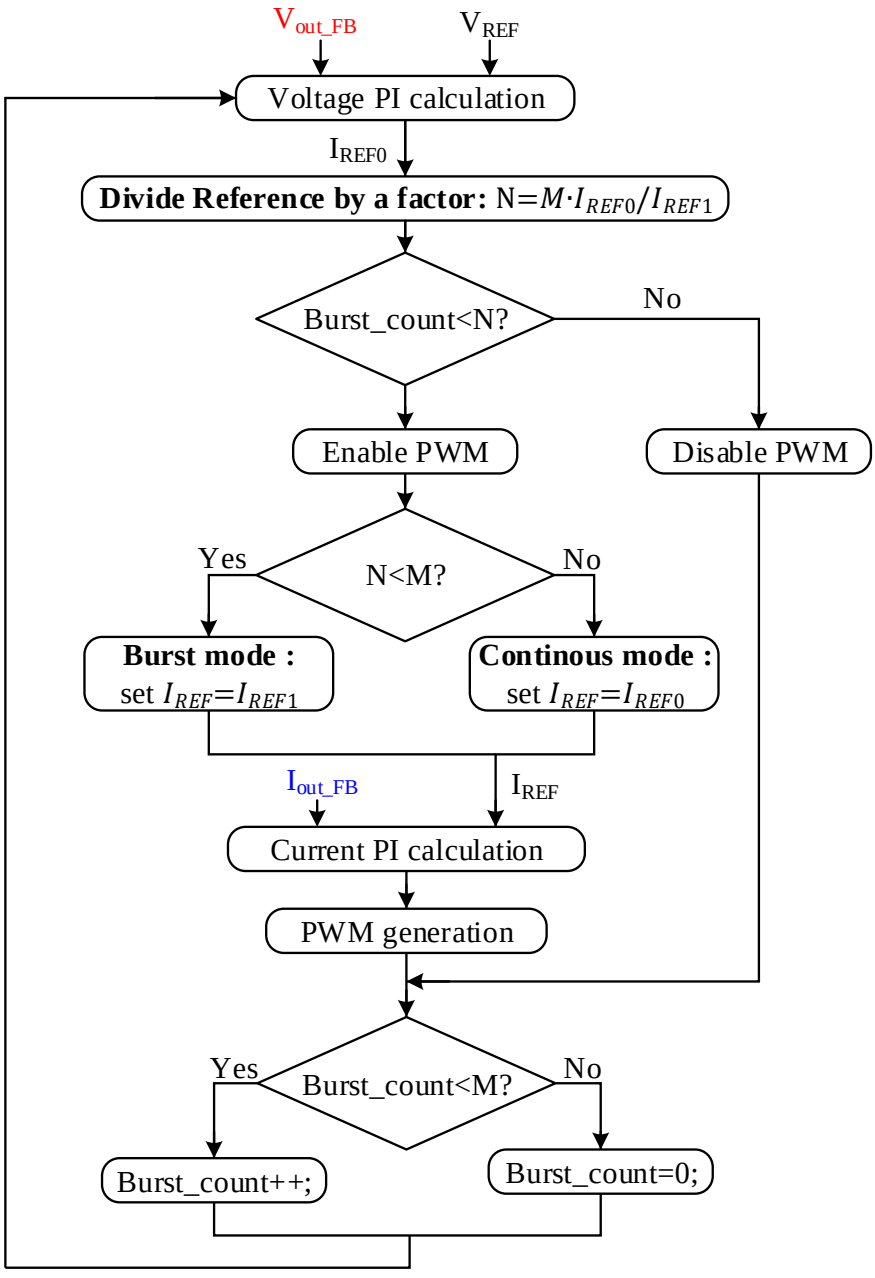


Figure 3-9 Controller flowchart of adaptive burst mode control loop.

Since I_{REF0} is updated by voltage PI every cycle, the burst mode controller can adaptively calculate the N value such that the average output current of the whole burst mode period (M cycles) can match with the real load current.

Since the converter switches for only N cycles in every M cycles, the switching loss is reduced. Besides, these N cycles are under current control with the reference I_{REF1}, so that ZVS can be achieved, and the overcurrent issue can be avoided.

3.3.2. Adaptive current loop PI calculation design

In adaptive burst mode control, the current loop's PI calculation is directly responsible for the control of output current. Since the current reference always has a step change at the beginning of every burst mode period, an adaptive current loop PI calculation is proposed to optimize the step response of the corresponding PI calculation.

The conventional current loop's PI calculation and output current waveform are shown in Fig. 10 (a). The current reference I_{REF} can be defined as in

$$I_{REF} = \begin{cases} I_{REF1}, & 0 < t \leq N \cdot T_S \\ 0, & N \cdot T_s < t \leq M \cdot T_S \end{cases}, \tag{3.19}$$

where, I_{REF1} is the minimum current reference to ensure ZVS and T_S is the converter switching period. It needs to be mentioned that output current frequency is double the converter switching frequency in the PSFB converters.

When the converter starts working in the burst mode, current reference I_{REF} will have a step change at the beginning of the burst mode period, t_0. Then, the conventional current PI controller needs the t_0~t_1 time slot to increase output current to the minimum ZVS current that I_{REF1} indicates, which results in hard switching at t_0~t_1. After t_2, the PI

value is reset to 0 and the same calculation repeats from t_3 to t_5. This method loses a lot of ZVS benefits as shown in t_0~t_1 and t_3~t_4 time slots and increases the N value due to the long start-up time of conventional PI calculation. The conventional current loop PI calculation can be represented as in

$$PI_2(t) = k_P \cdot error(t) + k_I \cdot \int_{t_0}^{t} error(t) \cdot dt, \tag{3.20}$$

$$\text{and } error(t) = I_{REF}(t) - I_{out_{FB}}(t). \tag{3.21}$$

Based on (3.20), it can be noticed that the integration calculation depends on the accumulation of transient error, which causes a long start-up time because the integration value is relatively small at the very beginning, around t_0.

To reduce the start-up time of conventional PI calculation, the integration value at the previous burst mode period can be added to the beginning of the next burst mode period, which can shorten the accumulation time of the transient error. Meanwhile, since the current PI output is stable from t_1 to t_2 as shown in the first burst mode period in Figure 3-10 (a), the error between I_{REF} and output current feedback I_{out_FB} can be assumed to be infinitesimally close to 0 during the stable state. Here, the current loop PI can be represented as in

$$PI_2(t) = k_I \cdot \int_{t_0}^{t} error(t) \cdot dt\,, \quad t_1 < t \leq t_2. \tag{3.22}$$

where, the integration of error(t) is equivalent to A_{S1} (area of S1, same naming method for A_{S2} and A_{S3}), shown in Figure 3-10 (a). Thus, (3.22) can be simplified to

$$PI_2(t) = k_I \cdot A_{S1}, \quad t_1 < t \leq t_2. \tag{3.23}$$

By adding the integration value at t_2 to the second burst mode period, the fast current loop PI calculation as shown in Figure 3-10 (b) can be represented by

$$PI_2(t) = k_P \cdot error(t) + k_I \cdot \left[A_{S1} + \int_{t_3}^{t} error(t) \cdot dt\right]. \quad (3.24)$$

A_{S1} in (3.24) helps current PI to output a higher value, which produces a larger duty cycle after the PWM generator and causes the output current to increase faster than it was in the first burst mode period. When the output current increases to I_{REF1} at t_{4a}, the current PI output is given by

$$PI_2(t_{4a}) = k_P \cdot 0 + k_I \cdot \left[A_{S1} + \int_{t_3}^{t_{4a}} error(t) \cdot dt\right], \quad (3.25)$$

where, $\int_{t_3}^{t_{4a}} error(t) \cdot dt$ can be equivalent to the area of S2. Thus, (3.24) can be simplified to

$$PI_2(t_{4a}) = k_I \cdot (A_{S1} + A_{S2}). \quad (3.26)$$

However, based on (3.23), the stable state current PI output should be $k_I \cdot A_{S1}$. Therefore, the current overshoot will appear from t_{4a}. When the current recovers to I_{REF1} at t_{4b}, the current PI output can be given by

$$PI_2(t_{4b}) = k_I \cdot \left[A_{S1} + A_{S2} + \int_{t_{4a}}^{t_{4b}} error(t) \cdot dt\right]. \quad (3.27)$$

Since *error(t)* is negative at the t_{4a}~t_{4b} slot, $\int_{t_{4a}}^{t_{4b}} error(t) \cdot dt$ is equivalent to -A_{S3}. Thus, (3.27) can be simplified to

$$PI_2(t_{4b}) = k_I \cdot (A_{S1} + A_{S2} - A_{S3}). \quad (3.28)$$

To avoid further under/overshoot, $PI_2(t_{4b})$ should be equal to the stable state current PI output as in

$$k_I \cdot A_{S1} = PI_2(t_{4b}) = k_I \cdot (A_{S1} + A_{S2} - A_{S3}). \tag{3.29}$$

Therefore, A_{S2} should be equal to A_{S3}, which means that the amplitude of overshoot depends on the area of S2. GaN device will get damaged if the current overshoot is too large. Thus, A_{S2} should be as small as possible. The minimum A_{S2} can be approximated as in

$$A_{S2} = \frac{1}{2} \cdot I_{REF1} \cdot (t_{4a} - t_3)_{min}. \tag{3.30}$$

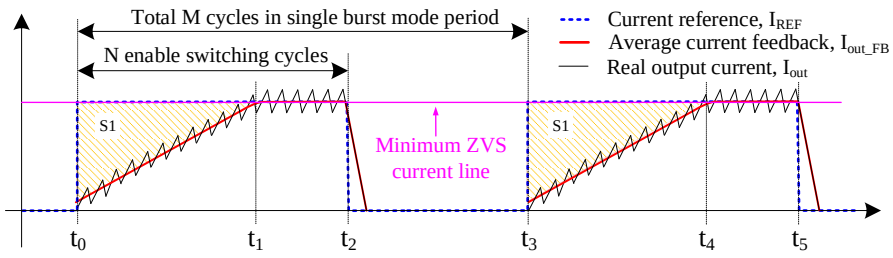
where, t_{4a}-t_3 is calculated by

$$\begin{aligned} t_{4a} - t_3 &= \frac{I_{REF1}}{D\dfrac{V_{in}}{N \cdot L_{out}} - (1-D)\dfrac{V_{out}}{L_{out}}} \\ &= \frac{I_{REF1}}{D\left(\dfrac{V_{in} + N \cdot V_{out}}{N \cdot L_{out}}\right) - \dfrac{V_{out}}{L_{out}}}. \end{aligned} \tag{3.31}$$

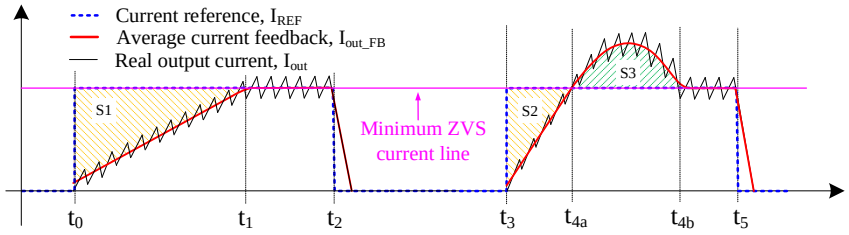
Since input voltage V_{in}, transformer turns ratio N, output inductor L_{out}, and output voltage V_{out} are fixed by converter specifications, only increasing duty cycle D can reduce A_{S2}.

In consideration of duty loss from the primary side to the secondary side and practical application in digital control, maximum duty cycle (less than 0.9, which is based on the discussion in section 3.2.1) may not sufficiently reduce t_{4a}-t_3 for some certain converter specifications.

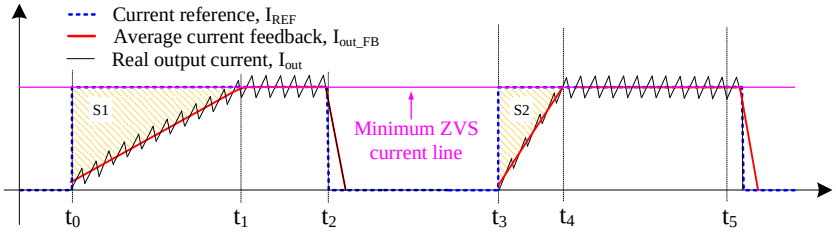
Therefore, the fast PI calculation cannot be generally applied to different specifications, without making certain further improvements.



(a) Conventional current loop PI calculation (slow output current increasing)



(b) Fast current loop PI calculation (fast output current increasing but inherent current overshoot S3)



(c) Adaptive current loop PI calculation (fast output current increasing and no inherent current overshoot)

Figure 3-10 Ideal output current waveforms of different current loop PI calculations.

The root cause of failure of fast PI calculation is that it adds total A_{S2} to the next period's integration calculation, which makes overshoot area 'S3' inevitable. A correction factor k is adopted in the adaptive current loop PI calculation as shown in Fig. 10 (c). k is multiplied to A_{S2} before it is added to the integration calculation in the second period. Then, (26) in fast PI calculation can be change to

$$PI_2(t_4) = k_I \cdot (k \cdot A_{S1} + A_{S2}). \tag{3.32}$$

To avoid any overshoot, $PI_2(t_4)$ should be equal to stable state current PI's output value, which is given by

$$k_I \cdot A_{S1} = PI_2(t_4) = k_I \cdot (k \cdot A_{S1} + A_{S2}). \tag{3.33}$$

Since there is 0 error at the stable state, (3.34) will be true as

$$k_I \cdot A_{S1} = I_{REF1}. \tag{3.34}$$

Then, by combining (3.30), (3.31), (3.33), and (3.34), k can be identified as in

$$k = 1 - \frac{1}{2} \cdot \frac{I_{REF1} \cdot k_I}{D\left(\frac{V_{in} + N \cdot V_{out}}{N \cdot L_{out}}\right) - \frac{V_{out}}{L_{out}}}. \tag{3.35}$$

Figure 3-11 shows the output current results of different current loop PI calculations. Where k=0 is equivalent to conventional PI calculation and k=1 is equivalent to fast PI calculation. The k=0.86 in the adaptive current loop PI calculation is deduced from (3.35).

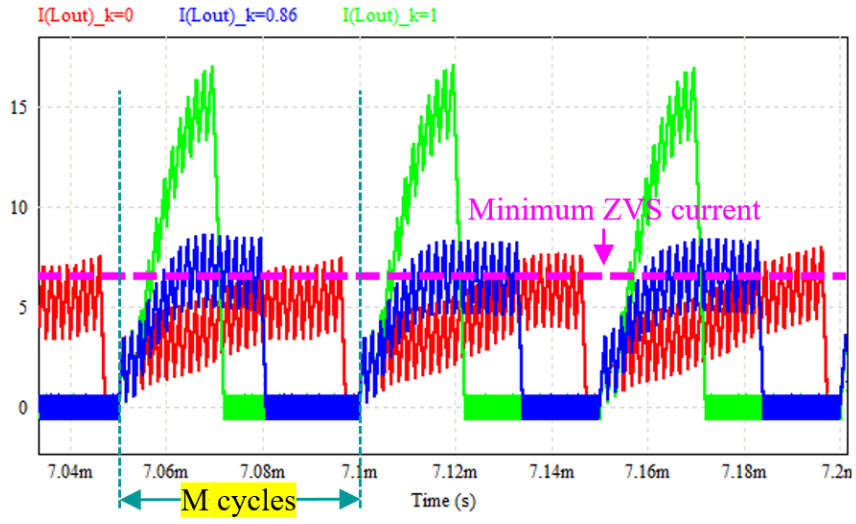


Figure 3-11 Results comparison of different current loop PI calculations. (k=0: conventional PI calculation; k=1: fast PI calculation; k=0.86: adaptive current loop PI calculation)

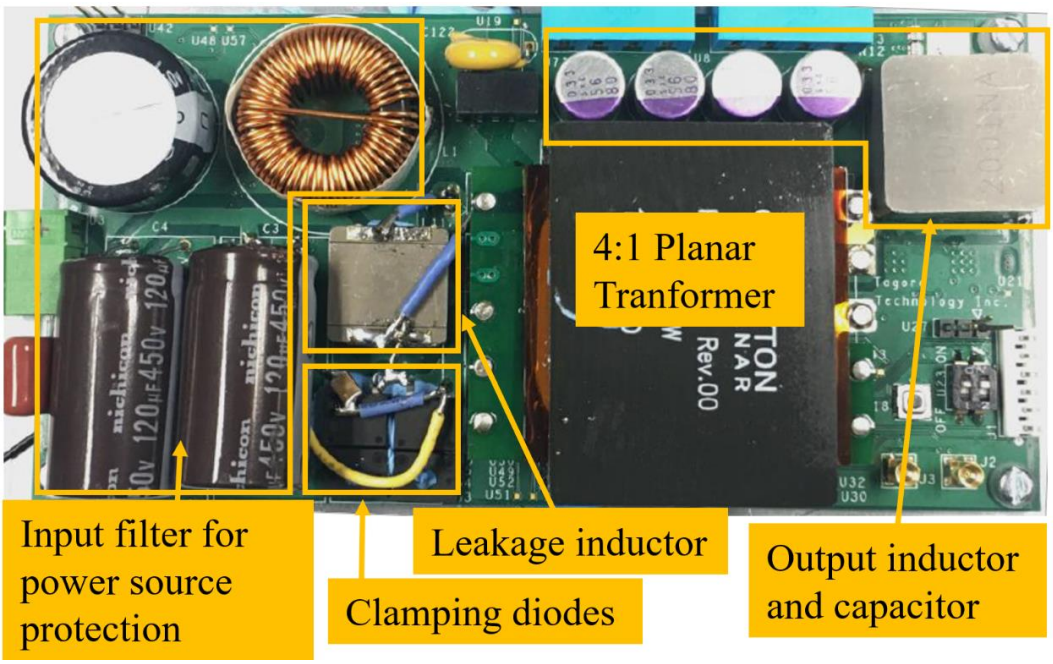
It can be further noticed that conventional PI calculation responds too slowly to the current reference step change. When M is small enough, output current cannot even

rise to the minimum ZVS current in a single burst mode control period. (M is chosen based on the condition that *fs/M* is >20 kHz to avoid audile noise).

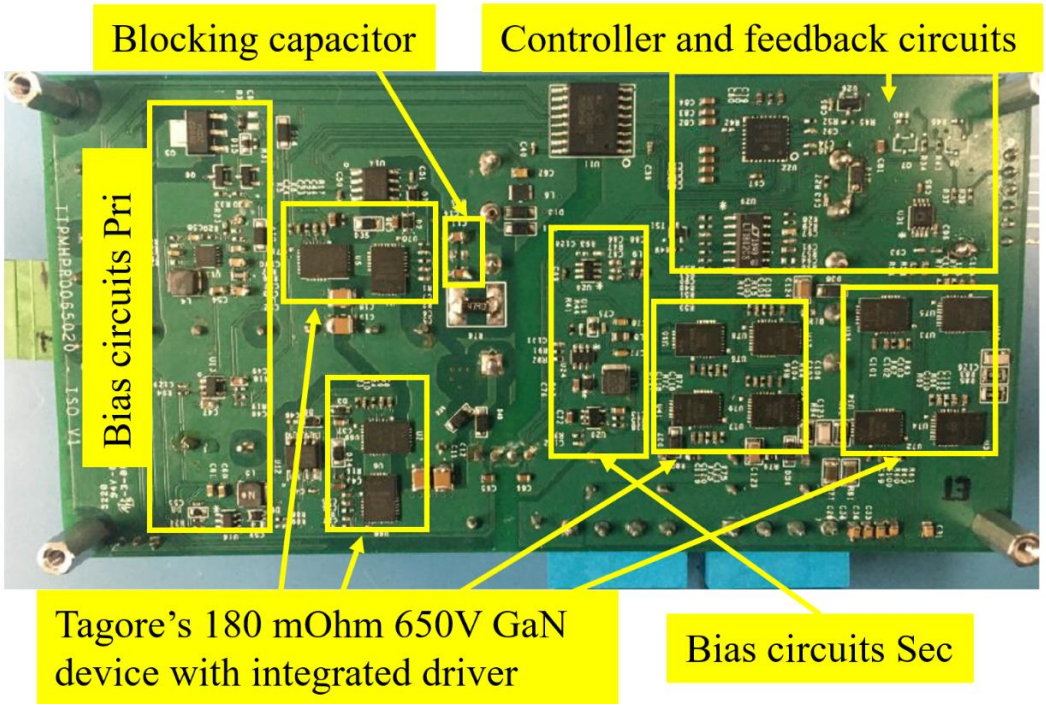
Regardless of the type of current loop PI calculation, the proposed burst mode control can adaptively calculate the N value to meet the average output current requirement in (3.18), which further proves its effectiveness.

3.4. Simulation and test results

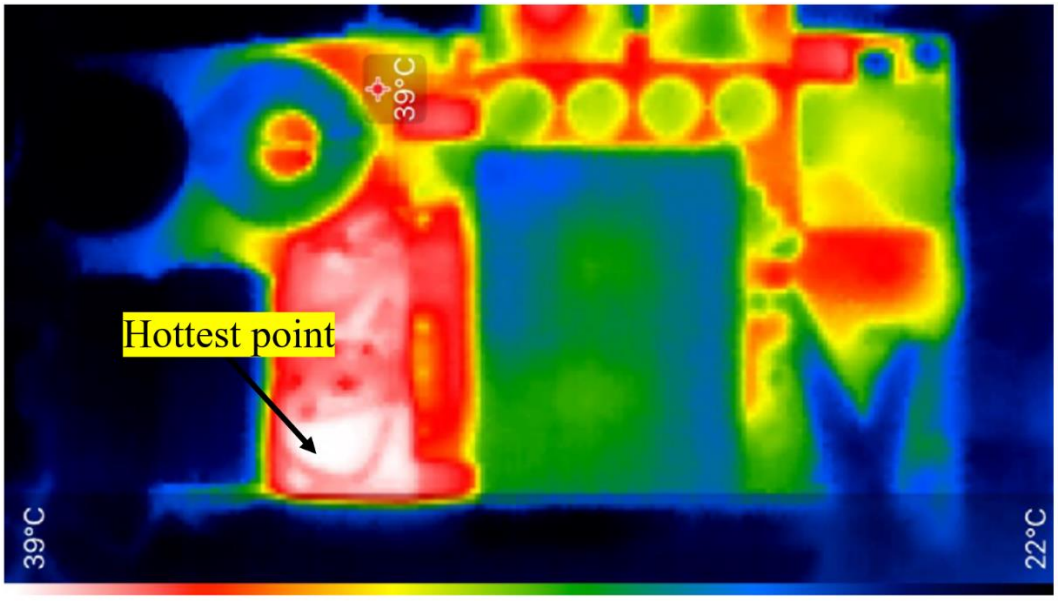
A PSFB converter prototype has been developed to verify the proposed design methods and adaptive burst mode control. The pictures of the hardware and full load thermal image are shown in Figure 3-12. The specifications of the converter and system parameters are given in Table 3.1.



(a) Experimental prototype top view



(b) Experimental prototype bottom view



(c) Full load operating thermal image (160 CFM air cooled)

Figure 3-12 Top and bottom views of experimental prototype, and thermal image at full load (maximum observed temperature is 39 °C).

Table 3.1 Experimental Protype – Specifications and Parameters

Parameters	Values
Input voltage, V_{in}	375 V
Output voltage, V_{out}	70 V
Output current, I_{out}	0 ~ 12 A
Switching frequency, f_s	300 kHz
Blocking capacitor, C_b	2 µF
External Leakage inductor, L_{ke}	3.3 µH
Output inductor, L_{out}	10 µH
Output capacitor, C_{out}	4*68 µF
Turns ratio of the transformer, N:1	4:1
Magnetic inductor of the transformer, L_M	245 µH
Internal leakage inductor of the transformer, L_{ki}	0.8 µH
Total number of switching cycles in single burst mode period, M	15
Minimum current reference to achieve ZVS, I_{REF1}	7.5 A
Correction factor of adaptive current loop PI calculation, k	0.86

It is noteworthy that based on Table 3.1, the minimum current reference I_{REF1} to achieve ZVS is supposed to be calculated as 5.76 A. However, considering the effect of the operating temperature on the leakage inductance and GaN devices' output capacitor (C_{oss}), a 30% margin is adopted to I_{REF1}. Therefore, the final I_{REF1} in Table 3.1 is listed as 7.5 A. In addition, M is set as 15 in this prototype controller, otherwise, a larger M value will produce audible switching noise (300 kHz/15=20 kHz).

Tagore Technology's 180 mΩ, 650 V, GaN FETs (TP44200NM) are adopted as both primary side and secondary side switches in this prototype. Integrated driver

reduces the noise on the gate driver and results in smoother turning on/off. The secondary side switching waveform is shown in Figure 3-13, which proves that diode clamping effectively clamps the V_{SEC} voltage and matches with the simulation result in Figure 3-7 (b). The full load operating thermal image shown in Figure 3-12 can visually prove that the diode clamping doesn't lead to significant power loss since the hottest point is only 39 ^{o}C under fan cooling.

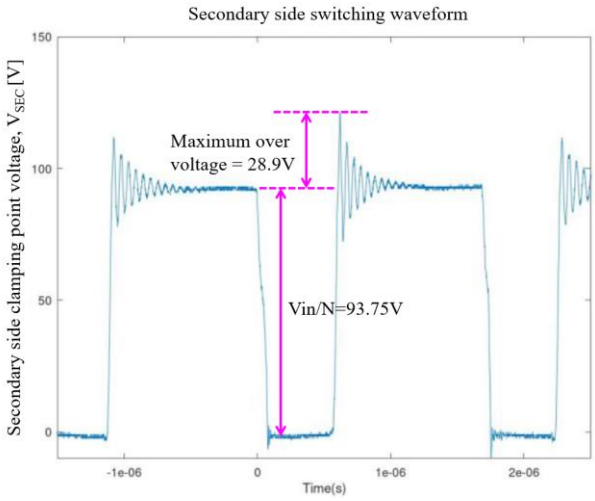


Figure 3-13 Secondary side clamping point, V_{SEC} waveform.

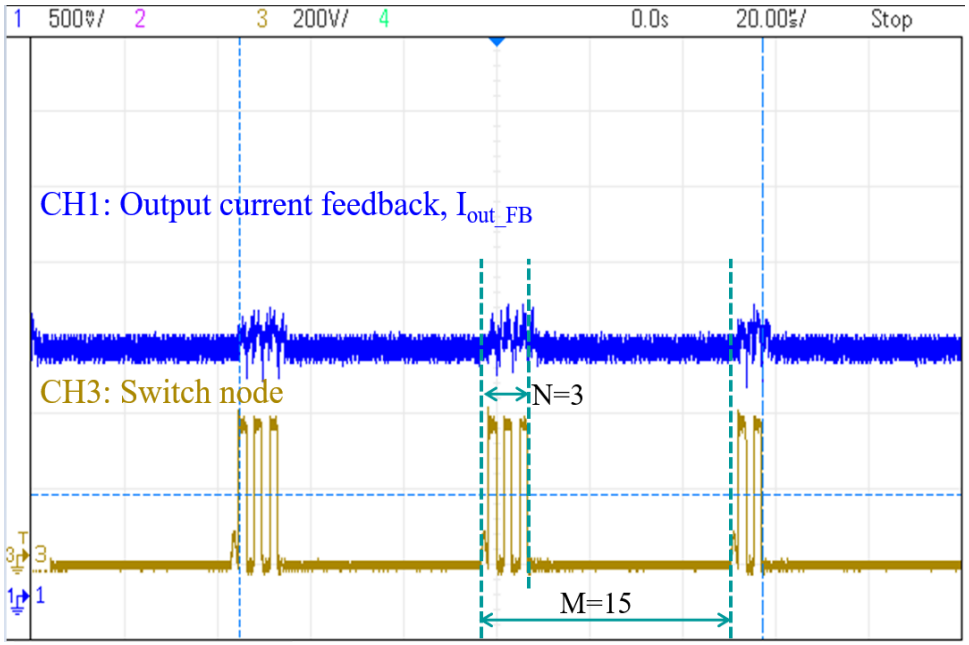
The steady state operating waveforms with the adaptive burst mode control strategy for different load conditions are shown in Figure 3-14. Since the output current cannot be directly probed, the output current I_{out} (before output capacitor as shown in Figure 3-1) feedback signal I_{out_FB} is used to linearly reflect the change in output current. The primary side leading leg's switch node waveform is also included in Figure 3-14 to indicate the number of switching cycles.

At very light load condition, the waveforms in Figure 3-14 (a) shows that the adaptive burst mode control operates similar to the conventional burst mode control, since the N value (number of PWM enabled switching cycles in a single burst mode

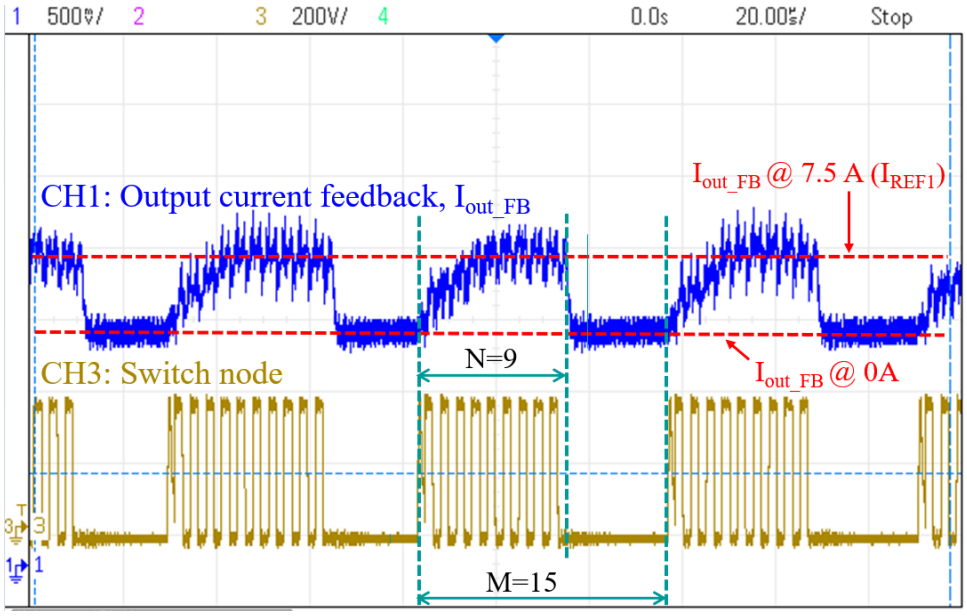
period) is too small for the controller to increase the output current to the minimum ZVS current I_{REF1}.

At light load condition, the waveforms in Figure 3-14 (b) show that the adaptive burst mode control can control the output current as I_{REF1} indicates. Most switching cycles can achieve ZVS to reduce switching loss which is the dominant power loss at light loads. No current overshoot appears when the output current increases, which protects the GaN devices from damages due to over-currents.

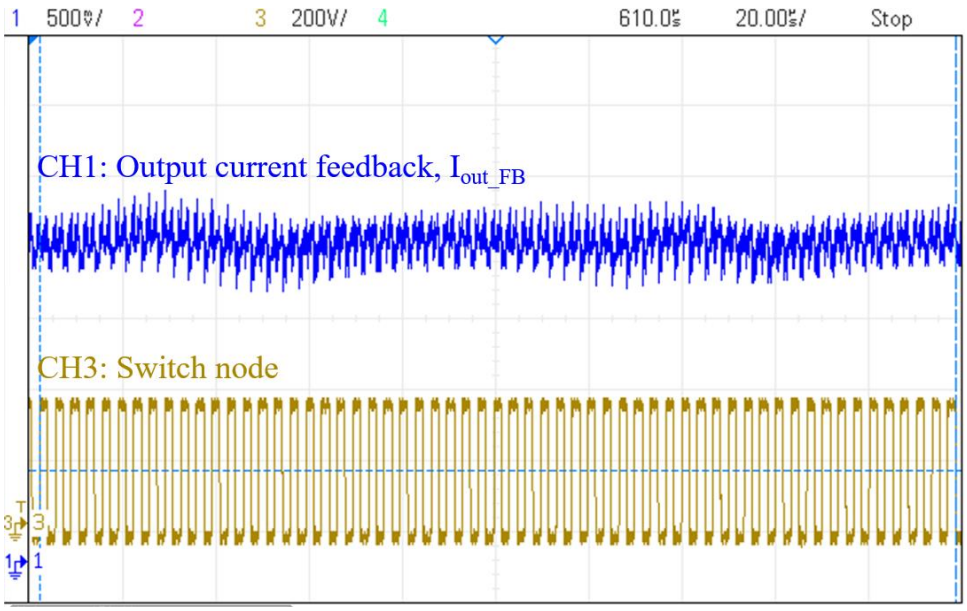
In the ideal case assumption that output current's rising time is infinitesimally small, N is supposed to be 7 to meet this 3.5 A load requirement as 7×7.5 A = 15×3.5 A. However, in a practical application, the output's rising time cannot be ignored. Therefore, N is shown as 9 in Figure 3-14 (b), which proves that the N value is adaptively calculated by the proposed burst mode controller.



(a) Burst mode operation with 300 mA load current (single burst mode period consists of M switching cycles and N cycles are enabled)



(b) Burst mode operation with 3.5 A load current (single burst mode period consists of M switching cycles and N cycles are enabled)



(c) Continuous mode operation with 8 A load current

Figure 3-14 Prototype converter's steady state operating waveforms by adaptive burst mode control with different load conditions. (7.5 A is set as minimum ZVS current reference I_{REF1} to help burst mode operating to achieve ZVS)

At the heavy load condition (over 7.5 A in this prototype), the converter can achieve ZVS naturally. Adaptive burst mode control calculates that N>M. Since the

control forces the converter to switch N cycles for every M cycles, N>M can make it operate in continuous mode. The continuous mode operating waveforms are shown in Figure 3-14 (c).

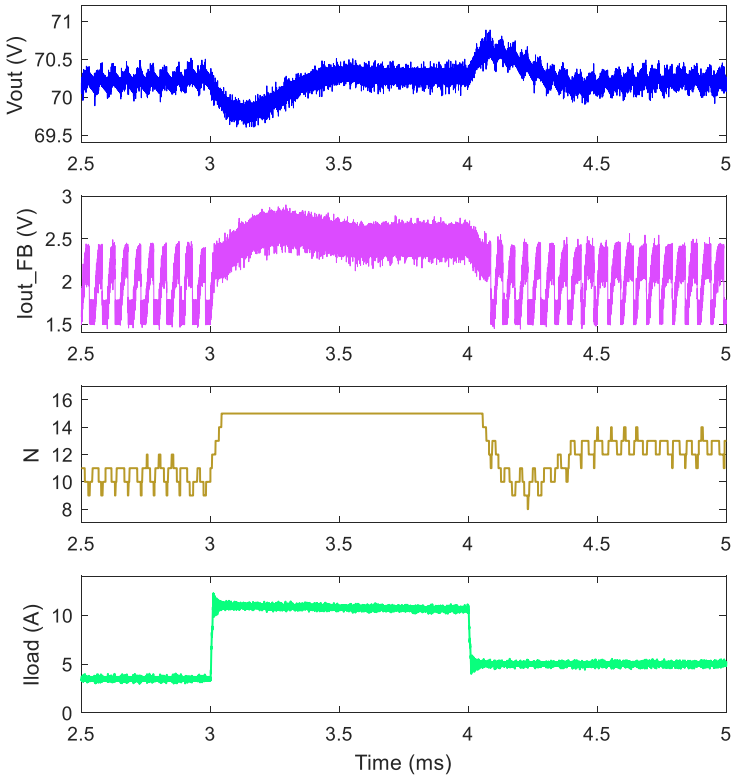
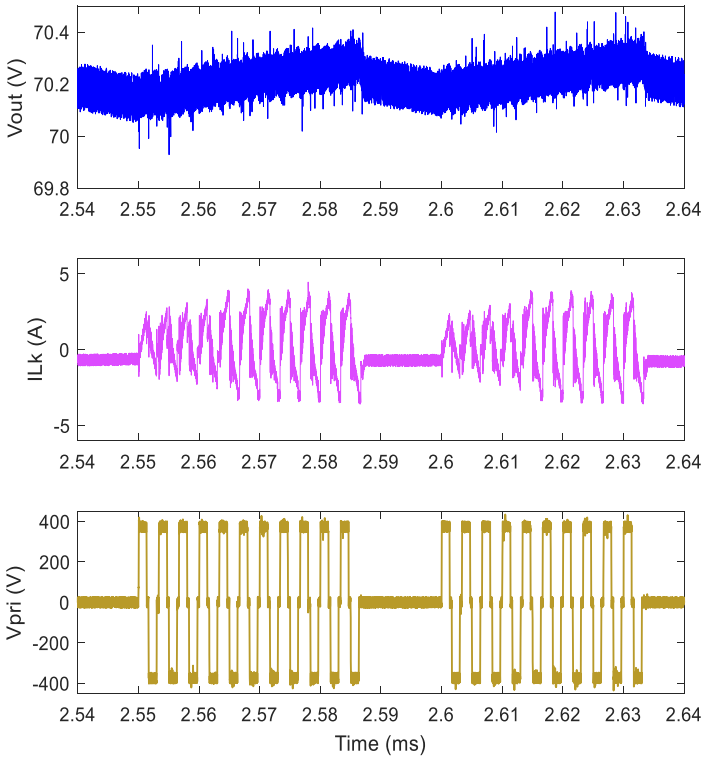


Figure 3-15 Prototype converter load transients (3.5 A to 11 A to 5 A) operating waveforms with adaptive burst mode control. (*N* waveform is the real time value calculated in the microcontroller, *N* = 15 means prototype operates in continuous mode)

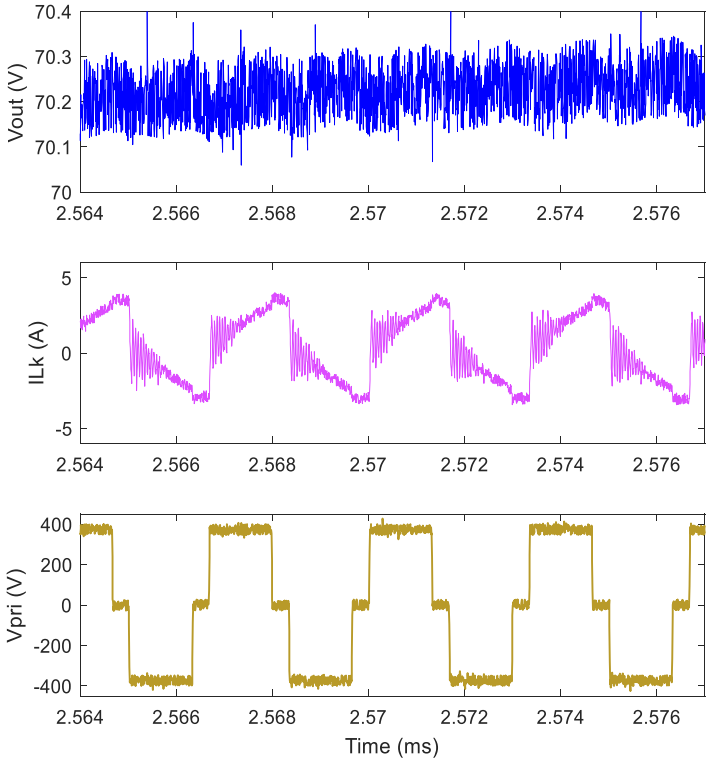
The prototype converter's load transient waveforms under adaptive burst mode control are shown in Figure 3-15. It may be noted that the waveforms shown in Figure 3-13, Figure 3-15 and Figure 3-16 have been plotted using MATLAB based on experimental data captured using oscilloscopes, to combine with other real time data such as N value from the microcontroller to indicate the converter's real time operation. As shown in Fig. 15, the proposed burst mode control can adaptively change the N value based on the different load conditions and can smoothly switch from burst mode to

continuous mode by increase N to 15 (M's value). In every burst mode period, output current (reflected by I_{out_FB}) can smoothly switch between 0 A and minimum ZVS current without any over-current. Less than 1 V output voltage under/overshoots are achieved during the load transients.

The primary side operating waveforms under adaptive burst mode control are shown in Fig. 16, which indicates that the blocking capacitor doesn't distort the transformer current and the proposed control strategy doesn't affect the normal operating of the PSFB converter. The output voltage waveform also proves that adaptive burst mode control doesn't produce large output voltage ripple. Figure 3-17 compares the efficiency of the prototype converter with/without adaptive burst mode control under different load conditions.



(a) Primary side operating waveforms for continuous two burst mode periods. (I_{Lk} is the leakage inductor current and V_{pri} is the voltage difference between the switching nodes of two legs)



(b) Zoomed in waveforms of primary side operating. (I_{Lk} is the leakage inductor current and V_{pri} is the voltage difference between the switching nodes of two legs)

Figure 3-16 Primary side operating waveforms during burst mode.

From the comparison in Figure 3-17, it is obvious to conclude that adaptive burst mode can effectively increase the power efficiency when the prototype converter cannot naturally achieve ZVS (load current less than 7.5 A in this prototype). A significant efficiency improvement of up to 5% is possible when the load current is less than 4.5 A. Moreover, Figure 3-17 also shows that adaptive burst mode control has the benefit of a wider efficiency-improved load range, compared to the conventional burst mode control. Conventional burst mode is typically applied from no load to 20% load (0 A to 2.4 A in this prototype) to prevent continuous uncontrolled duty cycle, producing high peak currents that can damage the devices.

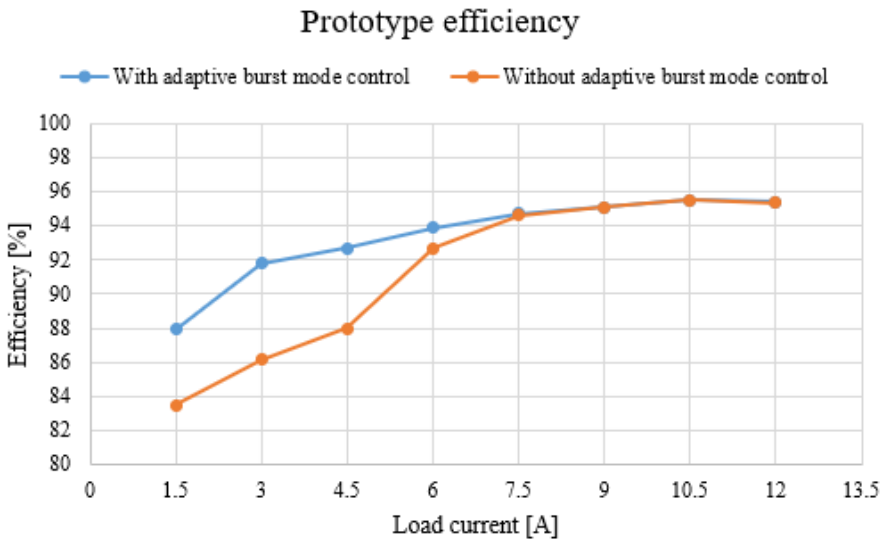


Figure 3-17 Prototype efficiency with and without adaptive burst mode control. (DC biasing power loss is 9 W at no load condition)

3.5. Summary

The main issues faced by GaN-based PSFB converters, such as load-dependent ZVS, transformer saturation, and secondary side ringing, were analyzed in detail and solved in this paper. An adaptive burst mode control was proposed to improve the power efficiency at light load. This adaptive burst mode control could achieve both smaller equivalent switching frequency and smaller single switching loss (ZVS for most switching cycles) at the light load condition, which dramatically improved the light load efficiency. A correction factor 'k' was designed in the current loop PI calculation to ensure that the adaptive burst mode smoothly switches the output current between 0 A and minimum ZVS current. A 375 V input 70 V output 800 W prototype was built, and the test results verify the effectiveness of the proposed approach. The efficiency comparison also shows a big improvement from 88% to 92.5% at around 3 A load current. The proposed approach can be very effective in applications such as laboratory

power supplies, telecom/server power supplies, etc., which usually face a wide range of load conditions.

Paper publication:

Y. Yao, G. S. Kulothungan and H. S. Krishnamoorthy, " Improved circuit design and adaptive burst mode control in PSFB converters for higher efficiency over a wide power range," *IEEE Access* (2nd revision).

CHAPTER 4. IMPROVED PPS DESIGNS FOR PULSED POWER AMPLIFIERS II

To practically realize the second stage fast converter discussed in chapter 2, this chapter presents the advanced improvement designs of GaN based buck converter operating at higher device switching frequency (HDSF) that helps to reduce filter size and increases the overall converter power density as well.

4.1. Digital controller practical issues for over MHz buck converter

HDSF operation requires controllers with high bandwidth and minimum time delay. This can be achieved by analog controllers which are widely used for HDSF converters. On the other hand, digital controllers are more desirable due to their ability to interface with digital systems, lower sensitivity to parameter variations, flexibility to implement sophisticated control schemes, and potentially faster design process [70]. A digital controller for GaN FET converters has been utilized in [71]. The control technique used in [71] is an open-loop voltage control which is not preferred for practical power converters. Moreover, the voltage control is slower than the current control in the buck converter. Hence, a digital current control technique is a better option for GaN-based buck converter. The existing digital current control methods are in the order of a few hundreds of kHz [71][72]. In addition, these methods use a high number of feedback loops, which lead to more computational time and delayed response. These affect the converter's response speed [73]. The delay can be made insignificant if the converter is operated at lower controller bandwidth. However, for GaN-based power converters, lower bandwidth is not preferred in order to achieve fast response.

The conventional two-loop control (outer voltage loop and inner current loop) has been implemented in [74] by utilizing a hybrid control technique on a single-chip microcontroller. It uses a built-in analog comparator of the microcontroller for cycle-by-cycle peak current control wherein the comparator reference is obtained using digital voltage control. The slope compensator and digital to analog converter (DAC) of the microcontroller are used to avoid sub-harmonic oscillation [74]. However, this method can only be applied to switching frequencies of a few hundreds of kHz due to the typical limitations in microcontroller's DAC (slow response time of 400 ns) [75][76]. For HDSF (>1 MHz) operation, the converter needs a DAC with much faster response. A DAC with slow response speed results in improper slope compensation which leads to subharmonic oscillation and causes instability.

Hence, a detailed analysis has been carried out in later sections to analyze the effect of DAC limitation on digital peak current (DPC) control under HDSF (>1 MHz) operation. A digital hysteretic current (DHC) control technique has been developed in this chapter to control the MHz converter without any subharmonic oscillation when microcontroller’s hardware limitation is taken into consideration. The contribution of this chapter is that it provides a detailed comparative study on choosing appropriate control technique for the buck converter for a given microcontroller and switching frequency by considering the hardware limitation. A 70 V to 48 V 2.4 kW 1.5 MHz GaN-based buck converter is designed and simulated to compare the performance of DPC control and DHC control and verify the analysis.

4.2. Digital peak current (DPC) control and related hardware Limits

The schematic of the buck converter with DPC control is shown in Figure 4-1. The inductor current IL and the output voltage V_{out} are fed to the microcontroller. The current and voltage feedback gains are K_i and K_v respectively. The set point V_{ref} is compared with feedback voltage K_v*V_{out} to apply digital proportional and integral (PI) controller. The controller generates digital reference for peak current control V_{PI_out}. To incorporate slope compensation, this reference V_{PI_out} is subtracted with triangle waveform V_{slope} and the resultant value will be converted to analog signal by DAC, to generate analog reference for comparator A1. The comparator output drives the GaN FETs Q_1 and Q_2.

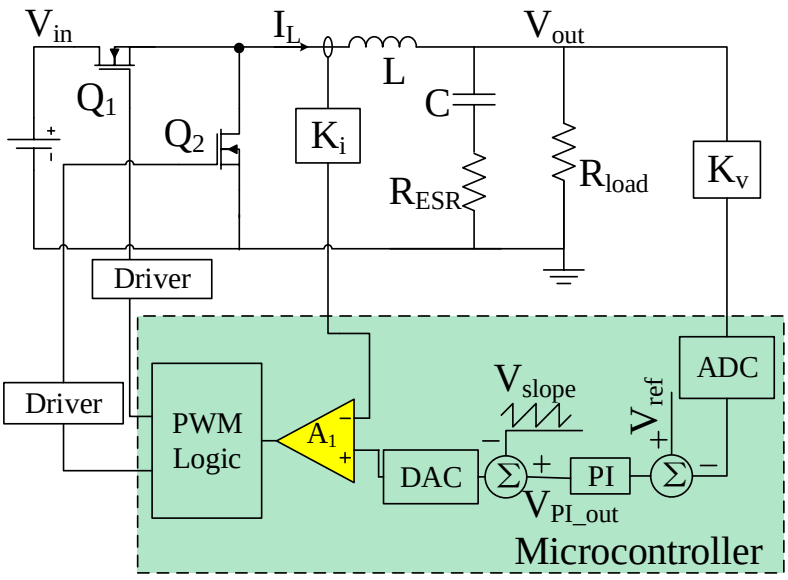


Figure 4-1 Digital peak current control buck converter.

The operating waveforms of DPC control of the buck converter without slope compensation are shown in Figure 4-2 (a). The blue line is the sensed inductor current K_i*I_L in steady state. In DPC control, PI controller provides a current reference V_{PI_out}

to adjust the inductor current and therefore regulate the output voltage to desired level. At the beginning of every cycle, Q_1 is turned on and the inductor is charged using input voltage V_{in}. Hence the current K_i*I_L increases and when it reaches V_{PI_out} the comparator A_1 output goes low. This turns off the device Q_1 and turns on Q_2. The inductor current decreases when the Q_1 is turned off.

From Figure 4-2 (a), it can be observed that when perturbation $\triangle I_L(k)$ is added as green dash line shown, the current magnitude at the end of the cycle (at $t = T_s$) is not same as that of the start of cycle (at $t = 0$). This difference in the current magnitude increases every switching period and leads to instability. A large difference between the current magnitudes at start of the cycle and end of the cycle increases the Q_1 turn on time (greater than the switching period) of as shown by red-dotted waveform in Figure 4-2 (a). In such scenarios the switching frequency is lower than the desired frequency. A continuous change in the switching frequency causes the subharmonic oscillation.

In order to avoid subharmonic oscillation, a slope compensation is adopted in the peak current control technique as shown in Figure 4-2 (b). There are two current waveforms shown in Figure 4-2 (b); the blue waveform shows the desired current waveform and the green (dashed) waveform shows a perturbed waveform from the desired waveform. It could be seen that with the slope compensation the perturbed waveform converges to desired waveform within definite number of switching cycles. The condition on the slope value m_3 of V_{slope} to eliminate the subharmonic oscillation is given by

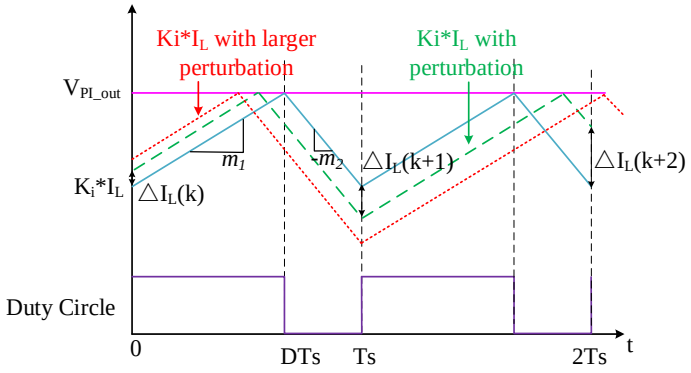
$$0.5 \cdot m_2 < m_3 < m_2, \tag{4.1}$$

where m_2 is the falling slope of the sensed inductor current K_i*I_L. The raising slope m_1 of the inductor current and the falling slope m_2 can be derived using the two switching states of the buck converter and can be obtained as

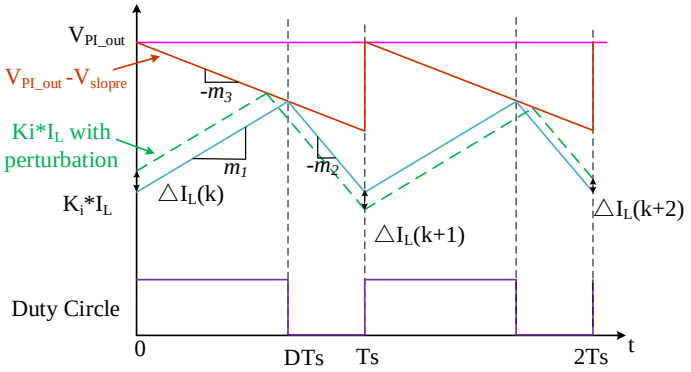
$$m_1 = \frac{K_i(V_{in} - V_{out})}{L}, \tag{4.2}$$

$$\text{and } m_2 = \frac{K_i V_{out}}{L}. \tag{4.3}$$

However, the desired slope V_{slope} as shown in Figure 4-2 (b) cannot be obtained using the microcontroller for HDSF due to performance limitations (conversion and recovering time delays) of the DAC.



(a) without slope compensation



(b) with slope compensation

Figure 4-2 Ideal operating waveforms of DPC control.

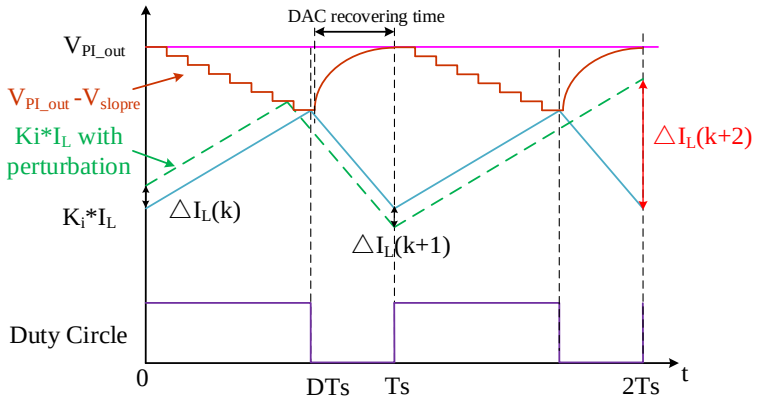


Figure 4-3 Practical operating waveforms of DPC control.

A microcontroller realizable slope compensation waveform is shown in Figure 4-3 with the DPC control. The slope waveform V_{PI_out}-V_{slope} has two regions a slope region and recovery region. The recovery time should be completed before the start of next switching cycle. The fastest recovery time for the microcontroller DAC is 400ns. For the converter switching frequency of 1.25 MHz, this value corresponds to 50%. Hence the microcontroller can only able to provide slope compensation only for duty ratio less than 50%. If the required duty ratio above 50% and if the DAC recovery time is too long, the sensed inductor current cannot be compensated by the slope properly as shown in Figure 4-3. This leads to subharmonic oscillation when there is a $\triangle I_L(k)$ perturbation in the current. The oscillation results in the reduction of the switching frequency, increased output ripple and slow transient response. Hence, the converter might not meet the desired specifications. In other words, when buck converter's switching frequency is higher than 1.25 MHz, most microcontrollers currently available in the market cannot provide sufficient slope compensation because of the DAC recovery time.

4.3. Digital hysteresis current (DHC) control and related hardware limits

The digital hysteresis current (DHC) control schematic is shown in Figure 4-4. The feedbacks to microcontroller are similar as that of DPC control discussed in Section 4.2. The difference is that the PI output reference signal V_{PI_out} is added and subtracted with the hysteresis band $\triangle V_{band}$. Hence two references are obtained using single V_{PI_out} signal. By comparing these references with the sensed feedbacks, the inductor current is limited within the hysteresis band of $2*\triangle V_{band}$.

The operating waveforms of buck converter with DHC control is shown in Figure 4-5. It can be found that the DHC control does not require a slope compensation compared to the peak current control as in Figure 4-2. The perturbation $\triangle I_L(k)$ only affects the phase of the inductor current rather than magnitude. In this control technique, the average inductor current is controlled to V_{PI_out} and the oscillation in the inductor current is damped. This ensures the stability of system. The challenge in using the DHC control technique is that it requires two analog comparators to realize hysteresis comparison. However, this can be overcome by choosing a microcontroller with two analog comparators. The switching frequency of DHC control can be obtained as (4.4) using $\triangle V_{band}$, m_1 and m_2,

$$f_{sw} = \frac{1}{\frac{2\Delta V_{band}}{m_1} + \frac{2\Delta V_{band}}{m_2}}. \tag{4.4}$$

Substitute (4.3) into (4.4), then

$$f_{sw} = \frac{K_i V_{out}(V_{in} - V_{out})}{2\Delta V_{band} L V_{in}}. \tag{4.5}$$

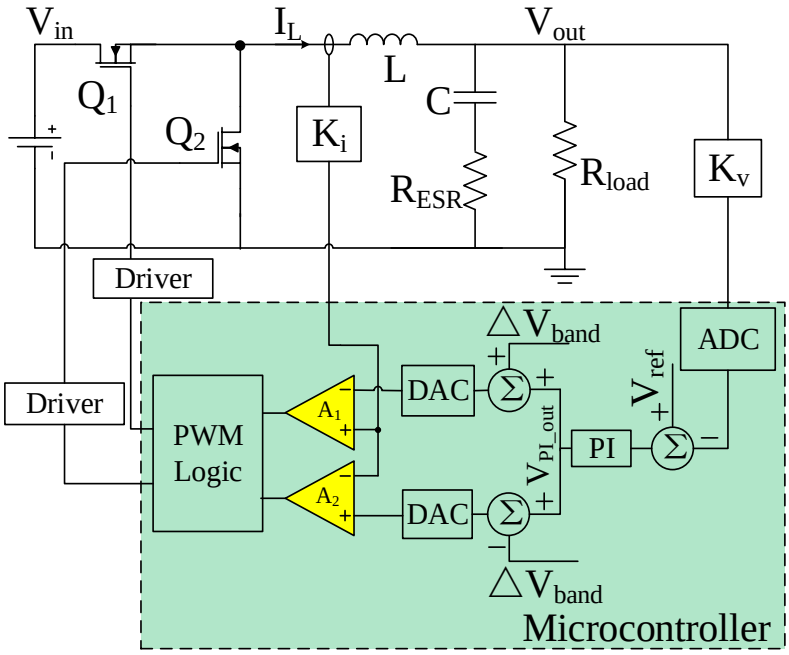


Figure 4-4 Digital hysteresis current control buck converter.

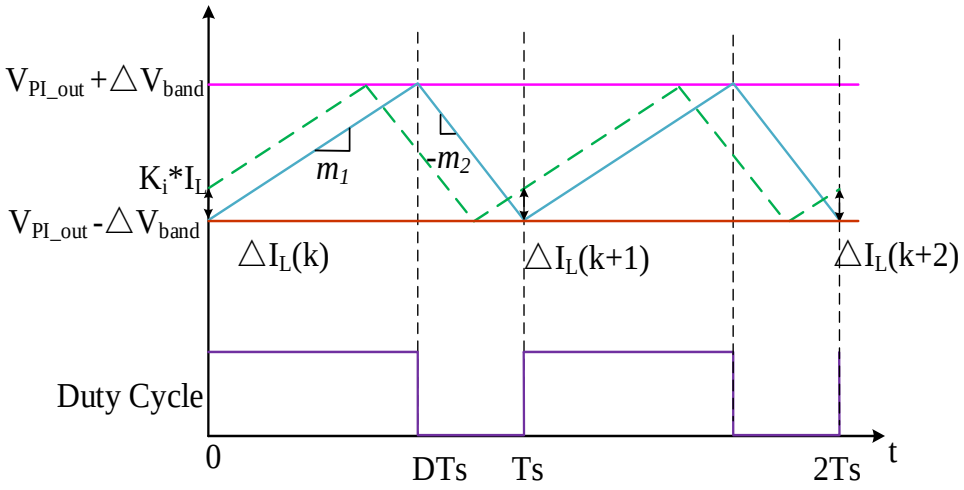


Figure 4-5 Operating waveforms of DHC control.

4.4. Simulation Results

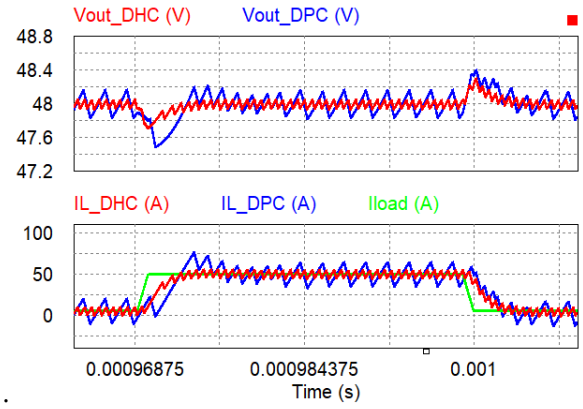
Table 4.1 Specification of designed buck converter

Parameter	Value
Input voltage V_{in}	70 V
Output voltage V_{out}	48 V
Output capacitor C_{out}	282 µF
ESR of output capacitor	6 mΩ
Output inductor L_{out}	1 µH
ESR of output inductor	0.6 mΩ
Switching frequency f_{sw}	1.5 MHz
Load impedance R_{load}	0.96 Ω ~ 9.6 Ω
Output voltage feedback gain K_v	0.05
Inductor current feedback gain K_i	0.04
PI's proportional gain	2
PI's integral gain	4.3
Sampling frequency	5 MHz
DAC recovering time	400 ns

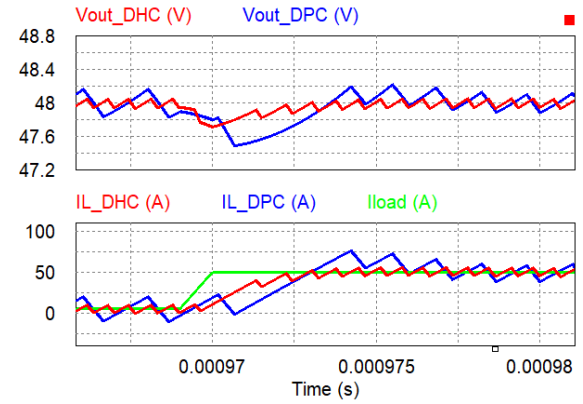
A buck converter is designed and simulated to compare the performance of DPC and DHC control techniques. The specification of the buck converter is shown in

Table 4.1. The GaN system's GaN device (GS61008P) has been selected to evaluate the high frequency converter performance. The power converter is simulated using Power SimTech's PSIM software (version 11.1.7) with SPICE model of the GaN FET devices. Since the outer voltage loops are same in two control methods, the PI configurations are set as same values to ensure fair comparison. PI values are determined based on the small signal model discussed in reference [74]. DAC

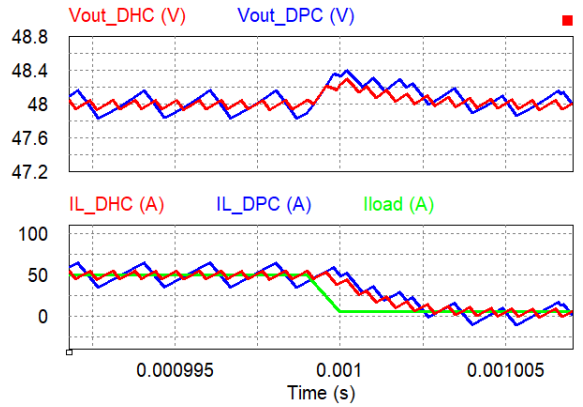
recovering time is included in the simulation and the waveforms of two control methods are shown in Figure 4-6.



(a) Transient response of load step change



(b) zoomed view of transient during rise time



(c) zoomed view of transient during fall time

Figure 4-6 Full load transient response of practical DHC control and practical DPC control.

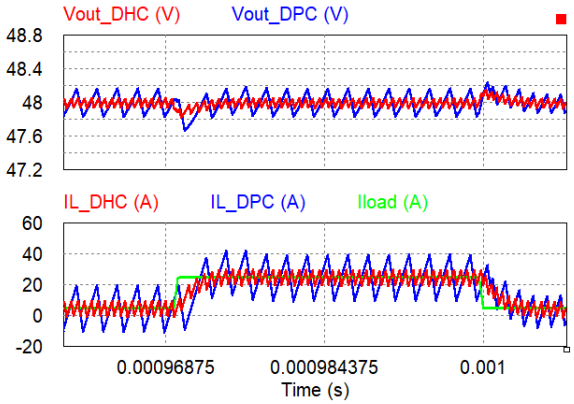
V_{out_DHC} and V_{out_DPC} are the buck converters' output voltages under DHC control and DPC control respectively. I_{L_DHC} and I_{L_DPC} are the corresponding inductor currents. I_{load} is the load current.

It can be noticed that the slope compensation is insufficient in the DPC control since DAC recovering time is 400 ns which corresponds to 60% duty for 1.5MHz switching frequency and results in subharmonic oscillations. Due to the oscillation, DPC control's output voltage ripple is larger and transient load response speed is slower compared with the DHC control.

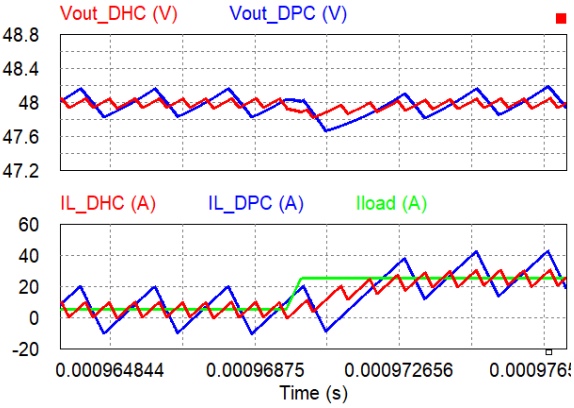
It could also be observed that there are larger undershoot and overshoot during transients using DPC control compared to DHC control. The reason is that in the DPC control technique the inductor current ripple frequency is lower than the switching frequency due to the subharmonic oscillations.

However, during load off transient period the inductor current ripple frequency of DPC control technique is same as that of the desired switching as shown in Figure 4-6 (c). The duty cycle during the transient time is less than 50% and, therefore, even though with improper slope compensation, the desired switching frequency achieved in transient. However, in steady state, the switching frequency is reduced due to improper slope compensation when the duty cycle is above 50%.

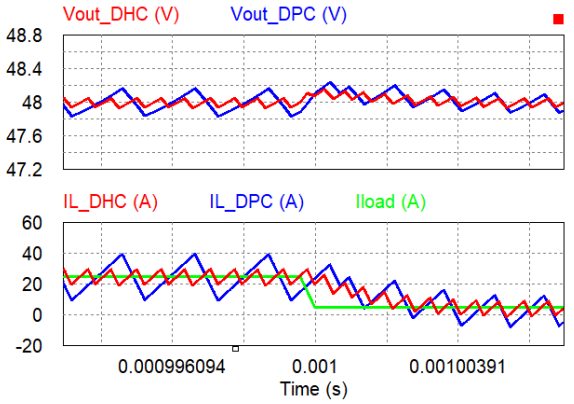
The half load (25A) step change transient response of practical DHC control and practical DPC control is shown in Figure 4-7, which shows that the subharmonic oscillation is not affected by the load current and DHC control can maintain stable output in different load conditions.



(a) Transient response of load step change



(b) zoomed view of transient during rise time



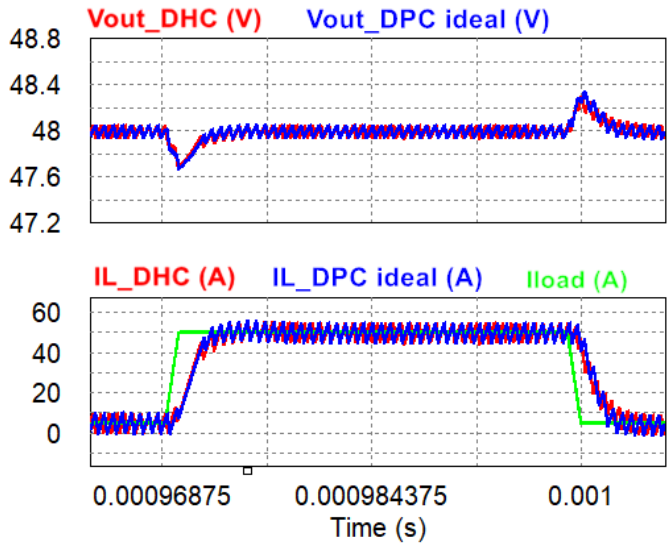
(c) zoomed view of transient during fall time

Figure 4-7 Half load transient response of practical DHC control and practical DPC control.

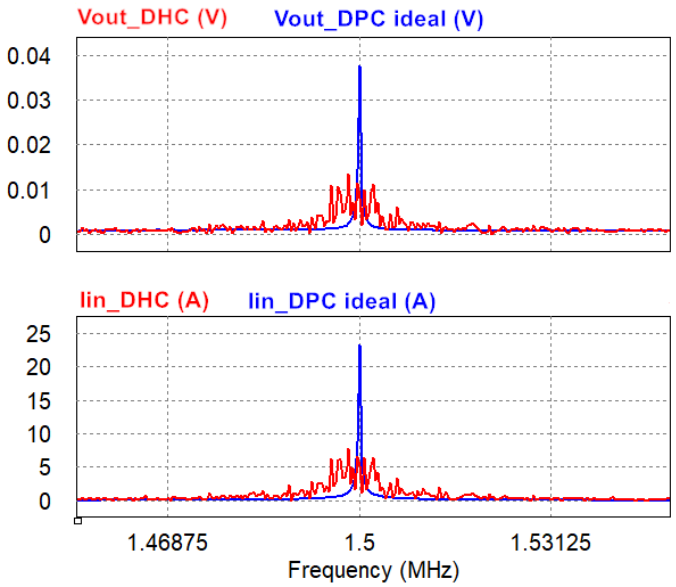
The performance of practical DHC control and ideal DPC control (DAC recovering time becomes zero) is also compared and shown in Figure 4-8. Figure 4-8

(a) shows the transient response comparison between practical DHC control and ideal DPC control, which proves that DHC control can have equivalent performance with ideal DPC control.

The additional benefit in using DHC control is that the switching frequency amplitude (0.04) is distributed among different frequencies with amplitude less than 0.015 as shown in Figure 4-8 (b). This reduces input side filter size when compared to DPC control. Figure 4-8 (b) shows the comparison of the FFT analysis of output voltage and input current of DHC and ideal DPC controls. It can be observed that the voltage and current FFT spectrum with DHC control has multiple frequency components around the desired switching frequency but their magnitudes are small. Whereas, the voltage and current FFTs with DPC control have single frequency component with high magnitude. In other words, DHC control can disperse the switching frequency harmonics, which is helpful to reduce input side filter size and also mitigates the electromagnetic interference issue.



(a) Transient response of load step change



(b) FFT spectrum

Figure 4-8 Performance comparison between practical DHC control and ideal DPC control (a) Transient response, (b) FFT spectrum.

4.5. Summary

For high device switching frequency (>1 MHz) using GaN based power converters, high bandwidth controllers are required. However, due to the microcontrollers' hardware limitations, the conventional digital peak current (DPC) control technique introduces subharmonic oscillation and reduced switching frequency operation on the power converter. In this paper, a detailed analysis and comparison between DPC control and DHC control with hardware limitations have been performed. It was found that the digital hysteretic current (DHC) control can overcome this limitation without compromising on the switching frequency. DHC control achieved reduced output voltage ripple and reduced overshoot/undershoot compared to DPC control. The simulation results of 2.4 kW buck converter with a switching frequency of

1.5 MHz validated the advantages of the DHC control over DPC control technique on GaN FET converters.

Paper publication:

Y. Yao, K. G. Sambandam and H. S. Krishnamoorthy, "Comparative Study on Practical Implications of Digital Peak Current and Hysteresis Current Controllers for MHz Frequency DC-DC Converters," *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2020, pp. 1-5, doi: 10.1109/PEDES49360.2020.9379371.

G. Kulothungan, Y. Yao and H. Krishnamoorthy “Microcontroller-based Trapezoidal Slope Compensation Technique for Peak Current Mode Control at MHz Frequencies" *IEEE Transactions on Power Electronics* (under review).

CHAPTER 5. COMPACT PPS FOR NUCLEAR MAGNETIC RESONANCE (NMR) APPLICATIONS

Nuclear Magnetic Resonance (NMR) spectroscopy utilizing pulsed RF signals has been widely used in several applications such as subsea (or downhole) formation analysis, magnetic resonance imaging (MRI), etc. Since pulsed RF signal's instantaneous power can be over ten times of its average power, converters designed in peak power rating causes lower power density and higher cost, mainly due to the large capacitor bank requirement for energy transfer. The proposed architecture adopts a two-stage topology to reduce the required capacitance by over ten times, leading to a four-fold improvement in power density. The first stage is an isolated converter only supplying average power, therefore input filter and transformer sizes can get reduced. The second stage is a fast response boost converter followed by a RF transmitter to produce pulsed RF signals, so that the mid-point voltage after the first stage can be allowed to droop considerably, leading to a much smaller size of capacitors. Design methodologies for a 150 V DC to 400 V RF, 20 kW peak power converter are described. Simulation results and preliminary experimental results are provided to prove the concepts.

5.1. Conventional power supply for NMR application

Nuclear magnetic resonance (NMR) is widely used in logging while drilling (LWD) and wireline (WL) operations [77][78]. Compared to class A or class AB amplifiers, class D amplifiers have a significantly higher power efficiency to produce RF signals and excite the NMR probe [79][80]. A typical power converter for LWD is

shown in Figure 5-1 [81]. It includes an input filter, an energy storage block and a class D amplifier. As operating waveforms show, the transmitter antenna broadcasts RF signal out during on-state and the receiver antenna collects the echo radio during off-state, after which the waveforms are analyzed to detect the geological structure.

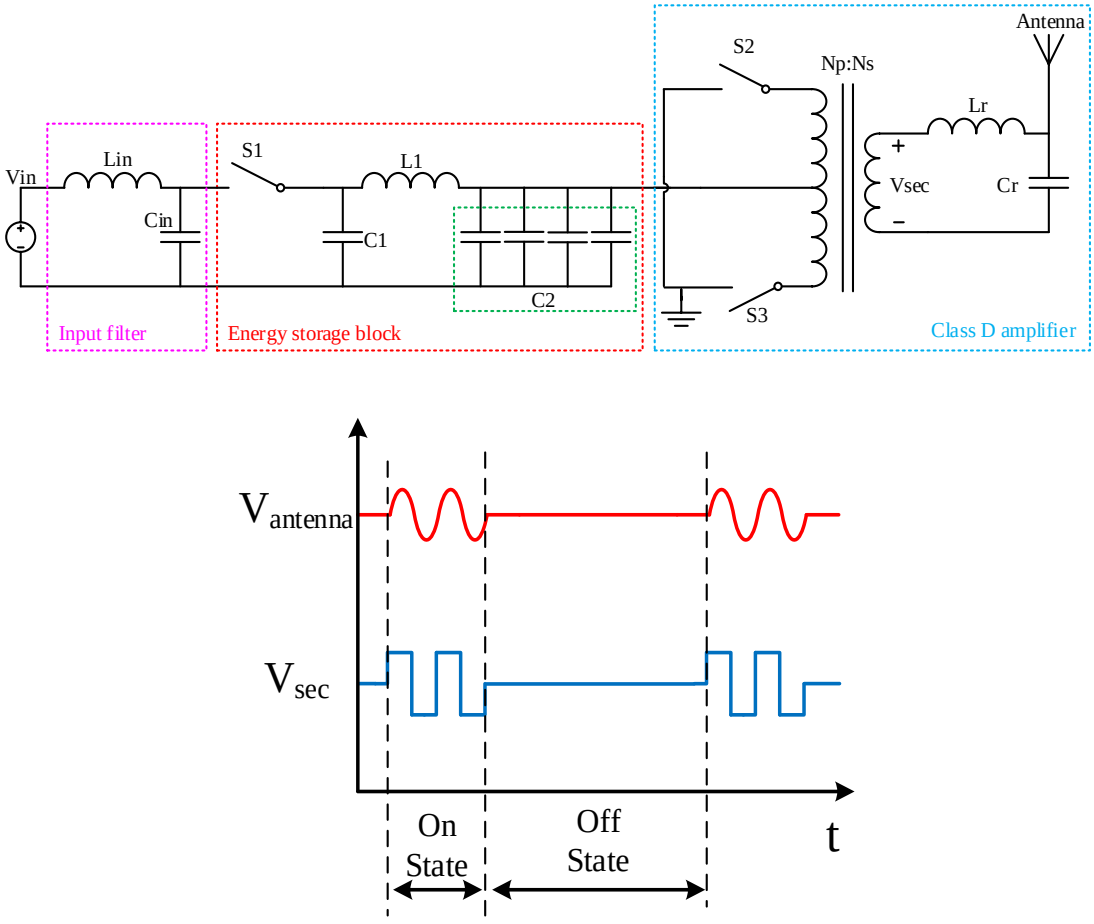


Figure 5-1 Typical power converter for antenna in NMR application and operating waveforms.

The power converter's operating principle is as follows: a) during the off-state, S1 turns on to charge the bulky capacitor C2, class D amplifier is off and transmitter antenna is inactive; b) during the on-state, S1 turns off, C2 supplies the voltage for the class D amplifier, S2 and S3 turn on alternately to produce a square wave which is boosted by the transformer to the secondary side. The boosted square wave voltages

Vsec goes through a LC resonant tank to produce RF sine waveform for the antenna to transmit. Input source Vin does not supply power to class D amplifier directly, otherwise the RF noise may affect the signal integrity. There are three major drawbacks for this type of power converters:

- During the on-state, S1 turns off and the entire energy is supplied by capacitor C2. In order to maintain the linearity of class D amplifier, the voltage across C2 can't drop dramatically. Therefore, large capacitance value (typically millifarads) has to be chosen, which results in a bulky volume, especially in the high voltage application. Due to the extreme environment of downhole applications, high temperature capacitors need to be adopted, which decreases the power density further. To make the matters worse, popular high temperature capacitors such as X7R [82] lose capacitance (by over 50%) at very high temperatures, so redundant design is also needed for such an extreme operating condition.
- In consideration of providing isolation, power converters as in Figure 5-1 need to use transformers with peak power rating (tens of kilowatts [83]-[85]). However, peak power only happens around ten percent of every period, which lead to a plenty of waste on the rating design of transformers. It makes transformer occupy a large volume and increase the cost of the whole power converter.
- Input filter is also needed to reduce the effect of pulse frequency harmonics on input source. The low pulse frequency force input filter's cut off frequency extremely small which needs large inductance and capacitance value. In consideration of high temperature environment and high voltage rating, the input filter also reduces power density heavily.

Focusing on these issues, a novel power converter architecture is proposed in this paper to increase power density, mainly by reducing the size of the energy storage capacitor C2, transformer and input filter – the main passive components in the converter.

5.2. Proposed architecture of system

The proposed two-stage converter architecture is shown in

Figure 5-2 and its main operating waveforms are shown in Figure 5-3. The isolated converter in

Figure 5-2 ensures that the load is isolated to the input source and only transmits the average power to capacitor C_{mid}. Thus, the power rating of this isolated converter will be lower, typically one tenth of the peak power needed by pulsed load. Since C_{mid} is charged by the average power during 90% of the time and discharged by the pulsed power in roughly 10% of the time, the voltage across C_{mid} varies periodically. Therefore, a boost converter is designed as the second stage in this topology to transfer the variable V_{Cmid} to constant output V_{out_boost} as the class D amplifier power supply.

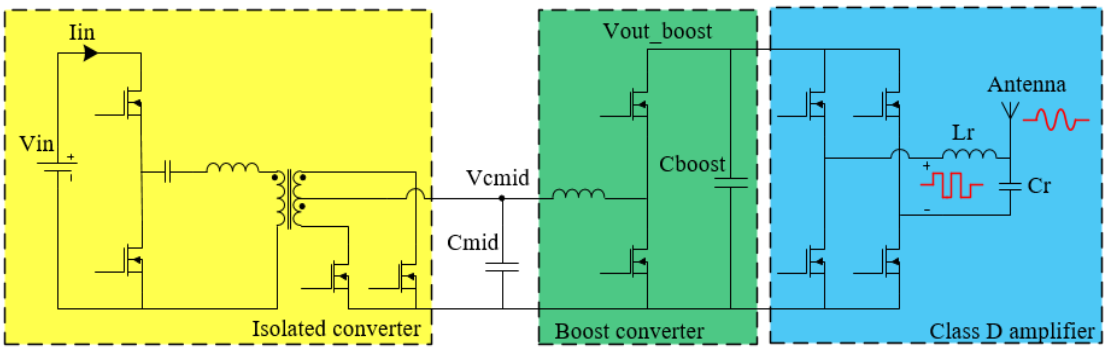


Figure 5-2 Simplified schematic of the proposed power converter for pulsed power in NMR application and operating waveforms.

Three primary benefits are achieved by this proposed topology:

1) The isolated converter outputs nearly constant power, which is the average of the load power in the next stage. Therefore, the power rating of the transformer gets reduced, hence reduces the size and cost.
2) The isolated converter outputting constant power also means that the input current drawn from the source is constant; hence, the pulsed frequency harmonics do not affect other circuits connected to the same input and leads to lower input filter size.
3) Since there is a boost converter to keep the class D transmitter's input voltage regulated, voltage across C_{mid} isn't required to be constant. In other words, as the main energy storage component, the energy utilization factor increases dramatically. Thus, the value of C_{mid} will be significantly smaller compared to the storage capacitor C2 in Figure 5-1.

These three benefits increase the power density of proposed architecture.

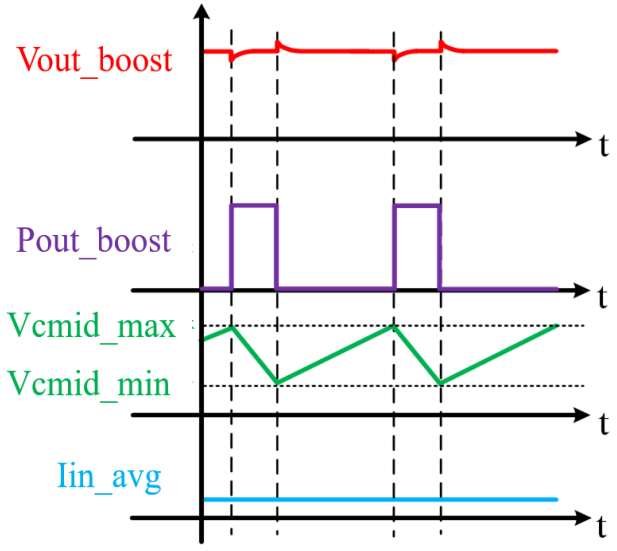


Figure 5-3 Proposed power converter operating waveforms.

5.3. Design and Analysis

A 150 V DC to 400 V RF, 20 kW peak power converter is taken as an example to show the design of parameters. Gallium nitride (GaN) devices GS66516B is used in this application, considering their wide band-gap suitable for very high temperatures and low ESR with high current rating. The specifications of converter are listed in Table 5.1.

Table 5.1 Converter Specific

Symbol	Parameter	Value
V_{in}	Input voltage	150 V
V_{Cmid}	Voltage across C_{mid}	130 V~150 V
V_{out_boost}	Output of boost converter	400 V
$V_{out\_boost\_pkpk}$	The under/overshoot range of boost's output	1%
P_{load_on}	Average load power during on state	10 kW
$P_{load\_on\_peak}$	Peak load power during on state	20 kW
T_{on}	On time of single scaning period	30 us
T_{off}	Off time of single scaning period	270 us
$P_{load\_average}$	Average load power	1 kW
f_{RF}	RF signal frequency	500 kHz
f_{pulse}	Pulse load frequency	3.3 kHz

5.3.1. C_{mid} value design

Since the isolated converter only processes the average power, the power difference between the input and pulse load should be compensated by the mid-point capacitor C_{mid}. From Table 5.1, it can be found that the input power is 1 kW while the

load power (on-state) is 10 kW. Thus, the energy needed from the mid-point capacitor C_{mid}, E, can be deduced by

$$E = (10\ kW - 1\ kW) \times Pulsewidth. \tag{5.1}$$

Here, the pulse width is 30 µs, so E is calculated as 0.27 J by

$$E = \frac{1}{2} C_{mid}\left(V_{Cmid\_max}^2 - V_{Cmid\_min}^2\right). \tag{5.2}$$

If the midpoint voltage is set to a stiff range like 148.5 V $\leqslant V_{Cmid} \leqslant$ 150 V (difference of 1% of V_{Cmid}), the value of midpoint capacitor can be calculated with (5.2). The result is around 1.2 mF which is a very large value. In addition, if the power supply of the class D transmitter has a requirement of 1% variation for the converter in Fig. 1, the voltage variation range for V_{C2} is also 1%, since there is no regulator after the storage capacitor C2. Therefore, the minimum capacitance value of C2 will also be 1.2 mF in this condition (even without considering the high temperature capacitance drift).

In order to reduce the size of mid-point capacitor, the voltage droop range should be maximized to increase energy utilization factor. In Table 5.1, the maximum voltage across C_{mid} is chosen as 150 V to make a fair comparison with the storage capacitor C2 in the conventional power converter, whose bias voltage is around 150 V, if the same input source is used. The minimum voltage across C_{mid} is set as 130 V to allow for a practically achievable step up ratio of boost converter design. Then, the minimum mid-point capacitance value calculated using (5.2) will be C_{mid} = 96 µF, which is 12 times smaller than energy storage capacitor C2 in Fig. 1. In practice, the input current cannot be limited as a single constant value because the average value of the load power always has some drift due to potential changes in pulse-width, devices and application

environment. To deal with this practical drift, the input current should be allowed to vary within a narrow range.

In consideration of certain voltage rating (>150 V) for mid-point capacitors (C2 in conventional topology and C_{mid} in proposed topology), tiny SMD ceramic capacitors cannot be adopted. Therefore, proposed converter's high power density advantage becomes more prominent with the using of aluminum electrolytic capacitor. The practical volume of capacitor C2 in conventional topology and C_{mid} in proposed topology has been compared in Table 5.2. To ensure a fair comparison, both capacitors are chosen from the UCY series from Nichicon company.

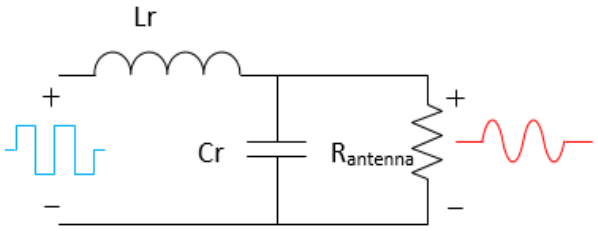
For Table 5.2, it can be obviously concluded that the volume of intermediate capacitor C2 can reduce around 10 times by adopting proposed topology.

Table 5.2 Mid-point capacitor size comparison

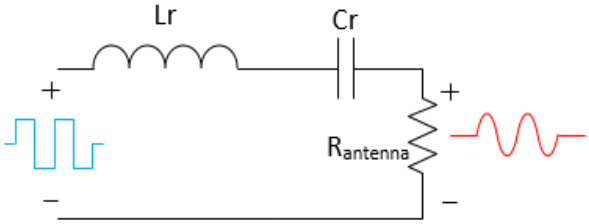
	Conventional topology	Proposed topology
C_{mid} minimum capacitance	1.2 mF	96 µF
C_{mid} practically applied	330 µF*4	100 µF*1
Part number	UCY2E331MHD9	UCY2E101MHD
Unit size (diameter*height)	18mm*41.5mm	16mm*21.5mm
Total volume	42220 mm^3	4321 mm^3

5.3.2. Resonant tank design

The main objective of the resonant tank is transferring the square wave output of H bridge into sine wave for the antenna. Different resonant tank topologies are shown in Figure 5-4.



(a) parallel resonant tank



(b) series resonant tank

Figure 5-4 Different resonant tank topologies.

The transfer functions of series resonant tank *Hs(s)* and parallel resonant tank *Hp(s)* can be derived as

$$H_p(s) = \frac{R_{antenna} // \frac{1}{SC_r}}{R_{antenna} // \frac{1}{SC_r} + SL_r} = \frac{R_{antenna}}{R_{antenna} + SL_r + S^2 C_r L_r R_{antenna}}, \tag{5.3}$$

$$\text{and } H_s(s) = \frac{R_{antenna}}{R_{antenna} + \frac{1}{SC_r} + SL_r} = \frac{R_{antenna} SC_r}{1 + R_{antenna} SC_r + S^2 C_r L_r}, \tag{5.4}$$

where, L_r is the resonant inductor, C_r is the resonant capacitor and $R_{antenna}$ is the equivalent load of the antenna.

Based on (5.3) and (5.4), resonant tanks' amplitude and phase response can be drawn as Figure 5-5.

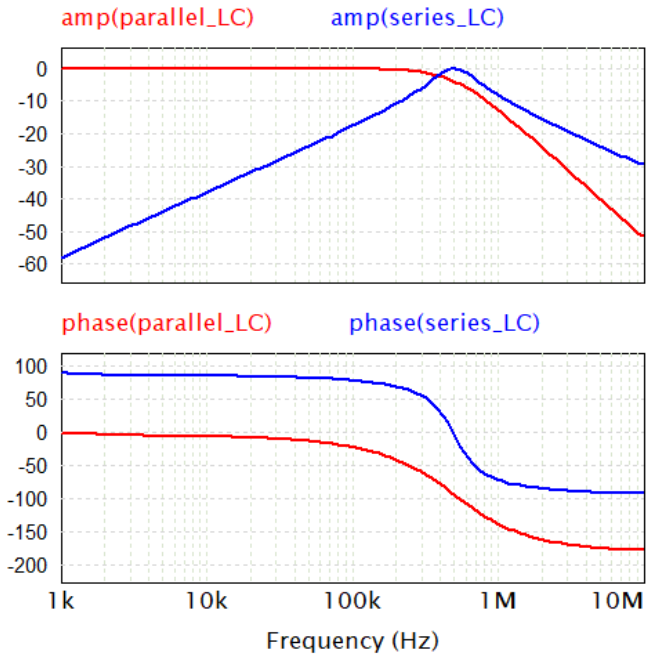


Figure 5-5 Different resonant tanks amplitude and phase response.

From Figure 5-5, it can be noticed that parallel resonant tank operates as a second order low pass filter, which can't filter out the harmonics at pulsed load frequency (3.3 kHz from Table 5.1). Hence, the sine wave has distortion under parallel resonant tank. Besides, the output signal will also have phase delay with respect to the input square wave at the resonant frequency.

In contrast, series resonant tank, operating as a band pass filter, is able to filter out the harmonics at pulse frequency because of the attenuation at low frequency. Therefore, the distortion of the output sine wave can be eliminated. Moreover, the phase delay at resonant frequency is 0 degree, so the sine wave will be in the same phase with input square wave. Thus, series resonant tank is a better candidate for this application.

The resonant frequency can be assumed as $f_o = \frac{1}{2\pi\sqrt{L_r C_r}}$. Thus, the product of L_r and Cr can be finalized. However, if $R_{antenna}C_r$ is too large, the quality factor of the resonant tank will be small, therefore, some harmonics will remain in the output sine wave. Otherwise, if $R_{antenna}C_r$ is too large, it will take longer time for output to rise to the desired levels. Thus, a trade-off should be taken care based on the requirement of output signal slew rate and harmonics requirement.

5.3.3. Isolated converter control loop design

Isolated converter is designed to only outputting average power to next stage, therefore constant power control loop is adopted as shown in Figure 5-6.

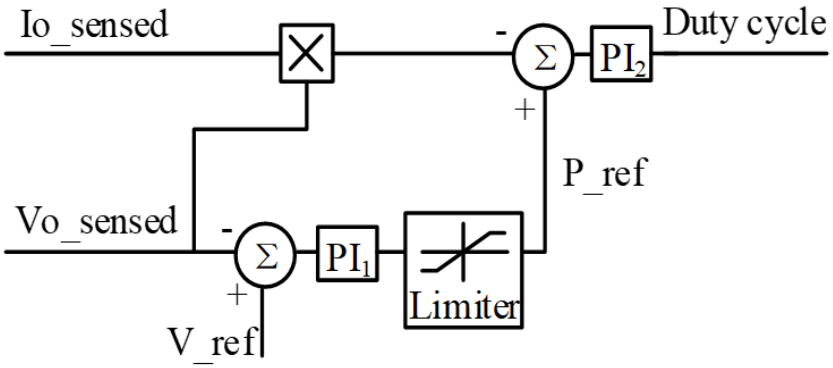


Figure 5-6 Isolated converter close loop controller.

Output voltage *Vo* and average output current *Io* are sampled and sent to controller. Outer voltage loop is designed with a very slow PI_1 (bandwidth is 1/10th of pulse frequency) to produce the constant power reference. The upper limit of limiter is set as the reference of average power at maximum load. For inner average power loop, *Io* and *Vo* are get multiplied to get the power information and PI_2 is designed with a high bandwidth (1/5th of switching frequency) to make sure the average power sensed

can accurately follow the power reference *P_ref*. Due to this average power controller, isolated converter can only output average power and do not response to pulsed load transient.

5.3.4. Input filter design

For standard conducted emissions test [17], the low frequency harmonics caused by load should be limited in the range of Figure 5-7 at the input side.

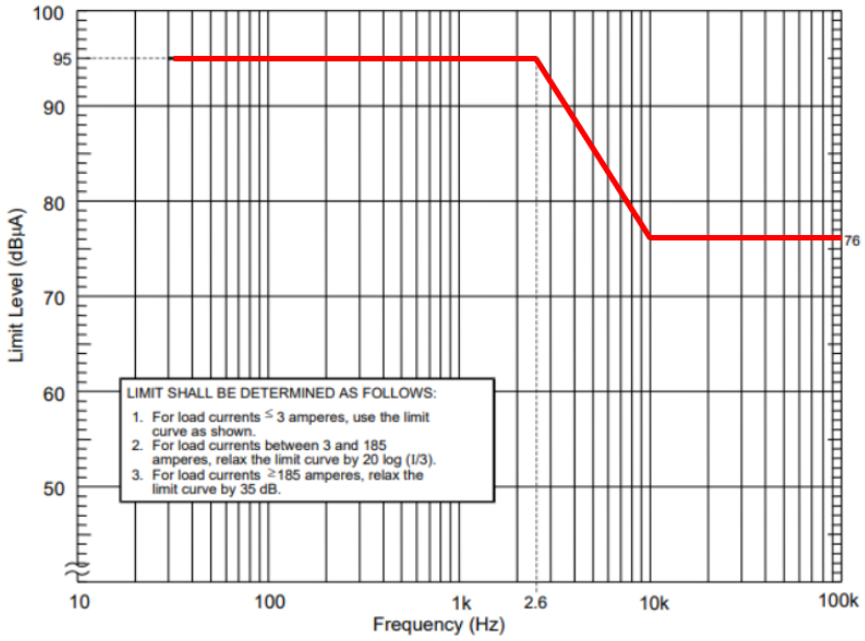


Figure 5-7 Harmonics requirement for conducted emissions test.

Based on this 150 V DC to 400 V RF application, the input side current harmonics at 3.3 kHz pulse frequency should be less than 95 dBuA, which is 56 mA. And the limit for 400 kHz switching frequency harmonics is 76 mA.

The input current of conventional topology can be simplified as a 90% duty cycle (α=0.9) square waveform with 7.4 A peak to peak current (Amax=7.4 A) and 300 us period (T=300 us) as Figure 5-8 illustrated.

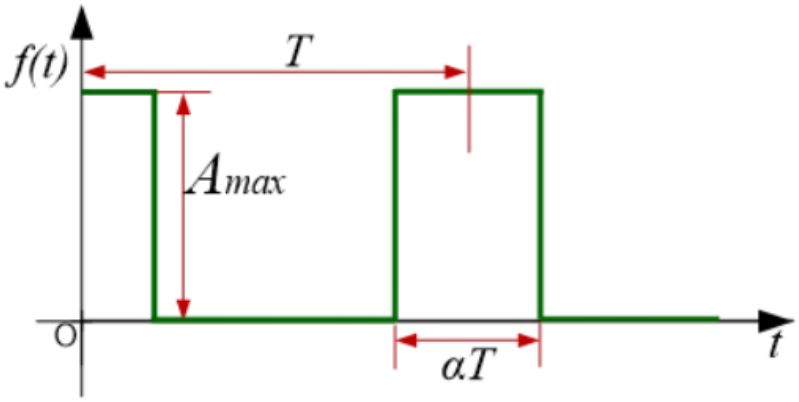


Figure 5-8 Simplified input current of conventional topology.

The Fourier series of a pulse wave is:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(\frac{2\pi nt}{T}\right), \tag{5.5}$$

where,

$$a_n = \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)\cos\left(\frac{2\pi nt}{T}\right)dt. \tag{5.6}$$

Thus, the 3.3 kHz harmonics in this application can be calculated as 1.45 A. To reduce current harmonics from 1.45 A to 56 mA, a -28 dB gain should be achieved by input LC filter at 3.3 kHz. Since LC filter is a second order filter which has -40 dB gain decrease per decade and -12dB gain decrease per double frequency, the LC resonant frequency should be below than (3.3 kHz/10) * 2=660 Hz. To achieve such a low frequency, a 470 μH inductor and 150 μH capacitor have to be adopted in this application.

On the contrast, proposed topology has already set the bandwidth of outer voltage loop at 1/10th of pulse frequency. Since it is a two pole system, the control loop

can naturally achieve -40 dB gain at pulse frequency, so LC filter is completely not needed in the proposed converter. Only some small capacitors are connected at input side to filter out the 400 kHz switching frequency.

The practical volume of input filter in conventional topology and proposed topology has been compared in Table 5.3. To ensure a fair comparison, both capacitors are chosen from the UCY series from Nichicon company. For Table 5.3, it can be concluded that the volume of input filter can reduce around 9 times by adopting proposed topology.

Table 5.3 Input filter size comparison

	Conventional topology	**Proposed topology**
Inductor	470 μH	N/A
Part number	ATCA-08-471M-V	
Size (diameter*height)	42.5mm*21.5mm	
Capacitor	150 μF	100μF
Part number	UCY2E151MHD1TN	UCY2E680MHD3TN
Size (diameter*height)	18mm*26.5mm	16mm*21.5mm
Total volume	37224 mm3	4321 mm3

One thing needs to be clarified that is the input capacitor value in proposed topology is not needed to be as large as 100 μF. The reason of choosing 100 μF is because it shares the same package size with the smaller capacitance values.

5.4. Simulation and experimental results

The simulation parameters are shown in Table 5.4. The model of GaN device GS66516B has been applied for the switches.

Table 5.4 Simulation parameters

Parameter	Value
Isolated converter	
Input voltage V_{in}	150 V
Voltage across C_{mid} V_{Cmid}	130~150 V
Switching frequency f_{iso}	400 kHz
Transformer's turn ratio n_p:n_s	1:1
Isolated converter output inductor L_{iso}	10 µH
ESR of L_{iso}	3.2 mΩ
Isolated converter output capacitor C_{mid}	100 µF
ESR of C_{mid}	5 mΩ
Input decouple capacitor C_{in}	100 µF
ESR of C_{in}	5 mΩ
Boost converter	
Output of boost converter V_{out_boost}	400 V
Switching frequency f_{boost}	1 MHz
Boost converter inductor L_{boost}	4.7 µH
ESR of L_{boost}	1.6 mΩ
Boost converter output capacitor C_{boost}	100 µF
ESR of C_{boost}	5 mΩ
H bridge	
Switching frequency	500 kHz
Resonant tank	
Resonant inductor L_r	10 µH
Resonant capacitor C_r	10 nF
Resonant frequency f_o	500 kHz
Equivalent load resistor $R_{antenna}$	13 Ω

The PSIM simulation waveforms are shown in Figure 5-9. From Figure 5-9, it can be concluded that V_{Cmid} varies in the designed range (130 V to 150 V) and V_{out_boost} variation is less than 1%, which meets the specification requirements.

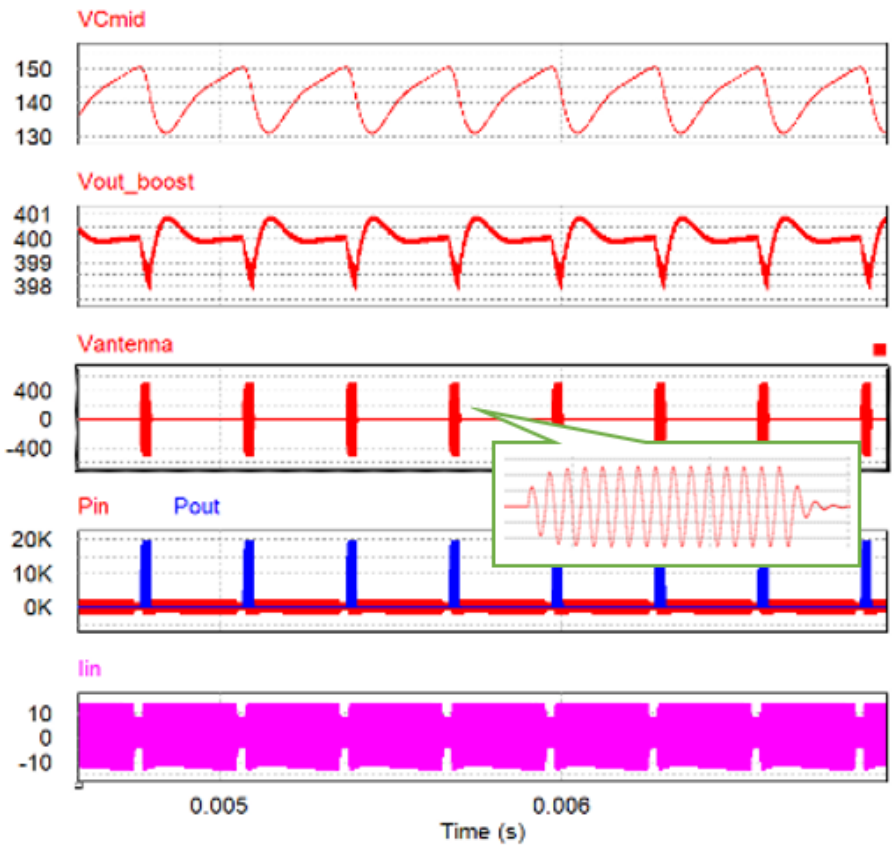


Figure 5-9 PSIM simulation results--(a) Mid-point capacitor voltage [V], (b) Output voltage of boost converter [V], (c) Antenna output voltage [V], (d) Proposed converter input power and output power [W], (e) Input current after input capacitor [A].

The input and output power waveforms show how the pulsed peak power requirement is supplied by the much lower average power, which proves the validity of the proposed topology about reducing the power rating of the transformer. The C_{mid} adopted in this simulation is only 100 µF. Including the 100 µF capacitor C_{boost} and 100 µF C_{in}, the total capacitance is 300 µF in this simulation, which proves that the capacitance is dramatically reduced by the proposed topology compared to the 1.2

mF+150 µF in existing power converters (Figure 5-1). And 470 µH inductor is also eliminated by the proposed converter. From the $V_{antenna}$ zoomed in waveform in Figure 5-9, it can be concluded that the series resonant tank operates properly to produce the sine wave without any phase delay and distortion due to the pulse frequency.

A scaled down laboratory experiment has been done to verify the isolated converter's average power control strategy. It can be noticed from Figure 5-10 that isolated converter can always output average power regardless of the load transient (*I_load*), so that input current (*I_in*) is nearly constant. In this condition, input LC filter for pulse frequency harmonics is completely eliminated by proposed topology.

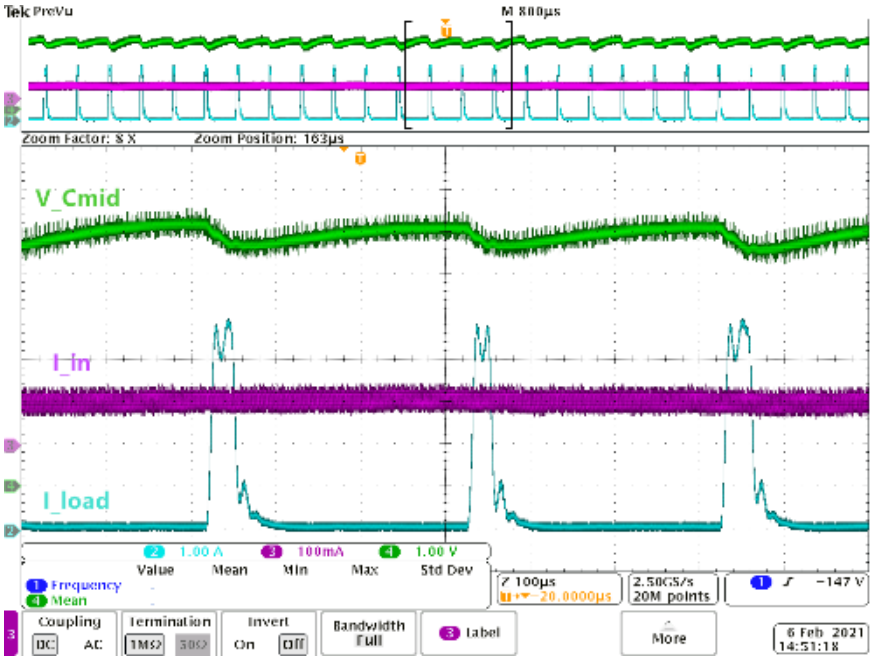


Figure 5-10 Scaled down pulsed load test results—(Ch. 2) Pulsed mode load current [A], (Ch. 3) Input current before input capacitor, (Ch .4) Mid-point capacitor voltage [V].

5.5. Summary

This section proposed a novel power converter architecture that can be applied in pulsed power NMR applications such as in subsea or downhole formation evaluation.

By adopting a two-stage topology, this architecture enforces the isolated converter to only transfer average power, which reduces its power rating and the volume of transformer and input filter. Furthermore, due to the boost converter in the second stage, the voltage stability requirement of the storage capacitor can be relaxed, so the volume of C_{mid} also decreased significantly. A 150 V DC to 400 V RF, 20 kW peak power converter is designed for a pulsed NMR application. Simulation and scaled down experimental results and design analysis are described to prove the validity of proposed topology.

The trade-off for this architecture is it needs more switches than conventional method. However, it can be fixed by adopting GaN devices which has quiet small size and power loss compared with conventional Si based devices. This approach can also be extended to other pulsed load applications such as Magnetic Resonance Imaging (MRI) in healthcare and pulsed radar. This architecture's benefits will be more prominent when the passive components are required in higher voltage rating and higher operating temperature.

Contribution:

1. A novel power converter architecture has been proposed and it can be applied in pulsed power NMR applications such as in subsea or downhole formation evaluation.
2. Proposed topology reduces the volume of transformer, input filter and C_{mid} due to unique control strategy.

3. A 150 V DC to 400 V RF, 20 kW peak power converter is designed for a pulsed NMR application. simulation, scaled down experimental results and design analysis are described to prove the validity of proposed topology.

Paper publication:

Y. Yao and H. S. Krishnamoorthy, "High Density Power Converter Design for Pulsed NMR Applications," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 5927-5932, doi: 10.1109/ECCE47101.2021.9596051.

CHAPTER 6. LINEAR ASSISTED FAST RESPONSE PPS

This chapter presents a linear assisted DC/DC converter to increase the response speed and power density of pulsed mode applications, including radar systems. The proposed architecture includes two power paths: (1) a full bridge converter as a high power path for voltage control to efficiently process the main power and (2) a linear amplifier as a low power path to achieve fast response speed by compensating current difference between high power path and pulsed mode load. Hence, though the high power path responds slowly, output voltage variations during pulsed transients can be reduced. GS66516B, 650 V Gallium Nitride enhancement mode high electron mobility transistors (GaN E-HEMT) are used as switching devices to enable higher operating frequency with less loss. Finally, a 400 V to 28 V, 900 W converter is designed for a 4 A (average) / 32 A (peak) pulsed load scenario. Simulation results and design analysis are described, proving the concept.

6.1. Existing linear assisted DC/DC converter

Pulsed power electronics, including radars, are widely used in modern applications, such as autonomous electric vehicles, weather forecasts, naval systems, etc. Power amplifiers (PAs), as the main loads in such power applications, operate in pulsed mode, which requires high energy in short bursts. PAs are traditionally supplied by power converters with large capacitors to avoid huge voltage variations that may harm the linearity of PAs and insert noise to the outputs of PAs. However, large capacitors reduce the power density, which causes a big issue in space-constrained environment, such as in a ship or an aircraft. For radars in naval ships, thousands of

transmit receive modules (TRXMs) are included to provide the final stage of amplification for transmitted signals and the first stage of amplification for received signals. Thus, inside the TRXMs, thousands of PAs are used, operating in pulsed mode. Figure 6-1 shows the power supply structure for a pulsed radar system with PAs. There will typically be hundreds of conversion units equipped with large capacitors, which will occupy huge space in a ship [34]. Moreover, since so many large capacitors are used, the reliability also becomes a significant concern.

An active capacitor converter has been proposed in [86] to reduce the number of capacitors, but it intentionally increases the output voltage ripple and can only be applied in low voltage and low frequency pulsed load conditions. A buck converter with active ramp tracking control has been proposed in [87] to achieve fast load transient response, but high switching frequency produces a lot of switching loss and reduces the power efficiency. A resonant converter topology has been adopted in [88] to supply power for pulsed load so that the switching loss can decrease, but its switching table control strategy for different loads delays the response speed and results in large output voltage variation. It can be concluded that in the application of pulsed load, it is difficult for single power converter to achieve small output capacitance, small output voltage variation, and high efficiency at the same time. Therefore, linear assisted power converters are proposed to solve this problem.

Several linear assisted power converter topologies have also been proposed before for other applications, to increase the response speed, and reduce the voltage variations. A series combination of DC/DC converter and linear amplifier has been presented in [89] for envelope tracking. It is a two-stage topology having the benefits

of fast response speed and small output capacitor, but it comes from the trade-off of low power efficiency because all the current flow through the linear stage. Some parallel combinations have also been proposed. For example, in [90]-[92], buck converters are used to supply main power, and linear amplifiers are used to improve response speed, but the control strategies are very complex. A band separation scheme is adopted in [93], but it has a high requirement on the cut-off frequencies matching between the four filters and, therefore, easy to be impacted by extreme application environments. Independent controls on the linear stage and switching stage are explored in [94], but the combiner (two diodes) between these two stages constrains the minimizing of the voltage variations caused by load transient changes, which has a negative influence on the PA's linearity.

To address these issues, this paper proposes a single-stage hybrid topology with two parallel power paths, adopting a full bridge converter as a high power path in parallel with a linear amplifier as a low power path to achieve high efficiency and fast response speed simultaneously.

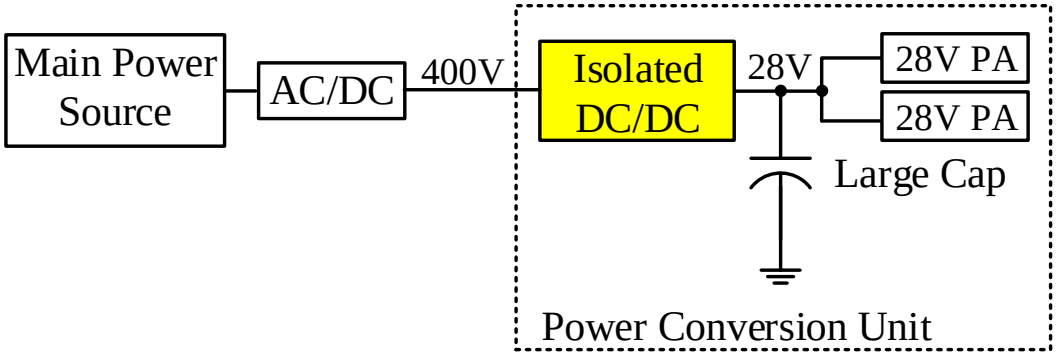


Figure 6-1 Power supply structure in a typical pulsed application with Pas.

A half bridge DC-DC converter is adopted to step down the input voltage and supply the linear amplifiers for efficiency improvement, which also makes PA loads

isolated to the high input voltage. Since linear amplifiers in low power paths only convert power at pulsed load change transients, a half bridge converter can supply power for tens of linear amplifiers at the same time. Thus, for a power supply of a pulsed radar that contains thousands of PAs, the space occupied by the half bridge converters can be shared by every single linear assisted DC/DC converter module to optimize space. 650 V Gallium Nitride enhancement mode high electron mobility transistors (GaN E-HEMTs) are used in the power stage to reduce switching losses. The advantages of proposed topology are as follows:

- High efficiency since linear amplifier only allows small transient power.
- Smaller output capacitor because of linear amplifier stage's fast response speed.
- Easier control strategy since high power path only deals with voltage feedback and low power path only handles current feedback, which allows these two power paths to operate in parallel without any control conflict.
- Economical for long lifetime application due to the smaller output capacitor.

6.2. Proposed architecture of the system

Figure 6-2 shows the block diagram of the proposed topology. The half bridge DC/DC converter in the low power path supplies voltage to multiple linear amplifiers in different low power paths. The proposed topology includes two power paths. The high power path is responsible for keeping output voltage constant and supplying main power to PAs load at high efficiency. The low power path senses the pulsed load current and only responds to the high frequency part of the transient change of load current by utilizing a high pass filter. It doesn't supply any current during the steady states, which

minimizes the low efficiency drawback of the linear amplifier. Since the high power path only takes care of output voltage and the lower power path only controls output current, these two paths don't have any conflict about operating in parallel. In other words, neither special control strategy nor combiner as in [93][94] is needed for the parallel operation, which also makes it easy to design frequency compensation for the control loop.

The operating principle of this topology is illustrated with the idealized waveforms in Figure 6-3: (1) At average power state, only high power path outputs current I_{hp} to PAs load I_{load}, low power path is off. (2) when I_{load} increases suddenly, due to its slow response speed, high power path gradually increases I_{hp} but cannot supply enough current to I_{load} timely. Thus, energy stored in output capacitor is used to supply for I_{load}, which drops the output voltage V_{out}. In the meantime, since low power path can respond to the high frequency part of transient change of I_{load}, it supplies current I_{lp} to compensate the current difference between I_{load} and I_{hp}, which reduces the current supplied by the output capacitor. Thus, V_{out} will not drop dramatically although output capacitor is small. Then I_{hp} increases to objective value and low power path turns off again. (3) when I_{load} decreases suddenly, high power path decreases I_{hp} but still due to its slow response speed, there is a period during which I_{hp} is larger than I_{load}. Thus, excess energy would be stored into the output capacitor, which would increase V_{out}. The low power path responds to the high frequency part of this I_{load} transient change and pulls most excess current to the ground, which reduces the voltage spark in V_{out}. Then I_{hp} decreases to steady value, and the low power path turns off again. Since most of the power flows through the high power path, which is highly efficient and low power path

only works during I_{load} transient change periods, the drawback of linear amplifier's low efficiency is minimized.

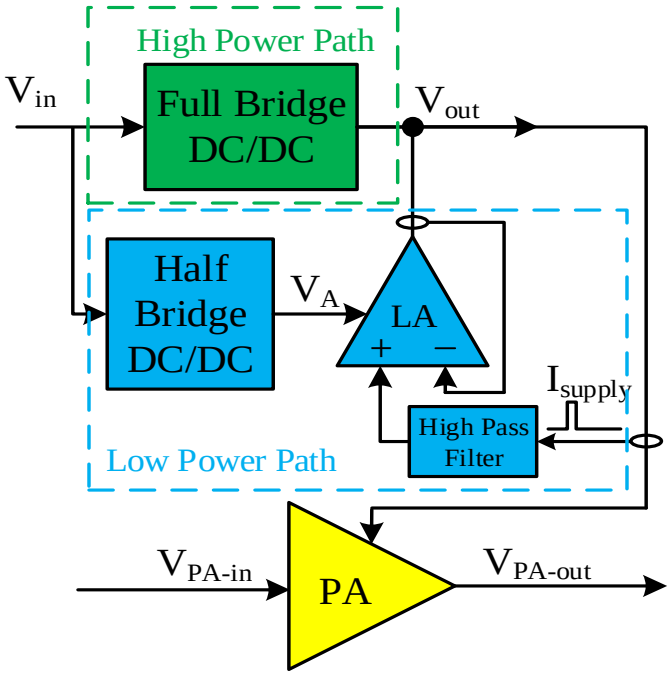


Figure 6-2 Block diagram of the proposed architecture.

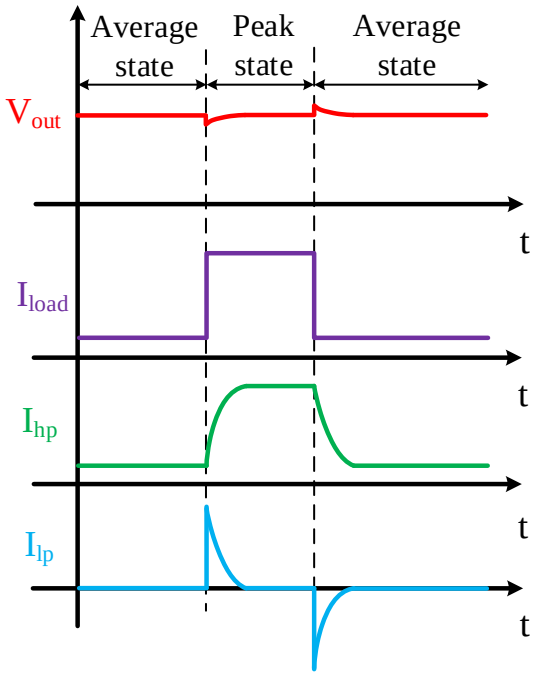


Figure 6-3 Idealized operating waveform.

6.3. Design and Analysis

6.3.1. High power path

The schematic of the converter is shown in Figure 6-4. The high power path involves an efficient full bridge converter. Only voltage control loop is adopted in this converter to maintain the constant output voltage. Current control loop is not needed here because current sharing can be processed by the current control loop in low power path, which makes it easier to design frequency compensation for this full bridge converter. Optimal switching frequency is chosen based on the trade-off between switching loss and sizes of L_1 and C_1, where the value of L_1 and C_1 can be calculated by [95]

$$L_{min} = \frac{\frac{n_2}{n_1}V_{in} - V_{out}}{\left(\frac{I_{out_{peak}-peak}}{t_{on}}\right)}, \tag{6.1}$$

$$\text{and } C_{min} = \frac{I_{out_{peak}-peak}}{\left(\frac{V_{out_{peak}-peak}}{t_{on}}\right)}, \tag{6.2}$$

where, n_1:n_2 is the transformer turns ratios, V_{in} is input voltage, V_{out} is output voltage, $I_{out_{peak}-peak}$ is the peak to peak value of output current, $V_{out_{peak}-peak}$ is the peak to peak value of output voltage, t_{on} is the on-state time every period. Since GaN E-HEMTs are used as switching devices, the operating frequency can be set a little higher, which means ton can be smaller for smaller L_1 and C_1.

More efficient soft switching resonant converters are not adopted as the high power path because in consideration of PAs operating in pulsed current load, converter

output current changes in an extremely wide range, which means the equivalent load resistor varies in a wide range. In the meantime, since the voltage transfer ratio is high in this application, the turns ratio $n_1:1$ is also large. This wide variation of load resistor and large turns ratio cause resonant tank's quality factor to change dramatically with load change, which means it is hard for a resonant converter to get soft switching during the entire output range. Thus, resonant converter is not an ideal option for this high voltage transfer ratio and wide load current range application.

6.3.2. Low power path

The schematic of high power path is also shown in Figure 6-4. A half bridge converter and linear amplifier are connected in series to compose the fast response speed low power path. The half bridge converter is used to step down input voltage to V_{out} plus a certain value (typically the threshold voltage of power MOSFET Q_7), so that Q_7 can work in saturated region and dissipate least power loss. Half bridge converter is adopted here because it can reduce the number of devices to achieve space saving. In addition, since only very small portion of current flows through low power paths, a half bridge converter is set as suppling voltage to tens of linear amplifiers in different low power paths to save the space further. This half bridge converter is also set to switch at higher frequency to reduce the size of transformer and output LC-filter.

Linear amplifier consists of two stages as shown in Figure 6-4. Amplifiers A_1 and A_2 are the first stage and responsible for amplifying the error voltage. MOSFET Q_7 and Q_8 compose of the second stage and are responsible for amplifying current. Two separate amplifiers are used in the first stage to control Q_7 and Q_8 independently to avoid

Q_7 and Q_8 turning on simultaneously, which will lose a lot of power and decrease the power efficiency.

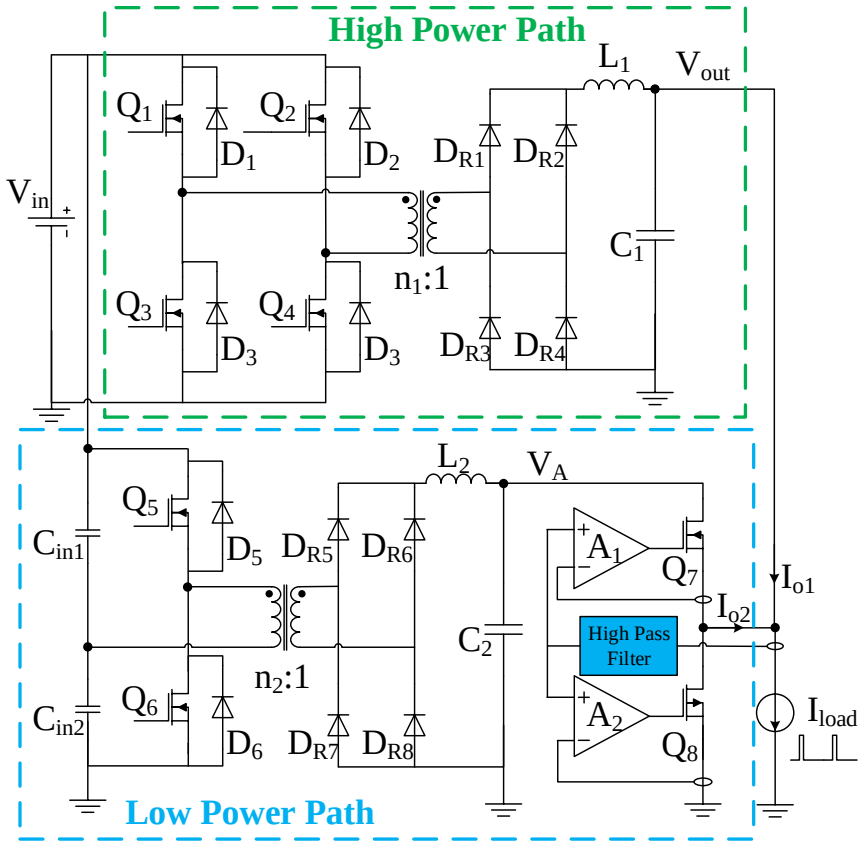


Figure 6-4 Schematic of proposed topology.

The cut-off frequency of high pass filter is designed based on the bandwidth of full bridge converter in high power path. The transfer function of full bridge converter is given in [96]

$$G(s) = \frac{\frac{n_2}{n_1}V_{in}}{s^2LC + s\left(\frac{L}{R_{load}} + R_dC\right) + \frac{R_d}{R_{load}} + 1}, \tag{6.3}$$

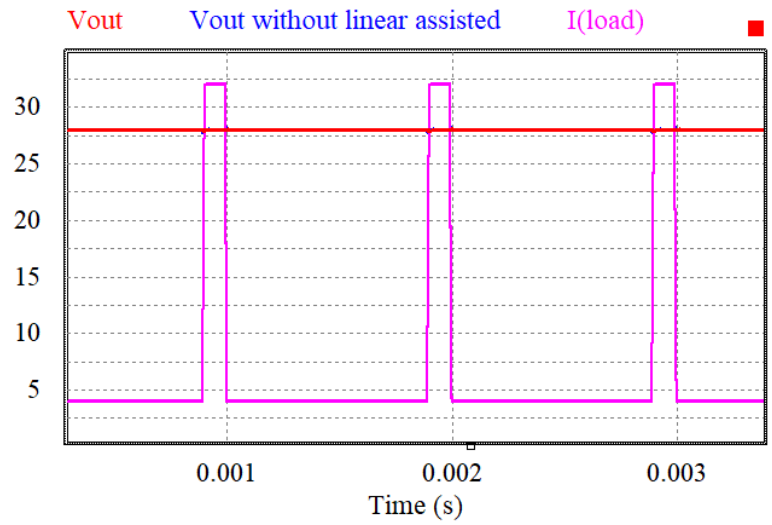
where $R_d=4L_kf_sn_2$, V_{in} is the input DC voltage, R_{load} is equivalent load resistance, L is the transformer leakage inductance referred to primary, f_s is switching frequency and $n_1:n_2$ is transformer turns ratio. From (6.3), it can be concluded that this full bridge

converter is a double-poles-system, which is unstable without frequency compensation. PI control can be adopted to insert one pair of pole and zero to make the system stable. Thus, depending on the PI control configurations, the final transfer function can be defined and the cut-off frequency of high pass filter can be decided.

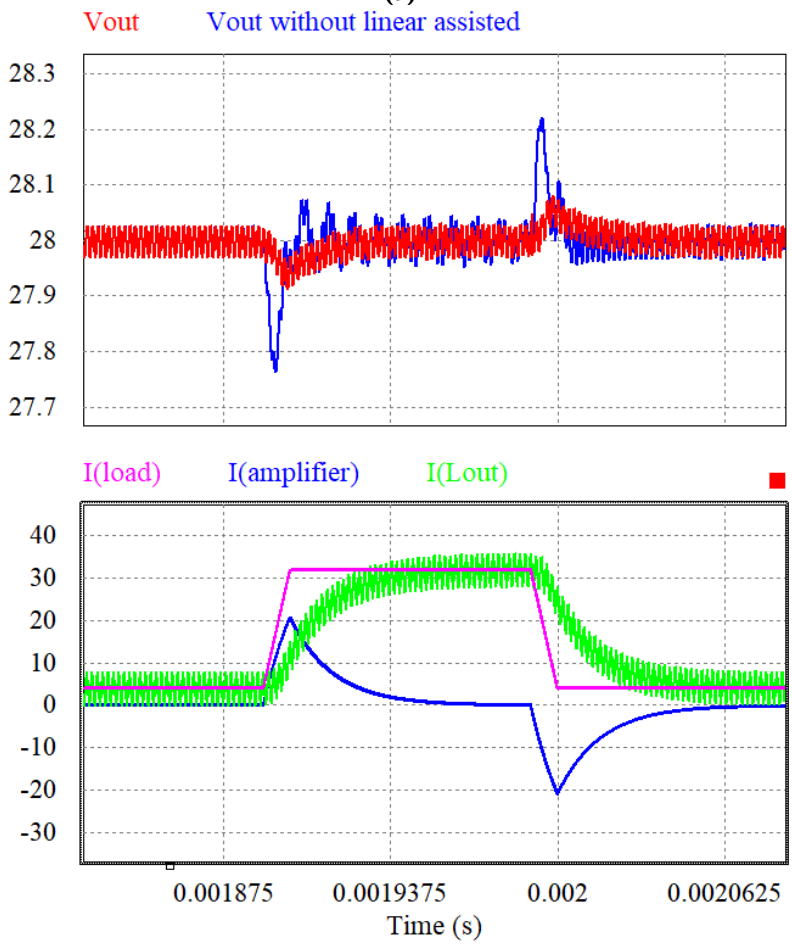
6.4. Simulation results and Data analysis

A 375 V to 28 V 900 W converter with 50 µF output capacitor was designed for a 4 A (average) / 32 A (peak) PA pulsed load and was simulated using PSIM. LTSpice model of GS66516B (650 V GaN E-HEMT) was used in the simulation.

Figure 6-5 shows the current sharing condition in two power paths when pulsed power is supplied, where I(Lout) is the inductor current of full bridge converter in high power path, I(amplifier) is the output current of low power path and I(load) is the pulsed load current. In addition, the proposed topology's output voltage response waveform is also compared with the waveform of same full bridge converter without linear assisted block. From the results, it can be concluded that lower power path responses only for the high frequency part of the load current transient and reduces the V_{out} ripple in comparison with the same full bridge converter without assisted linear amplifier. The peak to peak V_{out} ripple of proposed topology is 163 mV, far less than the 496 mV in same full bridge converter without linear assisted, and is only 0.58% of V_{out}, which proves the effectiveness of the proposed topology.



(a)



(b)

Figure 6-5 (a) Simulated waveforms of multi power pulses; (b) Zoom in figure of single power pulse with current sharing waveforms.

Table 6.1 Simulation Configurations Summary

Parameter name	Value
Input voltage V_{in}	375 V
Output voltage V_{out}	28 V
Inductor L_1 in full bridge converter	4 µH
ESR of Inductor L_1	0.75 mΩ
Capacitor C_1 in full bridge converter	50 µF
ESR of Capacitor C_1	6 mΩ
Inductor L_2 in half bridge converter	1 µH
ESR of Inductor L_2	0.19 mΩ
Capacitor C_2 in half bridge converter	10 µF
ESR of Capacitor C_2	30 mΩ
Number of linear amplifiers connected in one half bridge converter	10
Pulsed load current I_{load}	4A (average) / 32A (peak)
Rise and fall time of I_{load} change	10 us
Switching frequency of full bridge converter fs_1	500 kHz
Switching frequency of half bridge converter fs_2	1 MHz
Cut-off frequency of high pass filter	10 kHz
Turn ratios of transformer in full bridge converter, *np:ns*	6:1
Magnetizing inductance of transformer in full bridge converter	4.2 mH

Table 6.2 Different output capacitor simulation summary

Output capacitor	Capacitor Area	Peak to peak V_{ripple}
50 µF	156.95 mm^2	496 mV
100 µF	313.90 mm^2	361 mV
150 µF	470.85 mm^2	254 mV
200 µF	627.80 mm^2	169 mV

The main simulation configurations are summarized in Table 6.1. The peak to peak voltage ripple simulation results of same full bridge converter without linear assisted with different sizes of output capacitors are summarized in

Table 6.2. A 10 µF 75 V capacitor T521X106M075ATE050, whose size is 7.3mm×4.3mm×4mm (L×W×H) is used to estimate the area needed by output capacitor.

From

Table 6.2, it can be concluded that if only using a same full bridge converter without linear assisted, a 200 µF output capacitor will be used, which will occupy 627.8 mm2 PCB area for every single pulsed PA power supply. In comparison with only 50 µF capacitor needed in the proposed topology, 75% capacitor area can be saved in every single pulsed PA power supply. Capacitor used in half bridge converter is 10 µF (from Table I) and the area of this capacitor is divided by ten because ten linear amplifiers share power from one half bridge converter. So, the area of this capacitor can be ignored in single pulsed power supply.

6.5. Summary

This paper proposed a novel linear assisted DC/DC converter for the application of a single stage higher input voltage, pulsed mode power amplifier to increase response speed and reduce the output capacitors. It includes two power paths, the high power path responsible for voltage control and supplying main power, and the low power path for fast response speed. The current difference between high power path and pulsed load could be compensated to reduce the size of the output capacitor. A 375 V to 28 V 900 W GaN-based converter for a 4 A (average) / 32 A (peak) PA pulsed load was studied,

designed and simulated in this paper to prove the concept. The simulation results show that the maximum voltage ripple decreased over 2/3rd when compared with the same full bridge converter without linear assisted amplifier. With a 50 μF output capacitor, the voltage ripple is only 0.58% of output voltage, which proves this topology's practicality for power supply of PAs in pulsed load application. The capacitor area in this pulsed PA power supply is also analyzed and the result shows proposed topology can dramatically reduce the area occupied by capacitor.

Contribution:

1. A linear assisted DC/DC converter is designed for pulsed load to improve the response speed.
2. A band separation solution is proposed and verified by simulation to deal with the parallel output issue.

Paper publication:

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CHAPTER 7. CONCLUSIONS AND FUTURE WORK

7.1. Conclusions

This dissertation discussed the main issues of the PPS design and proposed several novel solutions for different pulsed power applications to overcome the low power density, low efficiency, and slow response speed issues.

Chapter 2 proposed a GaN-based two-stage power converter with novel control methods for LF pulsed load applications. With average current control, the first stage isolated converter transfers consistent average current to the second stage, which helps in reducing the input filter size to <17% of the one without average current control. A flexible intermediate voltage is applied to reduce the volume of the midpoint energy storage capacitor. Using the proposed digital input feed forward compensator in the second stage fast converter, poor line regulation issue caused by varying midpoint voltage Vmid was avoided. Hence, the V_{mid} range can be as large as possible without affecting Vdroop on the output voltage. A 375 V input 50 V output 800 W (average) / 4 kW (peak) converter prototype was built and tested. The experimental results validated the proposed topology and the control strategy. The converter's power densities are 168.5 W/in^3 and 80 W/in^3, without and with the heatsink, respectively. Table 2.2 summarizes the benefits of the proposed topology over other topologies. The effectiveness of the proposed concepts makes them attractive for pulse load applications requiring fast response and high power density, such as radar systems.

The main issues faced by GaN-based PSFB converters, such as load-dependent ZVS, transformer saturation, and secondary side ringing, were analyzed in detail and

solved in chapter 3. An adaptive burst mode control was proposed to improve the power efficiency at light load. This adaptive burst mode control could achieve both smaller equivalent switching frequency and smaller single switching loss (ZVS for most switching cycles) at the light load condition, which dramatically improved the light load efficiency. A correction factor 'k' was designed in the current loop PI calculation to ensure that the adaptive burst mode smoothly switches the output current between 0 A and minimum ZVS current. A 375 V input 70 V output 800 W prototype was built, and the test results verify the effectiveness of the proposed approach. The efficiency comparison also shows a big improvement from 88% to 92.5% at around 3 A load current. The proposed approach can be very effective in applications such as laboratory power supplies, telecom/server power supplies, etc., which usually face a wide range of load conditions.

Chapter 4 discussed the microcontrollers' hardware limitations on the conventional DPC control techniques. Detailed analysis and comparison between DPC control and DHC control with hardware limitations have been performed. It was found that the digital hysteretic current (DHC) control can overcome this limitation without compromising on the switching frequency. DHC control achieved reduced output voltage ripple and reduced overshoot/undershoot compared to DPC control. The simulation results of a 2.4 kW buck converter with a switching frequency of 1.5 MHz validated the advantages of the DHC control over DPC control technique on GaN FET converters.

Chapter 5 proposed a novel power converter architecture that can be applied in pulsed power NMR applications. By adopting a two-stage topology, this architecture

enforces the isolated converter to only transfer average power, which reduces its power rating and the volume of the transformer and input filter. Furthermore, due to the boost converter in the second stage, the voltage stability requirement of the storage capacitor can be relaxed, so the volume of C_{mid} also decreased significantly. A 150 V DC to 400 V RF, 20 kW peak power converter is designed for a pulsed NMR application. Simulation and scaled-down experimental results and design analysis are described to prove the validity of the proposed topology. The trade-off for this architecture is it needs more switches than the conventional method. However, it can be fixed by adopting GaN devices which have a quite small size and power loss compared with conventional Si based devices. This approach can also be extended to other pulsed load applications such as Magnetic Resonance Imaging (MRI) in healthcare and pulsed radar. This architecture's benefits will be more prominent when the passive components are required in higher voltage rating and higher operating temperature.

Chapter 6 proposed a novel linear assisted DC/DC converter for the application of a single stage higher input voltage, pulsed mode power amplifier to increase response speed and reduce the output capacitors. It includes two power paths, the high power path responsible for voltage control and supplying main power, and the low power path for fast response speed. The current difference between the high power path and pulsed load could be compensated to reduce the size of the output capacitor. A 375 V to 28 V 900 W GaN-based converter for a 4 A (average) / 32 A (peak) PA pulsed load was studied, designed, and simulated in this paper to prove the concept. The simulation results show that the maximum voltage ripple decreased over 2/3rd when compared with the same full bridge converter without a linear assisted amplifier. With a 50 µF output capacitor,

the voltage ripple is only 0.58% of output voltage, which proves this topology's practicality for power supply of PAs in pulsed load application. The output capacitor area in this pulsed PA power supply is also analyzed and the result shows proposed topology can dramatically reduce the area occupied by the output capacitors.

7.2. Future work

The work presented in this dissertation can be extended in various possible ways. A few are listed below:

1) Two stage structure's benefits have been proved in chapter 2 and chapter 5. Therefore, for other applications (e.g. narrow input voltage range), the first stage can be redesigned with LLC resonant or switch capacitor for even better efficiency and power density.
2) The adaptive burst mode proposed in chapter 3 can also be utilized in other switching power converters that have output current feedback to achieve better light load efficiency and reduced current rating.
3) The linear assisted methods proposed in chapter 6 can also be combined with the two stage structure proposed in chapter 2 and chapter 5 so that the response speed can furtherly increase without much power loss increases.

REFERENCES

[1] X. Huang, X. Ruan, F. Du, F. Liu and L. Zhang, "A Pulsed Power Supply Adopting Active Capacitor Converter for Low-Voltage and Low-Frequency Pulsed Loads," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9219-9230, Nov. 2018.

[2] F. J. C. M. Beckers, W. F. L. M. Hoeben, T. Huiskamp, A. J. M. Pemen and E. J. M. van Heesch, "Pulsed Corona Demonstrator for Semi-Industrial Scale Air Purification," *IEEE Transactions on Plasma Science*, vol. 41, no. 10, pp. 2920-2925, Oct. 2013.

[3] A. K. Jain, D. McIntosh, M. Jones and B. Ratliff, "A 2.5kV to 22V, 1kW Radar Decoy Power Supply Using Silicon Carbide Semiconductor Devices," *2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-10.

[4] Y. Gu, D. Zhang, M. Fang, X. Zhang and P. Qi, "Research on Low Input Current Ripple Two-Stage Converter for Low Frequency Pulsed-Power Applications," *IET Transactions on Power Electronics*, vol. 13, no. 2, pp. 340-345, February 2020.

[5] K. H. Kim, Y. R. Lee, J. H. Joo and D. M. Park, "2.7 - 3.1 GHz, 1.5 kW Pulsed Solid-State Power Amplifier with Automatic Gain Equalization Circuit for Radar Application," *2007 IEEE Radar Conference*, 2007, pp. 1044-1048, doi: 10.1109/RADAR.2007.374404.

[6] A. Mediavilla, A. Tobia and P. Colantonio, "1 Kw Compact L-Band Pulsed Power Amplifier for Radar Applications," *2011 Microwaves, Radar and Remote Sensing Symposium*, 2011, pp. 43-46, doi: 10.1109/MRRS.2011.6053597.

[7] Y. Fang, J. Chang, L. Leverich, P. Tom and C. Leader, "An 800-Watts Power Solution Module for L-band Pulsed Radar Applications," *2007 Asia-Pacific Microwave Conference*, 2007, pp. 1-4, doi: 10.1109/APMC.2007.4554691.

[8] A. K. Paul, A. V. Giridhar, K. K. Rai and A. Kirubakaran, "Generation of Pulsed Power for Radar Application," *2021 1st International Conference on Power Electronics and Energy (ICPEE)*, 2021, pp. 1-6, doi: 10.1109/ICPEE50452.2021.9358689.

[9] I. J. Lowe and C. E. Tarr, "A High-Power, Untuned Radio-Frequency Transmitter for Pulsed Nuclear Magnetic Resonance Spectroscopy" *Journal of Physics E: Scientific Instruments*, vol.1, no. 6, pp. 604-606, June 1968.

[10] Y. Zhang, P. Xia and Y. Yu, "Review of Nuclear Magnetic Resonance Magnet for Oil Well Logging," *IEEE Transactions on Applied Superconductivity*, vol. 10, no. 1, pp. 763-766, March 2000.

[11] C. E. Yarman, L. Monzón, M. Reynolds and N. Heaton, "A New Inversion Method for NMR Signal Processing," *2013 5th IEEE International Workshop on Computational Advances in Multi-Sensor Adaptive Processing (CAMSAP)*, St. Martin, 2013, pp. 260-263.

[12] J. Zhen, G. Gouws, R. Dykstra and C. Eccles, "Class D RF Amplifier for 20 Mhz NMR MOUSE Sensor," *2012 Sixth International Conference on Sensing Technology (ICST)*, Kolkata, 2012, pp. 13-16.

[13] J. Zhen, R. Dykstra, C. Eccles, G. Gouws, S. Obruchkov. "A Compact Class D RF Power Amplifier for Mobile Nuclear Magnetic Resonance Systems," *Review of Scientific Instruments*, Jul 2017.

[14] B. Li, W. Xu, H. Zhang, C. Zhao and L. Hanzo, "PAPR Reduction for Hybrid ACO-OFDM Aided IM/DD Optical Wireless Vehicular Communications," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 10, pp. 9561-9566, Oct. 2017, doi: 10.1109/TVT.2017.2698265.

[15] B. Adebisi, K. Anoh and K. M. Rabie, "Enhanced Nonlinear Companding Scheme for Reducing PAPR of OFDM Systems," *IEEE Systems Journal*, vol. 13, no. 1, pp. 65-75, March 2019, doi: 10.1109/JSYST.2018.2851847.

[16] M. C. Leifer and R. L. Haupt, "Power Amplifier and Power Supply Distortion of Pulse Compression Radar Chirps," *2016 IEEE Radar Conference (RadarConf)*, 2016, pp. 1-4.

[17] Advanced Test Equipment Corporation, "Conducted Emissions, Audio Frequency Currents and Radio Frequency Potentials," Available: https://www.atecorp.com/compliance-standards/mil/ce101ce102#:~:text=For%-20AC%20applications%2C%20MIL%2DSTD,power%20input%20leads%20including%20returns (Accessed Nov. 17, 2021)

[18] W. Xu, P. Upadhyaya, X. Wang, R. Tsang and L. Lin, "A 1A LDO Regulator Driven by a 0.0013mm^2 Class-D Controller," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 104-105, doi: 10.1109/ISSCC.2017.7870282.

[19] J. Yin, S. Huang, Q. Duan and Y. Cheng, "An 800 mA Load Current LDO with Wide Input Voltage Range," *2017 International Conference on Circuits, Devices and Systems (*ICCDS*)*, 2017, pp. 174-178, doi: 10.1109/ICCDS.2017.8120473.

[20] A. K. Jain, D. McIntosh, M. Jones, and B. Ratliff, “A 2.5 kV to 22 V, 1 kw Radar Decoy Power Supply Using Silicon Carbide Semiconductor Devices,” *Proc. Eur. Conf. Power Electron*. Appl., 2011, pp. 1−10.

[21] Y. Gu, D. Zhang, M. Fang, X. Zhang and P. Qi, “Research on Low Input Current Ripple Two-Stage Converter for Low Frequency Pulsed-Power Applications,” *IET Transactions on Power Electronics*, vol. 13, no. 2, pp. 340-345, February 2020.

[22] Y. Yao, H. S. Krishnamoorthy and S. Yerra, "Linear Assisted DC/DC Converter for Pulsed Mode Power Applications," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, Cochin, India, 2020, pp. 1-5

[23] P. F. Miaja, M. Rodriguez, A. Rodriguez and J. Sebastian, "A Linear Assisted DC/DC Converter for Envelope Tracking and Envelope Elimination and Restoration Applications," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3302-3309, July 2012

[24] Z. Yuan and H. Xu, "Pulse Power Supply with Faster Response and Low Ripple Current Using Inductive Storage and Interleaving Technology," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 1, pp. 54-62, March 2020

[25] D. Kim, J. Baek, J. Lee, J. Shin and J. -W. Shin, "Implementation of Soft-Switching Auxiliary Current Control for Faster Load Transient Response," *IEEE Access*, vol. 9, pp. 7092-7106, 2021.

[26] X. Huang, X. Ruan, F. Du, F. Liu, and L. Zhang, “High Power and Low Voltage Power Supply for Low Frequency Pulsed Load,” *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2859–2865

[27] Z. Yuan and H. Xu, "Pulse Power Supply with Faster Response and Low Ripple Current Using Inductive Storage and Interleaving Technology," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 1, pp. 54-62, March 2020

[28] J. Azurza Anderson, G. Zulauf, J. W. Kolar and G. Deboy, "New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322-338, 2020, doi: 10.1109/OJPEL.2020.3018220.

[29] T. P. Chow, I. Omura, M. Higashiwaki, H. Kawarada, and V. Pala, “Smart Power Devices and ICs Using Gaas and Wide and Extreme Bandgap Semiconductors,” *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 856–873, Mar. 2017.

[30] W. Saito, I. Omura, T. Ogura, and H. Ohashi, “Theoretical Limit Estimation of Lateral Wide Band-Gap Semiconductor Power-Switching Device,” *Solid-State Electronics*, vol. 48, no. 9, pp. 1555–1562, Sep. 2004.

[31] B. J. Baliga, Gallium Nitride and Silicon Carbide Power Devices. World Scientific Publication Company, 2016.

[32] Y. Gunaydin, "Impact of Temperature and Switching Rate on Forward and Reverse Conduction of GaN and SiC Cascode devices: A Technology Evaluation," *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*, 2020, pp. 782-787, doi: 10.1049/icp.2021.1067.

[33] Richards on RFPD Company, “Gallium Nitride (GaN) versus Silicon Carbide (SiC) In The High Frequency (RF) and Power Switching Applications,” Available: https://www.richardsonrfpd.com/docs/rfpd/Microsemi-A-Comparison-of-Gallium-Nitride-Versus-Silicon-Carbide.pdf\ (Accessed Nov. 20, 2021)

[34] T. Dickenson, “Raytheon: AMDR”, Available [21 February 2021]: https://flytoazuresky.tistory.com/attachment/cfile25.uf@221CE03A578233D01CBCA3.pdf (Accessed Nov. 20, 2021)

[35] M. C. Leifer and R. L. Haupt, "Power Amplifier and Power Supply Distortion of Pulse Compression Radar Chirps," *2016 IEEE Radar Conference (RadarConf)*, 2016, pp. 1-4.

[36] S. Cetin and A. Astepe, "A Phase Shifted Full Bridge Converter Design for Electrical Vehicle Battery Charge Applications Based on Wide Output Voltage Range," *2016 International Conference on Applied Electronics (AE)*, Pilsen, 2016, pp. 51-56.

[37] Rise time [Online]. Available: https://en.wikipedia.org/wiki/Rise_time#cite_ref-Orwp30_17-0 (2021, September 6).

[38] B. Yuan, M. -X. Liu, W. T. Ng and X. -Q. Lai, "Hybrid Buck Converter With Constant Mode Changing Point and Smooth Mode Transition for High-Frequency Applications," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 2, pp. 1466-1474, Feb. 2020.

[39] S. Yerra, H. Krishnamoorthy and Y. Yao, "Single Stage Three-Level Interleaved Buck Converter with Current Self-Balancing for Improved Point-of-Load

Performance," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, 2020, pp. 1-6.

[40] S. Pan and P. K. T. Mok, "A 10-MHz Hysteretic-Controlled Buck Converter with Single On/Off Reference Tracking Using Turning-Point Prediction for DVFS Application," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 11, pp. 4502-4515, Nov. 2019.

[41] Y. Yao, K. Gnana Sambandam and H. S. Krishnamoorthy, "Comparative Study on Practical Implications of Digital Peak Current and Hysteresis Current Controllers for MHz Frequency DC-DC Converters," *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2020, pp. 1-5.

[42] D. Doliya, "Feedback and Feedforward Control of Buck Converter with Parasitics," *2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, 2017, pp. 471-475.

[43] X. Gao, H. Wu, S. Gao, Z. Zhang and Y. Xing, "A Two-Stage Pulsed Power Supply for Low-DC-Voltage and Low-Frequency Pulsed-Current Loads," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2298-2309, Feb. 2021.

[44] D. Chowdhury, A. S. Md. Khalid Hasan and M. Z. Rahman Khan, "Scalable DC Microgrid Architecture with Phase Shifted Full Bridge Converter Based Power Management Unit," *2018 10th International Conference on Electrical and Computer Engineering (ICECE)*, 2018, pp. 22-25.

[45] H. Wang, M. Shang and A. Khaligh, "A PSFB-Based Integrated PEV Onboard Charger with Extended ZVS Range and Zero Duty Cycle Loss," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 585-595, Jan.-Feb. 2017.

[46] I. Lee, "Hybrid DC–DC Converter with Phase-Shift or Frequency Modulation for NEV Battery Charger," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 884-893, Feb. 2016.

[47] J. Kim, D. Kim, C. Kim and G. Moon, "A Simple Switching Control Technique for Improving Light Load Efficiency in a Phase-Shifted Full-Bridge Converter with a Server Power System," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1562-1566, April 2014.

[48] Y. Yao, H. S. Krishnamoorthy and S. Yerra, "Linear Assisted DC/DC Converter for Pulsed Mode Power Applications," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, 2020, pp. 1-5.

[49] X. Li, Y. Zhang, P. Fang and J. Liu, "Comprehensive Comparison of Three Typical Bridge Structure Isolated Soft Switching DC-DC Topologies in the Application of Locomotive Traction," *2019 IEEE International Conference on Industrial Technology (ICIT)*, 2019, pp. 1533-1540.

[50] A. M. Naradhipa, S. Kim, D. Yang, S. Choi, I. Yeo and Y. Lee, "Power Density Optimization of 700 kHz GaN-Based Auxiliary Power Module for Electric Vehicles," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5610-5621, May 2021.

[51] F. Hoffmann, P. K. Prasobhu, M. Liserre and G. Buticchi, "Overcoming Design Challenges in Low Voltage Gan Based PSFB Battery Charger," *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 1388-1393.

[52] Y. Cui, W. Zhang, L. M. Tolbert, F. Wang and B. J. Blalock, "Direct 400 V to 1 V Converter for Data Center Power Supplies Using Gan FETs," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 3460-3464.

[53] T. A. Pereira, "Optimal Design of Planar Transformer for GaN based Phase-Shifted Full Bridge Converter," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 2241-2248.

[54] P. K. Jain, W. Kang, H. Soin, and Y. Xi, “Analysis and Design Considerations of A Load and Line Independent Zero Voltage Switching Full Bridge DC/DC Converter Topology,” *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 649–657, Sep. 2002.

[55] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn and J. Rivas-Davila, "C_{OSS} Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10748-10763, Dec. 2018.

[56] L. Zhao, H. Li, X. Wu, and J. Zhang, “An Improved Phase-Shifted Full Bridge Converter with Wide-Range ZVS and Reduced Filter Requirement,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2167–2176, Mar. 2018.

[57] L. Zhao, H. Li, C. Xu, and X. Zheng, “Efficiency Improvement of an Adaptive-Energy-Storage Full-Bridge Converter By Modifying Turns Ratio of A Coupled Inductor,” *IEEE Trans. Power Electron*., vol. 33, no. 2, pp. 948–956, Feb. 2018.

[58] M. Borage, S. Tiwari, and S. Kotaiah, “A Passive Auxiliary Circuit Achieves Zero-Voltage-Switching in Full-Bridge Converter Over Entire Conversion Range,” *IEEE Power Electron Lett.*, vol. 3, no. 4, pp. 141–143, Dec. 2005.

[59] P. Das, M. Pahlevaninezhad, and A. K. Singh, “A Novel Load Adaptive ZVS Auxiliary Circuit for PWM Three-Level DC–DC Converters,” *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2108–2126, Apr. 2015.

[60] Z. Chen, S. Liu, and L. Shi, “Improved Zero-Voltage-Switching Pulse Width Modulation Full Bridge Converter with Self-Regulating Auxiliary Current,” *IET Power Electron.*, vol. 6, no. 2, pp. 287–296, Feb. 2013.

[61] J. Zhu, Q. Qian, S. Lu, W. Sun, and H. Tian, “A Phase-Shift Triple Full Bridge Converter with Three Shared Leading Legs,” *IEEE Journal Emerging Selected Topics Power Electron.*, vol. 6, no. 4, pp. 1912–1920, Dec. 2018.

[62] H. Wu, P. Xu, Y. Xing, L. Chen, and X. Xiao, “Two-Transformer-Based Full-Bridge Soft-Switching DC–DC Converter with Improved Characteristics,” *IET Power Electron.*, vol. 8, no. 12, pp. 2537–2545, Dec. 2015.

[63] H. Wu, L. Chen, and Y. Xing, “Secondary-Side Phase-Shift-Controlled Dual-Transformer-Based Asymmetrical Dual-Bridge Converter with Wide Voltage Gain,” *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5381–5392, Oct. 2015.

[64] K. Shi, D. Zhang, and Y. Gu, “Interleaved Current-Driven Phase-Shift Full-Bridge Converter with Magnetic Integration and Voltage Doubler Rectifiers,” *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8308–8321, Oct. 2018.

[65] Z. Guo, D. Sha, X. Liao, and J. Luo, “Input-Series-Output-Parallel Phase Shift Full-Bridge Derived DC–DC Converters with Auxiliary LC Networks to Achieve Wide Zero-Voltage Switching Range,” *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5081–5086, Oct. 2014.

[66] C. -E. Kim, "Optimal Dead-Time Control Scheme for Extended ZVS Range and Burst-Mode Operation of Phase-Shift Full-Bridge (PSFB) Converter at Very Light Load," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10823-10832, Nov. 2019.

[67] L. Sun, X. Zhang, B. Liu, S. Wang, Y. Wang and D. Xu, "Efficiency Optimization of Phase-Shift Full-Bridge through Adaptive Dead-Time and Burst-Mode at Very Light Load," *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, 2019, pp. 1-5.

[68] Datasheet, “GS66502B Bottom-side cooled 650 V E-mode GaN transistor Datasheet,” GaN System. [Online]. Available: https://gansystems.com/wp-content/uploads/2020/04/GS66502B-DS-Rev-200402.pdf

[69] Song-Yi Lin and Chern-Lin Chen, "Analysis and Design for RCD Clamped Snubber Used in Output Rectifier Of Phase-Shift Full-Bridge ZVS Converters," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 2, pp. 358-359, April 1998.

[70] Y. Lee, J. Lee and J. Kim, "GaN FET-based Synchronous Buck Converter with 10-Bit 4-Mhz Digital Pulse Width Modulator," *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Seoul, 2015, pp. 1762-1767

[71] G. Zhou and J. Xu, "Digital Peak Current Control for Switching DC–DC Converters With Asymmetrical Dual-Edge Modulation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 11, pp. 815-819, Nov. 2009

[72] G. Zhou, J. Xu, J. Wang and Y. Jin, "Comparison Study on Digital Peak Current, Digital Peak Voltage, and Digital Peak Voltage/Peak Current Controlled Buck Converter," *2009 4th IEEE Conference on Industrial Electronics and Applications*, Xi'an, 2009, pp. 799-804

[73] M. Hallworth and S. A. Shirsavar, "Microcontroller-Based Peak Current Mode Control Using Digital Slope Compensation," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3340-3351, July 2012

[74] A. Ugur and M. Yilmaz, "Digital Hybrid Current Mode Control for DC–DC Converters," *IET Power Electronics*, vol. 12, no. 4, pp. 891-898, 10 4 2019

[75] Microchip, "dsPIC33CK256MP508 FAMILY," 2019, [online] Available at: http://ww1.microchip.com/downloads/en/DeviceDoc/dsPIC33CK256MP508-Family-Data-Sheet-DS70005349G.pdf

[76] Texas Instruments, "TMS320F2837xS Microcontrollers," 2020, [online] Available at: https://www.ti.com/lit/ds/symlink/tms320f28375s.pdf?ts=15930-52429066&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTMS320F28375S

[77] Yiming Zhang, Pingchou Xia and Yunjia Yu, "Review of Nuclear Magnetic Resonance Magnet for Oil Well Logging," *IEEE Transactions on Applied Superconductivity*, vol. 10, no. 1, pp. 763-766, March 2000.

[78] C. E. Yarman, L. Monzón, M. Reynolds and N. Heaton, "A New Inversion Method for NMR Signal Processing," *2013 5th IEEE International Workshop on Computational Advances in Multi-Sensor Adaptive Processing (CAMSAP)*, St. Martin, 2013, pp. 260-263.

[79] J. Zhen, G. Gouws, R. Dykstra and C. Eccles, "Class D RF Amplifier for 20 MHz NMR MOUSE Sensor," *2012 Sixth International Conference on Sensing Technology (ICST)*, Kolkata, 2012, pp. 13-16.

[80] J. Zhen, R. Dykstra, C. Eccles, G. Gouws, S. Obruchkov. "A Compact Class D RF Power Amplifier for Mobile Nuclear Magnetic Resonance Systems," in *Review of Scientific Instruments*, Jul 2017.

[81] A. TYSHKO, "Enhanced Transmitter and Method for A Nuclear Magnetic Resonance Logging Tool," United State Patent US 9.405,035 B2, Aug. 2, 2016.

[82] AVX Corporation, " X7RDielectric General Specifications, " 06035C103KAT2A-AVX-datasheet. https://datasheet.octopart.com/06035C103KAT2A-AVX-datasheet-148183.pdf (Accessed Aug. 11, 2020).

[83] W. D. Braun, L. Gu, G. Scott and J. Rivas-Davila, "MRI Compatible DC Modulator for an Envelope Tracking Transmitter," *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, ON, Canada, 2019, pp. 1-4.

[84] J. Sabate, L. J. Garces, P. M. Szczesny, Qiming Li and W. F. Wirth, "High-Power High-Fidelity Switching Amplifier Driving Gradient Coils for MRI Systems," *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, Aachen, Germany, 2004, pp. 261-266 Vol.1

[85] Y. Gu, D. Zhang, M. Fang, X. Zhang and P. Qi, "Research on Low Input Current Ripple Two-Stage Converter for Low Frequency Pulsed-Power Applications," *IET Transactions on Power Electronics*, vol. 13, no. 2, pp. 340-345, February 2020.

[86] X. Huang, X. Ruan, F. Du, F. Liu and L. Zhang, "A Pulsed Power Supply Adopting Active Capacitor Converter for Low-Voltage and Low-Frequency Pulsed Loads," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9219-9230, Nov. 2018.

[87] J. Suh, J. Seok and B. Kong, "A Fast Response PWM Buck Converter with Active Ramp Tracking Control in a Load Transient Period," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 3, pp. 467-471, March 2019.

[88] A. P. Ambade, "Direct Power Control PWM Rectifier Using Switching Table for Series Resonant Converter Capacitor Charging Pulsed Power Supply," *2016 IEEE International Conference on Recent Trends in Electronics*, Information & Communication Technology (RTEICT), Bangalore, 2016, pp. 758-762.

[89] M. Vasic, O. Garcia, J. A. Oliver, P. Alou, D. Diaz, and J. A. Cobos, "Multi Level Power Supply for High Efficiency RF Amplifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 1078–1089, Apr. 2010.

[90] X. Xiong, Ruan, H. Xi, and J. Ge, “Feed-Forwarding the Output Voltage to Improve Efficiency for Envelope-Tracking Power Supply Based on a Switch-Linear Hybrid Scheme,” *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2106–2111, Aug. 2011.

[91] Ming-Tsun Tsai, Ching-Lung Chu, Char-Yong Siow and Syuan-Neng Jhao, "Design a Wide Output Range Power Supplies with Assisted Linear Amplifier," *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, 2017, pp. 1297-1301.

[92] J. Kim, S. Choi, I. Kim and W. Moon, "Design of Compact and High-Efficiency Power Supply and Power Amplifier for Parametric Array Transducer," *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Taipei, 2015, pp. 1-5.

[93] D. Li, Y. Zhang, M. Rodr´iguez and D. Maksimovic´, "Band Separation in Linear-Assisted Switching Power Amplifiers for Accurate Wide-Bandwidth Envelope Tracking," *2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh*, PA, 2014, pp. 1113-1118.

[94] P. F. Miaja, M. Rodriguez, A. Rodriguez and J. Sebastian, "A Linear Assisted DC/DC Converter for Envelope Tracking and Envelope Elimination and Restoration Applications," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3302-3309, July 2012.

[95] C. Andersson, “Design of a 2.5kW DC/DC Full bridg Converter,” M.S. thesis, Energy and Environment Dept., Chalmers Univ. of Technology, Göteborg,

Sweden, 2011. [Online]. Available: http://publications.lib.chalmers.se/records-/fulltext/173958/173958.pdf

[96] N. George, V. N. Panchalai and E. Sebastian, "Digital Feedback Control of a Full-Bridge DC-DC Converter with Input Voltage Based Gain Scheduling," *2014 Fourth International Conference on Advances in Computing and Communications*, Cochin, 2014, pp. 347-351.