# Power and Energy Management of Battery Energy Storage Systems for Grid Integration

by

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# ABSTRACT

Battery energy storage system (BESS) plays a critical role in grid applications, where it can perform services such as mitigation of the intermittency of renewable energy, grid frequency regulation, peak shaving, and grid voltage support/var compensation. To interface the BESS to the grid, Modular Multilevel Converters (MMC) are being widely considered, particularly for medium and high voltage applications. This dissertation develops power strategies and energy requirements for a BESS-MMC. The work starts from developing battery models for grid applications to system-level operation, including BESS and the electric grid.

A novel methodology to estimate the parameters of the equivalent circuit model (ECM) for lithium-ion battery cells focusing on their use in grid applications is developed. Parameter dependencies on the state of charge (SoC) and temperature are included in the proposed methodology and correlated through polynomial regression. Accelerated degradation tests are performed to obtain the parameter variation as the battery ages. The obtained information is helpful to design components in the BESS-MMC, controller parameters, SoC, and State of Health (SoH) estimation.

The dissertation also investigates the precise capacitor energy requirements for various operations of BESS-MMC, which include arm/phase power transfer. Further, the relation between the controller design and the submodule's capacitor sizing in terms of its energy requirements is also explored. Design guidelines for the module level voltage control to attenuate battery ripple and a detailed analysis of the capacitor energy requirement in each operating mode are presented.

Aiming to improve the BESS-MMC resiliency by maintaining it connected to the electrical grid, faulty scenarios involving asymmetric grid voltage conditions and an asymmetric power available in each phase and arm are considered. Several power and SoC balancing techniques with defined active power limits to avoid battery overuse are proposed and verified through C-HIL results.

The use of BESS-MMC as an interlinking converter (IC) between AC and DC microgrids in a hybrid microgrid environment is explored. This avoids the connection of battery modules into either DC or AC microgrid and provides complete decoupled operation between grids. Control strategies, as well as possible power management strategies, are proposed and verified through C-HIL results.

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# 1. INTRODUCTION

## 1.1 Background and motivation

Greenhouse gas emissions have been steadily increasing since the beginning of the 20th Century. In the United States, carbon dioxide ($CO_2$) generated by the use of fossil fuels are responsible for 80% of the total amount of greenhouse gas emissions, nearing 5.2 billion metric tons in 2020 [1]. Furthermore, the burning of oil, natural gas, and coal for the electricity and heat sector account for 25% of the global emissions [1]. In 2020, 4 trillion kWh of electricity was generated in generation facilities across the United States [2]. This number did not significantly change in 2021 when 4.12 trillion kWh was generated [3]. According to the U.S. Energy Information Administration (EIA), in 2021, 60.8% of the generation came from fossil fuels, 18.9% from nuclear, and 20.1% from renewable energy sources (RES) [3]. Based on this data, it can be stated that fossil fuel plays a major role in generating electricity. However, fossil fuels not only have effects on climate change but can also lead to air pollution and ocean acidification [4], [5]. Therefore, an eventual shift to more usage of RES can be beneficial in the short and long term.

Wind power generation (380 billion kWh), hydropower (260 billion kWh), and solar (115 billion kWh) were the leading RES in the electricity generation sector in 2021 [3]. Furthermore, small-scale solar photovoltaic systems (not connected to a power plant, e.g., rooftop) account for 49 billion kWh. Given RES incentives and decreased technology costs, by 2050, renewables are expected to supply 44% of U.S. electricity [6].

One of the major disadvantages of solar and wind power generation is its intermittency [7]. The electrical grid operates based on supply and demand, which means that generation and electrical loads must be met at all times to ensure system-wide stable operation and avoid blackouts [8]. Since the output power of RES cannot be perfectly predicted, especially in longer time horizons, the integration of RES can be considered challenging for grid operators' planning [9]. Similarly, predicting the total demand in residential areas can also be challenging, especially with the increased popularity of electric vehicles (EV) [10].

Storing energy during periods of elevated production and lower demand is a possible solution to balance the power fluctuations. The most common types of Energy Storage Systems (ESSs) are pumped hydroelectric, compressed air, flywheels, batteries energy storage system (BESS), and thermal storage [11], [12]. Pumped hydroelectric is, by a large margin, the most significant contributor to ESSs capacity, with 94% out of the total 25.2 GW available in the United States. The other 6% is split mainly between thermal storage (669 MW) and BESS (733 MW) [11]. The main difference between pumped hydroelectric and BESS in terms of their usage to solve the power fluctuation problem relates to their time scale use. BESS is primarily used in short to medium-term storage, commonly defined in seconds to hours. On the other hand, pumped hydro can be used for long-term energy storage, lasting from hours to weeks [13], [14].

Although pumped hydro have higher power and energy density, it has a very slow response time (on a scale of minutes [15]), and cannot be localized due to the site requirements. On the other hand, BESS can have response times in fractions of seconds, which makes it a good solution for short-term reliability services, such as the operating

reserves primary frequency response (seconds) and regulation (minutes to an hour) [16], [17]. In addition to operating reserves, applications of BESS in utility-scale grids are arbitrage (purchase off-peak energy and sell it during high prices), firm capacity (reliable power capacity supply), and blackstart (start-up system after failure) [16].

According to the International Energy Agency (IEA) and highlighted in Figure 1.1, globally, the BESS capacity reached 17 GW in 2020 [17], with China, Europe, and the United States leading the way. Seven gigawatts are classified as behind-the-meter (BTM), that is, BESS that is connected to the distribution system on the customer's side of the utility's service meter (e.g., rooftop solar PV with battery energy storage for later use). According to the Net Zero Emissions 2050 Scenario, the projected BESS capacity installed by 2030 should increase 35-fold to 600 GW [17].

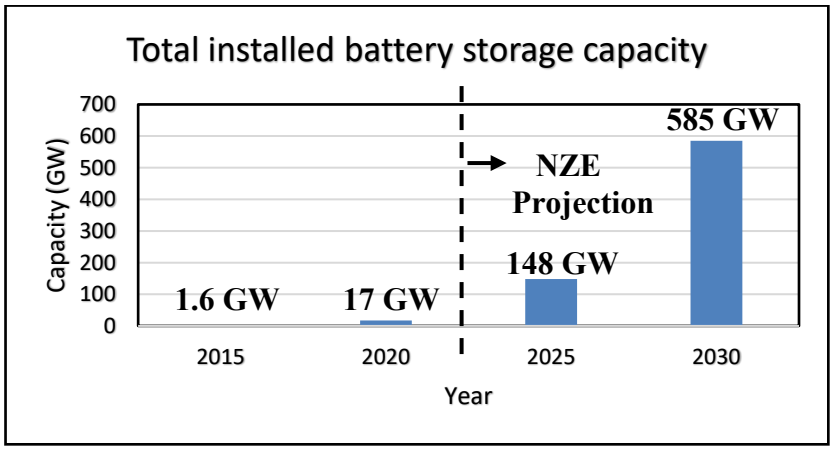



Figure 1.1. BESS capacity projected increase (2015-2030).

The following subsections review the technologies involved in BESS for utility grid applications, covering both battery chemistries and the power electronics involved. Each subsection also highlights the technologies used in this dissertation. Finally, the last two subsections discuss the research contributions of the dissertation, together with the dissertation outline.

## 1.2 Review of Battery Energy Storage Systems for Grid Applications

### 1.2.1 Battery Chemistry for Grid Applications

Lithium-ion (Li-ion) batteries are the most commonly used type of batteries in grid applications in terms of total installed power capacity. Li-ion batteries accounted for about 81% of all electrochemical storage in 2017 [18]. Compared to other common battery technologies (such as Lead Acid), Li-ion batteries have greater overall performance, providing higher power and energy density, efficiency, and relatively high lifetime [19].

Another contributing factor to the popularity of lithium-ion batteries is their decreasing costs. According to economic reports, the average price of lithium-ion batteries has fallen by 89% since 2010, from $1100/kWh to $137/kWh [20]. Nevertheless, as of 2021, the volatile price of the metals utilized in the batteries' cathodes can threaten this continuous decline [21].

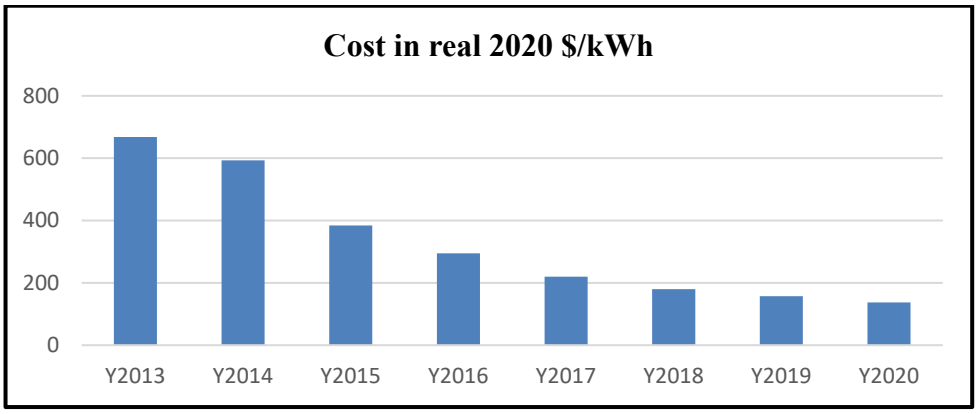



Figure 1.2. Lithium-ion battery cost trend.

Several subcategories exist within Lithium-ion batteries. These subcategories mainly difference concerns the material used in the cathode manufacturing process. Currently, many Lithium-ion batteries technologies are available: Lithium Iron Phosphate (LFP/LiFePO4), Lithium Nickel, Manganese Cobalt (NMC), Lithium Nickel

Cobalt Aluminum (NCA), Lithium Cobalt Oxide-based (LiCoO2), Lithium Manganese Oxide-based (LiMn2O4), among many others [19]. According to [22], Lithium Iron Phosphate (LFP/LiFePO4) and Nickel Manganese Cobalt (NMC) are the current mainstream options for storage applications and, together, are expected to make up 90% of the storage market.

Typical parameters to assess battery performance are efficiency, power density, lifetime, cost, and energy density. According to [19], [23], [24], NMC batteries have greater power and energy density and higher efficiency when compared to LiFePO4 batteries. However, in terms of battery cycles, LiFePO4 batteries can have up to four times greater lifetime when compared to NMC. Additionally, while [19] reports similar costs for LFP and NMC batteries at around $300/kWh, market reports suggest that LFP batteries are about 20-30% cheaper [25], [26], with the lowest price confirmed to be around $80/kWh [20].

According to [27], between 2018 and 2020, NMC and LiFePO4 batteries account for 60% and 11% of the safety incidents in electric vehicle applications. One reason that can potentially justify the differences between NMC and LiFePO4 batteries accidents is the thermal stability of the materials used in each technology. Battery tests performed in [28] and [29] have concluded that the thermal stability of LiFePO4 is much higher than that of NMC, which implies that LiFePO4 batteries ignite at much higher temperatures. Given all the aforementioned characteristics of LiFePO4 batteries, many researchers and engineers consider that this technology will continue to be the mainstream option during the next decade [27]. Consequently, this dissertation focuses on LiFePO4 batteries for all the battery-related tests and considerations.

Environmental concerns also arise while disposing of lithium-ion batteries. Lithium-ion batteries should be recycled at a dedicated battery recycler: a facility that receives batteries and separates components for reuse [30]. In [31], it is stated that only 6% of lithium-ion battery cells are being recycled, with the main focus on recovering copper, aluminum, and cathode materials. Improvements in the recycling process are required. However, it can be more challenging when manufacturers do not fully disclaim the materials within the batteries [32]. Finally, an intermediate step before recycling batteries would be repurposing them for different applications. A repurposing possibility that has been gaining attention is the use of degraded vehicle lithium-ion batteries in grid applications [33]-[35], which can delay the disposal of batteries while also providing economic benefits.

### 1.2.2 Power converters

Power Electronic Converters (PECs) are the technology employed to interface BESS to the electric grid [36]-[40]. Due to the decreasing cost of battery cells, the cost of PECs is expected to become more relevant to the system's overall cost. According to [41], PECs already account for 28 to 35% of the cost of lithium-ion based BESS, thus rivaling the cost of cells, which can vary from 35 to 46%. Given this economic scenario, there is a continuous push for increasing the efficiency and reliability of PECs.

The connection of batteries to the electric grid can occur at both low voltage (LV) and medium voltage (MV). LV networks have voltage levels defined as less than 1 kV, while MV levels are considered from 1 kV to 69 kV. In the literature, commonly considered MV are 3.3 kV, 11 kV, 13.8 kV and 33 kV [37]-[39]. Since the battery is a DC voltage source, a DC to AC voltage conversion stage is required for meeting the AC

utility grid voltage and frequency requirements. One of the most popular PEC topologies utilized to interface BESS and the utility grid is the 2-Level Voltage Source Converter (2L-VSC), shown in Figure 1.3.

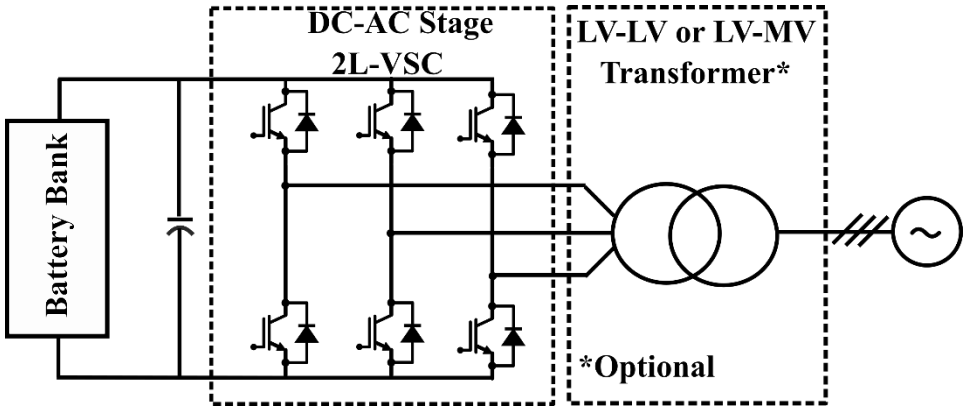



Figure 1.3. BESS integration to electrical grid through 2L-VSC DC-AC stage.

According to Figure 1.3, the batteries are connected in parallel to the DC-link capacitor. Similarly, the 2L-VSC can be replaced by 3-Level PEC topologies, such as the Neutral Point Clamp (NPC) and T-type, shown in Figure 1.4. Five-Level PEC topologies are also found in the literature [42]-[44], providing further improved harmonic performance to the detriment of increased costs and operational complexity.

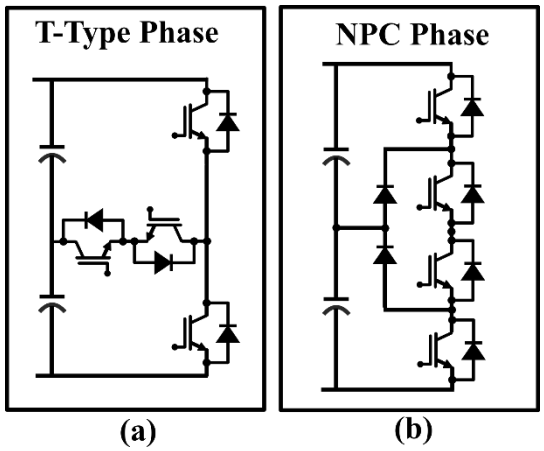



Figure 1.4. Examples of 3-Level converters: (a) T-type; (b) NPC.

After the DC-AC stage, the connection to the utility grid can be performed with or without transformers. For LV networks, the operator may request LV-LV transformers for galvanic isolation of the BESS [43]. For MV networks, commonly, an LV-MV step-up transformer is utilized. However, a transformerless connection can also be achieved through a series connection of semiconductor devices, as shown in Figure 1.5. By having multiple devices connected in series, the maximum blocking voltage requirement can be reduced as the voltage across each device is only a fraction of the DC-link voltage. However, the complexity of ensuring each device is turned on and off synchronously by the gate drivers and the higher switching losses are disadvantages of this solution [37].

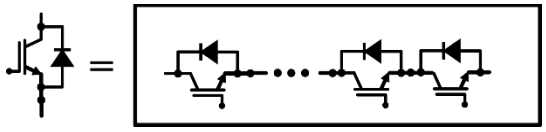


Figure 1.5. Series connection of semiconductors.

Considering a BESS connected to an MV network through a step-up line transformer (380V-11 kV), a DC-link voltage requirement can be established close to 600 Vdc. Since a single Li-ion battery cell has voltage levels that vary from 3 to 3.7 V, around 200-300 cells are required to be connected in series to meet the DC voltage requirement [40]. More cells must be connected in series if considering transformerless topologies. Figure 1.8 shows an additional DC-DC conversion stage that can be introduced between battery and DC-link to reduce this requirement. The DC-DC conversion stage boosts the voltage level of the batteries to meet the DC-link voltage requirements. Various topologies are available for the DC-DC stage. The synchronous boost converter, interleaved boost converter, and Dual-Active Bridge (DAB), shown in

Figure 1.7, can be listed as some of the most popular options because of their efficiency. The latter has the additional benefit of a medium/high-frequency transformer, thus providing galvanic isolation for the batteries and potentially replacing the bulky, costly, and lossy line-frequency transformer.

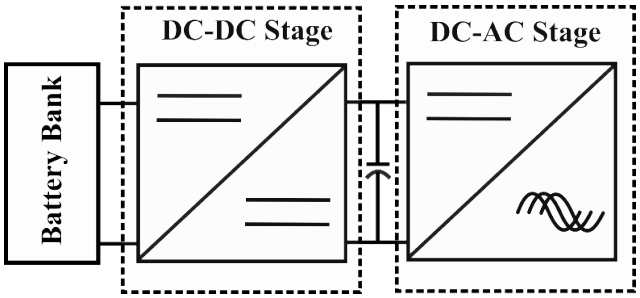



Figure 1.6. Dual Stage (DC-DC and DC-AC) BESS.

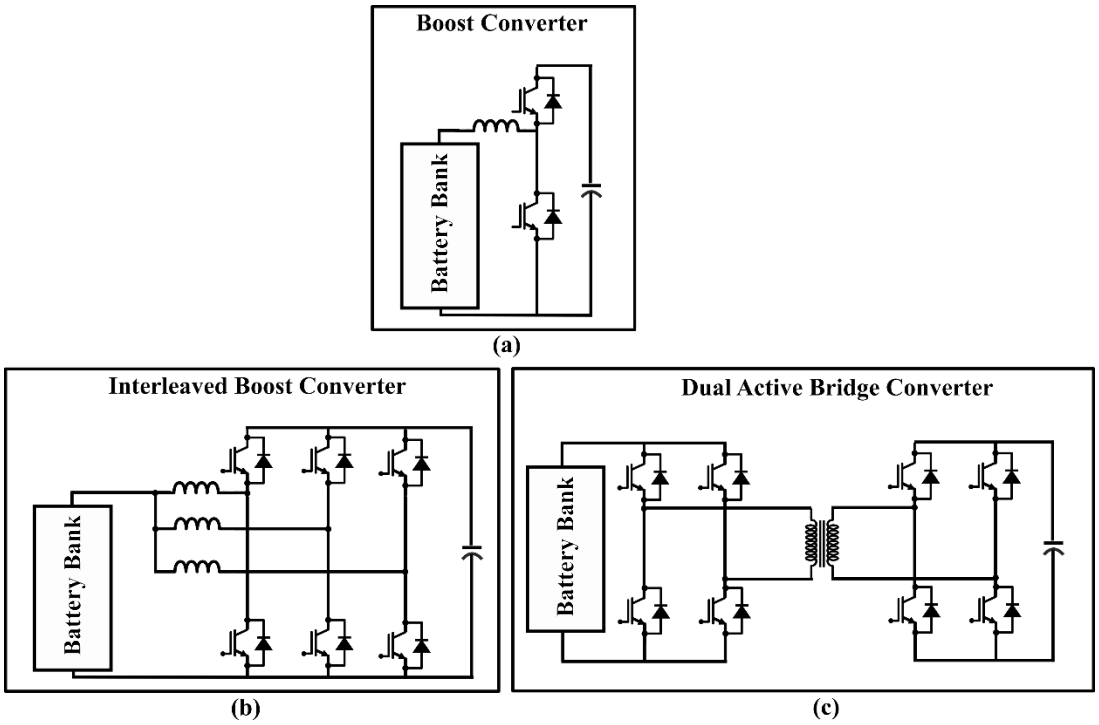



Figure 1.7. DC-DC stage PEC possibilities: (a) Boost converter; (b) Interleaved Boost Converter; (c) Dual Active Bridge Converter.

The connection of DC-DC PEC can also be modular. Connecting several battery packs in series can be avoided by utilizing DC-DC stages for each battery pack. Figure 1.8 shows two scenarios for the modular connection: series or parallel-connected output

[43]. Reliability improvement, system reconfiguration, and higher efficiency and power density can be listed as potential advantages of this connection [43].

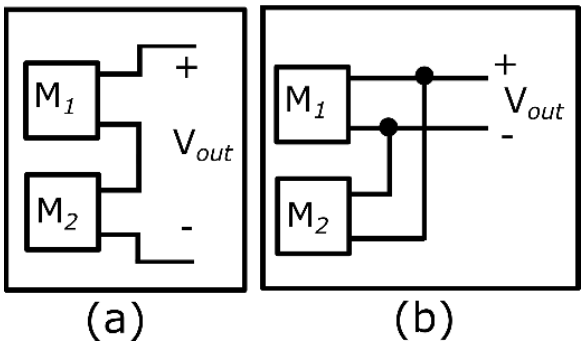
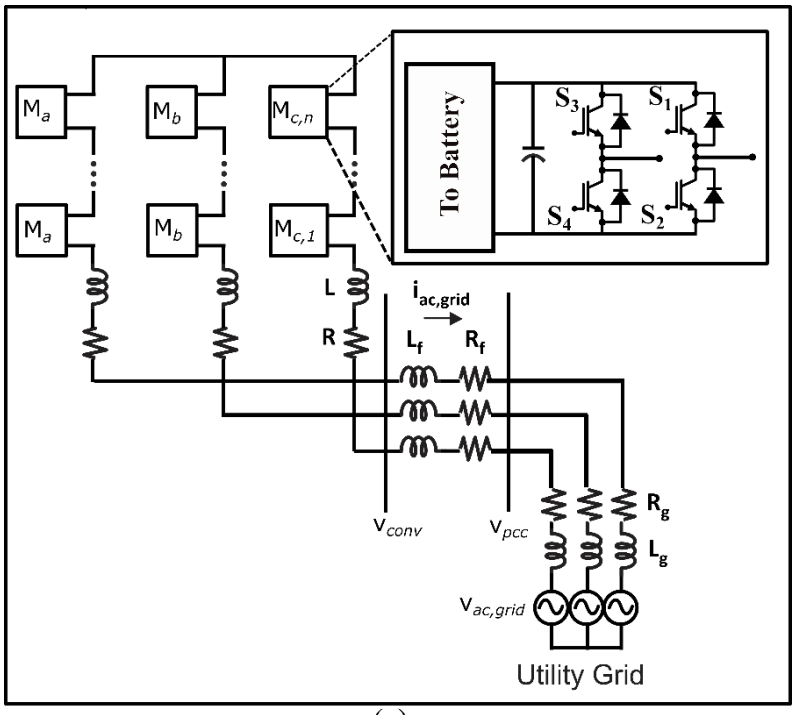


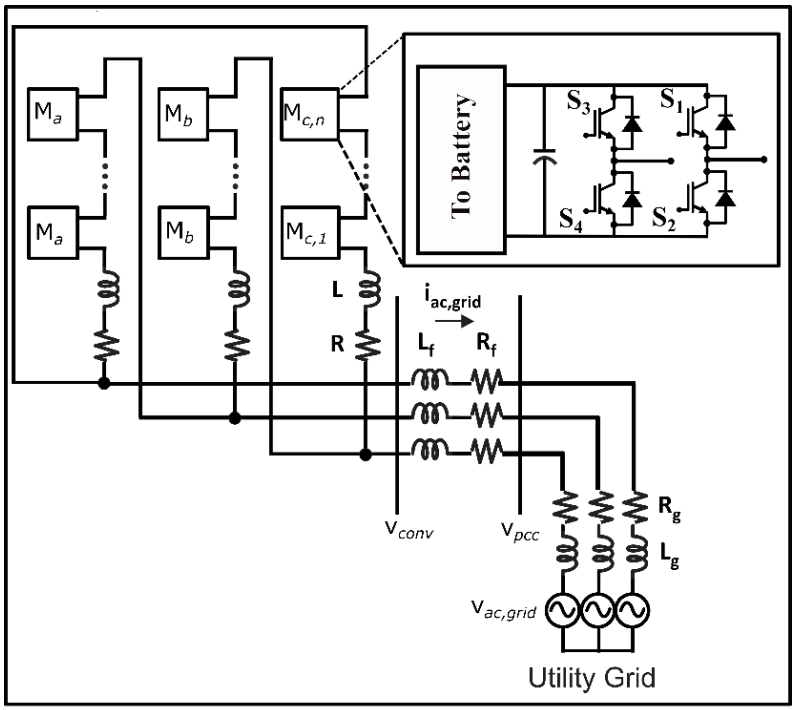

Figure 1.8. Dual Stage (DC-DC and DC-AC) BESS.

Another possibility to integrate low voltage battery packs into medium voltage electrical grids is by utilizing a family of converters known as Modular Multilevel Converters (MMC) [44]-[46]. The most common types of MMC are 1) the Single-Star Bridge Cell (SSBC); 2) Single-Delta Bridge Cell (SDBC), which is also known in the literature as Cascaded H-Bridge (CHB), and the 3) Double-Star connection, specifically the Double-Star Chopper Cell (DSCC). The different topologies are shown in Figure 1.9.

In many published research papers, including those that initially proposed the topology, the DSCC is referred to as simply MMC [47]-[49]. For convenience purposes, this terminology is also utilized interchangeably with DSCC throughout the dissertation, unless otherwise specified.


M_a
M_b
M_c,n
M_a
M_b
M_c,1
To Battery
S_3
S_1
S_4
S_2
L
R
i_ac,grid
L_f
R_f
R_g
L_g
V_conv
V_pcc
V_ac,grid
Utility Grid

(a)


M_a
M_b
M_c,n
M_a
M_b
M_c,1
To Battery
S_3
S_1
S_4
S_2
L
R
i_ac,grid
L_f
R_f
R_g
L_g
V_conv
V_pcc
V_ac,grid
Utility Grid

(b)

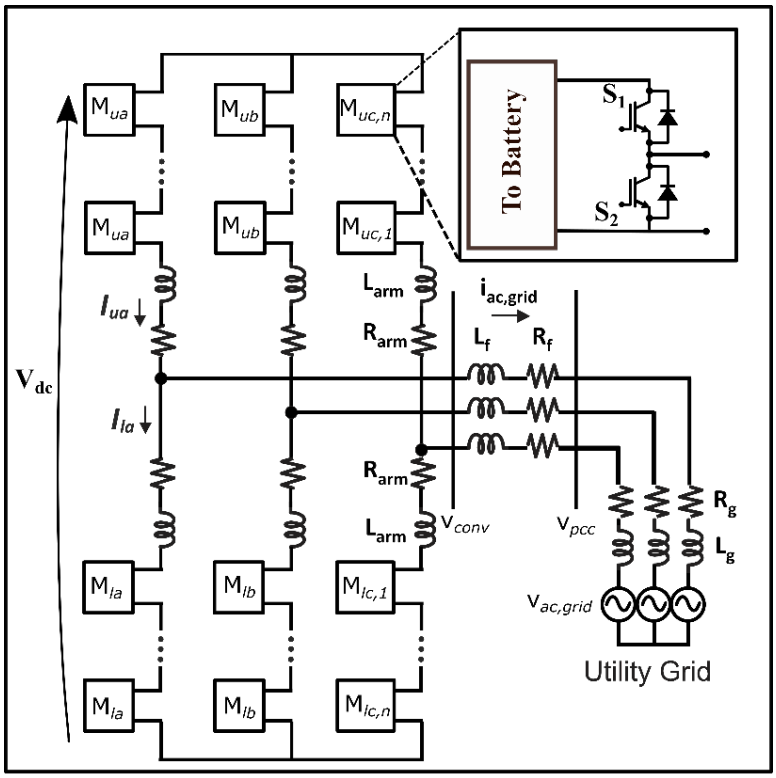



Figure 1.9. Modular Multilevel Converter topologies. (a) SSBC. (b) SDBC. (c) DSCC.

Figure 1.9 highlights that the energy storage elements are distributed among the different modules within this family of converters. Furthermore, these topologies are highly efficient. In a study presented in [37], a 30 MW BESS is integrated into a 22 kV electric grid. Five topologies are considered to interface with the grid: 2L-VSC, 2L-VSC with transformer, 3-Level, DSCC, and SSBC. The same number of DC-DC converters are considered for all topologies (for centralized topologies, the DC-DC converters have cascaded output to form the DC-link). This study shows that the DSCC and SSBC topologies have higher efficiency in all considered switching frequencies (from 2 to 6 kHz). The DSCC has a slight advantage with efficiency higher than 98% across all frequencies. The remaining 2L with transformer and 2L have efficiency lower than 96% at its highest, while the latter drops to 91% at its lowest. The 3L topology also

has considerably high efficiency, with 96.5% in the high switching frequency scenario. In terms of different outputted power, the DSCC also has the advantage when considering outputted power greater than 0.4 pu. According to this study, the main downfall of the MMC topologies is the capacitor requirements. Specifically, the MMC topologies require large capacitors to endure the harmonic oscillations in instantaneous power [37].

Because of high modularity, another critical advantage of the MMC is the fault-tolerant operation. Whenever a module fails, it can be removed from the process without impacting the system's operation by bypassing them [50], [51]. Finally, as the number of levels of the voltage synthesized by the converter increases with the number of modules, the MMC topologies have an overall much lower harmonic content when compared to 2L and 3L topologies. Given the listed advantages, this dissertation focuses on using the MMC topology as the DC-AC conversion stage between batteries and the utility grid. It must also be highlighted that the DC-DC bidirectional stage can be implemented in each module of the MMC, thus allowing even lower voltage batteries to be connected to the electrical grid.

### 1.2.2 Review of MMC operation

The MMC is comprised of n modules per arm, each containing a DC-link element (capacitor or battery energy storage element) and a half-bridge (chopper cell). Figure 1.9 shows an MMC with ideal voltage sources across each module. The voltage across the DC-link is $V_{dc}/n$.

There are four modes of operation for the MMC module assuming the use of IGBT technology switches:

- Current flows out of the module, and the upper switch is on: the DC-link discharges (Figure 1.11(a)).
- Current flows out of the module, and the upper switch is off: the module is bypassed (Figure 1.11(b)).
- Current flows into the module, and the upper switch is on: current flows through the diode and the DC-link is charged (Figure 1.11(c)).
- Current flows into the module, and the lower switch is on: the module is bypassed (Figure 1.11(d)).

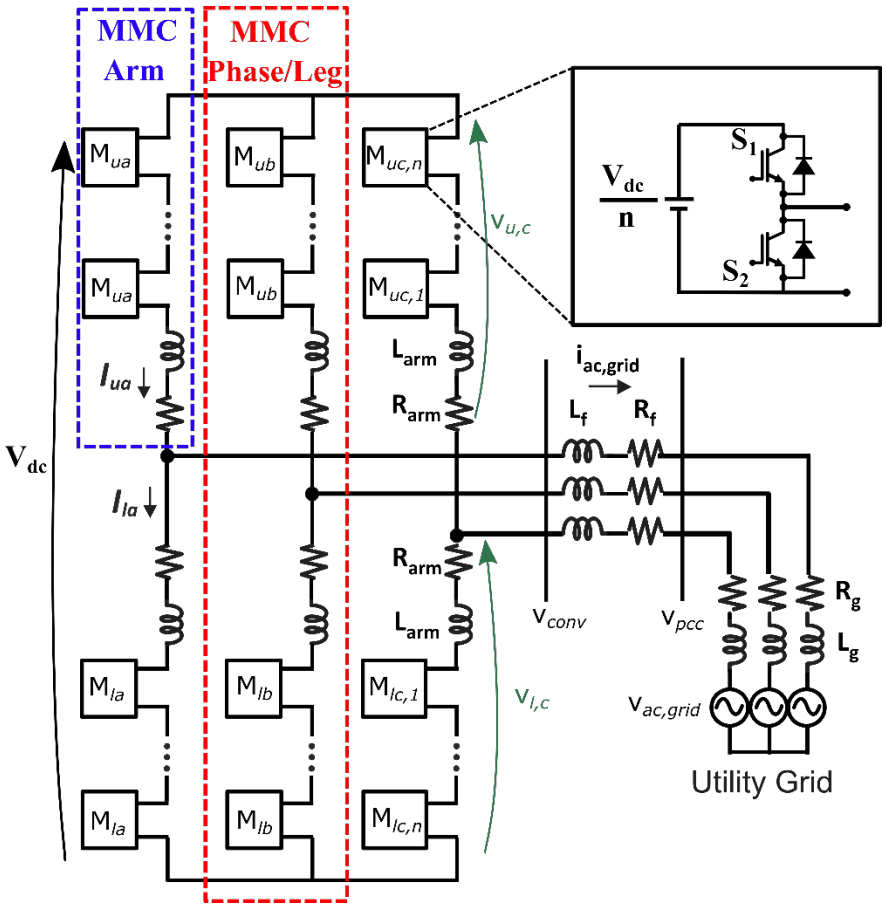



Figure 1.10. Basic MMC with ideal voltage source as DC-link for each module.

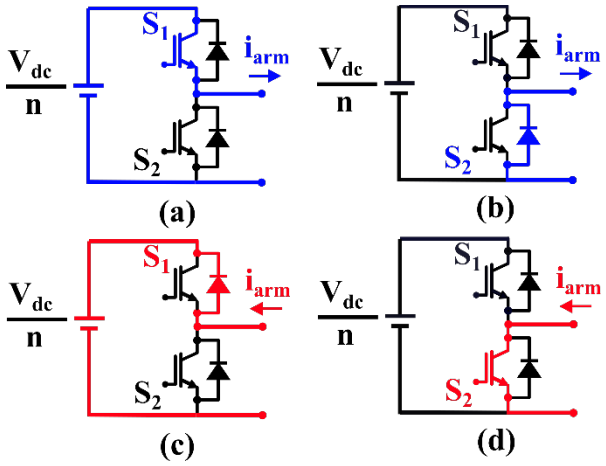



Figure 1.11. Modes of operation: (a) S1 on, current out; (b) S2 on, current out; (c) S1 on, current in; (d) S2 on, current in.

From Figure 1.10, the voltage across the upper and lower arms are

$$v_{u,k}(t) = \underbrace{\sum_{j=1}^{n}[s_{u,k}^{j} \cdot v_{dc}/n]}_{u_{u,k}} + L_{arm}\frac{di_{u,k}(t)}{dt} + R_{arm}i_{u,k}(t) \tag{1.1}$$

and

$$v_{l,k}(t) = \underbrace{\sum_{j=1}^{n}[s_{l,k}^{j} \cdot v_{dc}/n]}_{u_{l,k}} + L_{arm}\frac{di_{l,k}(t)}{dt} + R_{arm}i_{l,k}(t)\,, \tag{1.2}$$

where the subscripts u and l indicate upper and lower arms, respectively; the subscript k indicates phase (a, b or c). The superscript j indicates the module number. The constants $L_{arm}$ and $R_{arm}$ indicate arm inductance and resistance, respectively. The variable $s$ whether a module in a specific phase and arm is connected or bypassed; therefore $s$ assumes either the value 0 or 1. The variables $u_{u,k}(t)$, $u_{l,k}(t)$ are the voltages synthesized by all inserted modules in the upper and lower arms of a specific phase. Finally, $v_{u,k}(t)$, $v_{l,k}(t)$ are the voltage across the upper and lower arms.

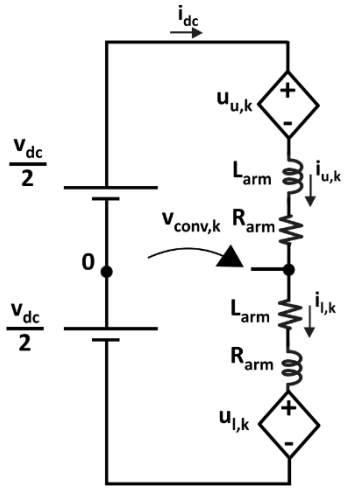



Figure 1.12. Single-phase representation of MMC.

In the paper where this topology is proposed [48], a single-phase representation is used to understand the output voltage of the MMC. The model is shown in Figure 1.12, from which Kirchhoff's Voltage Law (KVL) can be applied to obtain two expressions. The resulting expressions are

$$\frac{v_{dc}}{2} = u_{u,k}(t) + L_{arm}\frac{di_{u,k}(t)}{dt} + R_{arm}i_{u,k}(t) + v_{conv,k} \tag{1.3}$$

and

$$\frac{v_{dc}}{2} = u_{l,k}(t) + L_{arm}\frac{di_{l,k}(t)}{dt} + R_{arm}i_{l,k}(t) - v_{conv,k}\,. \tag{1.4}$$

From the current dynamic analysis presented in [48], the upper and lower arm currents are

$$i_{u,k} = \frac{i_{g,k}}{2} + i_{circ,k} \tag{1.5}$$

and

$$i_{l,k} = -\frac{i_{g,k}}{2} + i_{circ,k}\,, \tag{1.6}$$

where the subscript $g$ indicates grid and $circ$ indicates circulating current. These variables are inherent in the operation of the MMC. They are commonly used to describe the two degrees of freedom of the converter. The first degree of freedom relates to the operation of the MMC with the AC utility grid through the grid currents. The second degree of freedom is the current that circulates among the different phases of the converter, or simply the circulating current. Assuming the grid current direction indicated in Figure 1.10, the expression relating the AC utility grid side to the converter terminal is

$$v_{conv,k} = v_{g,k} + L_T \frac{di_{g,k}}{dt} + R_T i_{g,k}\,, \tag{1.7}$$

where the $L_T$ and $R_T$ are the total lumped inductance and resistance in the system (addition of filter and grid). Note that for simplification purposes, $i_{ac,grid}$ is simply written as $i_g$. Substituting (1.5), (1.6) and (1.7) into (1.3) and (1.4), and then both adding and subtracting the resulting equations, leads to

$$v_{dc} = u_{l,k} + u_{u,k} + 2L_{arm} \frac{di_{circ,k}}{dt} + 2R_{arm} i_{circ,k} \tag{1.8}$$

and

$$0 = u_{l,k} - u_{u,k} + L_{arm} \frac{di_{g,k}}{dt} + R_{arm} i_{g,k} - 2v_{g,k} + 2L_g \frac{di_{g,k}}{dt} + 2R_g i_{g,k}\,. \tag{1.9}$$

The results shown in (1.8) and (1.9) highlight that first-order differential equations govern both the circulating current and grid current. Furthermore, based on the superposition principle, the control variables $u_{l,k}$ and $u_{u,k}$ are used to independently control the current components. Particularly, the additional degree of freedom related to the circulating current can be exploited to transfer power between different modules

to achieve several objectives, such as balancing the state-of-charge (SOC) of batteries and power balancing strategies. Specifically, the circulating current can be used to exchange power between the different phases and arms of the MMC, as shown in Figure 1.13. The additional degree of freedom is fully utilized throughout the dissertation when proposing novel power balancing and SoC balancing techniques under specific scenarios that are described in the following chapters.

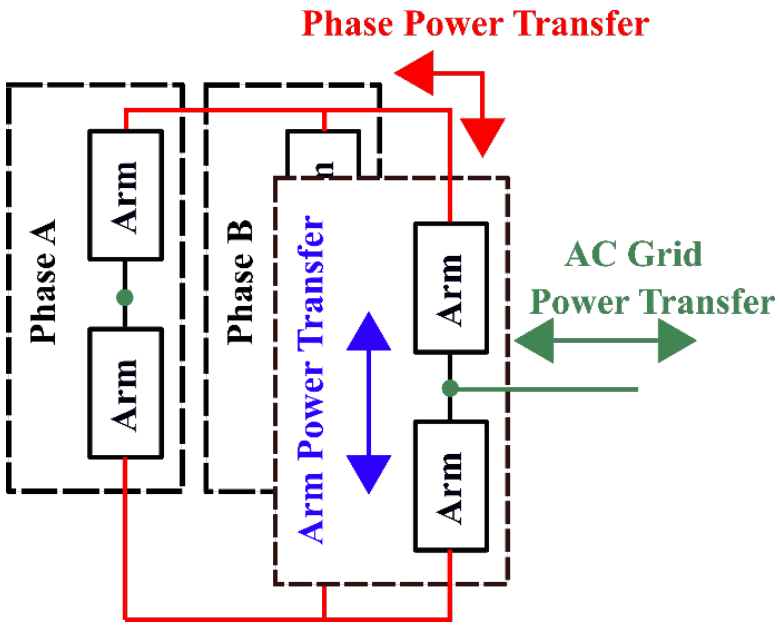



Figure 1.13. MMC power exchange.

### 1.3 Research Contributions

This dissertation focuses on different aspects of a BESS-MMC operation. The research contributions vary from an analysis at the battery level to the system level, highlighted in different colors in Figure 1.14. The research contributions are summarized below:

- At battery level: A novel methodology to estimate the equivalent circuit model parameters (ECM) of an LFP battery focusing on their use in grid

applications is presented. The parameters dependency on the state-of-charge (SoC) and the temperature are included. Correlation between parameters and the SoC is obtained through polynomial regression, with the goodness of fit measured by the coefficient of determination ($R^2$). Comparisons with classical approaches are drawn and showcase the accuracy of the proposed model. In addition, the battery cells are degraded based on the grid frequency regulation profile, aiming to identify the parameter value change over the battery usage. Identifying battery parameters, specifically its impedance, is helpful for fine-tuning control gains and designing circuit parameters in Battery Energy Storage Systems.

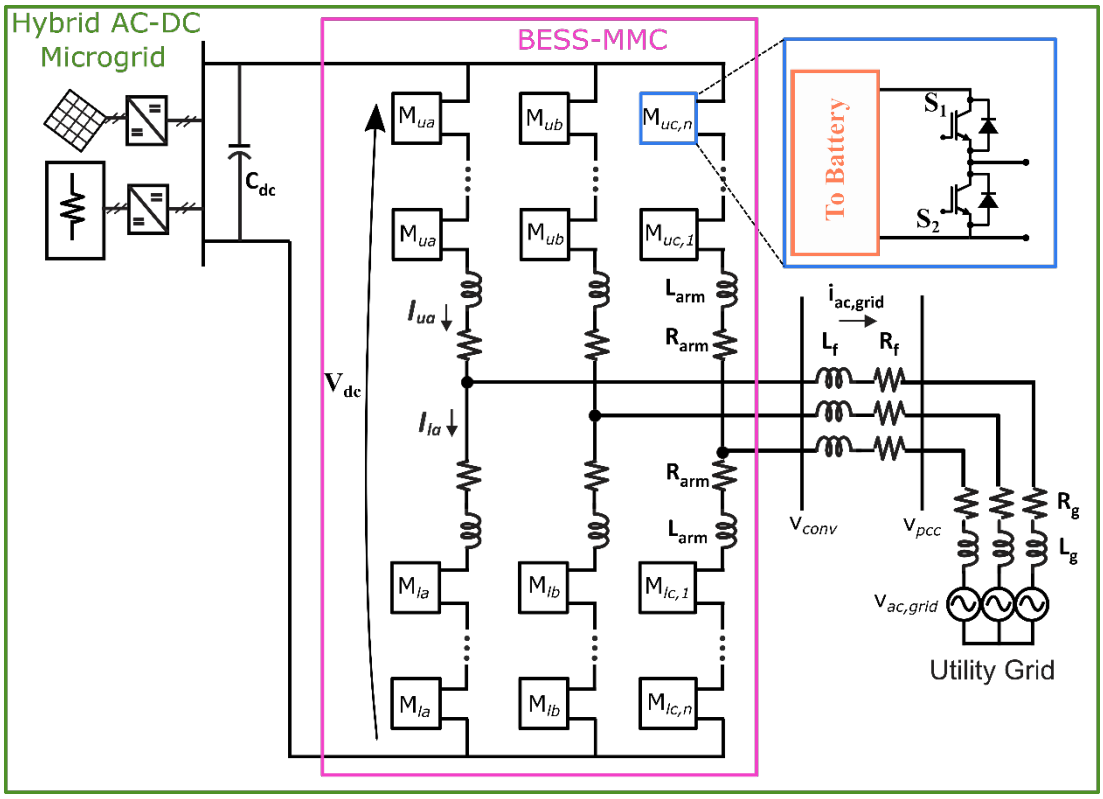



Figure 1.14. Dissertation contributions.

- At the MMC module level: Determining the sizing of the module's DC-link capacitor is of crucial importance for the safety and operational purposes of the BESS-MMC. A mathematical analysis is carried out in which the intrinsic relationship between battery impedance parameters, bidirectional converter controller, battery current ripple, and module's DC-link voltage fluctuation is fully exposed. Based on this relationship, the sizing of the DC-link capacitor can be found based on any configuration of MMC, irrespective of power and voltage level and the number of modules integrated.

- At BESS-MMC (including AC grid) level: Fault-tolerant and asymmetric (concerning the number of modules in the MMC) operation of the BESS-MMC is proposed in this thesis. The first scenario considers the continuous operation of the BESS-MMC during an asymmetric AC grid fault, which leads to asymmetric grid voltages. Because of the modular connection of batteries, power balancing is required to avoid power unbalance between the three phases of the converter, thus hindering phase SoC asymmetry. Additionally, if the phase SoC already has deviation during the grid faults, the battery charge must be balanced to prolong the operation during the adversity. The proposed strategies take the batteries' power limits as an input to avoid their overuse and triggering protection mechanisms. Asymmetric power available in each arm and phase is considered within the MMC in the second scenario. Given the symmetric operation with the grid, to inject the maximum power available, a novel strategy is proposed making use of power exchange between the different phases and arms.

- At Hybrid Microgrid level: Utilization of the MMC-BESS as an interlinking converter (IC) between the utility grid (or AC microgrid in grid-disconnected mode) and DC microgrid is proposed. With the MMC-BESS as IC, the topology's two degrees of freedom can be used to their full potential, i.e., achieving decoupled operation between AC and DC grids. This is possible because the circulating current is responsible for regulating the DC grid voltage while depending on the availability of the utility grid, the grid current control is used to either regulate AC grid frequency and amplitude (grid-disconnected) or any grid following operation (e.g., PQ control). This operation allows the resources connected on both AC and DC sides to operate in the grid following mode since the references are set either by the IC or the utility grid. Finally, power management strategies are proposed and discussed thoroughly.

### 1.4 Dissertation Outline

The dissertation is organized as follows:

1. Chapter 2 presents a state-of-charge (SoC) dependent equivalent circuit model (ECM) for LiFePO4 batteries based on statistical data obtained for a BESS providing grid frequency regulation. The dataset is obtained using an experimental setup with LiFePO4 battery cells, Arbin's battery testing unit, and a thermal chamber. Furthermore, accelerated aging tests are performed based on grid frequency regulation profile at temperatures near the safety operational limit of LiFePO4 batteries. In addition to the previously mentioned setup components, Gamry's galvanostat is used for electrochemical impedance spectroscopy (EIS) analysis. Results showcase the

appropriateness and accuracy of the proposed model and the impedance change of batteries over time.

2. Chapter 3 presents an analysis of the BESS-MMC with interfacing bidirectional converters for each modular-connected battery. Battery current ripple reduction requirements and implementation are obtained through digital filter-controller combinations without degrading the loop performance in terms of gain crossover frequency and phase margin. The chapter also presents the mathematical analysis to identify the MMC capacitor sizing. Results are validated through Controller Hardware-in-the-loop (C-HIL) results within the Typhoon HIL environment and using Texas Instruments Digital Signal Processors (DSPs).

3. Chapter 4 presents the operation of BESS-MMC under grid voltage asymmetry. Both power balancing and SoC balancing schemes with well-defined battery power limiters are presented. Furthermore, the proposed operation of the BESS-MMC with asymmetric power available in each arm and phase is also presented. C-HIL results are obtained for validation of the proposed strategies.

4. Chapter 5 presents the operation of the BESS-MMC as a salient feature of a hybrid DC/AC microgrid, i.e., as an interlinking converter between microgrids. Control strategies to highlight system resilience, decoupling effect between grids, and the power balancing strategies for both operating modes, are proposed and validated through Typhoon HIL results.

5. Chapter 6 summarizes the dissertation contributions, highlighting the principal features. The thesis is concluded after briefly discussing the future scope of research.

# 2. BATTERY IMPEDANCE PARAMETER ESTIMATION FOR GRID APPLICATIONS

## 2.1 Introduction

In Chapter 1, the current trends in BESS for grid applications are discussed. Further, Lithium-ion batteries, more specifically, LiFePO4, have been identified as one of the most commonly employed technologies for power exchange with the grid. The reason relates to its higher energy and power density compared to other technologies such as lead acid, nickel cadmium, nickel-metal hydride, etc. [52]. Furthermore, Li-ion batteries have extended life cycle capability. The combination of these characteristics makes Li-ion batteries highly desirable in grid energy storage and numerous applications such as portable electronics - laptops and smartphones, cordless power tools, and electric vehicles (EVs) [53].

Obtaining battery models is a fundamental step for the implementation of PEC controller design, DC-link capacitor/filter sizing, and Battery Management Systems (BMS). The latter can also be used for State-of-Charge (SOC) and State-of-Health (SOH) estimation. Battery models can be an electrochemical model (EM) or an electrical equivalent circuit model (ECM) [54]. Though EM is highly accurate, it is more complex and requires high computation to implement in real-time applications like BMS [54]. Nevertheless, there is a continuous effort to minimize the computational burden of such models as BESS are usually expensive and large, and any improvement can lead to economic gain [55]. ECM with simple electrical circuit components is an excellent alternative to EM for real-time applications and real-time emulator platforms.

However, the accuracy of ECM is highly dependent on the tested load profile. Hence, a model deemed accurate for a particular load profile may not have the same accuracy when used with a different load profile [55].

ECM parameters estimation can be divided into offline and online methods [56]. Offline methods use archived data to estimate the battery parameters, while online methods find the battery parameters in real-time. The offline method's limitation is the need for the load profile for the estimation, while the online method requires higher computational power and storage. Furthermore, although there is continuous research on the use of different algorithms for online estimation, the stability, robustness, and computational cost is still a challenging task [57].

The load profile is a critical aspect of characterizing the battery. For EV applications, numerous load profiles can be used to characterize the battery, such as the urban dynamometer driving schedule (UDDS) [58]. However, the load profiles for the grid energy storage applications are different from that of the EV applications [59]. In [60], a statistical data profile over a 3-year usage of a 1MW Battery Energy Storage System (BESS) is assessed. This chapter utilizes this statistical information to obtain a load profile for grid energy storage applications.

The parameters obtained for the ECM through the load profile can be dependent on the C-rate (magnitude of the current), the SoC, and the temperature. Genetic algorithm-based parameter estimation has been utilized to identify the ECM parameters with SoC dependency [61]. However, the correlation between the parameters and SoC using this methodology could not be represented by a simple linear curve. In [62], the ECM is identified as a “lumped parameter model,” in which the parameters are

correlated with the SoC and C-rate. However, the temperature is not considered. In [63], the parameters are identified using an iterative method based on the computation of the linear-parameter-varying state-space model. However, the results fail to converge and might result in instability.

In this chapter, an offline methodology that utilizes the load profile data, containing a range of C-rates, for obtaining ECM parameters that are dependent on temperature and SoC is proposed. To ensure the uniqueness of the solution, subspace identification has been used [64]. The parameter dependency on SoC is represented by a trend curve obtained using polynomial regression. Finally, two models are derived, one with SoC-dependent parameters and another with SoC-independent parameters. The experimental results for the proposed and conventional methods are discussed in detail. In addition, accelerated aging tests are performed at high temperatures to estimate the ECM parameter variation over the battery lifetime. The tests consist of continuously imposing a load profile (in this case, grid frequency regulation) over an extended period. Obtaining the maximum variation of the ECM parameters can be helpful in the design of components in BESS-MMC (e.g., capacitors) and control gain parameters.

## 2.2 Proposed SoC-dependent Equivalent Circuit Modeling

### 2.2.1 Equivalent Circuit Model

Equivalent circuit models (ECMs) are empirical models derived with a reduced number of battery parameters. ECMs have gathered attention for their simplicity and accuracy. The most common ECMs comprise a DC-voltage source ($V_{oc}$, i.e., open-circuit voltage), a series resistance ($r_{int}$) to represent the ohmic drop in the battery cell,

and a series connection of multiple parallel $rc$ components. The time constant of a parallel $rc$ is given by $\tau = rc$. ECMs differ by the number of $rc$ pairs considered. In this chapter, two of the most popular ECMs are considered: one based on a single $rc$ pair configuration and another based on two $rc$ pairs. The single $rc$ model, also called the "first-order $rc$ model," is one of the simplest ECMs used to characterize battery behavior. The double $rc$ model is widely known as the "second-order $rc$ model" in the literature. The $rc$ pairs for the second-order model (usually one with a short transient time and another with a long transient time) are sometimes associated with the charge transfer and diffusion electrochemical effects of the Li-ion battery. However, since ECMs are only empirical models and not electrochemical models, the $rc$ pairs cannot be associated with any specific electrochemical effects [65]. Instead, the $rc$ pairs can be seen simply as an emulation of the overall polarization effect of the terminal voltage when subject to a specific load. Figure 2.1 shows the general ECM configuration.

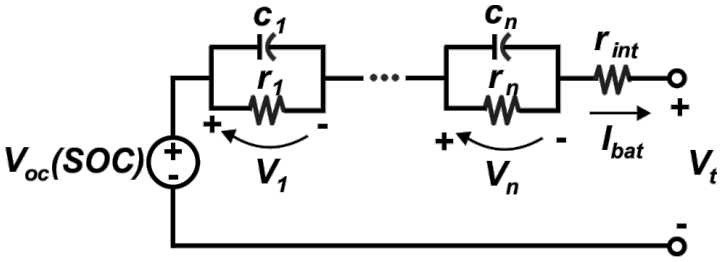



Figure 2.1. Battery equivalent circuit model.

The discrete-time state-space equations of the cell model are

$$\begin{bmatrix} SOC_{k+1} \\ V_{1,k+1} \\ \vdots \\ V_{n,k+1} \end{bmatrix} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & e^{-\frac{\Delta t}{r_1 c_1}} & \cdots & 0 \\ 0 & 0 & \ddots & 0 \\ 0 & 0 & 0 & e^{-\frac{\Delta t}{r_n c_n}} \end{bmatrix} \begin{bmatrix} SOC_k \\ V_{1,k} \\ \vdots \\ V_{n,k} \end{bmatrix} + \begin{bmatrix} -\eta \Delta t / Q_{nom} \\ r_1(1 - e^{-\Delta t / r_1 c_1}) \\ \vdots \\ r_n(1 - e^{-\Delta t / r_n c_n}) \end{bmatrix} I_{bat} \qquad (2.1)$$

and

$$V_{t,k+1} = V_{oc_k}(SoC) - r_{int}(SOC)I_{bat_k} - V_{1,k} - \cdots - V_{1,k}(t), \tag{2.2}$$

where the subscript $k$ and $k+1$ represent the k$^{th}$ and (k+1)$^{th}$ samples, respectively, $V_n$ is the voltage across the n$^{th}$ $rc$ pair, $\Delta t$ is the sampling time, $V_t$ is the terminal voltage of the cell, $Q_{nom}$ is the nominal capacity of the cell, $I_{bat}$ is the battery current, $r_n$ and $c_n$ are the respective resistance and capacitance values of the nth $rc$ pair. As mentioned previously, a single $rc$ pair ECM (n=1) and a two $rc$ pair ECM (n=1,2) are considered.

The ratio between discharge capacity and charge capacity can also be taken into consideration in ECM. This ratio is known as coulombic efficiency and is represented by the variable $\eta$ in (2.1) [65]. The coulombic efficiency varies with the cell chemistry and the temperature. However, the experimental results in Section 2.3 have shown that this value is found to be near unity. The ECM parameters are usually assumed as a constant value for simplicity. However, the parameters are needed to be considered as a function of temperature and open-circuit voltage for increased accuracy. The tests need to be performed under different temperatures to obtain the temperature-dependent parameters.

Most ECMs, such as the models analyzed in the comparative work presented in [54] do not take into consideration the parameters' dependency on the SoC and the C-rate. The C-rate is the rate at which the battery is discharged relative to its maximum capacity. For example, a battery with a capacity of 3.3Ah has C-rate 1C = 3.3 A. References [61]-[63] show the effect of the C-rate and the SoC on battery parameters. This can be visualized from equation (2.1), where the parameters can be considered as

constant values (e.g., $r_{int,} = R_{int}$) or varying with respect to SoC (e.g., $r_{int} = f(SoC)$) or with both SoC and C-rate (e.g., $f(SoC, C - Rate)$).

### 2.2.2 Performed Tests

Two different tests need to be performed to obtain each parameter of the ECM: a static test and a dynamic test. The static test is carried out to obtain the open-circuit voltage ($V_{OC}$) as a function of the SoC, while the dynamic test is carried out to obtain the parameters of the ECM.

The static test is performed by following the procedure presented in [65]. Under this procedure, the battery is slowly discharged (the discharge is done with a constant current profile at a C/30 rate) from its initial fully charged state until it reaches the minimum voltage specified by the manufacturer. The low C-rate makes the polarization effect to be minimal in scale. Similarly, the battery is slowly charged at a C/30 rate from its initial discharged state until it reaches its maximum voltage specified by the manufacturer.

To ensure that the battery is fully charged or discharged, the polarization effect has to be entirely eliminated. This can be achieved by applying a dither voltage signal at the battery terminals, as shown in Figure 2.2. The dither voltage signal is a repetitive frequency sweep with a peak-to-peak amplitude of 20 mV over the manufacturer's specified discharge and charge voltage limits.

The static test provides two open-circuit-voltage versus SoC curves: one curve during charging and another curve during discharging. These curves are combined to obtain a single curve that represents the relation of the open-circuit voltage and the SoC.

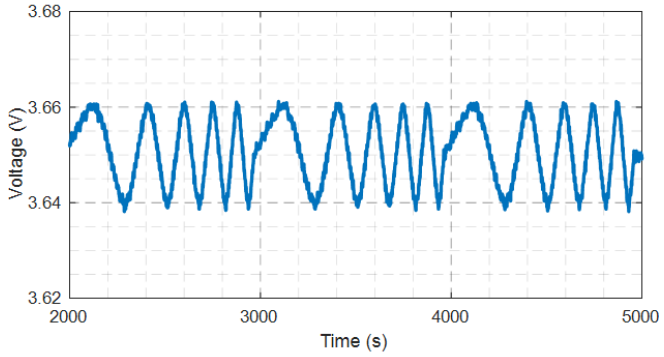



Figure 2.2. Dither signal for SoC calibration.

In this work, this test is repeated for three different sets of temperatures. According to the manufacturer's specification, the LFP battery should operate with maximum temperature of 45°C [66]. Considering the static operation of the battery (grid energy storage), it is feasible that a robust thermal management system can be employed to maintain the battery within safe temperature range [67]. Therefore, for this test, the chosen temperatures are 15°C, 25°C and 35°C. Figure 2.3 shows the result of the static test.

The dynamic test requires a dynamic load profile that must be representative of the grid energy storage application for obtaining parameter values that will yield more accurate results. The dynamic profile presented in Figure 2.4 is repeated for the cell at different SoCs (beginning from 90% down to 20%, with a 10% SoC step). The dynamic profile is obtained through three-years statistical data of a BESS [60]. The data suggests that most of the current pulses have a duration of less than 10 seconds, while their current amplitude varies with an average maximum value of C-rate 3C. Similar to the static test, the dynamic test is performed at three different temperatures (15°C, 25°C and 35°C).

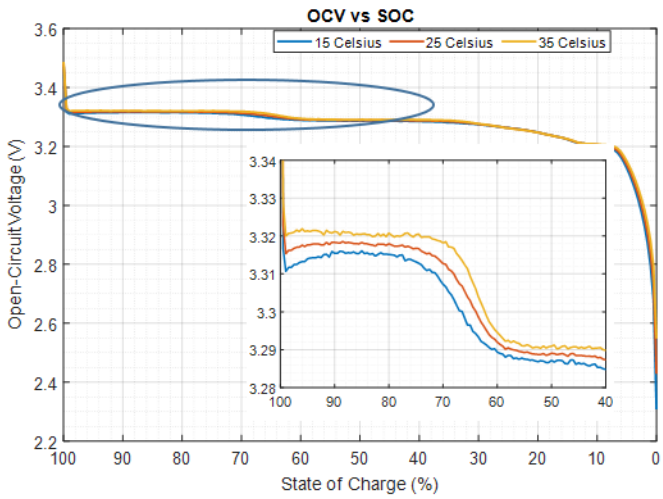



Figure 2.3 OCV-SoC relation at different temperatures.

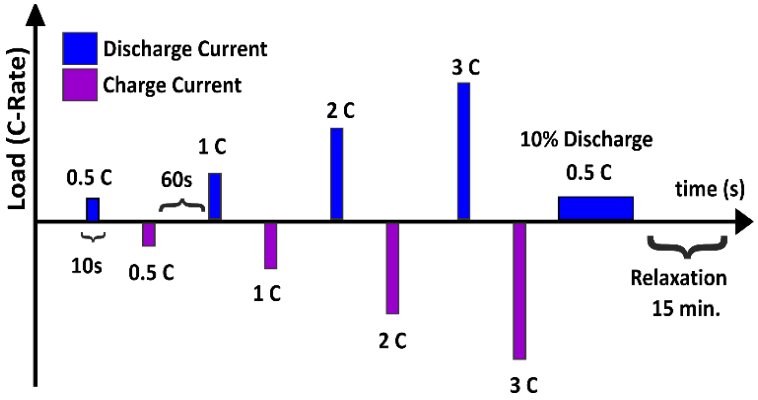



Figure 2.4. Dynamic load profile for a given SOC.

### 2.2.3 Lumped Parameter Model (Methodology 1)

The first methodology considered to calculate the ECM parameters is presented in [62]. The model considers only a single $rc$ pair in series with the internal resistance $r_{int.}$ The parameters can be calculated directly from a pulse profile. Figure 2.5 illustrates a pulse profile voltage response from which the parameters are obtained.

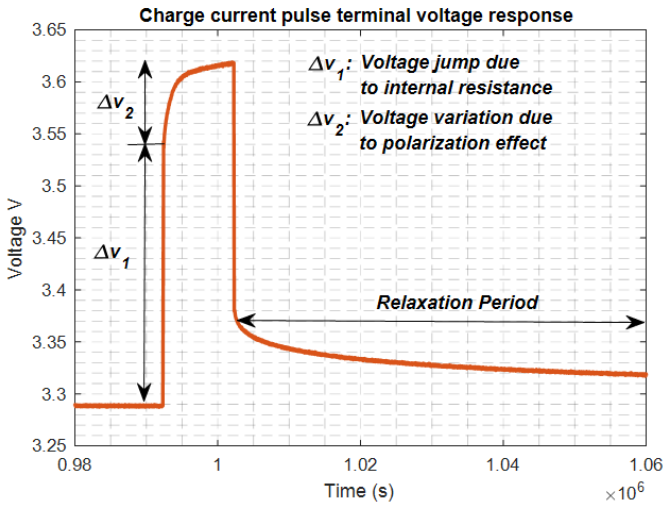



Figure 2.5. Terminal voltage rise/drop for a given pulse.

Using this methodology, the internal resistance is

$$r_{int} = \frac{\Delta V_1}{I_{bat}}, \tag{2.3}$$

where $\Delta V_1$ is the voltage jump caused by the applying current pulse and $I_{bat}$ is the amplitude of the pulse. The resistance $r_1$ of the rc pair is

$$r_1 = \frac{\Delta V_1 + \Delta V_2}{I_{bat}} - r_{int}, \tag{2.4}$$

where $\Delta V_1 + \Delta V_2$ is the voltage difference at the end and beginning of the pulse. The capacitance of the *rc* is calculated during the relaxation period. The approach in [65] is implemented, where the relaxation period (the time period until the next pulse appears) is used to calculate the time constant, and, consequently, the capacitance value is

$$c_1 = \frac{\Delta t_{relax}}{4R_1}, \tag{2.5}$$

where $\Delta t_{relax}$ is the relaxation period in seconds.

With this methodology, it is possible to calculate the parameters for every pulse at every SoC. As such, for each pulse application, it is possible to obtain the correlation between the parameters and the SoC, and the correlation between the ECM parameter and C-Rate. A detailed study on the results using this method is discussed in Section 2.3.

### 2.2.4 Subspace Identification Method (Methodology 2)

The second methodology considered to calculate the ECM parameters is based on the subspace identification technique [64]. This technique uses linear algebraic operations (such as singular value decomposition (SVD)) to identify the parameters based on the input/output information under the load profile. For the battery characterization, the input is the battery current and the output is the terminal voltage.

The steps to obtain the parameters are briefly described as follows:

1) Based on the load current and terminal voltage sample vectors, Hankel matrices are formed.

2) Using the projection of the matrices and SVD, the order of the system and state sequences are determined.

3) Least squares method is used to obtain the numerical value of the state-space matrix of the system, from which the ECM parameters can be directly computed.

A detailed mathematical analysis and derivation of the subspace identification can be referred in [64]. This technique has become quite popular for applications across different engineering areas, and its implementations are available in Python and MATLAB libraries.

### 2.2.5 Proposed Methodology (SoC-dependent parameters)

A new approach to the subspace identification method has been applied by considering separate datasets for different SoCs. Instead of having a single value for each parameter in the ECM, different sets of parameters for each SoC are identified. Hence, multiple ECMs that would accurately represent the battery behavior under specific SoC are derived. The correlation between the parameter values and the SoC can be described by a simple polynomial function (a quadratic function is considered). The ECM parameters are function of the SoC and described as follows:

$$r_{int}(SoC) = r_{int,2} \times (SoC)^2 + r_{int,1} \times (SoC) + r_{int,0}, \tag{2.6}$$

$$r_n(SoC) = r_{n,2} \times (SoC)^2 + r_{n,1} \times (SoC) + r_{n,0}, \tag{2.7}$$

and

$$c_n(SoC) = c_{n,2} + (SoC)^2 + c_{n,1} \times (SoC) + c_{n,0}. \tag{2.8}$$

From the above previous equations, $r_{int}(SoC)$, $r_n(SoC)$ and $c_n(SoC)$ are the SoC-dependent parameters, which are described by a quadratic function. The coefficients are obtained through polynomial regression. The quadratic function is chosen, and the fitness of the function is analyzed in the following section.

## 2.3 Experimental Results

The experimental tests are conducted using the Arbin battery testing unit LBT22023. Since three different temperatures are considered (15ºC, 25ºC and 35ºC), the TestEquity temperature chamber model 123C is also employed to soak the battery

to the predetermined temperature. The experimental setup is shown in Figure 2.6(a). The Li-ion iron phosphate cell 26650 from Dakota Lithium, shown in Figure 2.6 (b), is used for the tests performed. Table 2.1 indicates the specifications of the cell provided by the manufacturer.

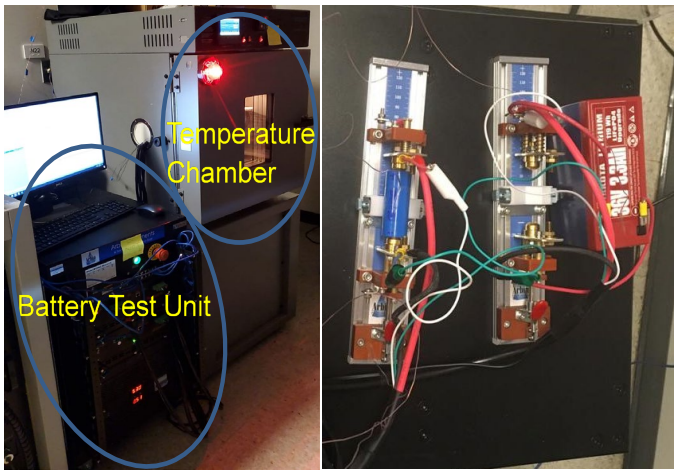



Figure 2.6. Experimental setup: (a) Battery testing unit and thermal chamber; (b) Batteries under test.

Table 2.1 Lithium-ion Iron Phosphate Cell Specifications

| **Parameter** | **Specification** |
|---|---|
| Nominal Capacity | 3.4 Ah |
| Nominal Voltage | 3.2 V |
| Discharge Cut-off Voltage | 2 V |
| Charge Cut-off Voltage | 3.65 V |
| Max. Discharge Current | 9.9 A |
| Max. Pulse Discharge Current | 5C |

The first methodology is used to investigate the dependency of the battery parameters on the C-rate and the SoC. The calculations are done for every pulse in the load profile. For this test, the ambient temperature of 25ºC is considered. The battery parameter $r_{int}$ as a function of SoC for different C-rate is shown in Figure 2.7. The battery parameter $r_{int}$ as a function of C-rate for different SoC is shown in Figure 2.8. It can be inferred from Figure 2.7 and Figure 2.8, that the obtained $r_{int}$ values are closely confined within a region of 5 $m\Omega$. Figure 2.8 shows that the variation of $r_{int}$ as a function of C-rate cannot be tracked by lower-order polynomial regression. These results contrast with the one obtained for $r_1$, in Figure 2.9 and Figure 2.10. In this case, it is observed that the variation of this parameter both as a function of SoC and as a function of C-rate can be described by a correlation curve.

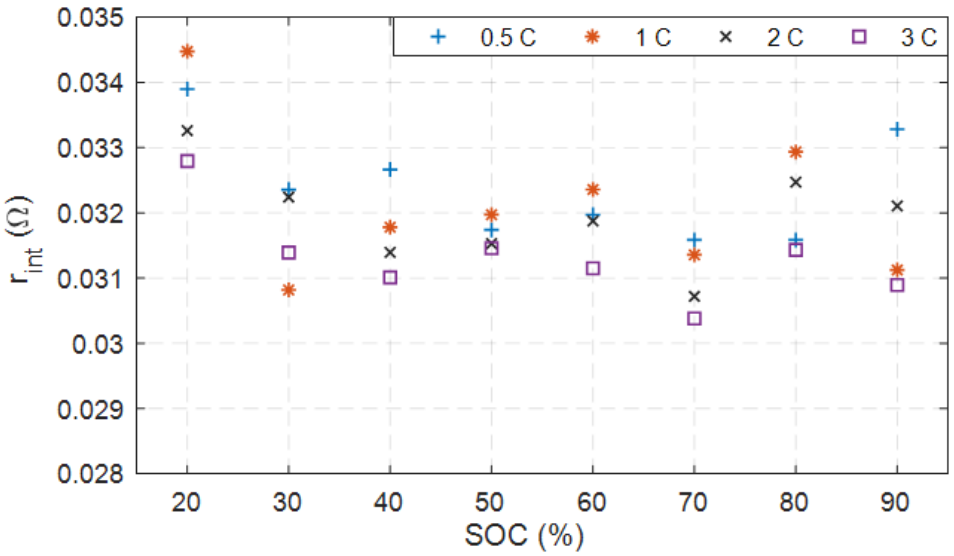



Figure 2.7. $r_{int}$ variation as a function of SoC for different C-rate at T=25°C using methodology 1.

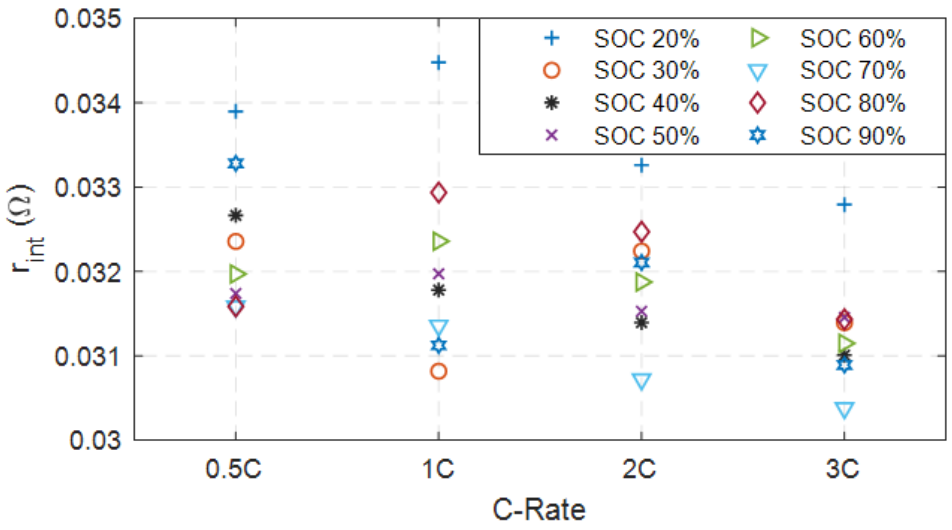



Figure 2.8. $r_{int}$ variation as a function of C-rate for different SoC at T=25°C using methodology 1.

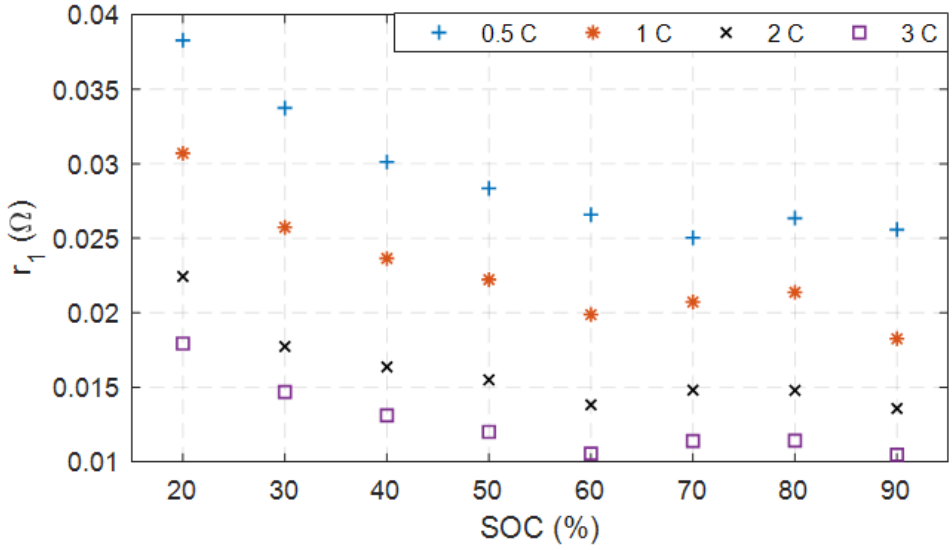



Figure 2.9. $r_1$ variation as a function of SoC for different C-rate at T=25°C using methodology 1.

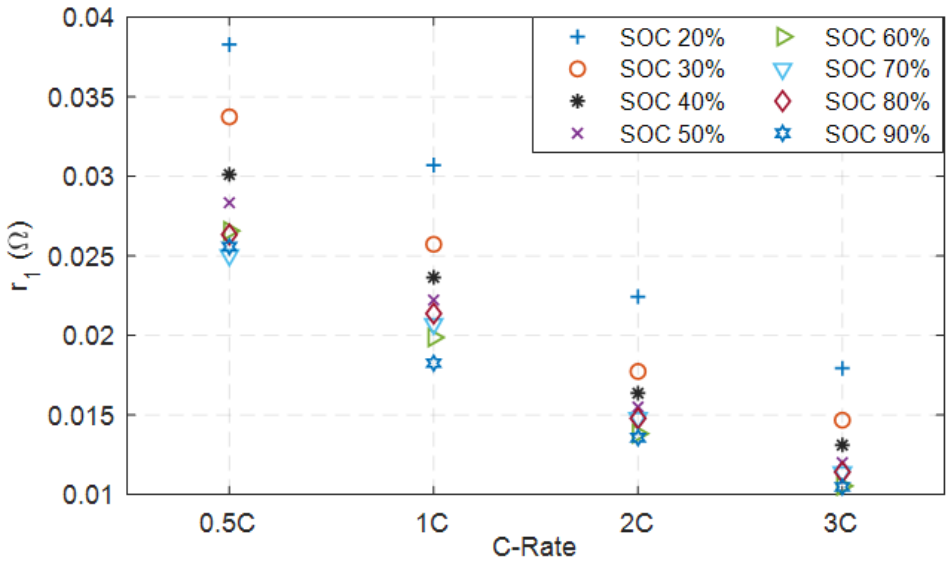



Figure 2.10. $r_1$ variation as a function of C-rate for different SoC at T=25°C using methodology 1.

The methodology 1 requires the calculation of every single parameter for all possible pulses, which illustrates the change of parameters under different scenarios. However a methodology that can find a single solution is more attractive with respect to battery modelling. This can be achieved with the methodology 2.

The values of $r_{int}$ and $r_1$ parameters of the battery using methodology 2 and the proposed method are shown in Figure 2.11. The results for different temperatures are also presented in Figure 2.11. Using polynomial regression, a quadratic function is obtained to describe the correlation between the parameters and the SoC. To quantify the described function for parameter change, the coefficient of determination, known as $R^2$, is used. In the worst-case scenario, the quality of the fitting is found to be $R^2 = 0.86$, using this methodology, while the best case fit is found as $R^2 = 0.86$. This indicates that the parameter values calculated based on the experimental results at different SoC are found to be near the trend line obtained.

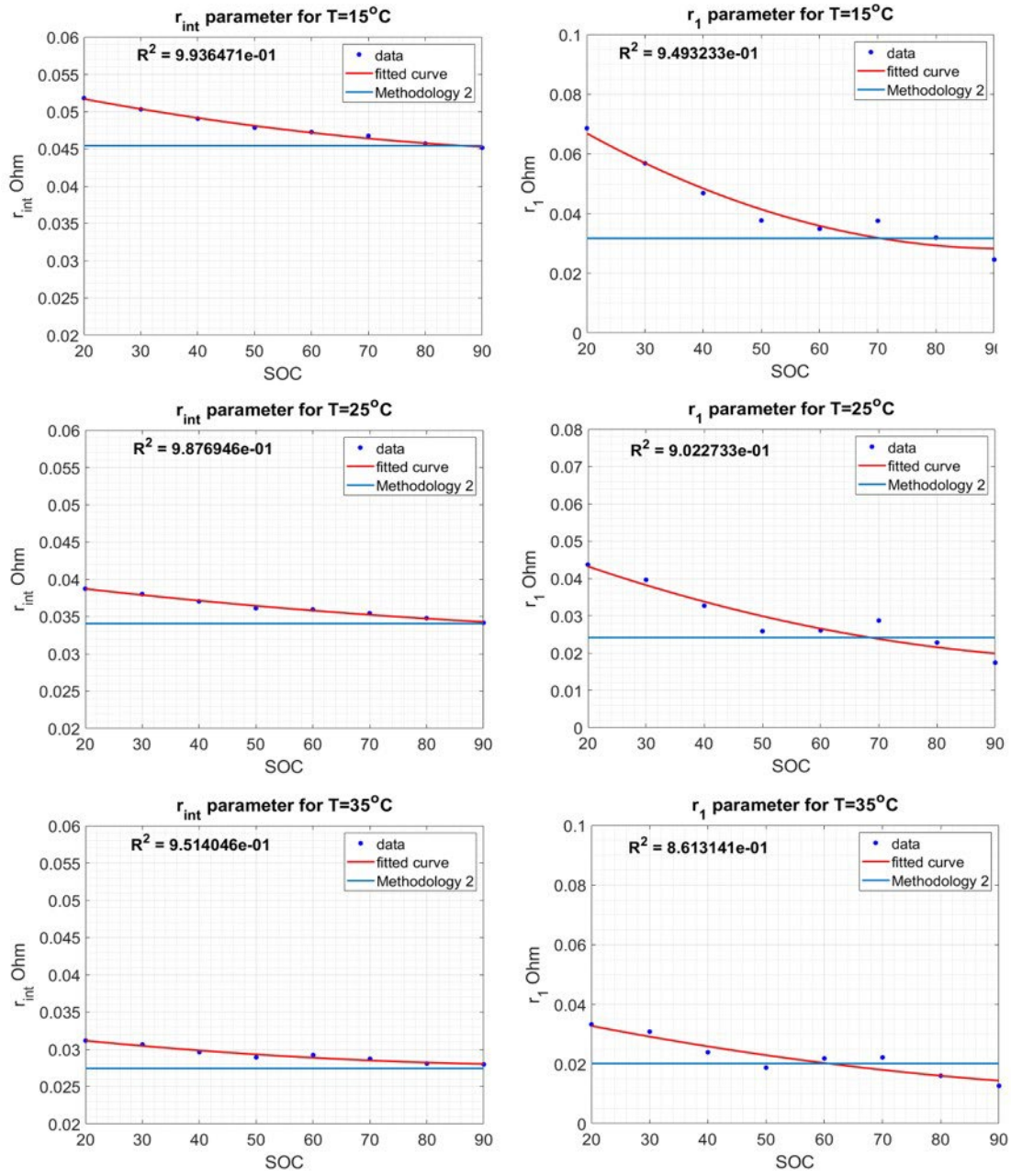



Figure 2.11. Proposed methodology SoC and ECM parameters correlation.

The measured terminal voltage during the dynamic test is shown in Figure 2.12. The terminal voltage estimated by methodology 2 and the proposed method for 90%, 50% and 30% SoC, along with measured voltage, are shown in Figure 2.13, Figure 2.14 and Figure 2.15, respectively, at T=35ºC.

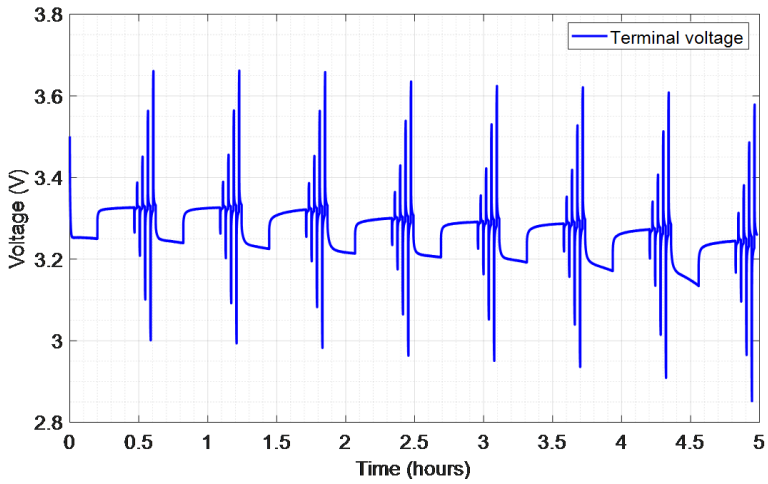



Figure 2.12. Battery terminal voltage obtained for complete load profile at 35°C.

The transients shown in Figure 2.13(a), Figure 2.14(a) and Figure 2.15(a) are for the discharge and charge pulses with an amplitude of 2C. The transients shown in Figure 2.13(b), Figure 2.14(b) and Figure 2.15(b) are for the 10% discharging period. The model considered for this analysis is comprised of a single $rc$ pair. From Figure 2.14(b) and Figure 2.15(b), it can be observed that the SOC-dependent model has better estimation of the terminal voltage during the discharge periods. Furthermore, for the 2C pulse transient, the SoC-depent model has shown to be more accurate in all scenarios.

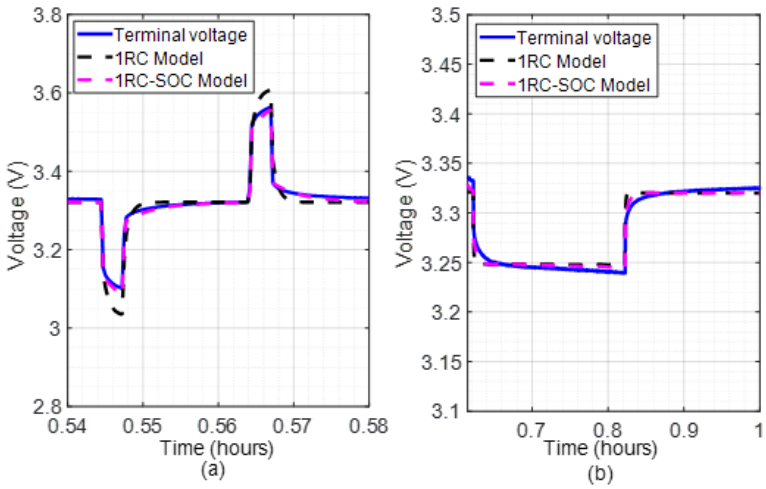



Figure 2.13. Terminal voltage estimation at 35°C and 90% SoC: (a) 2C-Pulse (b) Discharging period.

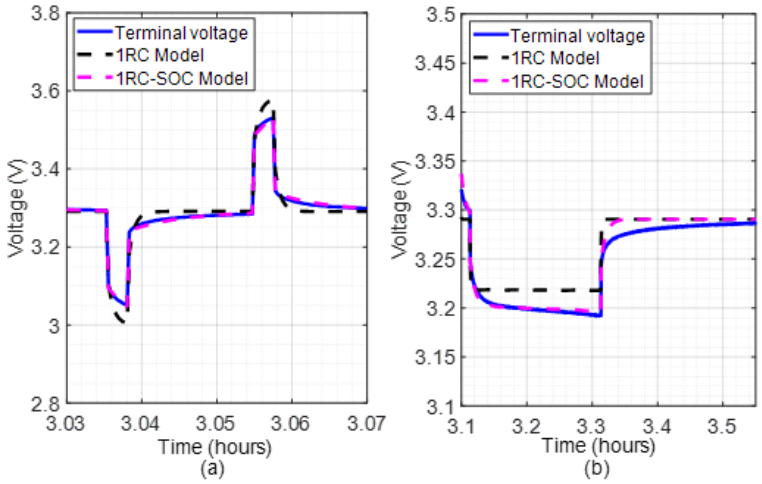



Figure 2.14. Terminal voltage estimation at 35°C and 50% SoC: (a) 2C-Pulse (b) Discharging period.

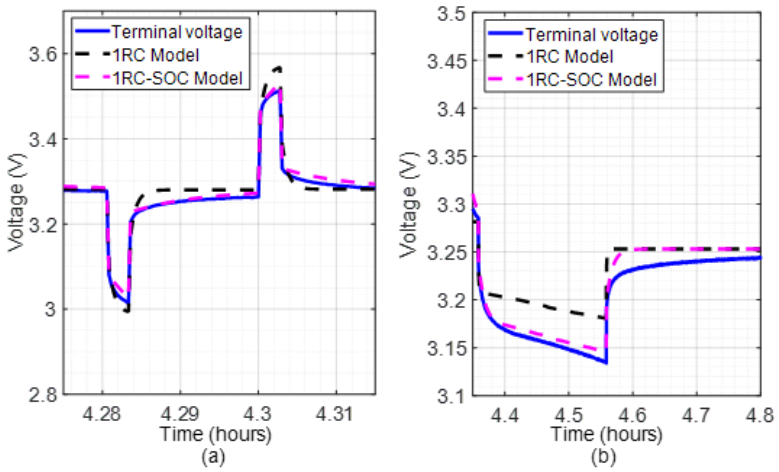



Figure 2.15. Terminal voltage estimation at 35°C and 30% SoC: (a) 2C-Pulse (b) Discharging period.

Finally, assuming the whole dataset, the root-mean-square error (RMSE) as the main metric is used to assess the accuracy of the model. This value needs to be as low as possible to estimate SoC and SoH accurately. Another comparison metric is the instantaneous peak error (PKE). The PKE, essentially, indicates the worst-case scenario terminal voltage estimation error obtained through the whole dataset. The PKE occurs

during the pulse train in the dynamic test.Table 2.2 summarizes the RMSE and PKE of the terminal voltage for the model obtained using methodology 2 and the proposed modification with SoC-dependent parameters. In addition to the results shown in Figure 2.13 through Figure 2.15, where only single $rc$ models were considered, quantitative results for models with 2 $rc$ pairs are also obtained and shown in Table 2.2.

In the best-case scenario, the RMSE obtained for the proposed SoC-dependent models are 8.3 mV (single $rc$) and 7.3 mV (double $rc$). This happens for the test with temperature T=35ºC. The addition of the $rc$ pair reduces the RMSE by 1 mV. The RMSE obtained for the proposed method is approximately 50% lower than that of the methodology 2 (17.6 mV, for single $rc$ and 14.4 mV for double $rc$).

Table 2.2. Lithium-ion Iron Phosphate Cell Model RMSE and PKE

| **Error** | **Model** | | | |
|---|---|---|---|---|
| | ***1RC*** | ***2RC*** | ***1RC-NL*** | ***2RC-NL*** |
| ***T=35ºC*** | | | | |
| RMSE | 17.6 mV | 14.4 mV | 8.3 mV | 7.3 mV |
| PKE | 109.7 mV | 96.7 mV | 57.5 mV | 57.5 mV |
| ***T=25ºC*** | | | | |
| RMSE | 23.3 mV | 18.8 mV | 9.9 mV | 8.4 mV |
| PKE | 148.7 mV | 132.7 mV | 86.3 mV | 84.7 mV |
| ***T=15ºC*** | | | | |
| RMSE | 35.5 mV | 30.3 mV | 15.5 mV | 13.1 mV |
| PKE | 228.3 mV | 219.9 mV | 133.7 mV | 134 mV |

It can be concluded that the inclusion of the SoC correlation in the ECM can greatly increase the overall accuracy of the model. The highest RMSE obtained for the proposed method occurs at T=15ºC with 15.5 mV (in case of single $rc$ model) and 13.1 mV (in case of double $rc$ model). Finally, the SoC-dependent models also reduce the PKE by a large margin (from 109.7 mV to 57.5 mV for the single $rc$ model). However, it is observed that further addition of the $rc$ pair does not decrease the PKE significantly, as when compared to the single $rc$ model (they are almost the same).

## 2.4 Accelerated degradation test

The LiFePO4 batteries considered in this dissertation have a lifetime that can last for years, which makes it challenging to obtain desired information regarding the degradation behavior of the battery within a reasonable timeframe [68], [69]. To circumvent this issue, accelerated ageing tests can be employed, where specific stress factors are imposed to the battery. Specifically, the main stress factor to achieve faster degradation for batteries is the temperature. Other commonly considered stress factors are SoC at which the battery is stored, SoC swing and pulse amplitude (C-Rate) [70].

In the following subsection, accelerated life tests for LiFePO4 batteries under frequency regulation mission profile is performed. Trend curves for capacity fade (degradation) under different stress factors, and specific battery parameter changes over time are obtained.

### 2.4.1 Load profile and degradation test setup

A load profile based on a frequency-regulation application of an energy storage system, presented in [71], is utilized. The profile is normalized in power and presented

over a 24-hour period. The dataset suggested in [71] is based on real data obtained over one year and provided by PJM Interconnection. A 24-hour standard deviation was used to measure the aggressiveness of the profile. Each profile was categorized into days with low, average, and high standard deviations. Based on the 24-hour profiles, 2-hour representative load profiles are obtained with low, average, and high standard deviation. As suggested by [71], a 24-hour profile is obtained by considering three 2-hour average profiles, one 2-hour high deviation profile, three 2-hour average profiles, one 2-hour high deviation profile, and four 2-hour average profiles. It is important to highlight that all profiles are energy neutral, which means that the SoC is retained back to its original value (assuming coulumbic efficiency near unity) after the two-hour cycle. The overall standard deviation of the profile obtained is 0.4. Figure 2.16 shows the implemented load profile for the battery degradation.

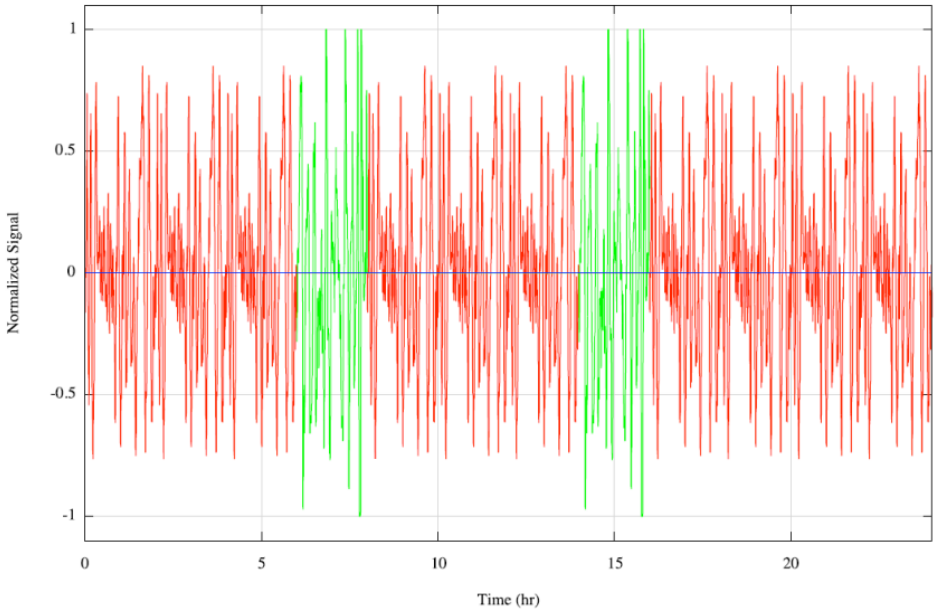



Figure 2.16. Degradation load profile as suggested.

To achieve accelerated aging of the LiFePO4 batteries, cycling tests are performed at high temperatures ($T_{max}$=43°C). Furthermore, the maximum C-rate selected is 1C. These temperature and C-rate values are chosen as per the manufacturer's specifications.

Besides temperature, SoC is also considered a stress factor. Since the load profile is energy neutral, the SoCs deviate around specific preset values. Three preset SoC values of 75%, 50%, and 25% are chosen. The batteries are soaked in a Yamato DVS602C drying oven at the selected temperature, while the Arbin LBT22023 battery testing unit is used to cycle the batteries with the chosen load profile. The batteries are soaked in a Yamato DVS602C drying oven at the selected temperature, while the Arbin LBT22023 battery testing unit is used to cycle the batteries with the chosen load profile. The battery test setup is shown in Figure 2.17.

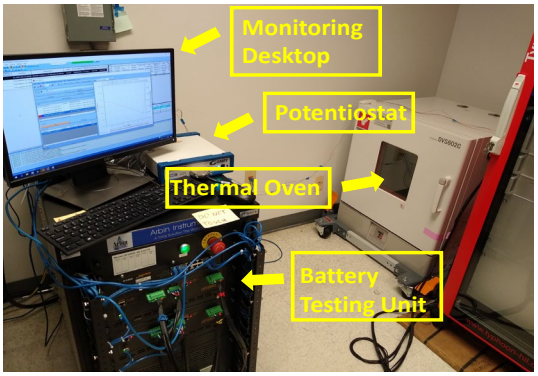



Figure 2.17. Battery test setup for degradation tests.

The list of batteries under test and stress factors can be summarized below:

- Battery 1: Aggressiveness: Standard deviation of 0.4, base SoC 75%, temperature 43 °C.

- Battery 2: Aggressiveness: Standard deviation of 0.4, base SoC 50%, temperature 43 ºC.
- Battery 3: Aggressiveness: Standard deviation of 0.4, base SoC 25%, temperature 43 ºC.

### 2.4.2 Accelerated degradation test results

After eight 24-hour cycling periods, a performance check is completed. The performance check comprises of capacity test and Electrochemical Impedance Spectroscopy (EIS) test, which is performed by the Gamry potentiostat/galvanostat, shown in Figure 2.17.

The capacity test is performed at ambient temperature (25ºC) to obtain a trend curve to describe the capacity fade under different stress factors. The obtained values are then utilized to estimate the remaining useful life of the battery.

The EIS tests are performed both at 43ºC and at ambient temperature. The EIS tests are performed to track the impedance changes of the battery after each degradation cycling period. Specifically, ECMs are designed based on the EIS results, from which the internal resistance of the battery is estimated. The internal resistance is of crucial importance since it determines the battery power capability and can be correlated to battery capacity fade [68], [70]. Within the scope of this dissertation, this impedance information is useful for designing circuit parameters of the BESS-MMC and, since the battery impedance is part of the system's plant, optimization of controller parameters.

### 2.4.2.1 Capacity fade results

The tests are performed during a period equivalent to 120 days (4 months). Figure 2.18 shows the capacity fade for the different batteries. Each horizontal division of Figure 2.18 is equivalent to 8 days.

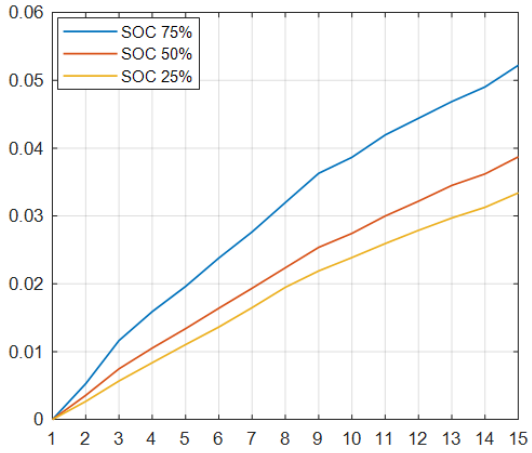



Figure 2.18. Capacity fade obtained for the batteries under test.

Similar to the findings presented in [72], batteries that are stored or operated at higher SoC levels degrade faster. This behavior is due to the relationship between electrode potential and the rate of parasitic side reactions. Since the battery has a higher voltage at higher SoCs, the parasitic reactions also increase, leading to faster degradation [73]. The maximum degradation obtained over the period under test is 5.3% for SoC = 75%, while the minimum occurs for SoC = 25% with 3.4%. Even though the batteries are under increased stress conditions, the degradation rate is considerably low because of the more realistic load profile. In [72], more aggressive profiles are considered, in which case the batteries are able to degrade at faster rates. However, the profile is based solely on charging and discharging pattern that does not necessarily follow a specific application. The capacity fade to determine the end of life (EOL) of

the battery is a design parameter. An arbitrarily chosen value, but commonly considered in the literature, is a capacity fade equivalent of 20% [72]. This EOL criterion is based on the criterion used in electric vehicle applications [74], [75].

#### 2.4.2.2 Internal resistance change

The internal resistance is obtained through the EIS dataset. After every eight days, Gamry Instruments Interface 1010E galvanostat performs an EIS test to obtain the frequency response of the bode plot. The galvanostat excites the battery by injecting an AC current, thus obtaining the battery voltage as an output. Furthermore, the galvanostat performs an AC frequency sweep. Thus, the battery impedance can be obtained across a predetermined frequency spectrum. In this test, the frequency range considered is from 10 kHz to 10 mHz. The amplitude of the galvanostat current is chosen as C/5, with the intent to avoid triggering non-linear behaviors of the battery [65].

Two-RC models are implemented within the Gamry Echem Analyst environment. The battery impedance parameters are obtained using simplex solvers based on the EIS dataset. The internal impedance increase is shown in Figure 2.19. Note that to compress the data, the increase is shown for every 32 days (i.e., the results are shown after four 8-day degradation tests). The battery internal resistance increase follows a similar pattern to that of the capacity fade. Therefore, the battery with the highest capacity fade also experiences the highest internal resistance increase (up to 11.5% after degradation of 5.3%). When considering an EOL of 20%, the internal resistance of the battery can increase up to 80% [70]. Table 2.3 compiles the actual values obtained for the internal resistance during the test.

The results obtained are for a single LiFePO4 battery cell. When considering a battery pack comprised of several series-connected cells, a comparable internal resistance increase occurs. More details regarding the use of the battery impedance information are presented in Chapter 3.

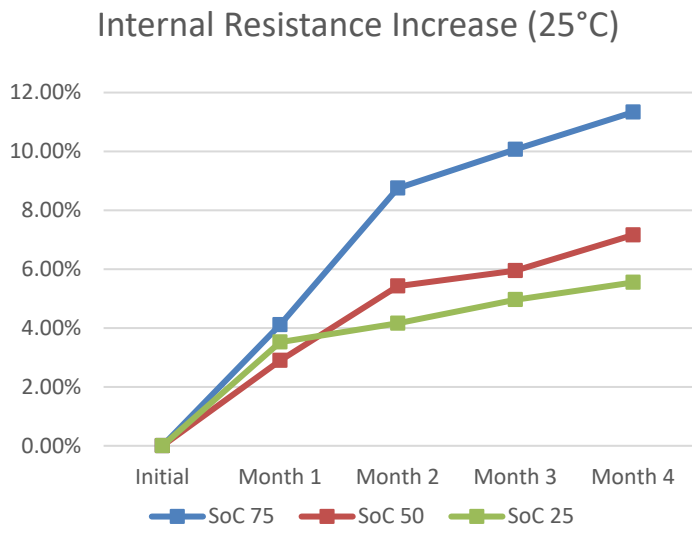



Figure 2.19. Internal resistance increase.

Table 2.3. Internal resistance value during degradation test

| | ***SoC 75*** | ***SoC 50*** | ***SoC 25*** |
|---|---|---|---|
| Initial | 30 mΩ | 30.0 mΩ | 29.7 mΩ |
| Month 1 | 31.2 mΩ | 30.9 mΩ | 30.7 mΩ |
| Month 2 | 34.0 mΩ | 32.5 mΩ | 32.0 mΩ |
| Month 3 | 37.4 mΩ | 34.5 mΩ | 33.6 mΩ |
| Month 4 | 41.6 mΩ | 36.9 mΩ | 35.5 mΩ |

## 2.5 Conclusions

This chapter proposes a new offline methodology to obtain SoC dependent battery parameters for grid energy storage applications. Using the subspace identification technique, the proposed method correlates the SoC and the battery parameters under different temperatures. The SoC-dependency is well described by a trend curve obtained by the polynomial regression. In the worst scenario, the fitness obtained is $R^2 = 0.86$, which indicates that the trend curve is within closed proximity of the calculated discrete values. Finally, the accuracy of the proposed method is validated by comparing it with the conventional model. In addition, the proposed method has been tested for single and double resistive-capacitive pairs-based battery models. Results have shown that the proposed model improves the accuracy of the terminal voltage estimation by approximately 50%. The proposed modeling could be used to design circuit parameters, controller gains and implement BMS algorithms (e.g., SoC and SoH) of BESS in grid energy storage applications. Finally, accelerated aging tests at high temperatures are performed to obtain the ECM parameter (internal resistance) change over the battery lifetime. The tests are performed with three battery cells at different SoC stress conditions, 75%, 50%, and 25%. Over a period of 4 months, it is obtained that the battery with higher SoC has degraded the most (5.3% capacity fade). During the same period, the internal resistance of the battery cell increased by almost 11% of its original value.

## 2.6 Publications

- J. M. L. Fonseca, G. Sambandam Kulothungan, K. Raj and K. Rajashekara, "A Novel State of Charge Dependent Equivalent Circuit Model Parameter Offline Estimation for Lithium-ion Batteries in Grid Energy Storage Applications," *2020 IEEE Industry Applications Society Annual Meeting*, 2020, pp. 1-8.

# 3. REDUCED CAPACITOR ENERGY REQUIREMENTS AND BATTERY BIDIRECTIONAL DC-DC CONVERTER CONTROL OF BESS-MMC

## 3.1 Introduction

Power Electronic Converters are the technology employed to interface BESS to the electric grid. Modular Multilevel Converters (MMCs) are becoming increasingly popular as a means to integrate low-voltage battery packs into higher voltage grids. However, one of the main disadvantages of the MMC as compared to other topologies, is that the MMC requires higher capacitance values. The reason is that each capacitor experiences current component oscillations at mainly grid frequency and its second harmonic [37]. These current components cause voltage oscillations that need to be maintained within certain limits for safety and operational purposes. The voltage ripple is commonly set to 10% of the DC voltage in each submodule [76]-[78]. To limit the ripple to this design value, a capacitor energy requirement of 30-40 kJ/MVA is commonly considered for the design of the capacitor in each submodule [79]. However, this guideline was envisaged for HVDC-MMC applications. Many papers related to the integration of batteries with this topology utilize the same energy requirement [76], [80], [81], while other researchers do not mention whether any guideline was utilized or if the sizing was chosen empirically [82]-[84], [85].

The expected operation of the MMC impacts the capacitor energy requirements. In [86], the energy requirements are calculated for different operating power factors. It is shown that the highest capacitor energy requirements occur when the MMC provides

reactive power compensation. Therefore, it can be hypothesized that a similar situation might occur when considering the BESS-MMC. However, as an extension of [86], additional operational requirements for BESS-MMC are the prolonged power transfer between the different MMC phases and arms. The phase power transfer and arm power transfer are used to perform per-phase power balancing and per-phase/arm SoC balancing [83]-[85], [87]. In both scenarios, the power transfer occurs through the additional degree of freedom of the MMC, i.e., the circulating current. The phase power exchange is commonly performed with a DC circulating current, while the arm power transfer is achieved through AC (at grid frequency) circulating currents [87]. Therefore, different from the analysis presented in [86], the currents that flow within the MMC are not limited to the ones related to the grid operation but also include the DC and AC circulating currents. This scenario results in different capacitor energy requirements for the BESS-MMC.

The capacitor energy requirements are also closely related to the current that flows through the DC-link. However, there are different possibilities for battery connection to a module, as shown in Figure 3.1. Batteries can be directly connected to the submodule with or without a DC-link capacitor or through bidirectional DC-DC converter (BDC) [88]. Connection without a DC-link capacitor (Figure 3.1(a)) results in low and high-frequency battery current ripple, potentially leading to premature aging [88], [89]. If the batteries are connected with DC-link capacitors (Figure 3.1(b)), the current that flows into the submodule is shared between the capacitor and battery according to their impedances. This scenario might lead to different capacitor energy requirements, as the battery impedance is dependent on many factors such as SoC, SoH,

and chemistry, as described in Chapter 2 and [90], [91]. Finally, with an interfacing BDC (Figure 3.1(c)), more flexibility can be obtained as it is possible to ensure that

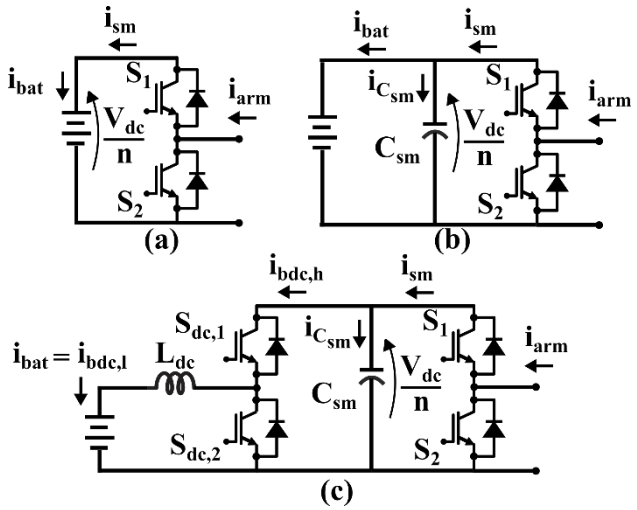



Figure 3.1. Different types of battery connection to the MMC submodule: (a) direct connection as DC-link; (b) connection in parallel with capacitor; (c) connection with bidirectional converter with L filter.

battery current ripple is minimal and only the capacitor experiences current ripple, or increase the battery current ripple and possibly reduce the ripple flowing into the capacitor. To ensure no impact on the battery lifetime, the first scenario is considered in this chapter.

When connecting energy storage elements to the MMC, there are mainly two ways to control the DC-link voltages in each module. The first one can be performed using an outer average voltage loop of the grid current control. This is virtually the same way that an MMC without energy storage would be controlled. Thus, energy control loops may be required to suppress energy deviation amongst arms and phases of the MMC. Further, sorting algorithms may need to be utilized to balance capacitor voltages within each arm. In [76], such a strategy is employed for a single-phase MMC. The energy storage elements are controlled directly through a current-control strategy of the

interfacing DC-DC converter. The current reference is calculated based on the BESS power, the number of modules, and the energy storage voltage. This strategy requires bidirectional communication between modules and the main control of the MMC.

Another approach, which has been described in [77], [78], is to control the module's voltage through the interfacing DC-DC converter using an outer voltage loop. The voltage loop controller outputs the battery current reference for a high gain crossover (GC) frequency inner current loop. With this strategy, the battery power is not regulated through the module. Instead, it is indirectly selected based on the power demand of the grid. This can cause a few issues for the operation of the BESS-MMC. First, if the outer voltage loop is much slower than the grid current control, large load steps may cause the DC-link voltages to reach unsafe operation regions. This can be alleviated by having feed-forward terms (requiring communication between MMC and module control) for the battery-current control since they have a much higher GC frequency. However, coordinating the GC frequency of the module's voltage loop and the MMC output power loop (adding a transient to the reference of the current loop) can be an alternative to the increased communication requirements. Because of the reduced requirements, the outer-voltage loop strategy is utilized in this dissertation.

### 3.1.1 Bidirectional converter voltage loop

An issue caused by the voltage loop controller strategy is due to the DC-link voltage feedback. The BDC controls the submodule's DC-link voltage through a dual-loop structure with an inner current and outer voltage loop. During normal operation of the MMC, the DC-link voltages contain significant 60 and 120 Hz components [92]. The low-frequency ripple in the sensed DC-link needs to be suppressed for the reference

current of the inner loop, as it can lead the inner current loop to inadvertently track the reference oscillation and cause a low-frequency battery current ripple to appear. A PI controller designed at low frequencies can be utilized to damp the oscillations. However, the amount of damping is limited or severely affects the gain crossover frequency and phase margin of the voltage loop. Cascading finite impulse response (FIR) and infinite impulse response (IIR) filters with the voltage PI controller is an option to dampen the incoming low-frequency ripple [83], [84], [93]-[97]. With the disadvantage of increased microcontroller memory requirements, FIR filters such as the moving average (MAF) filter and FIR comb filter can be potentially used for this task [96], [97]. However, IIR filters such as a Butterworth low pass filter (LPF) and notch filter (NF) have more design flexibility. In [83],[93], an LPF is added in series with the PI controller or directly at the feedback of the voltage sensing. The LPF, however, adds significant phase lag to the system, requiring the voltage loop to have low gain crossover frequencies to obtain a high phase margin. In [84], [94], and [95], notch filters (NF) are utilized at grid frequency and second harmonic. In [84] and [95], notch filters at 60 and 120 Hz are considered cascaded with the voltage loop PI controller. However, design guidelines are not discussed. In [94], a novel BDC interface is proposed, where additional components such as half-bridge, inductor, and buffer capacitor are considered. Furthermore, an NF at grid frequency is designed based on the quality factor. However, in terms of gain and phase decay, the impact on the voltage loop is not assessed. The attenuation that needs to be provided by the NF is intrinsically related to the voltage variation experienced by the DC-link capacitor, which depends on the capacitor sizing. Improving the performance of the voltage loop relies on firstly determining the capacitor voltage

variation, followed by analyzing the NF design requirements and their impact on the voltage loop performance in terms of gain and phase margin.

In [85], the BESS-MMC operates with phase power exchange and BDC controllers designed with NF at 60 and 120 Hz. Neither the NF design requirement nor the capacitor sizing is discussed. This chapter additionally presents systematic design considerations for digital controllers in BESS-MMC, alongside the impact of BESS-MMC operation on the capacitor energy requirements. Therefore, the main contributions of this chapter include the following:

1) Identifying that capacitor energy requirements are different for systems with batteries coupled to DC-link directly and systems with batteries connected through a DC-DC converter.
2) The required attenuation that needs to be provided by the digital controller of BDC at different frequencies is calculated to minimize battery current ripple.
3) The capacitor energy requirements while minimizing the battery current ripple are estimated assuming the operation of BESS-MMC injecting active and reactive power, i.e., as an Energy Storage – Static Compensator (ES-STATCOM [98], [99]) with: i) Grid currents only; ii) grid currents and phase power transfer; iii) grid currents and arm power transfer.
4) The capacitor energy requirement is independent of power, voltage level, and number of submodules. Further, the analysis can be reutilized to obtain requirements for any ratio of battery power to MMC rated power.

This chapter is organized as follows: Section 3.2 briefly discusses the different types of battery connections and the reason for using BDC to interface battery and

MMC. Sections 3.3 and 3.4 concisely show the modeling of the MMC and BDC structure under study. Section 3.5 shows the design considerations for the controllers of BESS-MMC bidirectional converters, considering both PI controllers and NF, emphasizing their impact on the loop gain and phase margin. Section 3.6 discusses the capacitor energy requirements for the operation of BESS-MMC, assuming power exchange with the grid, between phases, and between arms. Finally, the control and study are validated on a Typhoon-HIL platform with embedded controllers in Section 3.7. The conclusions are drawn in Section 3.8.

### 3.2 Connection of batteries to MMC

As discussed in the previous subsection and shown in Figure 3.1, there are different battery connection possibilities for the MMC-BESS. Each connection leads to different types of current and voltage ripple in the battery, causing the battery to have unnecessary charge and discharge cycles [88]. The most common approaches for connecting the batteries are connecting a battery in parallel to a capacitor or through a BDC, shown in Figure 3.1(b) and Figure 3.1(c), respectively. The first option splits the SM current between battery and capacitor. Accordingly, the capacitor current is

$$i_{C_{sm}} = \sum_{\beta=-\infty}^{\infty} i_{sm,\beta\omega} \left( \frac{Z_{bat,\beta\omega}}{Z_{bat,\beta\omega} + Z_{C_{sm},\beta\omega}} \right), \tag{3.1}$$

where $i_{sm}$ is the current flowing into the SM, $\beta$ is an integer, $\omega$ is the grid frequency, and $Z$ represents impedance. Equation (6) implies that a capacitor with a much lower impedance than the battery at a specific frequency will experience greater power and energy ripple at that particular frequency.

By including the BDC, the battery voltage level can be boosted to the required nominal value of the DC-link voltage while also controlling the currents that flow into the battery. The low-frequency battery ripple is suppressed by having high-bandwidth current control, thus effectively increasing the impedance of the battery-BDC and causing the current at these frequencies to flow only through the capacitor. This scenario also hinders the impact of the battery impedance on the current ripple by ensuring that controllers consider the battery impedance variation in their design. Given the advantages mentioned earlier, the connection with BDC is chosen for this dissertation. Modeling and control design of the BDC are presented in Section 3.4 and Section 3.5 .

### 3.3 BESS-MMC control

In Chapter 1, the dynamic equations that govern the grid and circulating currents are defined (Equations (1.8) and (1.9), respectively). In (1.9), ignoring the grid-voltage disturbance and assuming $u_{l,k} - u_{u,k} = 2v_k$, the transfer function that relates grid currents and the converter voltage is

$$\frac{i_{g,k}}{v_k}(s) = \frac{1}{s\left(\frac{L_{arm}}{2} + L_T\right) + \left(\frac{R_{arm}}{2} + R_T\right)}. \tag{3.2}$$

The grid current control strategy is employed in the synchronously rotating reference frame. As such, additional cross-coupling elements are present that need to be considered in the control structure. Figure 3.2(a) shows the grid current control strategy utilized in this chapter. An outer power loop is commonly employed to generate the grid current references.

Similarly, for the circulating current equation presented in (1.9), by defining $-u_{l,k} - u_{u,k} = 2v_{circ,k}$. The $v_{dc}$ disturbance is ignored, and the transfer function that relates the circulating current and its related voltage is

$$\frac{i_{circ,k}}{v_{circ,k}}(s) = \frac{1}{sL_{arm} + R_{arm}}. \tag{3.3}$$

Given the 120 Hz oscillations in the DC-link voltage, the circulating current control needs to suppress the oscillating components of the circulating current, thus decreasing power losses. The control loop is designed with high bandwidth with the aid of a PI controller [100]. Figure 3.2(b) shows the per-phase circulating current control.

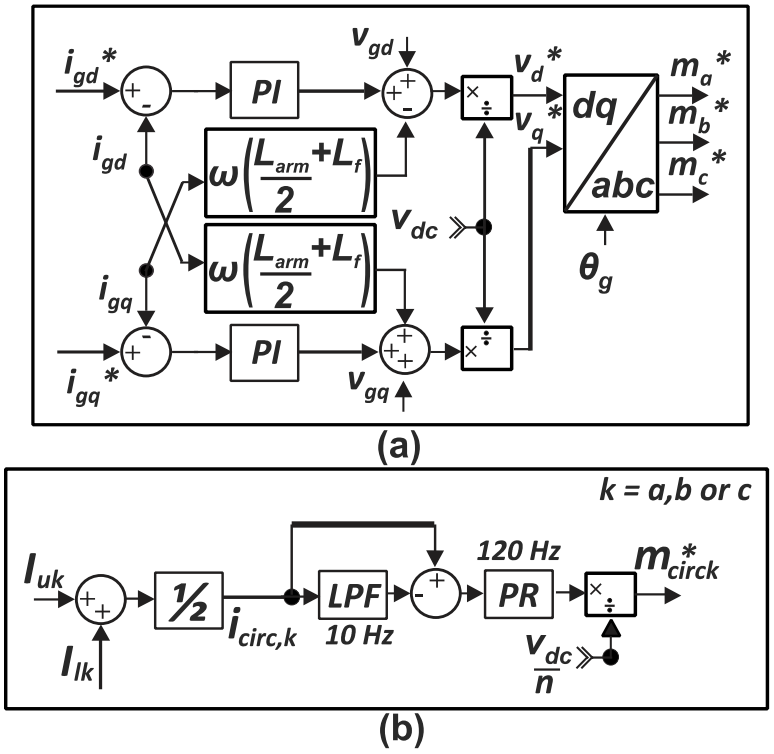



Figure 3.2. MMC side current control.(a) Grid current;(b) Circulating current..

Finally, adding the $v_{dc}$ disturbance, the modulating signals for the upper and lower modules are

$$\begin{cases} m^*_{u,k} = -m^*_k + m^*_{circ,k} + \dfrac{1}{2} \\ m^*_{l,k} = m^*_k + m^*_{circ,k} + \dfrac{1}{2} \end{cases}, \tag{3.4}$$

where $m^*_k$ and $m^*_{circ,k}$, are the normalized modulating signals related to the grid current control and circulating current control, respectively.

### 3.4 Bidirectional converter modeling and control

The operation stages of the interfacing synchronous boost converter are shown in Figure 3.3.

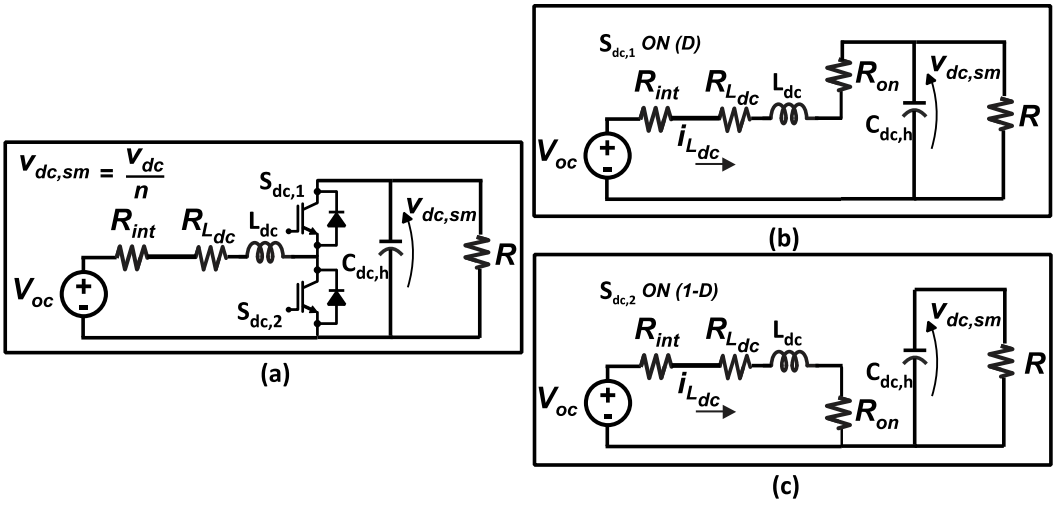



Figure 3.3. (a) Bidirectional converter; (b) Operation stage ($S_{dc,1}$ ON); (c) Operation stage ($S_{dc,2}$ON).

Assuming continuous conduction mode, small-signal modeling through state-space averaging [101] is utilized to obtain the converter dynamics. The obtained transfer functions are

$$\begin{bmatrix} G_{id}(s) \\ G_{vd}(s) \end{bmatrix} = \begin{bmatrix} \dfrac{\hat{i}_{L_{dc}}}{d}(s) \\ \dfrac{\hat{v}_{dc,sm}}{d}(s) \end{bmatrix} = \frac{\begin{bmatrix} \dfrac{-\overline{v}_{dc,sm}}{L_{dc}}\left(s + \dfrac{2}{C_{dc,h}}\left(\dfrac{P}{\overline{v}_{dc,sm}^2}\right)\right) \\ \dfrac{P}{\overline{v}_{dc,sm}DC_{dc,h}}\left(s + \dfrac{1}{L_{dc}}\left(\dfrac{-D^2\overline{v}_{dc,sm}^2}{P} + R_T\right)\right) \end{bmatrix}}{s^2 + s\left(\dfrac{1}{RC_{dc,h}} + \dfrac{R_T}{L_{dc}}\right) + \dfrac{1}{L_{dc}C_{dc,h}}\left(\dfrac{R_T}{R} + D^2\right)}, \tag{3.5}$$

where the hat superscript indicates linearized variables and the ones with bar superscript indicate average values. Note that D is related to the duty cycle of the top switch. Furthermore, $P = \overline{v}^2_{dc,sm}/R$ and is equal to the submodule power. Finally, $R_T$ is defined as the sum of the internal resistance of the battery, $R_{int}$ (discussed in Chapter 2), the inductor resistance, $R_{Ldc}$, and the switch drain-source resistance $R_{(ds)on}$.

A dual-loop control strategy is employed, in which an outer-loop voltage controller provides the current reference for the inner-loop current controller. The transfer function that relates the voltage and the inductor current is

$$G_{vi}(s) = \frac{\hat{v}_{C_{dc,h}}}{\hat{i}_{L_{dc}}}(s) = \frac{-PL_{dc}}{\overline{v}^2_{c_{dc,h}}DC_{dc,h}}\left(\frac{s + \dfrac{1}{L_{dc}}\left(\dfrac{-D^2\overline{v}^2_{c_{dc,h}}}{P} + R_T\right)}{s + \dfrac{2}{C_{dc,h}}\left(\dfrac{P}{\overline{v}^2_{c_{dc,h}}}\right)}\right). \tag{3.6}$$

Figure 3.4 shows the simplified linearized system (not accounting for analog filters or transport delay). Besides the feedforward related to the duty-cycle, a feedforward for the inductor current can also be included. For the BESS-MMC under study, the feedforward proposed is calculated based on the AC power ($P_{BESS}$), the total

number of submodules ($n$), the submodule voltage ($\bar{v}_{dc,sm}$) and the duty-cycle of the buck/boost converter.

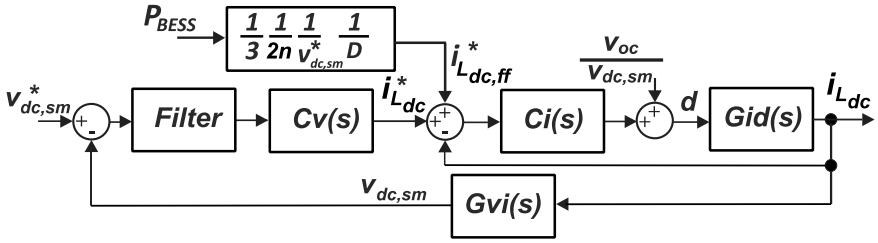



Figure 3.4. Simplified linearized system representation without analog filters and transport delay.

The feed-forward is crucial as it allows faster dynamics for load steps. As such, the submodule's voltage transient (overshoot and settling times) can be significantly reduced. However, it must be highlighted that this requires communication between the individual module's control and the overall BESS power. Therefore, this can potentially decrease the reliability of the BESS.

### 3.5 BDC Controller and Filter Design Procedure

Both compensators $C_i(s)$ and $C_v$(s) represent PI controllers. The main considerations for designing the voltage and current loop controller are discussed in the next subsections.

#### 3.5.1 PI Controller Design of Current loop

While designing the inner-loop current controller, the following remarks apply:

- If the feedforward component is not present, the current controller's performance relies on how fast it tracks the reference provided by the voltage loop. Thus, the GC frequency requirement can be simply selected to be much higher (at least 5-10 times) than that of the voltage loop. However, if the

feedforward component is considered, the loop GC frequency should be greater than the power loop frequency. This design allows the module's current control to quickly match the MMC side load demand with minimal impact on the DC-link voltage.

- The current-control performance is subject to the 60 and 120 Hz voltage disturbances caused by the MMC operation. This may lead to low-frequency oscillations in the battery current. In order to significantly reject these disturbances, the current control should have a GC frequency much greater than 60 and 120 Hz. Empirical results have shown that good performance can be achieved by selecting the GC frequency to be 10-20 times higher than the oscillating component to be suppressed. Note that this requirement can be reduced if the feedforward term $v_{oc}/v_{dc,sm}$is added at the output of the current controller [83].

### 3.5.2 PI Controller Design of Voltage loop

The outer loop voltage controller can be designed to guarantee that the loop has a GC frequency less than a fifth to a tenth of that of the inner current loop, thus guaranteeing decoupled operation [102]. Further, if no feedforward term is considered for the current reference, the GC frequency for the voltage loop needs to be at least 5-10 times faster than the grid power loop. Thus, significant transient in the DC-link voltage is avoided. In [103], the time constant of the power loop is considered to be between 5ms-500ms. Assuming a first-order system characteristic for the power loop, this leads to a required voltage loop GC frequency variation from 10-20 to 1000-2000 rad/s. In addition to the decoupling requirements of the loops, the voltage controller

must suppress the DC-link voltage ripple, ensuring no ripple in the current reference input, $i_{Ldc}^{*}$. To achieve this requirement, both a PI controller and PI+NF are considered.

#### 3.5.2.1 Required voltage attenuation

According to [76]-[78], a 10% voltage variation around the nominal value is expected for the operation of the MMC. Enough attenuation must be provided between the voltage feedback and the current reference generation, guaranteeing that the battery current ripple is greatly limited with respect to the battery current rated value. The required attenuation changes according to the amplitude of the voltage oscillation at a particular frequency and can be calculated as

$$G_{att,\omega} = \frac{\alpha_{Curr-ripple,\omega} \times i_{bat,rated}}{\alpha_{Volt-ripple,\omega} \times v_{dc,sm}}, \tag{3.7}$$

where $\alpha_{ripple}$ indicates the percent of voltage and current with respect to rated DC link voltage and rated battery current. Based on the capacitor energy, and knowing oscillations are mainly at 60 and 120 Hz, $\alpha_{Volt-ripple}$ can be approximated to

$$\alpha_{Volt-ripple,\omega} = \frac{\Delta e_{\omega}}{CV_{C_{sm}}}, \tag{3.8}$$

where $\Delta e_{\omega}$ is the energy ripple at frequency $\omega$ and can be obtained as shown in Section 3.6. For simplification purposes, it is possible to consider a scenario where mainly grid frequency is present. Therefore, defining $\alpha_{volt-ripple}$ to be 10% of the rated DC-link voltage will lead to the highest attenuation requirement [104]. The same requirement can be considered for the remaining frequency components (e.g., 120 Hz).

The attenuation found through (3.7) can be adjusted accordingly to the design specifications. As the voltage ripple considered decreases, the attenuation requirements are also reduced.

#### 3.5.2.2 PI controller design

The PI controller transfer function and the gain of the transfer function as a function of the frequency are described as

$$PI(s) = K_p \frac{(s + T_i)}{s} \tag{3.9}$$

and

$$\left|PI\right|(\omega) = K_p \frac{\sqrt{\omega^2 + T_i^2}}{\omega}. \tag{3.10}$$

The zero location, determined by the parameter $T_i$, can be placed at a frequency below the grid frequency to obtain maximum attenuation of oscillations at grid frequency and its second harmonic [105]. The attenuation at frequencies beyond the zero location is set by the gain $K_p$, which should be below unity to ensure damped oscillations.

Designing the voltage loop PI controller to attenuate the capacitor voltage oscillations may cause the loop dynamics to be poor in terms of gain crossover frequency and phase margin. It is more advantageous to design the voltage loop to achieve good performance and verify whether the obtained PI controller provides enough damping afterward. If the damping provided is insufficient, the loop can be redesigned iteratively until both gain crossover frequency, phase margin, and oscillation

damping are satisfactory. However, meeting the three design specifications might be challenging, in which case, the addition of the NF can be beneficial.

### 3.5.2.2 Notch filter design

The NF can be designed to attenuate the most relevant oscillating components (60 and 120 Hz). The continuous time-domain transfer function of the notch-filter is

$$G_{notch}(s) = \frac{s^2 + 2D_z\omega_f s + {\omega_f}^2}{s^2 + 2D_p\omega_f s + {\omega_f}^2}, \tag{3.11}$$

where $\omega_f$ is the notch-frequency, $D_z$ is the zero-damping coefficient, and $D_p$ is the pole damping coefficient. The latter two can be designed as a function of $a_\Delta$, $a_{\omega f}$ and $\Delta\omega_f$, as shown in Figure 3.5. For this application, $\Delta\omega_f$ can be chosen to be a function of the grid frequency. Therefore, it is assumed that the grid-frequency variation is around $\pm 1.2$ to $\pm 2.4$ Hz. Further, following the guidelines presented in [106], it is assumed that $a_{\omega f,dB} = 2a_{\Delta,dB}$. Therefore $a_{\omega f}$ is chosen to provide minimum attenuation considering the expected grid variation.

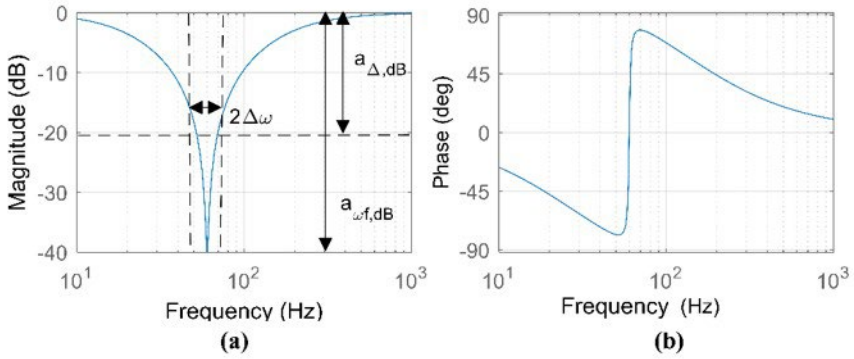



Figure 3.5. Notch filter characteristics. (a) Magnitude;(b) Phase.

The notch filters add phase lag and change the gain at frequencies around the notch frequencies. Assuming a combination of h cascaded NF structures, the gain and frequency responses are

$$|NF|(\omega)=\prod_{h=1}^{j}\frac{\sqrt{\left(-\omega^2+{\omega_{fh}}^2\right)^2+\left(2D_{zh}\omega_{fh}\omega\right)^2}}{\sqrt{\left(-\omega^2+{\omega_{fh}}^2\right)^2+\left(2D_{ph}\omega_{ph}\omega\right)^2}} \tag{3.12}$$

and

$$\angle NF(\omega)=\sum_{h=1}^{j}\left(\tan^{-1}\left(\frac{\omega+\omega_{fh}\sqrt{1-{D_{zh}}^2}}{\omega_{fh}D_{zh}}\right)+\tan^{-1}\left(\frac{\omega-\omega_{fh}\sqrt{1-{D_{zh}}^2}}{\omega_{fh}D_{zh}}\right)\right)+ \sum_{h=1}^{j}\left(-\tan^{-1}\left(\frac{\omega+\omega_{fh}\sqrt{1-{D_{ph}}^2}}{\omega_{fh}D_{ph}}\right)-\tan^{-1}\left(\frac{\omega-\omega_{fh}\sqrt{1-{D_{ph}}^2}}{\omega_{fh}D_{ph}}\right)\right), \tag{3.13}$$

where the subscript $\omega_{fh}$, $D_{zh}$, and $D_{ph}$ are the parameters of the NF designed at the h$^{th}$ multiple of the grid frequency. Table 3.1 shows the gain and the phase lag of several NFs combinations designed at 60 Hz. Note that all filters also include a cascaded NF at 120 Hz with $a_\Delta=-20$dB and $\Delta\omega_f=2.4\pi$ rad/sec.

From Table 3.1, it can be observed that the designed filters with attenuation of -20dB (NF1 and NF3) have minimal gain attenuation for frequencies up to 20 Hz. However, a phase lag up to -17.98° is introduced (NF3). As such, when designing a PI controller, the influence of the filters' gain can be neglected. At the same time, for higher GC frequency systems (12 and 20 Hz), the phase margin drops significantly. Therefore, if a certain phase margin constraint has to be met, the phase lag introduced by the NFs must be added to the design.

Table 3.1 Notch Filter gains and phases

| **Notch Filter** | **Gain and Phase at different frequencies** | | |
|---|---|---|---|
| | ***5 Hz*** | ***12 Hz*** | ***20 Hz*** |
| NF1<br>$a_\Delta = -20\text{dB}$<br>$\Delta\omega_f = 2.4\pi$ rad/sec | -0.005 dB<br>-2.34° | -0.031 dB<br>-5.78° | -0.1 dB<br>-10.24° |
| NF2<br>$a_\Delta = -40\text{dB}$<br>$\Delta\omega_f = 2.4\pi$ rad/sec | -0.448 dB<br>-18.7° | -2.24 dB<br>-40.52° | -5.03 dB<br>-57.81° |
| NF3<br>$a_\Delta = -20\text{dB}$<br>$\Delta\omega_f = 4.8\pi$ rad/sec | -0.019 dB<br>-4.15° | -0.11 dB<br>-10.24° | -0.358 dB<br>-17.98° |
| NF4<br>$a_\Delta = -40\text{dB}$<br>$\Delta\omega_f = 4.8\pi$ rad/sec | -1.528 dB<br>-33.46° | -5.588 dB<br>-59.42° | -9.767 dB<br>-72.95° |

When increasing the desired attenuation to -40dB (NF2 and NF4), a significant phase lag is introduced even at lower frequencies. Further, the effect of the filter gain also needs to be considered in the controller design, especially at higher frequencies. This greatly increases the complexity of the PI design. As such, these filters should be avoided for higher GC frequency systems, as they lead to very poor performance. This is the case since the maximum achievable phase margin is greatly reduced. This scenario is possible if the power loop GC frequency is too high and the feedforward component is not present.

Note that given the boost characteristic of the DC-DC converter, a right-hand plane (RHP) zero is added. The addition of the NF combination (at 60 and 120 Hz) leads to significant phase decay around 60-120 Hz. Therefore, designing a controller for GC frequencies near/greater than 60 Hz can be almost impossible unless either the pole or RHP zero are located at much higher frequencies. Finally, details regarding the digital implementation of the NF are discussed in [106].

### 3.6 Capacitor energy requirements for the operation of BESS-MMC

The capacitor energy requirement analysis assumes the presence of a BDC between the DC-link capacitor and the battery, as shown in Figure 3.1(c). In accordance with Section 3.5, the BDC is controlled so that the battery current ripple is limited, leading to the submodule current ($i_{sm}$) ripple to flow entirely through the capacitor.

The primary purpose of the MMC is to synthesize sinusoidal voltages at grid frequency. The average switching functions that dictate how $S_1$ and $S_2$ switch are originally defined in (3.4). However, under the assumption that the modulating signal related to the circulating current is much smaller than the remaining components ($|m_{circ,j}| \ll |0.5 \pm m_j|$), (3.4) is rewritten for the upper and lower arms as

$$s_{j,upper}(t) = \frac{1}{2} - \frac{m}{2}\sin\left(\omega t + \theta_v\right) \tag{3.14}$$

and

$$s_{j,lower}(t) = \frac{1}{2} + \frac{m}{2}\sin\left(\omega t + \theta_v\right), \tag{3.15}$$

where $j$ indicates the converter phase, m is the modulating index related to AC grid operation, and $\theta_v$ is the phase angle of the synthesized voltage. Equations (3.14) and

(3.15) imply symmetrical operation of submodules within the same arm. The submodule and capacitor currents are

$$i_{sm,upper}(t) = s_{j,upper}(t)\, i_{arm}(t) \tag{3.16}$$

and

$$i_{C_{sm}}(t) = \tilde{i}_{sm,upper}(t). \tag{3.17}$$

In (3.17), the superscript ~ indicates oscillating components. These oscillating components in the SM's capacitor cause a power ripple, which leads to energy ripple, and voltage variations. In most scenarios, the voltage ripple is designed to be limited to 10%. Under this assumption, the voltage ripple effect on the power ripple is limited, and the power ripple in each module is

$$\Delta p_{C_{sm}}(t) = V_{C_{sm}}\, i_{C_{sm}}(t). \tag{3.18}$$

The energy ripple for the whole arm is defined as

$$\Delta e_{upper}(t) = V_{dc} \int i_{C_{sm}}(t) dt. \tag{3.19}$$

The overall energy for the arm is

$$E_{upper}(t) = E_{nom} + \Delta e_{upper}(t), \tag{3.20}$$

where $\Delta e_{upper}(t)$ is the energy ripple around the nominal energy, which is defined as

$$E_{nom} = \frac{nC_{sm}V_{C_{sm}}^2}{2}. \tag{3.21}$$

Note that $\Delta e_{upper}(t)$ takes positive and negative values. As such, the minimum and maximum values $E_{upper}(t)$ can assume are

$$E_{upper,\max} = E_{nom} + \max\left(\Delta e_{upper}(t)\right) \tag{3.22}$$

and

$$E_{upper,\min} = E_{nom} - \left|\min\left(\Delta e_{upper}(t)\right)\right|. \tag{3.23}$$

During the BESS-MMC operation, it must be ensured that the voltage does not go beyond specific limits for protection and control purposes. The limits are

$$\left(1-k\right)V_{C_{sm}} \le V_{C_{sm}} \le \left(1+k\right)V_{C_{sm}}, \tag{3.24}$$

where k can theoretically vary between 0 to 1. Selecting k to be 0.1 leads to a maximum voltage of $1.1V_{C_{sm}}$ and a minimum voltage of $0.9V_{C_{sm}}$ (max. 10% voltage ripple). Note, however, that (3.18) may not hold for significant ripple amplitudes. According to the specified minimum and maximum voltage limits selected, the corresponding minimum and maximum values for the energy in the arm are

$$\frac{nC_{sm}(1-k)^2 V_{C_{sm}}^2}{2} \le E_{upper}(t) \le \frac{nC_{sm}(1+k)^2 V_{C_{sm}}^2}{2}. \tag{3.25}$$

The variable $E_{upper,max}$ can be, in the worst case, equal to the right term of inequality (3.25), while $E_{upper,min}$ be, in the worst case, equal to the left term of inequality (3.25). By substituting (3.20) in (3.22) and (3.23) and assuming the previously discussed worst condition of $E_{upper,min}$, and $E_{upper,max}$, expressions that

relate the maximum and minimum values of energy ripple, $k$, capacitor voltage, $n$, and capacitance can be obtained. The expressions are

$$(2k+k^2)\frac{nC_{sm}V_{C_{sm}}^2}{2} \geq \max\left(\Delta e_{upper}(t)\right) \tag{3.26}$$

and

$$(2k-k^2)\frac{nC_{sm}V_{C_{sm}}^2}{2} \geq \left|\min\left(\Delta e_{upper}(t)\right)\right|. \tag{3.27}$$

Equations (3.26) and (3.27) lead to the minimum capacitance requirements

$$C_{sm} \geq \frac{2\max\left(\Delta e_{upper}(t)\right)}{nV_{C_{sm}}^2\left(2k+k^2\right)} \tag{3.28}$$

and

$$C_{sm} \geq \frac{2\left|\min\left(\Delta e_{upper}(t)\right)\right|}{nV_{C_{sm}}^2\left(2k-k^2\right)}. \tag{3.29}$$

Substituting (3.28) and (3.29) into (3.21), the minimum nominal energy values are

$$\begin{aligned} E_{nom}^{'} &\geq \frac{\max(\Delta e_{upper})}{(2k+k^2)} \\ E_{nom}^{''} &\geq \frac{\left|\min(\Delta e_{upper})\right|}{(2k-k^2)} \end{aligned}. \tag{3.30}$$

To ensure that the minimum and maximum voltage values are within limits defined in (3.24), the nominal energy is defined as

$$E_{nom} = \max(E_{nom}^{'}, E_{nom}^{''}). \tag{3.31}$$

Figure 3.6 illustrates the regions where $E_{nom}$ takes either $E'_{nom}$ or $E''_{nom}$ as a function of $k$ and the ratio between $\max(\Delta e_{upper})$ to $\min(\Delta e_{upper})$. Within the $E_{nom} = E'_{nom}$ region, the maximum voltage $(1+k)V_{dc}$ is reached, whereas the minimum voltage will be greater than $(1-k)V_{dc}$. Alternatively, the $E_{nom} = E''_{nom}$ region implies that the minimum voltage is reached, while the maximum voltage will be less than $(1+k)V_{dc}$. From Figure 3.6, if $k = 0.1$, $E_{nom}$ will be equal to $E''_{nom}$, unless $\max(\Delta e_{upper})$ is 10% greater than $\min(\Delta e_{upper})$. The energy storage requirement in terms of total energy storage per transferred VA [86] is calculated as

$$W_{conv} = \frac{6}{S_{conv}} E_{nom}. \tag{3.32}$$

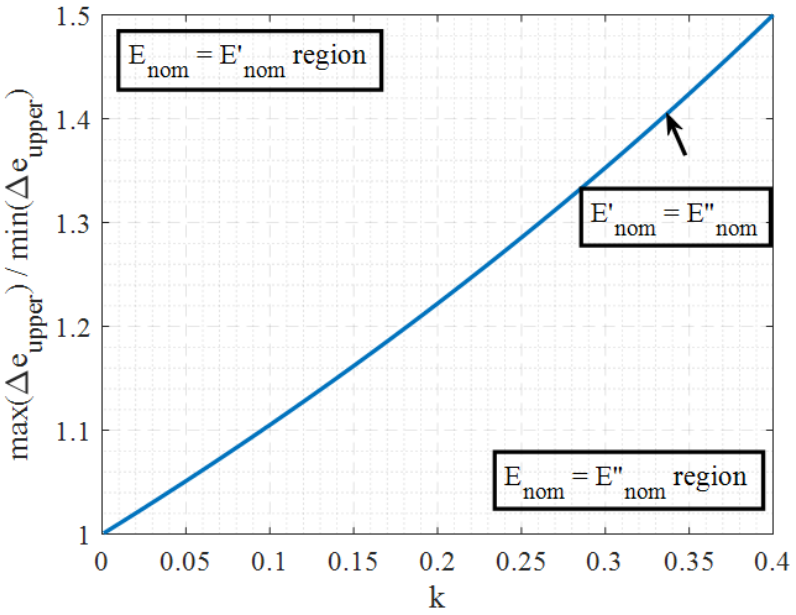



Figure 3.6. Relation between $(E'_{nom}, E''_{nom})$ for $E_{nom}$.

The following subsections describe the capacitor energy storage requirements for the different types of operation for a BESS-MMC system.

### 3.6.1 Power transfer to AC Grid

If the only currents that flow through the BESS-MMC arms are related to the operation of the MMC with the utility grid, the upper arm current in phase A, $i_{arm}$, is

$$i_{arm}(t) = \frac{I_g}{2}\sin(\omega t + \phi_i), \tag{3.33}$$

where $I_g$ is the peak value of the grid currents, and $\phi_i$ is the grid current phase angle. Based on this assumption, the energy variation is expressed as

$$\Delta e_{upper}(t) = V_{dc}\left(-\frac{I_g}{4\omega}\cos(\omega t + \phi_i) + \frac{mI_g}{16\omega}\sin(2\omega t + \theta_v + \phi_i)\right). \tag{3.34}$$

Equation (3.34) is function of $V_{dc}$, which can change depending on the grid voltage. The variable $V_{dc}$ can be replaced by the MMC rated three-phase power, current magnitude, and modulating index. The new expression for the energy variation is

$$\Delta e_{upper}(t) = \frac{S_{conv}}{12m\omega}\left(\frac{-4I_g}{I_{g,nom}}\cos(\omega t + \phi_i) + \frac{mI_g}{I_{g,nom}}\sin(2\omega t + \theta_v + \phi_i)\right). \tag{3.35}$$

According to (3.30)-(3.32), the capacitor energy storage requirement per transferred VA ($W_{conv}$) is dependent on the modulating index, grid current amplitude (in p.u.), and the grid current phase angle. Figure 3.7 shows the energy requirement change as a function of the aforementioned variables, assuming $\theta_v = 0$. Increasing the arm current amplitude or decreasing the modulating index increases the energy requirement. The current phase angle $\phi_i$ also affects $W_{conv}$, where the worst-case scenario occurs when injecting mainly inductive currents to the grid ($\phi_i = 90^o$). Taking

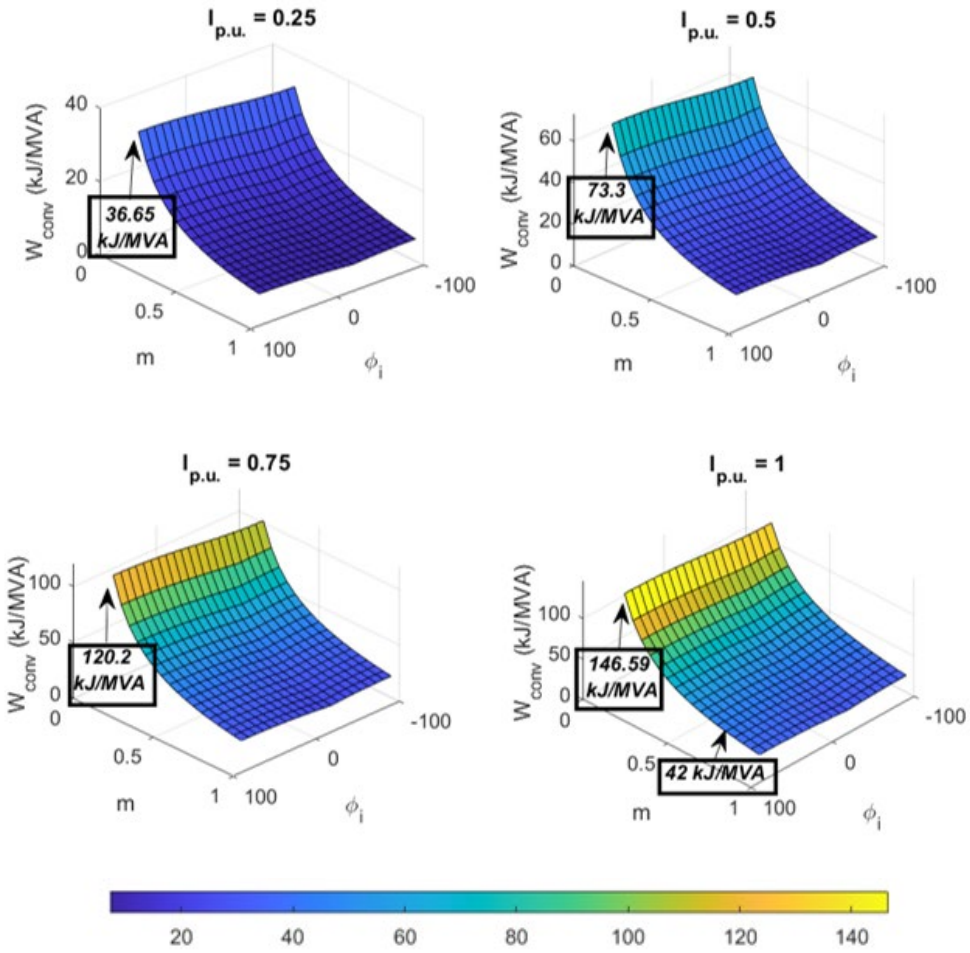



Figure 3.7. Energy requirements assuming that the arm currents are only with grid currents.

a modulating index of 0.8, the energy requirement obtained for the worst scenario is 42 kJ/MVA, which is near the requirement considered in most designs.

### 3.6.2 Phase power transfer

If the only currents that flow into the MMC arms are the grid currents and the DC-current component utilized for phase balancing, the arm current for the upper arm of phase A can be defined as

$$i_{arm}(t) = \frac{I_g}{2}\sin(\omega t + \phi_i) + I_{dc}. \tag{3.36}$$

Considering the connection of a BESS-MMC with only a virtual common DC-bus (i.e., without connecting any component to the DC-ports), the DC currents for each phase must satisfy

$$\sum_{i=a,b,c} I_{dc,i}(t) = 0. \tag{3.37}$$

The DC current in each phase is described as the ratio between the DC power transfer between a specific phase and the remaining two to the DC link voltage ($P_{dc}/V_{dc}$). The variable $P_{dc}$ can be rewritten as a function of the nominal per phase active power and the per phase grid active power. The resulting expression is

$$P_{dc} = k_1 \frac{\left(S_{conv}\xi - S\cos(\phi_i)\right)}{3}, \tag{3.38}$$

where $k_1$ is the utilization factor of the available active power and $\xi$ is the ratio between $P_{conv}$ and $S_{conv}$. Assuming a lossless system, the variable $\xi$ correlates the rated power of the batteries and the rated power of the MMC. Dividing (3.38) by $V_{dc}$ and replacing the latter by its expression as a function of rated power, modulating index, and nominal grid current, the DC current for a specific phase is

$$I_{dc} = \frac{mI_{g,nom}k_1}{4}\left(\xi - \frac{S\cos(\phi_i)}{S_{conv}}\right). \tag{3.39}$$

The relation $Scos(\phi_i)/S_{conv}$ can be defined as the ratio between the active power at a given condition and the rated apparent power of the converter, with an interval range of $[0, \xi]$. To maximize the DC current, it is assumed that $cos(\phi_i) \approx 0$, as the greatest energy requirement occurs with $(\phi_i) = 0$. Under this assumption, a new

expression can be obtained for the energy ripple. The energy ripple expression is obtained as

$$\Delta e_{upper}(t)=\frac{S_{conv}}{12m\omega}\left(\begin{array}{l}-\frac{4I_g}{I_{g,nom}}\cos(\omega t+\phi_i)+\frac{mI_g}{I_{g,nom}}\sin(2\omega t+\theta_v+\phi_i)+\\ +2m^2k_1\left(\xi-\frac{S\cos(\phi_i)}{S_{conv}}\right)\cos(\omega t+\theta_v)\end{array}\right). \tag{3.40}$$

The following result assumes that $\xi = 1/\sqrt{2}$, indicating that the MMC can inject the maximum active power from the batteries while providing the same reactive power. The variable $\xi$ can be modified for any combination as per the BESS-MMC design. Figure 3.8 illustrates $W_{conv}$ for different values of modulating index and $k_1$ while assuming $\phi_i = 90^o$ and nominal grid currents.

Figure 3.8 shows that the energy requirement, while assuming $k_1 = 0$, matches with those related to grid current only since there is no phase power transfer. Furthermore, as $k_1$ increases to 1, the energy requirement also increases. However, this

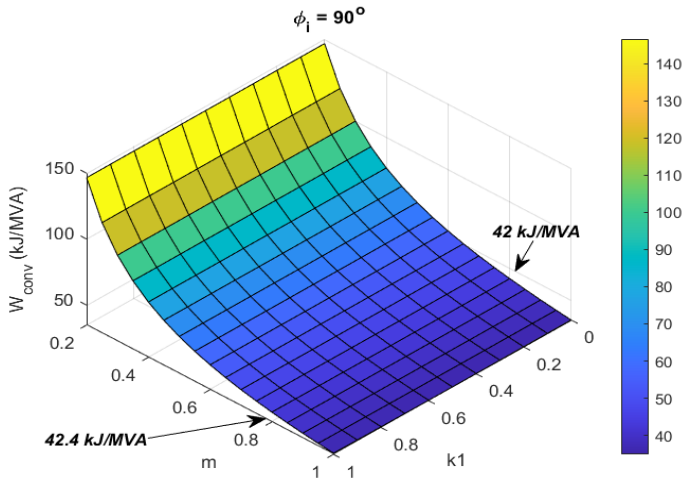



Figure 3.8. Energy requirements assuming that arm currents are grid and DC circulating currents.

increase is only marginal, which indicates that the DC phase power transfer hardly affects the capacitor energy requirements.

### 3.6.3 Arm power transfer

The arm power transfer strategy is based on developing circulating AC (at fundamental frequency) currents of positive and negative sequence that, by interacting with the synthesized voltages on the upper and lower arms, result in active power transfer [87]. The synthesized voltages on the upper and lower arms are related to the operation with the AC grid. The arm current for the upper arm phase A is

$$\begin{aligned} i_{arm}(t) = \frac{I_g}{2}\sin(\omega t + \phi_i) + I_\Delta^+ \sin(\omega t + \theta_v + \gamma^+) \\ + I_\Delta^- \sin(\omega t + \theta_v + \gamma^-) \end{aligned} . \tag{3.41}$$

where $I_\Delta^+$ and $I_\Delta^-$ are the positive and negative sequence circulating current amplitude, respectively, and $\gamma^+$ and $\gamma^-$ are the positive and negative sequence phase displacement with respect to the synthesized grid voltages, i.e., the phase displacement with respect to $\theta_v$. From the expressions presented in [87], the variables $I_\Delta^+$, $I_\Delta^-$, $\gamma^+$, and $\gamma^-$ are

$$\begin{cases} I_\Delta^+ = \dfrac{4}{3mV_{dc}}\left(P_{\Delta a} + P_{\Delta b} + P_{\Delta c}\right) \\ \gamma^+ = \tan^{-1}\left(\dfrac{0}{P_{\Delta a} + P_{\Delta b} + P_{\Delta c}}\right) \end{cases} \tag{3.42}$$

and

$$\begin{cases} I_\Delta^- = \dfrac{4}{3mV_{dc}}\sqrt{\left(2P_{\Delta a} - P_{\Delta b} - P_{\Delta c}\right)^2 + 3\left(P_{\Delta b} - P_{\Delta c}\right)^2} \\ \gamma^- = \tan^{-1}\left(\dfrac{\sqrt{3}\left(P_{\Delta b} - P_{\Delta c}\right)}{\left(2P_{\Delta a} - P_{\Delta b} - P_{\Delta c}\right)}\right), \end{cases} \tag{3.43}$$

where $P_{\Delta i}$ is the active power transferred between upper and lower arms for a specific phase. Similar to the phase power transfer analysis, the arm power transfer is rewritten as a function of the nominal per arm active power and the per arm grid active power. The arm power transfer is

$$P_{\Delta i} = k_{3i}\frac{\left(S_{conv}\xi - S\cos(\phi_i)\right)}{6}, \tag{3.44}$$

where $k_{3i}$ is the utilization factor of the available per arm active power. Note that assuming a positive value for $P_{\Delta i}$ leads to the upper arm providing power to the lower arm, while the opposite occurs for a negative $P_{\Delta i}$. Inherently, $k_{3i}$ can vary from -1 to 1. Replacing (3.44) into (3.42) and (3.43), and $V_{dc}$ by its expression as a function of rated power, modulating index, and nominal grid current, the variables $I_{\Delta}^{+}$, $I_{\Delta}^{-}$, $\gamma^{+}$ and $\gamma^{-}$ are:

$$\begin{cases} I_{\Delta}^{+} = \dfrac{I_{g,nom}}{6}\left(\xi - \dfrac{S\cos(\phi_i)}{S_{conv}}\right)\left(k_{3a}+k_{3b}+k_{3c}\right) \\ \gamma^{+} = \tan^{-1}\left(\dfrac{0}{k_{3a}+k_{3b}+k_{3c}}\right) \end{cases} \tag{3.45}$$

and

$$\begin{cases} I_{\Delta}^{-} = \dfrac{I_{g,nom}}{6}\left(\xi - \dfrac{S\cos(\phi_i)}{S_{conv}}\right)\sqrt{\left(2k_{3a}-k_{3b}-k_{3c}\right)^2 + 3\left(k_{3b}-k_{3c}\right)^2} \\ \gamma^{-} = \tan^{-1}\left(\dfrac{\sqrt{3}\left(k_{3b}-k_{3c}\right)}{\left(2k_{3a}-k_{3b}-k_{3c}\right)}\right). \end{cases} \tag{3.46}$$

For a complete analysis, all phases and arms need to be assessed. The reason for that is because each arm experience a different energy ripple, given by the interaction of the arm's synthesized voltage and the arm current. For convenience purposes only the upper arm of phase A is considered in this dissertation. Nevertheless, the energy

ripple for the remaining arms can be easily obtained using the same steps. Therefore, the energy ripple across the capacitor for the upper arm of phase A is

$$\Delta e_{upper}(t) = \frac{S_{conv}}{36m\omega}\left( -\frac{12I_g}{I_{g,nom}}\cos(\omega t+\phi_i) + \frac{3mI_g}{I_{g,nom}}\sin(2\omega t+\theta_v+\phi_i) + \right.$$
$$+\left(\xi - \frac{S\cos(\phi_i)}{S_{conv}}\right)\left(k_{3a}+k_{3b}+k_{3c}\right)\left(-4\cos(\omega t+\theta_v+\gamma^+) + m\sin(2\omega t+2\theta_v+\gamma^+)\right) + \quad .$$
$$\left.+\left(\xi - \frac{S\cos(\phi_i)}{S_{conv}}\right)\sqrt{\left(2k_{3a}-k_{3b}-k_{3c}\right)^2+3\left(k_{3b}-k_{3c}\right)^2}\left(-4\cos(\omega t+\theta_v+\gamma^-) + m\sin(2\omega t+2\theta_v+\gamma^-)\right)\right)$$

(3.47)

The capacitor energy requirement can be obtained as a function of $k_{3a}$, $k_{3b}$, $k_{3c}$, the modulating index, and the p.u. value of the grid currents. Since the worst-case scenario for the grid currents occurs with $\phi_i = 90^o$, the following is considered under the arm power transfer analysis: 1) $S\cos(\phi_i)/S_{conv} = 0$; 2) and $I_g/I_{g,nom} = 1\ p.u$; 3) $m = 0.8$. Under these assumptions, $W_{conv}$ is function of only $k_{3a}$, $k_{3b}$, $k_{3c}$, as illustrated in Figure 3.9.

Note from Figure 3.9 that as $k_{3a}$ increases, both the maximum and minimum energy requirements also increase. Furthermore, for all scenarios, the maximum energy requirement occurs when $k_{3b} = 1$ and $k_{3c} = -1$, whereas reversing the sign of these variables leads to the minimum energy requirement. Figure 3.9 also highlights that $W_{conv}$ almost doubles the previous conditions, being estimated at 81.1 kJ/MVA. This implies that if the original energy requirement was utilized to design the capacitor and the arm power transfer was utilized, the voltage ripple would surpass the specified limit of 10%.

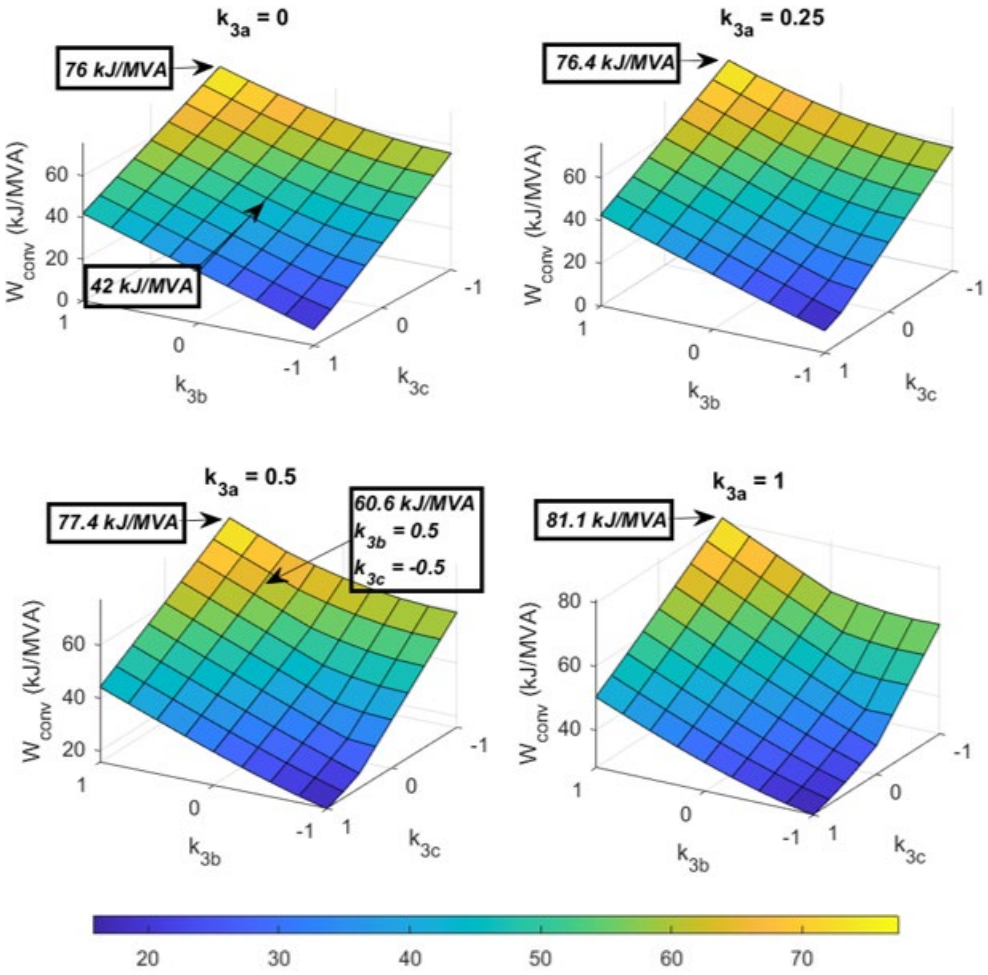



Figure 3.9. Energy requirements assuming that arm currents are grid and AC circulating currents.

### 3.6.4 BESS-MMC capacitor energy requirement remarks

As mentioned in the introduction, according to current literature guidelines, the capacitor energy requirements for BESS-MMC should be around 30-40 kJ/MVA. However, it is clear from the analysis that this might not be the case for a system where the battery is connected to the DC-link capacitor through a bidirectional converter. In the scenario where only grid currents are flowing, the minimum requirement obtained is 42 kJ/MVA, which is numerically closer to the higher limit presented in [79]. Furthermore, for a BESS-MMC, prolonged phase power transfer and arm power transfer

are required to achieve power and SoC balancing. The impact of these two operating modes was not previously investigated.

Considering both grid currents and phase active power transfer, the requirement marginally increases to 42.4 kJ/MVA. This result implies that the capacitor sizing increase is almost negligible irrespective of the active power exchange level. Therefore, any system designed with a capacitor energy requirement closer to 40 kJ/MVA would also meet the phase power transfer requirement.

Finally, considering grid currents and arm power transfer, the capacitor energy requirement almost doubles to 81.1 kJ/MVA. Therefore, if such an operation is expected, the capacitor sizing needs to be doubled as it is directly proportional to the energy requirement. This has substantial implications for the cost of the MMC-BESS since, according to [37], the capacitor cost is a significant disadvantage. However, one possible way to reduce the requirement is by limiting the active power exchange levels. Figure 3.9 shows that by limiting the arm active power exchange to only half the available power, the energy requirement reduces to 60.6 kJ/MVA, which is only a 44% increase in the operation with grid and phase power transfer. Limiting the arm active power exchange, however, would lead to slower arm SoC balancing can be achieved. Therefore, there is a trade-off between fast SoC balancing and capacitor sizing.

### 3.7 Controller hardware-in-the-loop results

A system comprised of AC grid and BESS-MMC is implemented using two Typhoon HIL604 devices, as shown in Figure 3.10(a). Three TMS320F28335 microcontrollers are utilized to control the MMC-BESS converters (an additional microcontroller is utilized for protection/enable purposes). The implementation within

the C-HIL environment is shown in Figure 3.10(b). The system parameters are shown in Table 3.2.

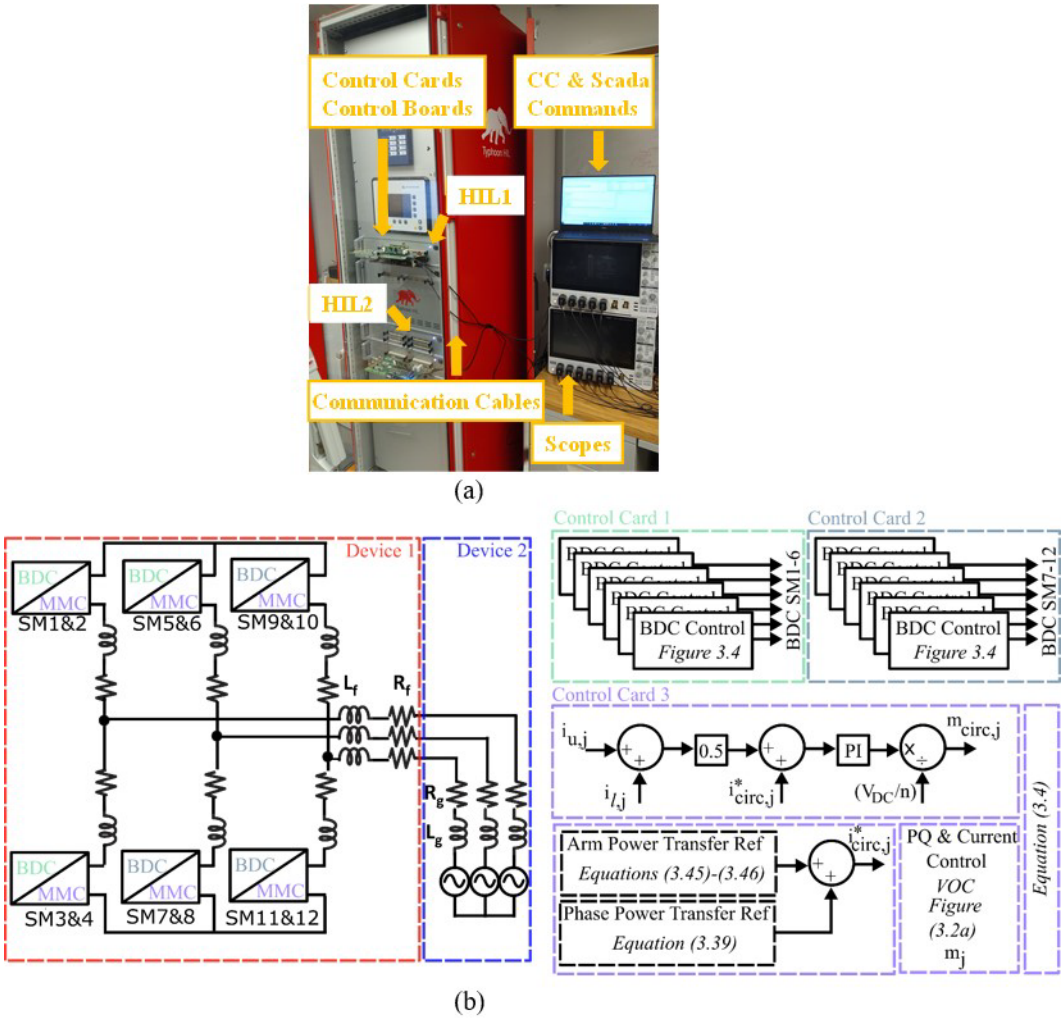



Figure 3.10. C-HIL setup. a) Experimental testbed; (b) Implementation in Typhoon and microcontrollers.

Table 3.2 MMC based BESS parameters

| Parameter | Parameter description | Specification |
|---|---|---|
| | ***MMC-side*** | |
| $P_{BESS}$ | BESS rated active power | 4.2 kW |
| $S_{CONV}$ | MMC rated power | 6 kVA |
| $v_g$ | Grid phase voltage | 120 $V_{RMS}$ |
| $L_{AC} + L_{arm}/2$ | MMC equivalent inductance | 2 mH |
| $R_{AC} + R_{arm}/2$ | MMC equivalent resistance | 75 $m\Omega$ |
| $n$ | Number of SMs per arm | 2 |
| $V_{DC}$ | DC-link voltage (Total MMC) | 400 $V_{DC}$ |
| - | ***Bidirectional converter-side*** | |
| $L_{dc}$ | BDC inductance | 560$\mu$H |
| $R_T$ | BDC equivalent series resistance | 0-1Ω (0.5Ω nom.) |
| $V_{oc}$ | Battery open-circuit voltage | 51.2 Vdc |
| $P$ | SM power | $1 - 350W$ (rated) |
| $d$ | Duty ratio | 0.2-0.3 (0.25 nom.) |
| $i_{bat}$ | Rated inductor/battery current | 7 A |

### 3.7.1 BDC controllers parameters and NF design

The BDC controllers are designed according to (3.5) and (3.6). The current loop is designed with a high gain crossover frequency ($f_{gc}$) and phase margin, 2.1 kHz and 70°, respectively. The $f_{gc}$ for the grid current loop is 2.1 kHz with a phase margin of 90°.

Different PI controllers are designed for $C_{vi}(s)$. Figure 3.11(a) shows the open-loop system frequency response with $f_{gc}$ criteria of 5 Hz, 12 Hz, and 20 Hz. The phase margin for all systems is selected as 70°.

Figure 3.11(b) shows the attenuation provided by each of these controllers. The attenuation to 60 and 120 Hz components, provided by the PI controllers, is seen to decrease with the increase in gain cross-over frequency of the open-loop system. For $f_{gc} = 5$ Hz, the maximum attenuation observed is -20 dB. To observe the effect of the phase margin on the attenuation of the oscillating components, Figure 3.11(c) shows different PI controllers with $f_{gc}$ =20 Hz and phase margins from 60° to 90°. It can be observed that by decreasing the phase margin, the PI controller provides more attenuation. However, this effect is not as noticeable as changing the system's $f_{gc}$. The controller with $f_{gc} = 5$ Hz and 70° phase margin is selected for the results in this subsection.

For the values presented in Table 3.2, assuming $\alpha_{Curr-ripple}$ in (3.7) to be 1% and $\alpha_{Volt-ripple}$ to be 10% of the rated DC-link voltage, the required attenuation at grid frequency is at least -42 dB. A similar approach can be utilized to determine the attenuation at 120 Hz or by directly calculating the required attenuation making use of the energy ripple information shown in Section 3.6. Figure 3.12 shows the controller with $f_{gc} = 5$ Hz and 70° phase margin, which is selected for the results in this chapter, with the addition of NF1 from Table 3.1. By adding NF1, as designed following the guidelines in Section 3.5.2.2, the voltage loop is not significantly affected, as highlighted in Figure 3.12.

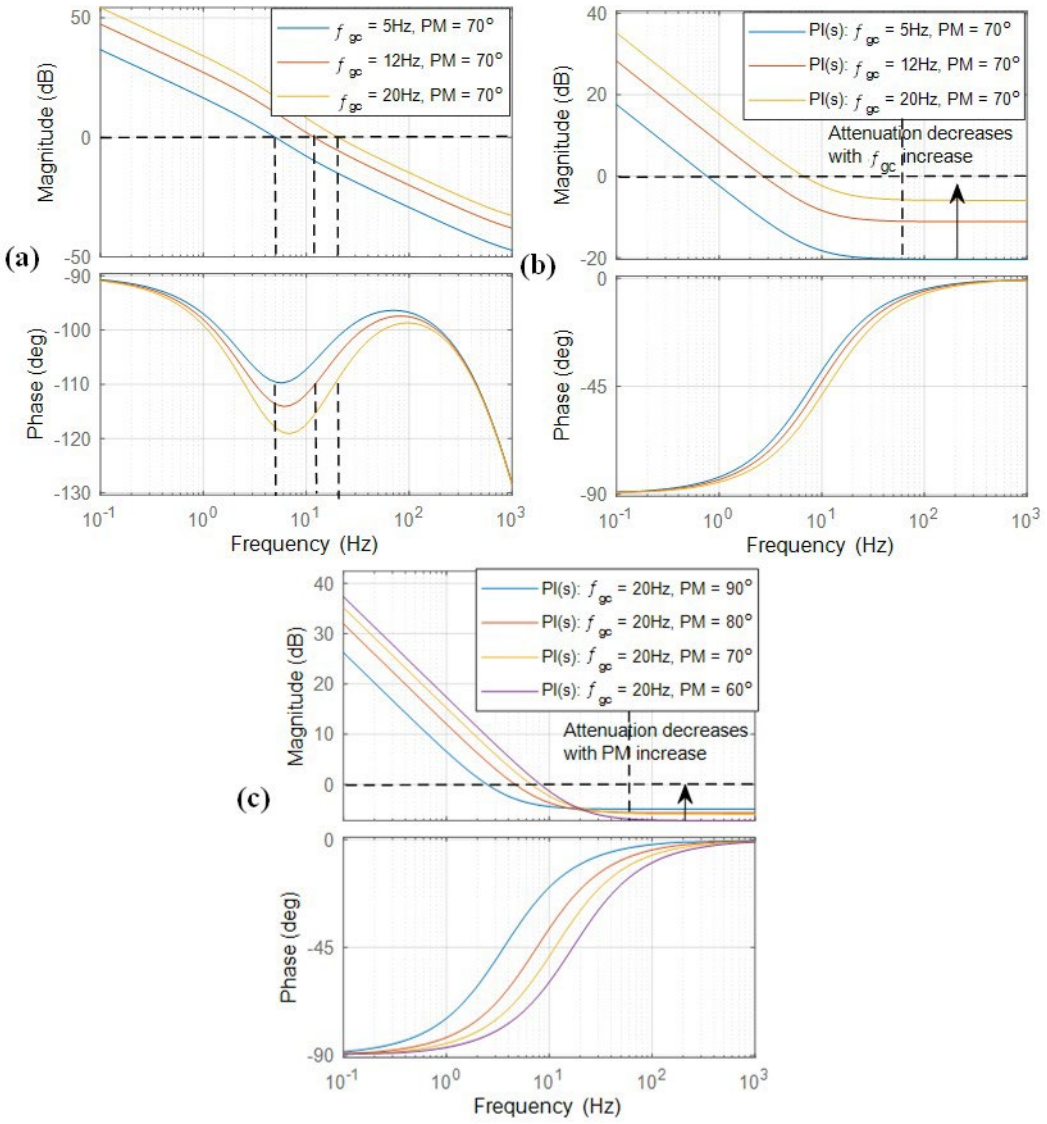



Figure 3.11. Voltage loop controllers and filter analysis. (a) Open-loop response for different PI controllers;(b) GC frequency impact on attenuation;(c) Phase margin impact on attenuation.

### 3.7.2 Capacitor sizing validation

Three scenarios are investigated for each MMC arm current condition: 1) grid only currents; 2) grid and phase power transfer; 3) grid and arm power transfer. All scenarios assume the injection of inductive currents towards the grid at the MMC's

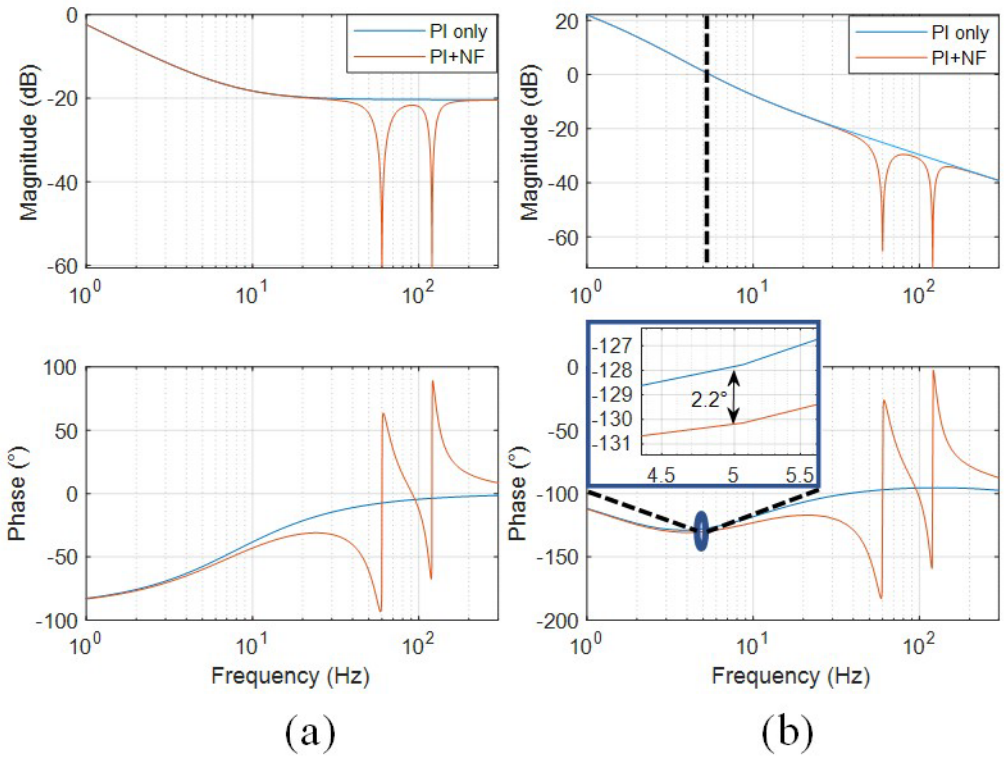



Figure 3.12. Bode plot: (a) PI and PI+NF; (b) Open-loop $G_{vi}$ with PI and PI+NF.

maximum power rate, as this is the expected worse scenario. Based on the estimated capacitor energy requirement, the capacitor for each scenario is calculated as

$$C_{sm} = 2nE_{nom} \Big/ (nV_{C_{sm}})^2 . \tag{3.48}$$

### 3.7.2.1 Grid currents only

In the first scenario, the capacitor energy storage requirement in terms of transferred VA is 42 kJ/MVA. The corresponding capacitor value is estimated as 1.1 mF. Figure 3.13 and Figure 3.14 show the phase A upper arm current, the battery current (assuming PI and PI+NF configuration), circulating current, and capacitor voltage variation. Since the aim is to limit the capacitor voltage to 10% of its nominal value, the strategy ensures that the maximum or minimum voltage limit is reached. In both Figure

3.13 and Figure 3.14, the lower limit of 180 V is obtained. These results validate the analysis since severely limiting the current ripple leads to mainly SM's current ripple flowing into the SM capacitor. The capacitor voltage FFT is shown in Figure 3.15. The amplitude of the oscillations at 60 Hz and 120 Hz are 15.3 V and 3.2 V, respectively. The attenuation obtained at 60 Hz for the battery current ripple is almost -60 dB (-20 dB from the PI controller and an additional -40 dB from the NF). For a BDC with only a PI controller, the oscillation at 60 Hz and 120 Hz is 1.47 A and 0.3 A, respectively (-20 dB attenuation), highlighting that the PI controller cannot attenuate the current ripple.

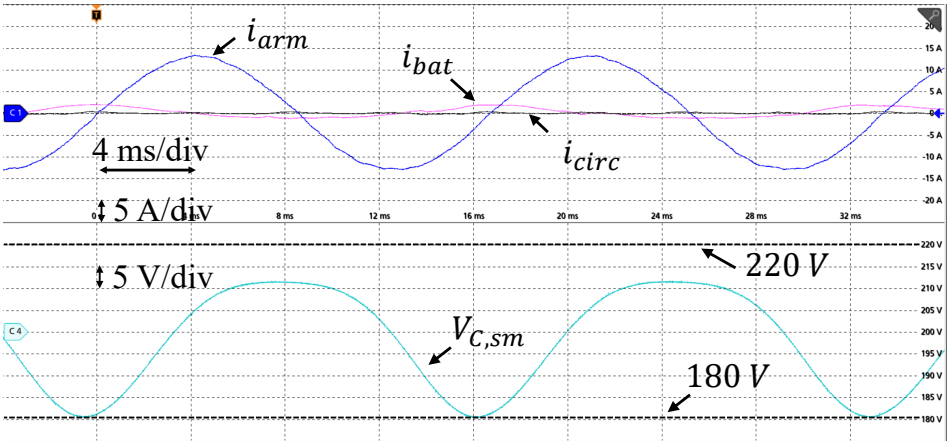



Figure 3.13. C-HIL results under grid power exchange (PI).

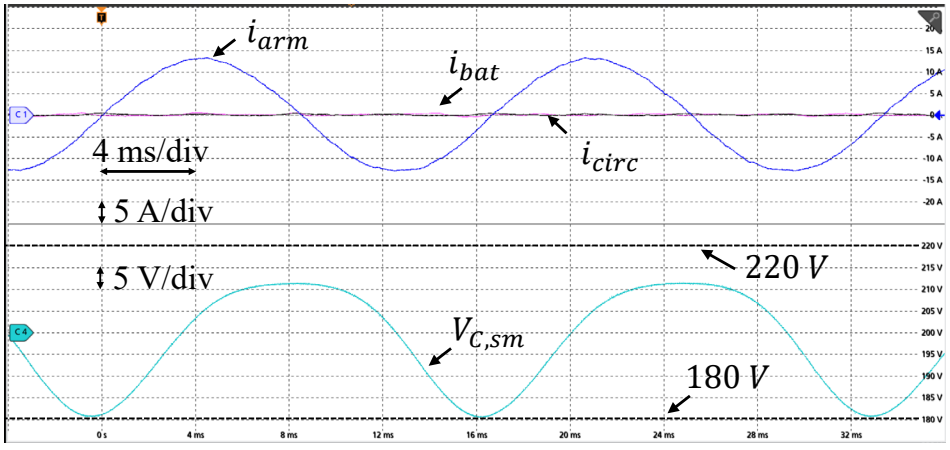



Figure 3.14. C-HIL results under grid power exchange (PI+NF).

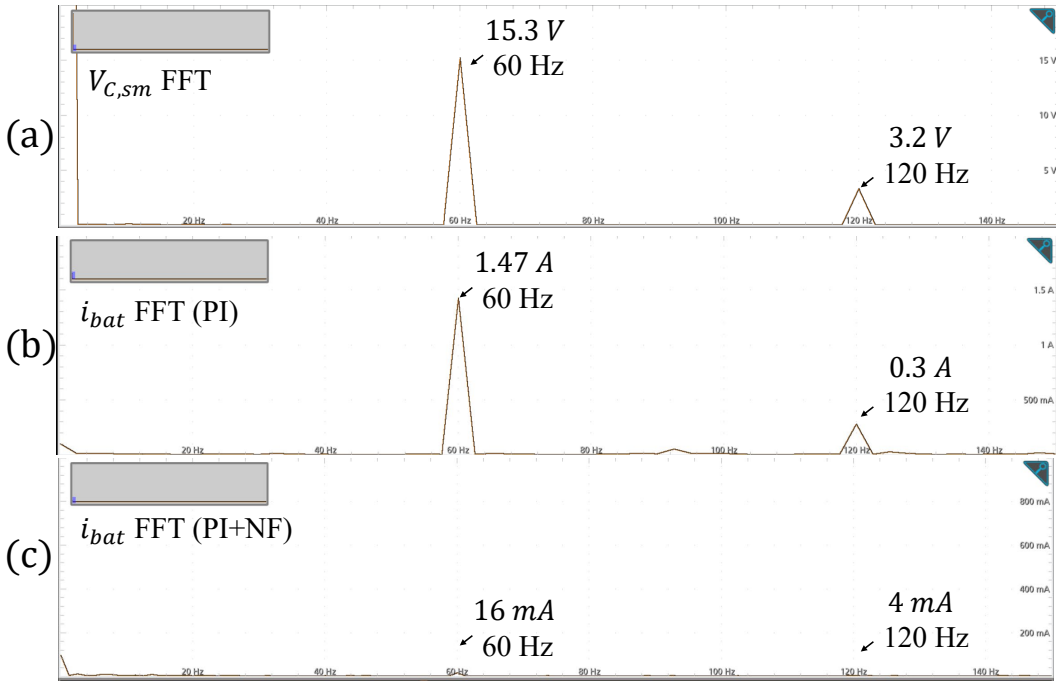



Figure 3.15. C-HIL FFT ripple: (a) Capacitor voltage; (b) battery current with PI; (c) battery current with PI+NF.

### 3.7.2.2 Grid and phase power transfer

In the second scenario, the capacitor energy requirement in terms of transferred VA does not significantly change from the one where only grid power exchange is considered. Results shown in Figure 3.16 are obtained utilizing the capacitor value of 1.1 mF. Even though the phase sinks its rated value of 1.4 kW (Figure 3.17), the capacitor voltage ripple is kept within the 10% oscillation. The minimum voltage value of 180 V is not surpassed, in accordance with the analysis presented in Section 3.6.

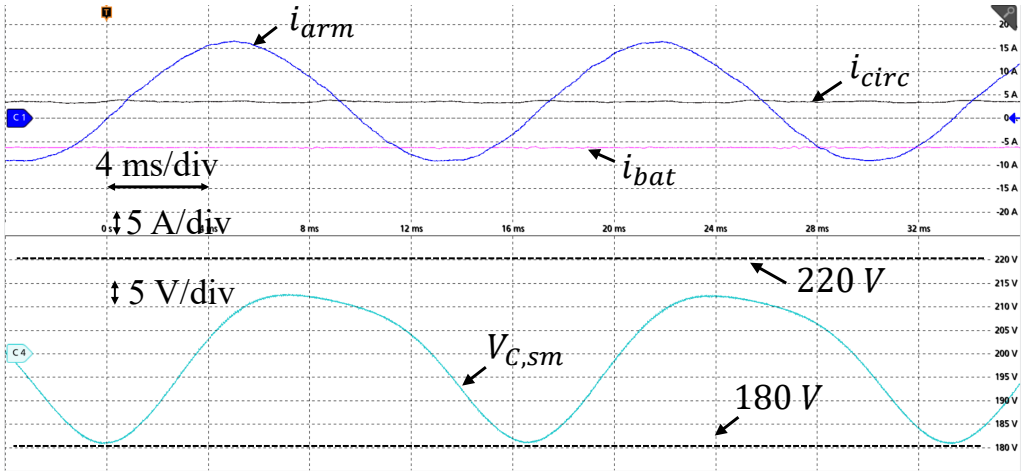



Figure 3.16. C-HIL results under grid and phase power exchange.

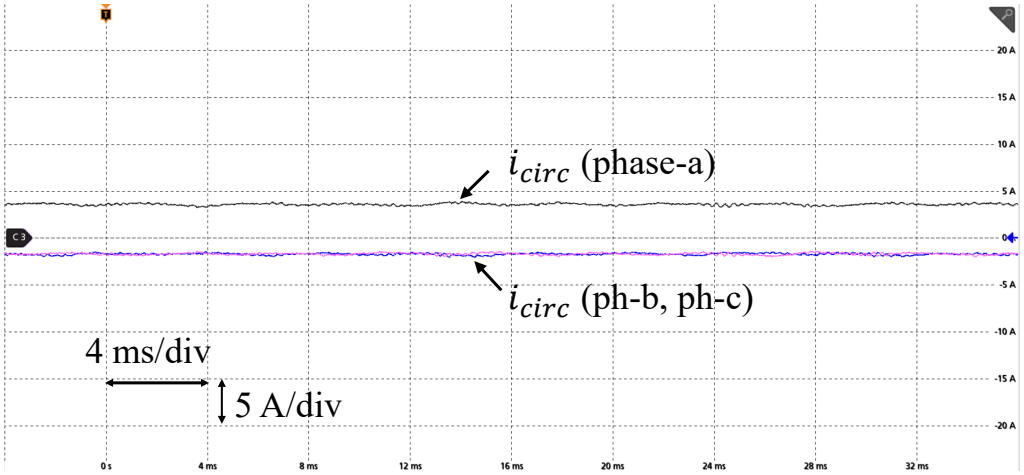



Figure 3.17. C-HIL results under grid and phase power exchange (circulating current).

### 3.7.2.3 Grid and arm power transfer

In the third scenario, $W_{conv}$ is 81.1 kJ/MVA, which leads to a capacitor value of 2.2 mF. This increase can be limited by reducing the maximum arm power transfer. Figure 3.18 shows a power exchange at half the power rating of the arms (350 W), thus assuming $k_{3a} = k_{3c} = 0.5$ and $k_{3b} = -0.5$. The circulating currents are shown in Figure 3.19. At this condition, the energy requirement drops to 60.6 kJ/MVA, leading to a

capacitor of 1.5 mF. The capacitor voltage ripple is kept within the limitations as designed.

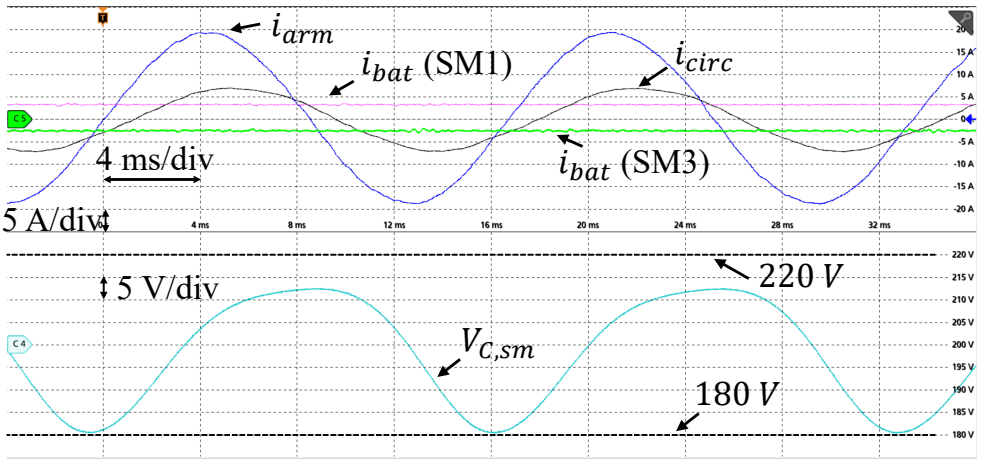



Figure 3.18. C-HIL results under grid and arm power exchange.

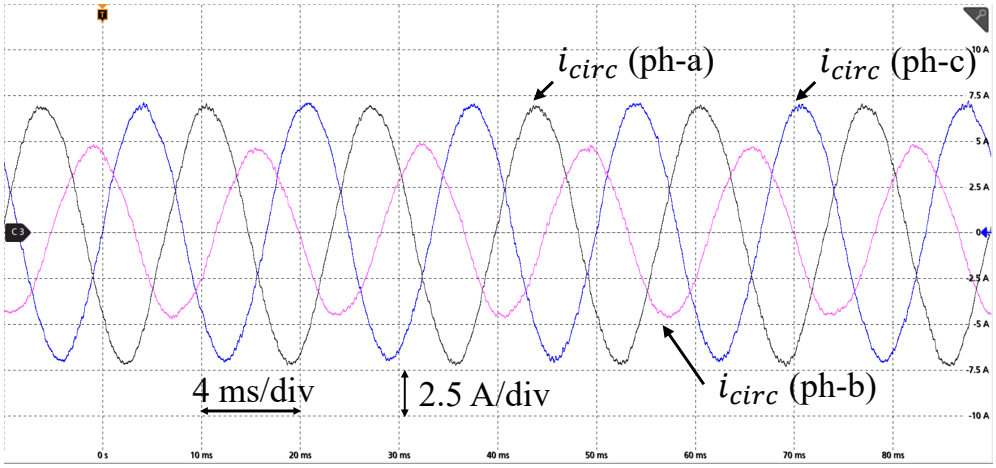



Figure 3.19. C-HIL results under grid and arm power exchange (circulating current).

### 3.7.2.4 Capacitor sizing comparison

As discussed in Section 3.6, the capacitor energy requirement, $W_{conv}$, is the same irrespective of converter power level, number of modules, and DC-link voltage. Therefore, Table 3.3 highlights a comparison between different capacitor designs in BESS-MMC with BDC in terms of $W_{conv}$. The sample references included did not state $W_{conv}$. However, based on the parameters given (number of modules, power level,

voltage level, and capacitance value), the equivalent $W_{conv}$ can be calculated. Note that the BESS-MMC papers do not assume the operation as discussed in the previous sections. Instead, the papers focus on either control strategies or modeling. Table 3.3 should be viewed as how the different configurations should be changed to conform with the scenario established for BESS-MMC operation under the different operation modes discussed throughout the previous sections. In two cases ([107] and [93]), the less stringent scenario with $W_{conv} = 42.4$ kJ/MVA is not observed. This indicates that the operation of BESS-MMC as an ES-STATCOM would cause a capacitor voltage deviation greater than 10%. For the third case [87], the $W_{conv}$ obtained is 92.8 kJ/MVA, which is greater than the worst-case scenario, i.e., ES-STATCOM operation with arm active power transfer, which only requires 81.1 kJ/MVA.

Table 3.3 $W_{CONV}$ assessment for different scenarios

| **Reference** | **Scenario** | $\boldsymbol{W_{conv}}$ | $\boldsymbol{W_{conv}}$ ***required change*** |
|---|---|---|---|
| Ref [107] | $n = 2$;<br>$V_{C_{sm}}$ =60 V<br>$S_{MMC}$ =2.83 kVA<br>$C_{sm}$= 3 mF | 23 kJ/MVA | +85 % (phase)<br>+254 % (arm) |
| Ref [93] | $n = 10$;<br>$V_{C_{sm}}$ =80 V<br>$S_{MMC}$ =21 kVA<br>$C_{sm}$= 2.1 mF | 19.2 kJ/MVA | +121 % (phase)<br>+323 % (arm) |
| Ref [87] | $n = 6$;<br>$V_{C_{sm}}$ =4.4 kV<br>$S_{MMC}$ =37.2 MVA<br>$C_{sm}$= 9.89 mF | 92.8 kJ/MVA | -54 % (phase)<br>-12.6 % (arm) |

## 3.8 Conclusion

This chapter discusses design considerations of the controllers related to a BESS-MMC with the energy storage elements connected through a half-bridge (buck/boost) bidirectional converter. Models for both MMC and BDC are derived from

which the controllers can be designed. Further, the relation between the BDC current ripple and the submodule capacitor voltage ripple is described to obtain guidelines for the design of the BDC control to improve controller performance and reduce current ripple. By ensuring this optimal operation, a detailed analysis of the capacitor energy requirement in terms of transferred VA ($W_{conv}$) of a BESS-MMC, with full active and reactive power capabilities, is developed and validated through a C-HIL environment. The minimum capacitor energy requirement is found to be very similar while considering only grid power exchange and both grid and phase power exchange. However, BESS-MMC operation using grid and arm power exchange leads to doubling the requirements. Limiting the arm power exchange rate can be a good option to mitigate the capacitor sizing increase.

### 3.9 Publications

- J. M. L. Fonseca, S. R. P. Reddy and K. Rajashekara, "Design of Digital Controllers for the Reduction of Low-Frequency Harmonic Currents in Double Star Chopper Cell-based Battery Energy Storage Systems," *2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2021, pp. 1-8.

- J. M. L. Fonseca, S. R. P. Reddy and K. Rajashekara, “Reduced Capacitor Energy Requirements in Battery Energy Storage Systems based on Modular Multilevel Converters “. *IEEE Transactions on Industry Applications (under review)*.

# 4. POWER AND STATE-OF-CHARGE (SOC) BALANCING STRATEGIES FOR BESS-MMC UNDER ASYMMETRIC CONDITIONS

## 4.1 Introduction

Modular Multilevel Converter (MMC) is a flexible topology that can be used as a power conversion for Battery Energy Storage Systems (BESS). Based on the arrangement of batteries, there are two types of BESS-MMC: one centralized on the common dc link of MMC and one distributed on the dc side of each module. The latter is the most common approach as it guarantees higher efficiency, reduced voltage requirement, and higher battery redundancy [108], [109]. Because of this advantage, the distributed approach is utilized throughout the dissertation. Although there are clear advantages of using the distributed approach, power management strategies based on the power transfer between the different phases and arms of the MMC are required to achieve flexible operation. This chapter addresses the operation of the BESS-MMC under grid-voltage asymmetry and asymmetric available phase and arm power.

### 4.1.1 Operation under grid-voltage asymmetry

Clear guidelines are available for the low-voltage ride through (LVRT) operation of RES (e.g., wind and solar power generation) under stringent grid-code regulations. These guidelines are not directly translated to BESS applications, given their bidirectional operation characteristics. Nevertheless, few proposals regarding the operation of BESS, including scenarios for LVRT, are reported in [84], [110]. In [110], a strategy utilizing a three-phase two-level converter topology as an interface between

energy storage and the grid is deployed. The strategy involves injecting positive sequence components of active and reactive power in a symmetric grid voltage scenario. In [84], a BESS-MMC with both DC and AC ports is considered. The LVRT scenario considers a short-circuit on the AC side. Thus, the control strategy prevents power exchange between BESS and AC grid.

During an asymmetric grid voltage scenario, a BESS-MMC can experience a severe power imbalance. This is because the batteries are connected in a modular fashion and can experience uneven charging/discharging operation in each phase. Furthermore, the power imbalance is closely related to the LVRT strategy employed. The operation under asymmetric grid voltage conditions can cause uneven SoC of the batteries among phases, affecting the resiliency of the BESS operation with the grid over the long run. Therefore, balancing the SOC in each phase is essential under this scenario.

SoC balancing techniques for a BESS-MMC under DC and AC grid fault conditions are reported in [84], [111]. However, both strategies assume a balanced AC grid active power for their operation, which may not occur during an LVRT scenario. In [112], the SoC balancing strategy does not consider the fact that the grid active power limits for each phase may be different. The previously mentioned strategies are developed based on the calculation of the mismatch between average phase SoC and the average BESS SoC, multiplied by a coefficient, thus leading to power references for per-phase SoC balancing. No clear guidelines on selecting this coefficient are presented in the literature. Choosing a high coefficient value may result in power references that exceed rated power limitations or overmodulation.

To overcome the abovementioned issues, this chapter investigates different control strategies to balance the active power among the phases of the BESS-MMC during AC grid voltage asymmetry. This involves control strategies that are external and internal to the converter. The external strategy is achieved through grid-current control. The internal strategy balances the active power of the BESS, making use of circulating currents that flow internally to the converter. Finally, a per-phase SOC balancing strategy is proposed in which per-phase power limits are well defined. Safe and quick per-phase SoC balancing is achieved while still meeting the faulty grid power demands. The proposed active power and SOC balancing strategies are discussed in Section 4.2 and Section 4.3. Section 4.4 presents the results of the proposed strategies.

### 4.1.2 Operation under asymmetric phase and arm power conditions

As mentioned in Chapter 3, each module's DC-link voltage is controlled through the bidirectional DC-DC converter (BDC). Given this scenario, the battery power in each module is not controllable through the BDC. Irrespective of the grid voltage conditions (either symmetric or asymmetric), the MMC operates symmetrically when exchanging power with the grid from the upper and lower arm perspectives. In other words, if a phase injects a certain power into the grid, it is expected that half of the power is provided by each arm. However, this operation may not be ideal under asymmetric arm power conditions. If one-quarter of the total available power in a phase is contained in one of the arms (consequently, three-quarters is available in the complimentary arm), the battery power of the arm may go above limits while providing rated power towards the grid. A similar scenario occurs if the rated power of the BESS-

MMC is not evenly split among the three phases. A generalized scenario combines both phase and arm asymmetric power conditions.

A particular case of phase and arm power asymmetry is with a different number of modules per arm/phase. If the power available in each module is the same, but $n$ number of modules are connected in the upper arm of a certain phase, and $(n - n_f)$ are connected in the lower arm, an asymmetric condition arises. This scenario may occur by design or by assuming fault-tolerant operation of the MMC where $n_f$ modules have failed and are bypassed.

Power balancing strategies can be deployed for all the mentioned scenarios to make the operation more flexible. Different control objectives can be selected while developing the power balancing strategies: 1) injecting the BESS-MMC maximum power available, 2) obtaining the same power utilization ratio with respect to its available power, 3) obtaining the same SOC utilization ratio (i.e., the batteries are charged and discharged at the same rate with respect to SOC). Among the three identified strategies, strategy 1 is the most critical as it deeply impacts the power setpoint range that the grid operator can request. Therefore, this strategy is discussed in this chapter.

Asymmetric MMC conditions have been discussed in the literature [113]-[117]. The scope of the study for BESS-MMC configurations is 1) all modules are integrated with batteries; 2) a combination of modules with integrated batteries and without batteries (only DC-link and MMC side half-bridge) [113]. Note, however, that the second scenario requires the DC-link voltage to be controlled by the grid current control, the use of energy loops to balance power, and the power of each battery to be controlled

by the BDC [113]-[117]. However, in this chapter, since the batteries' power cannot be directly controlled, power coordination is obtained using the circulating current. The proposed strategies are discussed in Section 4.4, while the results are shown in Section 4.5.

## 4.2 Phase power and SoC balancing under ac grid voltage asymmetry

If each phase has the same modulating signal, phase-shifted by $120^{\circ}$, the converter can be simplified to a voltage-source interacting with the grid (at the point of common coupling) through the filter impedance ($L_f$), as shown in Figure 4.1. Assuming that the two voltage sources are phase-shifted by $\delta$, the power that flows from the BESS to the grid in each phase is

$$P_{g,k} = \frac{V_{conv,k} V_{pcc,k} sin(\delta)}{\omega L_f}. \tag{4.1}$$

Note that, in a grid voltage asymmetry scenario, $V_{pcc,k}$ differs among the different phases. Thus, if $V_{conv,k}$ is the same for all phases, the grid active power will differ among the different phases. Because the active power is unbalanced, without properly addressing this issue, there will be an uneven use of the batteries within each phase of the converter.

Given this condition, it is possible to differentiate two ways to balance the active power among the BESS: externally to the MMC and internally to the MMC.

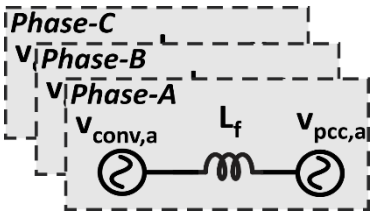



Figure 4.1. Single-phase analysis of the interaction between MMC based BESS and grid.

### 4.2.1 Balancing active power externally to the MMC

The basis for achieving active power balancing externally to the MMC involves synthesizing an unbalanced voltage at the output. For instance, if phase a ($V_{pcc,a}$) has a different magnitude than that of phases b and c ($V_{pcc,b}$ $and$ $V_{pcc,c}$), it is possible to synthesize $V_{conv,a}$ different than $V_{conv,b}$ and $V_{conv,c}$, while achieving the same $P_{g,k}$ among the different phases. In real-time control applications, this idea is implemented by decomposing the unbalanced system into three balanced systems with different sequences (positive, negative and zero). It must be noted that for the system under consideration, there is no zero-sequence path for the current to flow. Hence, the equivalent zero-sequence system is not addressed in this chapter. According to [118], the three-phase active and reactive power are

$$\begin{cases} P_g = P_0 + P_{s2}\sin(2\omega t) + P_{c2}\cos(2\omega t) \\ Q_g = Q_0 + Q_{s2}\sin(2\omega t) + Q_{c2}\cos(2\omega t) \end{cases}, \tag{4.2}$$

where $P_0$, $P_{s2}$ and $P_{c2}$ are the amplitudes of the average, sine, and cosine active power components, respectively. Further, $Q_0$, $Q_{s2}$ and $Q_{c2}$ are the amplitudes of the average, sine, and cosine reactive power components. If a system is completely balanced with only positive-sequence components, the oscillating components are not present. However, in unbalanced systems, the oscillating components appear by the interaction

between currents and voltages of different sequences. The relation [118] can be described by

$$\begin{bmatrix} P_0^* \\ Q_0^* \\ P_{c2}^* \\ P_{s2}^* \\ Q_{c2}^* \\ Q_{s2}^* \end{bmatrix} = \frac{3}{2}\begin{bmatrix} v_{pcc,d}^{+} & v_{pcc,q}^{+} & v_{pcc,d}^{-} & v_{pcc,q}^{-} \\ v_{pcc,q}^{+} & -v_{pcc,d}^{+} & v_{pcc,q}^{-} & -v_{pcc,d}^{-} \\ v_{pcc,d}^{-} & v_{pcc,q}^{-} & v_{pcc,d}^{+} & v_{pcc,q}^{+} \\ v_{pcc,q}^{-} & -v_{pcc,d}^{-} & -v_{pcc,q}^{+} & v_{pcc,d}^{+} \\ v_{pcc,q}^{-} & -v_{pcc,d}^{-} & v_{pcc,q}^{+} & -v_{pcc,d}^{+} \\ v_{pcc,d}^{-} & -v_{pcc,q}^{-} & v_{pcc,d}^{+} & v_{pcc,q}^{+} \end{bmatrix} \begin{bmatrix} i_{g,d}^{+*} \\ i_{g,q}^{+*} \\ i_{g,d}^{-*} \\ i_{g,q}^{-*} \end{bmatrix}, \tag{4.3}$$

where, the subscripts $d, q$ indicate direct and quadrature components on the synchronously rotating reference frame (SRF), and the superscripts $+, -$ indicate either positive or negative sequence components. From (4.3), it is possible to calculate current setpoints for different objectives: 1) constant reactive power (by setting $Q_{s2}^*$ and $Q_{c2}^*$to zero); 2) constant active power (by setting $P_{s2}^*$ and $P_{c2}^*$ to zero); 3) inject only positive sequence current to the grid ($i_{g,d}^{-*} = i_{g,q}^{-*} = 0$), thus having oscillating components in both grid active power and reactive power.

By selecting the constant active power objective, the current setpoints that would draw the same grid active power among the different phases of the converter can be obtained. This strategy is selected in order to externally balance the power of the MMC based BESS. The structure that controls both positive and negative sequence currents is shown in Figure 4.2. Furthermore, to obtain the positive and negative sequence voltages, the dual second order generalized integrator frequency-locked loop (DSOGI-FLL) with a positive/negative sequence calculator is utilized [119].

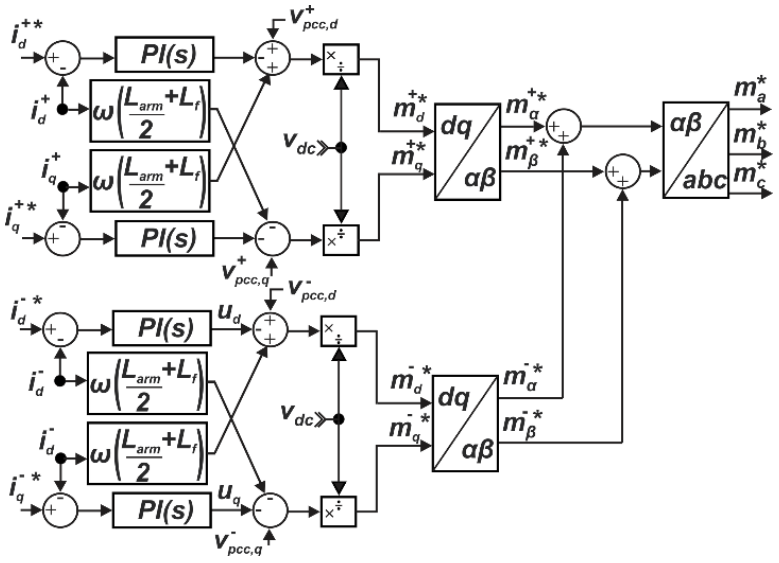



Figure 4.2. Positive and negative-sequence grid current control.

It must be pointed out that the above-mentioned strategy cannot fully balance the phase active power, but it can mitigate. This is due to the fact that asymmetric currents flow during the operation. Thus, the power losses internally to the MMC are different among the phases. Therefore, the per-phase SOC will eventually deviate if the system operates at this grid adverse scenario for an extended period.

### 4.2.2 Balancing active power internally to the MMC

Regardless of the grid current control objective (LVRT strategy) selected, the MMC can internally balance the average active power by making use of the DC component of the circulating current. For instance, if $P_{g,a} \neq P_{g,b} \neq P_{g,c}$, it is possible to redistribute the power through $P_{dc,a}$, $P_{dc,b}$ and $P_{dc,c}$, in such a way that the overall phase power, $P_a$, $P_b$ and $P_c$ are equal. However, it may be noted that these expressions are only concerning the single-phase average values of the per-phase power at BESS and grid sides. Furthermore, the per-phase BESS power can be obtained as a function of the

redistributed power as well as the power that is injected to the grid by the phase. Therefore, the overall expression is

$$P_k = P_{dc,k} + P_{g,k}, \tag{4.4}$$

where

$$P_k = \underbrace{\overline{\sum_{j=1}^{n} v_{sm_{u,j}} \cdot i_{sm_{u,j}}}}_{upper\ arm} + \underbrace{\overline{\sum_{j=1}^{n} v_{sm_{l,j}} \cdot i_{sm_{l,j}}}}_{lower\ arm}. \tag{4.5}$$

In (4.5), the bar superscript indicates the average value. In real-time, (4.5) is obtained by multiplying the module's voltage and current and by making use of moving-average filters (MAF). Figure 4.3 illustrates the interaction among the different powers from the aforementioned discussions.

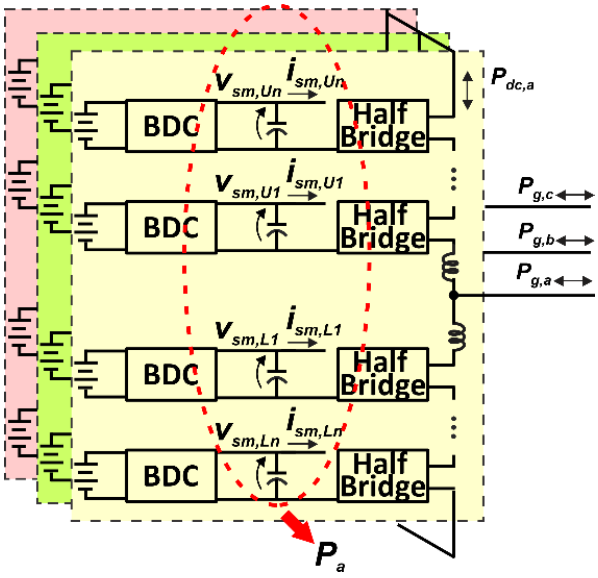



Figure 4.3. Average active power flow for the MMC based BESS.

It should also be highlighted that the DC component of the circulating current must meet the condition defined by

$$\sum_{k=a,b,c} i_{dc,k} = 0. \tag{4.6}$$

It follows from (4.6) that

$$\sum_{k=a,b,c} P_{dc,k} = 0. \tag{4.7}$$

The DC power reference in each phase is calculated by tracking the mismatch between the average power of the BESS and the actual power of a specific phase. The power reference is

$$\Delta P_k = \frac{P_a + P_b + P_c}{3} - P_k. \tag{4.8}$$

A PI-controller is utilized to regulate the power mismatch, by outputting the dc circulating current reference $i^*_{dc,k}$. Finally, this current reference is utilized in the circulating-current control which uses a high bandwidth current loop with a PI controller thus tracking the DC-circulating current reference and suppressing the most significant circulating current harmonic component [120], [121]. Figure 4.4 shows the steps to obtain the current reference, while Figure 4.5 illustrates the designed control structure.

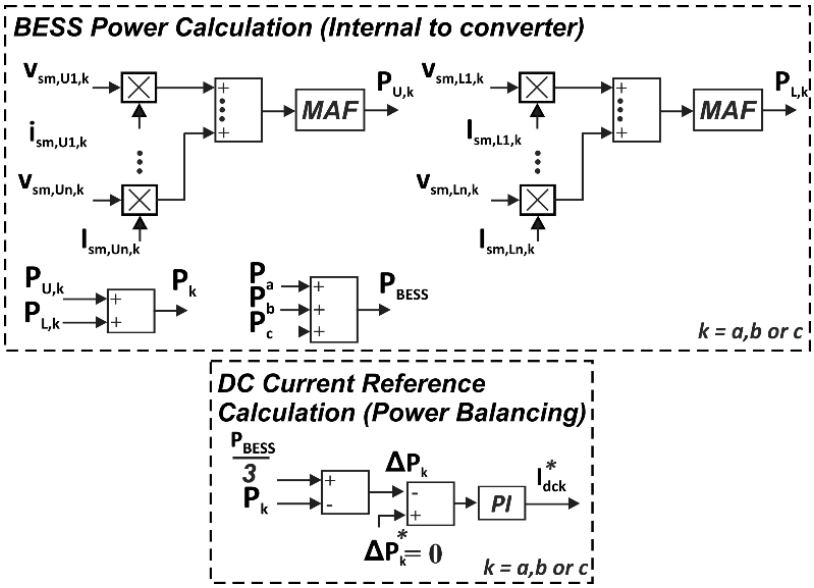



Figure 4.4. Active power balancing reference calculation.

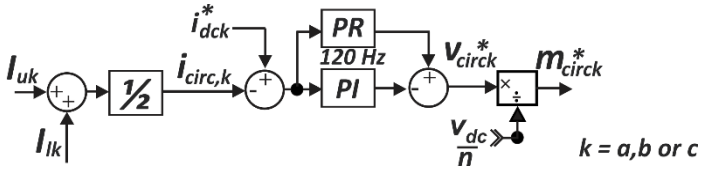



Figure 4.5. Circulating-current control structure.

The proposed strategy is valid if the per-phase power does not surpass its maximum limit during the grid-adverse scenario, thus grid-current limiters need to be employed.

### 4.2.3 Proposed SOC-balancing strategy with per-phase power limiter

The previous strategies can be employed for scenarios in which the per-phase SOC is balanced, and a grid-voltage asymmetry condition is present. However, per-phase SOC balancing would be required if the grid-adverse scenario starts and the per-phase SOC has deviated. As such, instead of calculating the active power mismatch and regulating it to zero through DC active power ($P^*_{dc,k}$), a SOC balancing strategy can be

deployed by intentionally promoting the per-phase average active power to be different among phases. Similar to the power balancing strategy shown in Section 4.2.2, the dc circulating current is utilized to perform the SOC balancing, thus (4.6) and (4.7) must be met.

The per-phase SOC deviation for a given phase k from the BESS average SOC is

$$\Delta SOC_k = \frac{SOC_a + SOC_b + SOC_c}{3} - SOC_k, \tag{4.9}$$

where the per-phase average SOC for any given phase k is calculated as

$$SOC_k = \left( \underbrace{\sum_{j=1}^{n} SOC_{u,j}}_{upper\ arm} + \underbrace{\sum_{j=1}^{n} SOC_{l,j}}_{lower\ arm} \right) \Big/ 2n. \tag{4.10}$$

The SOC balancing strategy takes place if at least one of the deviations is greater than the threshold defined by the accuracy of the SOC estimator. The estimation relies on the battery chemistry, mathematical model, and estimation method. The accuracy has been found to be as low as less than 0.25% for LiFePO4 batteries [122]. For this work, it is assumed that the SOC accuracy is 0.5%. As such, if all per-phase SOC deviations are less than this value, no SOC balancing is performed (in case of grid-voltage asymmetry, active power balancing is performed instead). It should be pointed out that once the threshold requirement to start the SOC balancing is met, and a single phase has deviation below the threshold, it will still be employed in the SOC balancing scheme.

From (4.9), if $\Delta SOC_k > 0$, phase $k$ needs to be charged. Conversely, if $\Delta SOC_k < 0$, phase $k$ provides power to the remaining phases. Based on this, two conditions are possible: 1) two phases charge while one discharges; 2) one phase charges while two discharge.

Different from the per-phase SOC balancing strategies presented in [84], [111], and [112], the developed strategy is based on the average active power available in each phase ($P_{lim,k}$).

The available power is

$$P_{\lim,k} = \pm\frac{P_{BESS,rated}}{3} - P_{g,k}, \tag{4.11}$$

where $P_{BESS,rated}$ is the BESS' rated active power. Therefore, for the following analysis, the power values are the same for the three-phases, however, different values amongst the phases can also be set. Furthermore, the sign of this variable flips according to $\Delta SOC$. If the phase charges, $P_{BESS,rated}/3$ has a negative sign, while it would have a positive sign if the phase discharges.

In each phase, the per-phase grid average active power is

$$P_{g,k} = \frac{3}{2}\left(v_{conv,k_\alpha} i_{g,k_\alpha} + v_{conv,k_\beta} i_{g,k_\beta}\right). \tag{4.12}$$

The components in the $\alpha\beta$-stationary reference frame are obtained by making use of the quadrature signal generators based on the SOGI structure [119].

After identifying the power available for each phase, $P^*_{dc,k}$ is set according to the flowchart shown in Figure 4.6. Further, the actual value for $P_{dc,k}$ and the DC circulating

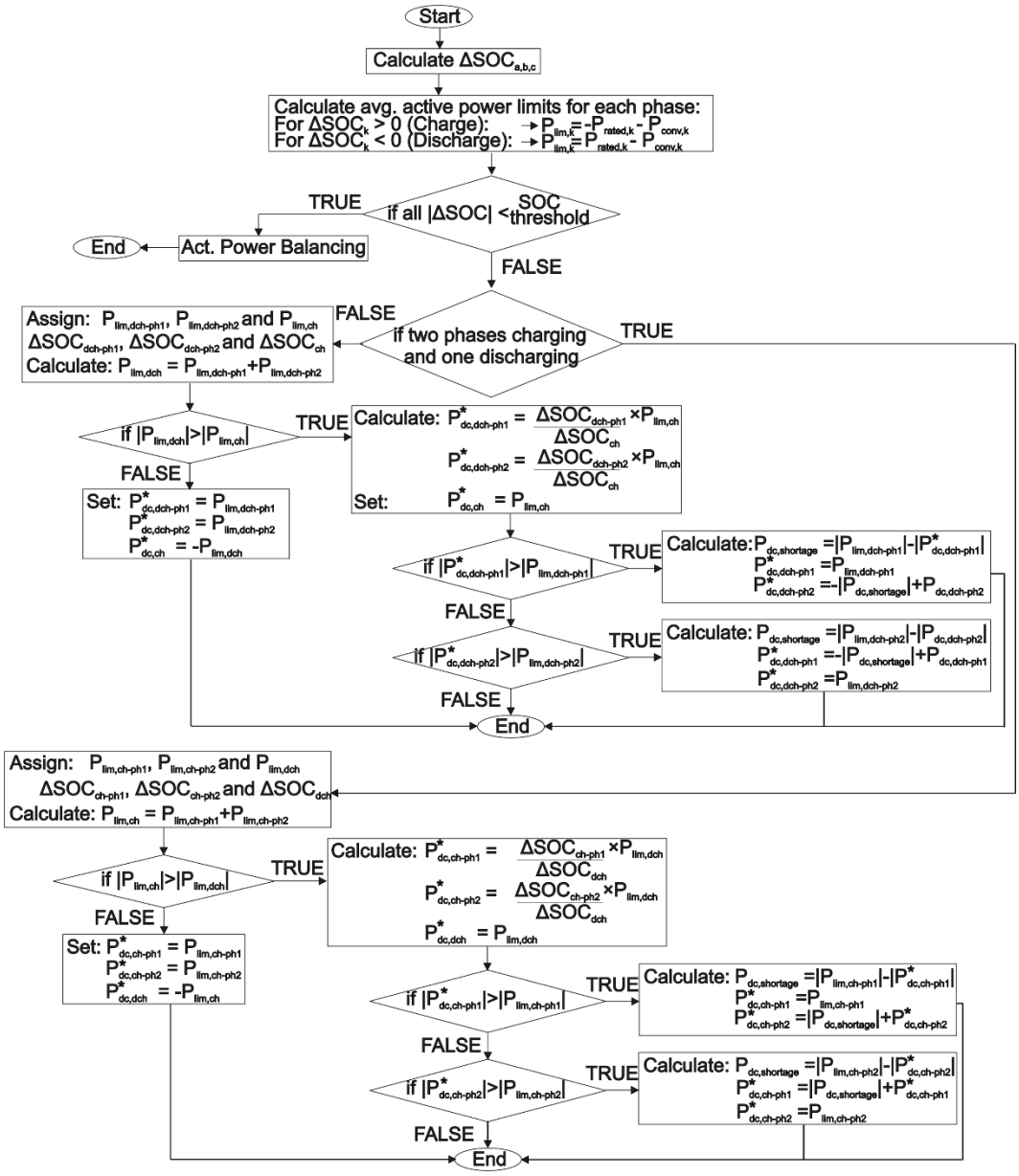



Figure 4.6. Per-phase SOC balancing flowchart.

current reference are calculated as shown in Figure 4.7. Note that the strategy utilizes all the available power and is limited by (4.7). Thus, it can safely perform the per-phase SOC balancing at the fastest condition possible (power margins can be provided by slightly modifying (4.11) thus giving higher flexibility to the strategy). Furthermore,

since the grid-power conditions are continuously monitored, the reference setpoints are updated in real-time in case grid-power setpoints are modified.

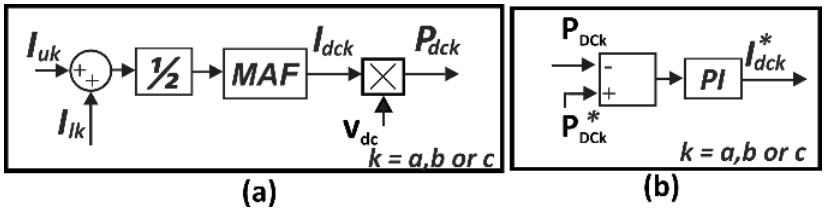



Figure 4.7. (a) DC circulating power reference calculation; (b) balancing flowchart DC circulating current reference calculation.

### 4.3 Arm power transfer under ac grid voltage asymmetry

In the previous chapter, the arm power transferred is discussed for the purposes of sizing the module's DC-link capacitor. The strategy utilized is first presented in [87]. The arm power transfer occurs through the interaction of the circulating current and synthesized arm voltage concerning the grid. In a more general way, the synthesized AC voltages concerning the grid have positive and negative sequence components (which are inherent during the operation under asymmetric grid voltage conditions). The voltages are:

$$\begin{cases} v_{u,a}(t) = -v_{l,a}(t) = V_p \cos\left(\omega t + \varphi^{(p)}\right) + V_n \cos\left(\omega t + \varphi^{(n)}\right) \\ v_{u,b}(t) = -v_{l,b}(t) = V_p \cos\left(\omega t + \varphi^{(p)} - 2\pi/3\right) + V_n \cos\left(\omega t + \varphi^{(n)} + 2\pi/3\right), \\ v_{u,c}(t) = -v_{l,c}(t) = V_p \cos\left(\omega t + \varphi^{(p)} + 2\pi/3\right) + V_n \cos\left(\omega t + \varphi^{(n)} - 2\pi/3\right) \end{cases} \quad (4.13)$$

where $V_p$ and $V_n$ are the amplitudes of the positive and negative sequence components, respectively. Furthermore, $\varphi^{(p)}$ and $\varphi^{(n)}$ represent the phase displacement of the positive and negative sequence voltages, respectively. In addition, the circulating currents are also defined as having positive and negative sequence components. These circulating components guarantee that the current does not flow through a fourth wire

in case a DC-link is connected across the positive and negative poles of the MMC. The circulating currents are

$$\begin{cases} i_{circ,a} = I_p \cos\left(\omega t + \gamma^{(p)}\right) + I_n \cos\left(\omega t + \gamma^{(n)}\right) \\ i_{circ,b} = I_p \cos\left(\omega t + \gamma^{(p)} - 2\pi/3\right) + I_n \cos\left(\omega t + \gamma^{(n)} + 2\pi/3\right) \\ i_{circ,c} = I_p \cos\left(\omega t + \gamma^{(p)} + 2\pi/3\right) + I_n \cos\left(\omega t + \gamma^{(n)} - 2\pi/3\right) \end{cases}, \tag{4.14}$$

where $I_p$ and $I_n$ are the amplitudes of the positive and negative sequence components, respectively. Furthermore, $\gamma^{(p)}$ and $\gamma^{(n)}$ represent the phase displacement of the positive and negative sequence currents, respectively.

In [87], only positive sequence voltages are considered. Furthermore, $\varphi^{(p)}$ is assumed to be zero. Therefore, the arm's active power transferred in each phase are

$$\begin{cases} P_{\Delta a} = \dfrac{V_p I_p}{2}\cos\left(\gamma^{(p)}\right) + \dfrac{V_p I_n}{2}\cos\left(\gamma^{(n)}\right) \\ P_{\Delta b} = \dfrac{V_p I_p}{2}\cos\left(\gamma^{(p)}\right) + \dfrac{V_p I_n}{2}\cos\left(\gamma^{(n)} - 2\pi/3\right) \\ P_{\Delta c} = \dfrac{V_p I_p}{2}\cos\left(\gamma^{(p)}\right) + \dfrac{V_p I_n}{2}\cos\left(\gamma^{(n)} + 2\pi/3\right) \end{cases}. \tag{4.15}$$

Similarly, the reactive power transferred in each phase are

$$\begin{cases} Q_{\Delta a} = -\dfrac{V_p I_p}{2}\sin\left(\gamma^{(p)}\right) - \dfrac{V_p I_n}{2}\sin\left(\gamma^{(n)}\right) \\ Q_{\Delta b} = -\dfrac{V_p I_p}{2}\sin\left(\gamma^{(p)}\right) - \dfrac{V_p I_n}{2}\sin\left(\gamma^{(n)} - 2\pi/3\right) \\ Q_{\Delta c} = -\dfrac{V_p I_p}{2}\sin\left(\gamma^{(p)}\right) - \dfrac{V_p I_n}{2}\sin\left(\gamma^{(n)} + 2\pi/3\right) \\ \sum Q = -\dfrac{3}{2} V_p I_p \sin\left(\gamma^{(p)}\right) \end{cases}. \tag{4.16}$$

Rearranging the abovementioned expressions, the circulating current references are calculated by

$$\begin{bmatrix} P_{\Delta a} \\ P_{\Delta b} \\ P_{\Delta c} \\ \sum Q \end{bmatrix} = A \begin{bmatrix} I_p \cos(\gamma^{(p)}) \\ I_p \sin(\gamma^{(p)}) \\ I_n \cos(\gamma^{(n)}) \\ I_n \cos(\gamma^{(n)}) \end{bmatrix}, \tag{4.17}$$

where

$$A = V_p \begin{bmatrix} 1 & 0 & 1 & 0 \\ 1 & 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 1 & 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ 0 & -3 & 0 & 0 \end{bmatrix}. \tag{4.18}$$

Note that if negative sequence voltage is present, a power mismatch from the expected value occurs. Defining $\alpha = V_n/V_p$, the arm power deviation from the expected value can be observed for different $\alpha$ and $\varphi^{(n)}$ conditions in Figure 4.8.

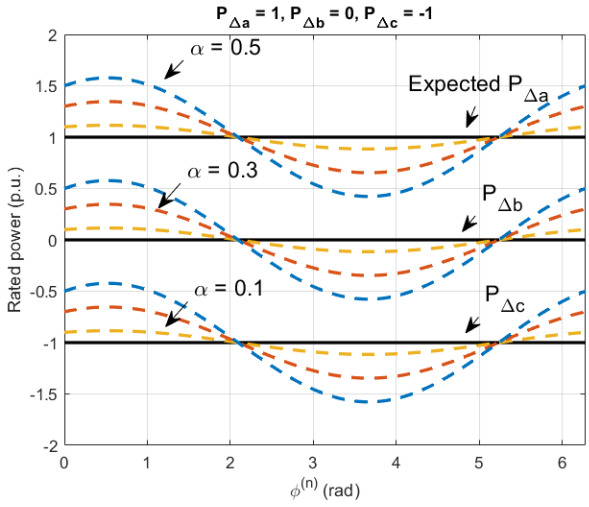



Figure 4.8. Arm power transfer deviation from expected value for different conditions.

A solution for the problem can be found if the negative sequence voltage is considered, leading to a new *A* matrix, defined as

$$A = \frac{V_p}{2}\begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \end{bmatrix}, \tag{4.19}$$

where:

$$\begin{aligned}
a_{11} &= \cos(\varphi^{(p)}) + \alpha\cos(\varphi^{(n)}), \\
a_{21} &= \cos(\varphi^{(p)}) - \frac{\alpha}{2}\cos(\varphi^{(n)}) + \frac{\alpha\sqrt{3}}{2}\sin(\varphi^{(n)}), \\
a_{31} &= \cos(\varphi^{(p)}) - \frac{\alpha}{2}\cos(\varphi^{(n)}) - \frac{\alpha\sqrt{3}}{2}\sin(\varphi^{(n)}), \\
a_{41} &= 3\sin(\varphi^{(p)}), \\
a_{12} &= \sin(\varphi^{(p)}) + \alpha\sin(\varphi^{(n)}), \\
a_{22} &= \sin(\varphi^{(p)}) - \frac{\alpha}{2}\sin(\varphi^{(n)}) - \frac{\alpha\sqrt{3}}{2}\cos(\varphi^{(n)}), \\
a_{32} &= \sin(\varphi^{(p)}) - \frac{\alpha}{2}\sin(\varphi^{(n)}) + \frac{\alpha\sqrt{3}}{2}\cos(\varphi^{(n)}), \\
a_{42} &= -3\cos(\varphi^{(p)}), \\
a_{13} &= \cos(\varphi^{(p)}) + \alpha\cos(\varphi^{(n)}), \\
a_{23} &= \frac{-\cos(\varphi^{(p)})}{2} - \frac{\sqrt{3}}{2}\sin(\varphi^{(p)}) + \alpha\cos(\varphi^{(n)}), \\
a_{33} &= \frac{-\cos(\varphi^{(p)})}{2} + \frac{\sqrt{3}}{2}\sin(\varphi^{(p)}) + \alpha\cos(\varphi^{(n)}), \\
a_{43} &= 3\alpha\sin(\varphi^{(n)}), \\
a_{14} &= \sin(\varphi^{(p)}) + \alpha\sin(\varphi^{(n)}), \\
a_{24} &= \frac{-\sin(\varphi^{(p)})}{2} + \frac{\sqrt{3}}{2}\cos(\varphi^{(p)}) + \alpha\cos(\varphi^{(n)}), \\
a_{34} &= \frac{-\sin(\varphi^{(p)})}{2} - \frac{\sqrt{3}}{2}\cos(\varphi^{(p)}) + \alpha\cos(\varphi^{(n)}), \\
a_{44} &= -3\alpha\cos(\varphi^{(n)}).
\end{aligned} \tag{4.20}$$

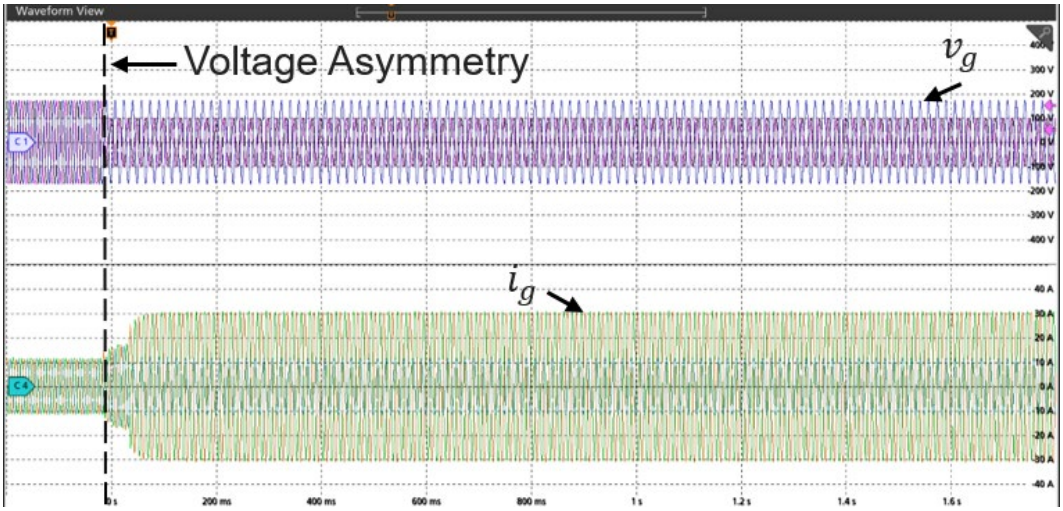
### 4.4 Controller hardware-in-the-loop results for asymmetric grid voltage scenarios

To validate the strategies, a downscaled BESS-MMC is implemented using the same C-HIL setup described in Chapter 3. A three-phase low voltage ($120V_{Ln,rms}$/60 Hz) grid system is considered. The complete parameters for the BESS-MMC are the same as shown in Table 3.2. The battery capacity is 0.033Ah, selected to speed-up the SOC deviation for this study.

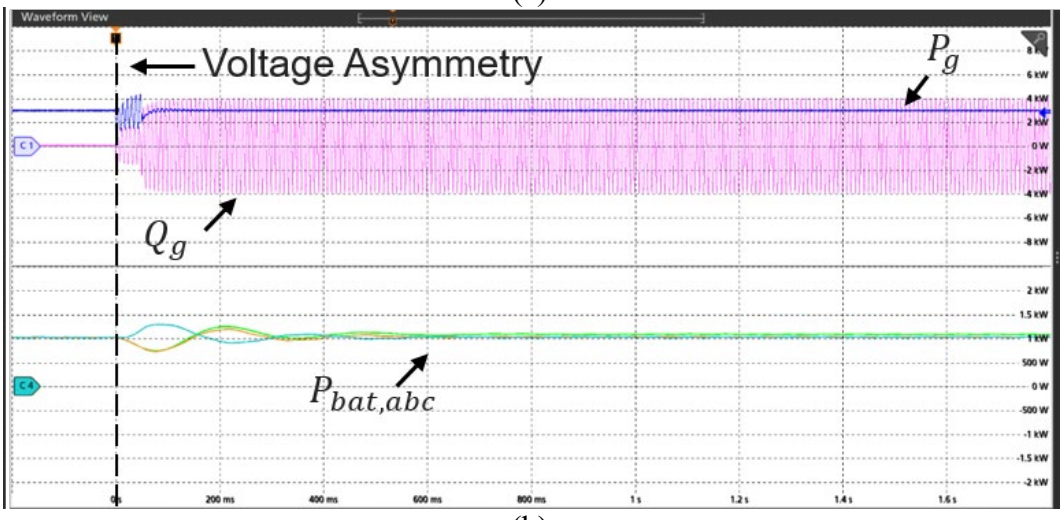
Two control target scenarios are considered to validate the proposed strategies. In both scenarios, the BESS is operated at rated power when a grid voltage asymmetry is introduced. The scenarios are: 1) $P_g^* = 3\,kW$and $Q_g^* = 0\,var$, with constant active power control (external power balancing) and balanced average per-phase SOC at 65%. 2) $P_g^* = 3\,kW$ and $Q_g^* = 3\,kvar$, with balanced grid-currents, with internal power balancing and without power balancing. The balanced average per-phase SOC at 65%.

Results for scenario 1 are shown in Figure 4.9. The power mismatch among the converter phases can be limited while maintaining the grid active power constant during grid voltage asymmetry. A small transient in the grid active power can be observed immediately after the asymmetry starts. This is due to the detection of the grid fault detector, which takes about 50 ms to take However, it must be pointed out that the mismatch cannot be entirely suppressed as power losses in each phase are different (given that the amplitude of grid currents in each phase are different), thus eventually deviating the SOC.

By introducing the internal power balancing strategy (Figure 4.10), the power deviation is limited, which leads to a balanced SOC operation.



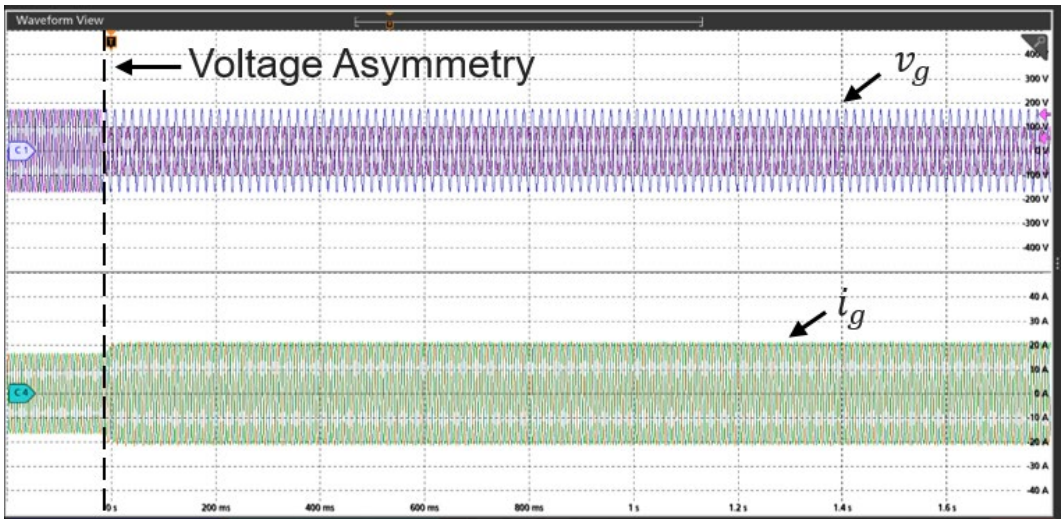

(a)



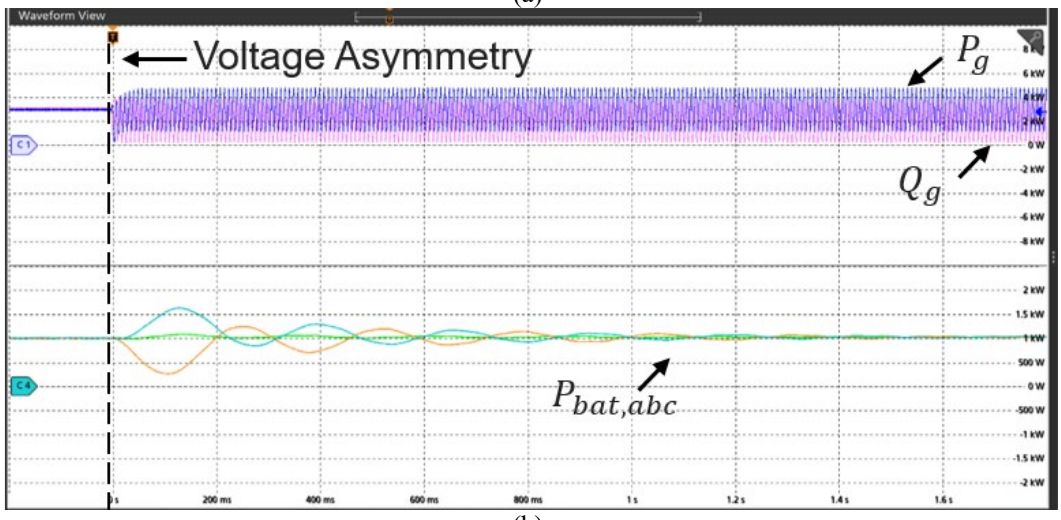

(b)

Figure 4.9. Scenario 1 - External power balancing. (a) Grid voltages (100V/div) and grid currents (10 A/div); (b) Grid active and reactive power (2 kW/div) and per-phase battery power (0.5 kW/div).

A third scenario, shown in Figure 4.11, is considered to assess the performance of the developed SOC-balancing strategy (assuming $SOC_a$= 0.8, $SOC_b$= 0.65 and $SOC_c$= 0.6). As soon as the asymmetry starts the power setpoints is $P_g^* = 3kW$ and $Q_g^* = 0\,kvar$. During this procedure, the positive-sequence injection LVRT strategy is utilized (balanced grid-currents), which leads to different average active power values in each phase (shown in Figure 4.11(a)). Regarding SOC balancing, three different SOC-balancing operation points are identified after the initial faulty scenario condition.



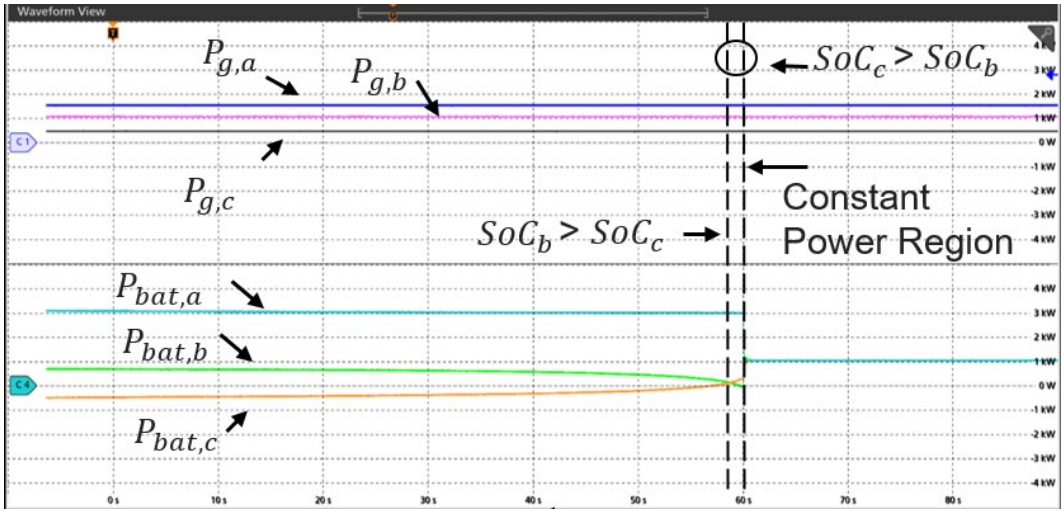

(a)



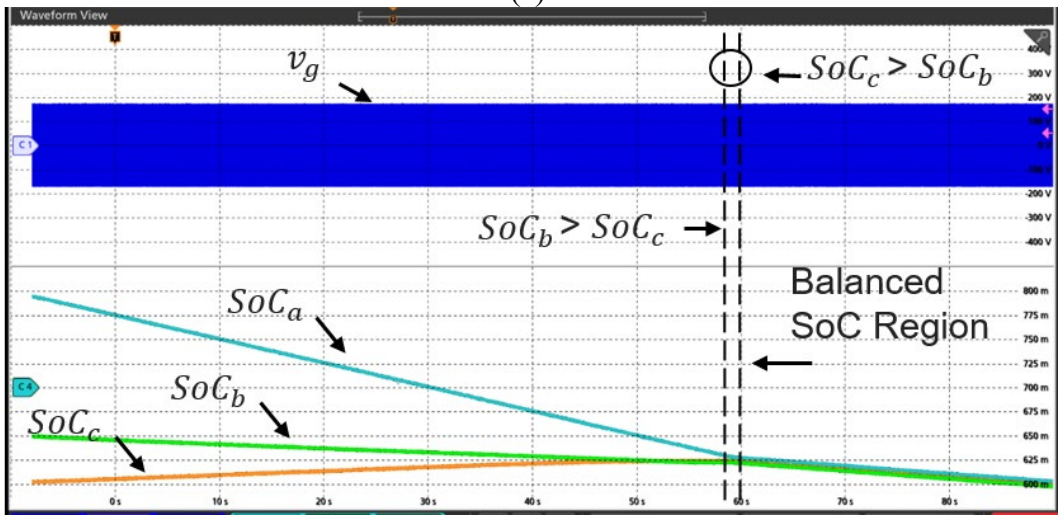

(b)

Figure 4.10. Scenario 2 - Internal power balancing. (a) Grid voltages (100V/div) and grid currents (10 A/div); (b) Grid active and reactive power (2 kW/div) and per-phase battery power (0.5 kW/div).

Region I: Figure 4.11(b) indicate the following SOC deviations: $\Delta SOC_a < 0$ (discharge), $\Delta SOC_b > 0$ (charge), and $\Delta SOC_c < 0$ (charge). Based on the grid average active power measurements shown in Figure 4.11(a), $P^*_{dc,k}$ for each phase is identified based on the proposed balancing structure. Figure 4.11(a) shows that phase A discharges at its rated value, whereas the remaining phases that absorb power from phase A charge at a slower rate.




(a)




(b)

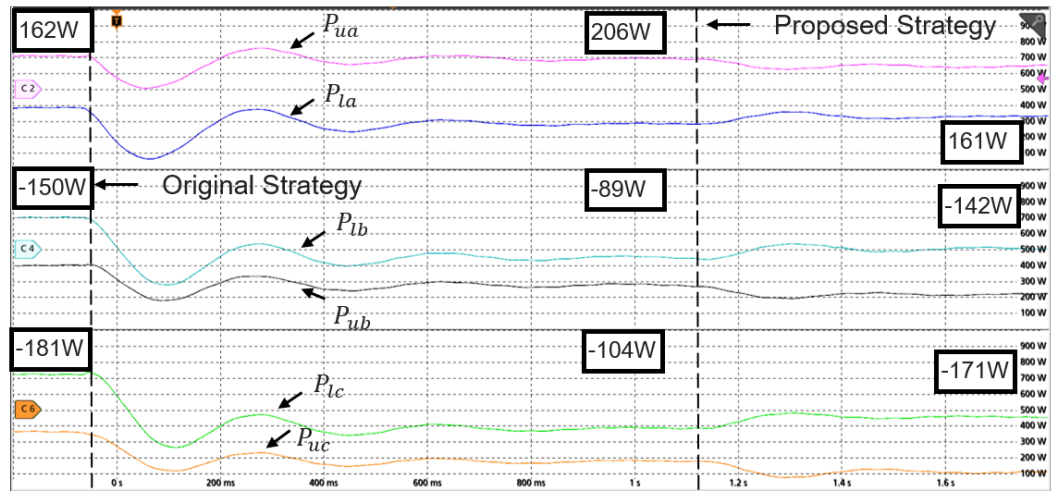
Figure 4.11. Scenario 3 – SoC balancing. (a) Per-phase grid average active power (1 kW/div) and per-phase battery power (1 kW/div); (b) Grid voltages (100V/div) and per-phase SOC (0.025/div).

Region II: While in Region I, $SOC_b > SOC_c$, in Region II $SOC_c > SOC_b$. During this region, phase C starts to be charged at a faster rate than phase B, as indicated in Figure 4.11(a). Note that only $P^*_{dc,a}$ setpoint for SOC balancing is still the same as in Region I.

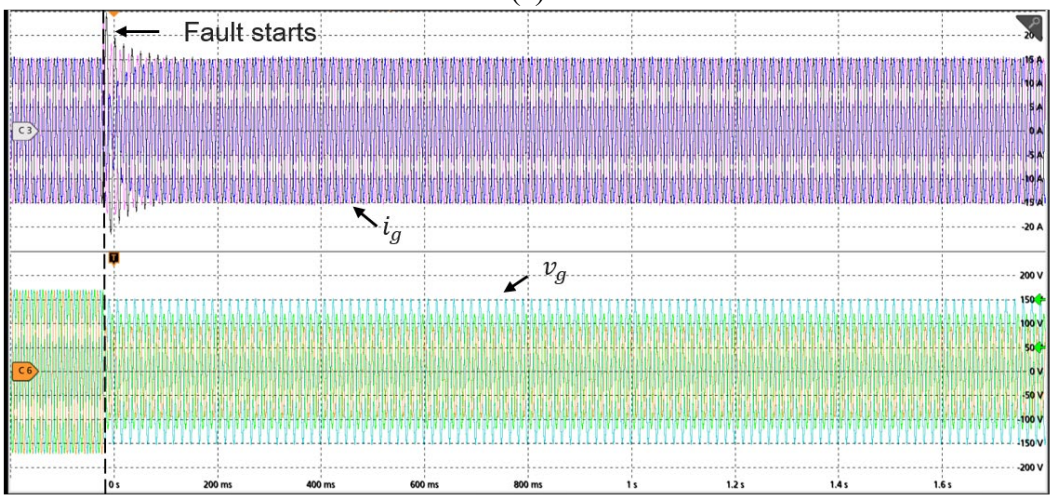
Region III: All SOC variations are within the 0.5% threshold. Therefore, no per-phase SOC balancing is performed. However, since the grid-voltage asymmetry is still present, the power balancing strategy (internal to the converter) is employed.

It can be seen from Figure 4.11(a) that the power for each phase did not exceed its rated limit with the proposed algorithm.

Finally, Figure 4.12 showcases the arm power transfer strategy during the grid voltage asymmetry. The setpoints for this scenario are $P_{\Delta a} = 150W$, $P_{\Delta b} = -150W$, $P_{\Delta C} = -150W$, and $\Sigma Q = 0\ var$. At some point, a grid voltage asymmetry starts, and the positive sequence injection (balanced currents) LVRT strategy is utilized. Before the asymmetry starts, the maximum deviation from the desired setpoint occurs in phase C, where 31 W from the expected power transfer setpoint is observed. This significant deviation can be assigned to round-up errors during the calculation of setpoints within DSP. The original strategy is still utilized as soon as the asymmetry starts. This leads to a maximum deviation of 61 W from the expected -150W in phase B. Phases A and C also observe a significant error, with 56 W and 54 W mismatch. This leads to almost 33% error during the voltage asymmetry while using the original strategy. Finally, the proposed method is implemented. The arm power transfer mismatch is 11 W for phase A, 8 W for phase B, and 21 W for phase C. This is a significant reduction and validates that the proposed strategy can improve the arm power transfer reference tracking during the grid voltage asymmetry.




(a)




(b)

Figure 4.12. Arm power transfer during grid voltage asymmetry. (a) Arm power transfer (100W/div); (b) Grid voltages (100V/div) and per-phase SOC (0.025/div).

### 4.5 Power balancing under asymmetric phase and arm power conditions

The scenarios discussed in Chapter 3 and Section 4.2 of this chapter assume that the battery power available in each phase and arm is the same. However, asymmetric conditions can occur in power available in each phase, each arm, and each module within the arm. In this chapter, asymmetry in the first two cases is addressed through the circulating current control.

To inject the maximum power available in the BESS-MMC to the utility grid, power must be transferred from the phase and arms with higher available power to the ones with lower available power. The following subsections discuss the battery power transfer setpoints.

### 4.5.1 Available phase power asymmetry

The phase power asymmetry scenario assumes that the power available in a particular phase, $P_{\mathrm{lim},k}$ ($k = a, b$ or $c$), is numerically different from the others. If no phase power transfer is performed, the maximum power that could be injected into the grid is

$$P_g = 3\eta_g \min\left(P_{\mathrm{lim},a}, P_{\mathrm{lim},b}, P_{\mathrm{lim},c}\right), \tag{4.21}$$

where $\eta_g$ is the efficiency of the grid active power transfer (from the battery to the point of common coupling). To inject the actual maximum power available, phase power must be transferred. The phase power transfer is

$$P_{dc,k} = \frac{\left(P_{\mathrm{lim},a} + P_{\mathrm{lim},b} + P_{\mathrm{lim},c}\right)}{3} - P_{\mathrm{lim},k}. \tag{4.22}$$

The new power available in each phase ($P'_{\mathrm{lim},k}$) is

$$\begin{cases} P'_{\mathrm{lim},k} = P_{\mathrm{lim},k} + P_{dc,k}\eta_{dc,k} & \rightarrow \text{if phase absorbing} \\ P'_{\mathrm{lim},k} = P_{\mathrm{lim},k} + P_{dc,k} & \rightarrow \text{if phase injecting} \end{cases}, \tag{4.23}$$

where $\eta_{dc,k}$ is the efficiency of the phase power transfer (assuming that phase $k$ absorbs power).

Finally, the grid active power setpoint is

$$P_g^* = 3\eta_g \left( \min\left( P'_{\text{lim},a}, P'_{\text{lim},b}, P'_{\text{lim},c} \right) \right). \tag{4.24}$$

### 4.5.2 Available arm power asymmetry

The arm power asymmetry scenario assumes that the power available in any arms ($P_{\text{lim},uk}$ and $P_{\text{lim},lk}$) is numerically different. If no arm power transfer is performed, the maximum power that could be injected into the grid is

$$P_g = 6\eta_g \left( \min\left( P_{\text{lim},ua}, P_{\text{lim},ub}, P_{\text{lim},uc}, P_{\text{lim},la}, P_{\text{lim},lb}, P_{\text{lim},lc} \right) \right). \tag{4.25}$$

To inject the actual maximum power available, arm power must be transferred. The arm power transfer is

$$P_{\Delta k} = P_{\text{lim},uk} - \frac{\left( P_{\text{lim},uk} + P_{\text{lim},lk} \right)}{2}, \tag{4.26}$$

where $P_{\Delta k}$ is the power transfer from the upper to the lower arm of phase $k$. The new power available in each arm is

$$\begin{cases} P'_{\text{lim},uk} = P_{\text{lim},uk} - P_{\Delta k} \\ P'_{\text{lim},lk} = P_{\text{lim},lk} + P_{\Delta k}\eta_{\Delta k} \end{cases} \rightarrow \text{if upper arm providing}$$
$$\begin{cases} P'_{\text{lim},uk} = P_{\text{lim},uk} - P_{\Delta k}\eta_{\Delta k} \\ P'_{\text{lim},lk} = P_{\text{lim},lk} + P_{\Delta k} \end{cases} \rightarrow \text{if upper arm absorbing}, \tag{4.27}$$

where $\eta_{\Delta k}$ is the efficiency of the arm power transfer in phase $k$.

Finally, the grid active power setpoint is

$$P_g^* = 6\eta_g \left( \min\left( P'_{\text{lim},ua}, P'_{\text{lim},ub}, P'_{\text{lim},uc}, P'_{\text{lim},la}, P'_{\text{lim},lb}, P'_{\text{lim},lc} \right) \right). \tag{4.28}$$

### 4.5.3 Combined available phase and arm power asymmetry (general scenario)

The scenarios described in the previous subsections can occur at the same time. When this occurs, the superposition theorem can be applied. This is only possible because the phase power transfer is performed with DC circulating current, while the arm power transfer is performed with AC circulating current. The grid active power setpoint for the generalized scenario is the same as presented in (4.29). However, the available power in each arm is now described as

$$\begin{cases} P'_{\text{lim},uk} = P_{\text{lim},uk} - P_{\Delta k} + 0.5P_{dc,k}\eta_{dc,k} \\ P'_{\text{lim},lk} = P_{\text{lim},lk} + P_{\Delta k}\eta_{\Delta k} + 0.5P_{dc,k}\eta_{dc,k} \end{cases}. \tag{4.29}$$

### 4.5.4 Asymmetry caused by different number of modules

When considering a different number of modules, such as a post-module failure, an inherent phase, and arm power asymmetry are present. Nevertheless, the setpoints for phase and arm power transfer, obtained in the previous subsections, are still applicable.

As discussed in Section 4.1.2, assuming that $n_f$ modules have failed in an arm, only $(n - n_f)$ modules are available. For a BESS-MMC, this results in a DC-link voltage in each module change from $V_{dc}/n$ to $V_{dc}/(n - n_f)$. Accordingly, if a bidirectional DC-DC converter interfaces the DC-link and the battery, the maximum

number of failed modules so that the BESS-MMC is still fully operational is obtained by

$$n_{f,\max} \le n - \text{ceil}\left(\frac{V_{dc}}{G_{\max} V_{oc}}\right), \tag{4.30}$$

where $G_{\max}$ is the maximum gain of the bidirectional converter and $V_{oc}$ is the battery voltage. For the bidirectional converter considered in this dissertation, $G_{max} = 4$.

### 4.5.5 The role of the power transfer efficiency

The power transfer equations obtained in the previous subsections consider the efficiency of each power transfer (grid, phase, and arm). Furthermore, the efficiency varies depending on the different operational conditions. Examples of how efficiency can be impacted are scenarios with a unity power factor and non-unity power factor. For the asymmetric number of modules scenario, the efficiency of the bidirectional converter may significantly change depending on the voltage gain. For maximizing the active power that can be transferred, information related to the efficiency in each type of transfer is required. However, this information may be challenging to obtain. Alternatively, assumptions concerning efficiency can be made. Specifically, if efficiency details are not available, it is essential to assume a lower efficiency to guarantee that the power limits of the batteries are not surpassed.

## 4.6 Controller hardware-in-the-loop results for asymmetric power conditions

Two scenarios are considered for the validation of the strategies presented in Section 4.5. The first scenario assumes grid phase power asymmetry, while the second

scenario assumes arm power asymmetry. The power available in each arm for both scenarios are presented in

Table 4.1. The efficiency assumptions are presented in Table 4.2. Finally, the overall BESS-MMC parameters are shown in Table 4.3.

Table 4.1 Available arm power

| **Parameter** | **Scenario 1** | **Scenario 2** |
|---|---|---|
| $P_{\mathrm{lim},ua}$ | 1.4 kW | 1.4 kW |
| $P_{\mathrm{lim},la}$ | 1.4 kW | 1.4 kW |
| $P_{\mathrm{lim},ub}$ | 1 kW | 1.4 kW |
| $P_{\mathrm{lim},lb}$ | 1 kW | 1.4 kW |
| $P_{\mathrm{lim},uc}$ | 1.2 kW | 1 kW |
| $P_{\mathrm{lim},lc}$ | 1.2 kW | 1.8 kW |

Table 4.2 Power transfer efficiency

| **Parameter** | **Value** |
|---|---|
| $\eta_{\mathrm{DC}}$ | 0.94* |
| $\eta_{\Delta\mathrm{k}}$ | 0.94* |
| $\eta_{\mathrm{g}}$ | 0.96* |

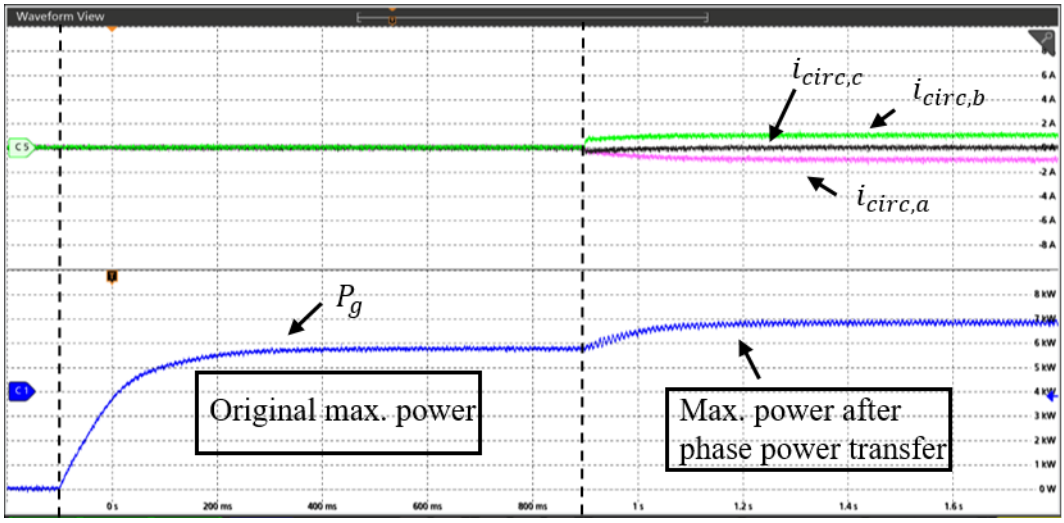
*Includes BDC efficiency

Table 4.3 BESS-MMC Parameters

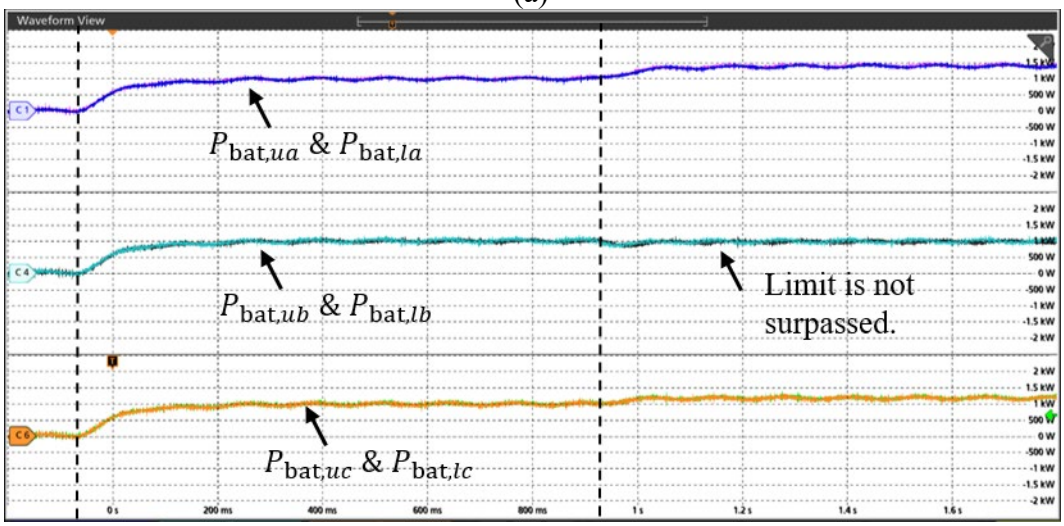
| Parameter | Parameter description | Specification |
|---|---|---|
| | ***MMC-side*** | |
| $v_g$ | Grid phase voltage | 120 $V_{RMS}$ |
| $L_{AC} + L_{arm}/2$ | MMC equivalent inductance | 2 mH |
| $R_{AC} + R_{arm}/2$ | MMC equivalent resistance | 75 $m\Omega$ |
| $n$ | Number of SMs per arm | 2 |
| $V_{DC}$ | DC-link voltage (Total MMC) | 400 $V_{DC}$ |
| - | ***Bidirectional converter-side*** | |
| $L_{dc}$ | BDC inductance | 560$\mu$H |
| $R_T$ | BDC equivalent series resistance | 0-1Ω (0.5Ω nom.) |
| $V_{oc}$ | Battery open-circuit voltage | 102.4 Vdc |
| $d$ | Duty ratio | 0.4-0.6 (0.5 nom.) |

Figure 4.13 shows the result for the phase power transfer scenario. Phase C has the same average as the total power available from the BESS-MMC, i.e., $P_{dc,c} = 0$. However, according to (4.22), $P_{dc,a} = -400$ W and $P_{dc,b} = 400$ W. Note that according to the notation adopted for the circulating current, negative $P_{dc,k}$ indicates that phase $k$ sources power to the other phases. The power that is transferred from phase A to phase B is calculated according to (4.22), where new $P_{\text{lim},a}$, and $P_{\text{lim},b}$ are obtained.

Finally, the grid active power setpoint $P_g^*$ is calculated based on (4.24). Figure 4.13(a) initially highlights the original maximum power available based on the minimum phase power, calculated by (4.21). Afterward, the phase power transfer starts




(a)

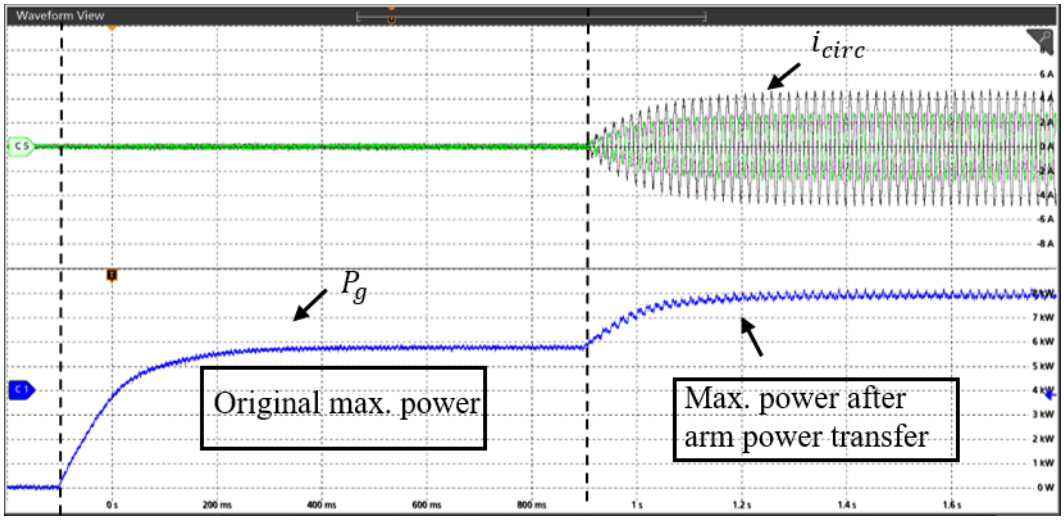



(b)

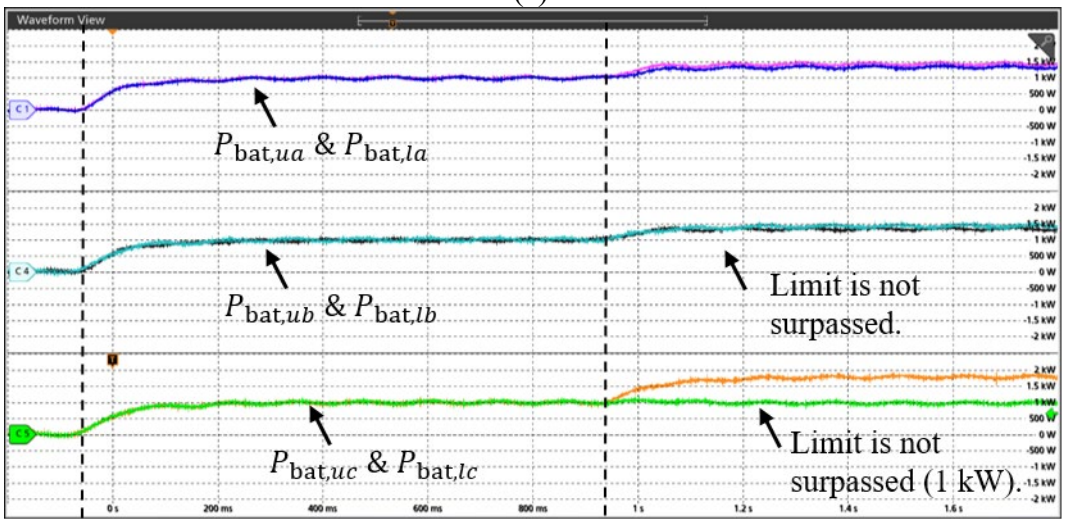
Figure 4.13. Scenario 1 – Phase power balancing to achieve maximum power transfer to the utility grid. (a) Circulating current (2 A/div) and grid active power (1 kW/div); (b) Battery power in each arm (0.5 kW/div).

to allow more power to be injected into the grid. Figure 4.13(b) shows that the battery power limits in each arm are not surpassed.

According to Table 4.1, the BESS-MMC in the second scenario does not contain phase power asymmetry. However, it can be observed that Phase C has arm power asymmetry. Therefore, arm power transfer is required to achieve the maximum grid active power.




(a)




(b)

Figure 4.14. Scenario 2 – Arm power balancing to achieve maximum power transfer to the utility grid. (a) Circulating current (2 A/div) and grid active power (1 kW/div); (b) Battery power in each arm (0.5 kW/div).

According to (4.26), $P_{\Delta c} = 400$ W, which indicates that the upper arm of phase C transfers active power to its corresponding lower arm. The new limits for $P_{\mathrm{lim},uc}$, and $P_{\mathrm{lim},lb}$ are calculated as described in (4.27). Finally, the grid active power setpoint $P_g^*$ is calculated based on (4.28). Figure 4.14(a) initially highlights the original maximum power available based on the minimum arm power, calculated by (4.25). Afterward, the

arm power transfer allows more power to be injected into the grid. Figure 4.14(b) shows that the battery power limits in each arm are not surpassed.

## 4.7 Conclusion

This chapter proposes control strategies to balance the active power and the per-phase SOC of a BESS-MMC operating under asymmetric grid voltage conditions. This strategy ensures resilient operation of BESS by maintaining uniform SOC among the battery modules distributed in each phase. Power balancing strategies are performed using controlled power exchange with grid and internal phase power exchange of converter. External balancing technique is achieved by maintaining constant three-phase active power. However, this LVRT strategy leads to mismatched internal losses, thus causing SOC deviation over a long period. This issue can be completely suppressed by internally balancing the power through the DC-circulating current (power). Balancing power internally has the advantage of allowing any LVRT strategy to be utilized. Finally, the DC-circulating power can also be used for per-phase SOC balancing under defined active power constraint limits. Based on the unbalanced grid active power information for each phase, the per-phase SOC balancing is performed based on power availability, which speeds up the balancing procedure.

Finally, this chapter also proposes power balancing strategies to achieve the maximum power available from the BESS-MMC to the electrical grid. The proposed strategies make use of both DC-circulating currents for phase power transfer and AC-circulating currents for arm power transfer. The power setpoints are calculated considering the efficiency of the power transfer strategies, thus avoiding that the battery operates above its rated limits. The BESS-MMC is implemented in Typhoon HIL604,

while the control and the proposed power management strategies are implemented with TI DSP28335 control cards.

### 4.8 Publications

- J. M. L. Fonseca, S. R. P. Reddy, K. Rajashekara and K. Raj, "Active Power and SOC Balancing Techniques for Resilient Battery Energy Storage Systems under Asymmetric Grid Voltage Scenarios," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 947-954, doi: 10.1109/APEC42165.2021.9487407.
- J. M. L. Fonseca, S. R. P. Reddy, K. Rajashekara, "Analysis of Internal Power Flow of BESS-MMC under grid voltage asymmetry" *IEEE Transactions on Circuits and Systems II: Express Briefs (to be submitted).*

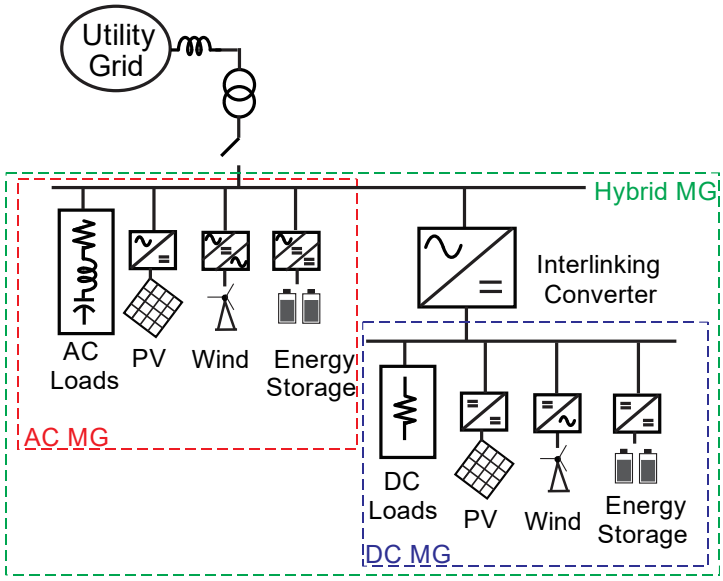
# 5. POWER MANAGEMENT STRATEGIES FOR HYBRID AC/DC MICROGRID WITH MMC BASED INTERLINKING CONVERTER INTEGRATED WITH BESS

## 5.1 Introduction

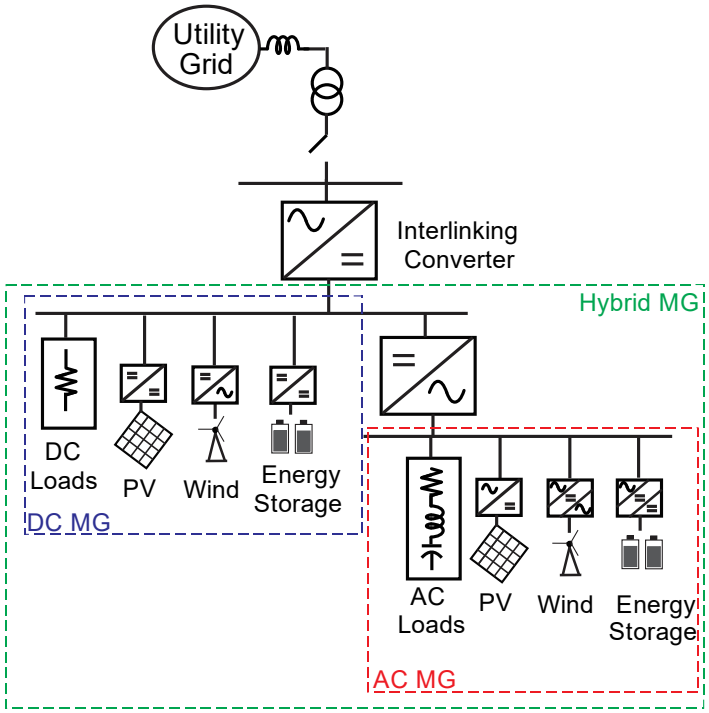
For the past few years, there has been a significant advancement in the grid integration of energy storage systems and renewable energy resources (RERs) [123], [124]. Most of the research focuses on AC microgrids since these microgrids can be developed from the existing structure/technology (transformers, protection devices, etc.) already available for the utility grid, with better feasibility in implementation. However, AC microgrids require synchronization of the RERs, multiple conversion stages, and there is an inherent circulation of reactive power. To increase the efficiency of connecting DC energy sources and overcome the limitations of AC microgrids, DC microgrids have also been explored. However, installing DC microgrids requires significant modification to the grid structure, thereby significantly increasing the cost. Combining both AC and DC microgrids would facilitate the connection of both AC and DC-based RERs, loads, and energy storage. Therefore, hybrid microgrids (HMG) can potentially be a less expensive alternative to implementing DC microgrids.

Given the relative novelty of the topic, several possible HMG architectures are explored in the literature. In [123], different types of HMG architectures are classified in an effort to identify trends and the different research contribution focus. The most common architectures are: coupled AC and decoupled AC. This classification relates to whether the utility AC grid is directly connected to the AC microgrid (coupled AC) or

connected through AC/DC-DC/AC stages (decoupled AC). Figure 5.1 shows the two types of HMG. To connect the DC microgrid to the AC microgrid and AC utility grid, the coupled AC HMG utilizes an interlinking converter (IC), as shown in Figure 5.1(a).




(a)




(b)

Figure 5.1. Commonly studied Hybrid Microgrid architectures. (a) Coupled AC; (b) Decoupled AC.

However, Figure 5.1(b) shows that for the decoupled HMG architecture, the AC/DC IC connected to the AC utility grid decouples both microgrids. An additional DC/AC converter is required to form the AC microgrid. For a HMG of the same power, one key disadvantage of using the decoupled AC HMG is that the AC/DC IC has to process the power of both AC and DC microgrid instead of only the AC microgrid. Although Figure 5.1 shows full galvanic isolation for both coupled and decoupled AC, partial isolation is also possible to reduce transformer sizing. Research papers that utilize coupled AC HMG architectures mainly focus on energy management, sizing, and system-level stability analysis [123]. For decoupled AC, the focus changes to the topology of the IC, its operation, and efficiency [123], [125], [126].

In HMG, battery energy storage system (BESS) connection is limited to either DC or AC microgrids, when 2-level Voltage Source Converters (2L-VSC) are employed as interlinking converters [127]. However, with the use of modular multilevel converter (MMC) topologies, there are additional ports available for integrating more DC output-based energy sources. One of the main MMC topologies, and the one considered throughout this dissertation, is the Double-Star Chopper Cell (DSCC). For HMG, the major advantage of utilizing DSCC as the MMC topology is that it allows low voltage BESS integration directly to the IC, instead of having to utilize either high voltage batteries or high gain bidirectional DC-DC converters (BDC).

Although several research papers focus on the MMC topology with the integration of ES, there is a limited discussion on its application towards HMGs, where both AC and DC generation and loads are present. According to [128], the power management strategies that are applicable to HMG architectures under utility grid-

connected (dispatched and undispatched modes) and islanded modes need to be evaluated. In [83], [107], the power flow from DC to AC side (and vice-versa) are discussed, while [84] goes further by extending the operation of such a system by considering grid fault scenarios. However, power coordination between AC and DC microgrids is not discussed. Further, operation under islanded conditions and related power management strategies are also not addressed.

This chapter proposes the use of an MMC based IC for a hybrid AC/DC microgrid. The chapter focuses on 1) increasing the resiliency of the MMC based IC for HMG and 2) analyzing the proposed power management strategies for the architecture under study. To achieve that, Section 5.2 provides the main details of the proposed architecture and control strategies for the operation under grid-connected and islanded modes. Section 5.3 proposes the power management strategies for the HMG under grid-connected and islanded modes. For validation purposes, Section 5.4 provides controller hardware-in-the-loop results of the implementation of the HMG within the Typhoon HIL environment. Finally, the conclusions are presented in Section 5.5.

## 5.2 Control strategies for the MMC based IC

The HMG architecture shown in Figure 5.2 is capable of operating in both grid-connected and islanded modes. Loads and RERs are connected in both DC and AC grids. One of the key aspects of the DSCC control is related to the module's DC-link voltage regulation. With the addition of the ES elements connected through a BDC (as shown in Figure 5.2), the DC-link capacitor voltage of each module is regulated by the DC-DC converter within the IC modules. This is the same strategy utilized in Chapters 3 and 4, which is selected based on the reduced communication requirements and no

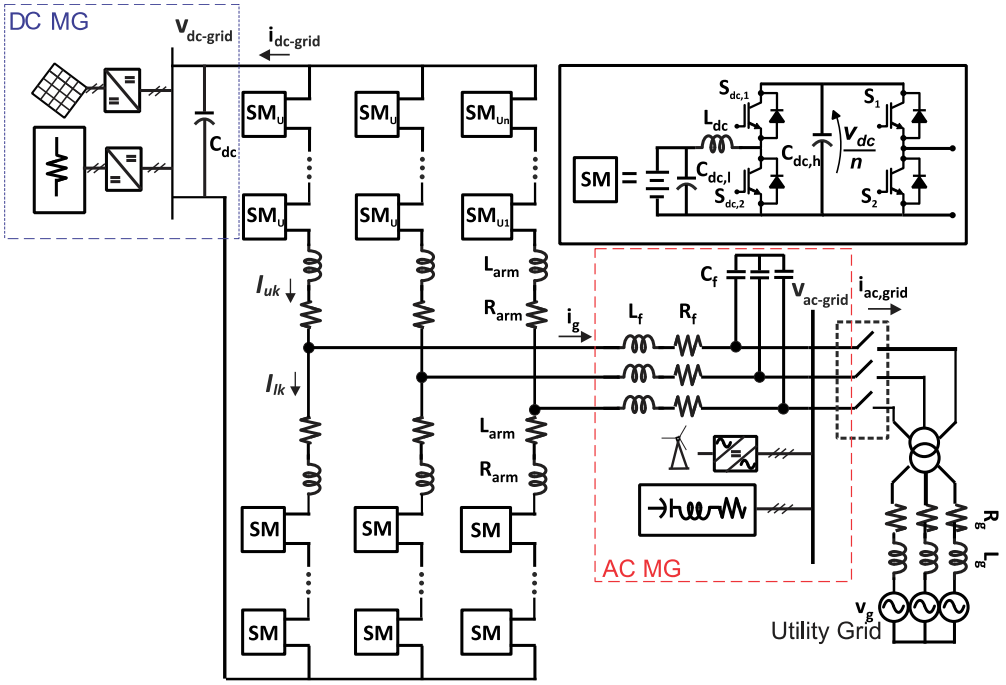



Figure 5.2. Hybrid AC/DC microgrid under study.

need for additional energy control loops/sorting algorithms. Similar to the previous chapters, the battery power is not regulated through the module. However, in this scenario, the power is now indirectly selected based on the power demand of both AC and DC microgrids.

During islanded mode, the utility AC grid is not available. Therefore, an AC grid-forming converter needs to be employed to create the AC grid. This can be either from AC microgrid RERs or through the IC itself. Since the grid-forming converter requires a reliable active source, the IC with integrated ES would be an obvious choice to operate as AC grid forming. Therefore, because of the simplicity to realize the control in both grid forming and grid-following modes, the strategy that utilizes the batteries/DC-DC converters to regulate the individual module's capacitor voltage is chosen. During any operating mode, the IC can be utilized to regulate the DC microgrid

voltage. In contrast to ICs based on 2L-VSC, the DC and AC microgrids are decoupled since the DSCC topology has two degrees of freedom (AC grid currents and circulating currents), as shown in Figure 5.3 and Figure 5.4.

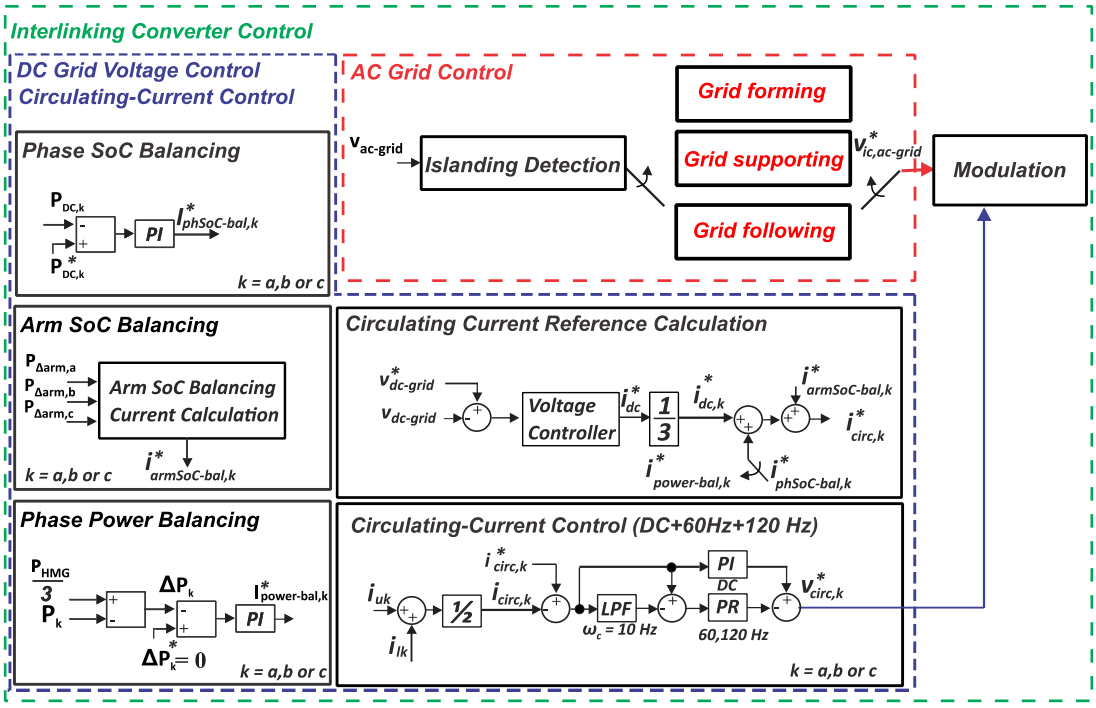



Figure 5.3. Interlinking converter control scheme.

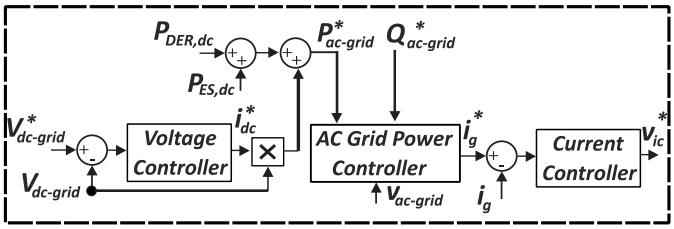



Figure 5.4. Interlinking converter control scheme.

The decoupling effect is guaranteed by making sure that the AC microgrid power steps do not affect the DC microgrid voltage. Alternatively, the DC microgrid power steps should not affect the AC microgrid. The metric utilized to observe decoupling is through the individual module's DC-link voltage. When a power step on either

microgrid happens, the DC-link voltage should not be affected. Therefore, the bandwidths of the DC grid voltage control loop, the AC grid power loop (in utility grid-connected mode), and the AC voltage loop (in grid-islanded mode) must be slower than that of the bidirectional converter's voltage loop.

According to Figure 5.3, the DC microgrid voltage regulation is performed through the circulating current control. The voltage controller outputs the current reference for regulating the DC microgrid voltage. This current can be equally split between the three phases of the MMC based IC if symmetrical use of each phase is preferred for the regulation. In addition to the DC microgrid voltage control, the circulating current control contains the following strategies to improve the resiliency of the IC: 1) SoC balancing (per-phase [85], inter-arm [87], and intra-arm), 2) Power balancing (per-phase) [85], and 3) Faulty SM circulating current suppression for asymmetric faulty SM operation [51].

The AC grid control selects the mode of operation according to the availability of the utility grid and the services to be performed. This can be split between grid-following (GFL), grid-forming (GFM), and grid-supporting modes (GSP). This includes PQ control with a low-voltage ride through capability (GFL) [118], V-f control with and without droop controls (GFM) [118], and virtual synchronous generator (VSG) emulation (GSP) with droop control loops [129]. In this chapter, both grid-following mode and grid-forming mode are considered for operations under utility grid-connected mode and grid islanded mode, respectively.

The modulating signals for the IC are the same as presented in Chapter 3. For convenience, they are also described in this chapter. Therefore, the modulating signals for the BESS-MMC are

$$\begin{cases} m^*_{u,k} = -m^*_k + m^*_{circ,k} + \dfrac{1}{2} \\ m^*_{l,k} = m^*_k + m^*_{circ,k} + \dfrac{1}{2} \end{cases}, \tag{5.1}$$

where $m_k$ and $m_{circ,k}$ are the normalized modulating signals related to the grid current control and circulating current control, respectively.

### 5.2.1 Grid following control

During grid-connected mode, the IC can operate in grid-following (PQ control). The control schematic for this operation mode is shown in Figure 5.5. To increase reliability, besides basic operation with the AC grid, low-voltage ride (LVRT) through strategies may be required during faulty AC grid scenarios. During these scenarios, several possibilities related to the control of the IC are possible. Positive sequence injection (PSI) and balanced 3-phase AC grid active power strategies are among the popular control objectives [118]. They both utilize positive and negative sequence current control. Another possible approach is the positive and negative sequence injection (PNSI), which may be a good option for compensating unbalanced loads in weak grids (high short circuit ratio). It should be pointed out that the DC microgrid voltage should not be affected during these scenarios.

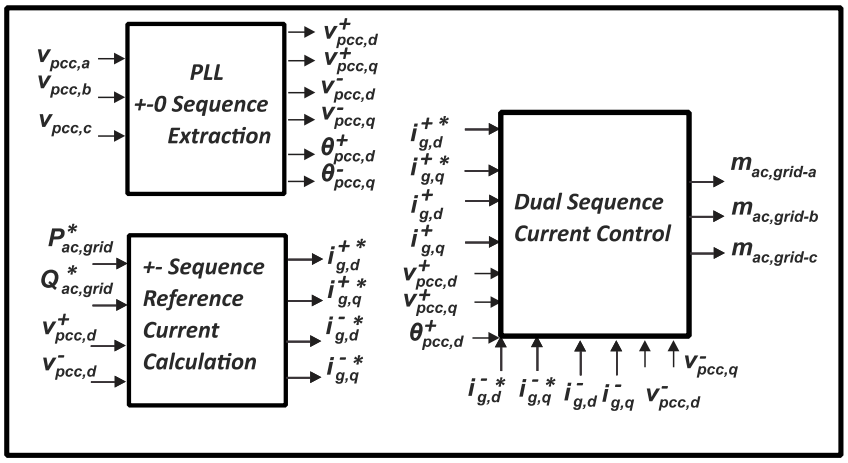



Figure 5.5. IC control under grid-connected mode (PQ control with positive and negative sequence current control).

### 5.2.2 Grid forming control

During grid-forming mode, the IC operates in V-f control. As such, both microgrids are formed by the same converter. This is one of the key features of utilizing the MMC with integrated ES as an IC. The power exchange between AC and DC microgrids is indirectly controlled by the IC. This means that there is no power balancing command that needs to be sent to the IC. Instead, the battery power within the IC and its state-of-charge (SoC) need to be monitored and sent to higher-level (microgrid) controls.

The control structure of the V-f control is shown in Figure 5.6. Note that positive and negative sequence voltage control is required as unbalanced loads may be connected. The negative-sequence voltage control regulates the negative-sequence voltage to zero in order to obtain balanced AC-grid voltages. Furthermore, note that because of the modular fashion in which the batteries are connected to the IC, the connection of unbalanced loads on the AC grid leads to power deviation in each phase of the IC. Ultimately, this result can cause per-phase SoC deviation. As such, the circulating current needs to be employed to balance out the power in each phase.

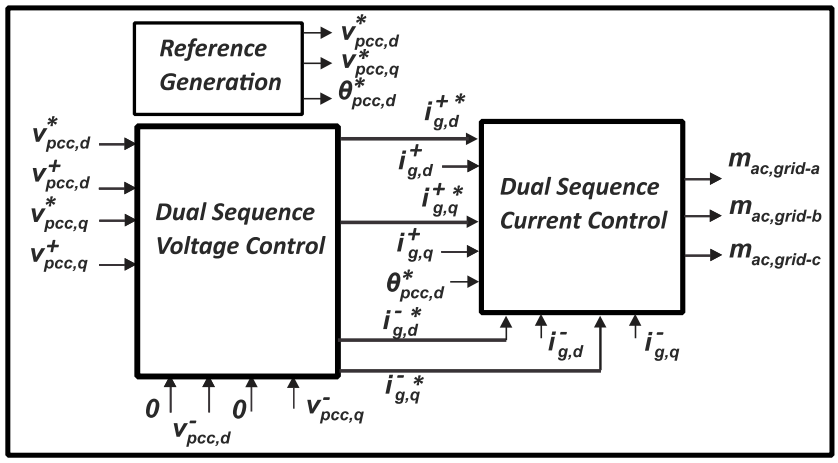



Figure 5.6. IC control under grid-islanded mode (V-f control with positive-negative sequence voltage and current control).

## 5.3 Power management strategies for the proposed HMG structure

The HMG may operate in either utility grid-connected (dispatched or undispatched) or islanded mode. The main difference relates to the different power coordination strategies, which focus on the power exchange between microgrids, IC, and the utility grid.

For this architecture, the net power of both AC and DC grids are

$$P_{AC} = P_{AC,GEN} + P_{AC,LOAD} \tag{5.2}$$

and

$$P_{DC} = P_{DC,GEN} + P_{DC,LOAD}, \tag{5.3}$$

where $P_{AC,GEN}$ and $P_{DC,GEN}$ represent the generation on the AC and DC side, respectively. Loads on AC and DC sides are represented by $P_{AC,LOAD}$ and $P_{DC,LOAD}$ respectively. Note that generation is assumed to be positive, while loads are assumed to be negative. The rating of the MMC based interlinking converter is defined as $P_{MMC}$. Assuming that the

generation capability in either microgrid is greater than their respective loads, the active power rating of the interlinking converter is

$$\boldsymbol{P_{MMC} = \max\left(P_{AC,GEN}, P_{DC,GEN}\right) + P_{BAT},} \tag{5.4}$$

where $P_{BAT}$ is the overall rating of the batteries coupled to the MMC and defined as:

$$\boldsymbol{P_{BAT} = \sum_{\beta=1}^{6n} P_{BAT,m_\beta},} \tag{5.5}$$

where $n$ is the number of modules in each arm and $P_{BAT,m}$ is the rated power of an individual battery pack connected to an MMC module. Further, the active power exchange between the interlinking converter and AC microgrid is defined as $P_{IC}$. It should be emphasized that the previous set of equations implies that the power rating of the interlinking converter can differ from the power rating of the batteries connected to it. Another consideration is that the batteries are capable of charging and discharging at the same rate.

In this chapter, any non-dispatchable power source (at either DC or AC microgrid) is operated under maximum power point (MPPT) or controlled PQ mode. For RERs connected to the DC microgrid, the power would naturally flow towards the ES within the IC unless the power is transferred to the AC side through the AC power loop (when the IC operates under PQ control). If the power ratings of the batteries are not surpassed, the AC grid can also be used to charge the batteries. Finally, in islanded conditions, the IC forms both DC and AC microgrids. As such, the power output of the IC is not regulated. This requires power coordination between the RERs and loads so that the system does not operate over its specified limits. Figure 5.7 summarizes the power

management overview for each scenario. In this chapter, two possible scenarios are addressed: utility grid-connected undispatched power mode and islanded mode.

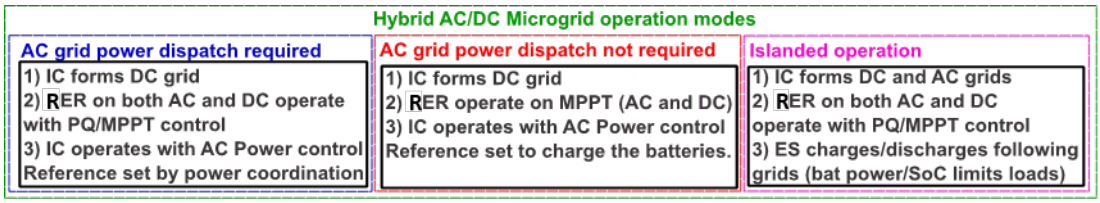



Figure 5.7. Overview of power management of the hybrid AC/DC microgrid under study.

### 5.3.1 Utility grid-connected undispatched power mode

During utility grid-connected undispatched power mode, the batteries can charge unrestrictedly. The generation on DC and AC microgrid sides can operate under peak power tracking. As such, the only power setpoint that must be defined in every situation is the interlinking converter AC grid power exchange, $P_{IC}$. This value must be set according to the DC microgrid power at which the batteries are to be charged. Figure 5.8 indicates the power setpoint for the interlinking converter for every possible scenario.

| $SoC_{BESS}$>=80% | |
|---|---|
| $P_{DC}$>0 | $P_{DC}$<0 |
| $P_{IC}$ injects $P_{DC}$surplus to utility grid | $P_{IC}$ absorbs $P_{DC}$deficit from utility grid |

(a)

| $SoC_{BESS}$<80% | | |
|---|---|---|
| $P_{DC}$>0 | | $P_{DC}$<0 |
| $P_{DC}$-$P_{BAT}$>=0 | $P_{DC}$-$P_{BAT}$<0 | |
| $P_{IC}$ injects ($P_{DC}$-$P_{BAT}$) to utility grid to abide battery power limits. | $P_{IC}$ absorbs ($P_{DC}$-$P_{BAT}$) from utility grid to charge battery at rated value. | $P_{IC}$ absorbs $P_{DC}$-deficit and $P_{BAT}$ from utility grid to supply DC loads and charge battery at rated value. |

(b)

Figure 5.8. Power management strategies for utility grid-connected undispatched power mode. (a) High SoC; (b) Low SoC.

### 5.3.2 Islanded mode

During islanded mode, the interlinking converter power is not controlled on both AC and DC sides, as it is forming both grids, i.e., the MMC is regulating both the DC microgrid voltage and the AC microgrid voltage and frequency. Therefore, to guarantee the system stability and ensure that the battery power is operated within its limits, the AC and DC-side generation need to be well controlled. Furthermore, in case generation is not available, the battery needs to be sized in such a way that it is capable of supplying power to essential loads for a certain period. To extend the period in which essential loads are powered, non-essential loads must be shed as the SoC of the batteries reduce. In this chapter, it is assumed that only essential loads are powered when $SoC_{BESS} < 80\%$. Shedding must also occur in scenarios where the AC and DC generation is not capable of fully powering the non-essential loads. Figure 5.9 shows a possible power management strategy that can be employed for this architecture.

| $P_{DC}+P_{AC}<0$ | | |
|---|---|---|
| $P_{BAT}+P_{DC}+P_{AC}>0$ | $P_{BAT}+P_{DC}+P_{AC}<0$ | |
| | $SoC_{BESS}>80\%$ | $SoC_{BESS}<80\%$ |
| $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ peak power track | Non-essential load shedding | $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ peak power track |

(a)

| $P_{DC}+P_{AC}>0$ | | | | |
|---|---|---|---|---|
| | $SoC_{BESS}>80\%$ | $SoC_{BESS}<80\%$ | | |
| | | $P_{DC}>P_{BAT}$ | $P_{DC}<P_{BAT}$ | |
| $P_{DC}>0$<br>$P_{AC}>0$ | $P_{DC,gen}$ supplies DC load<br>$P_{AC,gen}$ supplies AC load | $P_{DC,gen}$ supplies battery and DC loads<br>$P_{AC,gen}$ supplies AC loads | $P_{AC}>P_{DC}-P_{BAT}$ | $P_{AC}<P_{DC}-P_{BAT}$ |
| | | | $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ supplies battery and AC loads | $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ peak power track |

(b)

| $P_{DC}+P_{AC}>0$ | | | |
|---|---|---|---|
| | $SoC_{BESS}>80\%$ | $SoC_{BESS}<80\%$ | |
| | | $P_{DC}+P_{AC}>P_{BAT}$ | $P_{DC}+P_{AC}<P_{BAT}$ |
| $P_{DC}<0$<br>$P_{AC}>0$ | $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ supplies AC and remaining DC loads | $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ supplies battery AC and DC loads | $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ peak power track |

(c)

| $P_{DC}+P_{AC}>0$ | | | |
|---|---|---|---|
| | $SoC_{BESS}>80\%$ | $SoC_{BESS}<80\%$ | |
| | | $P_{DC}+P_{AC}>P_{BAT}$ | $P_{DC}+P_{AC}<P_{BAT}$ |
| $P_{DC}>0$<br>$P_{AC}<0$ | $P_{DC,gen}$ supplies DC and remaining AC loads<br>$P_{AC,gen}$ peak power track | $P_{DC,gen}$ supplies battery AC and DC loads<br>$P_{AC,gen}$ peak power track | $P_{DC,gen}$ peak power track<br>$P_{AC,gen}$ peak power track |

(d)

Figure 5.9. Power management strategies for islanded mode. (a) HMG sinking; HMG sourcing: (b) Both DC and AC sourcing. (c) DC sinking and AC sourcing. (d) DC sourcing and AC sinking.

## 5.4 Hardware-in-the-loop validation

For the following results, an MMC based IC with battery power ($P_{BAT}$) of 6 kW is considered. The MMC is comprised of 2 modules per arm. The batteries have a nominal voltage of 100V and a capacity of 5Ah. The AC grid voltage is considered to be 220 $V_{rms}$. The DC-link voltage is selected to be 400 V, thus each module is regulated to 200 V (2 modules per arm). Three Typhoon HIL 604 units are operated in parallel, emulating the AC microgrid, IC, and DC microgrid separately. The HIL testbed is shown in Figure 5.10, while Figure 5.11 shows the implementation of the power circuit within the different devices. For control purposes, the microgrid level power management strategies are implemented using Typhoon SCADA. The MMC based IC is controlled with four TI TMS320F28335 control cards, where two are utilized for controlling the twelve bidirectional converters, one for controlling grid-current and circulating currents, and the last one is utilized for protection, gate enable, and communication purposes. The AC and DC microgrids' resources are implemented

through 2L three-phase inverters and DC-DC converters (voltage-fed). Linear loads are considered on both AC (resistive-inductive) and DC sides (resistive), and the generation is 12 kW for both DC and AC sides. According to (4), the active power rating of the MMC based IC is 18 kW, and the maximum load for both AC and DC microgrids is 6 kW (12 kW in total), where 2 kW from each side is considered to be essential.

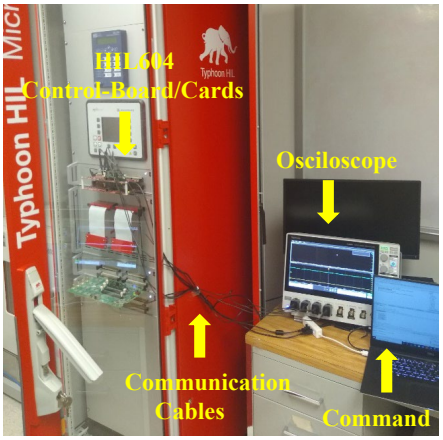



Figure 5.10. Typhoon HIL testbed.

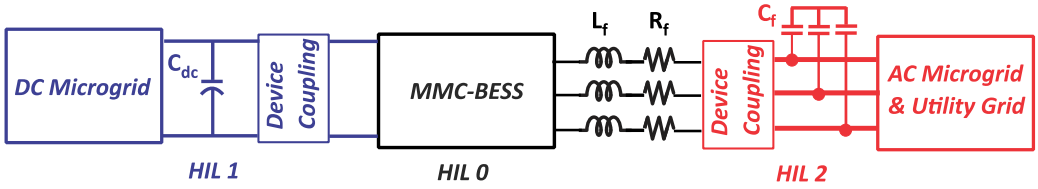



Figure 5.11. Hybrid AC/DC microgrid implementation.

### 5.4.1 Resilient and decoupled microgrid operation

The resilient and decoupled microgrid operation results focus on observing the effect of the AC grid operation on the DC microgrid voltage stability and islanded mode with unbalanced AC loads. Three scenarios are considered for verifying the operation of the system.

The first scenario assumes the presence of the utility grid. The DC microgrid sinks 1 kW while the IC provides 3 kW of active power to the electrical grid. The overall

power to be provided by the batteries within the IC is 4 kW. At some point, an AC grid-voltage asymmetry scenario starts where positive sequence injection (PSI) and balanced AC grid power LVRT strategies are applied to the IC. It can be observed throughout this ordeal that the DC microgrid is not affected under both LVRT strategies, as shown in Figure 5.12.

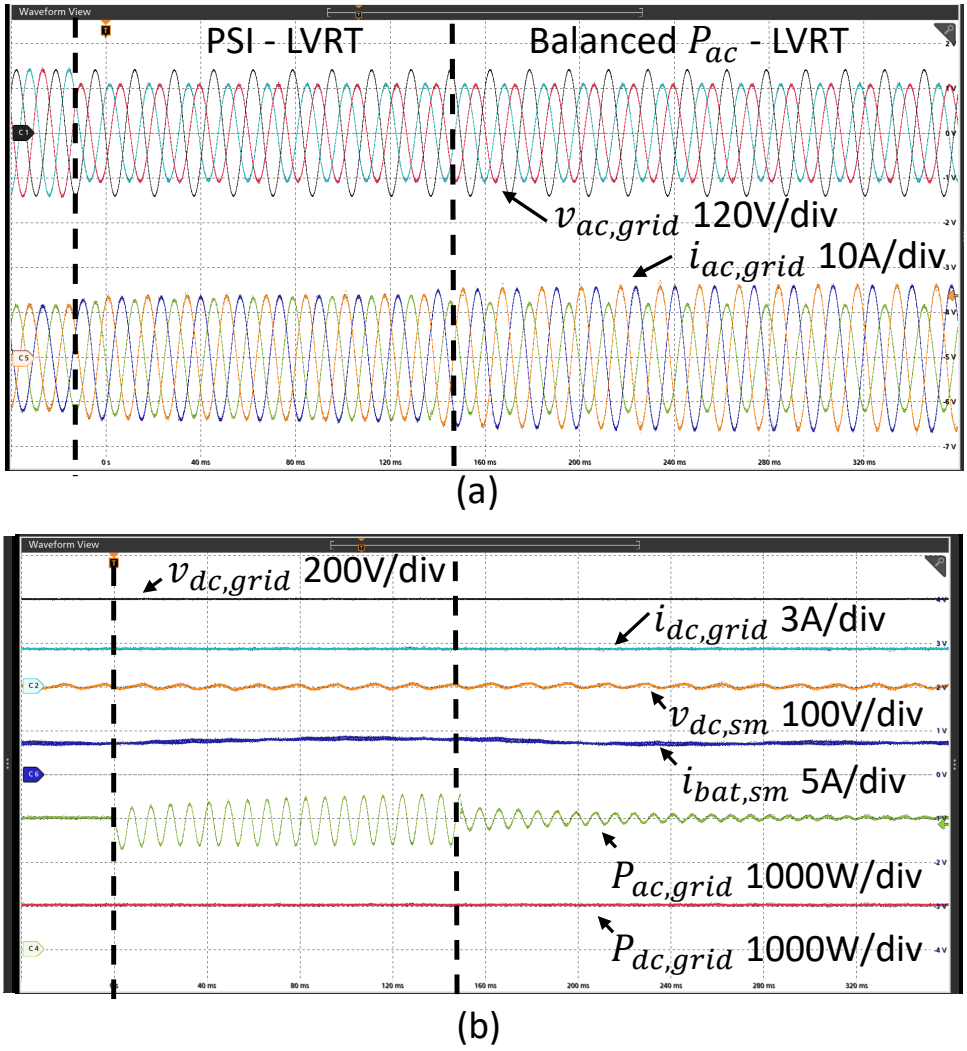



Figure 5.12. Grid-connected operation under grid-voltage asymmetry scenarios. (a) Grid voltages and currents; (b) DC microgrid voltage and current, battery current, AC (3-phase), and DC microgrid active power.

The second scenario is shown in Figure 5.13, where the HMG is also operating in utility grid-connected mode. The result shows the SM's DC-link voltage transient

response for an AC grid rated active power step. It can be observed that by properly matching the power bandwidth and SM DC-link voltage control bandwidth, the SM DC-link voltage is hardly affected. This leads to the DC microgrid voltage not observing significant transients, thus effectively decoupling AC and DC microgrids.

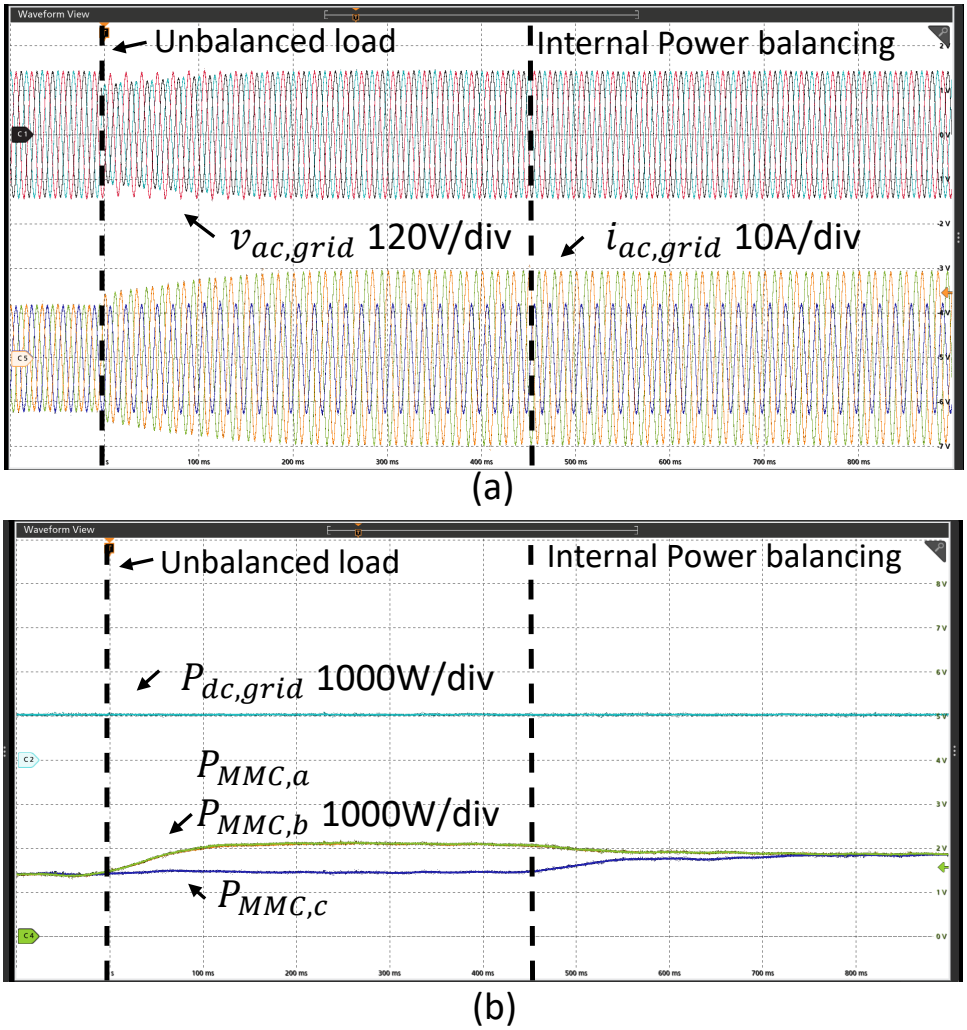



Figure 5.13. Islanded operation mode under unbalanced loads. (a) AC-grid voltages and currents; (b) DC microgrid power and MMC based IC per-phase active power (battery power deviation).

Finally, in Figure 5.14, the HMG operates under grid forming mode in islanded operation. The DC microgrid sinks 1 kW, while the AC microgrid sinks 3 kW when an unbalanced load is connected to the system. The power internally to the IC deviates in each phase, which requires the phase power balancing scheme to operate.

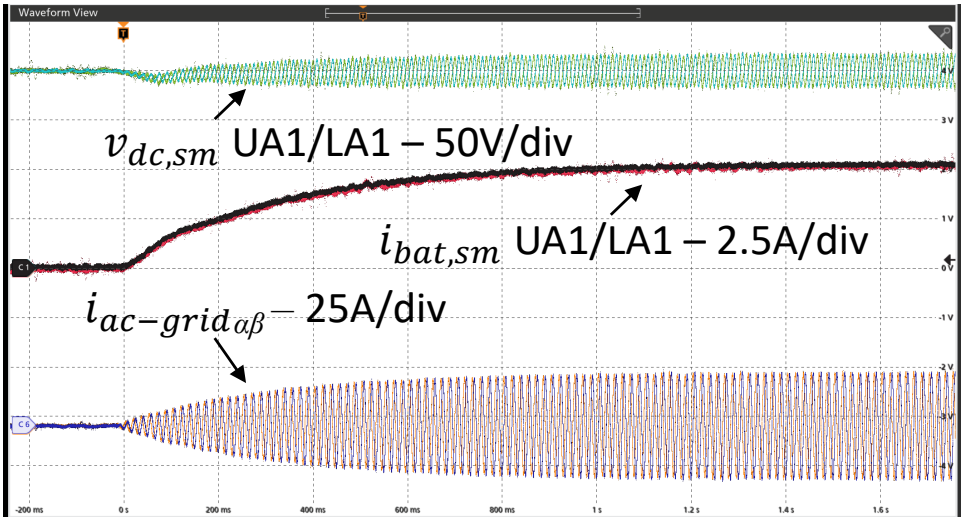



Figure 5.14. DC link voltage under AC grid power step (decoupling).

### 5.4.2 Power management strategies

To highlight the power management strategies, two scenarios, one in utility grid-connected mode and another in islanded mode, are considered.

The utility grid-connected mode assumes that the 6 kW DC-side load is connected to the DC microgrid while the DC generation is equal to 2 kW. Therefore, $P_{DC}$= -4 kW. Furthermore, $SoC_{BESS}$= 0.75; as such, the interlinking converter needs to absorb power from the AC grid equivalent to -10 kW (supplying both DC microgrid and charging the battery with $P_{BAT}$). At some point, the DC generation starts to increase at 1 kW/s from 2 kW to its rated value of 12 kW. Therefore, $P_{DC(end)}$= 6 kW. Accordingly, $P_{IC}$ is adjusted from -10 kW to 0 kW, as the power surplus from the DC microgrid will inherently charge the batteries (because of its DC microgrid forming capability). Figure 5.15 shows the results for this scenario. The notations are as defined in Section 5.3 .

The islanded mode assumes that $SoC_{BESS}$= 0.5 and only the essential loads are connected on both sides. The DC generation remains at 1 kW throughout the whole scenario, therefore, $P_{DC}$= -1 kW. The AC side generation is initially at 0 kW. Since an

essential load of 2 kW is connected to the AC side, the battery needs to provide an overall 3 kW active power to the grid. At some point, the AC generation increases from 0 to 3 kW, and since the MMC forms the AC microgrid, the AC side power surplus will inherently replace the battery usage at a rate of 1 kW/s. The results for this scenario are shown in Figure 5.16.

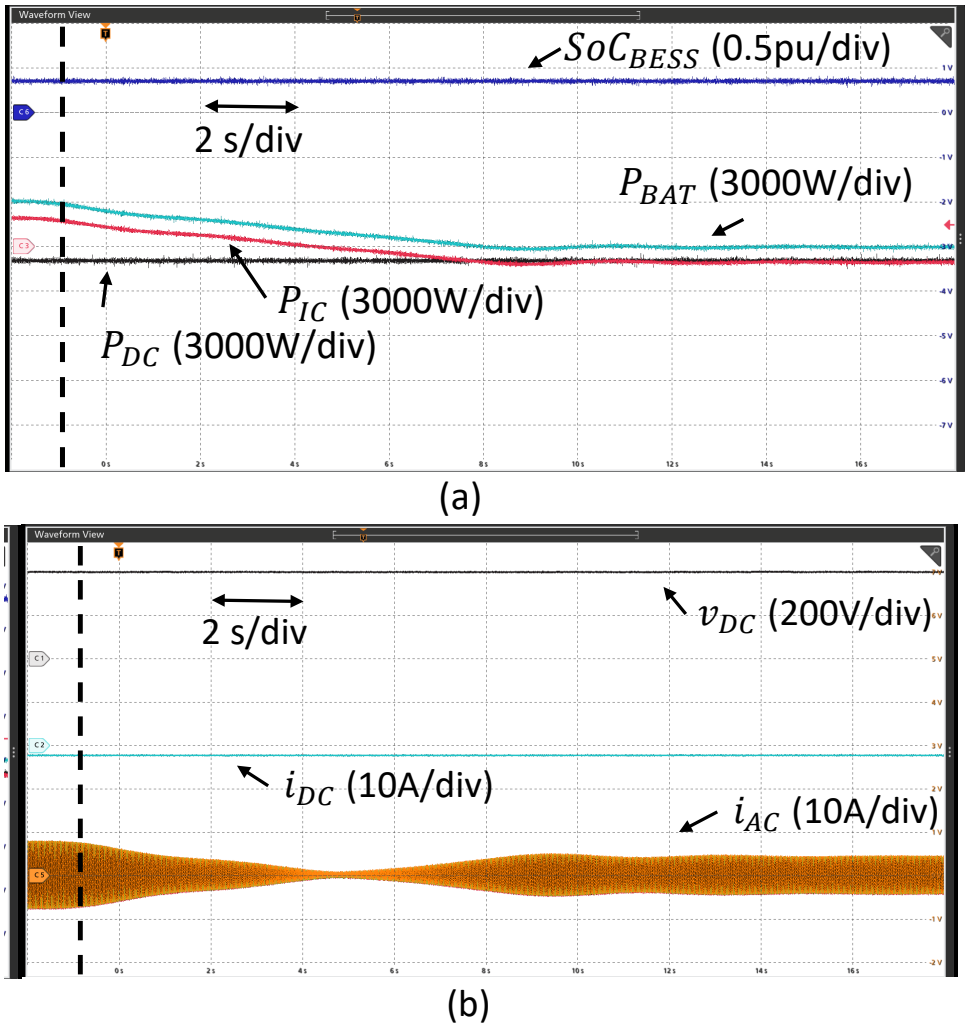



Figure 5.15. Power management for Islanded mode: (a) Battery SoC, interlinking converter power, DC microgrid power, and battery power; (b) DC microgrid voltage, DC microgrid current, and AC grid currents.

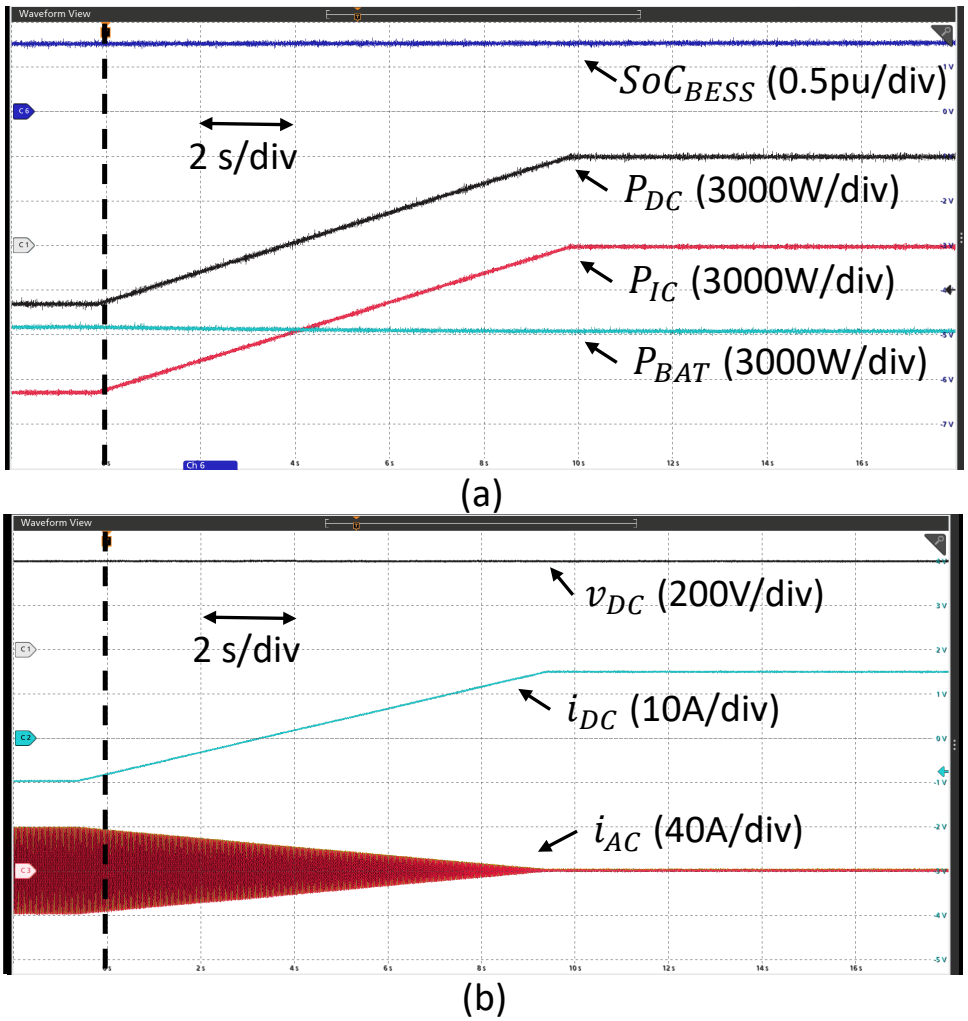



Figure 5.16. Power management for utility grid-connected undispatched power mode: (a) Battery SoC, interlinking converter power, DC microgrid power and battery power; (b) DC microgrid voltage, DC microgrid current and AC grid currents.

## 5.5 Conclusion

This chapter proposes the power management and control strategies related to an MMC based IC with integrated energy storage for HMG applications. The proposed architecture is capable of forming both AC and DC microgrids, while obtaining decoupled operation of AC and DC microgrids through its two-degree of freedom control loops. The power management strategies are discussed for grid islanded and grid-connected modes. HIL results that showcase the resiliency of the system under LVRT scenarios in utility grid-connected mode and unbalanced load conditions in grid-

forming mode are presented. Furthermore, results show the decoupled operation during AC grid power steps, where the module's DC link voltage is hardly affected. Finally, the implemented power management strategies highlight the power exchange between the DC and AC microgrids, IC, and utility grid (when available). The results show that the proposed architecture is capable of maintaining system-wide stability.

### 5.6 Publications

- J. M. L. Fonseca, S. R. P. Reddy and K. Rajashekara, "Resilient Operation of Hybrid AC/DC Microgrid with Interlinking Converter Based on Modular Multilevel Converter with Integrated BESS,". *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Houston-TX, 2022.

# 6. CONCLUSIONS AND FUTURE WORK

## 6.1 Conclusions

Battery energy storage systems (BESS) have a variety of essential applications related to the electrical grid, such as regulating grid frequency, reducing peak power, and mitigating the intermittency of renewable energy. The grid voltage support and var compensation of BESS are other functions that have gained much attention in recent years. Numerous studies have also been reported on the combined active and reactive power support operation from BESS. Hence, researchers have focused on developing high power and energy density lithium-ion (Li-ion) batteries for various applications including integration intthe o grid. This dissertation develops power strategies, and energy requirements for Modular Multilevel Converter (MMC) based BESS for grid integration. The presented work initially starts from developing battery models for grid applications to system-level operation, including BESS and the electric grid.

A novel method is presented for estimating the parameters of the equivalent circuit model (ECM) for lithium-ion battery cells, which is focused on their use in grid applications. The effect of temperature and state of charge (SoC) on parameters is incorporated into the proposed methodology and correlated using polynomial regression. It has been demonstrated that the proposed model increases the accuracy of terminal voltage estimation by approximately 50%. To obtain the parameter variations as the battery ages, accelerated degradation tests are performed. After a capacity fade of only 5.3%, the battery impedance is estimated to increase by 11%, indicating that the maximum variation should also be considered while designing circuit parameters, controller gains, and BMS.

A close correlation between the voltage oscillation in the DC-link of the MMC module and the battery current ripple is investigated in the context of the BESS-MMC. This dissertation examines the exact capacitor energy requirements for various operations of BESS-MMC, including arm/phase power balancing and State of Charge (SoC) balancing. The carried-out analysis assumes that the current ripple flowing into the MMC module only flows through the DC-link capacitor. This operation ensures that the battery current ripple is minimized and is achieved through the bidirectional DC-DC converter control. Given this scenario, it is found that for a BESS-MMC, the capacitor energy requirement can increase by almost 100% compared to a grid-connected MMC. This result implies that the capacitance value for each DC-link module has to be doubled for a fully operational BESS-MMC.

An attempt is made to improve the resiliency of BESS-MMC by maintaining its connection to the electrical grid. Fault scenarios that may result in asymmetric voltage conditions on the grid and an asymmetric number of modules connected in each arm are considered. Techniques for power and SoC balancing with defined active power limits are proposed and verified in a Controller-Hardware-in-the-Loop (C-HIL) environment. Both external (through grid currents) and internal (through circulating currents) power balancing techniques are possible for the asymmetric grid voltage scenario. However, only the internal power balancing allows different low voltage ride-through (LVRT) strategies to be employed. The proposed per-phase SoC balancing under the same asymmetric grid voltage scenario also benefits from using circulating currents. The SoC balancing power reference can also be set to the battery power limits, speeding up the balancing procedure. The proposed power balancing strategy for an asymmetric number

of modules per arm ensures that the maximum available power of the BESS can be injected into the AC grid. Furthermore, the transient from symmetric to an asymmetric number of modules per arm is also investigated. This transient result shows that the injection of harmonics to the AC grid due to the operation of the MMC in a nonlinear region can be limited by safely increasing the DC-link voltage level through the bidirectional DC-DC converter (BDC).

The BESS-MMC can be used to interconnect microgrids in a hybrid microgrid environment by acting as an interlinking converter (IC). As a result, there is no need to connect battery modules to either a DC or AC microgrid. Additionally, the inherent two-degrees of freedom of MMC result in a complete decoupling of the two grids. The decoupling effect between microgrids is corroborated by the resilient operation of the HMG under adverse AC grid scenarios, namely the AC grid voltage asymmetry (utility grid-connected mode) and unbalanced load (AC grid forming mode). Power management strategies are proposed for utility grid-connected (undispatched) and AC grid forming mode and validated in the C-HIL environment.

### 6.2 Scope for future work

1. Expand the BESS-MMC system to 6 modules per arm (36 modules total) by utilizing three Typhoon-HIL 604 units. Each unit emulates a specific phase of the converter, while two additional HIL 604 units can emulate the AC utility grid (and AC microgrid for Chapter 5). By expanding the BESS-MMC, a medium-voltage grid can be considered, with higher power levels.

2. Chapter 2 proposes a novel ECM for lithium-ion batteries that are used throughout the dissertation to design controller parameters and capacitor sizing, both

with the intent to minimize the battery current ripple. The estimation of SoC and SoH can be further investigated.

3. The operation of a hybrid microgrid can slightly impact the MMC DC-link capacitance sizing. The main difference from the analysis presented in Chapter 3 is the DC circulating current flowing into or out of the DC microgrid. Although the DC circulating current does not significantly impact the capacitor sizing, the precise increase in capacitor energy requirements can be generalized for this operation.

4. PI and PI+NF controllers are designed in this dissertation based on Laplace domain plants and then discretized for implementation in DSP. Two-degree-of-freedom (2DOF) PID digital controllers designed based on discretized plants can potentially improve the performance by both attending to the battery current minimization requirements and disturbance rejection (load steps).

5. The proposed hybrid microgrid under dispatched power grid-connected operation mode can be investigated.

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