Design and Calibration of Power-Efficient High-Speed SAR-Based ADCs

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To my parents

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ABSTRACT

High-speed analog-to-digital converters (ADCs) with medium-to-high resolutions find wide application in test equipment, wireline transceivers and wireless communication systems. While the successive-approximation-register (SAR) ADCs gain popularity recently owing to the advancing technology nodes. The goal of this dissertation was to explore the possibilities of further enhancing the operation speed of SAR-based ADCs and simultaneously pushing the leading edge of ADC power efficiency.

A commonly adopted approach to boosting the sampling rate of Nyquist ADCs is time-interleaving (TI), where the operations of multiple ADC channels are coordinated by a multi-phase clock to aggressively shorten the sampling period. Unfortunately, extra hardware and power overhead associated with multi-phase clock generation, multi-channel reference supply, data multiplexing and possibly signal buffering greatly limit the achievable efficiency of the ADC, especially with a large interleaving factor. In addition, interleaving errors resulted from channel mismatches undermines the linearity of the ADC and thus mandates complicated calibrations to maintain a decent accuracy. As such, power-efficient approaches to maximizing the conversion rate of single-channel ADCs are crucial for optimization of the overall architecture. To support this argument, three hardware prototypes with proposed architectures in 28-nm FDSOI have been fabricated and characterized with through measurements.

The first prototype is a two-step partially interleaved SAR ADC with fast noise reduction technique based-on loop-unrolled conversion. The inter-stage gain is

controlled by a background calibration mechanism to avoid linearity degradation. A test chip measures a Nyquist SNDR of 46.65 dB at 1 GS/s while dissipating only 2.1 mW.

The second hardware implementation is a single-channel SAR ADC with a double-rate comparator. The proposed architecture improves the ADC conversion rate and considerably decreases the power consumption at the same time. Clocked at 550 MS/s, the prototype ADC achieves a SNDR of 51.6 dB, consuming a total power of 1.28 mW. This translates into the best power efficiency among previously reported ADCs with >300 MS/s sampling rate.

Finally, a bypass-based opportunistic adaptive comparator offset calibration is proposed to acquire the full benefit of alternate-comparator acceleration. As demonstrated by an eight-time interleaved SAR ADC showing a 49.02-dB Nyquist SNDR with a total power consumption of 9.8 mW at 2.4 GS/s.

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INTRODUCTION

1.1 Motivation

Digital signal processing (DSP) plays an increasingly important role in modern communication systems due to its favorable attributes such as the high design flexibility, low hardware dimensions and short design cycle. However, dictated by the analog nature of the "real-world" signals, the operation of signal sensing needs to remain in analog domain. In this sense, the mechanism of converting the sensed analog signal into a stream of bit flow that can be recognized by the digital signal processors becomes crucial and may be inevitable for a long period of time. This is where the analog-to-digital converter (ADC) comes into play. As a bridge between the "real-world" signal and digital processing, the ADC interfaces analog frontends with the back-end digital units in a typical configuration of communication systems, as shown in Fig. 1.1.

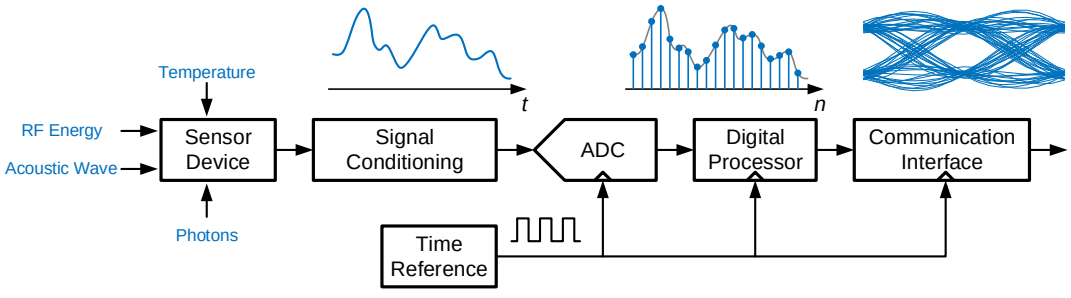


Figure 1.1. Typical configuration of communication systems.

Among the various applications, wireless and wireline transceivers mandate the use of high-speed ADCs with medium-to-high resolutions for fast and reliable communications. Implementations of such ADCs are no easy tasks since the operation speed and resolution construct a fundamental tradeoff. Aggressive enhancement on one of the two parameters usually leads into an inevitable degradation on the other. This requirement can be even more stringent if the system is to be integrated into a battery-powered mobile device, where the power efficiency is yet another limitation to be taken into consideration. Over the past few decades, the leading edge of the ADC power efficiency has been continuously pushed forward as the actively conducted research progresses. To date, less than 20-fJ/conv.-step efficiency has been achieved on giga-sample-per-second ADCs, according to the survey by Dr. Boris Murmann

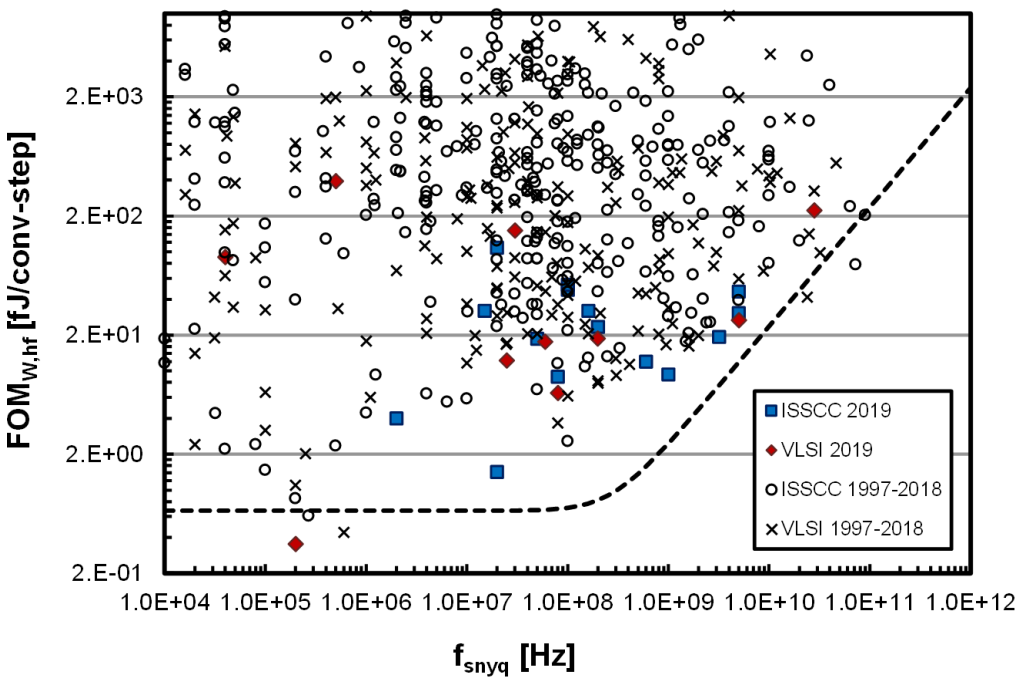


Figure 1.2. Walden FOMs of ADCs presented at ISSCC and VLSI.

(http://web.stanford.edu/~murmann/adcsurvey.html) [1]. Fig. 1.2 shows the plot of Walden Figure of Merit (FOM) of ADCs reported at ISSCC and VLSI between 1997 and 2019.

A majority of the giga-sample-per-second ADCs are implemented with pipelined architecture [2, 3, 4, 5], time-interleaved (TI) successive-approximation-register (SAR) architecture [6, 7, 8, 9] or a combination of the two [10]. While pipelined ADCs provide cascaded partial quantization and signal gain, both of which are attractive merits in implementing low-noise and high-speed conversion, the power overhead induced by the operational amplifier (op-amp) in the multiplying digital-to-analog converter (MDAC) stage makes them less suitable for applications with limited power budget. In addition, the low supply voltage of the advanced technology nodes poses a great challenge on the amplifier design and severely clamps the maximum input swing of the ADCs, incurring yet more power budget for noise suppression. Pipelined ADCs with ring amplifiers (ring-amps) [11, 12, 13, 14] or dynamic amplifiers [15] replaces the power-hungry conventional op-amps with more scaling-friendly and power-efficient amplification solutions. However, the non-conventional amplifications are subject to PVT variation and requires complex calibrations to maintain the target accuracy. TI SAR ADCs, on the contrary, are renowned for their low power consumption and mostly digital configuration, with the major drawback being the relatively low speed of individual ADC channels. Given a certain speed requirement, this translates into a large interleaving factor and thus, the associated overhead brought by the peripheral blocks such as the multi-phase clock generation, distributed reference buffers, data multiplexer and possibly hierarchical input buffers. In addition, calibrations of the inter-channel

mismatches for a large number of channels increase the implementation complexity and are more subject to residual errors. As such, a special focus is placed in this dissertation on improving the per-channel speed of SAR ADCs without sacrificing the power efficiency.

1.2 Main Contributions

A total of three hardware implementations are presented in this dissertation. Each with a unique architecture proposed to address the speed-accuracy tradeoff of SAR-based ADCs on a per-channel basis. All three works show competitive efficiencies in comparison to the state-of-the-art ADCs with similar resolutions and comparable speed.

The first prototype is a two-step partially interleaved SAR ADC with fast noise reduction technique based-on loop-unrolled conversion [16]. Unlike conventional noise reduction techniques that requires a series of repeated cycles, the proposed method employs a couple of comparators for a single comparison, taking advantage of the multi-comparator configuration of loop-unrolling. The comparators used in the second stage are a modified version of the StrongARM latch to further suppress the input-referred noise. The two conversion steps are interfaced with passive residue transfer to avoid active amplification. The inter-stage gain is controlled by a background calibration mechanism to avoid linearity degradation. A test chip measures a Nyquist SNDR of 46.65 dB at 1 GS/s while dissipating only 2.1 mW, showing a competitive Walden FOM of 12.1 fJ/conv.-step.

The second hardware implementation is a single-channel SAR ADC with a double-rate comparator [17]. Apart from eliminating the delay caused by the comparator reset from the critical path during normal conversion, the double-rate comparator also enables a seamless phase transition between the conversion and the offset calibration. In addition, the frequency of the clock that drives the comparator is effectively reduced by a half, which, in combination with the proposed asynchronous clock generation circuit, leads to significant power saving for the digital circuitry. The proposed architecture improves the ADC conversion rate and considerably decreases the power consumption at the same time. Clocked at 550 MS/s, the prototype ADC achieves a SNDR of 51.6 dB, consuming a total power of 1.28 mW. This translates into the best power efficiency among previously reported ADCs with >300 MS/s sampling rate.

Finally, an ADC architecture with several techniques to optimize the power efficiency and conversion rate is presented [18]. First, a pre-defined bypass window, introduced by the customized non-binary digital-to-analog converter (DAC), is used to modestly reduce the power consumption. Several conversion cycles are skipped as the input signal falls within the bypass window. Second, to enhance the operation speed, two alternate comparators are adopted in each ADC channel. And an opportunistic adaptive comparator offset calibration is proposed to eliminate the conversion rate degradation caused by the dedicated calibration cycle. The comparator offset is calibrated only when the bit bypass is triggered with the calibration step size adaptively set to acquire both fast convergence and small algorithm noise. In addition, the reference voltage of each ADC channel is provided by a pre-charged reservoir to avoid inter-channel crosstalk without introduction of power-hungry distributed reference buffers.

As demonstrated by an eight-time interleaved SAR ADC showing a 49.02-dB Nyquist SNDR with a total power consumption of 9.8 mW at 2.4 GS/s. The corresponding Walden and Schreier FOMs are 17.7 fJ/conv.-step and 159.9 dB, respectively.

1.3 Dissertation Organization

This dissertation is organized as follows: Chapter II starts with an introduction of the fundamentals of ADCs including different ADC architectures and ADC metrics for performance evaluation. Then, several modern design techniques in high-speed ADCs are discussed.

Chapter III presents the design and implementation of the two-step partially interleaved SAR ADC. The concept of fast noise reduction is described. Further, the scheme of the background gain calibration is discussed. Then, the overall ADC architecture along with detailed implementations of the key building blocks are presented. Finally, measurement results are shown and compared with the state-of-the-art publications.

Chapter IV elaborates on the implementation of the double-rate comparator-based single-channel SAR ADC. The architecture of the double-rate comparator along with the simulated performance are presented. Further, the implementation of the proposed half-rate clock generation circuit is shown. The measured ADC performance and a comparison with previously published works are given at the end of the chapter.

Chapter V details the design of the 8-channel interleaved SAR ADC. First, the use of the non-binary DAC-based bypass window is discussed. Then, the concept and

implementation of the opportunistic adaptive calibration, enabled by the conversion phase truncation of the bypass window, is detailed. Further, the reference reservoir used to eliminate the inter-channel crosstalk with a low overhead is discussed. Finally, the effectiveness of the proposed architecture is demonstrated by the measured performance shown at the end of the chapter.

Chapter VI concludes this dissertation and talks about the future directions.

CHAPTER II

OVERVIEW

2.1 ADC Architectures

ADC is big family that consists of quite a few members with different architectures. Each with its unique pros and cons and is thus designated for different kinds of applications. The discussion in this section is based only on the conventional architectures or implementations, the advanced conversion techniques associated with SAR-based ADC architectures are discussed in Section 2.3.

2.1.1 Oversampling ADCs

Oversampling ADCs are a type of ADCs that employ oversampling and possibly noise shaping to aggressively suppress the in-band noise of the conversion process. The most commonly known oversampling ADC is the delta-sigma modulator (DSM or ΔΣ-M). Fig. 2.1 shows the typical configuration of a DSM. Generally, this system is

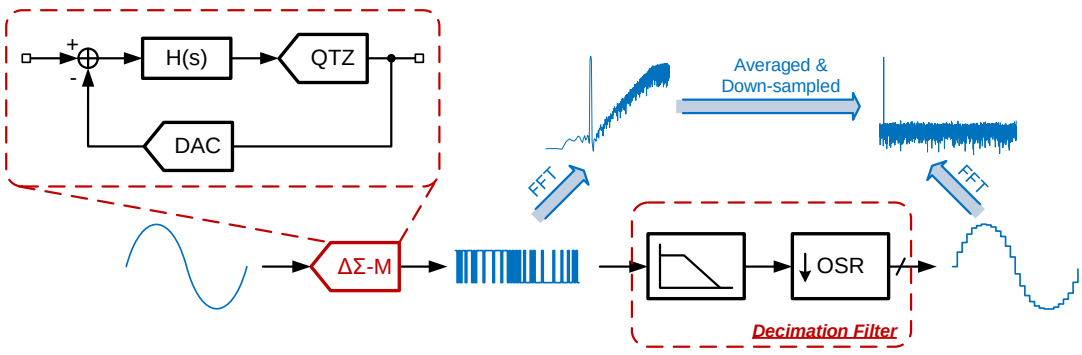


Figure 2.1. Typical configuration of a delta-sigma modulator.

composed of a loop filter, a quantizer and a feedback DAC. By following the system signal flow and deriving the transfer function for both the input signal and the noise introduced by quantizer, we have

$$STF = \frac{H(s)}{H(s)+1} \tag{2.1}$$

and

$$NTF = \frac{1}{H(s)+1}, \tag{2.2}$$

where $H(s)$ is the transfer function of the loop filter. As the loop filter is usually implemented as a low-pass filter with a gain of significantly higher than one, the signal transfer function (*STF*) can be approximated as one in most practical cases while the noise transfer function (*NTF*) is high-pass in nature with the zeros being the poles of *H*(*s*). In other words, the signal is passed from input to output theoretically without distortion while the low-frequency component of the quantizer introduced noise (mostly quantization noise and thermal noise) is attenuated.

The analog input is represented by the output in an "average" sense and the accuracy is not limited by the intrinsic resolution of the quantizer. This is an attractive attribute in implementing high-accuracy analog-to-digital conversions. However, the main drawback of this architecture is the rather limited signal bandwidth, which is on the order of several MHz or even kHz. The relationship between the signal bandwidth and the sampling rate is defined by

$$BW = \frac{f_S}{2 \cdot OSR}, \tag{2.3}$$

where *OSR* represents "oversampling ratio" and f_S is the sampling rate. Though this architecture can easily break the accuracy limit posed by the analog component matching and the intrinsic gain of the amplification stages with a low power consumption, the relatively low bandwidth efficiency caused by a large *OSR* renders the oversampling ADC an unpopular candidate for high-speed and broadband applications.

2.1.2 Flash ADCs

Flash ADCs are a kind of Nyquist ADC that compares the sampled input with a bank of references simultaneously. The block diagram of a flash ADC is shown in Fig. 2.2. It consists of track-and-hold (T/H) network, a resister ladder for reference generation, a bank of comparators and a thermometer-to-binary code converter. The operation of a flash ADC is very straightforward and does not involve signal feedback, so it achieves the fastest conversion rate among all other ADC architectures. However, as the number of comparators increases exponentially with the resolution and all

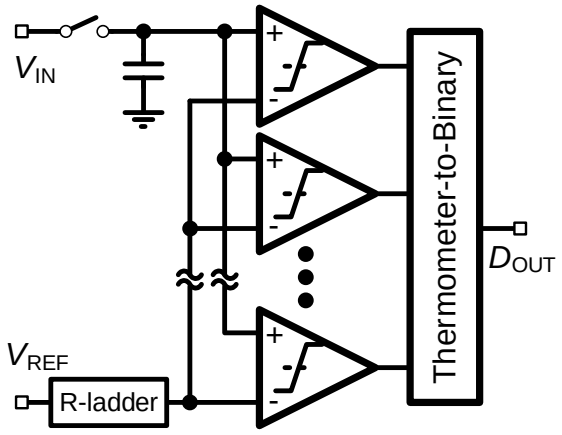


Figure 2.2. Flash ADC.

comparators need to be sized to meet the worst-case noise and/or offset requirement, the power efficiency drops drastically at high-resolution domain. In addition, the parasitics caused by the layout of a huge number of comparators can turn out to be problematic at high frequencies. All these limiting factors do not benefit much from the advancing technology scaling and thus highly restrict the applications of flash ADCs in modern communication systems, where the overall efficiency is one of the top priorities.

2.1.3 Pipelined ADCs

Pipelined ADCs segment the conversion process of a long series of digital bits into several steps, with the operation of adjacent steps pipelined for accelerated processing. The block diagram of a pipelined ADC is shown in Fig. 2.3. A pipelined ADC consists of a couple of cascaded MDAC stages. An MDAC stage is made up of a sub-ADC, a DAC and an operational transconductance amplifier (OTA). The sampled input is coarsely quantized by the sub-ADC in each stage, the output of the sub-ADC is then fed forward to the input of the OTA to generate the residue, which is amplified by the OTA before being sampled and processed by the next stage. The active gain provided by the MDAC relaxes the noise requirement on the backend stages and also

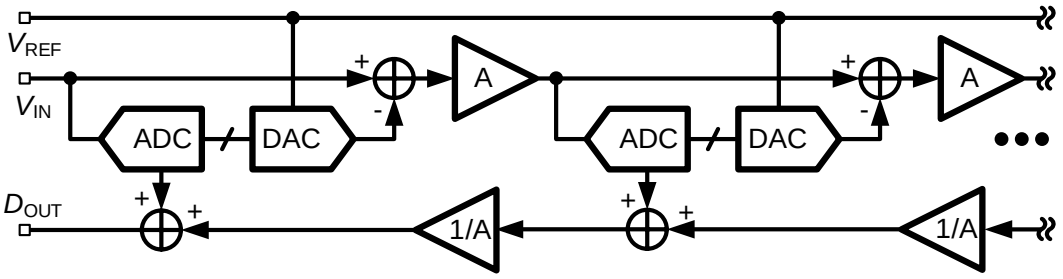


Figure 2.3. Pipelined ADC.

facilitates the reference supply, since a single reference can be fed to all stages without analog scaling. In ideal cases, the input and the output of each stage are mapped with

$$V_{IN} = \sum_{i=1}^{M} \frac{1}{A^{i-1}} D_{S,i} \cdot V_{REF} + V_{n,Q} \,, \tag{2.4}$$

where $D_{S,i}$ is the output of the ith stage, V_{REF} is the reference voltage, A is the gain (mostly closed loop gain) of the OTA and $V_{n,Q}$ is the quantization noise. The pipelined architecture is advantageous to acquire both high speed and high accuracy. However, the implementation of an OTA with both high bandwidth and high gain is nontrivial. This can be more challenging in advanced technology nodes due to the limited voltage headroom and low intrinsic gain of the MOSFETs, as will be detailed in Section 2.4.4.

2.1.4 SAR ADCs

The operation of SAR ADCs is based on binary search algorithm, which makes feedback the most crucial part in its implementation. Fig. 2.4 shows the block diagram of a SAR ADC. A SAR ADC is composed of a T/H network, a feedback DAC (mostly capacitive), a comparator and SAR logic. The input is sampled onto the DAC and

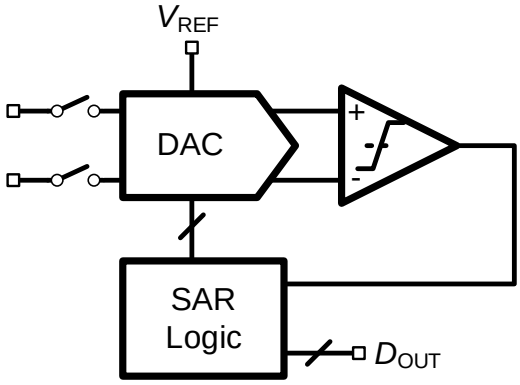


Figure 2.4. SAR ADC.

compared to a scaled reference by the comparator, the decision is then fed back by the SAR logic to update the reference before another comparison is made. The relationship between the input and output can be expressed as

$$V_{IN} = \sum_{i=1}^{N} \frac{1}{2^i} \cdot D_i \cdot V_{REF} \ , \tag{2.5}$$

where D_i is the *i*th bit and N is the ADC resolution.

This architecture is renowned for its high power efficiency, since the no active amplification is involved and only one comparator is required, regardless of the specific resolution. However, it suffers from relatively low speed. Except for the first cycle, each cycle needs to be directed by the decision made during the previous cycle. Hence the cyclic operation takes a large portion of the sampling clock period, which can be written as

$$T = N \cdot t_{dec.} + (N-1) \cdot \left(t_{SAR} + t_{set.} \right) + t_{samp.} \ , \tag{2.6}$$

where T is the sampling clock period, $t_{dec.}$ the comparator decision delay, t_{SAR} the SAR logic delay, $t_{set.}$ the DAC settling time and $t_{samp.}$ the time taken by sampling. As can be seen from Eqn. (2.6), there is a fundamental tradeoff between the sampling rate and the resolution. This used to limit SAR ADCs to low-speed applications only. Fortunately, as the MOSFETs and thus the parasitics keep shrinking in size, $t_{dec.}$ and t_{SAR} have improved considerably over the past years. In addition, techniques to break the speed-resolution tradeoff also help a lot in extending the applications of modern SAR ADCs to high-speed domain.

2.1.5 TI ADC

TI ADC is a popular architecture to break the single-channel speed limitation. Fig. 2.5 shows the block diagram of a TI ADC. A TI ADC consists of a couple of sub-ADC channels driven by a multi-phase sampling clock. All channels take turns to sample and quantize the input, and the outputs of all these channels are combined into a single output so that it is as if the input was quantized by a single ADC. In time domain, the interleaved sampling process can be expressed as [19]

$$\begin{cases} v_1(t) = v_{IN}(t) \cdot \sum_k \delta(t - kMT) \\ v_2(t) = v_{IN}(t) \cdot \sum_k \delta(t - kMT - T) \\ \dots \\ v_M(t) = v_{IN}(t) \cdot \sum_k \delta\left[t - kMT - (M-1)T\right] \end{cases}, \tag{2.7}$$

where V_i is the sampled input for the ith channel, M is the interleaving factor (the number of channels) and T is the sampling period of the interleaved ADC. In frequency domain, we have

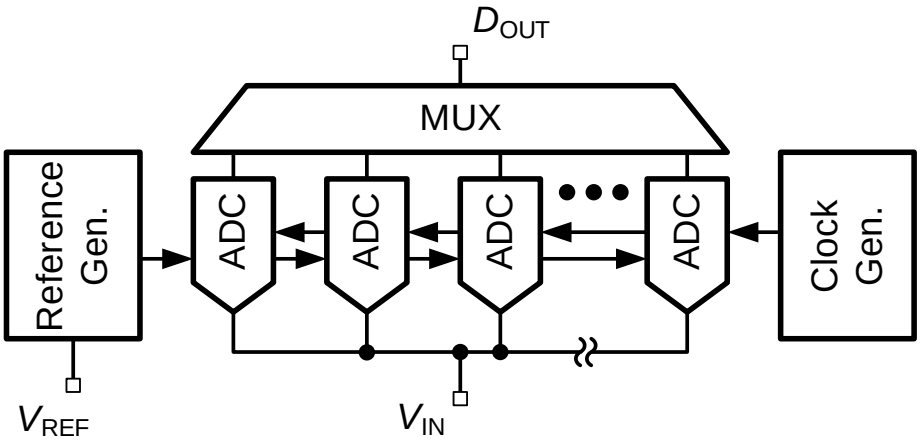


Figure 2.5. Time-interleaved ADC.

$$\begin{cases} V_1(f) = \dfrac{1}{MT} \cdot V_{IN}(f) * \sum_k \delta(f - \dfrac{k}{MT}) \\ V_2(f) = \dfrac{1}{MT} \cdot V_{IN}(f) * \sum_k \delta(f - \dfrac{k}{MT}) e^{-j2\pi fT} \\ \ldots \\ V_M(f) = \dfrac{1}{MT} \cdot V_{IN}(f) * \sum_k \delta(f - \dfrac{k}{MT}) e^{-j2(M-1)\pi fT} \end{cases} . \quad (2.8)$$

For each channel, this is a sub-sampling process and may result into aliasing (or folding back of the high-frequency components) if the signal bandwidth is not strictly limited to $\frac{1}{2MT}$. However, for $f = \frac{k}{MT}$ and $k \neq 0$, we have

$$1 + e^{-2\pi fT} + e^{-4\pi f \cdot 2T} + \ldots + e^{-2(M-1)\pi fT} = 0 . \quad (2.9)$$

Thus, if the output data from all channels are combined, the corresponding spectrum is given by

$$V_{final}(f) = \sum_{i=1}^{M} V_i(f) = V_{IN}(f), \quad (2.10)$$

which is an ideal restoration of the input signal.

The TI technique is supposed to enable a linear scaling of the overall conversion rate by a factor of the channel number *M* and keep the power efficiency unaffected, since the power and speed of each channel remain unchanged. Unfortunately, the interleaving overhead such as the multi-phase clock generation and buffering, multi-channel reference supply, data multiplexing and possibly hierarchical input buffering makes the ideally cost-free speed enhancement impossible. Further, the interleaving errors degrade the ADC performance severely if left uncalibrated. And even with calibration, the residual errors can be unbearable in an extensively interleaved ADC.

2.1.6 Other ADC Architectures

There are also some other ADC architectures such as the digital-slope ADC, time-domain ADC, algorithm ADC (cyclic ADC), etc. Also, it is worth mentioning that these ADC architectures are not mutually exclusive. In fact, a lot of modern ADC designs employ a combination of two or more of these architectures for better tradeoff or overall performance. Some examples will be detailed in Section 2.3.

2.2 ADC Performance Metrics

A number of terminologies are used for the description of ADC performances, as defined in this section. These terminologies are used throughout this dissertation.

Resolution (N) means the number of bits of the output of an ADC. An N-bit ADC has 2^N quantization levels. In some cases, the resolution may not be an integer. For example, a 2.5-bit MDAC stage has 7 different quantization levels.

Sampling rate (f_S) is the number of samples obtained per second. Also, it refers to the number of conversions that take place per second. The unit is samples per second (S/s).

Power (P) is the power consumption of the ADC, with the unit being Watt (W).

Input Swing (V_{FS}) is maximum input voltage that can be applied to the ADC without incurring clamping. It is usually measured with differential peak-to-peak voltage ($V_{pp,diff}$).

Signal-to-quantization noise ratio (SQNR) refers to the ratio of the input power to the noise power with ideal quantization. For a full-swing input, the SQNR relates to the resolution as

$$SQNR = 6.02N + 1.76 \ [dB]. \tag{2.11}$$

Signal-to-noise ratio (SNR) is the ratio of the input power to the random noise (mostly thermal noise) power. Once both the input swing and the noise power ($V_{n,RMS}^2$) are known, it can be calculated as

$$SNR = 10\log_{10}\left(\frac{V_{pp,diff}^2}{8V_{n,RMS}^2}\right). \tag{2.12}$$

Signal-to-noise-and-distortion ratio (SNDR or SINAD) is ratio of input power to the power of all error sources, including quantization noise, random noise and distortions.

Effective number of bits (ENOB) describes the effective resolution of an ADC and can be derived from SNDR as

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02}. \tag{2.13}$$

Its value is usually less than the nominal resolution N due to the inclusion of random noise and distortion.

Spurious-free dynamic range (SFDR) is the ratio of input power to the power of the strongest spurious tone.

Harmonic distortion (HD_x) is the ratio of the harmonic power to that of the fundamental.

Total harmonic distortion (THD) is the sum of the power of all harmonics normalized to the power of the fundamental.

Walden figure of merit (FOM_W) is a metric for power efficiency evaluation as proposed in [20]

$$FOM_W = \frac{P}{f_S \cdot 2^{ENOB}}. \tag{2.14}$$

The unit is Joules per conversion-step (J/conv.-step). The lower the value, the better.

Schreier figure of merit (FOM_S) is another metric for power efficiency. It is defined in [21] as

$$FOM_S = SNDR_{dB} + 10\log_{10}\frac{f_S}{2P}. \tag{2.15}$$

This FOM is fairer for high-resolution ADCs, where the main limiting factor is the thermal noise.

2.3 Errors and Non-Ideal Effects in SAR ADCs

2.3.1 Quantization noise

As the continuous input is mapped to an output with a finite number of quantization levels, a deterministic error is introduced. However, if the input signal is relatively busy over the full scale, this noise can also be modeled as a random process with uniform distribution over the range $\left(-0.5LSB, 0.5LSB\right)$. The quantization noise power can be calculated as

$$\sigma_{n,Q}^2 = \int_{-0.5LSB}^{0.5LSB} \frac{1}{LSB} v^2 dv = \frac{1}{12} LSB^2 . \tag{2.16}$$

2.3.2 *kT/C* Noise

The *kT/C* noise in ADCs relates mostly to the sampling process. The T/H circuit of an ADC can be modeled as an R-C network, as shown in Fig. 2.6. When turned on, the sampling switch can be regarded as a resistor R_{SW}, the power spectrum of the thermal noise associated with R_{SW} is thus

$$\overline{V_{n,R_{SW}}^2} = 4kTR_{SW} , \tag{2.17}$$

where $k = 1.38 \times 10^{-23} J / K$ is the Boltzmann constant and T is the thermodynamic temperature. After being filtered by the R-C network, the noise at the output can be expressed as

$$\sigma_{n,smp}^2 = \int_0^\infty \frac{4kTR_{SW}}{1+\left(2\pi f R_{SW} C_S\right)^2} df = \frac{kT}{C_S} . \tag{2.18}$$

As the switch is turned off, the noise voltage will be left on the sampling capacitor C_S and influence the incoming conversion process. Interestingly, the noise power is independent of R_{SW}, according to Eqn. (2.18).

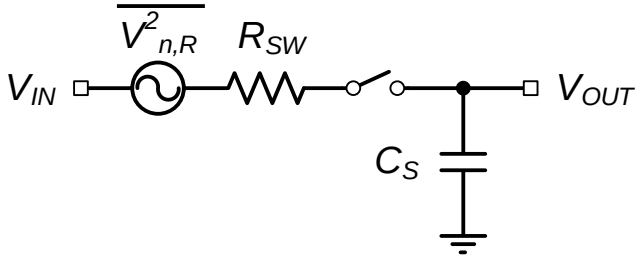


Figure 2.6. T/H network model for noise analysis.

2.3.3 Sampling Jitter

In the presence of sampling jitter, the sampling instance will be deviated from the ideal position in a random manner. This deviation incurs uncertainty on the sampled voltage and can be treated as a noise in this regard. Ignoring other non-ideal effects, the signal-to-jitter-induced-noise ratio is given by

$$SJNR = 20\log_{10}\frac{1}{2\pi f_{in}\sigma_j}, \tag{2.19}$$

where f_{in} is the input frequency and σ_j is the RMS jitter. As can be observed from Eqn. (2.19), the SJNR does not depend on the input swing. This is because the voltage uncertainty scales proportionally to the input amplitude, making the noise power closely track that of the signal. However, the SJNR does show a strong dependence on the input frequency, which is also intuitively understandable. An input with higher frequency changes at a higher rate, and this increases the voltage uncertainty for a fixed RMS jitter and input amplitude.

2.3.4 Comparator Noise

An ideal comparator has a well-defined threshold value and is able to map each input to a deterministic output. However, this is impossible in practical cases. Due to the noise of the comparator, the output is essentially a random process subject to Gaussian distribution, as depicted in Fig. 2.7.

For a comparator without offset, as the input becomes closer to zero, it will be more difficult for the comparator to make a correct decision. If the input is exactly zero, the voltage sensed by the comparator will be pure noise and there is a 50-50 chance for

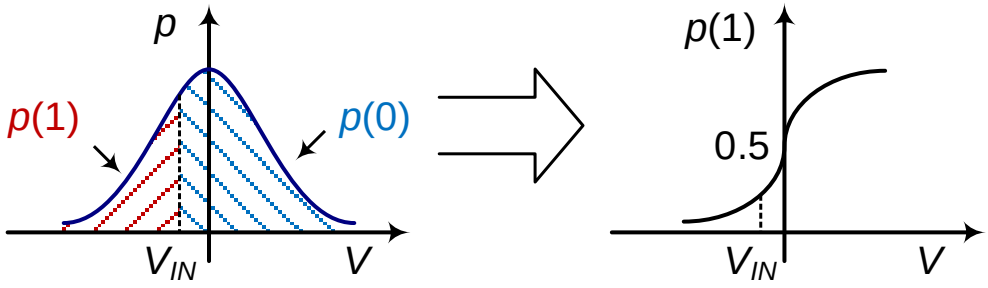


Figure 2.7. Output distribution of a noisy comparator.

the comparator to output one or zero, owing to the zero expectation of the random noise. As the output of the comparator is on digital level, the comparator noise is usually referred to the input to facilitate the analysis. The accurate calculation of the comparator input-referred noise is rather complicated and does not provide much insight in the design process. Hence, the exact value of the comparator noise is usually found out through simulations. From the probability density function of the Gaussian distribution, the probabilities of ones and zeros can be estimated by calculating the areas on the left half and right half of the input voltage, respectively. Then, the cumulative probability function can be generated accordingly, as shown on the right-hand side of Fig. 2.7. By sweeping the differential input voltage of the comparator and keeping a record of the probabilities of ones, a set of data can be collected and used for curve fitting. The fitted curve, resembling that of the cumulative probability function in shape, can then be used to estimate the root-mean-square (RMS) input-referred noise with decent accuracy, provided enough data points have been obtained.

The input-referred comparator noise does not add directly onto the input-referred noise of the ADC. Rather, a scaling factor (or noise gain) is needed for accurate analysis of the effect of comparator noise on the ADC. This scaling factor is a

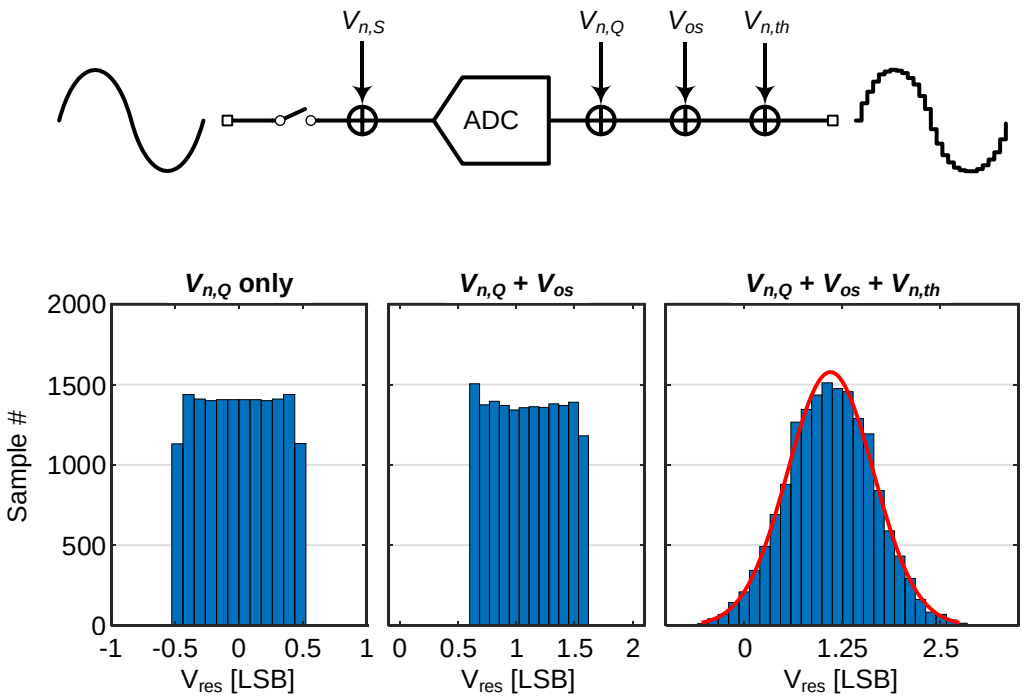


Figure 2.8. SAR ADC residue with different noise sources.

complicated function of the comparator noise itself and the specific architecture of the ADC [22]. But for simplicity, a pessimistic estimation can be made assuming a scaling factor of one, if the comparator noise is reasonably small and the conversion algorithm is not based upon redundancy.

Apart from noise, the comparator may also experience a DC offset, which alters the threshold of the comparison. This can be observed from the non-zero expectation of the Gaussian plot in a noise simulation. The errors caused by the random noise can be captured by sampling the residue upon completion of the SAR conversion. Fig. 2.8, shows the simulated distribution of the residue with quantization noise only, with quantization noise and offset as well as with quantization noise, offset and thermal noise, respectively. As can be seen from Fig. 2.8, the quantization noise results into

errors uniformly distributed over $(-0.5LSB, 0.5LSB)$, as predicted in Section 2.3.1. With offset and thermal noise included, however, the residue is approximately subject to a Gaussian distribution, as the noise performance is usually dominated by the thermal noise in a well-designed ADC.

2.3.5 Differential and Integral Non-Linearity

Differential non-linearity (DNL) and integral non-linearity (INL) describe the deviation of a practical quantizer from an ideal one after eliminating offset and full-scale errors. Specifically, DNL is the deviation of each code from its ideal width. While INL is the deviation of each code transition from its ideal location. Fig. 2.9 illustrates the concept of DNL and INL.

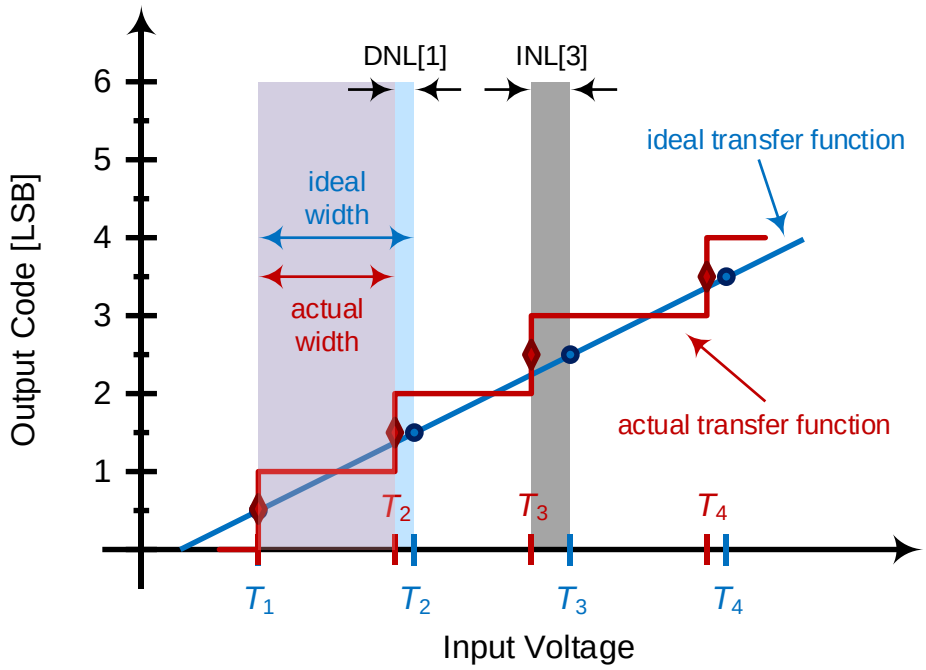


Figure 2.9. An example of DNL and INL of an ADC.

Mathematically, the DNL and INL are defined as

$$DNL[i] = \frac{T[i+1] - T[i]}{LSB} - 1, \;\; i = 1, 2, ..., 2^N - 2 \tag{2.20}$$

and

$$INL[i] = \sum_{k=1}^{i-1} DNL[k], \;\; i = 2, 3, ..., 2^N - 1, \tag{2.21}$$

respectively. Though both DNL and INL are deterministic errors, their measurements require multiple times of averaging to rule out the effect of random noise, which can be much larger than non-linear errors in actual implementations.

The code transitions can be measured by applying an extremely slow ramp input. However, it may not be an easy task to generate the required ramp signal with enough accuracy. In addition, AC decoupling capacitors are commonly placed before the ADC input in measurement setups for on-chip or on-board common-mode supply. This unfortunately poses a lower limit to the frequency of the ramp signal and thus affects the measurement accuracy. A more popular approach to pinpointing the transitions is to apply a sine wave as the input [23]. By collecting the ADC output and keeping track of the sample number in each code bin. The code transitions are then given by

$$T[k] = C - A\cos\left[\frac{\pi \times H_c[k-1]}{S}\right], \;\; k = 1, 2, ..., 2^N - 1, \tag{2.22}$$

where A and C are the amplitude and offset of the sine wave, respectively. S is the total number of received samples and $H_c[j]$ the cumulative histogram given by

$$H_c[j] = \sum_{i=0}^{j} H[i], \tag{2.23}$$

where $H[i]$ is the total number of samples received in code bin i.

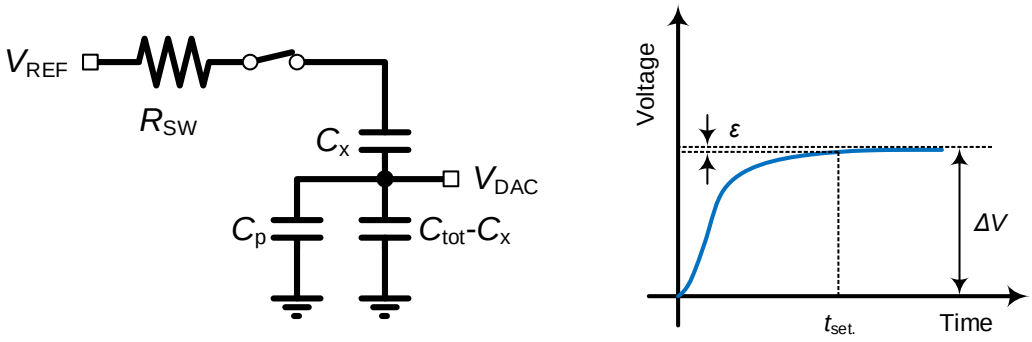


Figure 2.10. DAC settling model.

2.3.6 Incomplete DAC Settling

The capacitive DAC (CDAC) along with the DAC driver can be modeled as an R-C network. When DAC switching takes place, it requires a certain amount of time to settle to a given accuracy, this time is called the DAC settling time. Fig. 2.10 shows the DAC settling model. As the switch is turn on, a voltage step is injected into the network. Assuming a single-pole response, the transfer function can be derived as

$$\frac{V_{DAC}}{V_{REF}} = \frac{C_x}{C_{tot}+C_p} \cdot \frac{1}{1+sR_{SW}\dfrac{\left(C_{tot}-C_x+C_p\right)C_x}{C_{tot}+C_p}}, \tag{2.24}$$

where C_x is the capacitance being switched, C_{tot} is the total capacitance of the CDAC, C_p is the parasitic capacitance on the summing node, including the input capacitance of the comparator and the parasitic capacitance caused by routing, and R_{SW} is the on-resistance of the switch. The settling time is given by the equation

$$t_{set.} = -\tau \cdot \ln\frac{\varepsilon}{\Delta V}, \tag{2.25}$$

where τ is the timing constant of the R-C network and is given by

$$\tau = R_{SW} \frac{\left(C_{tot} - C_x + C_p\right) C_x}{C_{tot} + C_p}. \tag{2.26}$$

ε is the settling error and ΔV the difference between the final and initial voltages expressed as

$$\Delta V = V_{REF} \cdot \frac{C_x}{C_{tot} + C_p}. \tag{2.27}$$

Generally, it is desired to suppress the settling error ε to less than $\frac{1}{2} LSB$ to avoid accuracy degradation. According to Eqn. (2.25), the settling time requirement is gradually relaxed as the conversion proceeds from MSB to LSB. However, the timing budget might be really tight in high-speed implementations. If the DAC settling is not able to complete before the comparison is triggered, a possible decision error will occur.

2.3.7 Reference Ripples

Ideally, we would assume that the reference of a SAR ADC is a noiseless DC voltage that absorbs any high-frequency components including AC noise and transient spikes. However, the actual reference voltage can be an error source itself and should be factored in when budgeting the total ADC errors. The thermal noise on the reference is usually insignificant since the reference should be stabilized by a large capacitor or supplied by a voltage buffer with a low output impedance. Either way, the thermal noise voltage is negligible in comparison to other noise sources. The transient ripple, on the other hand, is another story. Since every time a capacitor in the CDAC is connected to the reference, a portion of the charge will be drawn by the capacitor and a reference ripple will occur. To suppress this ripple, either a sufficiently large capacitor or an

adequately fast buffer is needed, introducing high area or power overhead. How to inflict enough suppression on the reference ripple without a significant overhead is still an active research topic.

The insufficiently suppressed reference ripple will finally be coupled to the comparator input and cause spurs in the spectrum of the ADC output. As per the operation theory of SAR ADCs, the reference voltage is attenuated by a code-dependent factor before being subtracted from the sampled input in each conversion cycle. Hence the bit-wise errors introduced by reference ripple is also code-dependent and can be analyzed on a per-cycle basis with the help of Fig. 2.11. Before any DAC switching takes place, any disturbance on the reference voltage is equally coupled to the differential output of the DAC. However, as soon as the DAC switching takes place, the

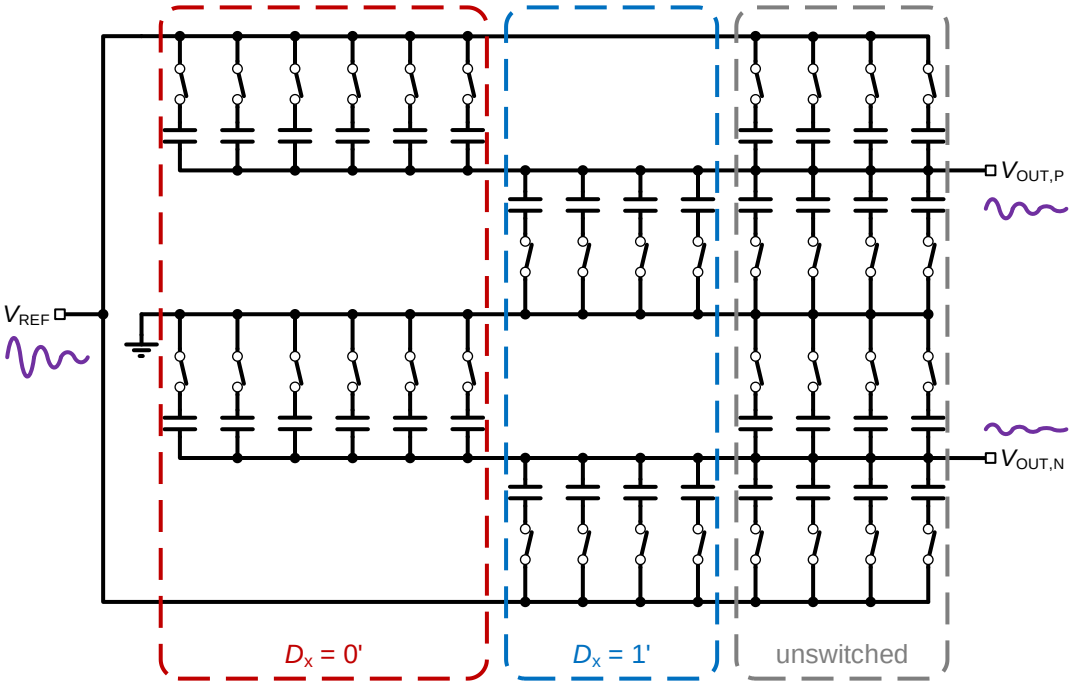


Figure 2.11. Bit-wise reference ripple error.

gain of the voltage divider formed by the capacitor array changes, causing unbalanced coupling and thus differential error, which can be expressed as

$$V_{e,diff} = \frac{-\sum_{i=1}^{N-1} D_i C_i}{C_{tot} + C_p} \cdot V_{rpl}\,, \tag{2.28}$$

where D_i is subject to

$$D_i = \begin{cases} 1, & V_{COMP} = 1 \\ -1, & V_{COMP} = 0 \\ 0, & unresolved \end{cases}. \tag{2.29}$$

Hand calculation of the performance degradation caused by reference disturbance can be quite cumbersome. Therefore, extensive simulations are usually required in the reference design of SAR ADCs.

2.3.8 Interleaving Errors

As briefly mentioned in Section 2.1.5, the signal restoration of a TI ADC is based upon cancellation of the aliasing caused by sub-sampling. However, a perfect cancellation is impossible in actual implementations. Any mismatch among the ADC channels will lead into residual aliasing, which is often referred to as interleaving spurs. Generally, the interleaving spurs may stem from three source, namely inter-channel offset mismatch, gain mismatch and timing mismatch. With these error sources taken into account, the time-domain representation of the sampled voltage in the *i*th channel is

$$v_i(t) = A_i\left[v_{IN}(t) + v_{off,i}\right] \cdot \sum_k \delta\left[t - kMT - (i-1)T - \Delta t_i\right],\ i = 1, 2, ..., M\ , \tag{2.30}$$

where A_i is the gain, $v_{off,i}$ is the offset and Δt_i is the timing skew. M is the total number of channels and $T = \frac{1}{f_S}$ is the sampling clock period of the overall ADC. The corresponding frequency-domain representation is

$$V_i(f) = \frac{1}{MT}\left[A_i V_{IN}(f) + v_{off,i}\right] * \sum_k \delta\left[f - \frac{kf_S}{M}\right] e^{-j2(i-1)\pi fT} e^{-j2\pi f\Delta t_i}. \quad (2.31)$$

The frequency-domain interleaving errors can then be derived as

$$V_{e,TI} = \sum_{i=1}^{M} V_i(f) - \left[A_{ref} V_{IN}(f) + \frac{v_{off,ref}}{T}\sum_k \delta\left(f - kf_S\right)\right]. \quad (2.32)$$

where A_{ref} and $v_{off,ref}$ are the best-fit gain and offset of the ADC output found with a sine-fit algorithm. Specifically, the offset-introduced spurs are given by

$$V_{e,off} = \sum_{i=1}^{M}\left[\frac{v_{off,i}}{MT}\sum_k \delta\left(f - \frac{kf_S}{M}\right) e^{-j2\pi f[(i-1)T+\Delta t_i]}\right] - \frac{v_{off,ref}}{T}\sum_k \delta\left(f - kf_S\right). \quad (2.33)$$

It is not difficult to see that these spurs located at $\frac{kf_S}{M}$ for $k = 0, 1, ..., M-1$. The spurs resulted from gain and timing mismatches can be expressed as

$$V_{e,gain\&skew} = \sum_{i=1}^{M}\left[\frac{A_i V_{IN}(f)}{MT} * \sum_k \delta\left(f - \frac{kf_S}{M}\right) e^{-j2\pi f[(i-1)T+\Delta t_i]}\right] - A_{ref} V_{IN}(f). \quad (2.34)$$

The gain and skew spurs are located at $\frac{kf_S}{M} \pm f_{IN}$ for $k = 1, 2, ..., M-1$.

Another error source associated with interleaving is the bandwidth mismatch. This error can be regarded as a combination of gain and skew mismatch, as can be analyzed with the help of Fig. 2.12. Assuming a sampling network with a sinewave

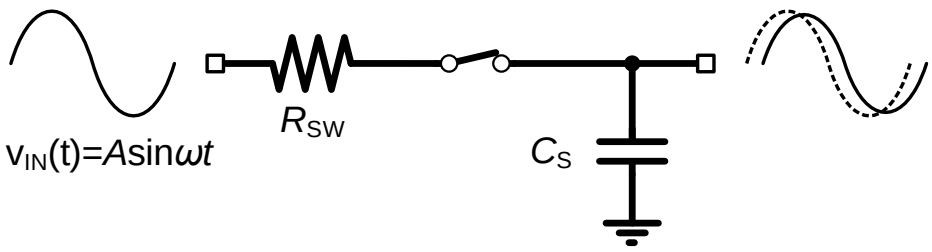


Figure 2.12. The effect of bandwidth on gain and skew.

input of $A\sin\omega t$. According to the I-V relationship of the resistor and capacitor, we can have a difference equation

$$\frac{dv_{OUT}(t)}{dt}+\frac{1}{R_{SW}C_S}v_{OUT}(t)=\frac{1}{R_{SW}C_S}v_{IN}(t). \tag{2.35}$$

By solving Eqn. (2.35), the time-domain output waveform can be found as

$$v_{OUT}(t)=\frac{A}{\sqrt{1+\left(\omega R_{SW}C_S\right)^2}}\cdot\sin\left[\omega t-\arctan(\omega R_{SW}C_S)\right]+c\cdot e^{-\frac{t}{R_{SW}C_S}}, \tag{2.36}$$

where $c\cdot e^{-\frac{t}{R_{SW}C_S}}$ is an error term dependent on initial state. If assuming enough tracking time, this error term is negligible due to sufficient settling. However, the output signal is attenuated by a factor of $\frac{1}{\sqrt{1+\left(\omega R_{SW}C_S\right)^2}}$ and phase-shifted by $\arctan(\omega R_{SW}C_S)$.

Thus if there is any noticeable difference in the 3-dB bandwidth $\frac{1}{R_{SW}C_S}$ among the interleaved channels, a mismatch in the gain and phase (timing) can be observed.

2.4 Design Techniques for High-Speed SAR-Based ADCs

2.4.1 Loop-Unrolling

Conventionally, a single comparator would be used throughout the conversion phase of a SAR ADC. It simplifies the design and does have any noticeable downside if operation speed is not one of the top priorities. In high-speed designs, however, this can potentially limit the maximum conversion rate of the overall architecture. Since the comparator needs to be reset before being re-triggered to erase any memory effect from the previous sample. If the signal is ready for comparison before the comparator reset is completed, the clock path delay then dictates the per-cycle conversion time.

To eliminate the comparator reset-caused delay, the concept of loop-unrolling is proposed in [24], where each bit cycle is completed with a dedicated comparator and the comparator reset not longer contributes to the critical-path delay. In addition, since each comparator can be directly connected to the CDAC, the need for a demultiplexing stage and thus the associated logic delay can be avoided. The configuration of a loop-

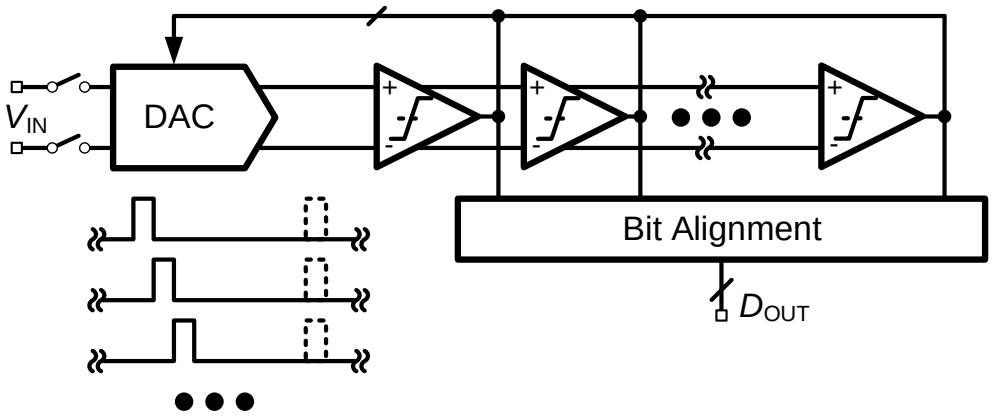


Figure 2.13. Loop-unrolled SAR ADC.

unrolled SAR architecture is depicted in Fig. 2.13. As long as dynamic comparators are used, this technique does not incur extra power. Hence it essentially trades area for speed gain.

The drawback of this architecture is the non-uniform offsets of the comparators. In conventional implementations, the non-zero comparator offset does not pose a problem to the conversion accuracy as it only results into a global offset. However, if multiple comparators with different offset are used during the conversion, a signal-dependent error will occur and degrade the static linearity of the ADC. Thus, either a foreground calibration or a background one is usually required to equalize the offsets.

2.4.2 Two-Bit-Per-Cycle Architecture

According to Eqn. (2.6), conversion time of SAR ADCs is determined by two factors, namely the number of bit cycles and the per-cycle period. Aimed at reducing the effective number of cycles, two-bit-per-cycle SAR architecture was proposed in

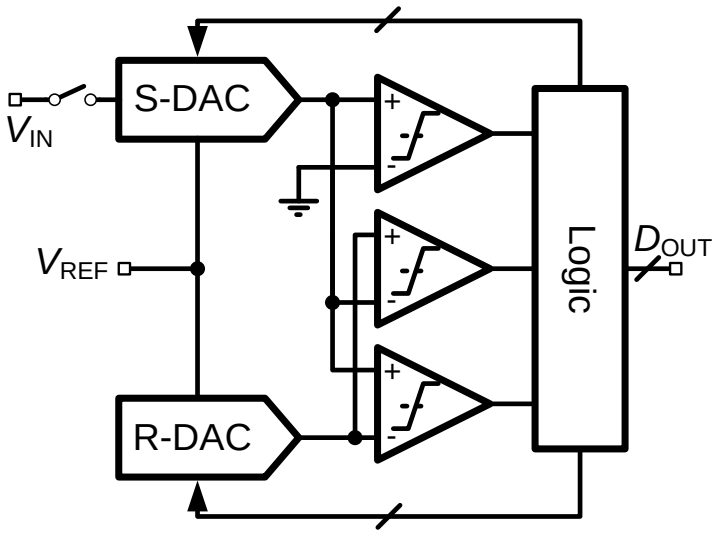


Figure 2.14. Two-bit-per-cycle SAR ADC.

[25]. As shown in Fig. 2.14, the two-bit-per-cycle architecture can be regarded as a combination of a flash ADC and a SAR ADC that utilizes three comparators to resolve 2 bits for each cycle. This theoretically cuts the conversion time by a half.

However, this conversion time truncation does not come free. First, it incurs area overhead as two extra comparators and one extra DAC are required as compared to a conventional SAR architecture. Second, it is known that flash ADC trades power for speed. Hence the semi-flash nature of the two-bit-per-cycle SAR architecture shows inferior power efficiency in comparison to their conventional counterparts. In addition, it loses the benefit of asynchronous timing. As more than one comparators are making decisions simultaneously, it can be very difficult to generate the next-cycle clock edge based on the current-cycle comparison. Finally, as with all other architectures utilizing multiple comparator, it mandates offset calibration to maintain a decent accuracy.

2.4.3 CDAC Redundancy

The operation of conventional SAR ADCs is based on a “pure” binary search algorithm, which does not provide any tolerance for intermediate errors. This can be explained with Fig. 2.15. If for any reason (noise, incomplete settling or reference disturbance) a wrong decision is made during one of the bit cycles, no matter how small the error is, this error will be irreversible and the final output will be wrong. This feature of the conventional binary search-based conversion makes the reference and CDAC designs unnecessarily challenging, confining its applications to low-to-medium-speed domain.

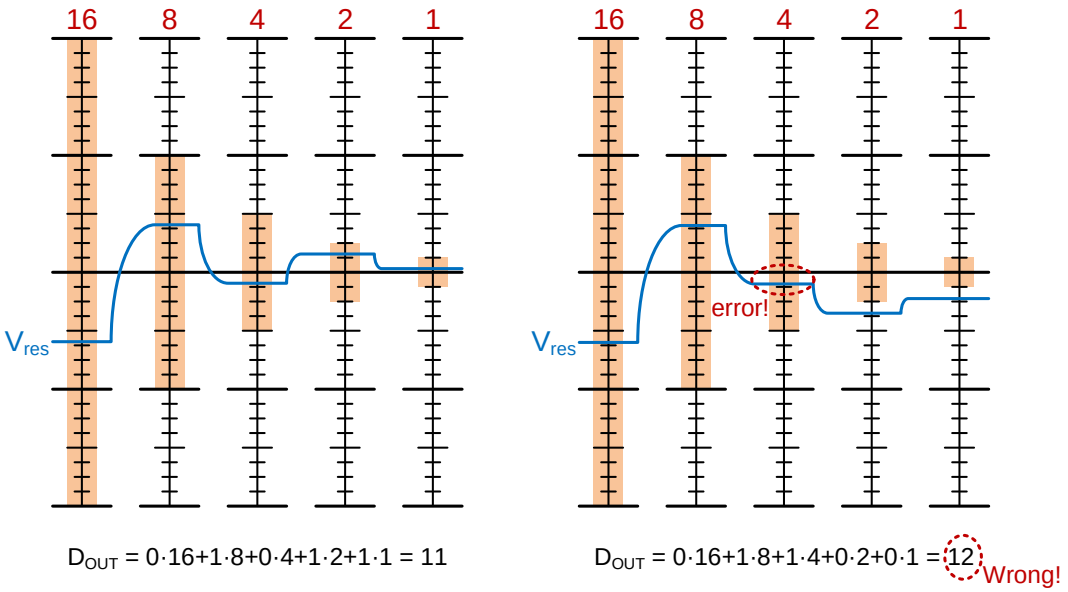


Figure 2.15. Binary search-based conversion trajectory with and without error.

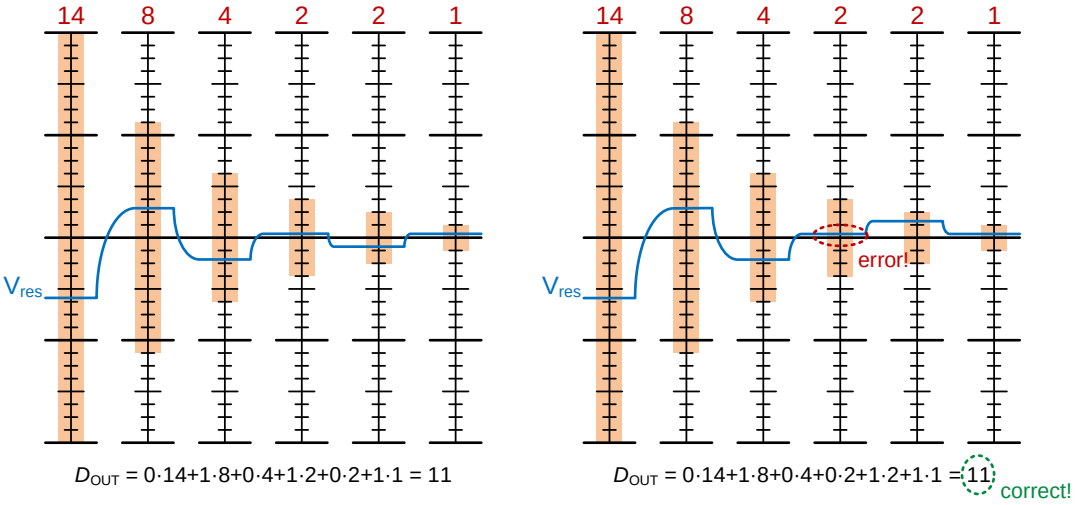


Figure 2.16. Redundant conversion trajectory with and without error.

To overcome the afore-mentioned limitation, CDAC redundancy [26, 27, 28, 29] reconstructs the CDAC to generate a sub-two radix for at least a portion of the bit weights, providing error tolerance for the cycles under coverage, as can be appreciated with the example shown in Fig. 2.17. In this example, the first four cycles are under the

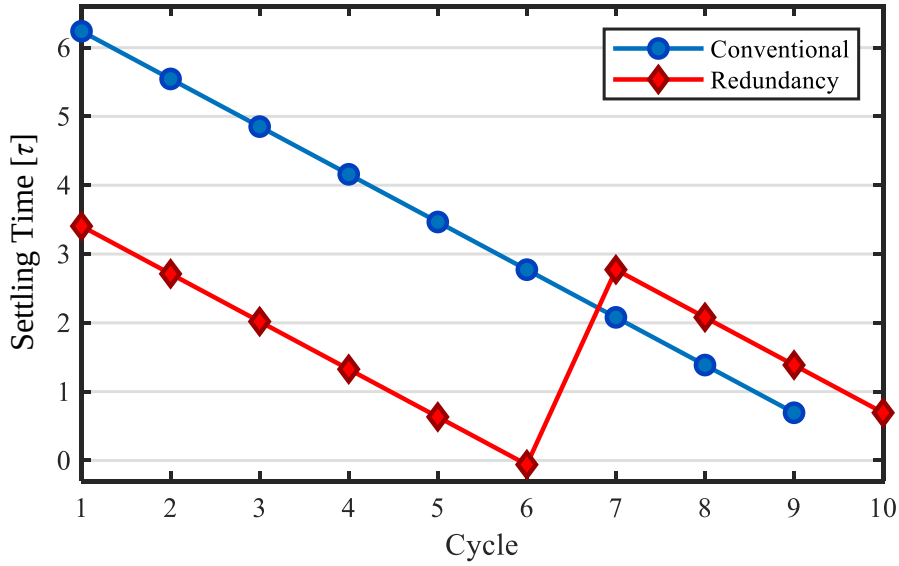


Figure 2.17. Per-cycle settling time requirement with and without CDAC redundancy.

coverage of redundancy. A decision error made during the fourth cycle is compensated in the fifth cycle and a correct final output is generated at the end of the conversion.

Fig. 2.17 shows the required settling time for each bit cycle with and without CDAC redundancy. In the conventional case, though the timing requirement decreases linearly from MSB to LSB cycles, the per-cycle delay dictates only by the worst-case settling for lack of error correction mechanism. This results into a relatively inefficient timing budget. In the implementation with CDAC redundancy, however, the worst-case requirement is greatly reduced, leading to an overall faster conversion.

The cost of this technique is the extra power consumption. Since extra cycles are needed to implement the redundancy, the energy consumed by each conversion is thus increased. In most cases, however, it is deemed as a fair trade in the sense that the power overhead is relatively low in comparison to other speed enhancing techniques.

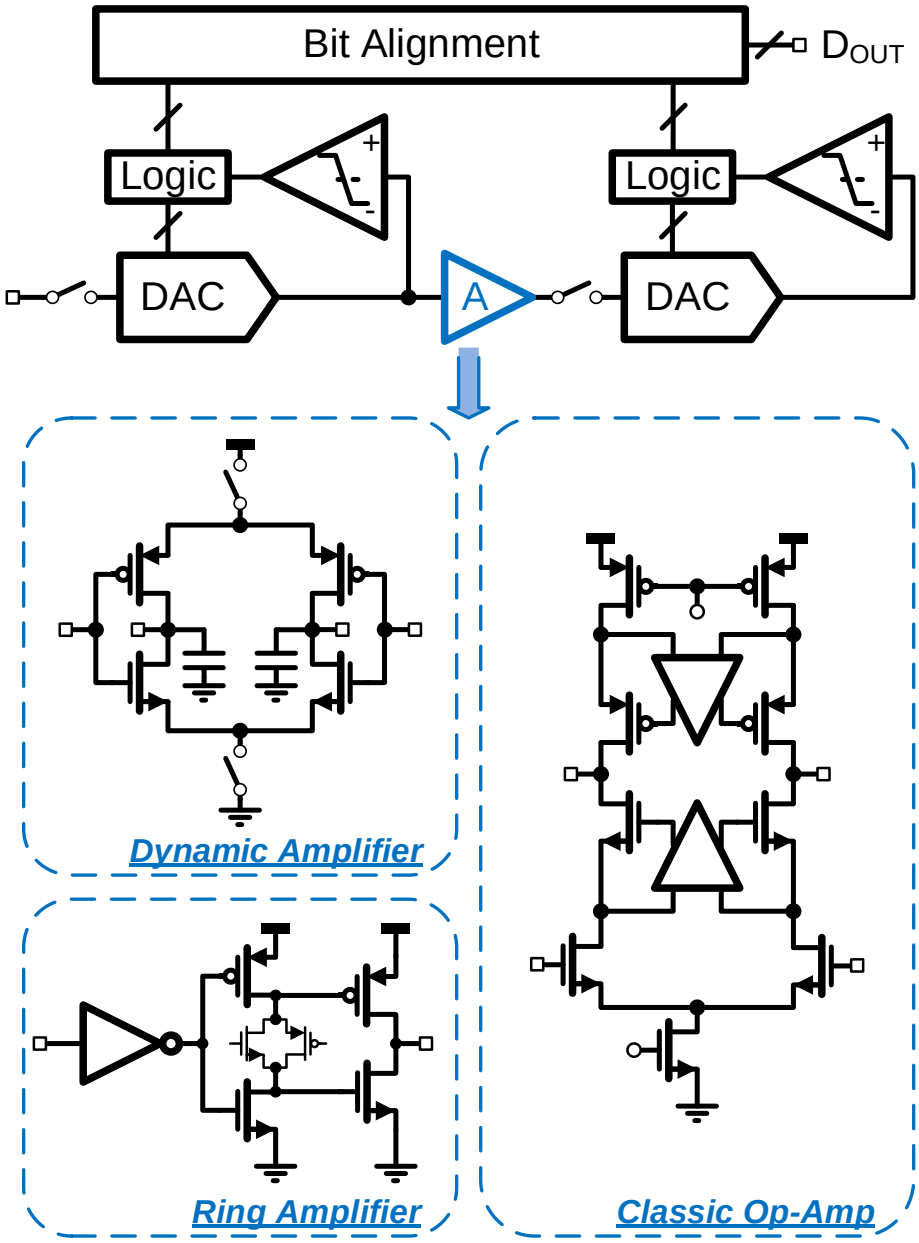


Figure 2.18. Pipelined SAR ADC.

2.4.4 Pipelined SAR Hybrid Architecture

The idea of pipelined SAR architecture [30] is to break the long series of SAR cycles into two or more steps and timing these conversion steps in a pipelined manner

for better tradeoff between resolution and speed. The block diagram of a two-stage pipelined SAR ADC is illustrated in Fig. 2.18. Two SAR stages are interfaced by an active amplifier for residue amplification, which can be extremely crucial in meeting the SNR requirement of some high-precision or low-supply applications. The architecture in question can be readily derived from a conventional pipelined ADC by implementing the sub-ADC as a SAR ADC.

Due to the similarity to the conventional pipelined ADCs, pipelined SAR ADCs inherit the design challenge of high-precision and high-speed analog amplification. When the concept of pipelined SAR architecture was first brought up, the classic op-amp (telescopic, folded-cascode, two-stage etc.) was directly adopted from the conventional pipelined ADCs for residue amplification. However, due to its analog nature, several issues manifest themselves as the downscaling of CMOS progresses. First, the amplifier DC gain is greatly reduced in advanced technology nodes because of channel length modulation. This creates a larger gain error when the op-amp is used in a closed loop. Also, the closed-loop gain can be more sensitive to gain variations. It is well known that the closed-loop gain is given by

$$A_{cl} = \frac{A_{ol}}{1+\beta A_{ol}}, \tag{2.38}$$

where A_{ol} is the open-loop gain and β the feedback factor, which is usually the capacitance ratio of the voltage divider. It can be seen from Eqn. (2.38) that any variation in A_{ol} is attenuated by a factor of $1+\beta A_{ol}$. For a large A_{ol}, the closed-loop gain A_{cl} is relatively flat over a wide voltage range. If A_{ol} is low, on the other hand, not

only does A_{cl} deviate from the ideal value $\frac{1}{\beta}$ significantly, but also it shows a higher dependence on A_{ol} and its variation. This introduces a gain error of second or higher order and can not be fully compensated with a first order calibration mechanism. Apart from the DC gain degradation, the low supply voltage of the advanced nodes poses a hard limit on the voltage headroom, which in turn limits the output swing of the amplifier and thus lowers the SNR for a certain noise budget. In addition, the reduced headroom enlarges the gain variation, aggravating the situation even more.

The afore-mentioned issues can be partly overcome by introducing non-conventional amplification solutions as such ring amplifiers and dynamic amplifiers, which greatly alleviate the headroom issue as no transistor stacking is required. However, as the gain of these amplifiers are more subject to PVT variations, the extra design complexity induced by gain calibrations is inevitable.

CHAPTER III

TWO-STEP SAR WITH FAST NOISE REDUCTION

3.1 Motivation

High-speed and medium-resolution ADCs are in great demand in wideband communication systems, where SAR-based architectures are attractive options due to the renowned high power efficiency and mostly digital configuration, which are considered as continuously expanded advantages as the technology node advances. However, as the only analog circuits in most SAR-based ADCs with medium resolutions, the comparators still consume a large portion of the total power to meet the stringent noise requirement imposed by a few critical comparisons. Adaptive-tracking-averaging [31] dramatically decreases the power consumption of the comparator by repeatedly performing the LSB conversion and applying averaging to suppress the equivalent input-referred noise. The data-driven noise-reduction technique [32] senses the critical comparisons during conversion by continuously observing the regeneration time of the comparators and comparing it to a preset threshold. The identified critical comparisons are then repeated 4 more times and the final output is generated with majority voting for noise suppression. These techniques improve the power efficiency by employing relatively noisy comparators for non-critical comparisons while selectively suppressing the comparator noise for critical ones. However, the degraded conversion rate due to the extra bit cycles is too high a price for high-speed applications.

SAR-assisted digital-slope ADC [33] takes advantage of the low noise nature of the digital-slope operation and achieves excellent power efficiency in high precision domain. However, the relatively slow operation speed of the digital-slope stage still makes it less attractive in GS/s operations without excessive interleaving.

In this chapter, we present a two-step partially interleaved loop-unrolled SAR ADC. A fast noise reduction technique is proposed to selectively suppress the comparator noise for critical comparisons. A modified StrongARM latch is adopted to further reduce the comparator noise. The gain error and mismatch induced by the partially interleaved architecture, together with the non-uniform offsets of the comparators, are addressed by calibration procedure constantly running in the background. Fabricated in a 28 nm FDSOI process, the ADC achieves a SNDR of 46.65 dB and a SFDR of 59.08 dB with a Nyquist input, while consuming 2.1 mW from a 1.1 V power supply. This translates into a Walden FOM of 12.01 fJ/conv.-step.

3.2 ADC Architecture

The architecture and timing diagram of the proposed ADC are shown in Fig. 3.1. The first stage carries out a 4-bit coarse quantization and generates the residue. The second stage consists of two 5-bit sub ADCs that operate in an alternate manner to enable the non-attenuated passive residue transfer [34]. The 5-bit quantization is completed in 6 conversion cycles with a 1-bit inter-stage redundancy and a 1-bit intra-stage redundancy. Loop-unrolled architecture is adopted for both stages to obviate the delay that would otherwise be imposed by the SAR logic and comparator reset time.

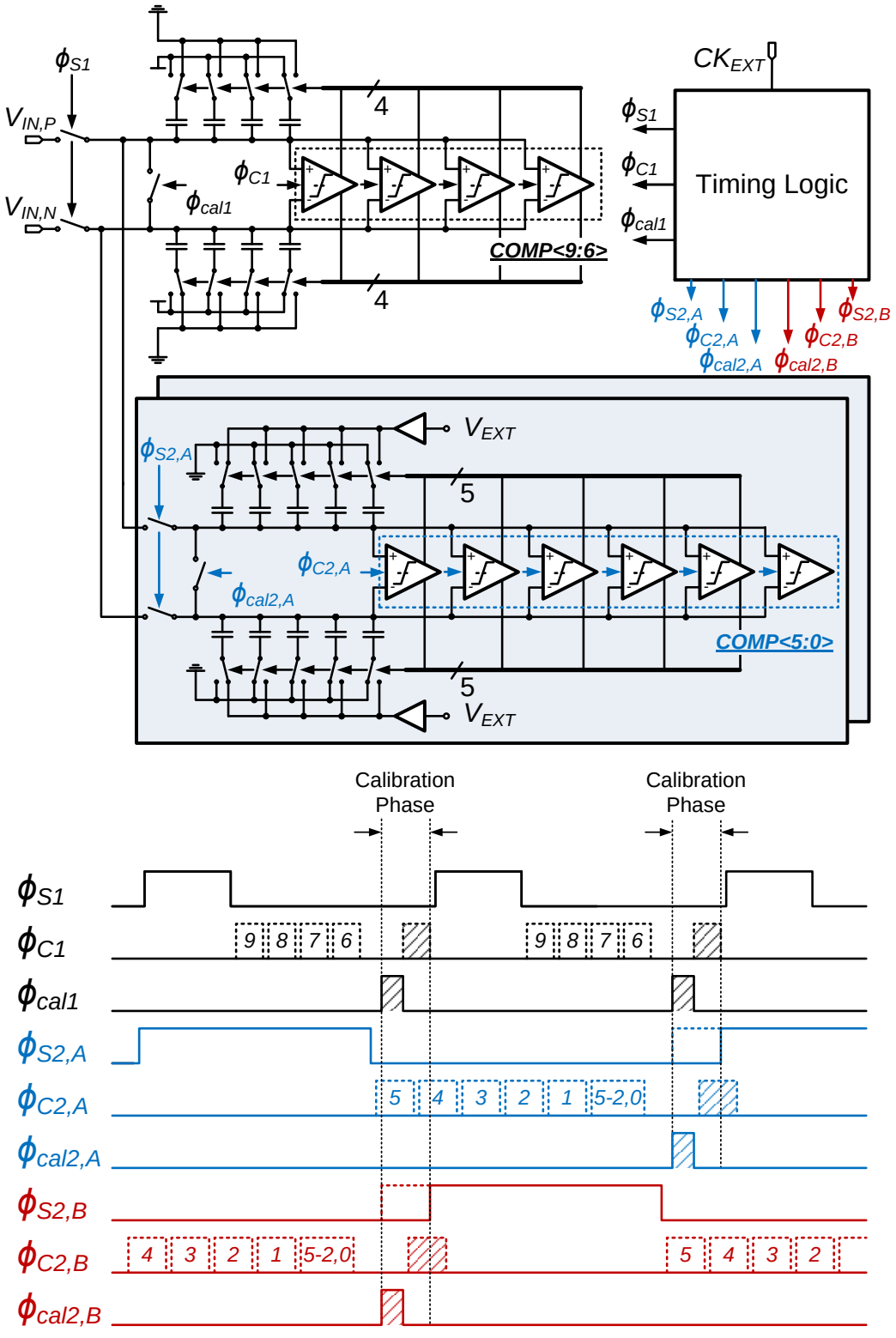


Figure 3.1. Architecture and timing diagram of the proposed ADC.

The last comparison in the second stage is performed by 5 comparators simultaneously to enable majority voting for a 2× noise suppression [32], as will be detailed in Section 3.3. The supply voltage (1.1 V) is used as the reference in the first stage. Since the residue is transferred to the second stage without any active gain, the reference voltage needs to be scaled down in the second stage and is thus provided by a set of reference buffers. To address the non-uniform offsets of the comparators and the inter-stage gain error, the ADC conversion is followed by a calibration phase, where either the offset calibrations of two stages are carried out simultaneously or the gain error is extracted and fed back to the reference buffer for gain alignment.

3.3 Fast Noise Reduction

Though a single comparator is usually employed for the whole conversion to simplify the design in conventional implementations, the comparator noise requirement varies significantly from bit to bit in the SAR algorithm, depending on the amplitude of the residue voltage. With properly sized comparators, the noise requirement is most critical in one bit cycle only [32]. However, it is not known in advance which comparison is the most noise-critical one since it differs from sample to sample. Detection of the noise-sensitive comparison increases the implementation complexity, especially when multiple comparators are used for enhanced operation speed.

Fortunately, decision errors, whether they are originated from noise or settling, can be absorbed by redundancy provided that the errors do not exceed the redundancy range and the conversion is free of errors in bit cycles that are not covered by

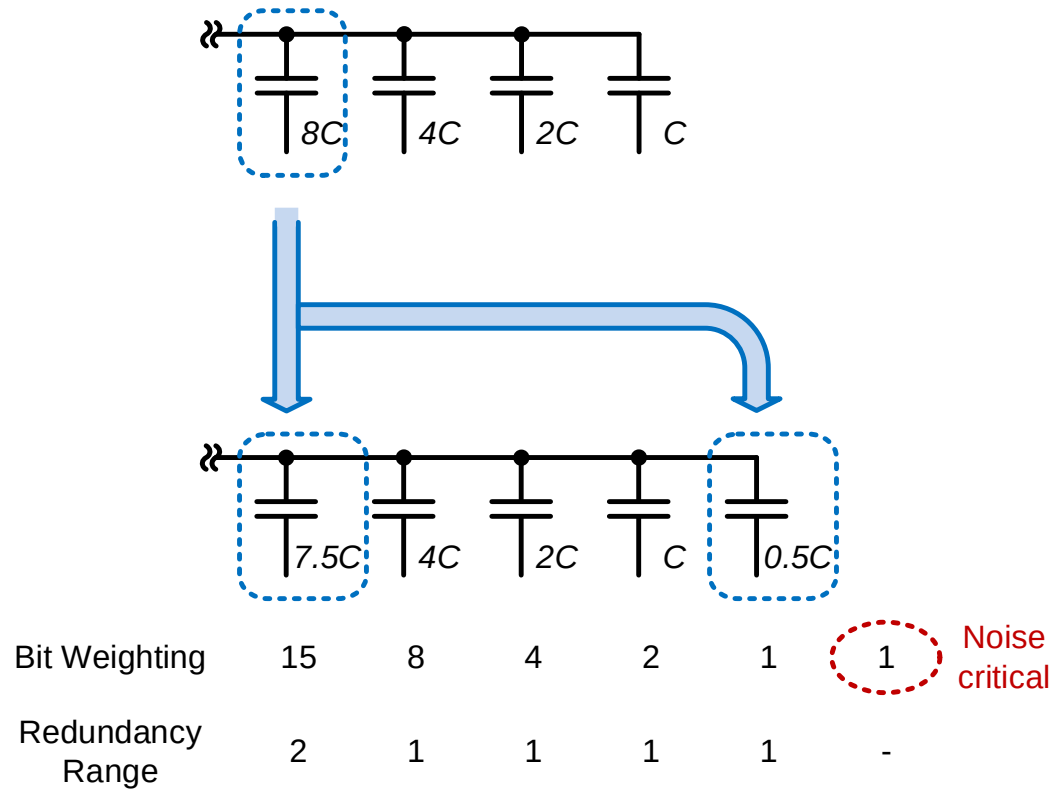


Figure 3.2. Construction of the redundant CDAC.

redundancy. In this work, the capacitor sizes in the second stage are 15, 8, 4, 2 and 1 unit(s), as shown in Fig. 3.2. This introduces a 1-LSB redundancy to the first 5 bit cycles. Since the settling requirement is greatly relaxed for the second stage, the redundancy is utilized to absorb errors due to noise only. As such, only the last cycle is not under the coverage of redundancy and mandates a low-noise comparator. While the noise requirement in the first 5 cycles is relaxed by a factor of 2, this theoretically translates into a ¾ power saving. In this work, instead of directly using a low-noise comparator, the last comparison is performed by 5 comparators (COMP<5:2> and COMP<0>) simultaneously. The raw outputs of the 5 comparators are then applied to a majority voting logic, where the final decision is generated. The benefits of this scheme

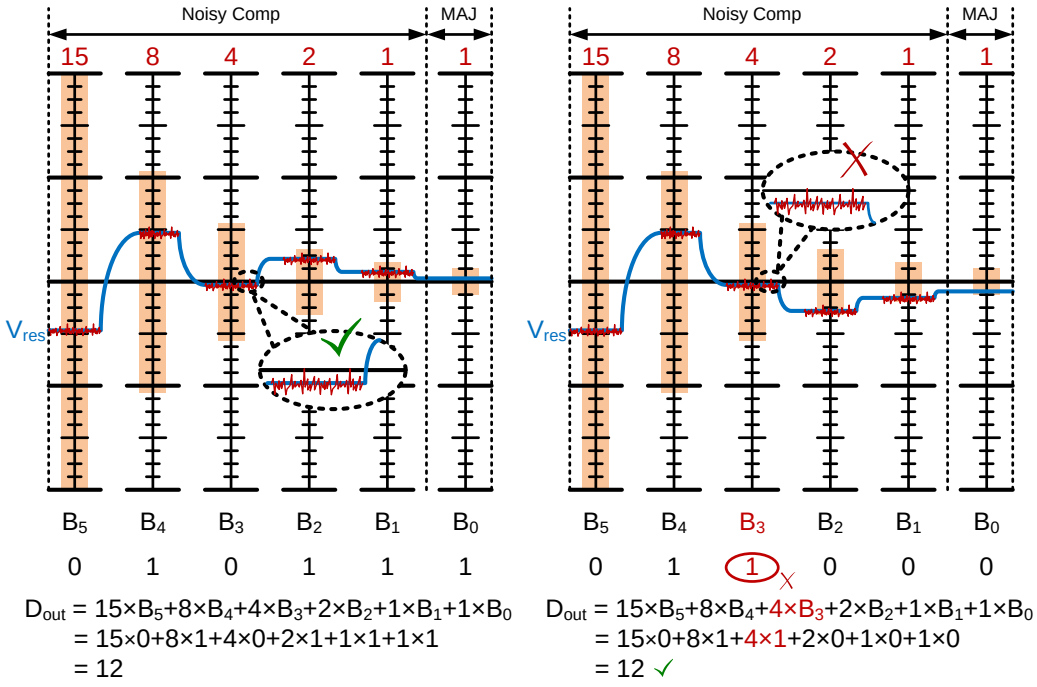


Figure 3.3. Redundancy-based noise-tolerant conversion.

are three-fold. First, not only the comparator noise, but also the noise from DAC and offset calibration process is suppressed. Second, the benefit of high-speed operation from loop-unrolled architecture is retained without area penalty, as no area-consuming low-noise comparator is really introduced. In addition, no demultiplexing stage is required between the reused comparators (COMP<5:2>) and the DAC, since the last bit comparison is not followed by DAC switching. Third, the design complexity is reduced. As illustrated in Fig. 3.3, as long as a correct decision can be made in the last cycle, the final result will be correct regardless of whether a decision error has been made during the noise-critical comparison from the first 5 cycles. The non-binary raw code of the ADC can be converted to the final binary output code with the help of only a few full adders, since the DAC shares an identical total weight with that of a conventional binary implementation.

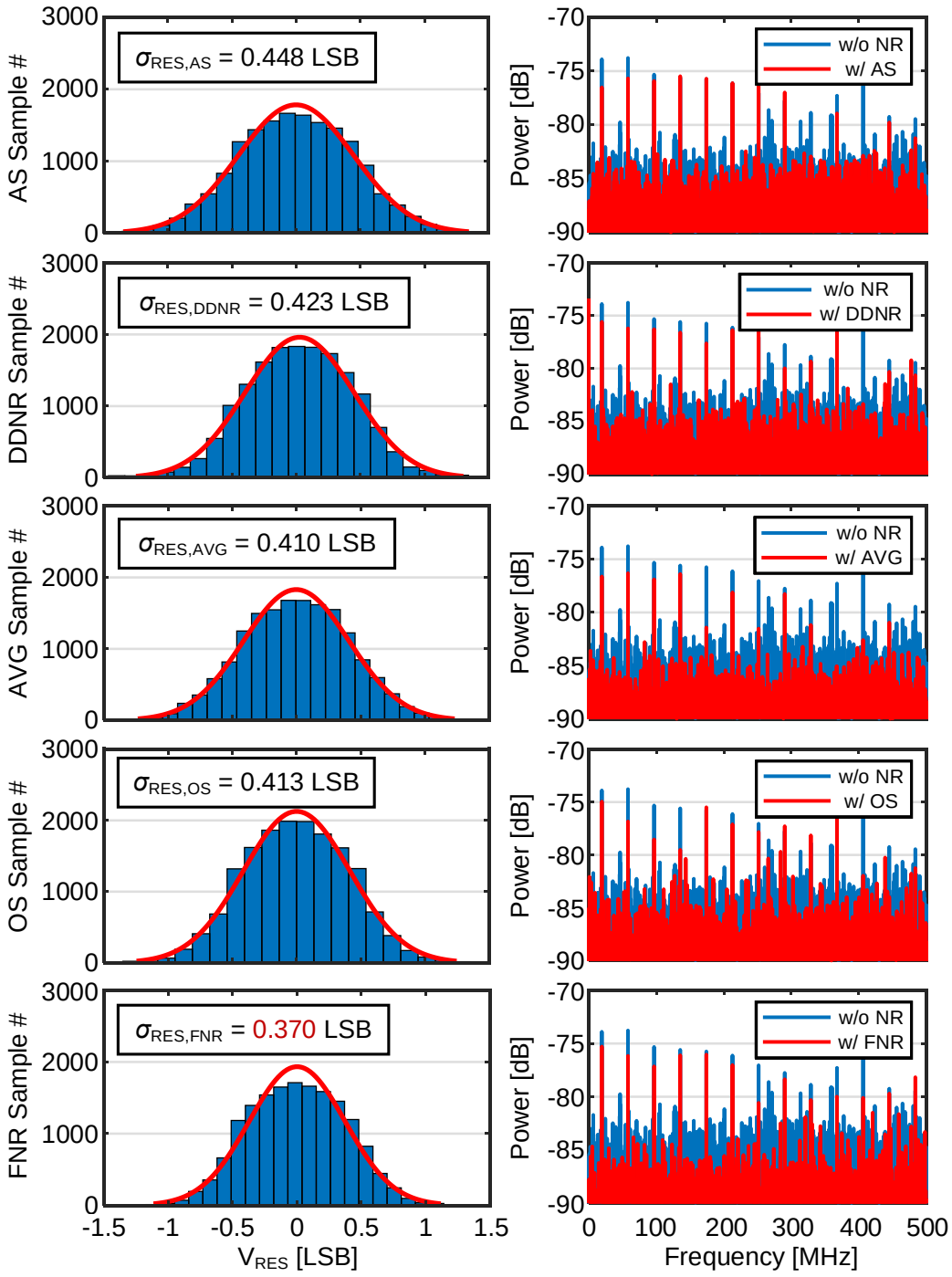


Figure 3.4. A comparison of residue and noise floor of fast noise reduction and other noise reduction techniques.

To theoretically evaluate the effectiveness of the fast noise reduction technique,

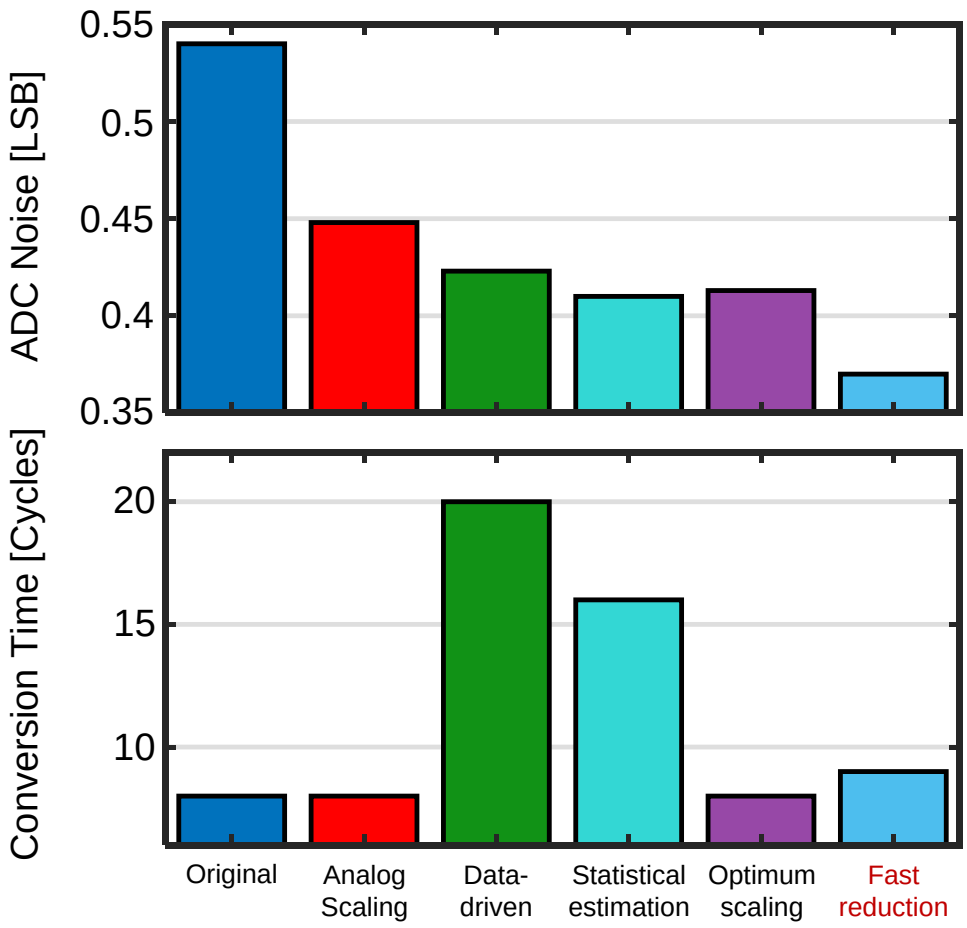


Figure 3.5. A comparison of the ADC noise and conversion time with different noise reduction techniques.

a behavior model simulation is conducted to compare the noise suppression effect of the proposed technique (FNR) against those of brute-force analog scaling, data-driven noise reduction (DDNR) [32], adaptive-tracking-averaging (AVG) [31] and optimum comparator scaling (OS) [35]. Assuming a four-time analog scaling suppresses the comparator input-referred noise by a factor of two, and the comparators in each technique are sized to maintain a same power consumption for all five cases. Fig. 3.4

shows the simulated residue (including quantization noise and thermal noise, as explained in Section 2.3.4) distribution and the corresponding power spectrum. The fast noise reduction achieves the lowest noise among all five techniques, as can be observed from both the distribution histograms and the frequency-domain plots. Fig. 3.5 compares the noise performance and the conversion times in the form of a bar plot. Comparing with techniques relying on repeated cycles (data-driven noise reduction and adaptive-tracking-averaging), the proposed technique shows a large advantage in terms of conversion time, as only one more cycle is needed to enable the noise reduction. When compared against solutions based upon design scaling (brute-force analog scaling and optimum comparator scaling), this technique is slightly slower, but achieves a much better effect of noise suppression. It is worth noting that though the optimum comparator scaling technique shows a much better noise performance than the brute-force analog scaling in this simulation, it is practically impossible to implement because it requires a scaling factor of $\sqrt{2}$ between adjacent conversion cycles.

3.4 Calibration Scheme

Since multiple comparators with small sizes are adopted in the ADC, the resulted offset variation from bit to bit degrades the linearity of the ADC if left uncalibrated. In addition, the ping-pong second stage of the ADC can potentially introduce an inter-stage gain error due to the unmatched capacitor sizes or/and the different reference voltages, which manifests itself in the form of a gap in the ADC transfer function.

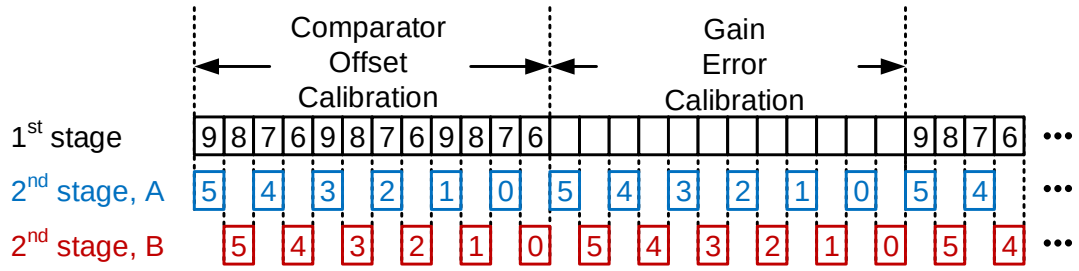


Figure 3.6. Calibration scheme.

To address both the offset and gain mismatch, a calibration phase is triggered upon completion of the conversion on a per-sample basis. The calibration scheme is depicted in Fig. 3.6. Offset and gain calibrations are carried out alternately. The offset calibration mode lasts for 12 clock cycles before toggling to the gain calibration mode and vice versa.

The gain calibration is executed in 3 steps, as can be seen from Fig. 3.7. Firstly, only one side (the positive side in the example) of DAC2 is connected to DAC1 through the second-stage sampling switch. Secondly, the reset switches turn on, equalizing the charge on both sides of the DAC. In the meantime, the bottom plates of all capacitors are reset to the default positions. Thirdly, the bottom plate of the LSB capacitor from the positive side of DAC1 is switched from V_{DD} to GND. While the MSB capacitor from the negative side of DAC2 is switched from V_{REF} to GND. Since in ideal cases, the MSB in the second stage should have the same weight as the LSB in the first stage due to the inter-stage redundancy, the top-plate voltages V_P and V_N should show zero difference. In the presence of gain error, however, the comparator in the second stage would see a non-zero input. The corresponding output can hence be used to drive the reference voltage towards the direction where the gain error is minimized. In this work,

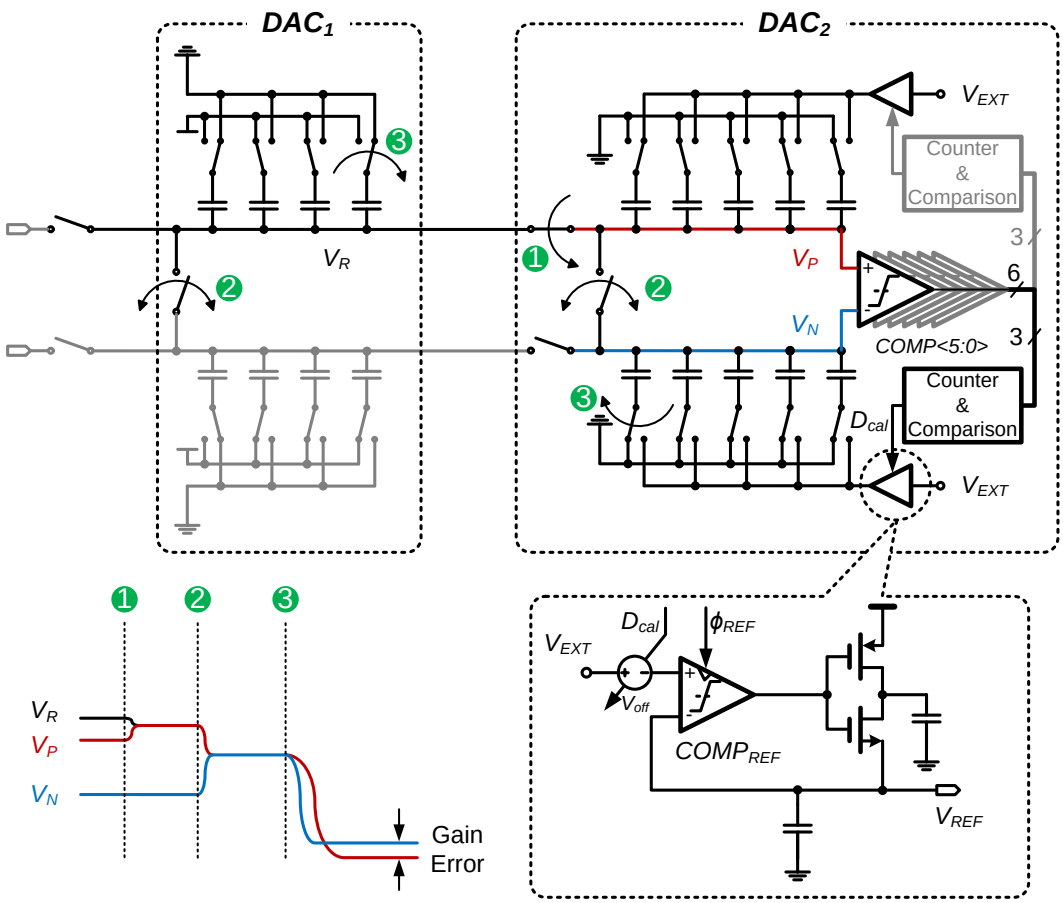


Figure 3.7. Proposed gain calibration.

the comparator output is accumulated and averaged before being fed to the reference buffer to alleviate the effect of noise and residual offset. The reference buffer adopts a comparator-based low-power architecture [36] with a programmable reference voltage, whose value is readily controlled by adjusting the offset of $COMP_{REF}$.

Based upon the gain calibration, the comparator offset calibration can be readily implemented with only a little modification. Generally, the 3 steps described in the gain calibration procedure are also carried out in sequence to extract the comparator offset. However, the DAC switching in the third step is disabled to rule out the impact of the remnant gain error. In addition, the comparator decisions are fed to the locally

positioned offset trimming circuits instead of the reference buffers. Such an arrangement enables simple toggling between the two calibration modes with only a few extra logic gates and switches.

3.5 Circuit Implementation

3.5.1 Dynamic Comparator

A modified version of StrongARM latch is used as comparators in the second stage and the reference buffers. The schematic is shown in Fig. 3.8. An extra input pair, along with a pair of charge pumps, are added to the latch for offset calibration. The multiple switches connected in series decreases the calibration step and thus the calibration noise [37]. Different from the conventional implementation, the modified latch is driven by two clocks. The tail current transistor (M_1) and two pullup switches (M_2 and M_3) are driven by clock CK, while the reset switches (M_4 and M_5) are controlled by CK_d, a delayed version of clock CK. This effectively extends the amplification phase of the comparator, leading to a reduced input-referred noise.

Conventionally, since switches M_2, M_3, M_4 and M_5 are released simultaneously, the amplification phase of the comparator comes to an end as soon as the drains of the input pair are discharged to V_{DD}-$|V_{TH,P}|$. As the cross-coupled transistors are turned on, the comparator is brought to the regeneration phase and the input pair quickly enter triode region, terminating the amplification procedure. Hence, the amplification time can be expressed as

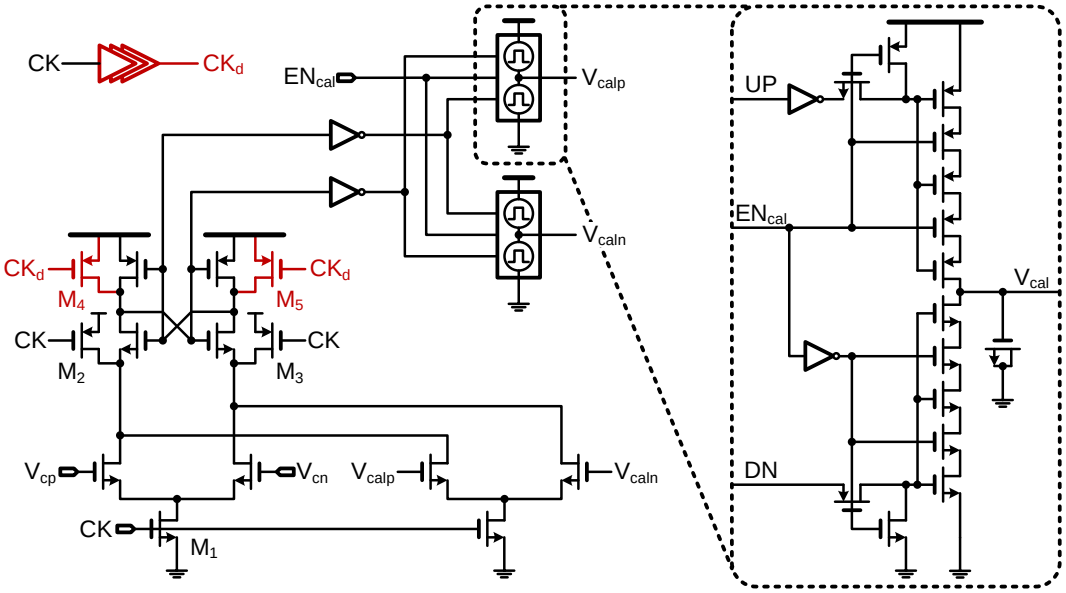


Figure 3.8. Comparator used in second stage and reference buffer.

$$\Delta t_A = \frac{C_P \cdot |V_{TH,P}|}{I_{DS}}, \tag{3.1}$$

where C_P is the parasitic capacitance seen at the drain of the input pair and I_{DS} is the average current flowing through the input pair. The gain of a dynamic amplifier is given by

$$A_V = \frac{g_m}{C_P} \cdot \Delta t_A . \tag{3.2}$$

When driven by a delayed clock, switches M_4 and M_5 can serve as current sources and provide current paths to the input pair even if the cross-coupled pair are turned on. The amplification time can then be approximated as

$$\Delta t_A = \max\left[\Delta t_d , \frac{C_P \cdot |V_{TH,P}|}{I_{DS}} \right], \tag{3.3}$$

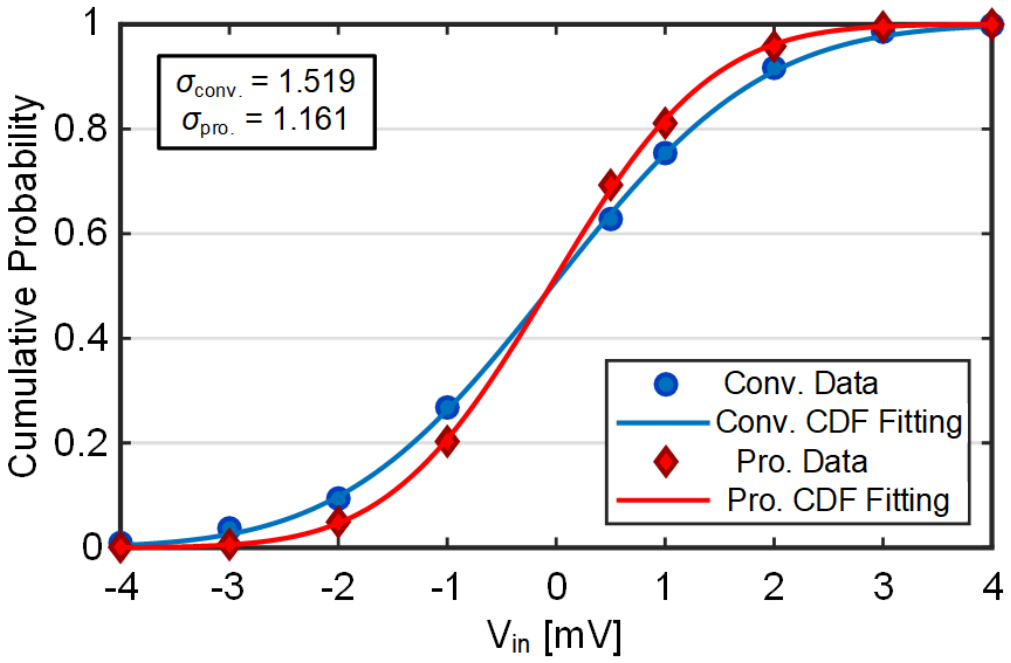


Figure 3.9. Simulated input-referred noise of conventional and proposed StrongARM latches.

where Δt_d is the delay between CK_d and CK. A sufficiently sized delay Δt_d prevents the regeneration from taking place before significant gain accrues, the amplification phase can thus be effectively extended. The higher voltage gain benefitting from extended amplification phase desensitizes the comparator to the effect of noise. According to simulation results, the modified StrongARM latch with a delay of 50 ps shows an extracted RMS input-referred noise of 1.1 mV, which is less than that of a conventional implementation with identical transistor sizes by a factor of 1.3, as shown in Fig. 3.9.

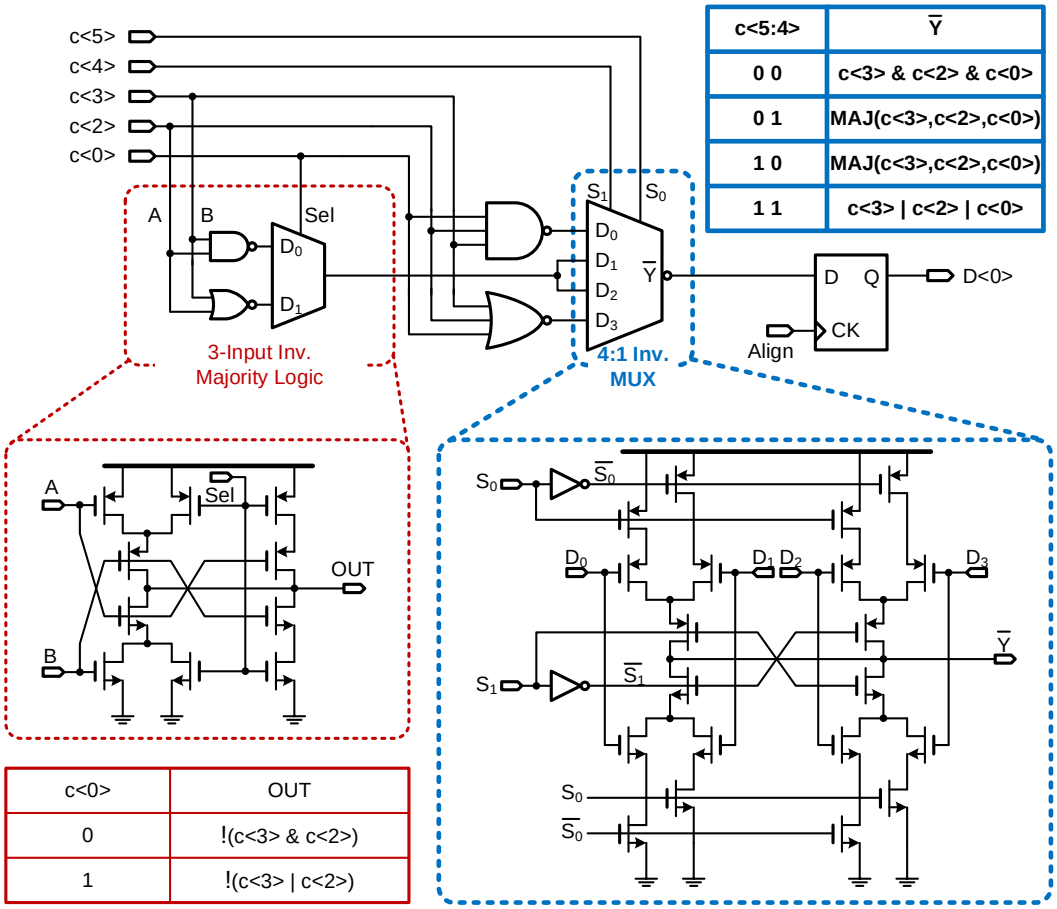


Figure 3.10. Schematic of the five-input majority voting logic.

3.5.2 Majority Voting Logic

Fig. 3.10 shows the schematic of the majority function adopted in this work. As COMP<5:2> and COMP<0> are used for the LSB decision, the comparator outputs are denoted as c<5:2> and c<0>, respectively. To simplify the implementation, the 5-input majority function unit is extended from a 3-input majority logic with the use of a 4-to-1 inverting MUX and a few standard logic gates. The modified truth table of the 4-to-1 inverting MUX is given in the upper right corner of Fig. 6. c<5> and c<4> are applied to the inverting MUX as two selection lines. In case of c<5:4>=00, c<3>, c<2> and

c<0> need to be all 1's for the final decision to be 1'. Hence, a 3-input NAND gate can be used to produce the output for case 00. Similarly, a NOR gate delivers the output if c<5:4>=11. For cases 01 and 10, at least two of c<3>, c<2> and c<0> need to be 1' to have a positive voting output. This can be checked with a 3-input inverting majority logic, which is implemented as an unconventional NAND/NOR gate to minimize the number of transistors. Owing to the simplified design, the 5-input majority function is realized with a hardware overhead of merely 46 transistors and a timing penalty of approximately 2 gate delays, which is of great importance in high-speed operations since more time can be budgeted for comparator regeneration.

3.6 Measurement Results

The prototype ADC has been fabricated in a 28 nm FDSOI process with an active area of 0.0073 mm^2, as shown in Fig. 3.11. The power breakdown and DNL/INL performances of the ADC are provided in Fig. 3.12. The ADC core dissipates a total of 2.1 mW from a 1.1 V supply, where only 0.9 mW is consumed by the comparators (including calibrations and reference buffers) thanks to the fast noise reduction technique. The ADC outputs are internally decimated by a factor of 91 to lower the data rate and facilitate data collection. The maximum DNL and INL are -0.62/+0.65 LSB and -0.63/+0.72 LSB, respectively.Fig. 3.13 shows the measured FFT plots with a low-frequency and a Nyquist input, respectively. Fig. 3.14 shows a plot of measured SNDR and SFDR versus the input frequency with a sampling rate of 1 GS/s. The SNDR and SFDR at the low input frequency are 47.89 dB and 65.98 dB, respectively. The

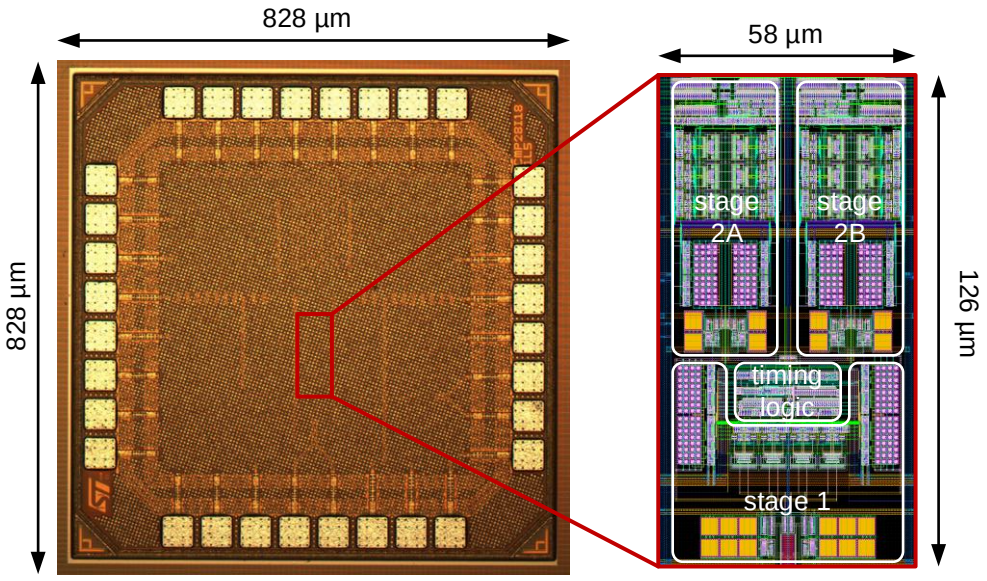
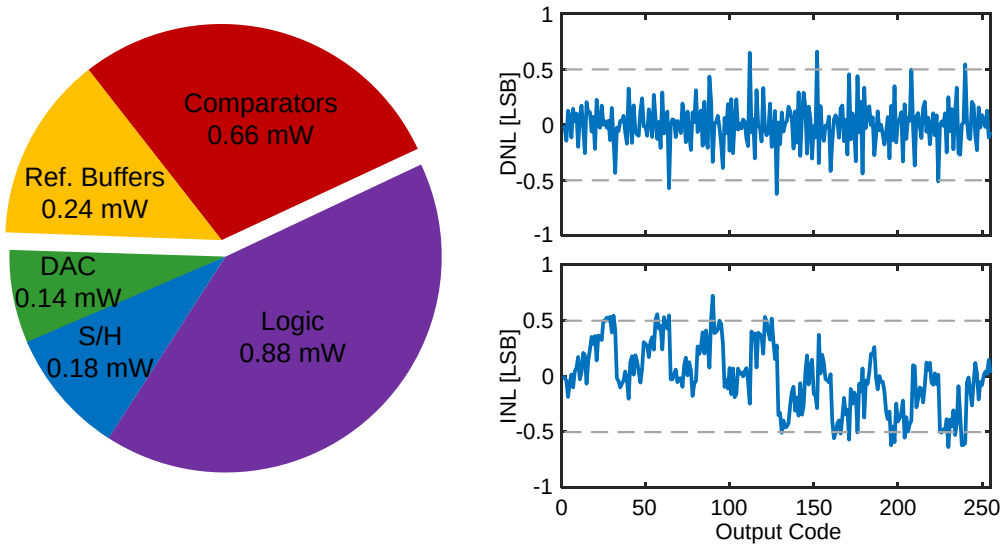


Figure 3.11. Chip micrograph and layout of the proposed ADC.



(a) (b)

Figure 3.12. (a) Power breakdown at 1.0 GS/s. (b) Differential and integral non-linearities.

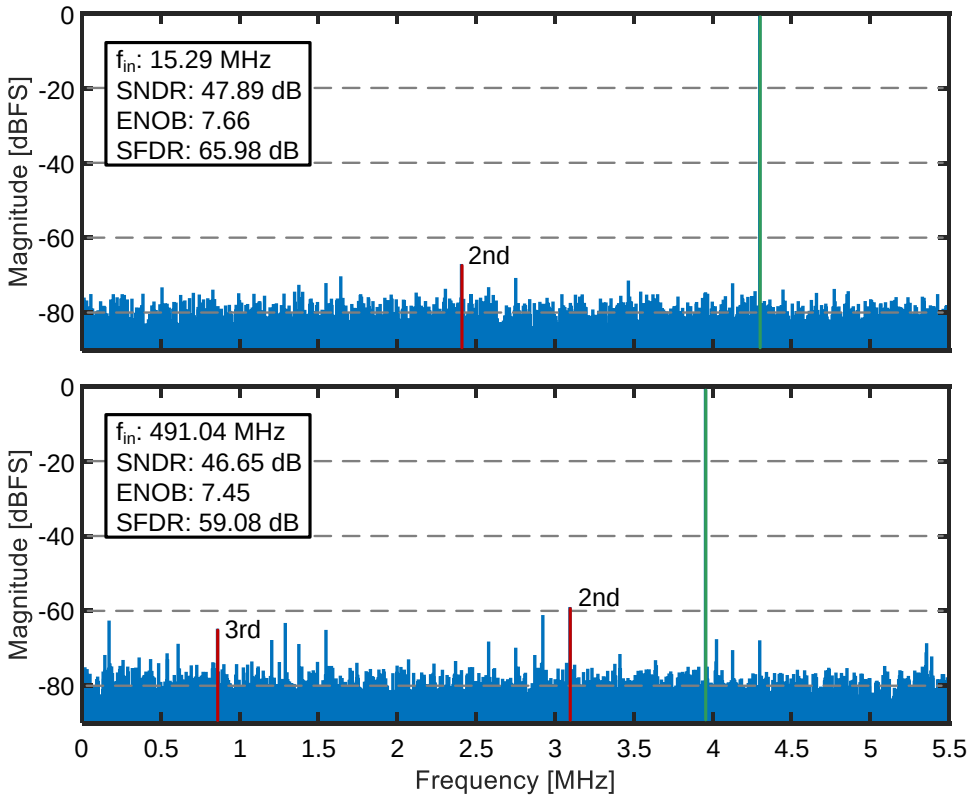


Figure 3.13. Measured power spectrum (91× decimated).

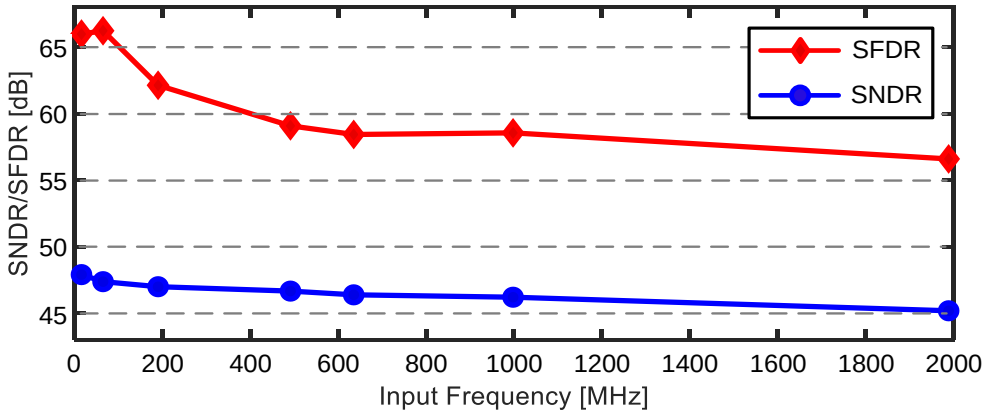


Figure 3.14. Measure SNDR and SFDR vs. input frequency.

Table 3.1. Performance Summary and Comparison

Specifications	[38]	[39]	[40]	[41]	This work
Architecture	TB ADC	Pipe. SAR	TI-SAR	Pipe. SAR	Pipe. SAR
Technology (nm)	65	40	28	65	28 FDSOI
Sample Rate (MS/s)	950	1100	2400	1200	1000
Resolution (bits)	8	8	7	8	8
Supply Voltage (V)	1.0	1.2	0.9	1.25	1.1
$SNDR_{@Nyquist}$ (dB)	45.0	45.0	40.05	43.7	46.65
$SFDR_{@Nyquist}$ (dB)	62.1	66.0	54.34	58.1	59.08
Power (mW)	2.3	4.0	5.0	5.0	2.1
FOM_W (fJ/conv.-s.)	18.5	25.0	25.3	35	12.01
Area (mm^2)	0.007	0.00165	0.0043	0.013	0.0073

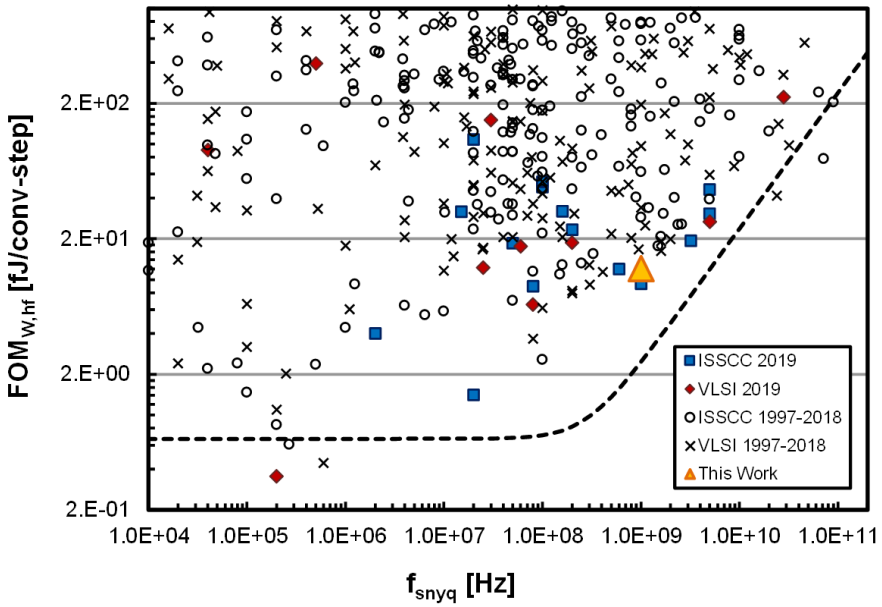


Figure 3.15. Comparison of Walden FOM with ADCs presented at ISSCC and VLSI between 1997 and 2019.

corresponding ENOB is 7.66 bits. The SNDR and SFDR degrades to 46.65 dB and 59.08dB, respectively, as the input frequency increases to the Nyquist frequency. The SNDR remains above 45 dB up to 2 GHz. Table I summarizes the performance of the ADC and provides a comparison with state-of-the-art GS/s 7/8-bit ADCs. Fig. 3.15 plots the Walden FOM of the prototype ADC against all ADCs presented at ISSCC and VLSI between 1997 and 2019.

CHAPTER IV

DOUBLE-RATE COMPARATOR-BASED SAR ADC

4.1 Motivation

High-speed successive-approximate-register analog-to-digital converters (SAR ADCs) with medium-to-high resolutions find wide application in test equipment, wireline transceivers and wireless communication systems owing to their advantageous power efficiency and scaling-friendly configurations. Recently, as the actively conducted research on breaking the speed limit keeps going and supplemented by the advanced technology nodes, SAR ADCs without extensive interleaving gradually gain popularity in the high-speed domain, which used to be dominated by their flash and pipeline counterparts.

To date, single-channel SAR ADCs with a variety of speed-enhancing techniques have been reported to achieve sampling rates of several hundreds of MS/s to over 1 GS/s, depending on the specific resolution [24, 37, 40, 42, 43, 44, 45, 46, 47]. 2b/cycle SAR ADCs [40, 42, 43, 44] shrink the conversion time by reducing the effective number of bit cycles at the cost of decreased power efficiency and increased design complexity. In addition, the 2b/cycle architecture decreases the benefit of asynchronous timing. This tradeoff usually limits the FOM to around 20 fJ/conv.-step [44]. The loop-unrolled architecture [24, 37, 45, 46], on the other hand, approaches the problem from a different perspective and aims at accelerating the conversion on a per-cycle basis. For a given decision time, the total delay of a typical SAR cycle is dictated

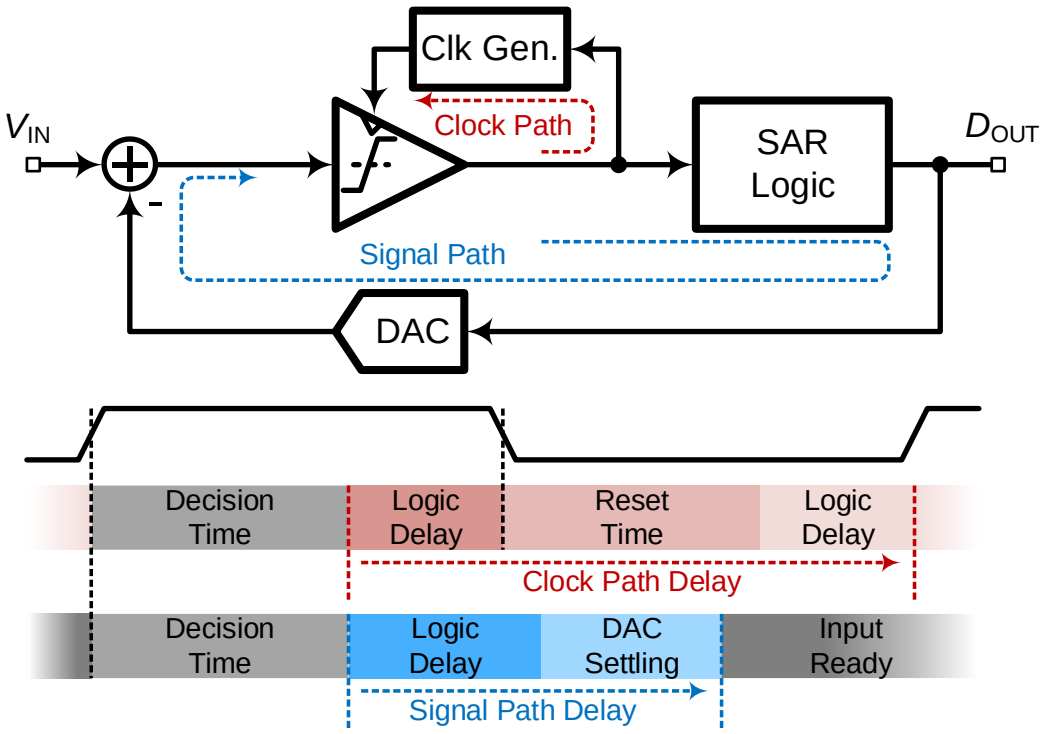


Figure 4.1. Clock and signal paths of the SAR conversion.

by the delays from either the signal path or the clock path, whichever is longer, as shown in Fig. 4.1. The extensive use of small size DACs and redundancy in today's ADC designs considerably relax the DAC settling requirement, making the clock path delay a bottleneck for high-speed operations. By employing a dedicated comparator for each bit cycle, the loop-unrolled architecture eliminates both the comparator reset time from the clock path and the memory delay from the signal path, which greatly reduces the cycle duration. The prices, however, are the non-uniform offsets of the comparator array as well as the area penalty. Efficient as it is in power, foreground trimming of the comparator offset may not be a practical solution since it lacks the mechanism to track the offset variation caused by PVT variation. On the other hand, background offset calibration can result into either a high power penalty or a long convergence time. This

drawback is particularly obvious as the resolution increases, since each comparator requires individual offset extraction. In [47], a single-channel SAR ADC with alternate comparators was proposed as a tradeoff between the speed improvement and the power penalty induced by background calibration. Though a portion of the speed gain is rebated as the memory delay still exists, the simultaneous calibration of quite a few comparators is avoided.

A long-neglected problem associated with multi-comparator-based cycle accelerations is the more complicated and thus power consuming comparator clock generation. Since the comparators operate at a frequency much higher than the ADC sampling rate, the associated clock generation logic needs to be as fast to keep pace. As a result, the comparators and the digital circuits are the two predominant contributors to the total power consumption in modern SAR ADCs [16, 24, 29, 47].

In this chapter, we present a single-channel SAR ADC with a double-rate comparator for conversion rate enhancement. Differing from the conventional comparator, which is triggered upon arrival of the clock rising edge and reset by the falling edge, the proposed double-rate comparator can be triggered by both the rising edge and the falling edge without reset. The benefits of the double-rate comparator are three-fold. First, it effectively removes the comparator reset time from the critical path, including the reset delay between the last conversion cycle and the calibration phase. Second, a portion of the power dissipated during reset can be saved, resulting into a modest power efficiency boost for the comparator. Third, the double-rate operation of the comparator effectively reduces the frequency of the asynchronous driving clock by a half. Hence, the clock generation scheme can be simplified to a large extent as

compared to the prior multi-comparator architectures. This results into a considerable power reduction of the digital parts.

4.2 Review of Conventional Comparators

The most commonly adopted comparator architectures are the Strong-ARM latch, the double-tail comparator and their variants. The Strong-ARM latch is a popular choice for ADC designers due mainly to its fully dynamic operation [48]. However, the single-stage design turns out to be problematic when a wide input common-mode range is required. The common-mode variation directly affects the tail current of the Strong-ARM latch and consequently the regeneration speed as well as the offset and noise. In addition, the Strong-ARM latch suffers from limited headroom when it comes to low-supply operations. The double-tail comparator [49] was proposed to improve the headroom and decision speed by carrying out the regeneration in a second stage, where a large transient current can be provided, at the cost of inevitably higher power. Another problem that comes with this architecture is it introduces an extra clock path to control the second tail current. The skew and jitter of the clock can thus alter the performance of the comparator.

Shown in Fig. 4.2 is a variant of the double-tail comparator [29], where the second stage is replaced by an SR latch. The regeneration current is controlled by the output of the first stage through the PMOS transistors, thereby eliminating the need for the extra clock path and simplifying the clock feeding. This modification also rebalances

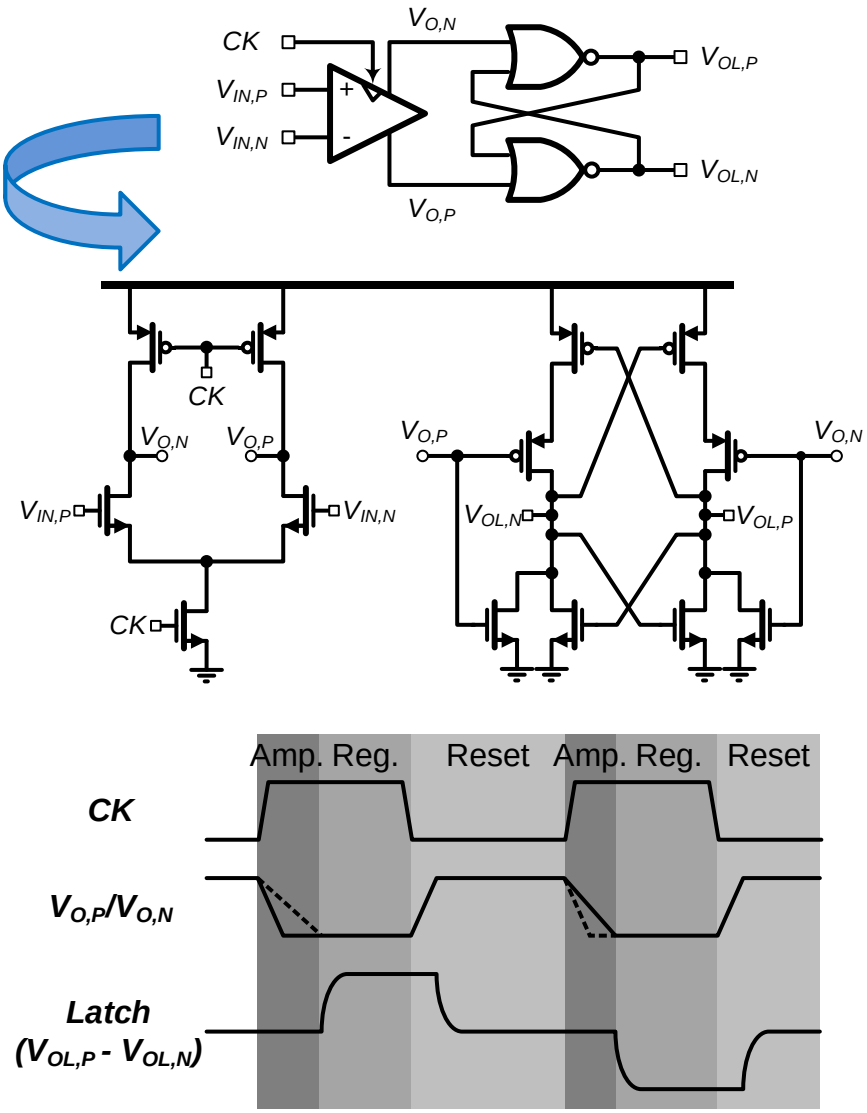


Figure 4.2. Conventional two-stage dynamic comparator.

the tradeoff between the power and speed and is suitable for applications with a tight power budget. As with its predecessors, the operation of this dynamic comparator can be broken into three phases. During reset phase, the clock remains low and the differential outputs of the dynamic amplifier are shorted to the power supply through a pair of switches. The rising edge of the clock marks the beginning of the amplification phase, where the outputs are discharged to ground with a rate dictated by the input

voltage. In doing so, the dynamic amplifier converts the input voltage difference into a difference in timing. The timing difference is then sensed by the SR latch to generate a rail-to-rail output.

At first sight, the fully dynamic structure of the comparator renders high power efficiency since no static current is drawn by any of the devices. Nonetheless, the power dissipated during reset can, to a certain extent, be viewed as being wasted, since no action is completed in this process. In addition, the reset phase after each amplification serves as a cooling time that inevitably prevents the comparator from making another decision immediately.

4.3 Proposed Double-Rate Comparator

To further increase the power efficiency and break the speed limit by removing the reset phase, we propose a double-rate comparator. The schematic is depicted in Fig. 4.3. The comparator is composed of a pre-amplifier, a pair of clocked sourcing/draining current sources (C-S/D-CS), two pseudo-differential inverter buffers and two SR latches (Latch-A and Latch-B). The offset calibration circuit is also included in the comparator module as an auxiliary building block to ensure an offset-compensated operation. All the blocks above are essential to the desired functionality and performance of the comparator, as will be detailed in the following sub-sections.

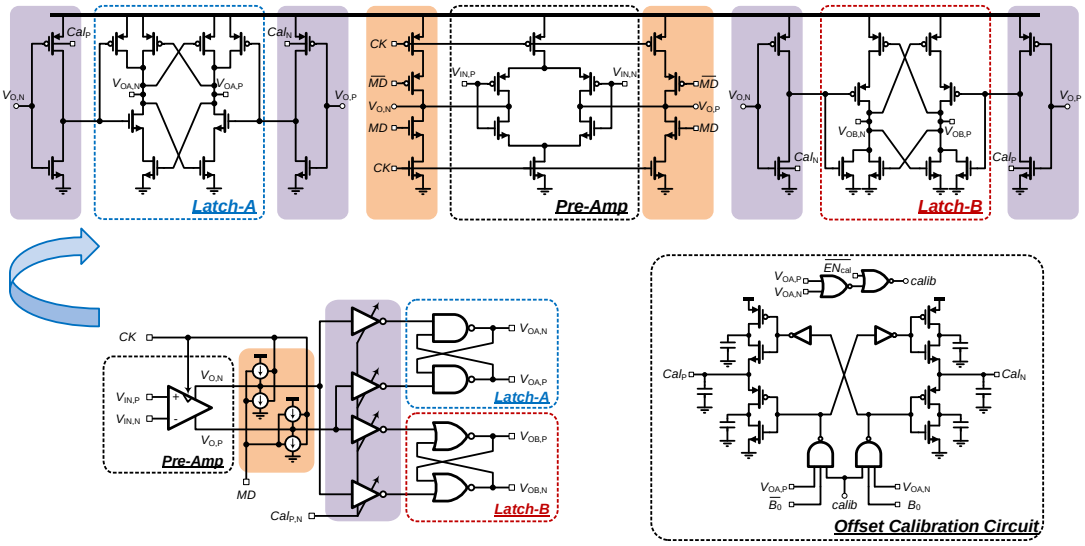


Figure 4.3. Schematic of double-rate comparator.

4.3.1 Pre-Amplifier and Regenerative Latches

The pre-amplifier and the regenerative latches are the main functional blocks of the proposed comparator. The pre-amplifier employs a pair of CMOS transistors for input sensing and is horizontally symmetrical in terms of topology. However, it differs from a conventional dynamic amplifier using complementary input for transconductance enhancement in the sense that the PMOS and NMOS pairs do not theoretically conduct current simultaneously. This is realized by driving the upper and the lower tail currents with the same clock signal CK, such that only one of the tail currents are enabled at one time. Consequently, the operation of the pre-amplifier can be decomposed into two phases according to the specific voltage level of the driving clock, as illustrated in Fig. 4.4. When the clock goes high, only the lower tail current is enabled, the pre-amplifier behaves like a conventional dynamic amplifier with NMOS inputs (Phase N). The outputs of the pre-amplifier ($V_{O,P}$ and $V_{O,N}$) gradually ramp down

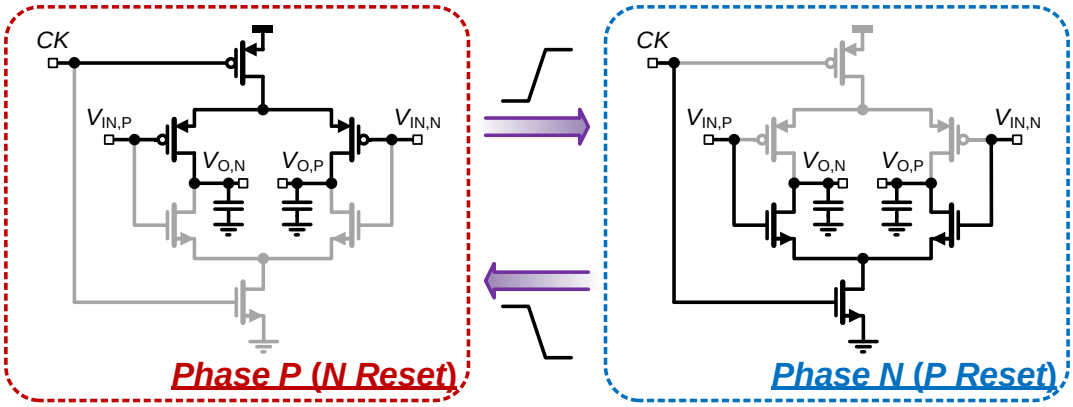


Figure 4.4. Phase P and Phase N of the pre-amplifier.

to ground by the input pair, turning the input difference into two falling edges with different delays. As the clock goes low, $V_{O,P}$ and $V_{O,N}$ are charged at different rates to the power supply by the PMOS pair (Phase P), resulting into two rising edges, which is complementary to the behavior in Phase N. Interestingly, Phase P can be regarded as a reset phase to Phase N and vice versa, as the differential components of the output will finally disappear at the end of each phase. This keeps the alternate amplification phases going indefinitely without reset. In each clock period, the pre-amplifier can provide two amplification phases with the same amount of charge as in a conventional implementation, which in theory translates into doubled power efficiency and speed. The advantage expands if the pre-amp stage is largely sized for noise optimization.

As the 3rd stage, Latch-A and Latch-B are complementary with respect to structure (NAND SR latch and NOR SR latch, respectively). After being amplified and inverted by the 2nd-stage inverter buffers, the Phase N and Phase P outputs of the pre-amplifier are respectively sensed by Latch-A and Latch-B, respectively. And thereby valid digital results are generated as the final outputs of the comparator.

4.3.2 Pseudo-Differential Inverter Buffers

In SAR ADCs with two or more comparators, one of the reasons for complicated clock generation is the kickback noise from the comparators, as shown in Fig. 4.5. The kickbacks can originate from two sources, with the first one being the clocked tail current, which draws current from the gate-source capacitance of the input pair and causes a common-mode variation and a deterministic differential error in the presence

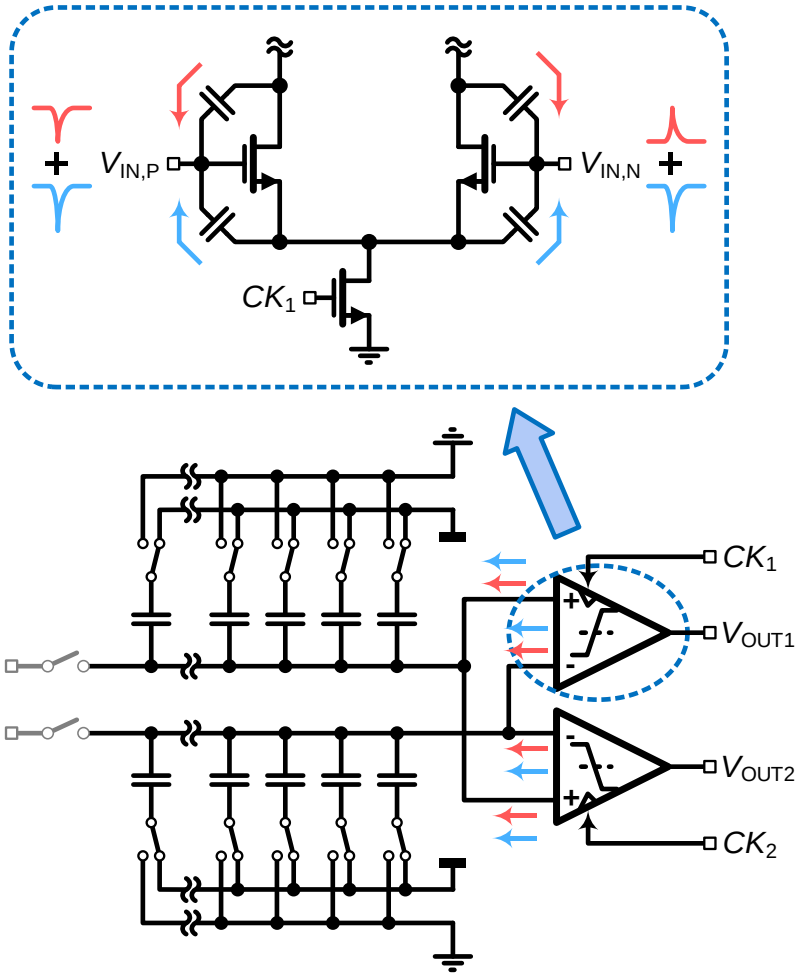


Figure 4.5. Common-mode and differential kickbacks in multi-comparator SAR ADCs.

of mismatch. The second source is the regenerating or resetting output coupled to the input through the gate-drain capacitance. Unless fully reset before the upcoming comparison, the kickback from the second source can lead into an output-dependent differential voltage shift on the input and degrades the ADC accuracy. As such, non-overlapping clocks are usually required to drive the comparators. Upon close scrutiny, the kickback from the first source, which is signal-independent, is quite benign in the double-rate comparator as it takes place every time the comparator is triggered. Hence the resulted offset variation can be easily captured by a calibration mechanism to avoid

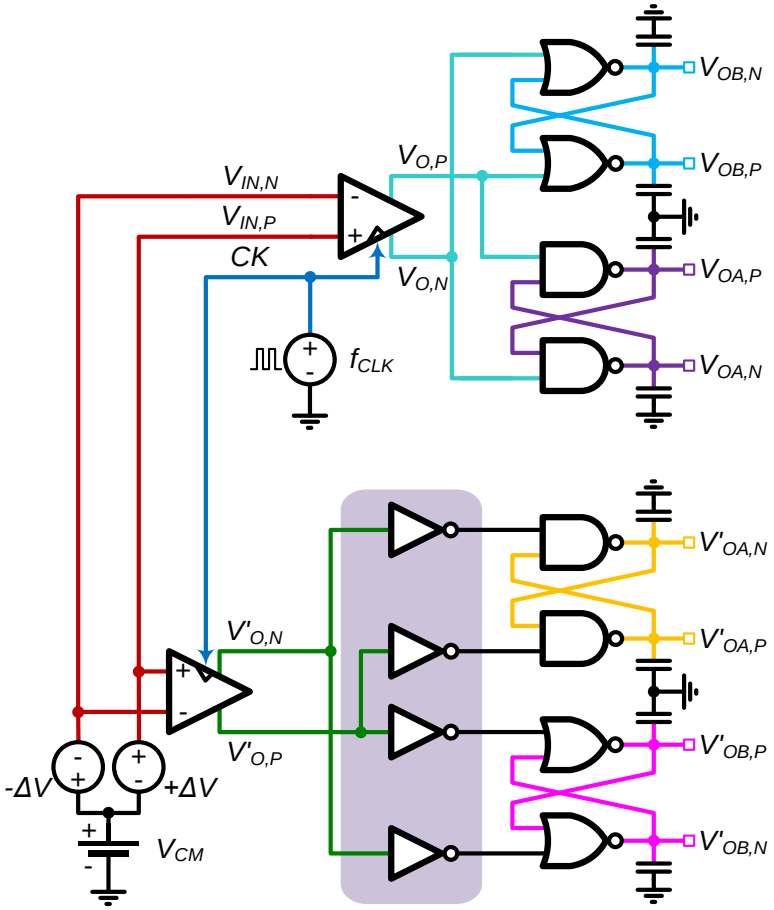


Figure 4.6. Circuit for kickback suppression analysis (V_{DD} = 1.1 V, f_{CLK} = 5 GHz, V_{CM} = 550 mV, $\Delta V = \pm 0.5$ mV).

accuracy degradation. However, since the output nodes of the pre-amp are shared between the two latches, they are quite sensitive to the output-dependent kickback. As stated in the previous sub-section, since Phase P and Phase N can be regarded as the reset phase to each other, when one of the two latches is regenerating, the other is resetting. The kickbacks from the resetting latch will create a transient differential voltage disturbance that keeps the regenerating latch from making a correct decision.

Fortunately, the kickback issue can be effectively resolved by inserting pseudo-differential inverter buffers between the pre-amplifier and the regenerative latches. Since the outputs of the inverter buffers are always slewing towards the same rail, the kickbacks due to large differential output swing is greatly suppressed. The effects of the

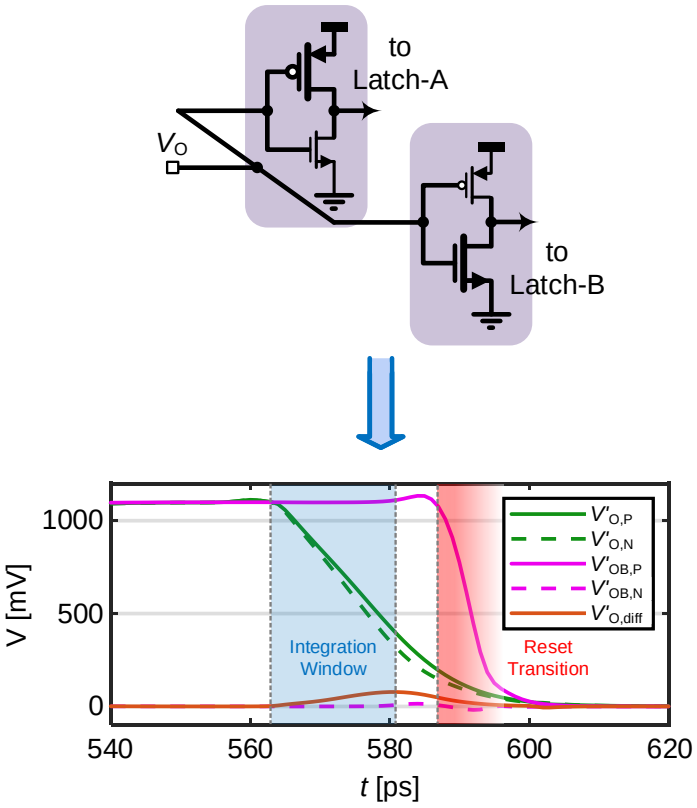


Figure 4.7. Skewed inverter buffers for reset transition control.

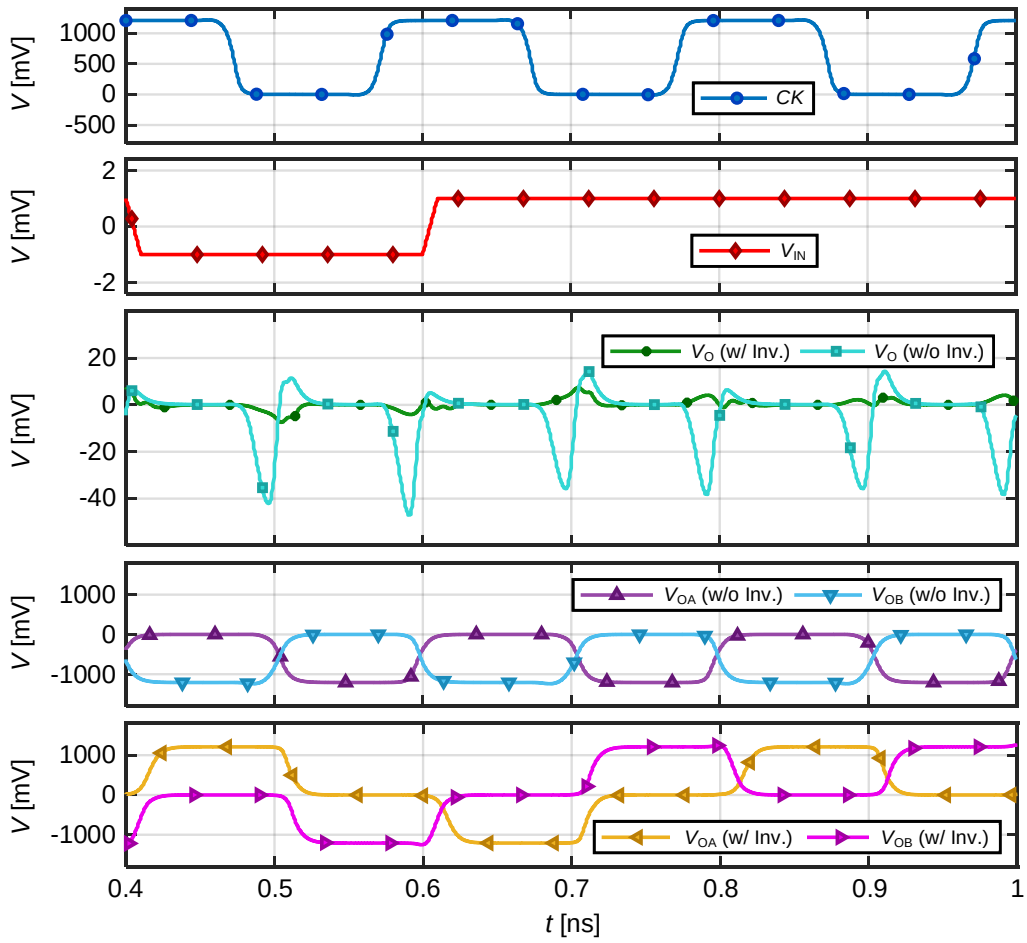


Figure 4.8. Transient waveforms with and without pseudo-differential inverter buffers.

pseudo-differential inverter buffers on kickback suppression is simulated with the circuit shown in Fig. 4.6, where a differential input of ±1 mV is applied simultaneously to two comparators with and without inverter buffers, respectively. Fig. 4.7 details the inverter buffer implementations. The inverter buffers preceding Latch-A and Latch-B are oppositely skewed to advance the initiation of regeneration while postponing that of reset, so that the kickback only takes place after the integration window, when enough gain has accrued. This further mitigates the effect of kickback. Fig. 4.8 shows the

transient waveforms with and without pseudo-differential inverter buffers (first row: clock, second row: differential input voltage, third row: pre-amp output voltage, fourth row: latches output without inverter buffers, fifth row: latches output with inverter buffers), the comparator without inverter buffers suffers from severe kickback noise on the pre-amp output nodes, and both latches keep toggling between reset and negative output, regardless of the input voltage polarity. The comparator with inverter buffers, on the other hand, shows little sign of kickbacks on the pre-amp output nodes. And the decisions accurately track the input polarity, demonstrating correct functionality of a comparator.

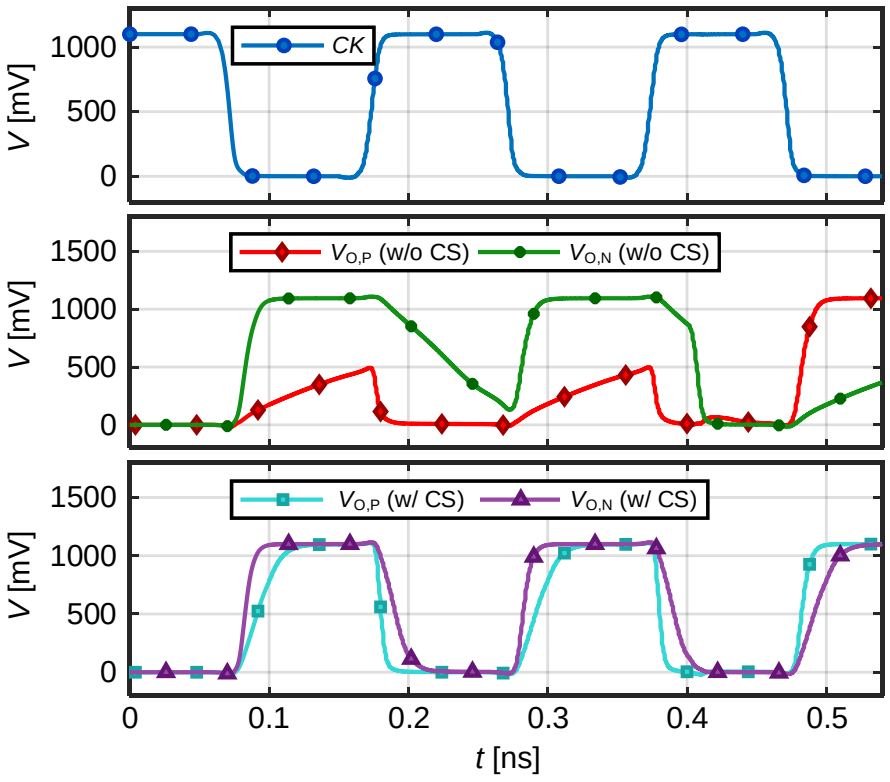


Figure 4.9. Transient waveforms on the pre-amp output nodes with the current sources enabled and disabled, respectively.

4.3.3 Clocked Sourcing/Draining Current Sources

Another issue associated with the reset-free complementary amplifications is the large input-induced incomplete charging or discharging of the pre-amp output nodes $V_{O,P}$ and $V_{O,N}$. The concept of alternate amplifications is based upon the assumptions that both $V_{O,P}$ and $V_{O,N}$ can be charged to V_{DD} and discharged to GND in a timely manner. However, this assumption does not hold in case one of the input transistors is turned off by an overly large input, which cuts off the current path and considerably slows down the charging or discharging process. This in turn leads to a memory-dependent offset. The integration of C-S/C-CSs solves the aforementioned issue by

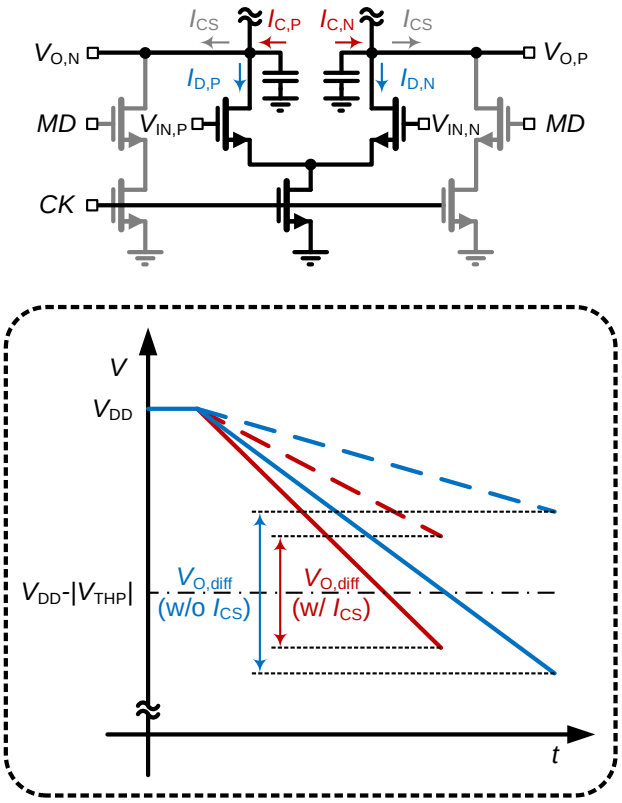


Figure 4.10. Amplification acceleration and gain reduction caused by the current sources.

providing extra current paths and accelerating the charging or discharging of $V_{O,P}$ and $V_{O,N}$. Fig. 4.9 shows the transient waveforms of $V_{O,P}$ and $V_{O,N}$ for a 400-mV input, with the current sources disabled and enabled, respectively.

The clocked sourcing/draining current sources do have some effects on the speed and noise of the comparator as explained in Fig. 4.10. Taking the Phase N operation as an example. First, the duration of the amplification phase is decreased by enabling the current sources, due to the larger common-mode currents. Specifically, the amplification time with the current sources disabled and enabled are

$$t_{amp} = \frac{C_O |V_{THP}|}{I_{CM}} \tag{4.1}$$

and

$$t_{amp,CS} = \frac{C_O |V_{THP}|}{I_{CM} + I_{CS}}, \tag{4.2}$$

respectively. C_O is the loading capacitance on the output nodes, $|V_{THP}|$ the threshold voltage of the next stage, I_{CM} the common-mode current drawn from each capacitance and I_{CS} the current drawn by the clocked current sources. Due to the reduction on the amplification time, the gain of the pre-amp is also decreased from

$$A_v = \frac{g_m t_{amp}}{C_O} = \frac{2|V_{THP}|}{(V_{GS} - V_{THN})_{1,2}} \tag{4.3}$$

to

$$A_{v,CS} = \frac{g_m t_{amp,CS}}{C_O} = \frac{I_{CM}}{I_{CM} + I_{CS}} \cdot \frac{2|V_{THP}|}{(V_{GS} - V_{THN})_{1,2}}, \tag{4.4}$$

where g_m is the transconductance and $\left(V_{GS}-V_{THN}\right)_{1,2}$ is the overdrive voltage of the input pair.

Now that the amplification is accelerated, the initial voltage during the regeneration process is decreased due to the reduced gain, which leads to a longer regeneration time. However, the resolving time of the comparator can still be reduced provided that regeneration time constant is much smaller than the amplification time. This is fortunately the case in comparator designs optimized for a low noise. The decision delay improvement can be expressed as

$$\Delta t_{dec.}=\frac{\left|V_{THP}\right|C_O I_{CS}}{I_{CM}\left(I_{CM}+I_{CS}\right)}-\tau\ln\left(1+\frac{I_{CS}}{I_{CM}}\right), \tag{4.5}$$

where τ is the regeneration time constant.

The drawback of the amplification acceleration is the increase in the input-referred noise of the pre-amp and also that of the comparator, since the noise is attenuated by the gain of the pre-amp when referred to the input. The pre-amp input-referred noise with the current sources deactivated and activated are [50]

$$\overline{V_{n,in}^2}=\frac{kT\left(V_{GS}-V_{THN}\right)_{1,2}^2}{\left|V_{THP}\right|C_O}\cdot\left[\frac{2\gamma}{\left(V_{GS}-V_{THN}\right)_{1,2}}+\frac{1}{2\left|V_{THP}\right|}\right] \tag{4.6}$$

and

$$\overline{V_{n,in,CS}^2}=\frac{kT\left(V_{GS}-V_{THN}\right)_{1,2}^2\left(I_{CM}+I_{CS}\right)}{\left|V_{THP}\right|I_{CM}C_O}\cdot \left[\frac{2\gamma}{\left(V_{GS}-V_{THN}\right)_{1,2}}+\frac{g_{ds6,7}\left(I_{CM}+I_{CS}\right)}{I_{CM}}+\frac{I_{CM}+I_{CS}}{2\left|V_{THP}\right|I_{CM}}\right], \tag{4.7}$$

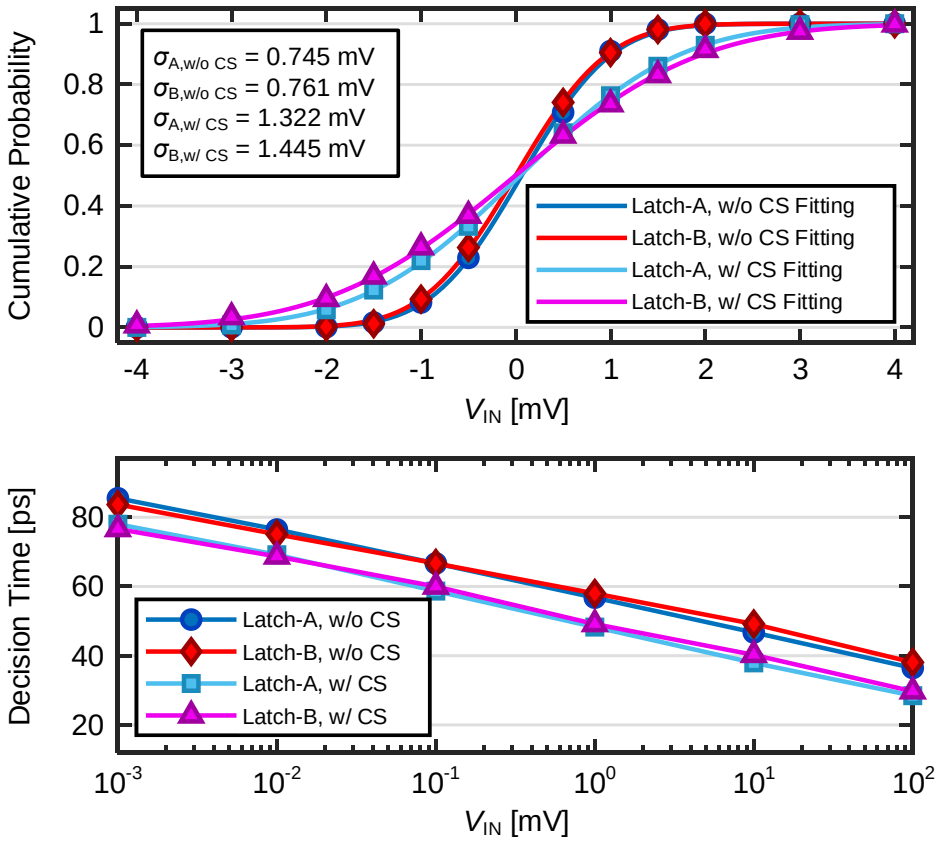


Figure 4.11. Simulated noise and decision speed of the double-rate comparator with the clocked current sources disabled and enabled, respectively.

respectively. As can be seen from Eqn. (4.6) and (4.7) that with the clocked current sources activated, the input-referred noise of the pre-amp can be much higher due to the non-zero I_{CS} and $g_{ds6,7}$. The noise contribution of the backend stages can be analyzed with hand calculation following the procedure described throughly in [50]. Here, since the comparator noise is dominated by that of the pre-amp, only the input-referred noise of the pre-amp is calculated for simplicity and the overall comparator noise is found out through simulations. Fig. 4.11 shows the simulated input-referred noise and decision delay of the double-rate comparator with the current sources enabled and disabled.

Fortunately, the increased noise of the double-rate comparator has little effect on the overall accuracy of the ADC. As an overly large input can only occur during the MSB cycles in a SAR ADC, the clocked current sources are enabled for the coarse conversion cycles only and remain disabled for the rest of the conversion phase to maintain a low-noise operation in noise-sensitive cycles. This naturally divides the operation of the comparator into two modes, namely the high-speed mode, where the clocked current sources are enabled, and low-noise mode, where the current sources are disabled.

4.3.4 Offset Calibration Circuit

Due to the two operation modes as well as the complementary amplifications of the comparator, there are a total of 4 different offset voltages, namely the offset of high-speed Phase N-Latch-A operation ($V_{off,AH}$), the offset of high-speed Phase P-Latch-B operation ($V_{off,BH}$), the offset of low-noise Phase N-Latch-A operation ($V_{off,AL}$) and that of low-noise Phase P-Latch-B operation ($V_{off,BL}$). As with multi-comparator architectures, the offset mismatch needs to be compensated to avoid linearity degradation of the ADC.

Since the mismatch between $V_{off,AH}$ and $V_{off,AL}$ and that between $V_{off,BH}$ and $V_{off,BL}$ are introduced by the clocked current sources only, they are rather small in value and can be readily absorbed by the redundancy in the MSB cycles, only the mismatch between $V_{off,AL}$ and $V_{off,BL}$ needs to be sensed and compensated. Thus in the following discussions, both $V_{off,AH}$ and $V_{off,BH}$ are assumed to be 0 for simplicity. To track the PVT variation and shorten the calibration phase, the mismatch sensing is performed in the

background by repeating one of the fine conversion cycles but with a different comparator configuration to avoid DAC reset and input shorting. In other words, one of the LSB comparisons is executed twice, triggered by different clock edges. If different decisions from the two comparisons are observed, then $V_{off,AL}$ and $V_{off,BL}$ will be adjusted towards the opposite direction so that $V_{off,AL}$ - $V_{off,BL}$ can be reduced. This is carried out with a charge sharing-based circuit as depicted in Fig. 4.3. The calibration voltage is applied to alter the body biasing of the inverter buffers, which simplifies the implementation of small calibration steps for a low algorithm noise. Since the offsets

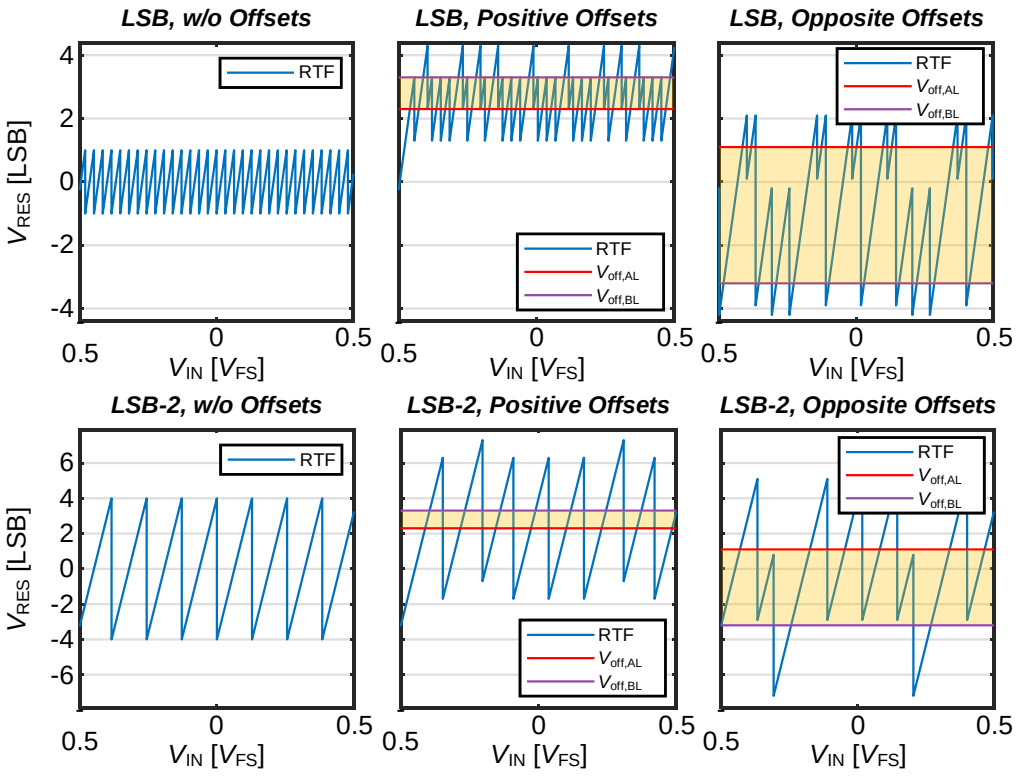


Figure 4.12. Residue transfer function of a 6-bit conversion at LSB cycle and LSB-2 cycle with no offsets, two positive offsets (2.3 LSB and 3.3 LSB) and two offsets with opposite polarity (1.1 LSB and -3.2 LSB).

are updated only when the residue is located between $V_{off,AL}$ and $V_{off,BL}$, it is then desired to maximize the probability that the residue falls within this active region.

The residue transfer functions of a SAR ADC differ from cycle to cycle and are affected by the offsets. Fig. 4.12 shows the residue transfer functions of the 6-bit fine conversions at LSB and LSB-2 cycles with no offsets, two positive offsets and two opposite offsets. It can be observed that most of the residues in the k^{th} fine cycle are distributed over the range

$$-V_{R,k}+V_{\min}<V_{RES}[k]<V_{R,k}+V_{\max},\ \ k=1,2,...,6, \tag{4.8}$$

where

$$V_{\min}=\min[V_{off,AL},V_{off,BL}] \tag{4.9}$$

and

$$V_{\max}=\max[V_{off,AL},V_{off,BL}]. \tag{4.10}$$

And $\pm V_{R,k}$ are the nominal upper and lower limits of the residue without being altered by offsets. To maximize the convergence rate as well as the sensitivity of the calibration mechanism, $V_{R,k}$ needs to be minimized. Consequently, the LSB cycle is repeated in this design to conduct mismatch sensing. Fig. 4.13 shows the convergence process of the calibration algorithm with the sensing position as a parameter. The input is the residue after the coarse conversion and is modelled as a uniformly distributed random process. The convergence rate increases considerably as the sensing position is swept from LSB-4 to LSB. Another favorable attribute brought by LSB sensing is that the algorithm can be more robust against slowly varying signals or signals with frequencies very close to integer times of the sampling rate.

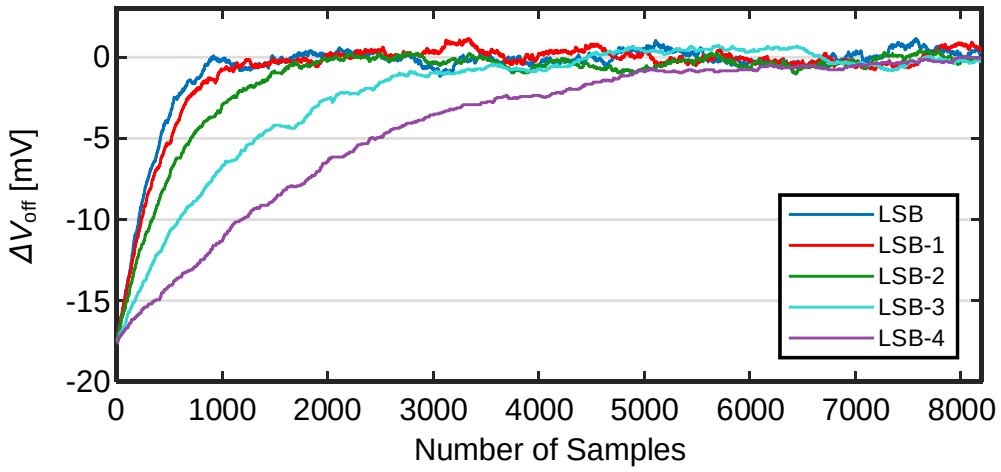


Figure 4.13. Convergence process of the offset calibration with different sensing positions.

Eqn. (4) holds as long as both $V_{off,AL}$ and $V_{off,BL}$ fall within the range of convergence given by

$$ROC = \left(-\sum_{i=1}^{k} V_{R,i}, \sum_{i=1}^{k} V_{R,i} \right), \; k = 1, 2, ..., 6 . \tag{4.11}$$

For LSB sensing, this range can be as large as ±64 LSB, a rather relaxed requirement. In terms of implementation and performance considerations, however, the acceptable offset distribution is usually confined by the calibration range and the SNR degradation, as the final offset may converge to a non-zero value and pose a limit on the input swing. In this design, the final offset value is strictly confined within ±16 LSB to have a well-controlled SNR degradation of less than 0.28 dB.

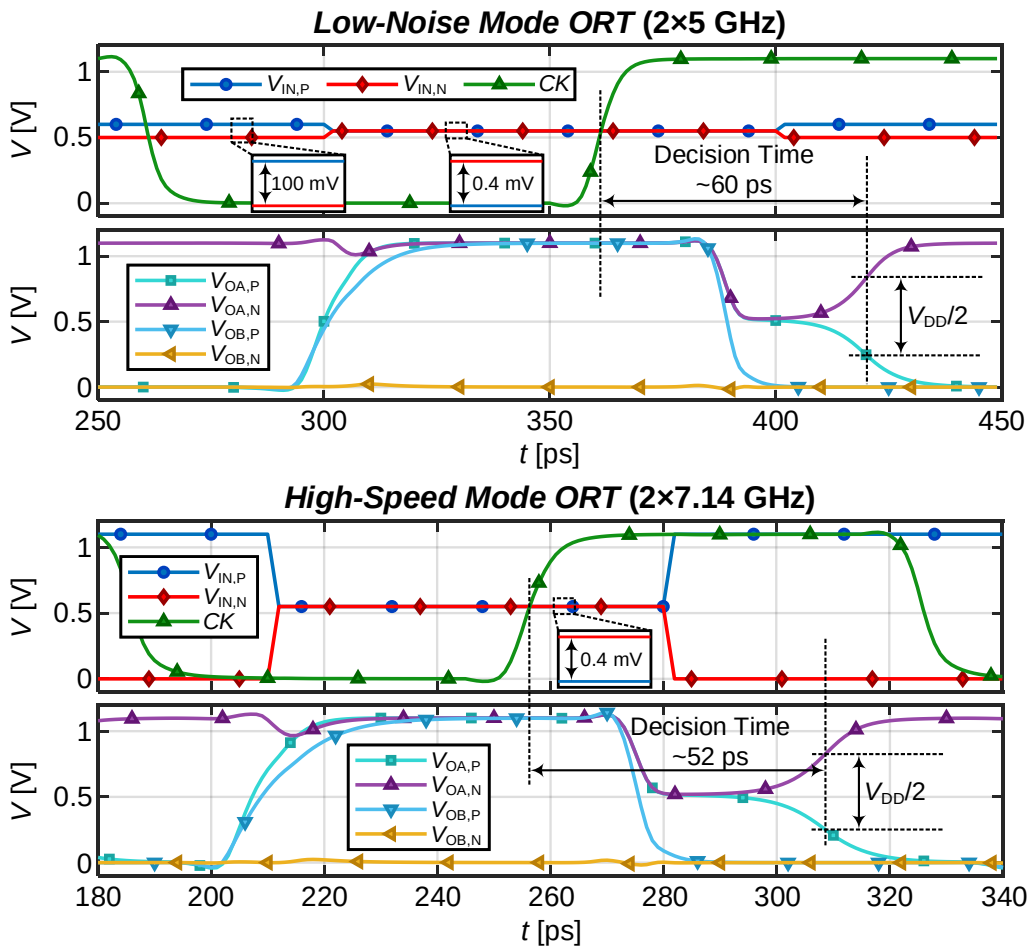


Figure 4.14. Simulated ORT performance of the double-rate comparator in low-noise and high-speed modes.

4.3.5 Comparator Performance Summary

Fig. 4.14 shows the simulated performance of the double-rate comparator under the overdrive recovery test (ORT) [51], which is known as the most stressful performance evaluation. When configured in the low-noise mode, the comparator is able to correctly resolve the input toggling between 100 mV (twice the full-scale residue in the first fine conversion cycle) and -0.4 mV (1/4 LSB) in two consecutive 10-GHz cycle.

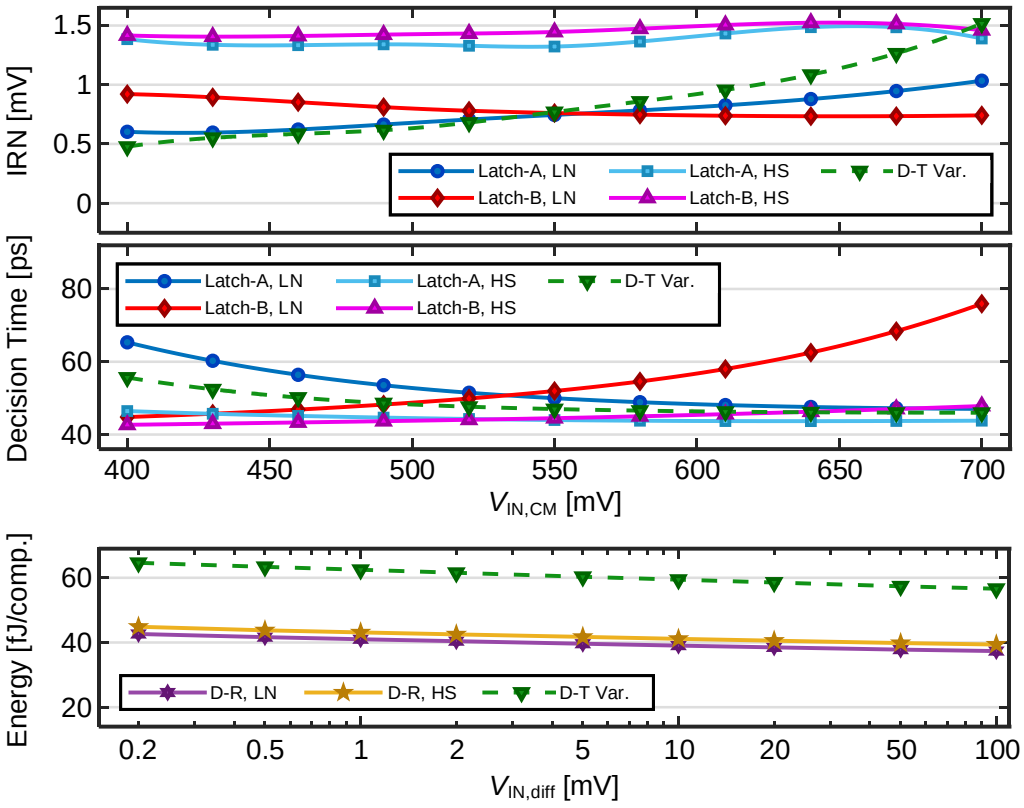


Figure 4.15. Input-referred noise and decision time vs. input common-mode as well as per-comparison energy vs. differential input.

Moreover, the comparator in high-speed mode passes the ORT at 14.28 GHz, with the input toggling between 1.1 V and -0.4 mV.

Fig. 4.15 shows the simulated input-referred noise and decision time over different input common-mode as well as the per-comparison energy as a function of the differential input. As a comparison, the performances of the dynamic comparator in [29] sized for similar input-referred noise to that in low-noise mode are also plotted. The double-rate comparator shows similar per-comparison energy in both modes and is more power-efficient than the variant of double-tail comparator thanks to the shared pre-amp.

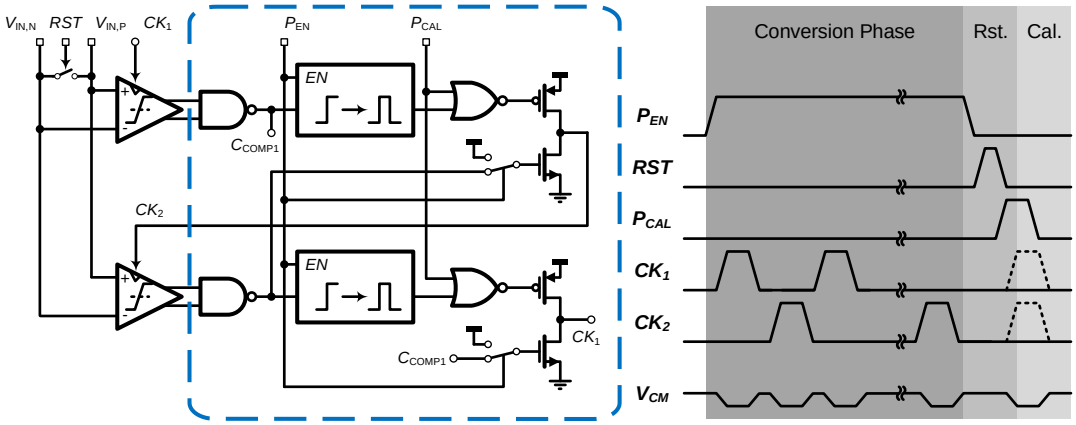


Figure 4.16. Typical clock generation circuit in an alternate-comparator-based SAR ADC.

4.4 Proposed Half-Rate Clock Generation

As mentioned in Section 4.1, the logic circuit in a multi-comparator-based SAR ADC is a major contributor to the total power consumption, due mainly to the high operating frequency and the relatively complicated asynchronous clock generation mechanism to coordinate the operations of multiple comparators. Sometimes up to about 40% of the ADC power can be consumed by the clock generation block. Fig. 4.16 shows a typical configuration for comparator clock generation used in alternate-comparator architectures [47]. Generally, it is important to keep the common-mode voltage relatively constant in SAR ADCs with medium-to-high resolutions, especially if the comparator offsets are compensated in the background. Since the offsets of most dynamic comparators are subject to common-mode variations, accurate detection of the offset from each comparator would be a difficult task if each comparison is performed at a different common mode. As such, only one comparator is kept active at a time to

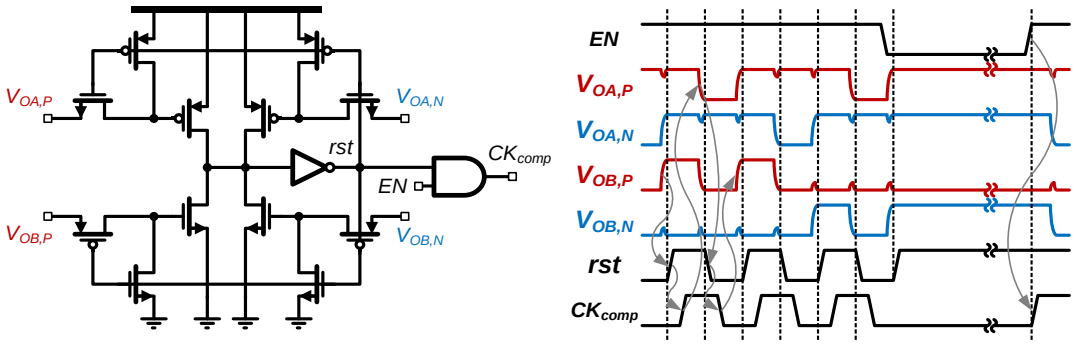


Figure 4.17. Proposed half-rate clock generation circuit for the double-rate comparator.

avoid the kickback-induced common mode decay. This requires the generation of non-overlapping clocks and thus quite a few combinational units, including the pulse generator.

In this work, the timing scheme is largely simplified by the double-rate comparator. As only a half-rate single-phase comparator clock is needed, the clock generation circuit can be implemented with merely a few logic gates, as depicted in Fig. 4.17. When the reset signal rst is high, the differential outputs of Latch-A, namely $V_{OA,P}$ and $V_{OA,N}$ are connected through a pair of NMOS switches to M_{P1} and M_{P2}. As soon as Latch-A makes a valid decision, one of the differential outputs will go low, resulting into a falling edge of rst. The outputs of Latch-A are then disconnected from M_{P1} and M_{P2} and the gate voltages of the PMOS pair are pulled up to V_{DD}. Meanwhile, turned on by the low level of rst, a pair of PMOS switches connect the outputs of Latch-B, i.e. $V_{OB,P}$ and $V_{OB,N}$ to M_{N1} and M_{N2}. The falling edge of rst propagates through an AND gate and yields a falling edge on the comparator clock CK_{comp}, which then enables the comparator for another decision. Once Latch-B finishes the regeneration, one of the

outputs will go high, producing a rising edge on rst to break the connection between Latch-B and the NMOS pair and to discharge the gates of the NMOS pair to GND. Simultaneously, Latch-A is linked to the clock generation circuit again, preparing for another round of comparison. The initiation and termination of the conversion phase is controlled by an enable signal EN.

The simple topology of the clock generation circuit helps to minimize the number of internal nodes, which, in combination with the halved operating frequency, reduces the power dissipation of this block by more than a half in comparison to the implementations in multi-comparator-based architectures and significantly improves the power efficiency of the ADC.

4.5 ADC Implementation

A prototype SAR ADC was implemented to verify the effectiveness of the proposed double-rate comparator and the associated clock generation mechanism. The block and timing diagram of the SAR ADC is shown conceptually in Fig. 4.18. Driven by an external clock CK_{EXT} with a 12.5% duty cycle, the front-end sampling switches are bootstrapped for higher bandwidth and improved linearity. A pair of cross-coupled dummy switches are attached to the frontend for feed-through cancellation [29]. The supply voltage is directly used as the reference for maximum input swing. Though not show in the figure, each capacitor in the DAC is equally separated into two sub-capacitors to maintain a constant common mode during switching. The 10-bit quantization is completed in 11 cycles with a 1-bit redundancy to absorb the decision

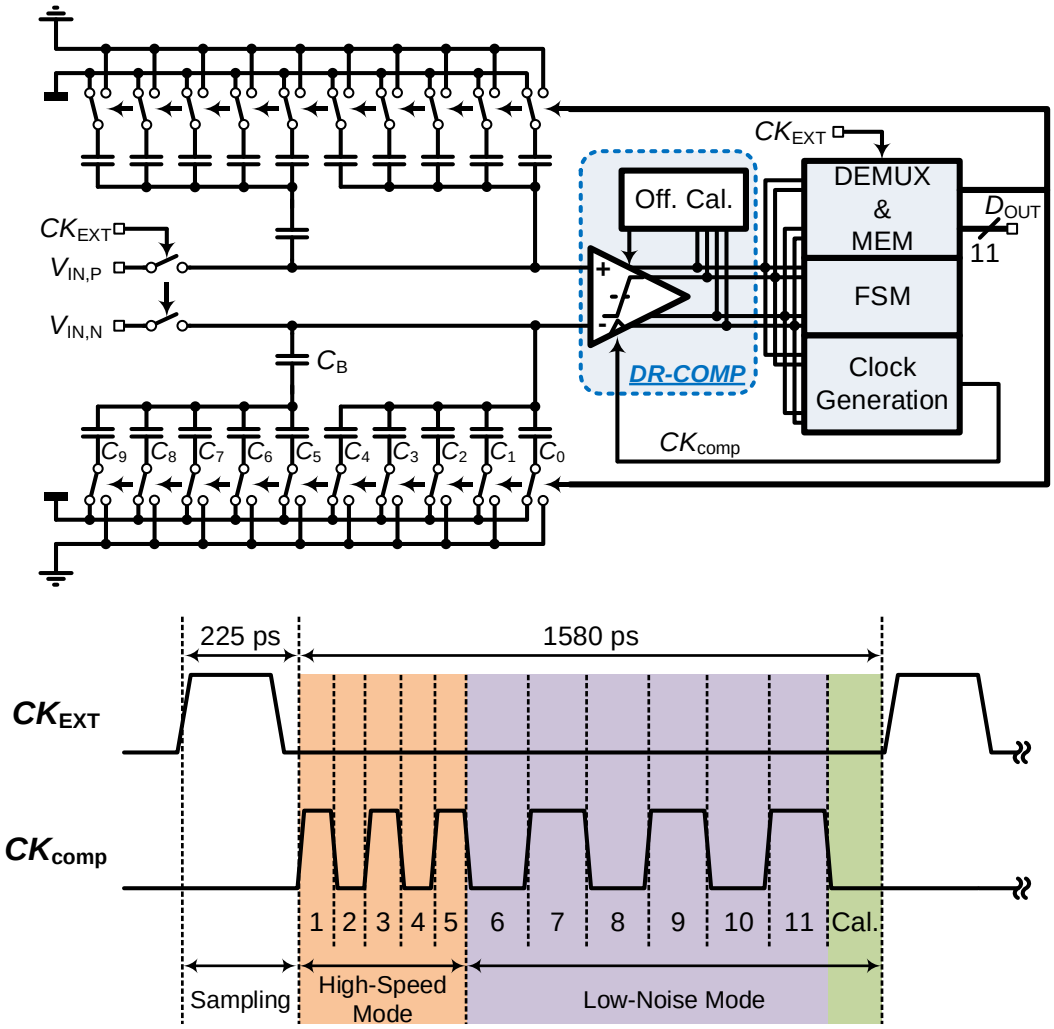


Figure 4.18. Block and timing diagram of the SAR ADC.

errors caused by incomplete settling, noise and offset mismatch between the coarse and fine conversions. A bridge capacitor C_B splits the DAC into the MSB array and the LSB array, leading to smaller capacitor sizes and faster settling. The DAC output is delivered to the double-rate comparator, which is triggered by the internally generated half-rate clock. The double-rate comparator is configured in high-speed mode for the 5-cycle coarse conversion. While the 6-cycle fine conversion as well as the offset calibration phase are carried out in low-noise mode to suppress the input-referred noise. The

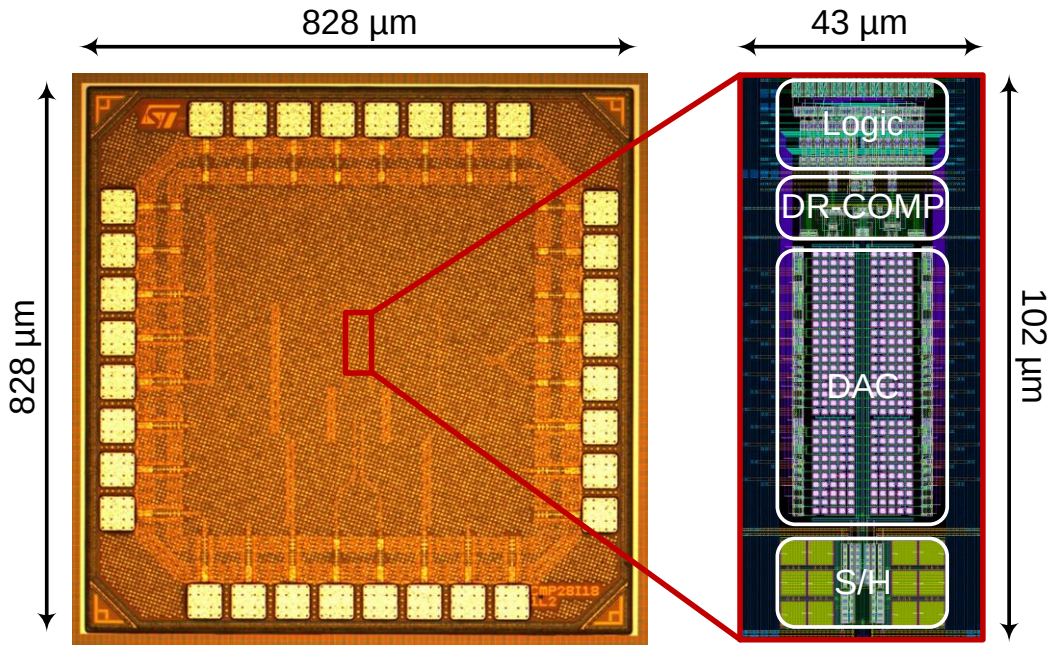


Figure 4.19. Chip micrograph and layout of the ADC in 28-nm FDSOI.

memory cells adopted in this design resemble those used in [41] to minimize the data-path delay and loading to the comparator.

The prototype ADC was fabricated in a 1P8M 28-nm FDSOI technology. Fig. 4.19 shows the chip micrograph and a zoomed-in layout view of the ADC core, which occupies an active area of 43 μm × 102 μm.

4.6 Measurement Results

The outputs of the ADC are decimated on chip by a factor of 45 to facilitate data collection. The power breakdown at around 550 MS/s is shown in Fig. 4.20. The ADC core consumes a total of 1.28 mW, where 0.28 mW and 0.23 mW are dissipated by the double-rate comparator and the clock generation circuit, respectively. Fig. 4.21 shows

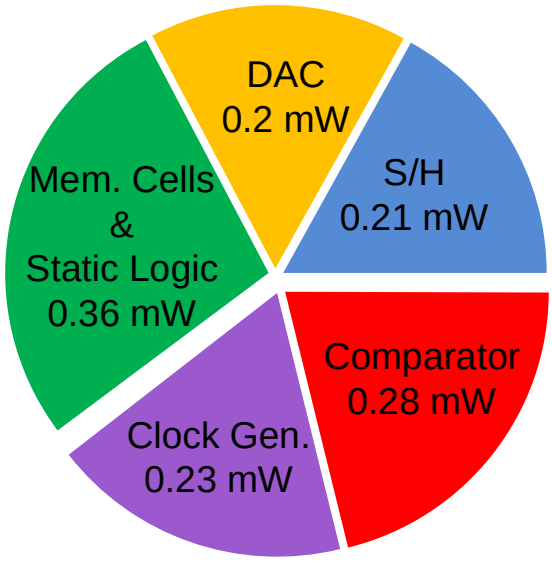


Figure 4.20. Power breakdown at around 550 MS/s.

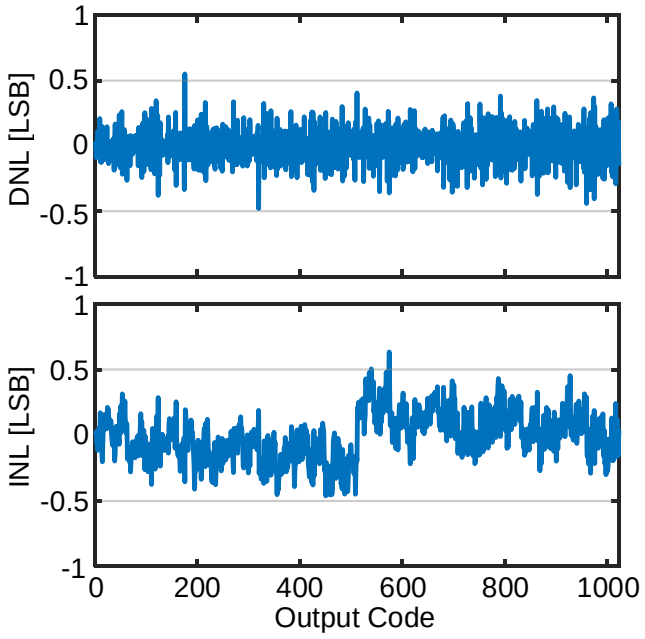


Figure 4.21. Differential and integral non-linearities.

the static linearity performance of the ADC. The maximum DNL and INL are -0.47/+0.54 LSB and -0.46/+0.63 LSB, respectively.

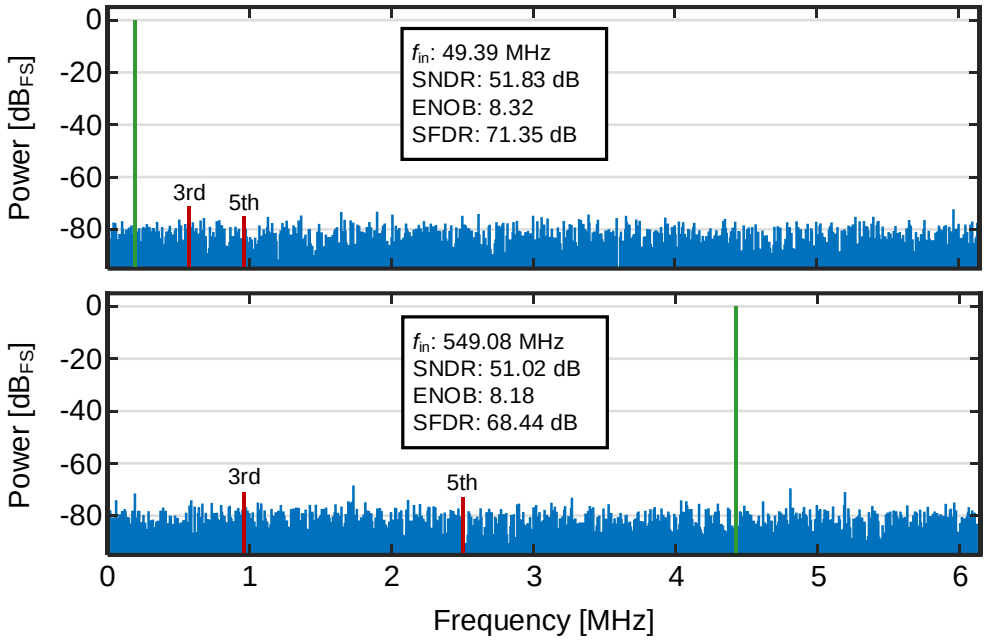


Figure 4.22. Measured output spectrum at 553.5 MS/s (×45 decimated).

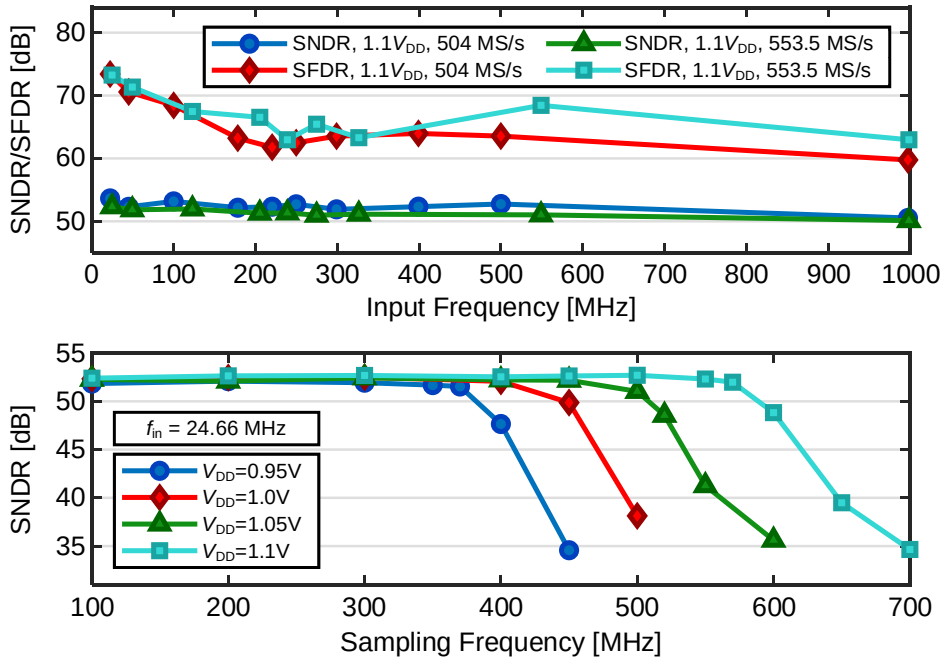


Figure 4.23. Measured SNDR and SFDR versus input frequency and sampling rate.

Table 4.1. Performance Summary and Comparison

Specifications	[29]	[43]	[44]	[63]	This work
Architecture	SAR	2b/c SAR	2b/c SAR	Pipe. SAR	SAR
Technology (nm)	20	65	40	28	28 FDSOI
Resolution (bits)	10	10	10	10	10
Sample Rate (MS/s)	320	400	300	500	550
Supply Voltage (V)	1.0	1.1	1.2	1.0	1.1
$SNDR_{@Nyquist}$ (dB)	50.9	51.9	47.0	56.6	51.6
$SFDR_{@Nyquist}$ (dB)	58.6	63.7	63.0	69.2	66.9
$ENOB_{@Nyquist}$ (bits)	8.16	8.33	7.51	9.11	8.28
Power (mW)	1.52	5.6	2.1	6.0	1.28
FOM_W (fJ/conv.-s.)	16.6	43.0	19.3	21.7	7.5
Core Area (mm^2)	0.0012	0.075	0.0085	0.015	0.0043

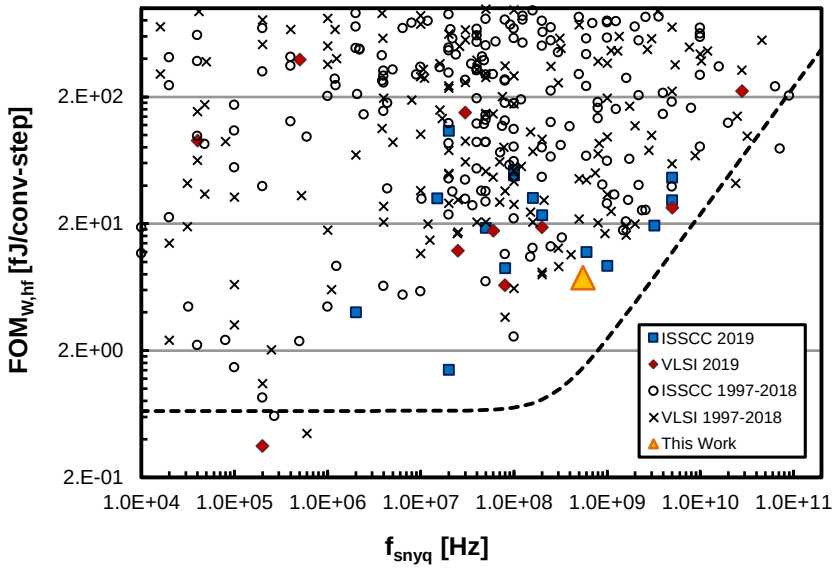


Figure 4.24. Comparison of Walden FOM with ADCs presented at ISSCC and VLSI between 1997 and 2019.

Fig. 4.22 shows the measured decimated spectrum at 553.5 MS/s, with 49.39-MHz and 549.08-MHz full-scale inputs, respectively. Fig. 4.23 shows the measured dynamic performance with the input frequency and the sampling frequency swept. Clocked at 553.5 MS/s, the ADC maintains a SNDR of above 51 dB with an input frequency of up to 550 MHz. As the input frequency increases to 1 GHz, the SNDR still stays above 50 dB, leading to a greater than 1-GHz ERBW. Supplied by 1.1 V, the ADC shows a relatively constant performance as the sampling rate increases from 100 to 580 MS/s. Beyond 580 MS/s, however, a performance drop occurs due to the incomplete calibration phase and SAR cycles.

Table 4.1 summarizes the measured performance and compares it against the state-of-the-art single-channel SAR-based ADCs with comparable speed and resolutions. Fig. 4.24 compares the Walden FOM of the prototype ADC against all ADCs presented at ISSCC and VLSI between 1997 and 2019. This work shows a Nyquist FOM of 7.5 fJ/conv.-step, which is the best among previously reported ADCs with sampling rates of >300 MS/s [1].

CHAPTER V

TIME-INTERLEAVED SAR ADC

5.1 Motivation

Direct sampling receivers in broadband communication systems require ADCs with GS/s sampling rates, medium-to-high resolutions as well as excellent power efficiency. A lot of research efforts have recently been invested into the development of ADCs that meet these stringent requirements. TI pipeline ADCs [2, 3, 4, 5] provide optimum solutions to both high accuracy and sampling rates up to GS/s. However, the cost is also significant as the gain stages mandate power-hungry and complex op-amp designs, which puts a lower limit of several hundreds of milliwatts on the minimum possible ADC power consumption. In addition, the low supply voltage of the advanced technology nodes poses a great challenge on the amplifier design and severely clamps the maximum input swing of the ADCs, incurring yet more power budget for noise suppression. TI pipeline ADC with ring amplifiers [10] and TI pipelined SAR ADC with dynamic amplifiers [11] replace the classic operational transconductance amplifiers (OTAs) with more scaling-friendly architectures for power efficient residue amplification. However, as both the architectures are subject to PVT variations, complex calibrations are needed to address the gain errors and maintain the target accuracy. TI SAR ADCs [6, 7, 8, 9] have been a popular choice for achieving the afore-mentioned challenging requirements, due to their continuously increasing operation

speed and constantly decreasing power consumption as the downscaling of CMOS technology advances. However, the interleaving architecture induces extra power and area costs, especially with a large interleaving factor. These extra costs come from the multi-phase clock generation, multi-channel reference supply, data multiplexing and inter-channel mismatch calibrations, most of which are hard or impossible to avoid. As such, further improvement of the single-channel ADCs in terms of power efficiency and conversion rate is crucial for the optimization of the overall architecture. It is proposed in [47] that two alternate comparators can be employed to boost the conversion rate of a single-channel SAR ADC by eliminating comparator reset time from the critical path. However, the background calibration used to address the offset mismatch lowers the speed gain and induces power overhead.

In the past few years, demands for energy efficiency and long battery life in biomedical applications have stimulated the development and refinement of SAR ADCs with window-based bypass switching techniques [52, 53, 54, 55, 56], where sampled input signals that fall within a pre-defined bypass window can be quantized with fewer conversion cycles, avoiding unnecessary DAC switching and comparisons. However, the power efficiency improvements in [52, 53, 54, 56] are degraded by the extra power consumption of the bypass detection mechanism. A VCO-based comparator is adopted in [55] to generate both the decision bit and bypass information simultaneously without power penalty. However, the relatively slow operation speed of the VCO-based comparator makes it less attractive as a candidate for high-speed applications.

In this work, two alternate comparators are adopted in each ADC channel as in [47] for enhanced operation speed and the concept of bypass window is borrowed from

the works for biomedical applications with a tailored implementation to enable modest power efficiency improvement in high-speed operations. Instead of tuning the comparator offsets on a regular basis at the cost of compromised conversion rate as in most works, the comparator offsets are opportunistically calibrated when bit cycle bypass is triggered, where the ADC conversion time will be considerably shorter as compared to normal cases. Different from the offset calibration scheme reported in [57], the opportunistic calibration does not require a reference comparator that needs to be triggered twice per conversion for self-calibration and mismatch sensing, respectively. This leads into a lower power consumption. In addition, the reference voltage of each ADC channel is provided by a pre-charged reservoir to prevent the inter-channel crosstalk without introduction of power-hungry distributed reference buffers. These techniques are demonstrated by a 10-bit 8-channel time-interleaved SAR ADC fabricated in a 28 nm FDSOI process. Clocked at 2.4 GS/s, the ADC achieves a Nyquist SNDR of 49.02 dB while consuming only 9.8 mW from a 0.9 V supply, leading into a Walden FOM of 17.7 fJ/conv.-step and a Schreier FOM of 159.9 dB.

5.2 Bypass Window-Based Calibration

5.2.1 Review of the Bypass Window Technique

The operation of a bypass switching SAR ADC can be appreciated with a 6-bit example, as depicted in Fig. 5.1. Assuming for simplicity that each bit cycle consists of a comparison and a DAC switching. A ±2-LSB bypass window is applied to the first 4 bit cycles (P_1-P_4). Two switching trajectories (one with bypass switching and one

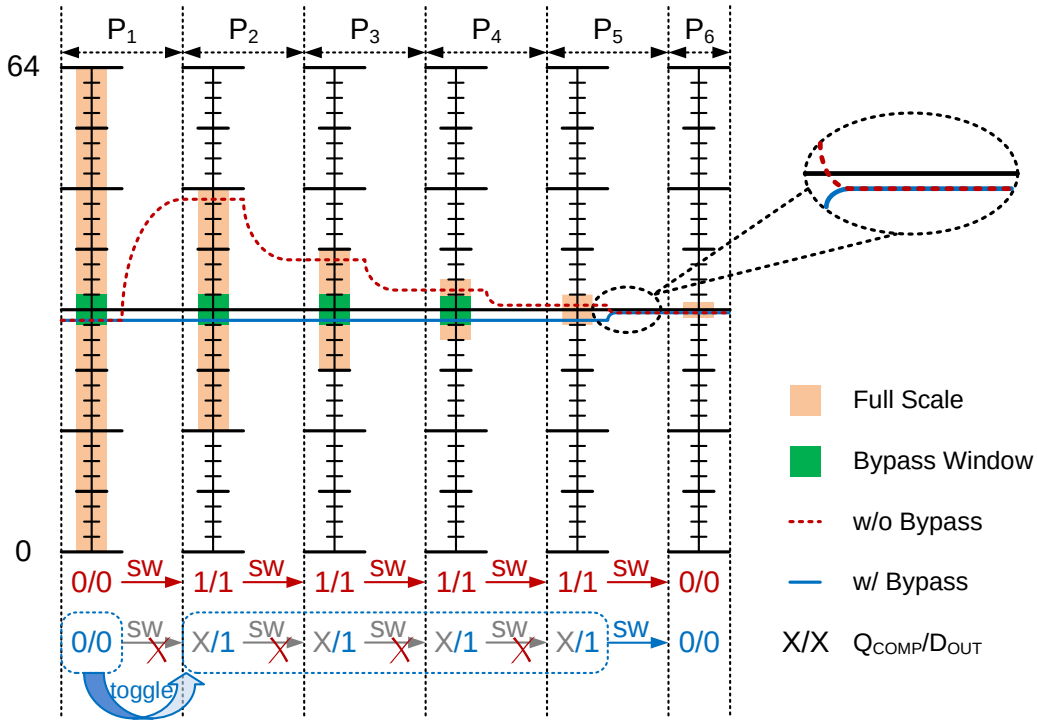


Figure 5.1. Comparison of a 6-bit conversion process between conventional SAR ADCs and bypass window-based SAR ADCs.

without) for the same input are shown in one plot. As the input is located within the bypass window, which is of the same size as the full-scale range of P_5, the quantization of the input can thus theoretically be completed without activating P_1-P_4. As can be seen from Fig. 5.1, the two trajectories converge to the same value in P_6, indicating identical conversion results for the last bit. To yield a completely identical results between the two trajectories, the results from P_2-P_5 need to be set correctly. Fortunately, this is not difficult since they are highly predictable and show the opposite polarity to the result obtained from P_1. Though the comparison in P_1 cannot be practically avoided in bypass switching-based conversion as it is not known beforehand if the signal falls within the bypass window, the comparison result can be used to direct the DAC switching in P_5.

As such, the DAC switching in P_1-P_4, as well as the comparator strobing in P_2-P_5 can be avoided. This amounts to an avoidance of 4 complete cycles.

The typical configuration for a bypass window-based SAR ADC is shown conceptually in Fig. 5.2. Different from a conventional SAR ADC, the bypass window-based SAR ADC requires in general a bypass detection circuit, which may take a couple of forms depending on the specific implementation. In [52] and [53], the bypass detector is composed of two extra coarse comparators with one of the inputs in both comparators attached to a threshold voltage (V_R) defined by the window size. The two extra comparators are used to perform the first few bit cycles, some of which may be skipped provided the two comparators yield the same results, indicating the signal or residue has fallen into the bypass window. As the first architecture where the concept of bypass window is introduced, this configuration provides a straightforward solution to power efficiency enhancement by skipping unnecessary DAC switching and comparator strobing. However, the drawbacks are also obvious. First, the bypass window is essentially constructed for a single-ended detection, which is subject to common-mode variation or noise. In addition, false trigger of the bypass window can result into error codes. This rebates the practical benefits of energy saving as the extra detection circuit introduces considerable power overhead.

In [54], the bypass detector is implemented as a dynamic current correlator cascaded by a latch, which are integrated into the main comparator to provide the information about the absolute range of the residue. By adjusting the voltages on the gates of the MOS-CAPs ($V_{REF,BUMP}$ and $V_{REF,DIFF}$), the capacitance and thus the window

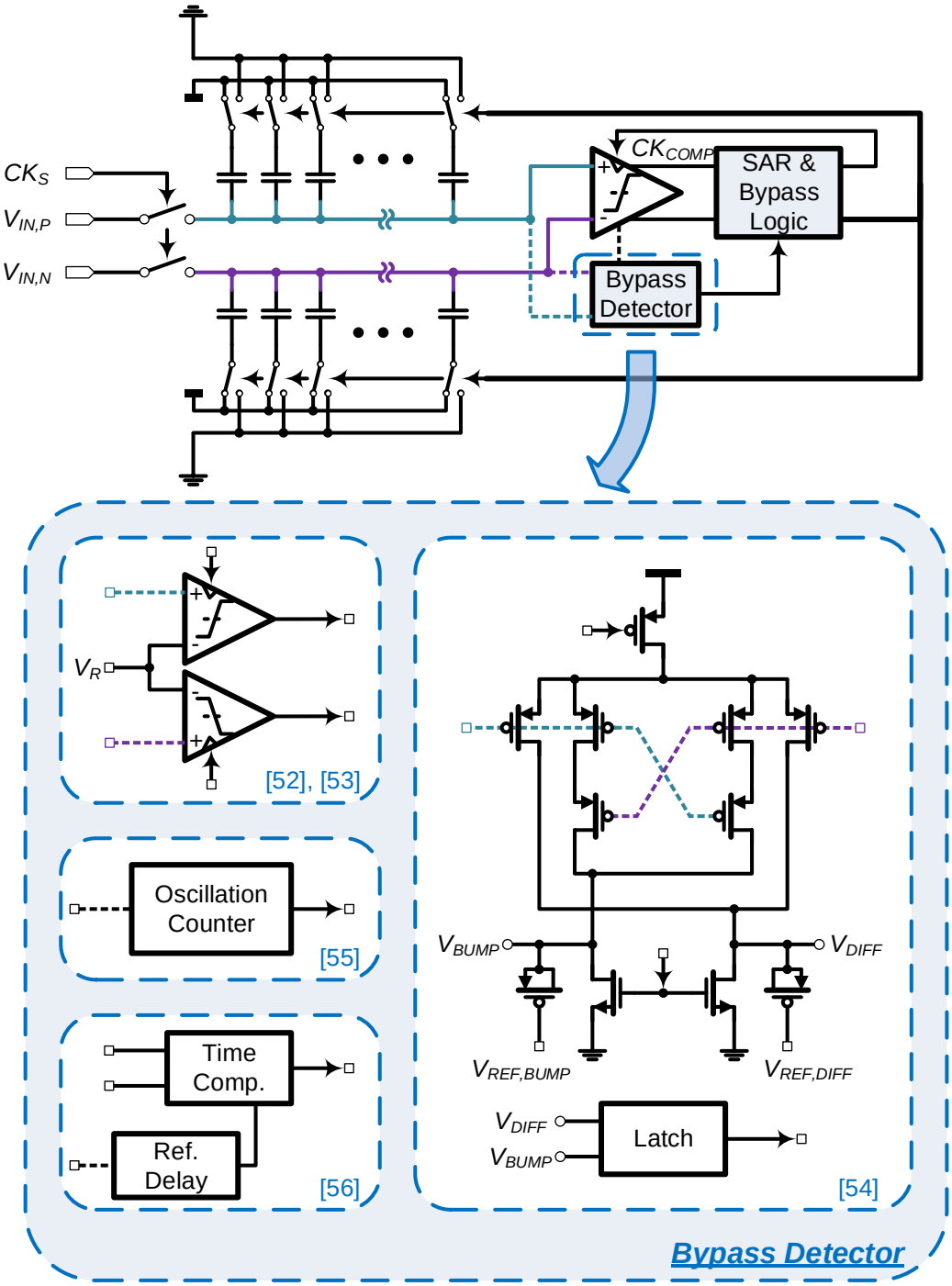


Figure 5.2. Typical configuration for a bypass window-based SAR ADC.

size can be tweaked. As such, complex calibrations are needed to obtain a well-controlled window size.

A low-cost solution to bypass detection is presented in [55], where a novel VCO-based comparator is adopted for both the polarity comparison and the construction of a bypass window. Since the number of oscillation cycles generated during the process of VCO-based comparison can serve as an approximate indicator of the input range, the bypass detection can be readily carried out by keeping a record of the oscillation cycles with a counter, whose output can then be used to trigger the bypass logic. However, this architecture is less attractive in high-speed domains due to the relatively low operation speed of the VCO-based comparator and the possibly elongated conversion process provided a background calibration is needed for window size adjustment.

It is proposed in [56] that the transient information of a latched comparator can be leveraged to estimate the amplitude of the input voltage. In combination with reference grouping, this architecture reduces both the maximum and the average number of conversion cycles. The main shortcomings, however, are that the redundancy range required for settling relaxation is highly limited and that time-based comparisons are prone to PVT variations. Moreover, the time-domain detection mechanism consumes extra power.

5.2.2 Proposed Low-Cost Bypass Window

Since the bypass window constructions in [52, 53, 54, 55, 56] are highly integrated into the operation of the comparator, it is almost impossible to implement them without significant cost in a high-speed SAR-based ADC architecture where multiple comparators are used to boost the conversion rate. To decouple the window size from the comparator operations and avoid complex calibrations, we propose to

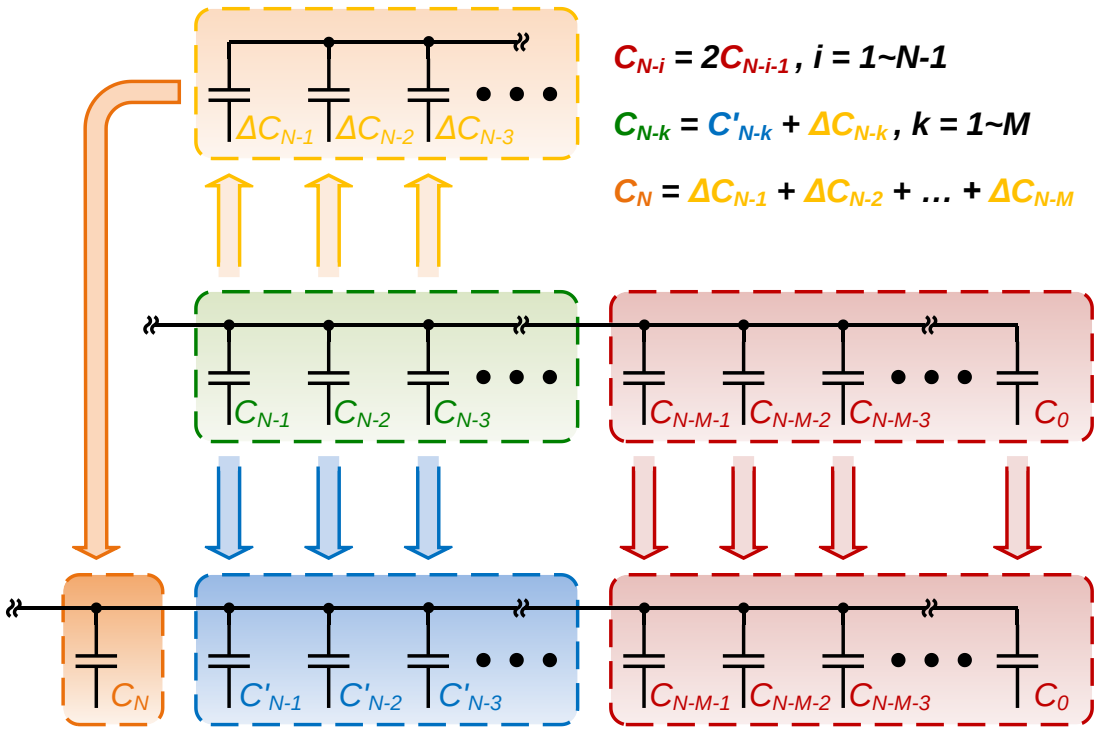


Figure 5.3. Construction of the proposed bypass window.

construct the bypass window by customizing the capacitive feedback DAC, where the window size can be well defined by the capacitor ratio.

The concept of the proposed low-cost bypass window is illustrated in Fig. 5.3. Assuming a binary DAC consisting of N capacitors, which are divided into two groups, namely C_{N-1} to C_{N-M} and C_{N-M-1} to C_0, where $C_0=C_u$ is the unit capacitor. In constructing the new DAC that enables the bypass window, each capacitor in the first group (C_{N-1} to C_{N-M}) is split into two sub-capacitors. This generates another two groups of capacitors, namely ΔC_{N-1} to ΔC_{N-M} and C'_{N-1} to C'_{N-M}. ΔC_{N-1} to ΔC_{N-M} are then merged into a single capacitor C_N, which is concatenated with C'_{N-1} to C'_{N-M} and C_{N-M-1} to C_0 to form the new DAC. The bypass window size is given by

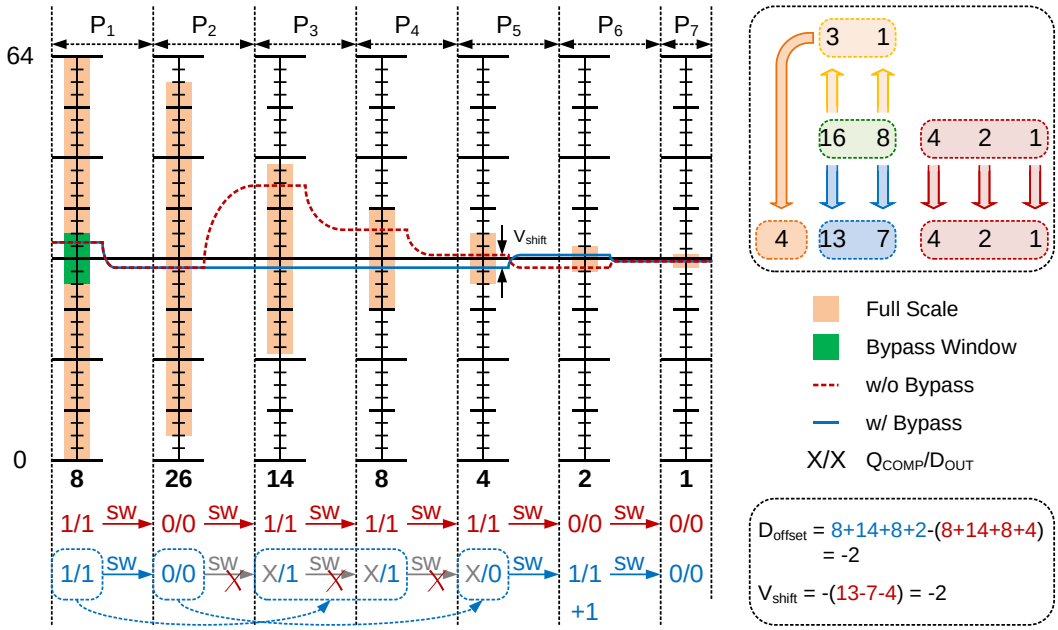


Figure 5.4. A 6-bit example of the proposed bypass switching.

$$win = \pm \frac{C_N}{C_u} LSB\,. \tag{5.1}$$

On the other hand, since the newly generated capacitor array is not binary-weighted, redundancies are introduced during the procedure of capacitor split and reformation. But to avoid overrange errors, the following relationship needs to hold

$$\Delta C_{N-i} \geq \sum_{j=i+1}^{M} \Delta C_{N-j},\ 1 \leq i \leq M-1\,. \tag{5.2}$$

The redundancy range for each bit can be expressed as

$$\begin{cases} \mathrm{Re}_i = 2\times C_i' - \sum_{j=i-1}^{N-M} C_j' - \sum_{k=0}^{N-M-1} C_k - C_0,\ N-M+1 \leq i \leq N-1 \\ \mathrm{Re}_{N-M} = 2\times C_{N-M}' - \sum_{k=0}^{N-M-1} C_k - C_0 \end{cases}. \tag{5.3}$$

Fig. 5.4 shows a 6-bit example of the proposed bypass switching. The first two capacitors in a conventional binary array are split into two groups, $13(2^4\text{-}2^1\text{-}2^0)$, $7(2^3\text{-}$

2^0) and $3(2^1+2^0)$, $1(2^0)$. Then $3(2^1+2^0)$ and $1(2^0)$ cells are combined into a single capacitor to be positioned before all other capacitors to generate a bypass window with a size of 8 LSB (±4 LSB). In case different decisions are made in the first two cycles, indicating the signal falls within ±4 LSB around the common mode, the bypass switching will be triggered and the DAC switching in P_2-P_4 together with the comparator operations in P_3-P_5 will be skipped. However, due to the voltage shift between the two trajectories after the bypass, an offset of -2 is resulted in the bypass-based output. Hence it has to be removed from the raw codes during post processing for the ADC output to be correct.

5.2.3 Opportunistic Adaptive Comparator Offset Calibration

As a main drawback of ADC architectures that adopt more than one comparator for conversion acceleration, the non-uniform offsets need to be compensated in the background to track the PVT variation. Unfortunately, the speed gain can be highly rebated by the background calibration in the sense that a portion of the conversion time has to be allocated to offset extraction. To avoid conversion rate compromise due to regularly triggered compensation mechanism for the offset mismatch of the alternate comparators, an opportunistic adaptive comparator offset calibration is proposed in this paper, taking advantage of the bypass window-based conversion truncation.

The control scheme of the proposed offset calibration is depicted in Fig. 5.5. The scheme is based upon a two-comparator architecture. However, it can be easily generalized to architectures where more comparators are utilized by applying some small changes. In normal cases, the complete conversion phase takes N + 2 cycles. Each

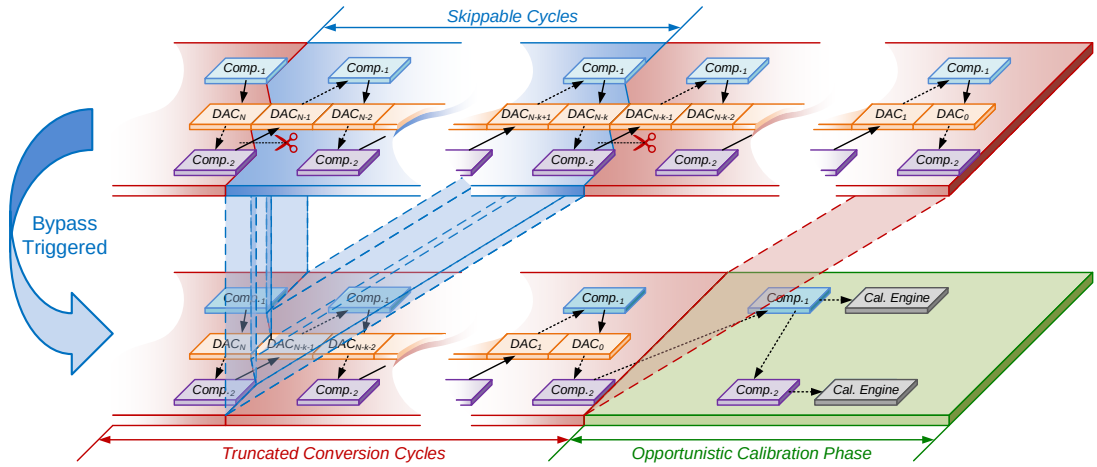


Figure 5.5. DAC and comparator control scheme of the proposed opportunistic offset calibration.

cycle involves the operation of a comparator and a DAC switching, with an exception of the last cycle, where the DAC switching is unnecessary and thus removed. Upon triggering of the bypass window, k cycles are to be skipped and the incision will be sutured by directing the switching of DAC_{N-k-1} with the decision of the second comparison. This truncates the conversion phase into N - k + 2 cycles. In the meantime, Each time the bypass window is triggered, the conversion can be completed in less cycles than normal cases, an opportunistic calibration phase is then inserted between the truncated conversion phase and the next sampling phase to extract and update the offset of the comparators. Since the calibration phase is only activated as the bypass switching is triggered, the comparator offset is updated only when the input falls within the bypass window. a certain requirement, dictated by the specific window size, is posed on the input voltage, as explained in Fig. 5.6. Though this requirement on input voltage can be easily met in broadband communication systems, the convergence speed of the calibration algorithm can be affected because the comparator offsets are updated less

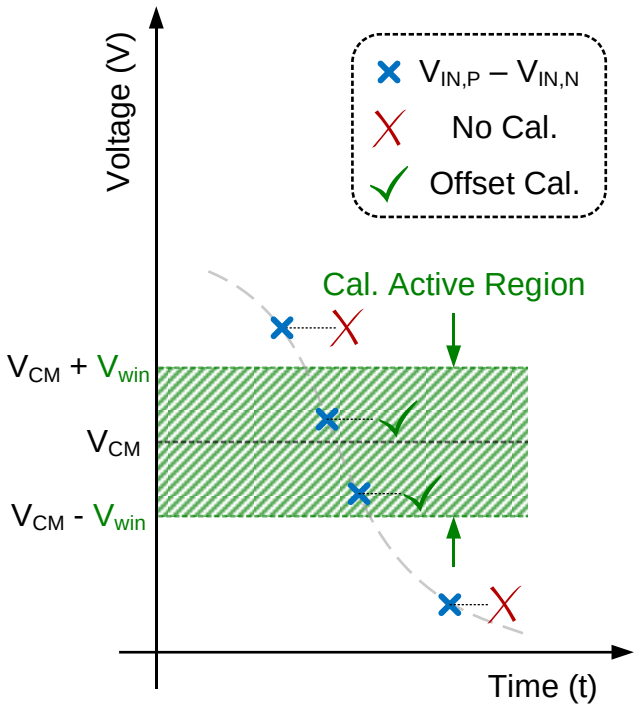


Figure 5.6. Input range limitation of the offset calibration.

frequently then in conventional cases. To partially compensate for the reduced convergence rate, an adaptive calibration technique is adopted.

For calibration procedures using a single step size, there is always a tradeoff between the convergence speed and the algorithm noise. Small calibration steps suffer from slow convergence but produce less noise after settling, which is in stark contrast to large calibration steps. To break the tradeoff, the step size has to be adaptively set according to the specific stage of the calibration settling. Fig. 5.7 depicts the calibration setup and logic flow. During calibration phase, the comparator input is shorted by a switch. And then the comparator is strobed, the output is collected and processed by the calibration circuits, which are made up of the adaptive control logic and two pairs of switched-capacitor charge pumps (SCCPs) with per-step transfer charges ΔQ_C and ΔQ_F,

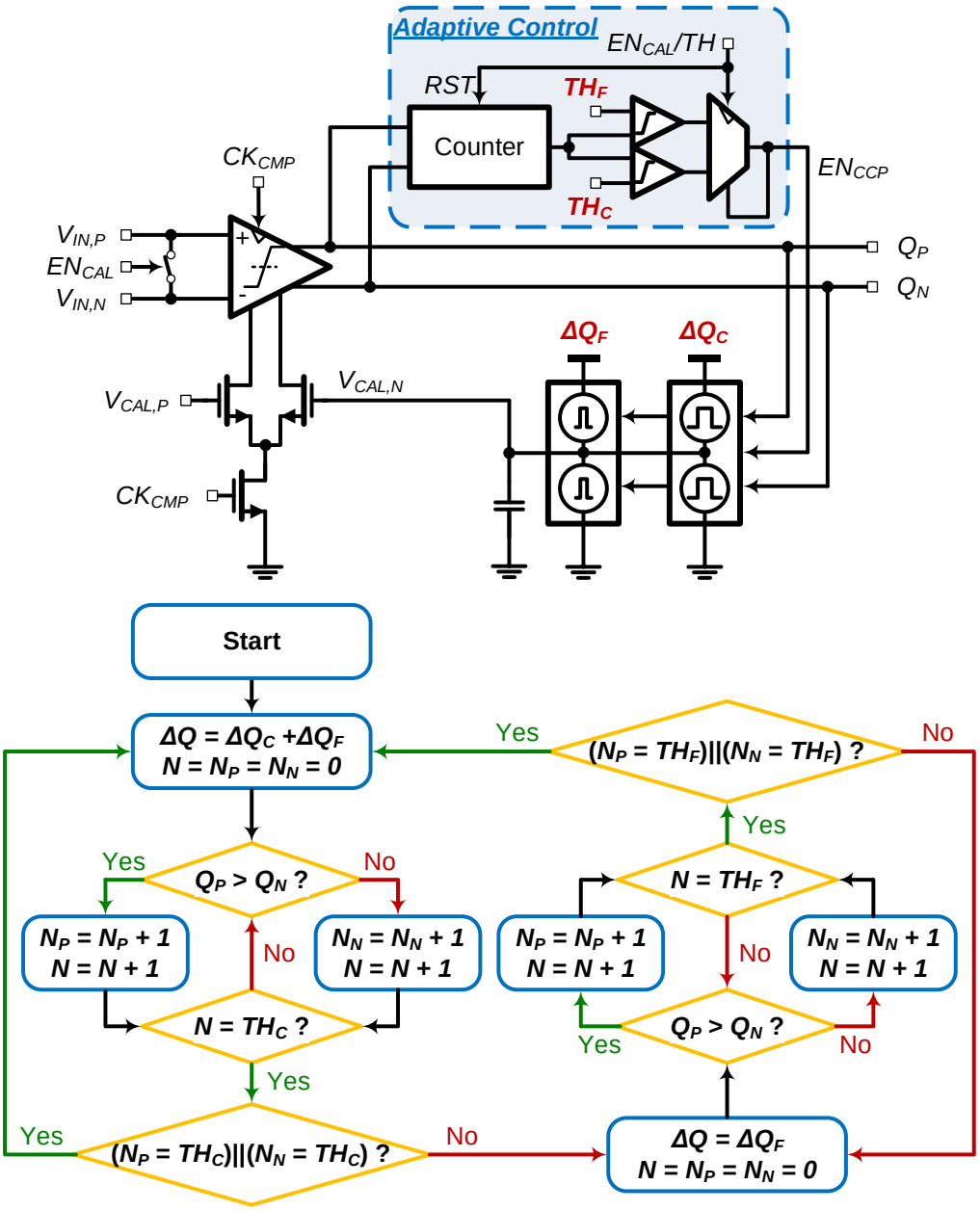


Figure 5.7. Setup and logic flow of the adaptive offset calibration.

respectively. The outputs of the SCCPs are fed to a second input pair of the comparator to alter the offset. The adaptive step size control is achieved by a counter cascaded by two digital comparators with a threshold value of TH_C and TH_F, respectively. The outputs of the SCCPs are fed to a second input pair of the comparator to alter the offset.

The adaptive step size control is achieved by a counter cascaded by two digital comparators with a threshold value of TH_C and TH_F, respectively. The outputs of the digital comparators are multiplexed and used to drive the coarse SCCP as an enable signal. Upon initiation, the step size is set to $\Delta Q_C + \Delta Q_F$ by asserting the coarse charge pump enable signal EN_{CCP}. This helps to accelerate convergence. Each time the comparator makes a decision in calibration phase, the counter updates the number of positive decisions, N_P, or that of negative decisions, N_N, accordingly. For every TH_C decisions, if all of them are of the same polarity, indicating the calibration voltages $V_{CAL,P}$ and $V_{CAL,N}$ are still way from convergence, the step size is kept unchanged. Otherwise, the calibration algorithm is considered as having converged and the coarse charge pump is turned off, changing the step size to ΔQ_F. As ΔQ_F is sized considerably smaller than ΔQ_C, $V_{CAL,P}$ and $V_{CAL,N}$ fluctuate around the final value, producing negligible calibration noise. At this stage, the counter still keeps a record of N_P and N_N, but the comparison is performed against another threshold TH_F. If either N_P or N_N reaches TH_F within TH_F calibration cycles, indicating a large offset shift is detected and the calibration voltages need to converge to a new value, the coarse charge pump is turned back on, changing the step size to $\Delta Q_C + \Delta Q_F$, the calibration process is then reset to the initial state. Otherwise, the convergence is considered as being maintained and the step size remains unchanged.

The settling behavior of the proposed adaptive calibration is greatly affected by three important parameters, i.e., TH_C, TH_F and the ratio of ΔQ_C to ΔQ_F ($\Delta Q_C/\Delta Q_F$). To explain the effects of the three parameters on the algorithm convergence and noise, behavioral simulations are conducted and the results are shown in Fig. 5.8. TH_C decides

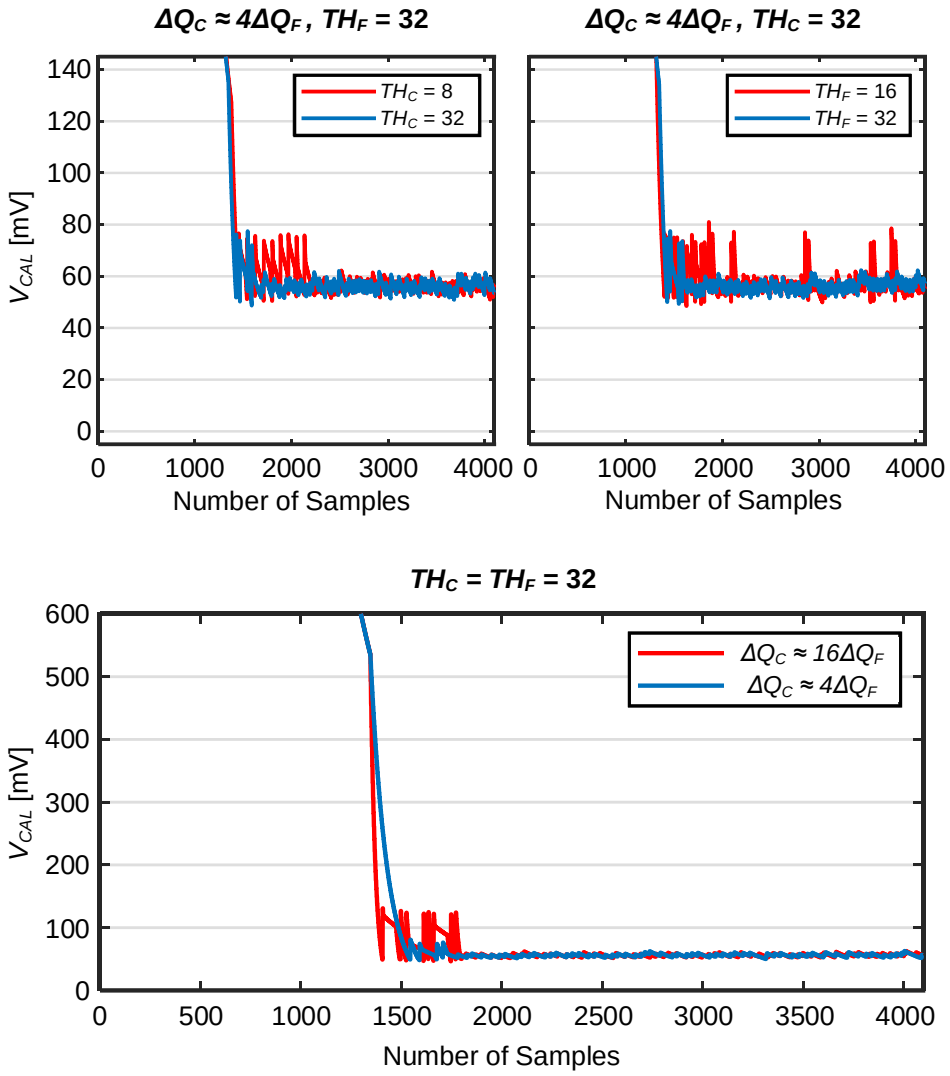


Figure 5.8. Effects of the three parameters (TH_C, TH_F and ΔQ_C/ ΔQ_F) on the calibration convergence and noise.

how difficult for the step size change from $\Delta Q_C + \Delta Q_F$ to ΔQ_F to take place. In analogy, TH_F determines the likelihood of the step transition from ΔQ_F to $\Delta Q_C + \Delta Q_F$. The value of $\Delta Q_C/\Delta Q_F$ dictates the gap between the coarse and fine steps and thus the smoothness of the transition. Its effect resembles that of TH_C. In general, TH_C needs to be sized large enough to avoid or reduce frequent toggling between the two calibration steps when the

system is trying to converge. This is because if TH_C is sized too small, a state of convergence could be wrongfully perceived by the system when the calibration voltages are still far from the target value. Then the step size is switched to ΔQ_F. After TH_F cycles of updates, the calibration voltages are still not settled due to the small size of ΔQ_F. The step size is then switched to $\Delta Q_C + \Delta Q_F$ again. This situation can be deteriorated if the value of $\Delta Q_C/\Delta Q_F$ is too large, as the gap between the two steps has to be filled by more cycles of toggling. On the other hand, a relatively large TH_F is also desired to prevent false detection of large offset shift after the state of convergence has been reached. However, a too large TH_F can excessively desensitize the system to offset variation and slow down the convergence to the new final value. The worst-case settling usually happens when the calibration voltages are near supply rails, as the difference between the positive step and the negative step of the SCCP comes to the maximum level. Since the operation of SCCP is based upon charge sharing between the two capacitors, the calibration voltage can be expressed by [58]

$$V_{CAL}[k+1] = \frac{V_{CAL}[k] \cdot C_{CAL} + V_{SW} \cdot C_{SW}}{C_{CAL} + C_{SW}}, \tag{5.4}$$

where V_{SW} is the voltage across C_{SW}, which is used for charge sharing. As $V_{CAL}[k]$ is near to one supply, V_{SW} can be either very close to or very far from $V_{CAL}[k]$, depending on the switching direction. This creates the largest difference between the up and down step and sets the lower limit of TH_C and TH_F as well as the upper limit of $\Delta Q_C/\Delta Q_F$ for a specific settling requirement. In this work, TH_C, TH_F and $\Delta Q_C/\Delta Q_F$ are set to 32, 32 and 4 respectively for optimized convergence rate, algorithm noise and hardware implementation, which is detailed in Section 5.4.2. A comparison between the

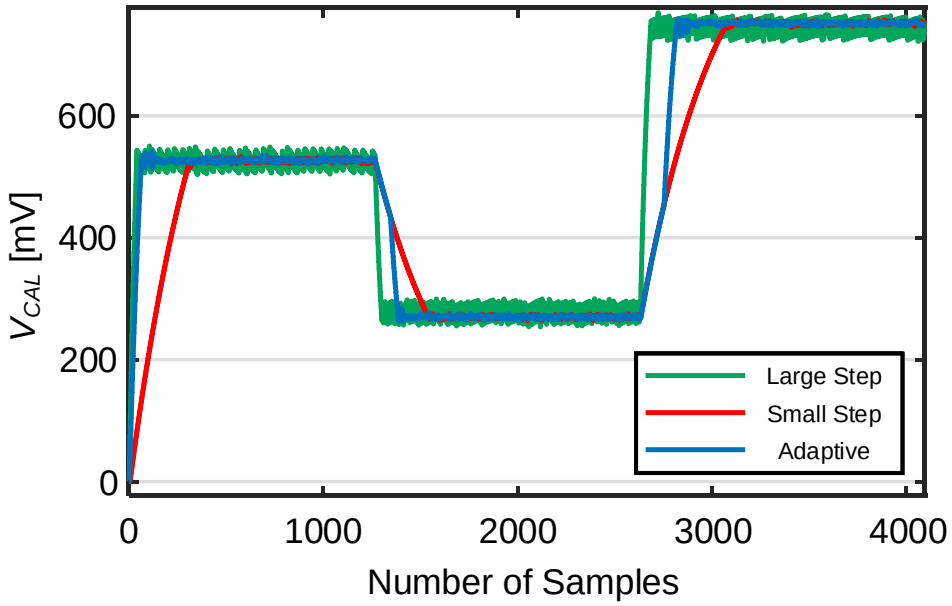


Figure 5.9. Comparison of the offset calibration with large, small and adaptive steps (TH_C=TH_F=32, $\Delta Q_C \approx 4\ \Delta Q_F$).

calibration algorithm settling with large step, small step and the proposed adaptive step is illustrated in Fig. 5.9. As can be seen from the plot, the adaptive-step calibration shows almost the same convergence rate as the large-step calibration during startup, while the calibration noise is of identical level to the small-step calibration after convergence. Though due to the desensitization effect of TH_F, the adaptive system reacts more slowly than the large-step one to large offset shifts, it maintains a faster convergence as compared to the small-step system. This speed advantage grows more obvious as the offset shift becomes larger.

5.2.4 Discussion on the Effects of the Bypass Window

Since the power contributed by the comparators and the SAR logic is largely correlated with the operation frequency, it can be estimated by the average number of cycles per conversion, as shown in Fig. 5.10. Assuming a sine input, since the sampling instant of the ADC is evenly distributed across the time axis, the probability that the input signal falls within ($V_{CM} - V_{win}$, $V_{CM} + V_{win}$) can be expressed as

$$P_{win} = \frac{4\Delta t}{T} = \frac{2\arcsin\left(\frac{2V_{win}}{V_{FS}}\right)}{\pi} = \frac{2\arcsin\left(\frac{2win}{2^{N_{res}}}\right)}{\pi}, \tag{5.5}$$

where N_{res} is the resolution of the ADC. It is not difficult to summarize that the number of bit cycles with and without bypass switching are $\log_2 win + 2$ and $N_{res} + 1$, respectively. The average cycle number is thus

$$\overline{N_{cycle}} = P_{win}\left(\log_2 win + 2 + N_{cal}\right) + \left(1 - P_{win}\right)\left(N_{res} + 1\right), \tag{5.6}$$

where N_{cal} is the number of calibration cycles per trigger. Fig. 5.11 shows the average cycle number and the simulated DAC switching power as a function of the window size. A ±128-LSB bypass window can save up to around 6% of power, taking the power saving on comparators, logic and DAC into consideration. With the calibration phase inserted, the average cycle number does not show a significant variation over the window size, as the skipped cycles are partially replaced by the calibration ones. However, a modest reduction of 8.4% to 9.7% on the average cycle number is achieved in comparison to conventional cases with a regular calibration phase, which requires 12 full cycles for each conversion. In this work, to prevent large common-mode variation

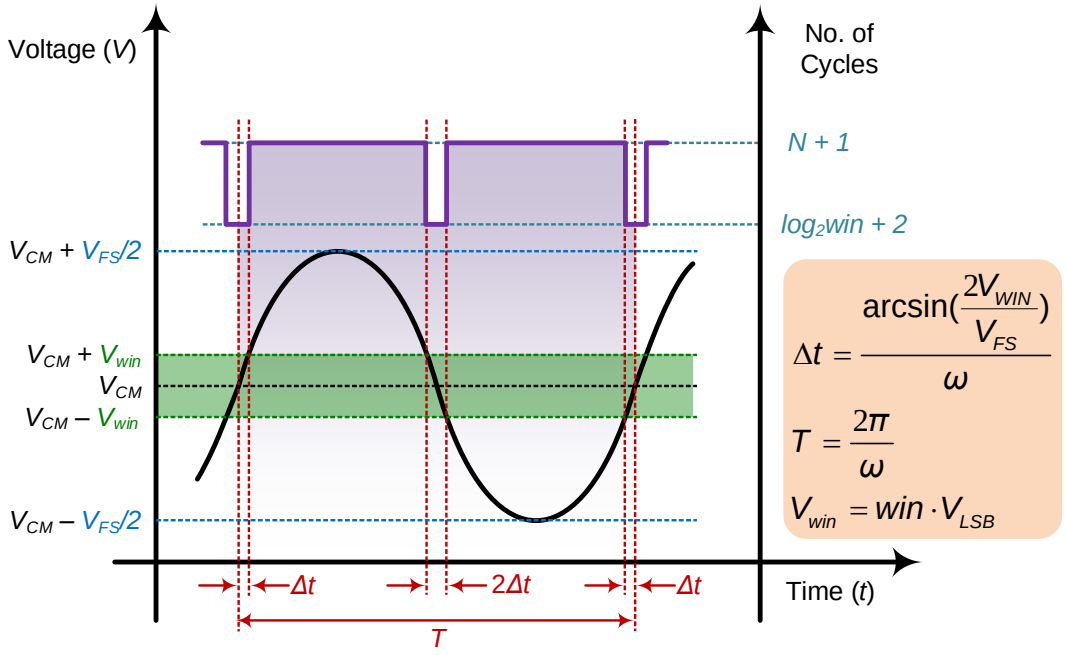


Figure 5.10. Estimation of the average cycle number.

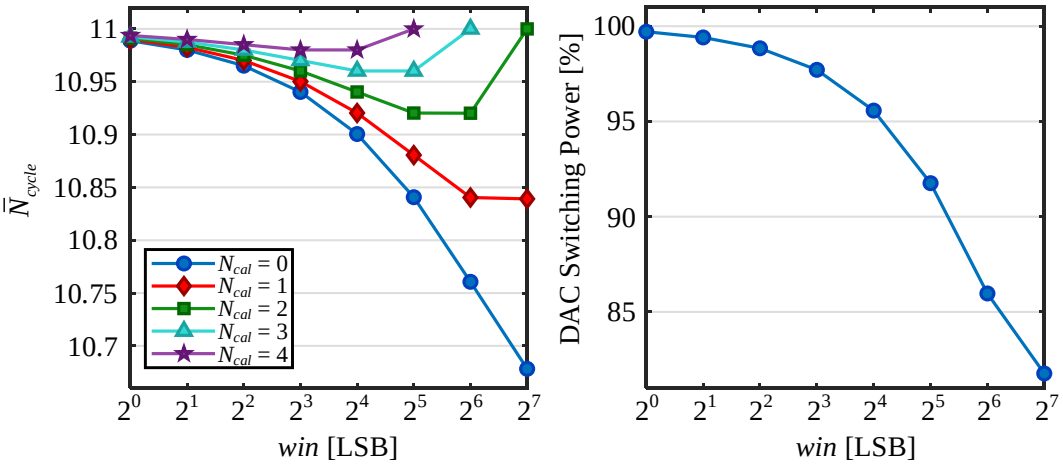
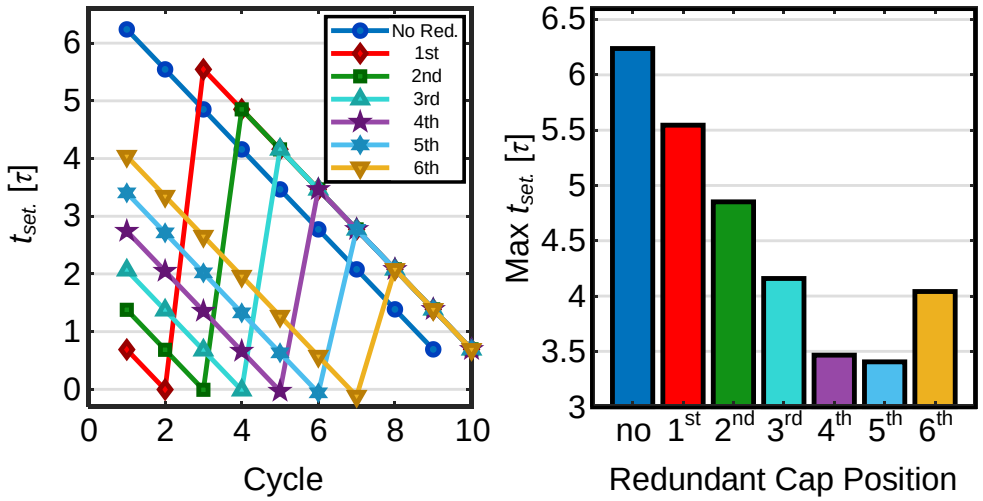


Figure 5.11. Average cycle number and normalized DAC switching power vs. window size.

without implementing kickback cancellation circuits, simultaneous calibration of both comparators is avoided. N_{cal} is set to 2 to calibrate both comparators in one calibration phase, so that the counter reset signal EN_{CAL}/TH in Fig. 5.7 can be shared to save power and area. In addition, the bypass window should enable the bypass of an even number of conversion cycles to retain an alternate operation of the two comparators and keep the logic simple. Based on these considerations, the window size is chosen as ±32 LSB in this implementation.

For the same window size, different redundancy range distributions pose different requirements on the DAC settling and thus affect the conversion rate of the ADC, For a window size of ±32 LSB, the conversion rate can be maximized by setting $[\Delta C_8, \Delta C_7, \Delta C_6, \Delta C_5]$ to $[20C_u, 8C_u, 3C_u, C_u]$. The settling time requirement for $\varepsilon \leq ½$ LSB of each cycle in a 10-bit ADC without redundancy and with a 1-bit binary-scaled



(a) (b)

Figure 5.12. (a) The settling time requirement of each cycle with and without redundancy. (b) The maximum settling time with different redundant cap positions.

redundancy [26] is depicted in Fig. 5.12(a), with the redundant capacitor position swept. As the clock delay in an asynchronous SAR ADC is set by the worst-case DAC settling time requirement, the maximum settling times among all cycles with different redundant capacitor positions are summarized in Fig. 5.12(b). The conversion rate boost with a 1-bit redundancy is maximized when the redundant capacitor is placed behind the 5th capacitor in a binary-scaled DAC. This decreases the maximum settling time to around

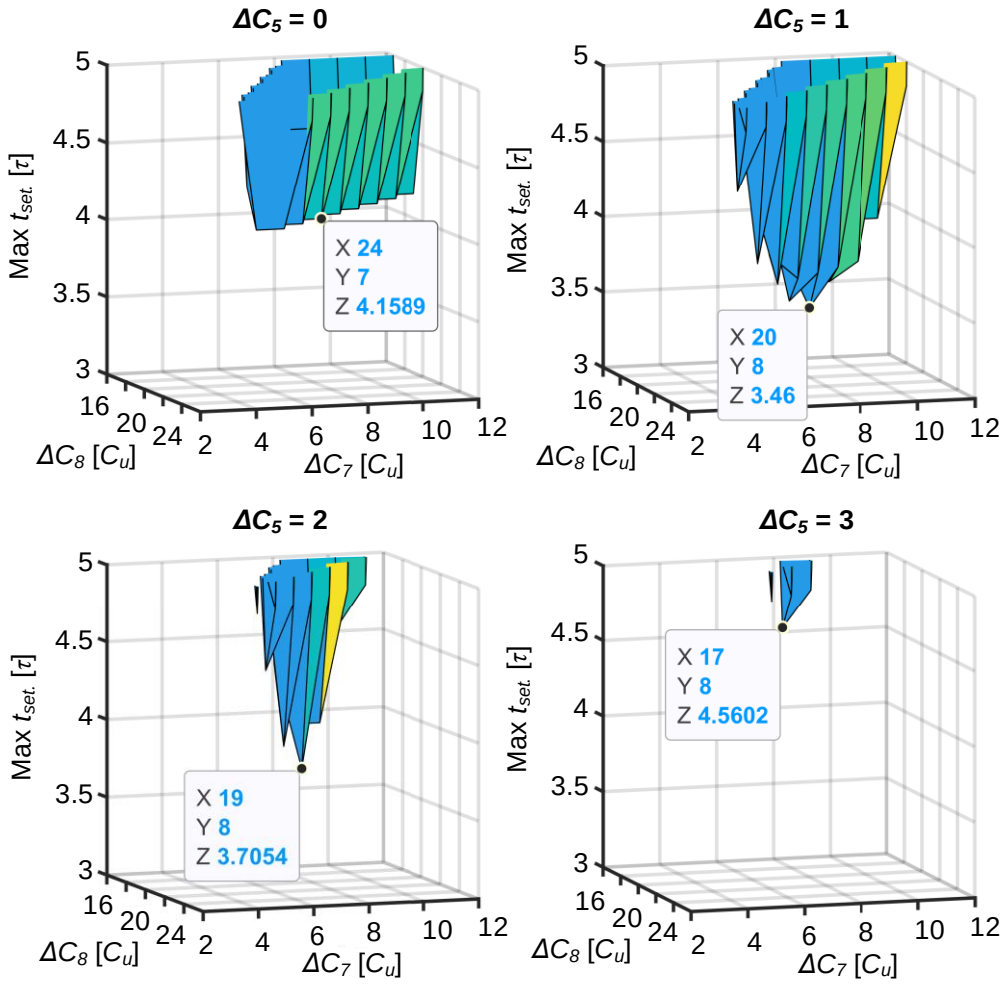


Figure 5.13. The maximum settling time with different capacitor distribution for win=32LSB.

3.4 τ. With the proposed bypass window, similar conversion rate enhancement can be achieved. Fig. 5.13 plots the maximum settling time of the conversion based on the proposed bypass window with the sizes of [ΔC_8, ΔC_7, ΔC_6, ΔC_5] swept. By setting [ΔC_8, ΔC_7, ΔC_6, ΔC_5] to [$20C_u$, $8C_u$, $3C_u$, C_u], the maximum settling time can be decreased to 3.46 τ, which is basically the same as can be achieved by the 1-bit binary-scaled redundancy. Hence, the bypass window can be implemented with almost no overhead as it provides the possibility for conversion phase truncation without degrading the conversion rate or burning extra power for input range detection. Due to layout considerations, we set [ΔC_8, ΔC_7, ΔC_6, ΔC_5] to [$20C_u$, $8C_u$, $4C_u$, 0] in the prototype ADC design, which results into a sub-optimal maximum settling time. However, this can be easily compensated by doubling the size of the DAC driver for the small-sized C_5. According to simulations, this leads to an 8.8% power saving per conversion and a 16% conversion rate boost as compared to a background-calibrated implementation [47, 58].

5.3 Proposed ADC Architecture

Fig. 5.14 shows the block and timing diagram of the overall ADC. The ADC consists of eight 300 MS/s 10-bit channels (SAR<7:0>). Both the input clock ($CK_{IN,P}$ and $CK_{IN,N}$) and the analog signal ($V_{IN,P}$ and $V_{IN,N}$) are on-chip terminated with a 100-Ohm resistor and distributed to each ADC channel with a tree structure to minimize the timing skew. The 8-phase low-frequency sampling clocks (CK_{S0-7}) are generated locally from the 2.4 GHz master clock (CK_{MST}) with a ring counter-based clock divider [59].

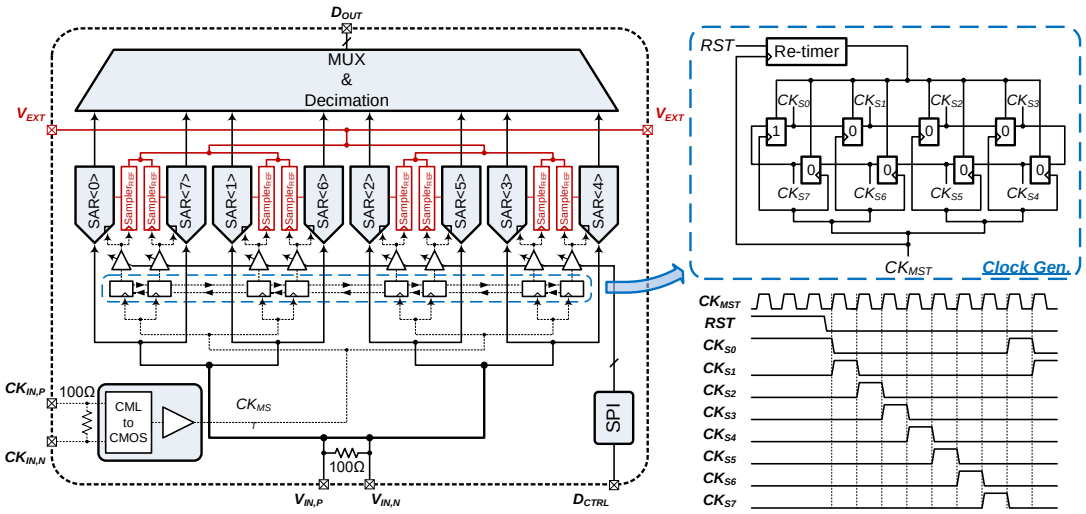


Figure 5.14. Block and timing diagram of the proposed ADC.

The external asynchronous reset signal (RST) is re-timed with CK_{MST} to guarantee a synchronous operation of the clock divider and set the initial state of each flip-flop. The clock divider is followed by a set of digitally controlled delay elements (DCDEs) for delay trimming. A dedicated clocked pre-charged reservoir provides and updates the reference voltage for each ADC channel on a periodic basis, avoiding inter-channel crosstalk caused by signal-dependent reference ripples. The ADC outputs are decimated and multiplexed before sending off chip through a set of buffers to facilitate data collection.

The block and timing diagram of each ADC channel is shown in Fig. 5.15. Each ADC channel is composed of a pair of bootstrapped sampling switches with feedthrough cancellation, a split-capacitor DAC tailored to enable the bypass window function, two alternate comparators, an array of memory cells, bypass switching logic, comparator clock generation and a clocked charge reservoir with a bootstrapped switch. During sampling phase, the analog input signal is sampled onto the DAC while the charge

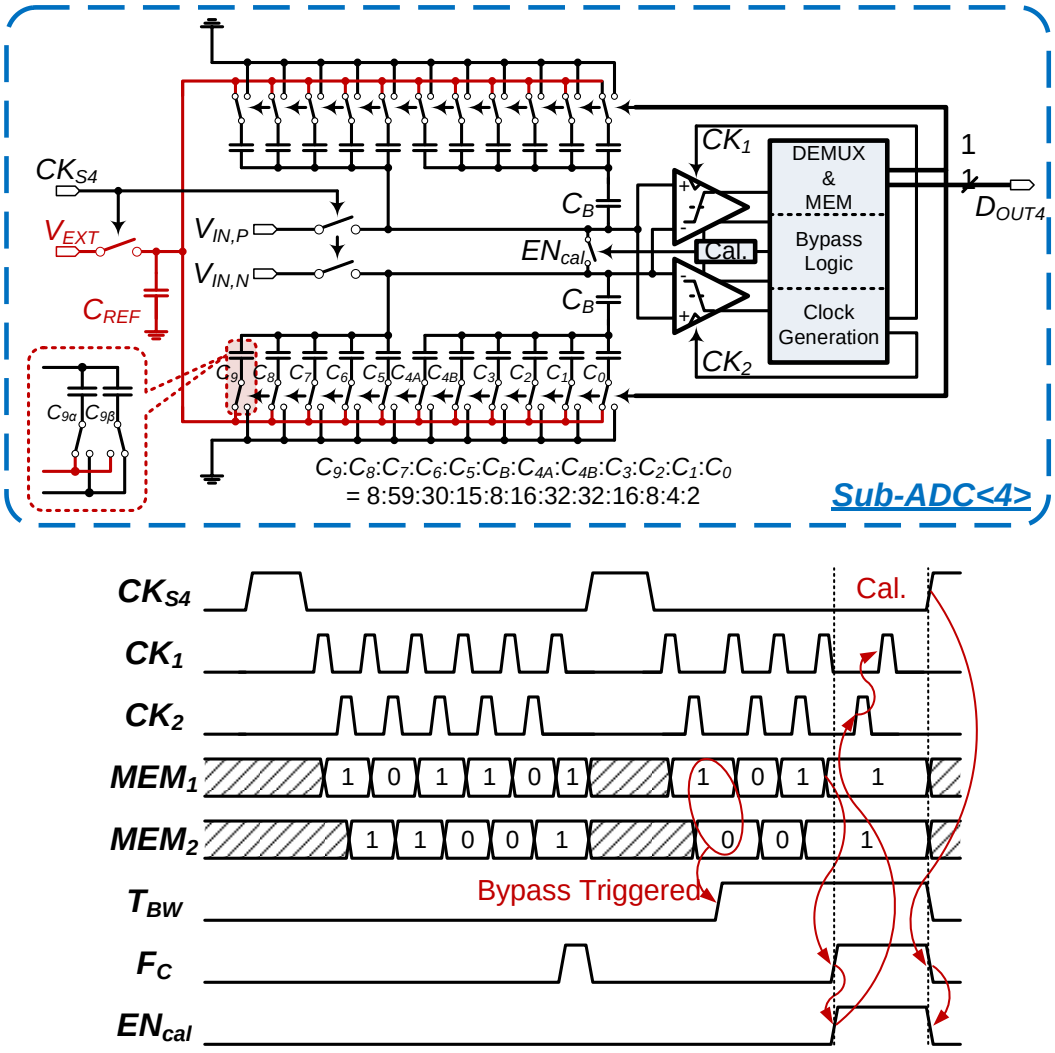


Figure 5.15. Block and timing diagram of a sub-ADC.

reservoir (C_{REF}) is replenished by the external reference voltage (V_{REF}). During conversion phase, the 10-bit quantization is completed in 11 cycles in normal cases. As the bypass switching is triggered, the bypass window triggering indicator (T_{BW}) will be asserted, the conversion procedure is then truncated to 7 cycles. Upon completion of the conversion procedure, the conversion-finished indicator (F_C) will be asserted until the next rising edge of the sampling clock. When both T_{BW} and F_C are active, a calibration phase is activated, where the offsets of the two comparators are calibrated in turn.

5.4 Implementation of Key Building Blocks

5.4.1 The Distributed Reference Charge Reservoir

A main limiting factor of the SNDR of SAR-based high-speed ADCs is the signal-dependent reference ripple caused by DAC switching. This can be more problematic in time-interleaved ADCs if a single reference supply is shared by all the ADC channels, since the reference ripple caused by the DAC switching of one channel can be coupled to the other channels in the form of inter-channel crosstalk. The most commonly adopted solution to the crosstalk is to use distributed reference buffers with a global bias, as shown in Fig. 5.16. However, as the reference voltage V_{REF} needs to

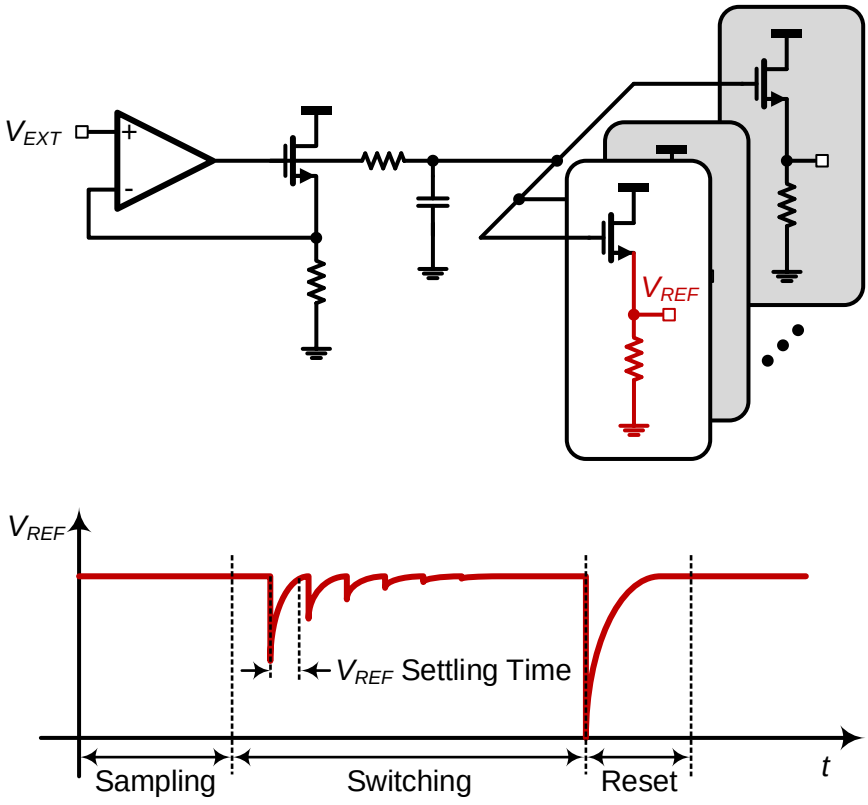


Figure 5.16. Conventional distributed reference buffer.

settle before the corresponding decision to yield a correct result or confine the error to a certain range, a small output impedance is desired, which dictates large static current. This inevitably introduces non-negligible power penalty [6, 8].

To address the settling errors caused by the crosstalk, a dedicated charge reservoir is employed to provide reference voltage for each ADC channel. This turns the global reference ripple into a local signal-dependent reference drop due to the charge drawn from the reservoir by the DAC. Though the reference drop during DAC reset $\Delta V_{REF,R}$ can be more severe than the voltage drop during conversion $\Delta V_{REF,S}$, it has little impact on the conversion accuracy as the reference is replenished before the next conversion. As such, only $\Delta V_{REF,S}$ is of interest. The signal dependency of the reference drop $\Delta V_{REF,S}$ can be analyzed quantitatively with a simplified DAC switching model [60] shown in Fig. 5.17. The reservoir C_{REF} is charged to $V_{REF,1}$ during sampling phase. In the meantime, the bottom plates of the α_{1p}, α_{0p}, α_{1n} and α_{0n} units are connected to the reservoir, while those of the β_{1p}, β_{0p}, β_{1n} and β_{0n} units are grounded. During conversion phase, only units α_{0p}, α_{0n}, β_{1p} and β_{1n} will be switched while units α_{1p}, α_{1n}, β_{0p} and β_{0n} remain unchanged. Due to the differential operation of the DAC, we can assume $\alpha_{1p} = \beta_{0n} = \alpha_1$, $\alpha_{0p} = \beta_{1n} = \alpha_0$, $\beta_{1p} = \alpha_{0n} = \beta_1$ and $\beta_{0p} = \alpha_{1n} = \beta_0$. The reference voltage drops to $V_{REF,2}$ at the end of the conversion. According to the law of charge conservation, we can write

$$\begin{aligned}&\left(V_{IN}-V_{REF,1}\right)\left(\alpha_1+\alpha_0\right)C_0+V_{IN}\left(\beta_1+\beta_0\right)C_0\\&=\left(V_R-V_{REF,2}\right)\left(\alpha_1+\beta_1\right)C_0+V_R\left(\alpha_0+\beta_0\right)C_0\end{aligned}, \tag{5.7}$$

$$\begin{aligned}&V_{REF,1}C_{REF}+\left(V_{REF,1}-V_{IN}\right)\alpha_1C_0-V_{IN}\beta_1C_0\\&=V_{REF,2}C_{REF}+\left(V_{REF,2}-V_R\right)\left(\alpha_1+\beta_1\right)C_0\end{aligned}. \tag{5.8}$$

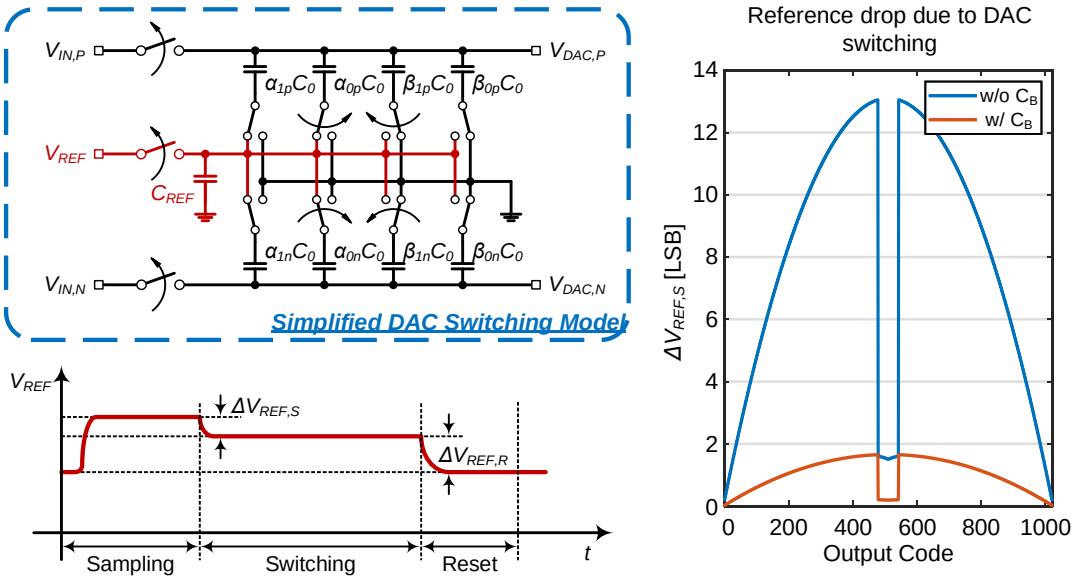


Figure 5.17. DAC switching model and signal-dependent reference drop of the charge reservoir.

where V_{IN} is the sampled input voltage and V_R is the residue. By solving (8) and (9), the reference drop during DAC switching can be derived as

$$\Delta V_{REF,S} = V_{REF,1} - V_{REF,2} = \frac{\frac{2(\alpha_1\alpha_0 + 2\alpha_0\beta_1 + \beta_1\beta_0)}{\alpha_1 + \alpha_0 + \beta_1 + \beta_0} \cdot C_0}{C_{REF} + \frac{2(\alpha_1 + \alpha_0)(\beta_1 + \beta_0)}{\alpha_1 + \alpha_0 + \beta_1 + \beta_0} \cdot C_0} \cdot V_{REF,1}. \quad (5.9)$$

In this work, the reservoir C_{REF}, which is approximately 80 pF in each ADC channel for sufficient suppression of the reference drop, is implemented with MOS capacitors for minimized area penalty. In addition, a bridge capacitor C_B is used to reduce the effective unit capacitance C_0 and thus the equivalent total capacitance of the DAC. A plot of the reference drop $\Delta V_{REF,S}$ versus the output code with and without C_B is given on the right-hand side of Fig. 5.17. The external reference voltage V_{EXT} is routed

to each local reservoir with a tree structure to maintain a well-matched RC constant among the channels.

5.4.2 Bypass Switching Logic

The implementation of the bypass switching logic is illustrated in Fig. 5.18. The outputs of the two comparators are demultiplexed and stored with an array of memory cells. The memory cells are turned on and connected to the comparators one by one with an asynchronously generated enable signal WR, so that each comparator is loaded by only one memory cell at a time to ease the driving pressure. The positive feedback provided by the cross-coupled NMOS transistors M_1 and M_2 accelerates the data transfer from the comparator to the DAC and decreases the critical-path delay. To minimize the delay imposed by the bypass logic, a replica of C_4 is introduced in the DAC. To show the difference, we denote the C_4 controlled by $D_{DAC,P,N}$<9:8> and by $D_{DAC,P,N}$<4> as C_{4A} ($C_{4\alpha,PA}$, $C_{4\beta,PA}$, $C_{4\alpha,NA}$ and $C_{4\beta,NA}$) and C_{4B} ($C_{4\alpha,PB}$, $C_{4\beta,PB}$, $C_{4\alpha,NB}$ and $C_{4\beta,NB}$), respectively. In normal operations, a total of 11 memory cells (MEM<10:0>) are enabled sequentially to receive the results from the 11 conversion cycles. And the outputs of MEM<10:1> ($D_{DAC,P,N}$<9:0>) are used to direct the switching of $C_{9\text{-}5}$, C_{4B} and $C_{3\text{-}0}$, respectively. In case MEM<10> and MEM<9> yield different results, which is sensed by a few standard gates, MEM<8> will remain off while MEM<4> is to be enabled instead. As the timing delay induced by the logic gates is not on the critical path, it has little influence on the ADC conversion rate as long as MEM<4> can be enabled before a valid decision of the comparator is generated. At the same time, the switching of C_8 is to be intercepted while the switching of C_{4A} will take place, directed

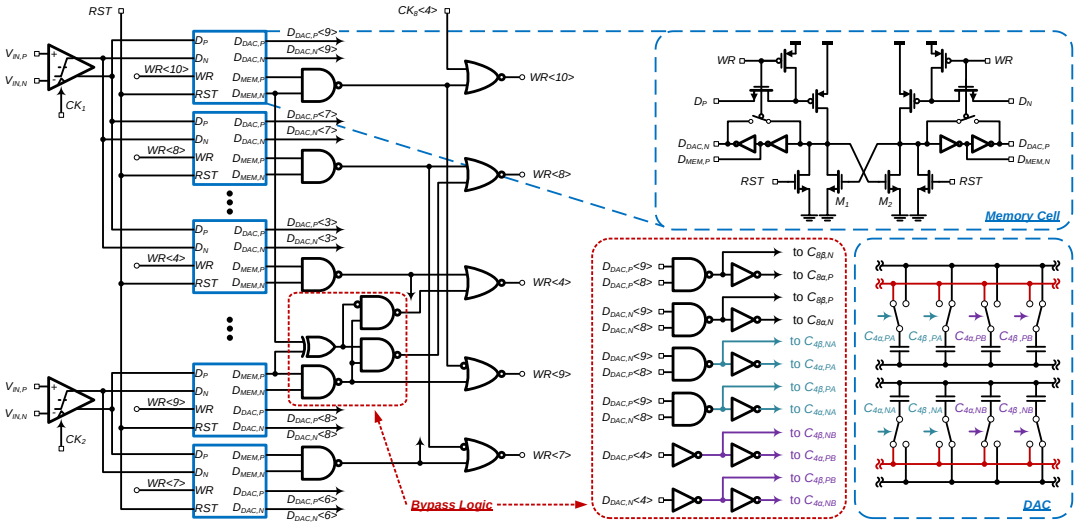


Figure 5.18. Implementation of the bypass switching logic.

by $D_{DAC,P,N}$<8>. Following this procedure, MEM<3:0> will be enabled in turn to complete data storage and switching control, whereas MEM<8:5> remain disabled for the rest of the conversion phase. Such an arrangement makes sure that one and only one of C_{4A} and C_{4B} is to be switched during each conversion and the situation where the C_4 has to be simultaneously controlled by $D_{DAC,P,N}$<8> and $D_{DAC,P,N}$<4> is avoided. This effectively minimizes the critical-path delay incurred by the extra logic. Simple as it is, the bypass switching logic guarantees that the skippable 4 cycles are plucked out of the conversion procedure as deemed possible and suturing the incision by seamlessly connecting the last 5 cycles with the first 2.

5.4.3 Comparator with Calibration Engine

The simplified schematic of the comparator with opportunistic adaptive offset calibration is shown in Fig. 5.19. The comparator is implemented as a StrongARM sense-amplifier latch for its fast decision. Transistor M_1 shorts the common source node

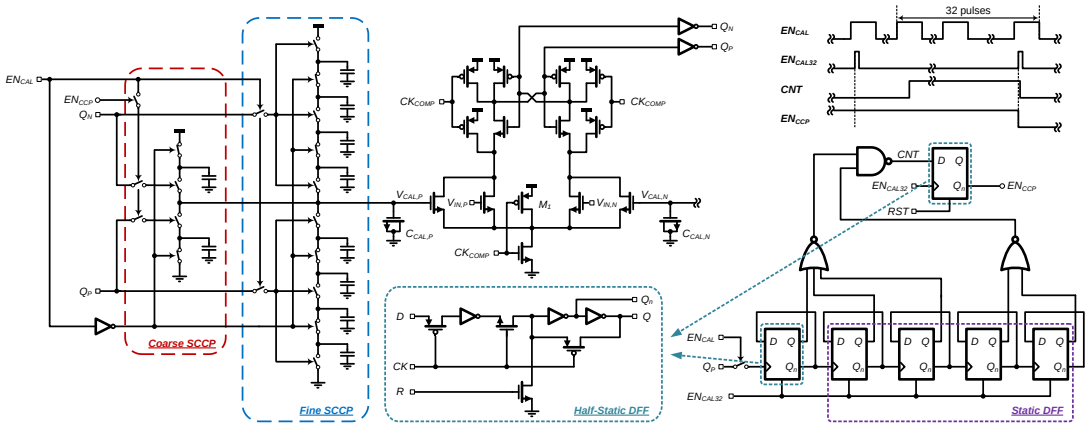


Figure 5.19. Comparator with opportunistic adaptive offset calibration.

to V_{DD} to present a constant parasitic capacitance during reset phase. An extra down-scaled input pair is introduced to compensate for the comparator offset. The voltages on the gates of the extra input pair $V_{CAL,P/N}$ are updated by two sets of SCCPs with different per-transfer charges, which in turn alters the comparator offset. Given a fixed integration capacitor $C_{CAL,P/N}$, the calibration step for each individual SCCP can be readily controlled by the number of intermediate voltages between power supplies and $V_{CAL,P/N}$ [58]. The fine SCCPs incorporate 4× intermediate voltage as compared to the coarse SCCPs, thus achieve a calibration step 4× smaller than that of the coarse SCCPs.

As mentioned in Section II-C, since both the two thresholds TH_C and TH_F for adaptive step control are set to 32, the counter and digital comparator can thus be shared to simplify the design and save the area. Apart from sharing the counter and comparison logic, a number of measures are taken to decrease the power consumption and layout area. First, as the number of positive and negative decisions N_P and N_N play interchangeable roles in determining the calibration step size, only NP is recorded while N_N is estimated by 32 – N_P. Second, though a 6-bit counter is theoretically required to

generate an output ranging from 0 to 32, a 5-bit counter is employed in this implementation since the states 0 and 32 can be combined into a single state, where the 5-bit output of the counter is 00000, indicating that all decisions in 32 calibration phases are either positive or negative. Third, the counter logic is asynchronous. This eliminates the need for extra logic gates, 5 D flip-flops (DFFs) are all it takes to construct the counter. Also, the power consumption can be reduced as not all DFFs are triggered for each per-bit update, which is in stark contrast to its synchronous counterpart. Fourth, the first DFF in the counter as well as the control signal latching DFF are carried out with a half-static structure to shrink the number of transistors. As these DFFs are driven by short pulses and thus the leakage when the clock CK is high can be neglected. However, the rest of the DFFs are clocked by slowly varying signals and need to be fully static to prevent errors due to leakage.

The timing diagram is shown in the upper right corner of Fig. 5.19. For each 32 calibration phases, a pulse will be generated on EN_{CAL32}, which latches the output of the comparison logic CNT to either enable or disable the coarse SCCP. Meanwhile, the counter is reset for a new round of recording.

Due to the leakage of the SCCPs, the RMS calibration noise after convergence can be correlated to the input amplitude and frequency, which indirectly determine the offset update frequency in this design. This issue is alleviated by employing small switches and large capacitors in SCCPs. Fig. 5.20 shows the differential V_{CAL} over different input amplitude and frequency. For a near-full-swing amplitude, an increase in the RMS algorithm noise can be observed if the sampled input is slowly varying. However, as long as the sampled input is relatively busy, the algorithm noise shows

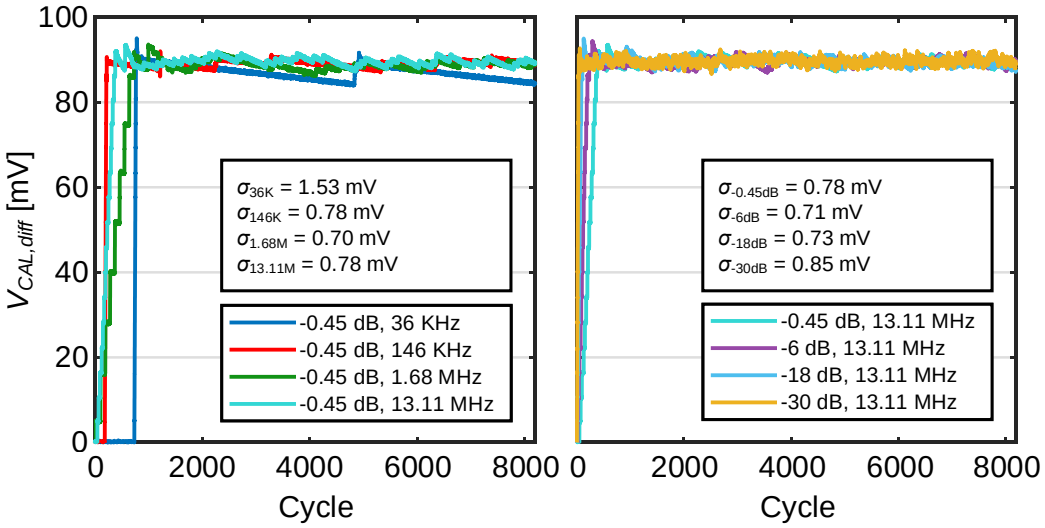


Figure 5.20. Differential calibration voltage V_{CAL} with different input amplitude and frequency.

little dependence on the input amplitudes. The calibration engine introduces a negligible power overhead on the order of tens of μW and a typical IRN of approximately 0.16 mV.

Thanks to the afore-mentioned design measures, the calibration engine occupies approximately the same area as the StrongARM latch and can be easily embedded into the modular design of the comparator. In addition, the power consumption introduced by the adaptive control logic is negligible due to the low operation speed and simple configuration.

5.5 Measurement Results

The ADC has been fabricated in a one-poly eight-metal (1P8M) 28 nm FDSOI process with a core area of 217 µm × 672 µm (including the area of the reference charge reservoir). The chip micrograph and zoomed-in layout view of the ADC core are shown in Fig. 5.21. The total single-ended sampling capacitance is around 360 fF, where the DAC takes approximately 70%.

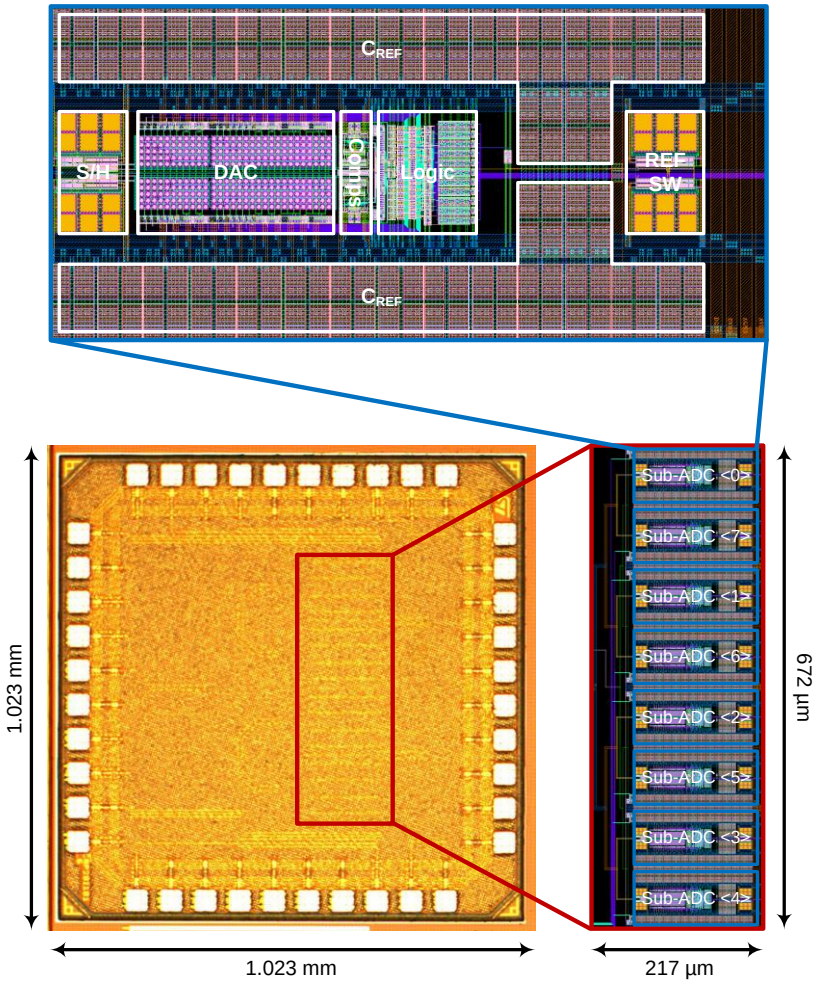


Figure 5.21. Chip micrograph and layout.

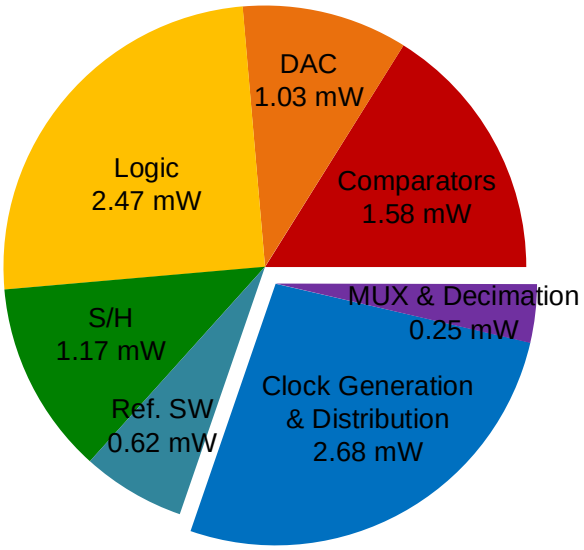


Figure 5.22. Power breakdown at 2.4 GS/s.

The ADC impairments such as inter-channel offset, gain and timing mismatch are calibrated off chip. Before the timing mismatch correction, the offset and gain mismatches are calibrated at low frequency by extracting and equalizing the estimated offset and gain of each ADC channel [61]. The timing skew compensation is performed by trimming the DCDEs at a 2.4-GHz input, where the skew spurs are the most obvious. The DCDE settings are found based on sine-fitting of the ADC output data [62], which are internally decimated by a factor of 49 to facilitate data transmission and acquisition.

The power breakdown at 2.4 GS/s and 0.9 V is shown in Fig. 5.22. The ADC consumes a total of 9.8 mW, where 2.93 mW (2.68 mW for clock generation & distribution and 0.25 mW for MUX & decimation) is contributed by the interleaving overhead. The comparators including the opportunistic adaptive calibration engine dissipate 1.58 mW. The bootstrapped reference refresh switches consume merely 0.62 mW, which amounts to around 6% of the total power.

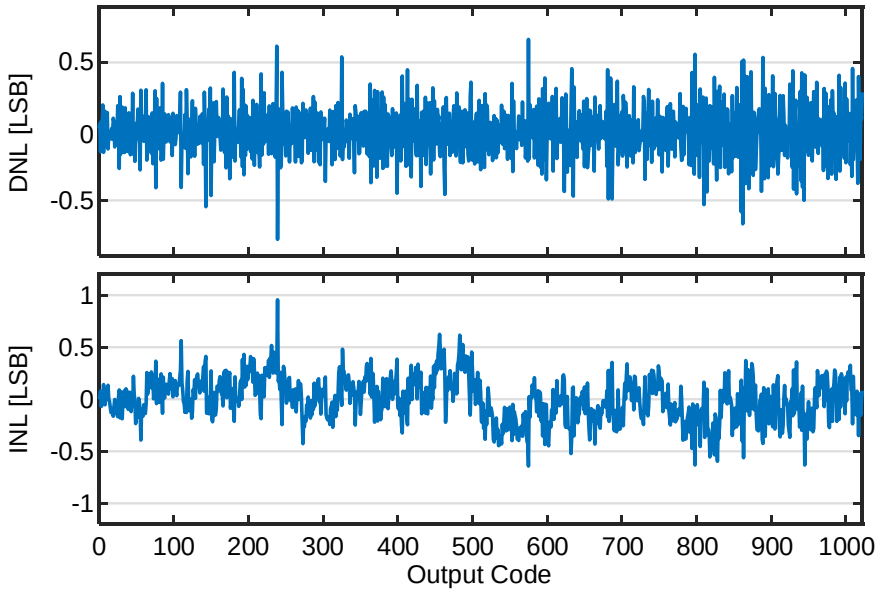


Figure 5.23. Measured differential and integral non-linearities.

The static performance of the ADC was measured by applying an 8.42-MHz input signal with an amplitude slightly larger than the full swing. Fig. 5.23 depicts the measured differential nonlinearity (DNL) and integral nonlinearity (INL) performances of the ADC. The maximum DNL and INL are -0.78/+0.67 LSB and -0.64/+0.96 LSB, respectively.

Fig. 5.24 shows the FFT plots with an input frequency of around 832.29 MHz before and after calibration. The measured SNDR and SFDR after calibration are 51.61 dB and 65.99 dB, respectively. The resultant ENOB is 8.28 bits.

Fig. 5.25 shows the input frequency sweep before and after the calibration. The SNDR at low frequency is around 53 dB, limited mainly by the comparator noise. At Nyquist frequency, the SNDR degrades to 49.02 dB due mainly to the residual interleaving spurs and harmonics. The corresponding Walden FOM at low and Nyquist

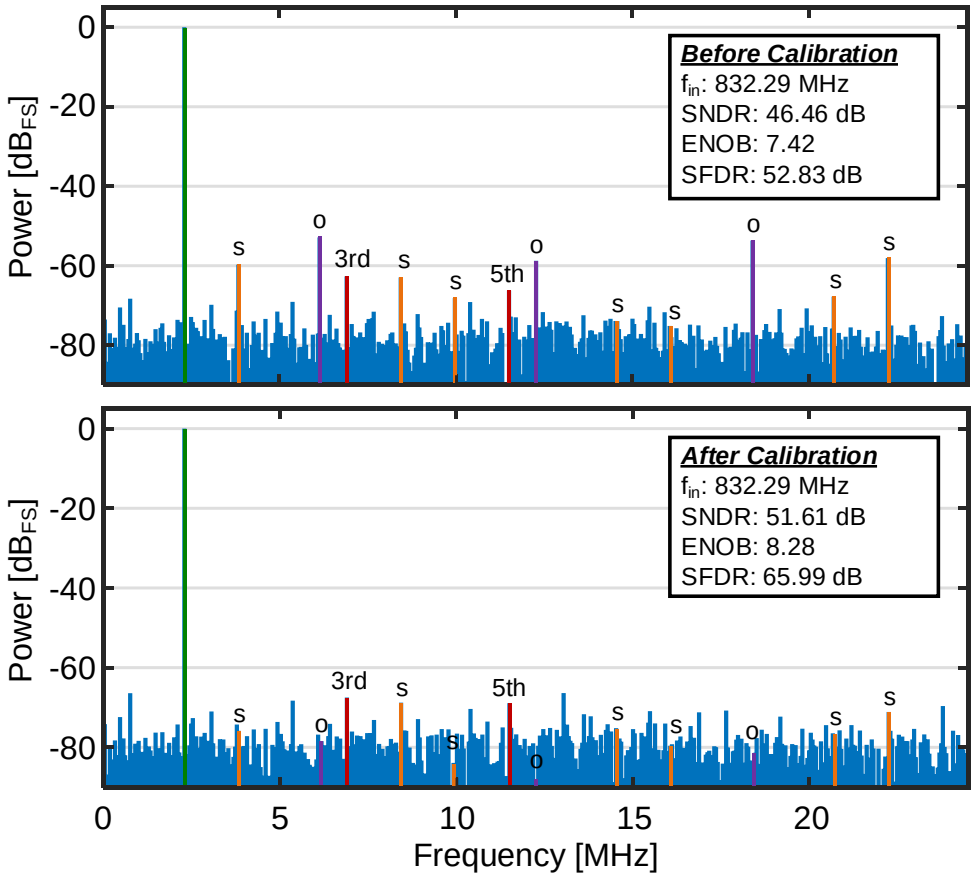


Figure 5.24. Measured ADC output spectrum without and with calibration (49× decimated).

frequency are 11.6 and 17.7 fJ/conversion-step, respectively. And the resultant Schreier FOM at low and Nyquist frequency are 163.5 and 159.9 dB, respectively. The SNDR stays above 48 dB up to 2.4-GHz input frequency.

Fig. 5.26 shows the measured SNDR and SFDR versus the input amplitude with a 51-MHz input. The measured dynamic range is 52.1 dB. Fig. 5.27 shows the measured SNDR with a low-frequency input over different supply and input common-mode voltages.

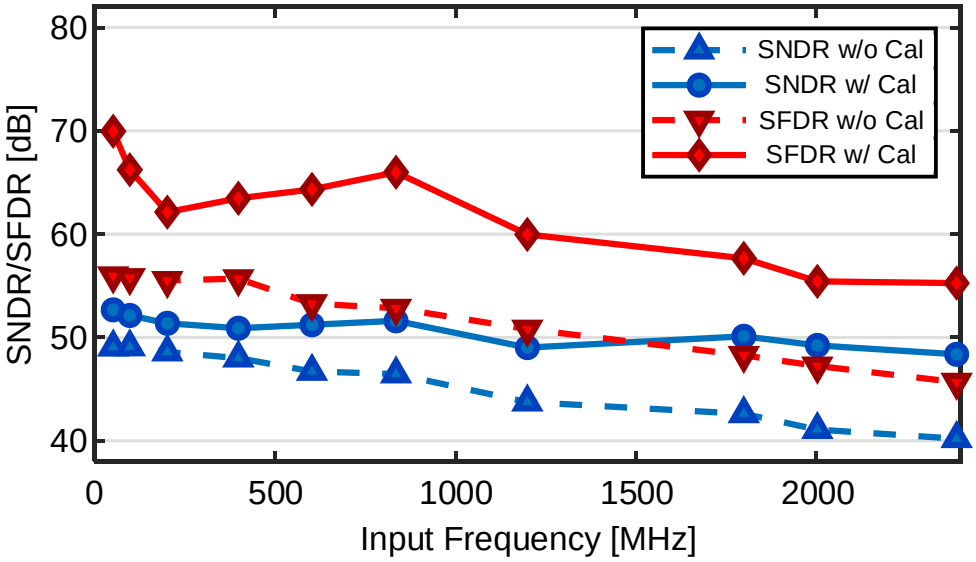


Figure 5.25. Measure SNDR and SFDR versus input frequency.

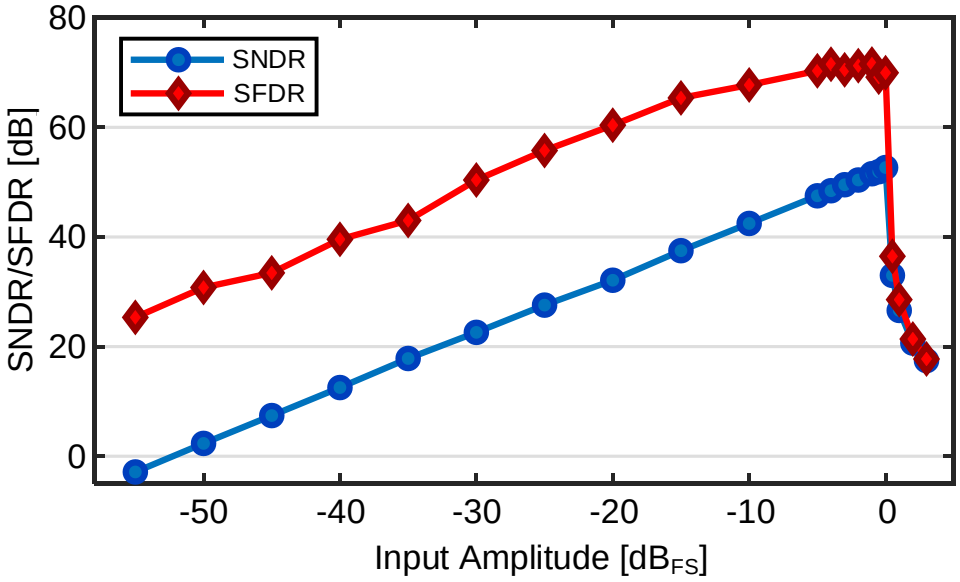


Figure 5.26. Measure SNDR and SFDR versus input amplitude.

Table 5.1 summarizes the ADC performance and compares it against recently published TI-SAR ADCs with comparable sampling rates and resolutions. Fig. 5.28

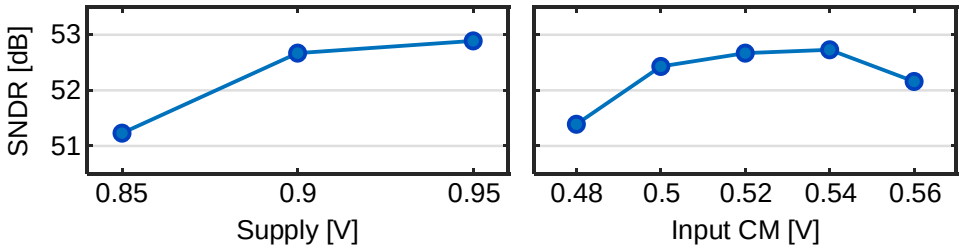


Figure 5.27. Measured SNDR with low-frequency input (~50 MHz) over different supply and input common-mode.

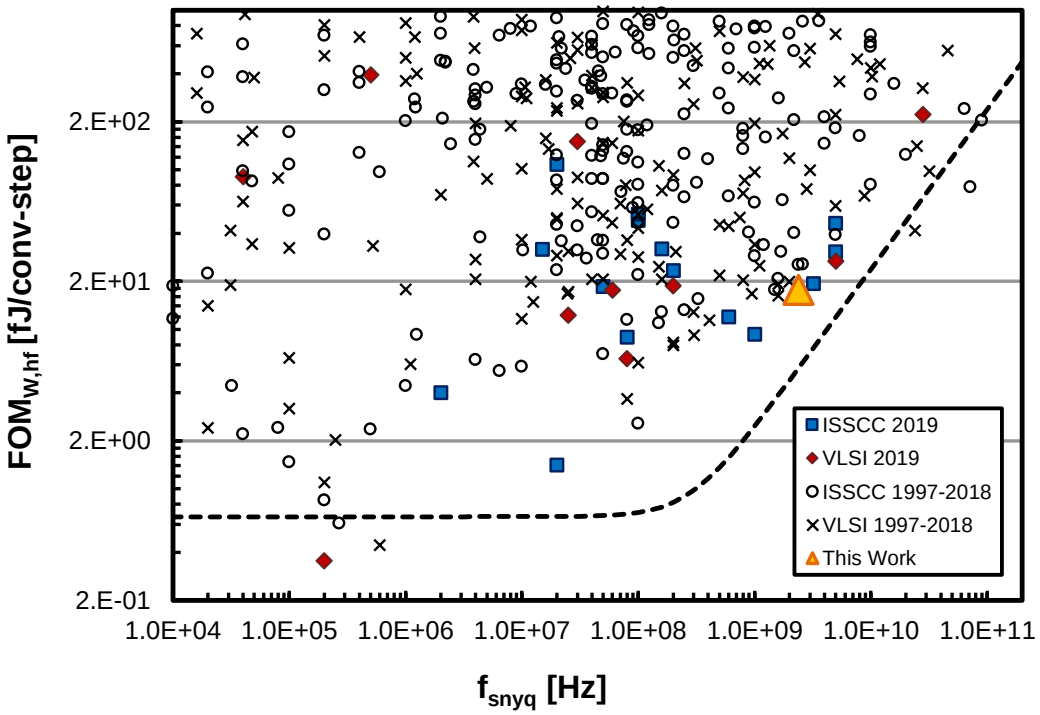


Figure 5.28. Comparison of Walden FOM with ADCs presented at ISSCC and VLSI between 1997 and 2019.

plots the Walden FOM of all ADCs presented at ISSCC and VLSI between 1997 and 2019 [1]. With a Nyquist Walden FOM at 2.4 GS/s of 17.7 fJ/conv.-s., the proposed

Table 5.1. Performance Summary and Comparison

Specifications	[6]	[7]	[8]	[9]	This work
Architecture	TI-SAR	TI-SAR	TI-SAR	TI-SAR	TI-SAR
# of Channels	12	16	16	4	8
Technology (nm)	28	40	28-FDSOI	16	28 FDSOI
Resolution (bits)	10	10	11.2	10	10
Sample Rate (GS/s)	5	2.6	5	2	2.4
Supply Voltage (V)	1.0	1.1	1.8/1.0/0.8	0.85/1.5	0.9
$SNDR_{@Nyquist}$ (dB)	42	50.6	51.7	50.1	49.02
$SFDR_{@Nyquist}$ (dB)	54.5	57.8	59.2	56	59.97
$ENOB_{@Nyquist}$ (bits)	6.68	8.11	8.29	8.03	7.85
Power (mW)	76	18.4	150	10.4	9.8
FOM_W (fJ/conv.-s.)	165	25.6	95.5	20	17.7
Area (mm^2)	0.57	0.825	0.184	0.014	0.145

ADC achieves the best Walden FOM among ADCs with sampling rates of higher than 2 GS/s.

CHAPTER VI

CONCLUSION AND FUTURE DIRECTIONS

6.1 Conclusion

High-speed analog-to-digital converters (ADCs) with medium-to-high resolutions find wide application in test equipment, wireline transceivers and wireless communication systems. Yet, implementations of the afore-mentioned conversion systems with utmost power efficiency turn out to be no easy tasks. In order to push the leading edge of the ADC efficiency, a total of three works are presented in this dissertation, each with a unique architecture proposed to achieve a better tradeoff among power, accuracy and speed.

A partially interleaved 1 GS/s 8-bit two-step SAR ADC is presented as the first work. A fast noise reduction technique is proposed to increase the power efficiency. A modified StrongARM latch is adopted for further noise suppression. The gain error and comparator offset are tackled by background calibrations. Fabricated in a 28 nm FDSOI technology, the ADC achieves a SNDR of 46.65 dB at Nyquist with a sampling rate of 1 GS/s, while consuming 2.1 mW from a 1.1 V supply. This translates into a Walden FOM of 12.01 fJ/conv.-step.

The second work introduces a double-rate comparator architecture that is used in pair with a half-rate clock generation mechanism in a SAR ADC for sampling rate enhancement. In addition, the proposed techniques greatly reduce the design complexity

and improve the power efficiency by 20%-30%. The effectiveness of the proposed design concept is verified with a 10-bit 550-MS/s prototype single-channel SAR ADC fabricated in a 28-nm FDSOI process.

The third work is a power-efficient time-interleaved SAR ADC. Alternate comparators are employed for each ADC channel for speed enhancement. A distributed reference charge reservoir is adopted to prevent the inter-channel crosstalk at a low cost. A bypass window, introduced by the customized capacitive DAC, is applied to the SAR-based conversion to give rise to bit cycle skipping for qualified input. The redundancy generated along with the bypass window achieves similar effect of conversion acceleration to the conventional 1-bit binary-scaled redundancy, resulting into extremely low overhead for the bypass window. In addition, the selective bit cycle truncation induced by the bypass window breaks the uniformity of the length of conversion phase, which provides the time slot for opportunistic offset calibration. As such, the non-uniform offsets of the two comparators are compensated without degrading the sampling rate. An adaptive calibration engine is proposed to compensate for the reduced convergence rate due to the less-frequently triggered calibration phase.

6.2 Future Directions

The proposed fast noise reduction technique requires the knowledge of ADC noise for design optimizations. However, ADC noise is a topic rarely explored. Though the noise performance of a single comparator or amplifier has been well studied and documented, the exact effect of the comparator or amplifier noise on the overall ADC

system remains a mystery to a lot of designers and researchers. To date, the most widely adopted method for noise analysis is through extensive simulations, which can be rather inefficient in terms of time. Thus, a well-developed model for fast analysis of the ADC noise is desired. Specifically, the comparator noise does not refer directly to the overall input noise of a SAR ADC as intuition suggests. Instead, it is attenuated by a factor dependent upon the comparator noise itself, causing a pessimistic estimation of the ADC noise in most cases. In addition, the bit-wise noise contribution of the comparators shows a strong dependence on the location of the bit cycle as well as the redundancy distribution. It is therefore desirable to derive a closed-form expression of the ADC noise as a function of the bit-wise comparator noise.

TI-SAR ADCs achieve GS/s speed with outstanding power efficiency thanks to the speed boosting techniques. However, the effective resolutions are confined to less than 8.5 bits for lack of amplification mechanism. Brute-force SNR enhancement by means of design up-scaling severely degrades the power efficiency. Thus it would promising to explore the possibility of architectures with both high speed and high accuracy by combining the speed boosting techniques with modern amplification solutions.

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