Design and Fabrication of a Controller for a Digital Phase Locked Loop

A Dissertation

Presented to

the Faculty of the Department of Electrical and Computer Engineering

University of Houston

In Partial Fulfillment

of the Requirements for the Degree

Doctor of Philosophy

in Electrical Engineering

by

Donald Troha

December 2012

Design and Fabrication of a Controller for a Digital Phase Locked Loop

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Abstract

A controller for an all digital phase locked loop which operates by pulse addition and removal is investigated. Being a first order system, the digital phase locked loop is more limited in regard to parameter controls than its second order analog counterpart. A loop with a fast lock time generally has poor phase/frequency accuracy, while a loop programmed for high accuracy will have slow lock time. Given that the digital phase locked loop is digitally programmable, a set of parameters may be selected which will minimize the lock time of the loop. Once the loop is locked, the parameters may be changed to alter the loop bandwidth and increase the loop accuracy. A controller circuit has been designed to adjust loop parameters in such a manner thereby optimizing loop performance.

The exclusive-OR phase detector which is commonly used with the pulse addition/removal type digital phase locked loop has a phase lock range of plus or minus a quarter of a cycle. This work investigates the loop response to an incoming signal which is outside of the phase lock range of phase detector and inside the frequency lock range of the loop. A sub-circuit is proposed to improve the lock time of the loop when it encounters an incoming signal with these characteristics.

The proposed circuits were designed using integrated circuit layout tools and submitted to a semiconductor manufacturer for fabrication. The controller concept and results of simulations and prototype experiments are presented.

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Chapter 1 Introduction

The digital phase locked loop has advantages as well as disadvantages in comparison to its analog counterpart. The ability to program the loop digitally and dynamically through a controller provides the opportunity to overcome some of the shortcomings of the digital phase locked loop. Standard CMOS design cells and fabrication processes simplify the design process so that digital phase locked loops can be designed and fabricated without the critical resistor and capacitor parameter tuning requirements of analog phase locked loops.

A number of digital phase locked loop styles are described in the literature. The controller discussed in this report is designed to operate in conjunction with the type of digital phase locked loop designed by Draper Labs as described in references [1] and [2]. This variety of DPLL is also designated as an all digital phase locked loop (ADPLL) in the references and operated on the concept of pulse addition and removal. Due to the fact that the design consists entirely of digital components, it lends itself to dynamic adjustment of loop parameters. Since the loop is a first order system, the loop gain is the only design parameter available for establishment of loop performance [3]. A high gain is desired for good tracking which results in high bandwidth and fast lock time. However the locking accuracy will be low and the loop will not be able to distinguish between two signals with a small frequency separation. Using the programmable features of the DPLL, we can dynamically switch between fast-lock/wide-bandwidth and slow-lock/narrow-bandwidth.

The exclusive-or (EXOR) type phase detector has advantages over the edge-controlled phase detector (e.g., noise immunity). However, the lock range of the DPLL with an EXOR phase detector is only a half-cycle. If the initial condition of the loop is outside the half-cycle lock range, the loop may still lock, but it will transition slowly through this non-lock region causing excessive lock time.

The goal of this project is to design a controller to address these two issues, and to layout and fabricate the controller on a chip. The circuit is to be designed and simulated using Cadence design tools, and fabricated on a 0.5 micron process through Mosis. Two chips are needed: one for the DPLL and associated counters and registers and a second chip for the controller.

1.1 Organization

Previous work is discussed in Chapter 2 describing two alternative methods of controlling parameters for an all digital phase locked loop. Chapter 3 describes the concept of the first order DPLL which operates by pulse addition and removal. An analogy to the second order analog loop is presented. In Chapter 4 we review theoretical performance of the DPLL versus programmed loop parameters and look at performance trade-offs.

A key performance parameter for the phase locked loop is the time it takes to achieve a locked state. Chapter 5 discusses how lock time is measured, Chapter 6 describes the controller state machine for dynamic modification of loop parameters, and Chapter 7 analyzes the DPLL step function response to a

change in phase or frequency. The phase lock range of the EXOR phase detector has a significant effect on the lock time of the loop and this is described in Chapter 8.

Chapter 9 summarizes the design and layout of the controller circuit and Chapter 10 reviews the results of the fabricated circuits. Since the fabricated circuits did not operate as expected, a prototype of the controller was assembled and tested on a breadboard and results are presented in Chapter 11. Chapter 12 compares actual circuit results with predicted results from first order loop equations. Discussion, summary, and conclusions are presented in Chapter 13 and Chapter 14.

Chapter 2 Previous Work

2.1 Processor Control of Loop Parameters

It was proposed in reference [4] that the parameters of the DPLL could be controlled by a processor as shown in Figure 2.1. Phase data and lock conditions are retrieved from the loop and input into a microprocessor. A program is written for the processor to crunch the data and adjust loop parameters accordingly. For the simple case of switching between two or three sets of loop parameters, it is proposed here that this could be handled by a state machine and some logic circuitry instead.

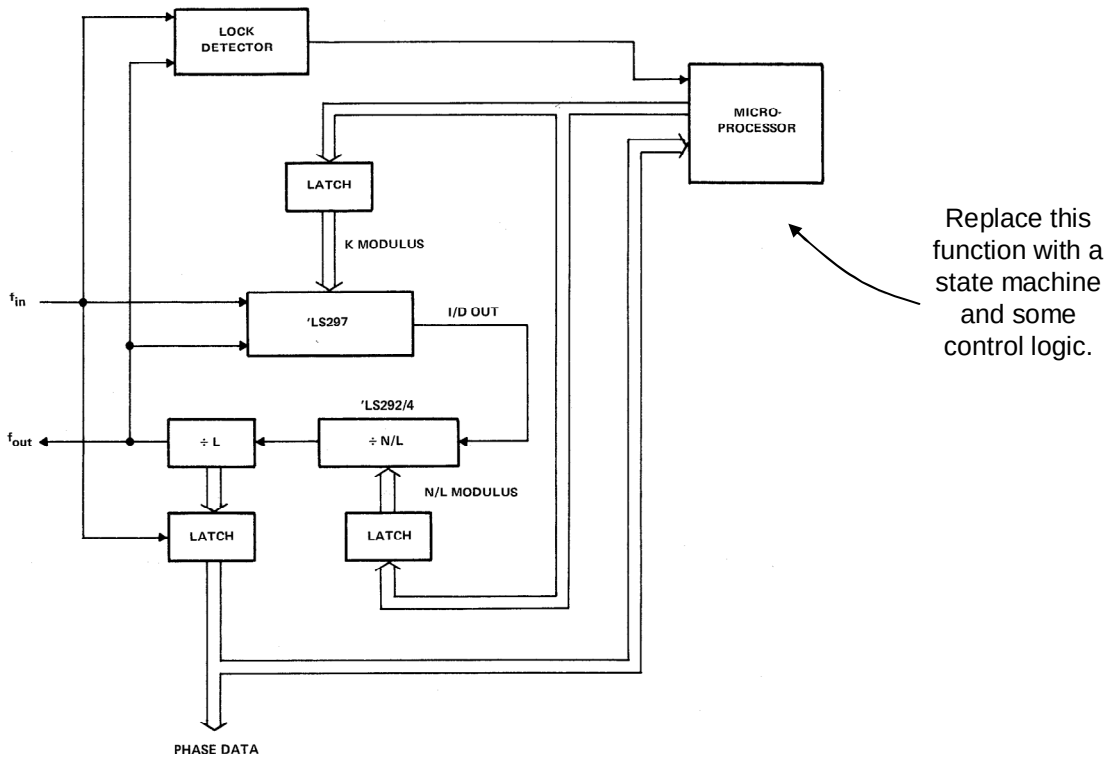
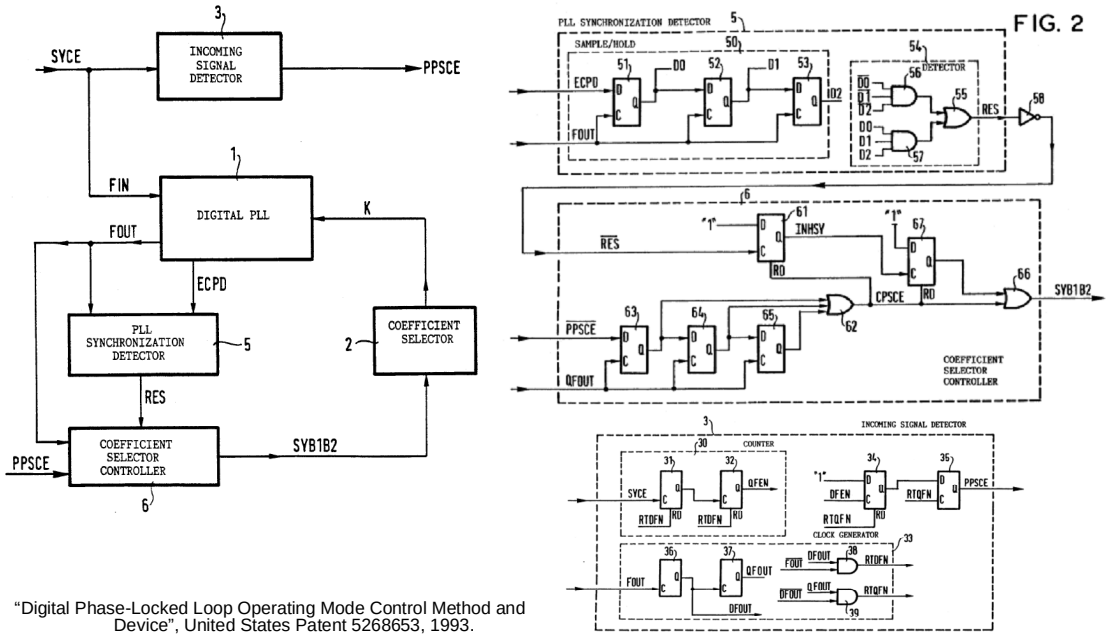


Figure 2.1 Previous work – Loop parameters controlled by a processor [4].

2.2 Lock Detection by Consecutive Samples

In reference [5], a different method was proposed for controlling the loop parameters as shown in Figure 2.2. In this case a series of three consecutive samples of the phase detector output is used detect a lock condition. An incoming signal detector detects the presence or absence of an input signal f_{in}. Outputs from the incoming signal detector and sync detector are then supplied to a coefficient selector circuit which switches between the two sets of loop parameters. The coefficient selector circuit looks for three consecutive samples of the "signal present" signal to select one coefficient. Detection of synchronization (lock) condition sends a reset signal to the coefficient selector circuit which causes the selection of the other coefficient.



"Digital Phase-Locked Loop Operating Mode Control Method and Device", United States Patent 5268653, 1993.

FIG. 2

Figure 2.2 Previous work – Sync detector and coefficient selector [5].

This implementation relies on the use of an edge triggered phase detector (ECPD) and relies on the jitter effect of frequency adjustment to detect a locked

condition. This jitter effect method of lock detection works best in applications where the incoming signal frequency is equal to the center frequency ($f_{in}=f_c$).

The controller described herein differs from either of these two previous methods. Phase data is read from the loop feedback counter and compared to an expected phase word to determine if the loop is in a locked or unlocked condition. The state machine steps through a predetermined set of loop conditions. This is described in more detail in Chapter 5 and Chapter 6. The use of an EXOR phase detector instead of the ECPD phase detector means the input and output signals will lock up ninety degrees out of phase instead of 180 degrees out of phase. The Figure 2.1 method relies on the ECPD phase detector implementation for proper operation.

Chapter 3 DPLL Concept

The functional block diagram of the all digital phase locked loop which operates by pulse addition and removal is shown in Figure 3.1.

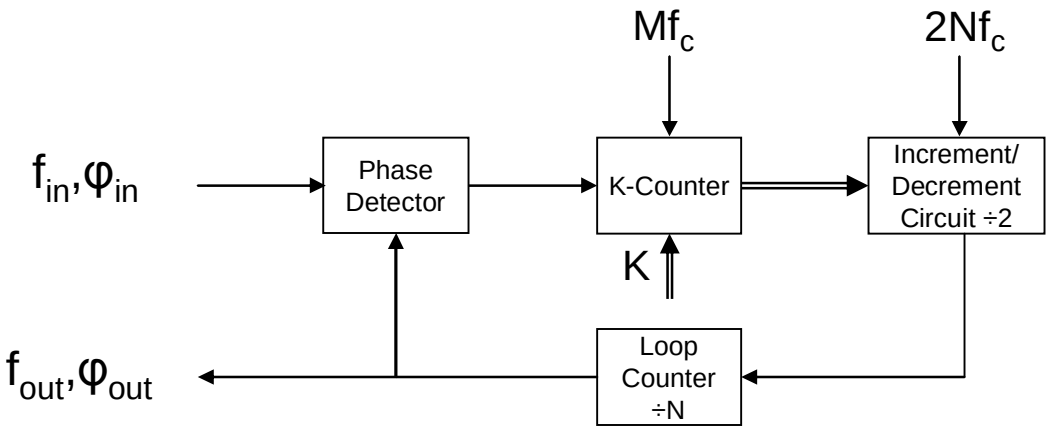


Figure 3.1 Basic Digital Phase Locked Loop [4].

The loop consists of a phase detector, a K-counter, an increment/decrement (I/D) circuit, and a divide by N (÷N) loop counter. The K-counter and I/D circuit take the place of the voltage controlled oscillator of the traditional analog phase locked loop (APLL). Two external clocks must be supplied to the circuit: K-clock (Mf_c) and I/D clock ($2Nf_c$), where M is an arbitrary constant, N is the modulus of the loop counter, and f_c is the center frequency of the loop. The two clocks may or may not be supplied from the same source. The input signal f_{in}/φ_{in} is the signal to be locked upon and f_{out}/φ_{out} is the regenerated signal which is phase-compared to the original input signal. Due to

the digital nature of this circuit, there will be an inherent amount of jitter on the regenerated signal f_{out}.

For comparison, a block diagram of an analog PLL is shown in Figure 3.2. Note the filter in place of the K-counter and the voltage controlled oscillator in place of the increment/decrement circuit.

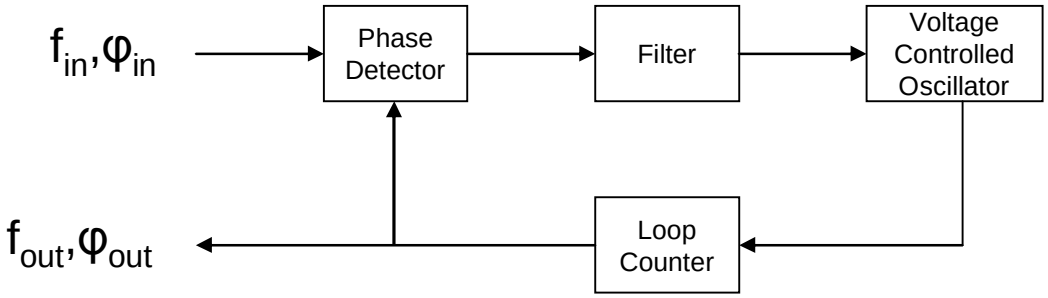


Figure 3.2 Analog Phase Locked Loop.

The step responses of a second order analog loop and a first order digital loop are shown for comparison in Figure 3.3. A second order loop step response is characterized by the loop natural frequency ω_n and damping factor ζ. The first

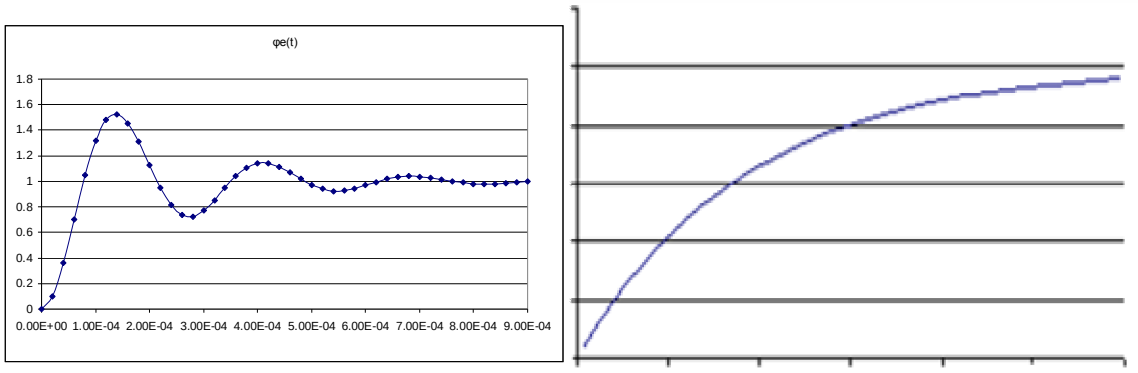


Figure 3.3 Step function response.
Second order damped sinusoid response (left) and first order exponential response (right).

order loop has an exponential step response controlled only by time constant τ (tau).

Having only one adjustable variable limits our ability to optimize loop performance in the case of the DPLL. The use of a controller can help us overcome this limitation through dynamic parameter control.

Chapter 4 Loop Performance versus K

The gain of the digital phase locked loop is controlled by the modulus, K, of the K-counter. Table 4.1 lists lock time, bandwidth, lock range, and phase/freq accuracy versus K for a loop with a given set of parameters. Plots in Figure 4.1 through Figure 4.4 illustrate graphically the data from the chart. Figure 4.1 shows that the lock time increases with K. Figure 4.2 shows that the bandwidth decreases with K. Figure 4.3 shows that the lock range decreases with K. Figure 4.4 shows that the phase/frequency accuracy improves (becomes smaller) with increasing K.

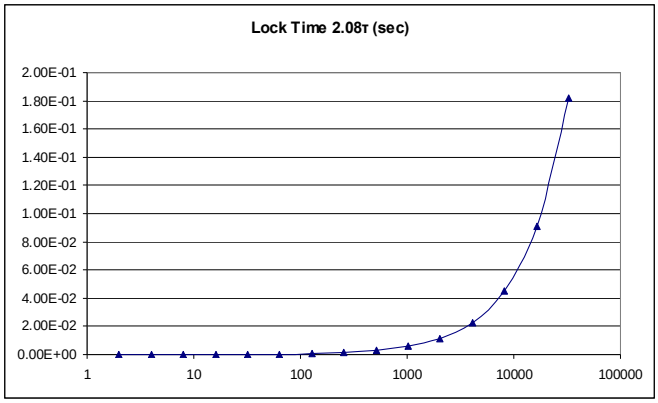


Figure 4.1 Lock time versus K.

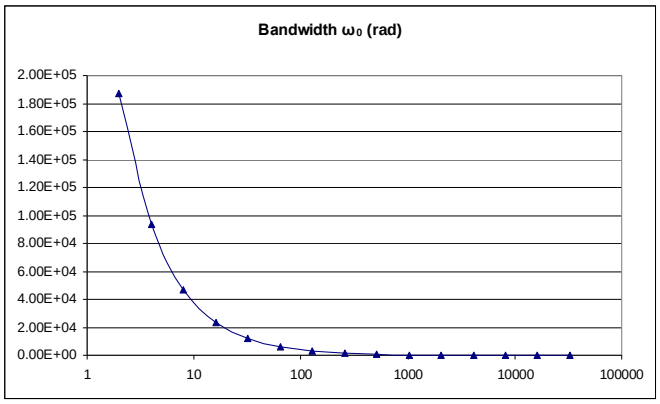


Figure 4.2 Bandwidth versus K.

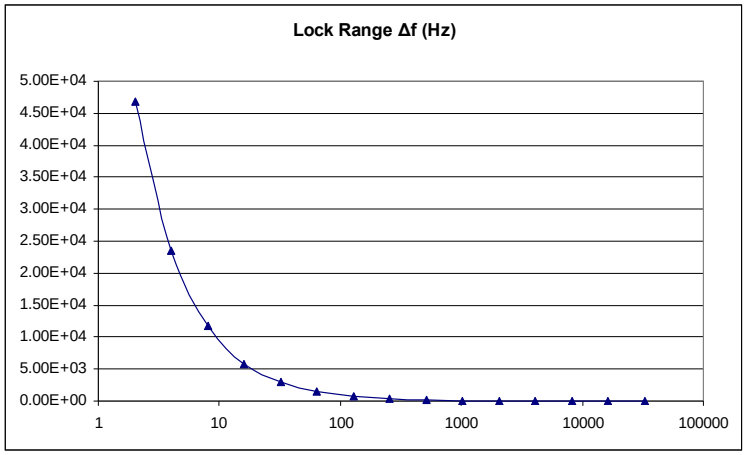


Figure 4.3 Lock range versus K.

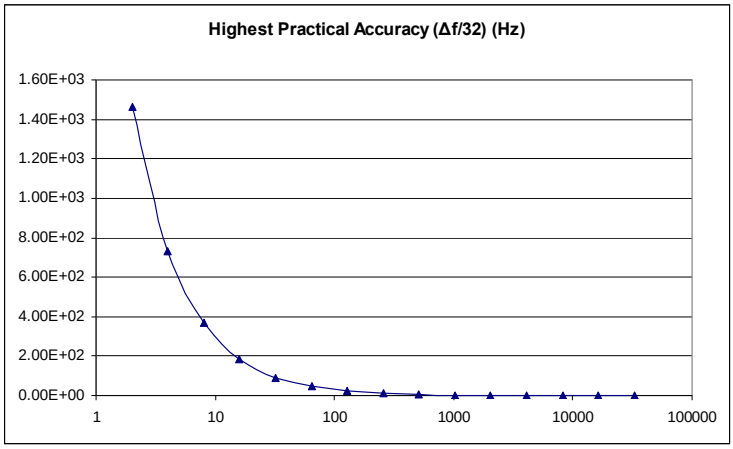


Figure 4.4 Phase/Freq accuracy versus K.

From Figure 4.1 we can see that a low number for the K modulus will give us a fast lock time. Figure 4.4 indicates that a high number is needed for the K modulus for better accuracy. Ideally we would like to have both fast lock time and high accuracy. So a circuit is proposed which will program a low K modulus for fast locking, then switch to a high K number after locking to facilitate accurate decoding of phase or frequency information.

Table 4.1 Tradeoffs - Lock time, Bandwidth, Phase Accuracy.

K bits	K	τ	Lock Time 2.08τ	Bandwidth $\omega_0=1/\tau$	Lock range Δf	Highest theoretical accuracy Hz (1/256 cy)	Highest practical accuracy Hz (1/32 cy)
0001	2	5.33E-06	11.09E-06	187.50E+03	46.88E+03	183.11E+00	1.46E+03
0010	4	10.67E-06	22.19E-06	93.75E+03	23.44E+03	91.55E+00	732.42E+00
0011	8	21.33E-06	44.37E-06	46.88E+03	11.72E+03	45.78E+00	366.21E+00
0100	16	42.67E-06	88.75E-06	23.44E+03	5.86E+03	22.89E+00	183.11E+00
0101	32	85.33E-06	177.49E-06	11.72E+03	2.93E+03	11.44E+00	91.55E+00
0110	64	170.67E-06	354.99E-06	5.86E+03	1.46E+03	5.72E+00	45.78E+00
0111	128	341.33E-06	709.97E-06	2.93E+03	732.42E+00	2.86E+00	22.89E+00
1000	256	682.67E-06	1.42E-03	1.46E+03	366.21E+00	1.43E+00	11.44E+00
1001	512	1.37E-03	2.84E-03	732.42E+00	183.11E+00	715.26E-03	5.72E+00
1010	1024	2.73E-03	5.68E-03	366.21E+00	91.55E+00	357.63E-03	2.86E+00
1011	2048	5.46E-03	11.36E-03	183.11E+00	45.78E+00	178.81E-03	1.43E+00
1100	4096	10.92E-03	22.72E-03	91.55E+00	22.89E+00	89.41E-03	715.26E-03
1101	8192	21.85E-03	45.44E-03	45.78E+00	11.44E+00	44.70E-03	357.63E-03
1110	16384	43.69E-03	90.88E-03	22.89E+00	5.72E+00	22.35E-03	178.81E-03
1111	32768	87.38E-03	181.75E-03	11.44E+00	2.86E+00	11.18E-03	89.41E-03

Chapter 5 Lock Time Measurement

5.1 Digital Readout of Phase Data

A digital readout of phase error can be obtained by latching the stages of the N-counter with one edge of the input signal f_{in} [4]. This is shown in Figure 5.1. Either edge can be used to latch the data. Figure 5.2 illustrates latching of the data with the rising edge of f_{in}. Figure 5.3 illustrates latching data with the falling edge. For the data collection experiments conducted for this work, the rising edge of f_{in} is used for the latching of phase data from the loop counter. Figure 5.3 and Figure 5.4 also illustrate the difficulty of obtaining an accurate readout if the edges of the f_{out} N-stages line up the latching edge of f_{in}. Adding some delay to the latching edge allows us to avoid the loop counter jitter for a more stable phase capture.

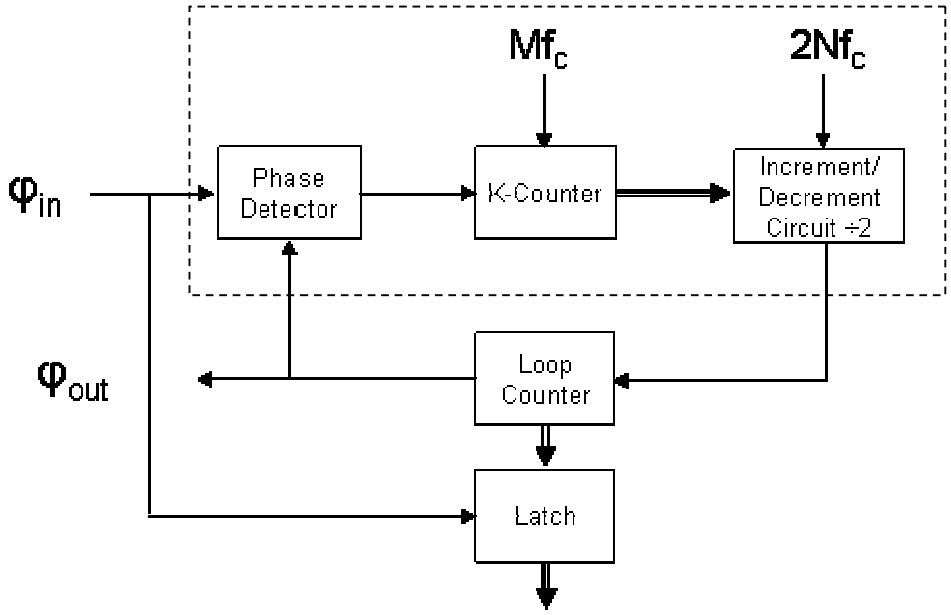


Figure 5.1 Phase data can be latched from the outputs of the N-counter.

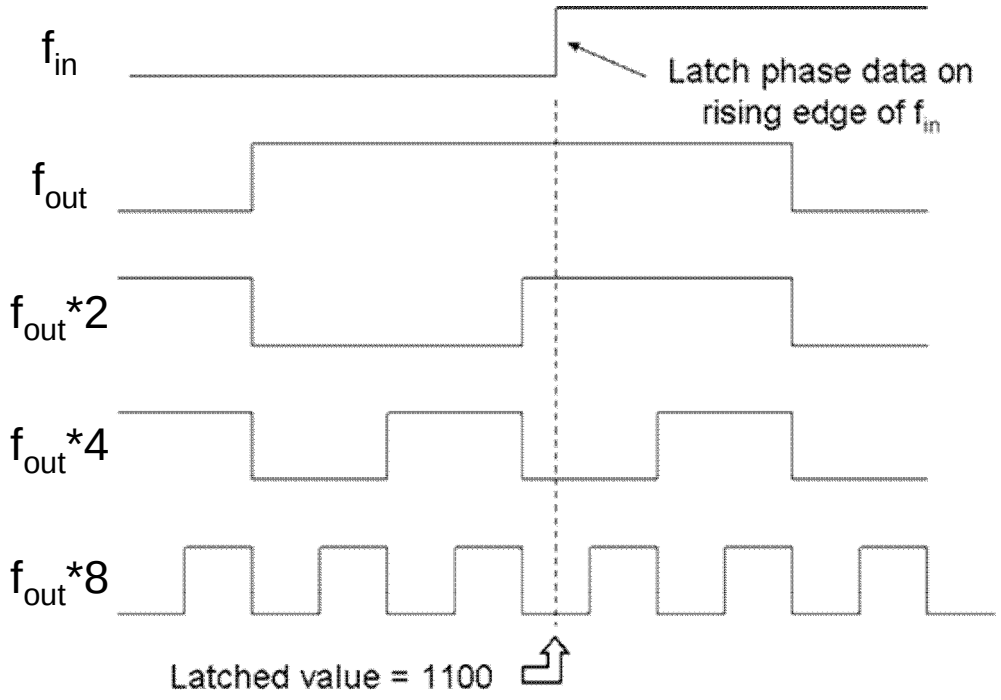
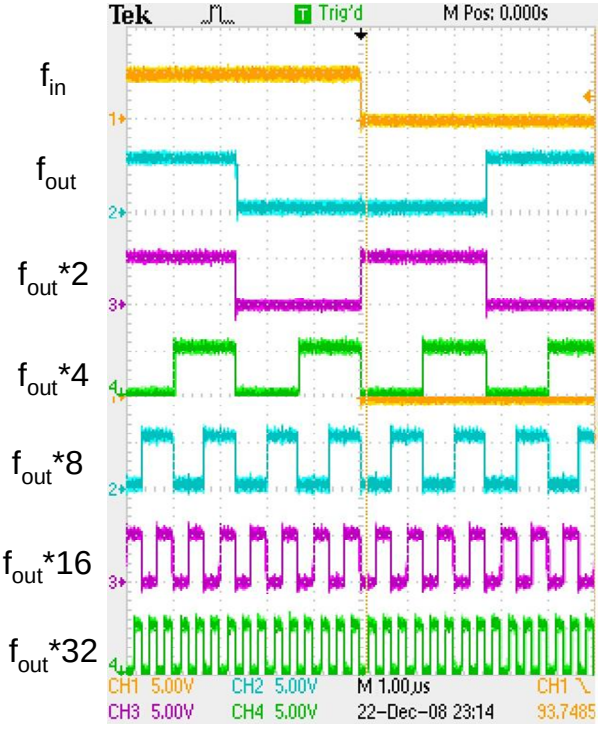


Figure 5.2 Phase data can be latched from N-counter on rising edge of f_{in}.



f_{in}, f_{out}, and five intermediate stages of N-counter

If f_{in} edge lines up the edges of ÷N stages, it will be difficult to latch. Solution: add delay to f_{in}.

Figure 5.3 Scope plot of f_{in} and several stages of the N-counter.

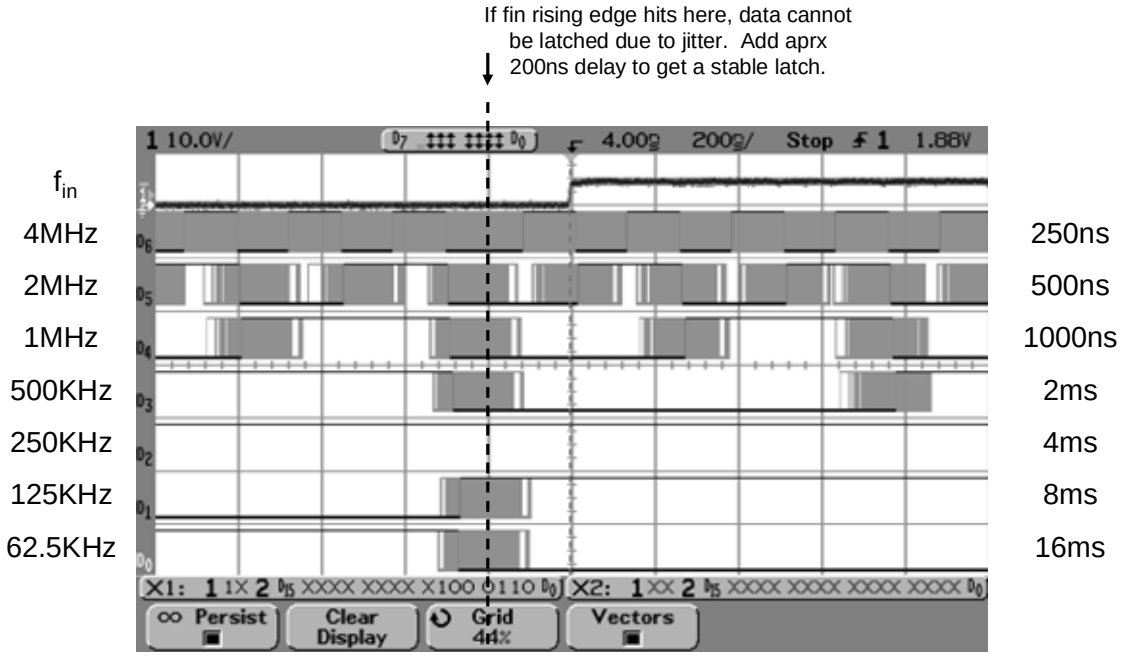


Figure 5.4 Five LSBs from N-counter have stable data on rising edge of f_{in}.

The output of the latch can be compared with an expected value to determine whether the loop is locked. The block diagram of a circuit to perform this function is shown in Figure 5.5.

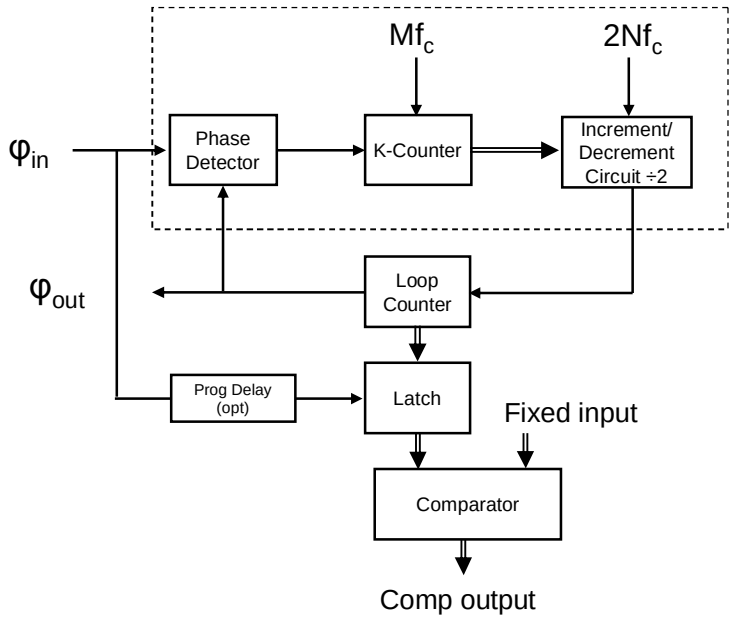


Figure 5.5 Comparing latched phase data with a fixed word.

If $f_{in} \neq f_c$, the latch output will be different for different values of K which are programmed into the K-counter. Given that we are switching between wide lock range and narrow lock range, a pair of comparators can be used – one for wide lock range checking and one for narrow lock range checking. The outputs of the comparators can be fed into a state machine which will switch between different values of K for the K-counter. This is illustrated in Figure 5.6.

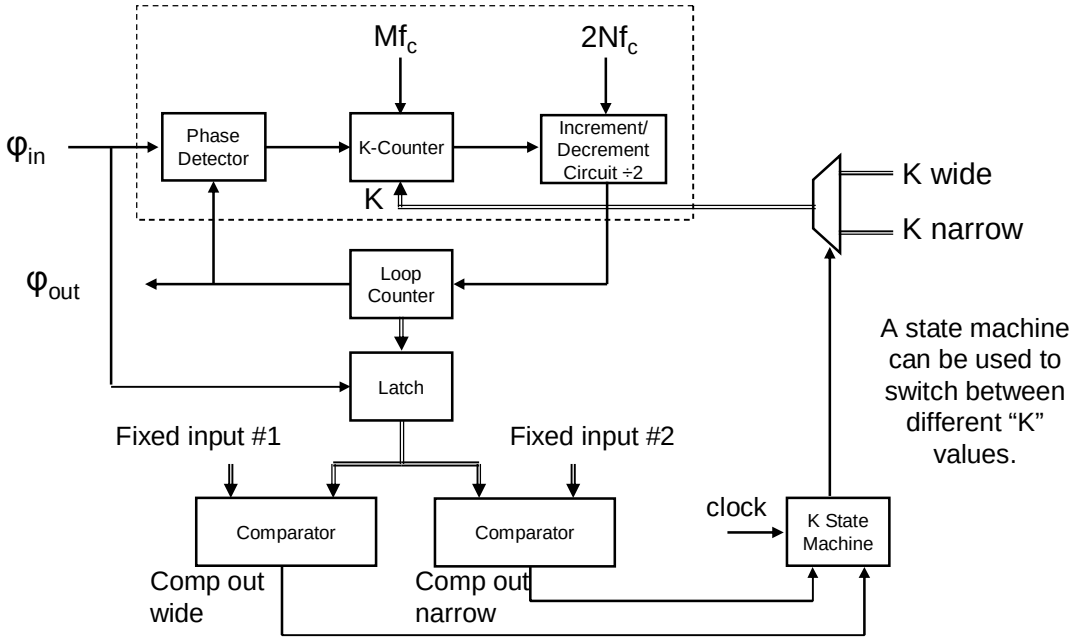


Figure 5.6 Digital Phase Locked Loop with Latch, Comparator, & K-Select.

5.2 Lock Time Experiment Methodology

To run lock time experiments, a test setup was implemented to periodically take the loop out of lock and force to loop to re-lock. This could be done my muxing the input with a static signal (stuck low or stuck high) or by muxing the input with the inverse of itself as shown in Figure 5.7. It turns out that muxing the input with the inverse of itself is worst-case. Muxing with a low or

high does not necessarily take the loop out of lock because the output of the EXOR phase detector could still be approximately 50% under these conditions. So the ID circuit will just continue to turn out an equal number of increments and decrements, resulting in zero phase change.

The lock time is the time it takes to re-lock the loop after the input signal is inverted. The loop is considered locked if a match is reached on one of the comparators.

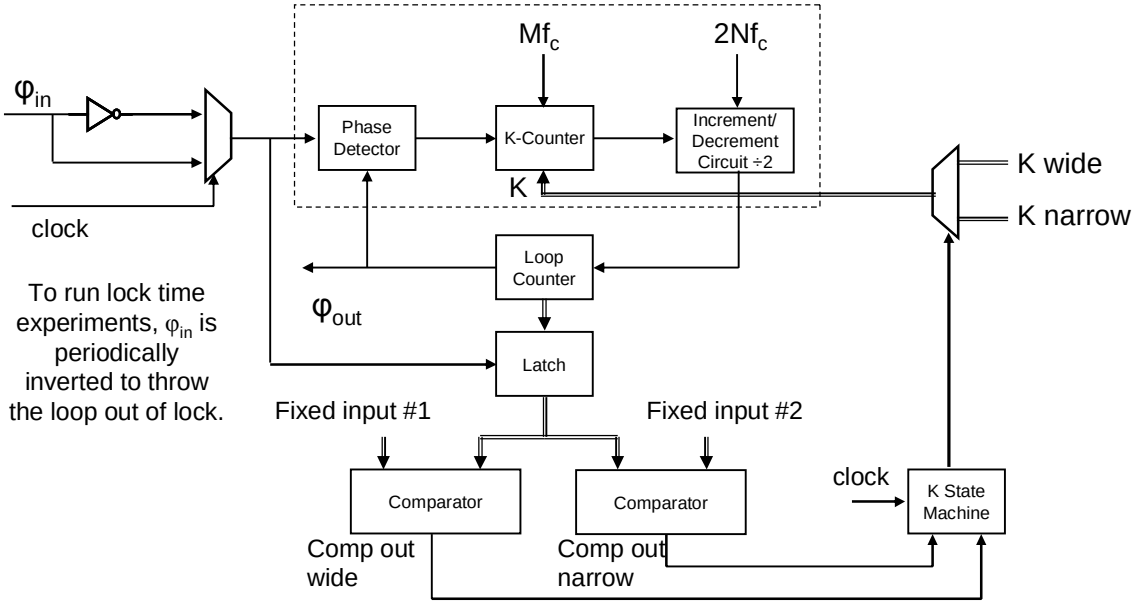


Figure 5.7 Experimental setup to periodically take the loop out of lock.

Chapter 6 K State Machine

To work around the lock time versus bandwidth issue, it is desirable to have an arrangement where the loop parameters are set for fast lock if the loop is in an unlocked condition. Once the loop is locked, the loop parameters may be changed for narrow bandwidth and higher accuracy.

A state machine can be used to change the bandwidth on the fly to adjust between wide bandwidth and narrow bandwidth. This is shown in diagram form in Figure 6.1 and in tabular form in Table 6.1.

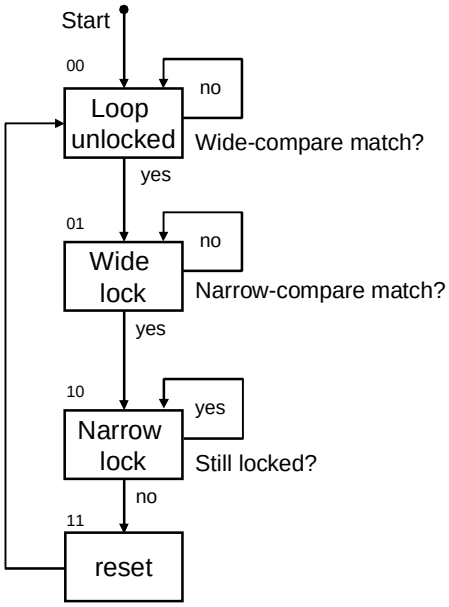


Figure 6.1 State machine diagram.

The state machine has four states: unlocked, wide lock, narrow lock, and reset. If the input signal to the loop is absent or out of lock, the state machine starts with the unlocked state. In this state the loop is attempting to lock with a

wide lock range. A compare match for a wide lock condition sends the state machine to the next state which is the wide lock state. Upon moving into the wide lock state the loop parameters are changed so that the loop is attempting to lock with a narrow lock range. A compare match for a narrow lock condition sends the state machine to the narrow lock state. In the narrow lock state the controller checks for a compare mismatch on the narrow lock condition which will send the state machine to a reset state and back to the unlocked state.

Table 6.1 K State Machine Table.

State	State counter	UL	LW	LN	Rout	CW	CN	Count enable	Next state
Unlocked	**00**	**1**	**0**	**0**	**0**	**0**	**X**	**0**	**Unchanged**
	00	**1**	**0**	**0**	**0**	**1**	**X**	**1**	**Locked wide**
Locked Wide	**01**	**0**	**1**	**0**	**0**	**x**	**0**	**0**	**Unchanged**
	01	**0**	**1**	**0**	**0**	**x**	**1**	**1**	**Locked narrow**
Locked Narrow	**10**	**0**	**0**	**1**	**0**	**x**	**1**	**0**	**Unchanged**
	10	**0**	**0**	**1**	**0**	**x**	**0**	**1**	**Reset**
Reset	**11**	**0**	**0**	**0**	**1**	**x**	**X**	**1**	**Unlocked**

Notes:

UL – unlocked
LW – locked wide
LN – locked narrow
Rout – reset output
CW – compare wide match
CN – compare narrow match

The state machine can be constructed with a two-bit counter and some control logic. The schematic diagram of a digital logic circuit which performs this function is shown in Figure 6.2. A pair of 5-bit comparators performs a check to determine if the loop is “locked wide” or “locked narrow.” An external clock is

supplied to the counter. The clock period should be less than the lock time of the loop, and the clock rate should be slower than the center frequency of the loop. The unlocked (UL) output can be used to control the modulus of the K-counter.

In breadboard experiments, it was found that because of increment/decrement adjustment of f_{out}, jitter can cause a false reset if all five bits are used to determine a Reset on compare narrow (CN). Therefore, only a gross check on the two least significant bits is used to determine an out of lock condition.

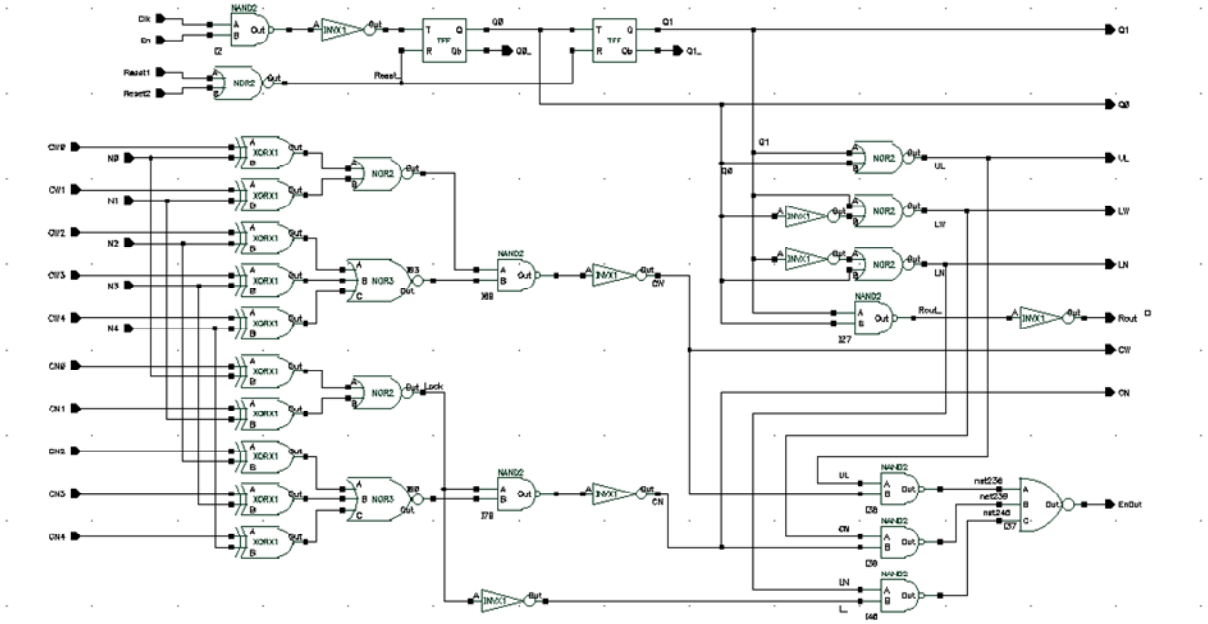


Figure 6.2 K state machine and comparator logic.

Chapter 7 Step Function Response

To study how the loop responds to a change in phase, we model the loop as a first order control system and determine the step-function response of the system. A control systems diagram of a first order loop is shown in Figure 7.1 and associated equations are shown below [6], [7].

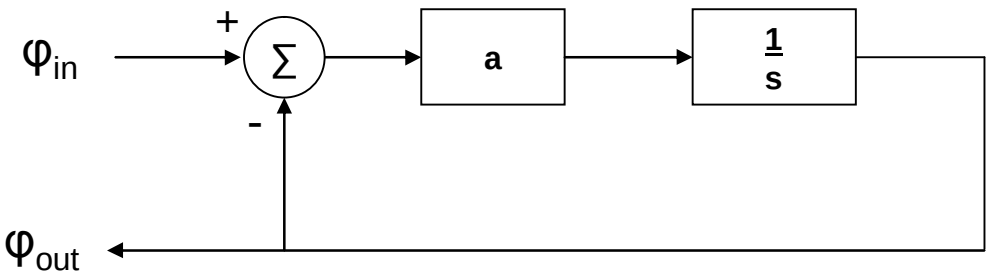


Figure 7.1 First order loop control systems representation.

The control system equation for the loop can be expressed as

$$H(s) = \frac{a}{s+a}, \tag{1}$$

where the constant a is the bandwidth of the loop. Equation (1) has a time domain solution of

$$h(t) = ae^{-at}. \tag{2}$$

The loop has a step function phase error response of

$$\phi_e(t) = \phi_e(0)e^{-\frac{t}{\tau}}. \tag{3}$$

The time constant τ is a function of the K-counter modulus K, the N-counter modulus N, and the K-clock frequency Mf_c, or

$$\tau = \frac{KN}{2Mf_c}. \tag{4}$$

With M, N, and f_c normally fixed, we can adjust the time constant by adjusting K. The initial condition phase error $\varphi_e(0)$ must be in the range of ±¼ cycle and for the case of $f_{in}=f_c$, the final steady state phase error $\varphi_e(\infty)$ will be zero plus or minus some jitter.

For lock time calculations Equation (3) can be solved for t as

$$t = -\tau \ln \frac{\phi_e(t)}{\phi_e(0)}, \tag{5}$$

where $\varphi_e(0)$ is the initial phase error and $\varphi_e(t)$ is the ending phase error.

The loop parameters used for lock time simulations and experiments are:

f_c =62500 Hz,

f_{in}=62400 Hz or 62500 Hz,

k_d=4,

N=128,

K=2^1 through 2^{15},

Mf_c=24 MHz,

$2Nf_c$=16 MHz.

The K-counter modulus K is variable and other parameters are fixed. Clock rates were chosen based on the operating frequency of 0.5 micron process CMOS circuits and availability of off-the-shelf clock chips for prototyping.

For loop evaluations the input frequency is equal to the center frequency ($f_{in}=f_c$) or slightly off-center ($f_{in}\neq f_c$) as listed above. Given $f_{in}=f_c$, the phase error should be zero after a suitable period of lock time. Lock time can be measured by one of the following methods:

1. The time to reach $\varphi_e(\infty)$ plus or minus a small delta, e.g., 1/32 cycle or

0.03125 cycle.

2. The time to reach a match on five of the seven outputs of the N-counter.
3. The time for the phase error to settle within 12.5% of its final value, or 2.08τ .
4. The time for EXOR phase detector output to reach a duty cycle of 50% plus or minus a small delta.

Five latched outputs of the N-counter correspond to 1/32 of a cycle or about 0.03125 cycles. For K=16, from Equation (4) we have a time constant τ of 42.7μs. Starting at worst case phase error of 0.25 cycles it takes the loop about 90μs to reach a locked value of 0.03125 cycles. This may be calculated using Equation (5) using an initial phase error of $\varphi_e(0)=¼$ and a final phase error of $\varphi_e(t)=1/32$. A graph of the phase error versus time for the above set of loop parameters with K=16 is illustrated in Figure 7.2 as calculated in a spreadsheet.

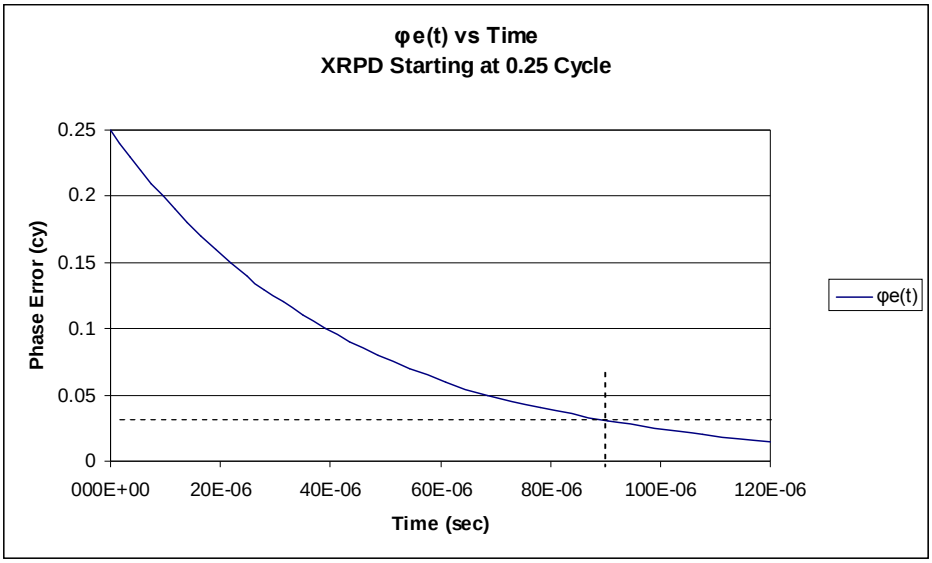


Figure 7.2 Step function response, wide lock range, K=16, 90μs lock time.

Using LTSpice [8], a simulation of this condition was conducted and is shown in Figure 7.3. The lock time is the time it takes for the output of the phase detector to reach a duty cycle of approximately 50%. This takes about 90µs in the simulation and matches well with the spreadsheet prediction.

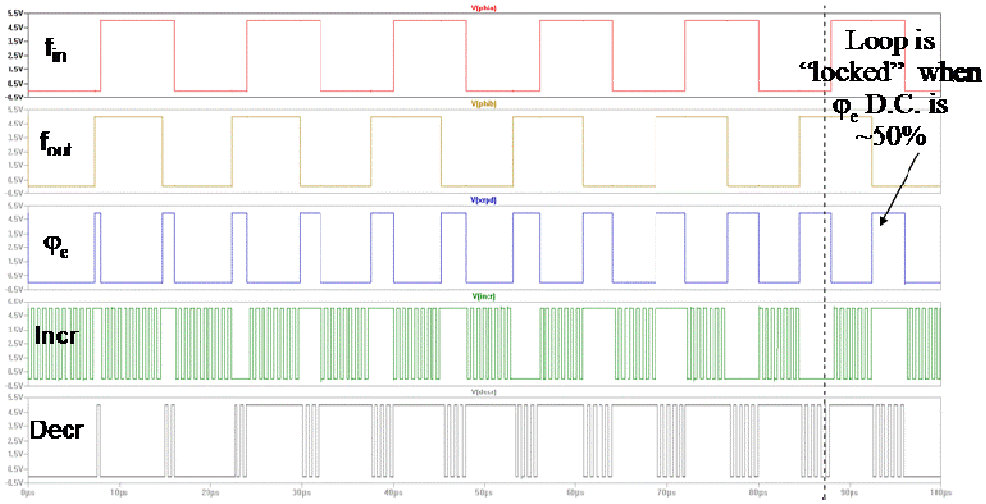


Figure 7.3 Spice simulation of loop step response, 0.25 cy to 0 cy, K=16.

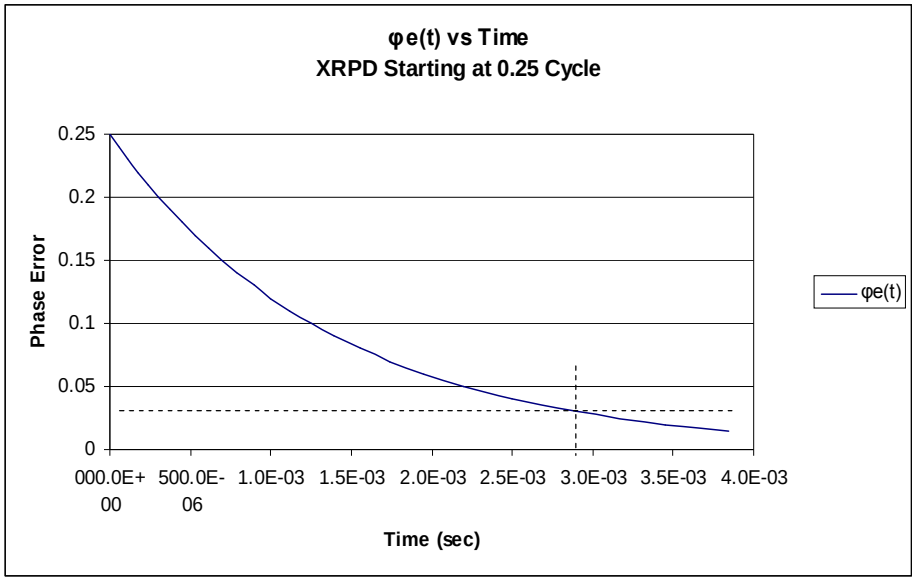


Figure 7.4 Step function response, narrow lock range, K=256, 2.84ms lock time.

Changing K to 256 results in an increase in lock time to about 2.8ms as illustrated in Figure 7.4. Spice simulation was not performed for the case of K=256 due to the excessive simulation time required.

Due to the lengthy lock time at K=256 versus K=16, it would be desirable to initially set K=16 for fast lock time, then switch to K=256 after the loop is locked to achieve the benefits of narrow bandwidth. Figure 7.5 shows hypothetical lock results with an initial setting of K=16, then switching to K=256 after the phase moves within a sufficiently small delta of $\varphi_e(\infty)$. This is the effect we wish to achieve with the K state machine and controller circuit.

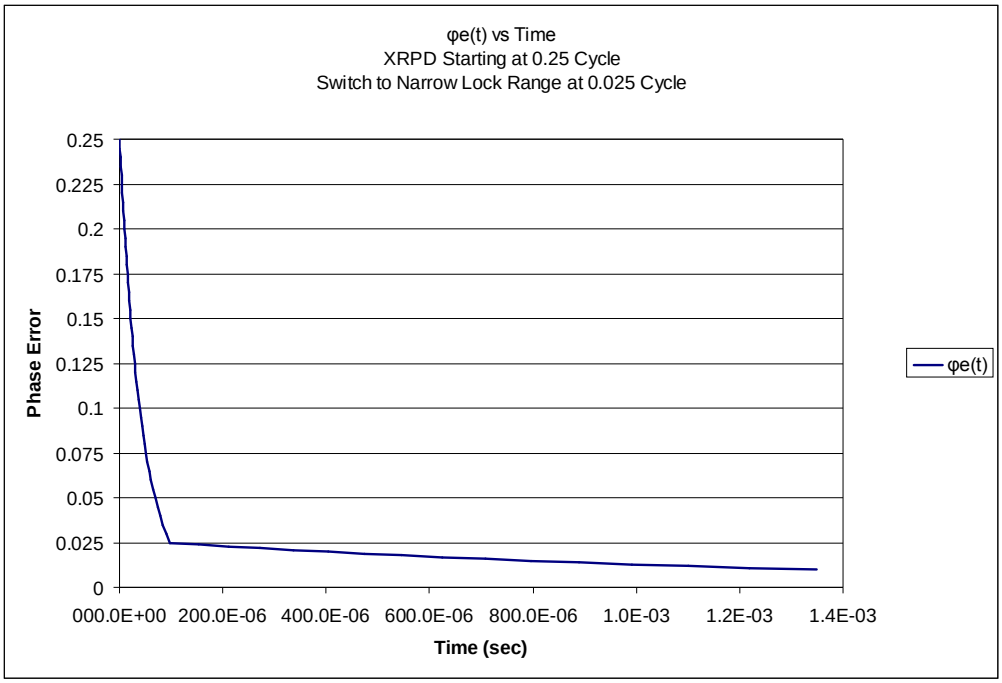


Figure 7.5 Phase error versus time. Wide lock range, lock, switch to narrow.

Chapter 8 Phase Detector Issues and Improvements

In the course of conducting initial lock time experiments associated with the controller and state-machine, it was observed that lock time was taking longer than predicted by the first order step response equations for the loop. Investigation showed that this was due to situations where the input signal initial phase was outside the phase lock range of the EXOR phase detector.

8.1 EXOR Phase Detector Lock Range

Zero phase error is defined in the references as a 50% duty cycle error signal at the output of the phase detector. This is the case when the input signal is equal in frequency to the loop center frequency ($f_{in}=f_c$) and the loop has had sufficient lock time for the phase error to reach steady state. When the input signal f_{in} is not equal to the center frequency f_c, the steady state phase error will deviate from 50%. The lock range for a loop with EXOR phase detector is ±¼ cycle as shown in Figure 8.1.

If the frequency of the incoming signal is within the lock range of the loop, but the initial phase is outside the ±¼ cycle lock range, the loop can still lock after transitioning through this non-lock region. However, the phase will adjust in an inverted exponential curve manner until it reaches the lock region, and then it will adjust in the normal exponential manner. This is illustrated in Figure 8.2.

If the phase starts out at the worst case value of 0.5 cycles, it will move slowly away from 0.5 cycle point, accelerate through the 0.25 point, and then

slow down as it approaches 0.0 cycles. Thus starting with an initial phase error of 0.5 cycles instead of 0.25 cycles could easily double the lock time of the loop.

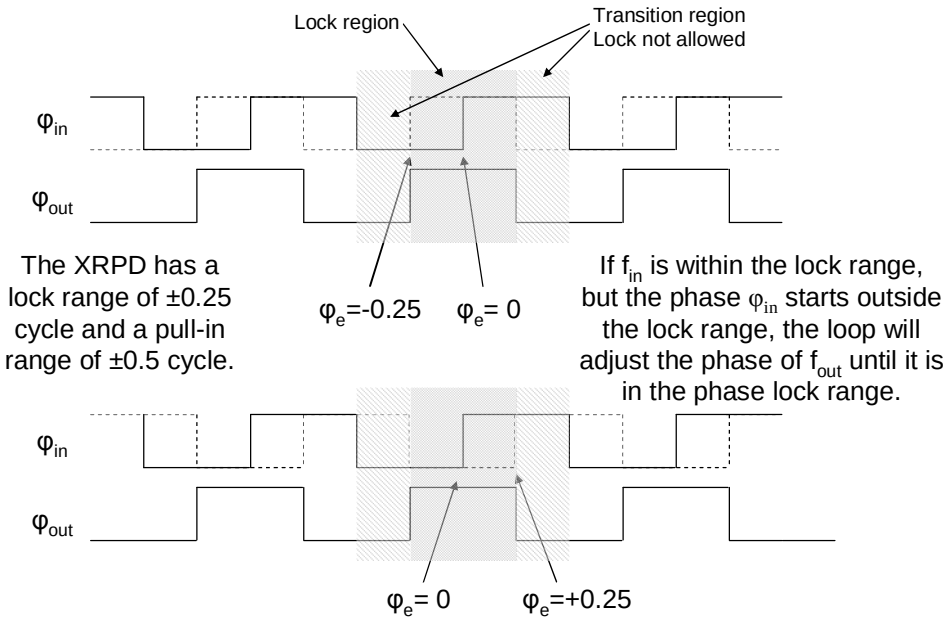


Figure 8.1 EXOR phase detector, lock range and transition range.

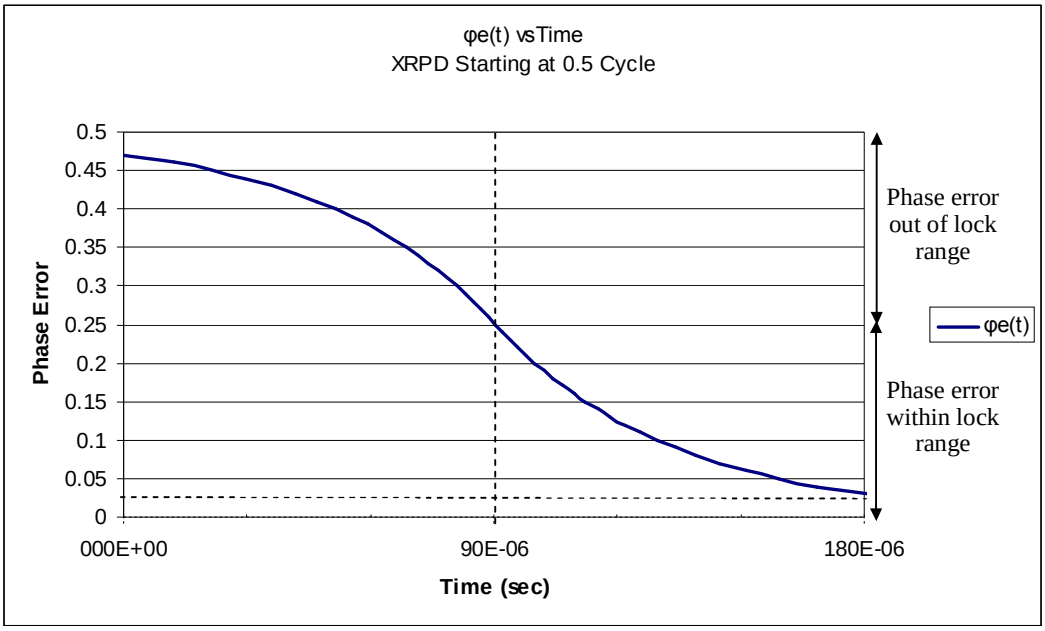


Figure 8.2 Inverted exponential response in 0.5 cy to 0.25 cy range.
Normal exponential response in 0.25 cy to 0 cy range.

To verify this behavior, a spice simulation was executed and plotted. Figure 8.3 illustrates a spice simulation of the lock sequence when the initial phase error is outside the lock range of the loop. In this example, the phase detector output starts with a duty cycle of approximately 50% and gradually decreases to 0%. At 0%, it crosses over into the lock range of the loop and starts increasing again back to 50% where it is considered locked.

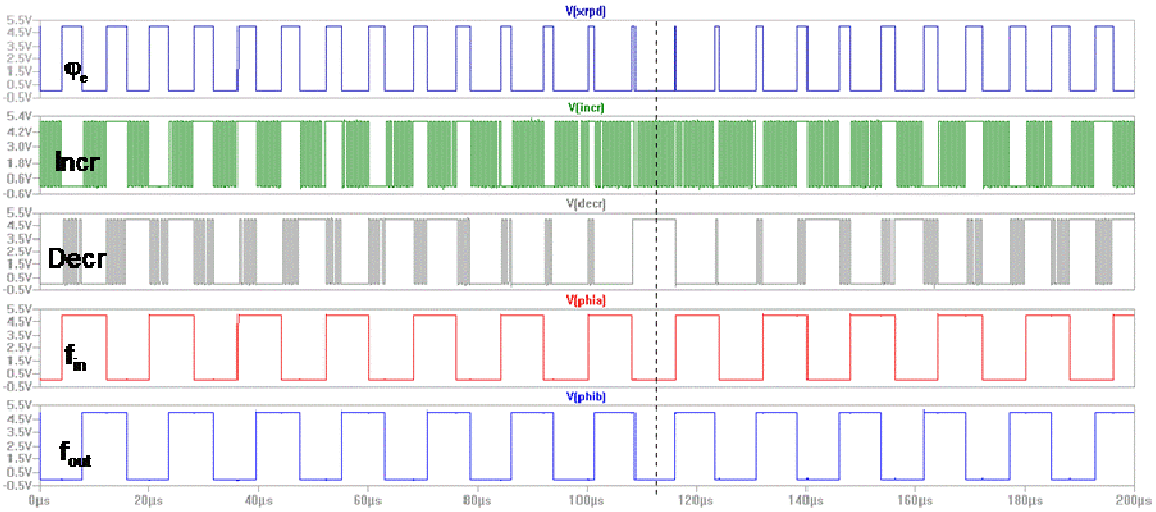


Figure 8.3 Spice simulation, initial phase error outside of lock range.

8.2 EXOR Phase Detector AND Gate Solution

Figure 8.4 illustrates a solution to the out of lock range problem. An AND gate is inserted between the EXOR phase detector and the K-counter and the D_0 bit from the N-counter is AND-gated with the output of the phase detector. When φ_{in} is out of lock range a '0' will be latched on D0. This forces the U_D signal low, which will force the K-counter to count only in one direction (increment). When φ_{in} is within lock range, D_0 is high, the EXOR output will pass through the AND gate, and the loop will lock normally. The disadvantage of this arrangement

is if φ_{in} is on the wrong side of the pull-in range, it will take extra time to move into the lock range. Spice simulation for this arrangement is shown in Figure 8.5.

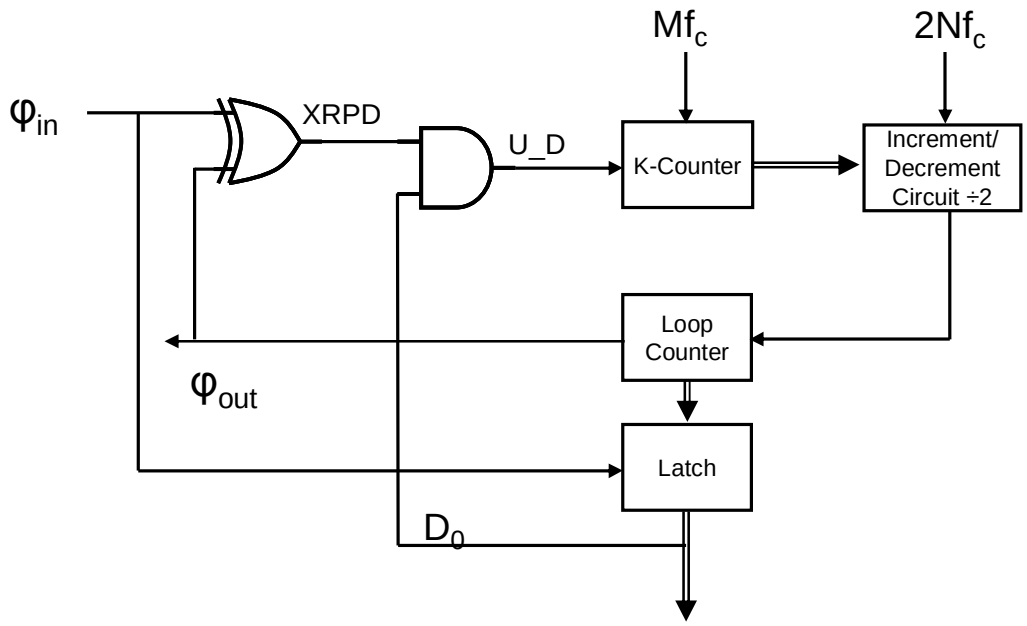


Figure 8.4 AND gate solution to out-of-lock-range problem.

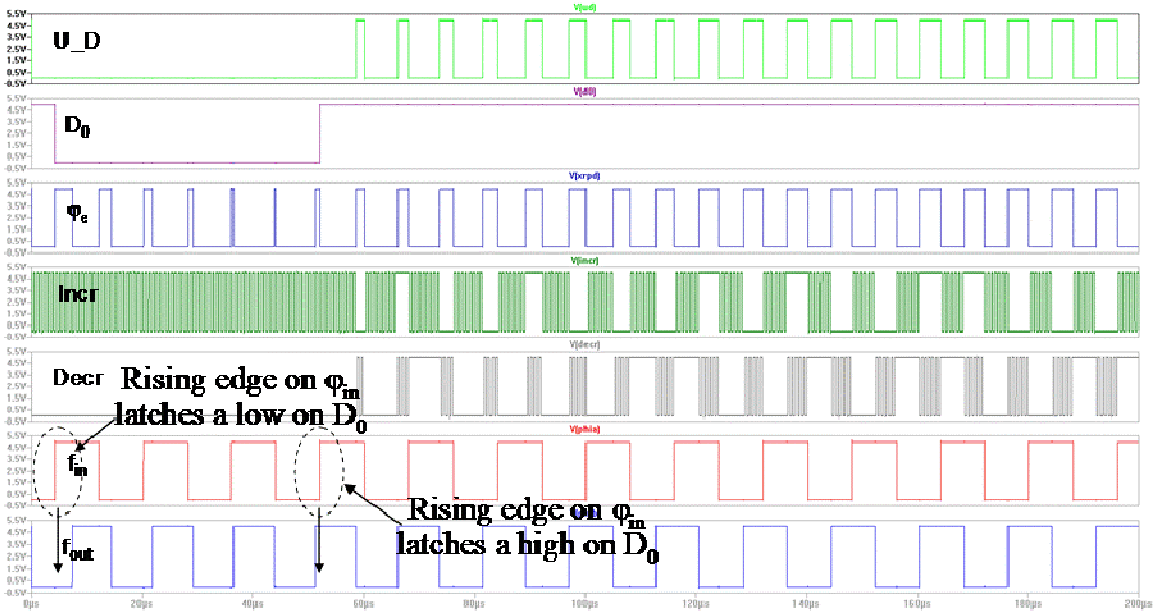


Figure 8.5 Spice simulation of AND gate solution.

8.3 EXOR Phase Detector Latch/Mux Solution

A better way to approach the out-of-lock-range issue would be to take the shortest path to return to lock range by forcing the K-counter to count only up or only down depending on whether the incoming phase is lagging or leading the output signal phase. A possible solution to the EXOR out-of-lock-range issue based on this concept is shown in Figure 8.6. When the input phase φ_{in} is out of lock range, the D_0 bit from the N-counter latch selects the output of the phase detector latch to pass through the multiplexer. The N_1 output from the N-counter is used to latch the output of the phase detector. N_1 latches a high if φ_{out} is leading forcing K-counter to count down (decrement). N1 latches a low if φ_{out} is lagging forcing K-counter to count up (increment). When φ_{in} is in lock range D_0 selects the EXOR output through the multiplexer and the loop will lock normally.

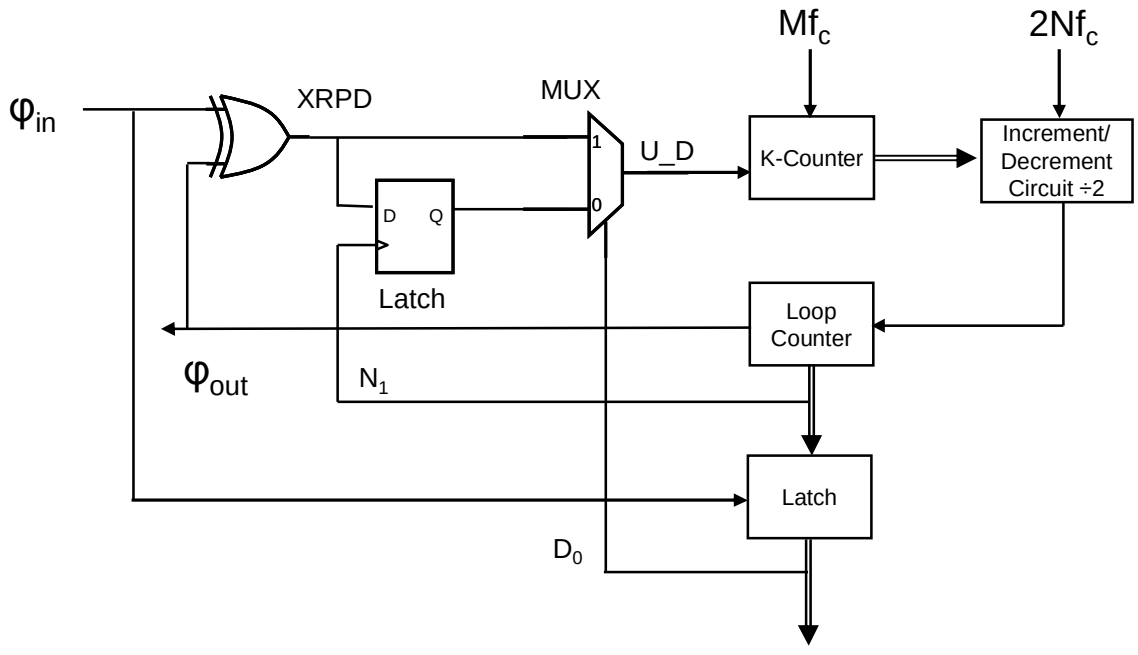


Figure 8.6 Latch/mux solution to out-of-lock-range problem.

Figure 8.7 illustrates waveforms from a spice simulation for the above circuit for the case of φ_{out} lagging and Figure 8.8 illustrates the case of φ_{out} leading. In both cases the lock time is faster than using just the EXOR phase detector without the latch/mux modifications.

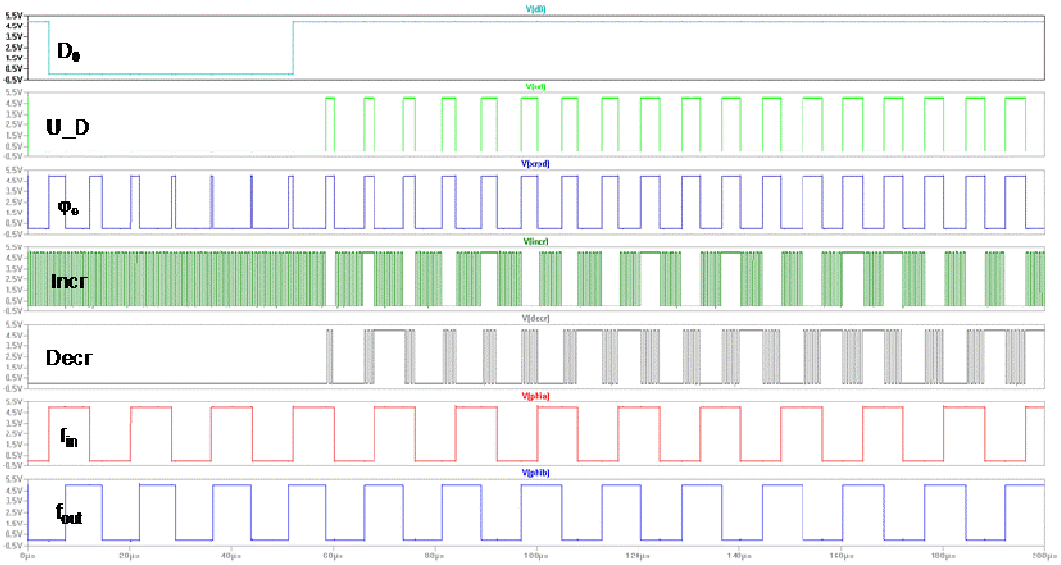


Figure 8.7 Spice simulation, latch/mux, f_{out} lagging.

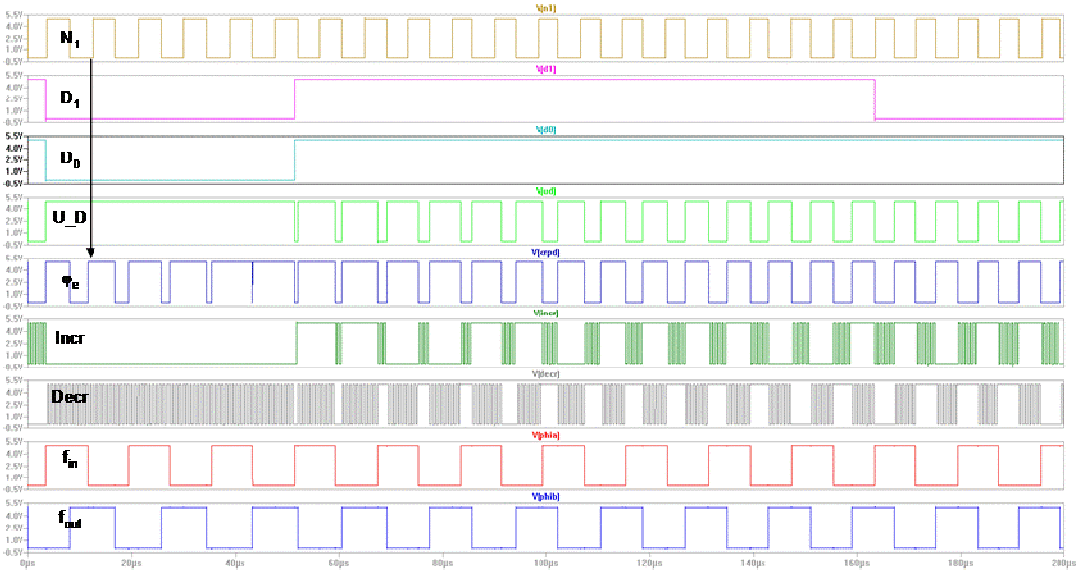


Figure 8.8 Spice simulation, latch/mux, f_{out} leading.

Chapter 9 Design and Layout of the Controller

The circuit was designed using Cadence design tools for manufacturability on 0.5μm CMOS integrated circuit technology. To simplify the design publicly available libraries were used whenever possible. NCSU_TechLib_ami06 [9] was used for basic elements such as MOS transistors and vias. For logic elements, the UT_AMI06 [10] and OSU_AMI06 [11] libraries were used. These libraries were designed to work with the NCSU_TechLib_ami06 library. In some cases the required logic functions were not available in either of these libraries, so these blocks had to be designed from scratch. The text by Hodges, Jackson, and Saleh [12] was used as a guide for design of these logic elements. For pad design, the mAMI05P pad cell library was used, which is available from the Mosis web site [13].

Although a commercially available pulse addition/removal type DPLL is available as an off-the-shelf component, it was desirable to reduce overall package count of the circuit. Thus the DPLL was redesigned to include normally external components. This also provided an opportunity to prove out the Cadence layout process and Mosis circuit manufacturability flow. The K-counter was modified for a minimum K-counter modulus of 2^1 as compared to the off-the-shelf DPLL which has a minimum K-counter modulus of 2^3. This provided for the opportunity to perform some low-K lock time experiments which could not be performed with the off-the-shelf unit. The capability for resetting the counters was included in the design along with a ring oscillator for performance

measurement. A single chip with the controller and DPLL components would have required two Mosis “TinyChip” units and would have put the pin count over forty pins. Thus two chips were needed, one for the DPLL and associated components and one for the controller circuit. The Cadence schematic for the DPLL circuitry is shown in Figure 9.1.

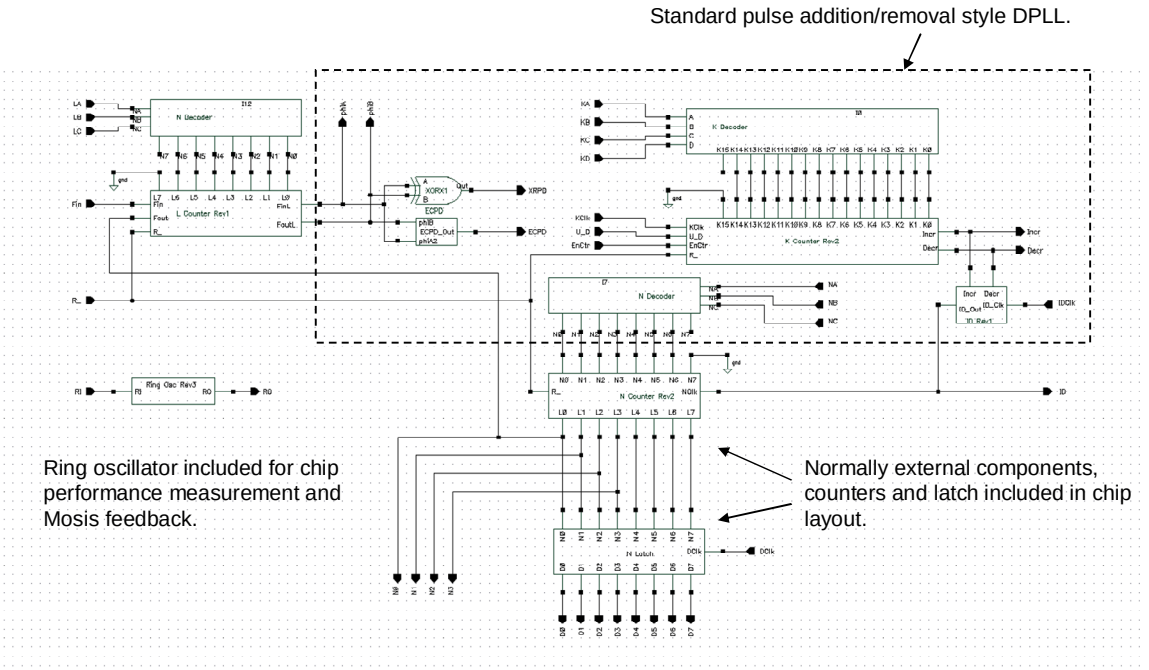


Figure 9.1 DPLL cadence schematic.

Blocks inside the dotted line are those normally available in the of-the-shelf version of the pulse addition/removal type DPLL. Counters and latches which are normally external components were included in the chip to facilitate interface with the controller. Although the “L-counter” was included for lock range widening, it was determined that widening of the lock range slows down the lock time. L-counter experiment results were therefore discarded as the goal of this project is to improve lock times. A ring oscillator was included on the chip for

performance measurement and comparison with the Mosis, ON Semiconductor wafer test structures. The layout of the DPLL chip is shown in Figure 9.2.

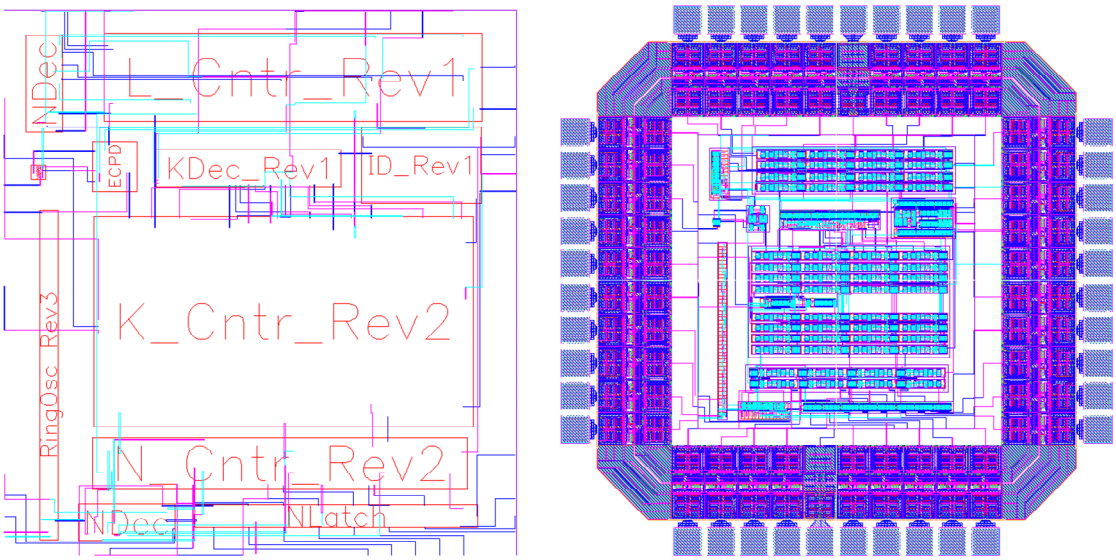


Figure 9.2 DPLL layout for Mosis submission.

The schematic diagram for the controller for the loop is shown in Figure 9.3. Both the K state machine controller and the phase detector latch/mux modifications are included in the circuit layout. A toggle latch (T flip-flop) was designed to construct the two bit counter. Other components are standard logic gates. The layout is shown in Figure 9.4. The die size of the controller is much smaller than the pad frame so some dummy polysilicon had to be added to cover the unused die space to meet the manufacturer's CMP polishing rules.

Both chips were submitted for fabrication on the 1/17/12 Mosis ON Semiconductor C5 run (V21G) and packaged chips were received 4/30/12. Design statistics for the two chips are listed in Table 9.1 and Table 9.2**.**

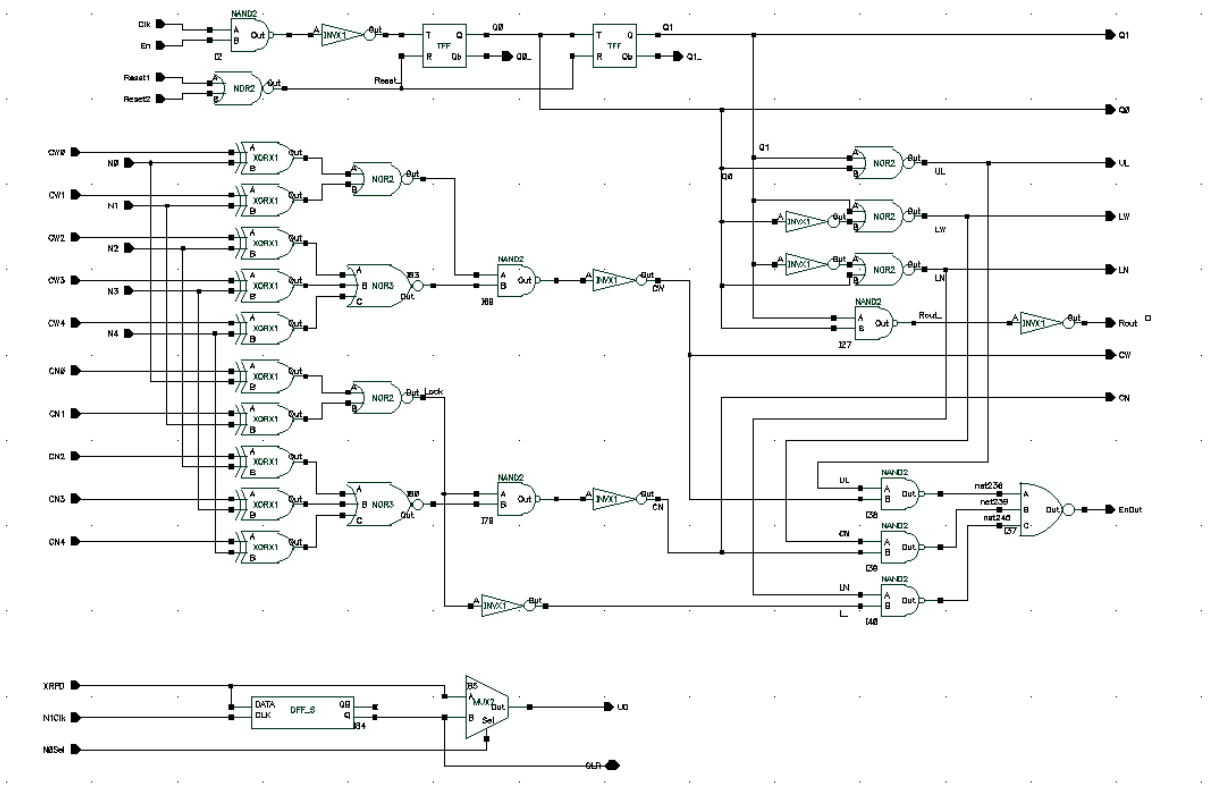


Figure 9.3 DPLL K state machine Cadence schematic.

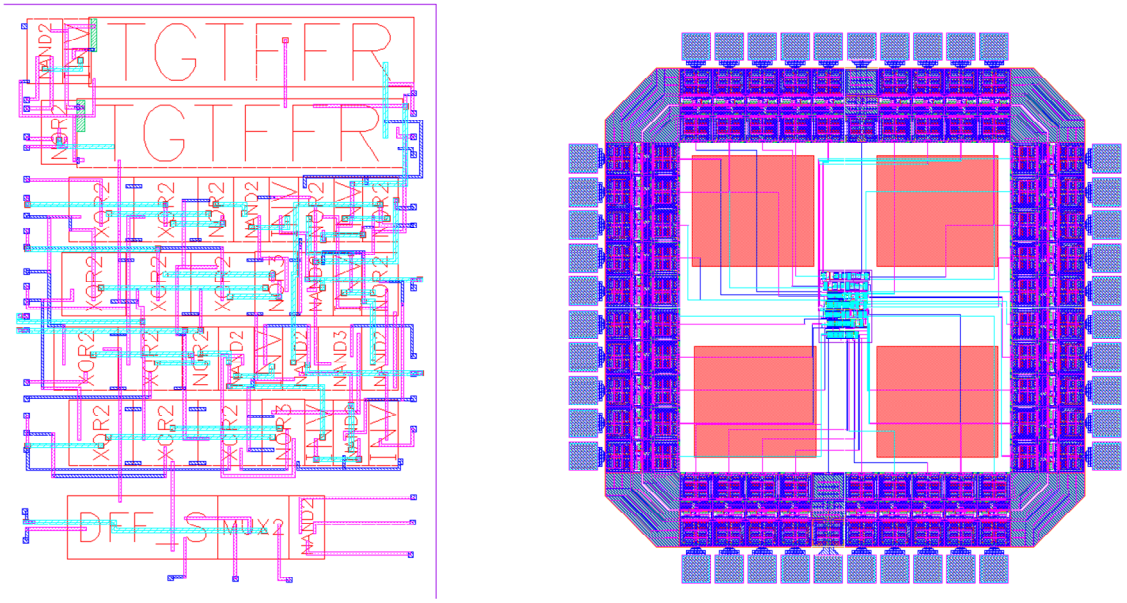


Figure 9.4 DPLL controller layout for Mosis submission.

Table 9.1 DPLL Revision 3 Design Statistics.

Nets	1472
Terminals	40
Pmos transistors	1490
Nmos transistors	1489

Table 9.2 DPLL Controller Design Statistics.

Nets	170
Terminals	40
Pmos transistors	146
Nmos transistors	136

Chapter 10 Test Results of First Pass Fabricated Chips

Initial chips manufactured through Mosis were received on schedule 4/30/12 and were non-functional due to excessively slow output transition times. The chips were manufactured on Mosis run V21G (ON Semiconductor C5F). Scope plots were taken on the actual circuits and simulations were run in attempt to explain the problem.

Examining output waveforms, it was found that rise and fall times were slower than expected. Figure 10.1 and Figure 10.2 show typical transition times. In the figures, the top waveform is the input to a multiplexer at approximately 732Hz; the middle waveform is the output of the multiplexer and input to a NAND gate configured as inverter; and the bottom waveform is the output of the NAND gate.

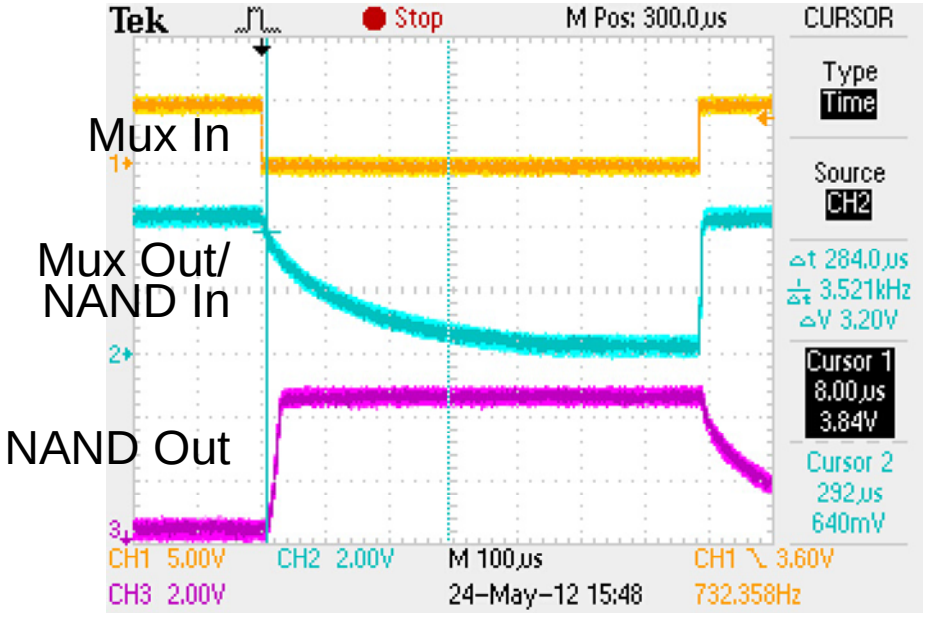


Figure 10.1 Output fall time (middle) 284µs.

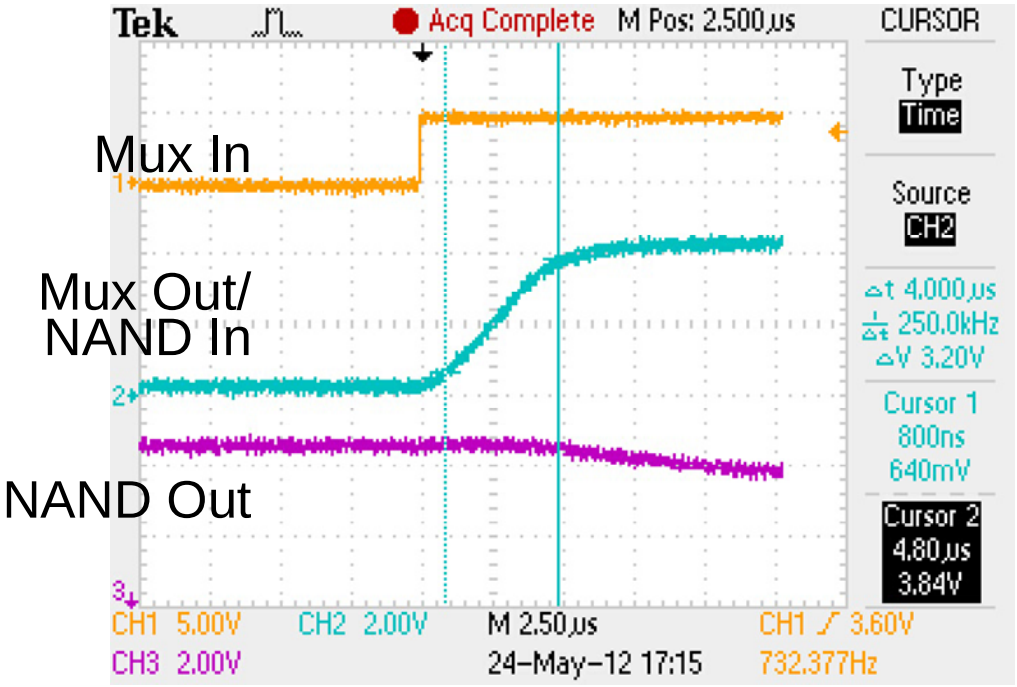


Figure 10.2 Output rise time (middle) 4µs.

The fall time is about 284µs as shown in Figure 10.1 and the rise time is about 4µs as shown in Figure 10.2. This is causing the individual gates to run quite slow, in the 700-1000Hz range. Expected performance is >100MHz. Internal sub-blocks are non-functional even at speeds under 1KHz, indicating an internal issue, as opposed to a problem with the bond pads.

For comparison, transition times were checked on a pair of inverters from an earlier Mosis run, Ami05 T86Z. This is shown in Figure 10.3. The top waveform is the input to the first inverter at about 64KHz; the middle is the output of the first inverter and input to second inverter; and the bottom is the output of second inverter. Transition times are <10ns which is normal for this process/design.

Simulations were performed on the circuit designs in attempt to explain

the behavior of the fabricated circuits. Simulations were run on the circuits as-is with 0.6µm via sizes and with a 0.5µm shrink. Both of these produced normal transition times. Simulations were also run with and without bond pads. These also produced normal waveforms.

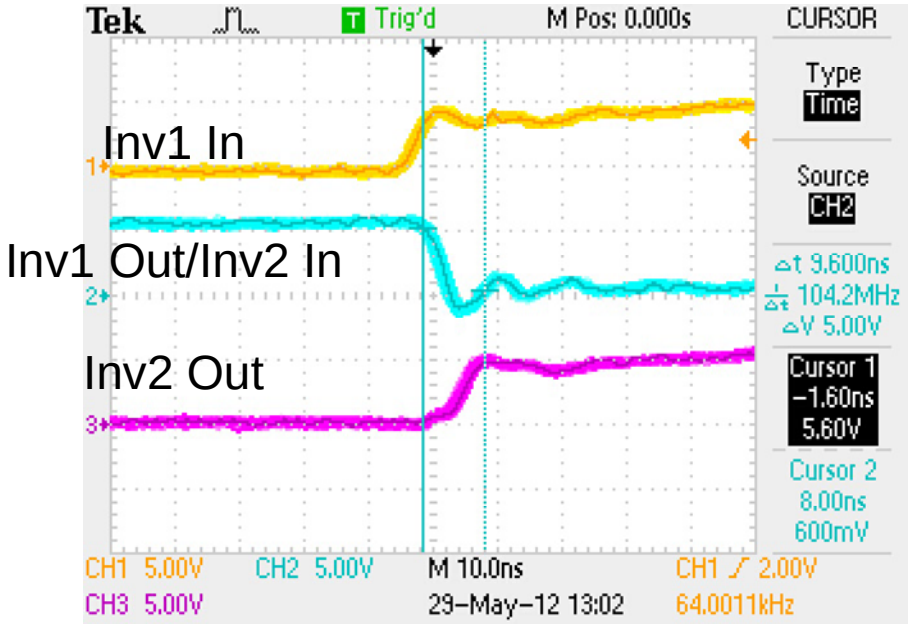


Figure 10.3 AMI 05 T85Z, normal transition times.

Next, some simulations were performed to reproduce the behavior of the fabricated circuits. The next two figures illustrate simulation of a gate with and without bond pads to determine whether the problem was in the pads or internal to the chip. Figure 10.4 shows simulation of a NAND gate without pads. Transition times are normal. Figure 10.5 shows simulation of a NAND gate with pads included. Transition times are in the 15-20ns range, higher than the transition times of actual silicon shown in Figure 10.3, but in line with expectations. Figure 10.6 shows simulation of a NAND gate with pads shrunk by 5/6 to achieve 0.5µm via size. Transition times are similar to Figure 10.5.

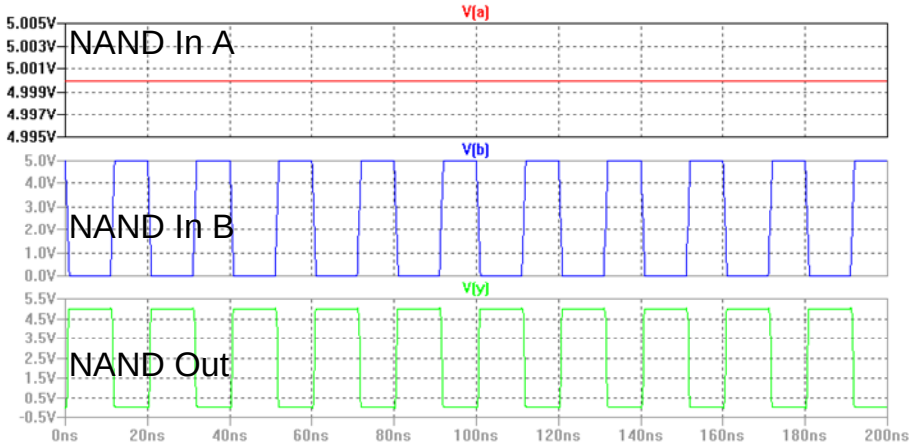


Figure 10.4 Simulation NAND gate with caps, no pads.
Normal transition times.

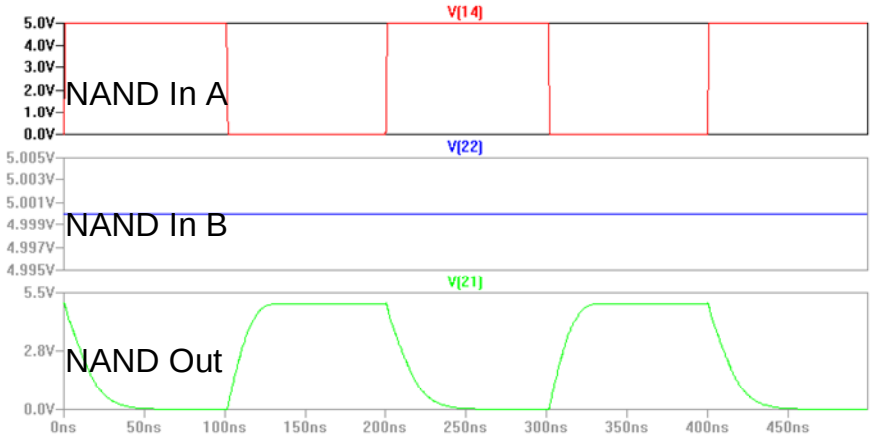


Figure 10.5 Simulation NAND gate with caps, with pads.
Normal transition times.

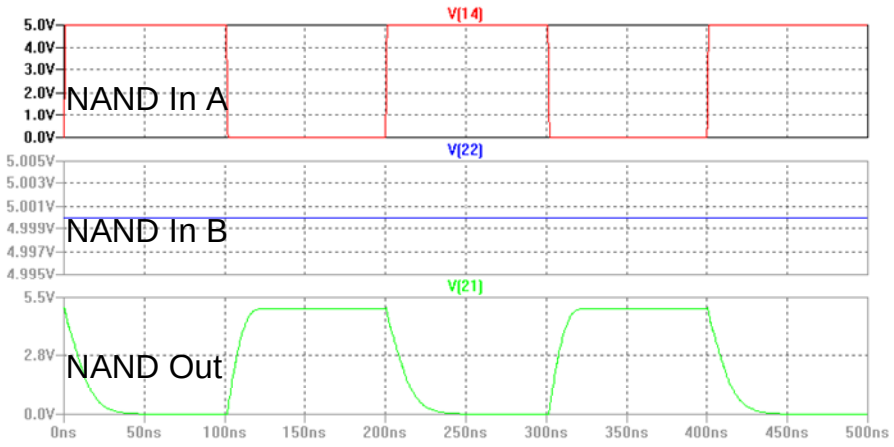


Figure 10.6 Simulation NAND gate shrunk to 0.5µm with caps, with pads.
Normal transition times.

The next few simulations were done with some anomalies inserted. Figure 10.7 shows simulation of a NAND gate with the p-well bias removed (increased from 0V to 5V). Vol is increased, but transition times are not affected.

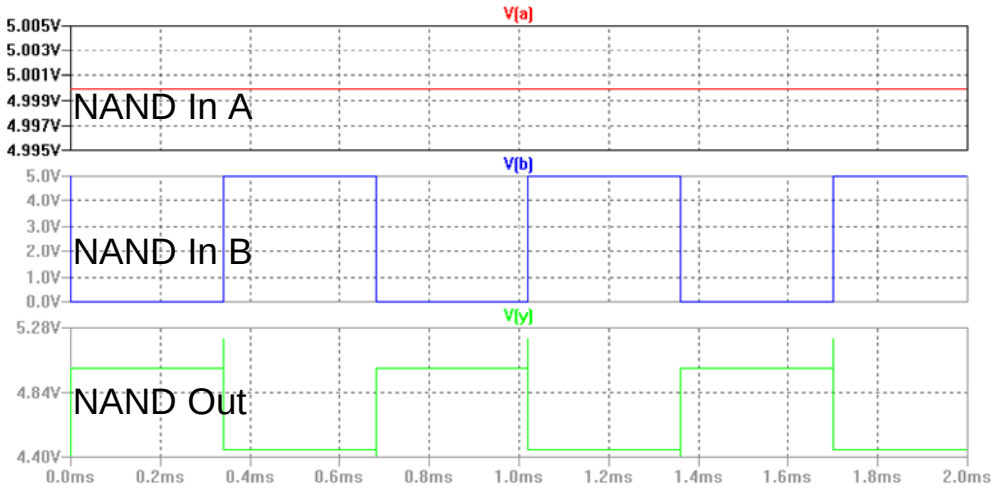


Figure 10.7 Simulation NAND gate with p-well bias removed.
Normal transition times, high vol.

Figure 10.8 shows the effect of inserting a large resistance (5000MΩ) between the two series pulldown (NMOS) transistors in the NAND gate. This reproduced the slow fall time problem.

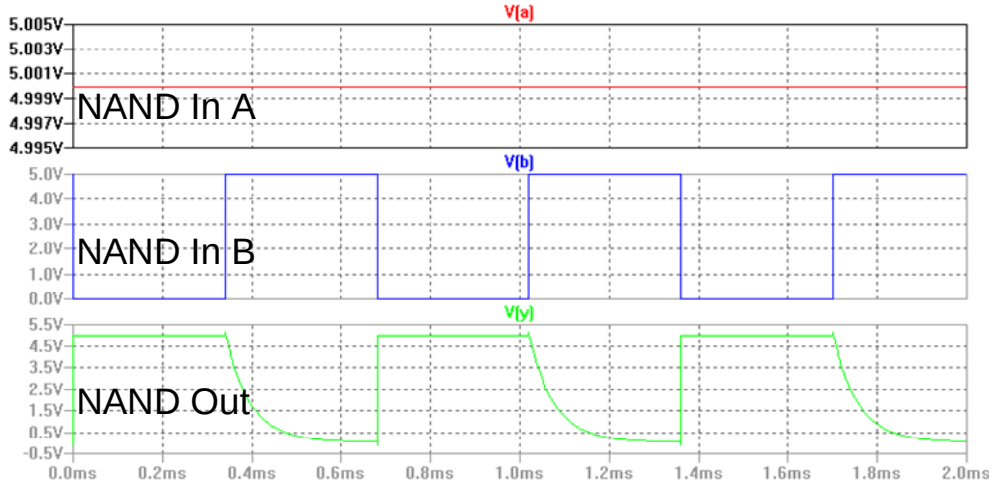


Figure 10.8 Simulation NAND gate, large resistance in NMOS structure.

Figure 10.9 shows that loading the output with a large capacitance (10nF) can also reproduce the slow fall time. The rise time of this simulation however is slower than that of the faulty circuits.

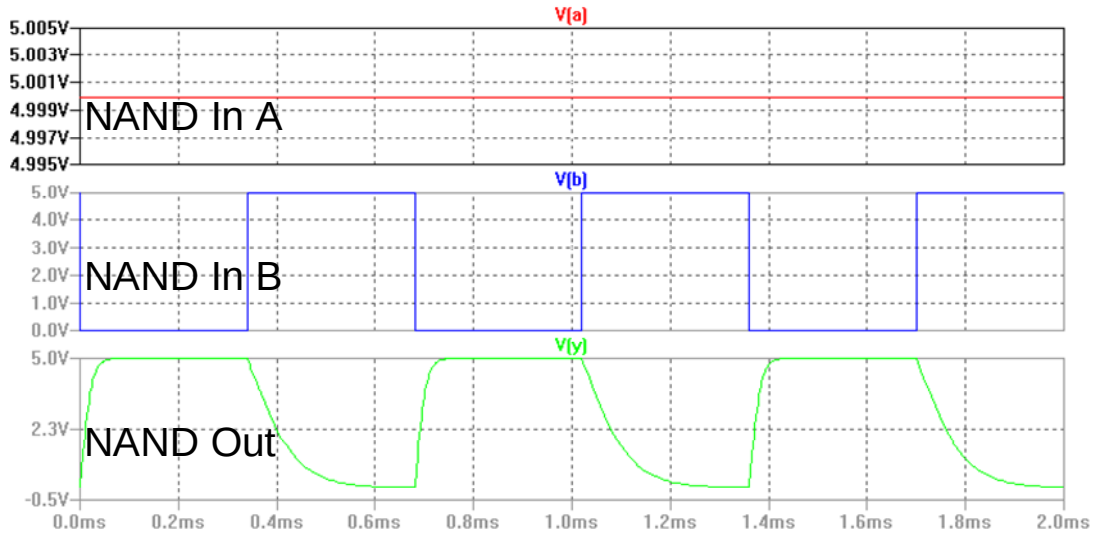


Figure 10.9 Simulation NAND gate with large capacitor on output.

In summary, simulations show that a large series resistance in the gate pulldown structure or a large capacitive load on the gate outputs could cause the slow transition times observed in Mosis ON Semiconductor C5F fabrication run V21G. Prior Mosis fabrications using the AMI 05 process did not exhibit these transition time issues.

Subsequent discussions with Mosis personnel revealed that the failing circuits were processed by ON Semiconductor with the Ami_C5F/N layer map. Previous passing circuits were processed by Ami using the Mosis SCN3M_SUMB layer map. This was traced to a menu selection error in the project request menu on the Mosis web site. There is a difference between the two layer maps at the n-plus layer. The Mosis SCN3M_SUMB layer map calls

the n-plus layer “N_PLUS_SELECT,” while the Ami_C5F/N layer map calls this mask “N_PLUS_BLOCK.” With the N_PLUS_BLOCK mask in place of N_PLUS_SELECT, there would have been no N+ implant for the NMOS source and drain. In place of the NMOS transistor we have effectively a large resistor to ground. Thus on a high to low transition, the output will drift to ground with an RC time constant. This was simulated by replacing the NMOS transistor with a 7.5Mohm resistor to ground with an 18pF load (package pin = 2pF, scope probe = 16pF). This simulation reproduces the ~284µs fall time observed on the failing units. The PMOS transistors might have been misprocessed also, receiving N+ implant where there should be none, resulting in 4µs rise time instead of expected 10-15ns. However, this could not be reproduced with spice simulations.

The two failing circuits were re-submitted for fabrication through Mosis with the correction for the Mosis SCMOS design rules. The two circuits are on the Mosis V27K ON Semiconductor fabrication run which is due at the time of this publication.

Chapter 11 Breadboard Test Results

Due to the lengthy fabrication times, the circuits described herein were prototyped on a breadboard with equivalent logic circuits and checked for functionality while waiting for the supplier to manufacture the circuits. Loop parameters used for lock time experiments were listed earlier and are repeated below. K is variable and other parameters are fixed:

f_c =62500 Hz,

f_{in}=62400 Hz or 62500 Hz,

k_d=4,

N=128,

K=2^1 through 2^{15},

Mf_c=24 MHz,

$2Nf_c$=16 MHz.

Lock time is measured by the time to reach a match on five of the seven outputs of the N counter.

11.1 Lock Time Unmodified DPLL

First, lock time measurements were taken without controller modifications. To perform measurements, the input signal is periodically inverted to take the loop out of lock as shown in Figure 11.1. Lock time is determined by comparing the latched output of the loop counter to a fixed value and measuring the time to reach a match as indicated by the comparator output. Relevant signals are

displayed on an oscilloscope for observation and data collection.

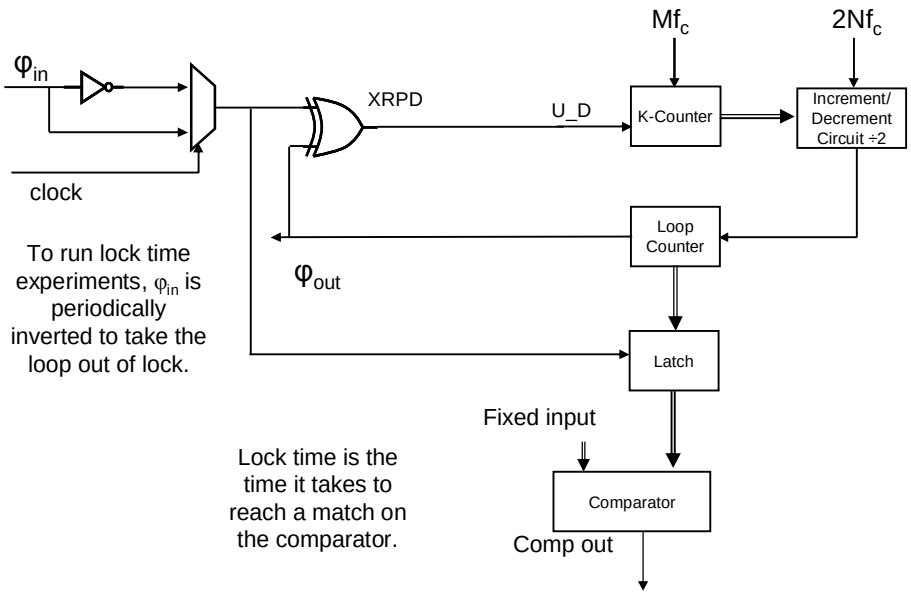


Figure 11.1 Circuit for lock time experiments, no KSM or XRPD modifications.

Using this method to measure the lock time, scope snapshots were taken of the signal waveforms and measurements taken from the scope display. The result for the case of wide lock range with a K value of 16 is shown in Figure 11.2.

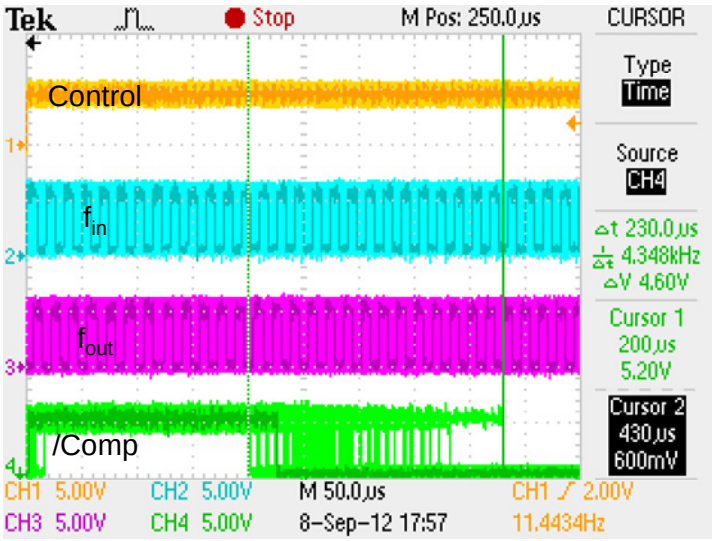


Figure 11.2 Lock time, K=16, $f_{in} \neq f_c$.

The control line to the multiplexer is clocked at a rate which will allow adequate time for the loop to lock. The comparator output goes high when the loop is taken out of lock. When a match is reached, the comparator output will transition low and the loop is considered locked. A series of lock time measurements conducted over a period of time produces a range of lock times as shown in the figure. In the example in Figure 11.2 the lock time varies over a range of 200µs to 430µs.

For the case of narrow lock range with a K value of 512, the lock time is in the range of about 4.84ms to about 5.68ms as shown in Figure 11.3. For charting results the average of the high and low values are used.

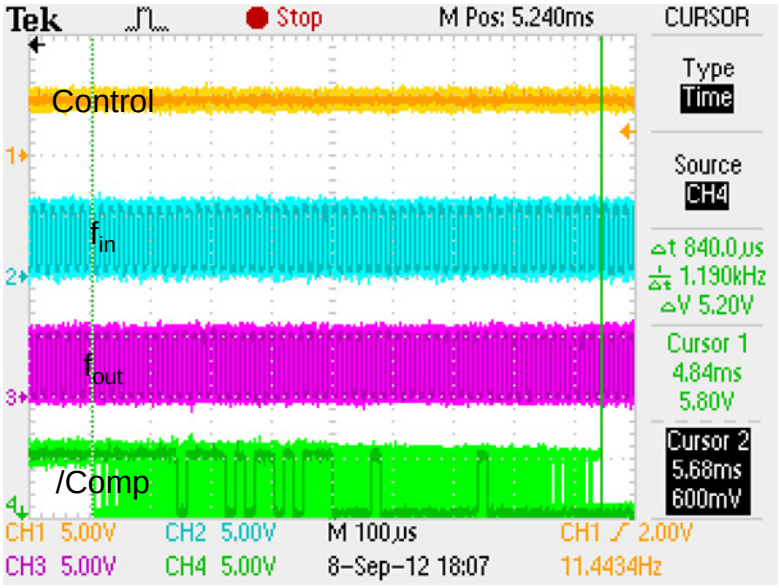


Figure 11.3 Lock time, K=512, $f_{in} \neq f_c$.

Measured lock times for various values of K are listed in Table 11.1 and charted in Figure 11.4 for the case of f_{in}=62400Hz and f_c=62500Hz. Included in

the table for each value of K are the latched 5-bit word from the N-counter and the clock delay required to latch a stable reading from the counter. Minimum and maximum lock time readings from the scope plots are listed along with the calculated average of the minimum and maximum. For values of K which are greater than 512, the input frequency of f_{in}=62400Hz is outside of the lock range of the loop, so these are not charted. Lock time increases with increasing K as expected.

Table 11.1 Measured Lock Times without Acceleration, $f_{in} \neq f_c$.

				Lock time (sec)		
K	K dcba	N43210	LatchDelay	min	max	avg
2	0001	01101	0ns	62.00E-06	188.00E-06	125.00E-06
4	0010	01101	0ns	48.00E-06	182.00E-06	115.00E-06
8	0011	11101	400ns	94.00E-06	214.00E-06	154.00E-06
16	0100	11101	0ns	218.00E-06	422.00E-06	320.00E-06
32	0101	00011	200ns	220.00E-06	940.00E-06	580.00E-06
64	0110	00011	0ns	620.00E-06	1.72E-03	1.17E-03
128	0111	10011	200ns	1.24E-03	1.96E-03	1.60E-03
256	1000	01011	200ns	2.42E-03	2.66E-03	2.54E-03
512	1001	00111	0ns	5.20E-03	5.64E-03	5.42E-03

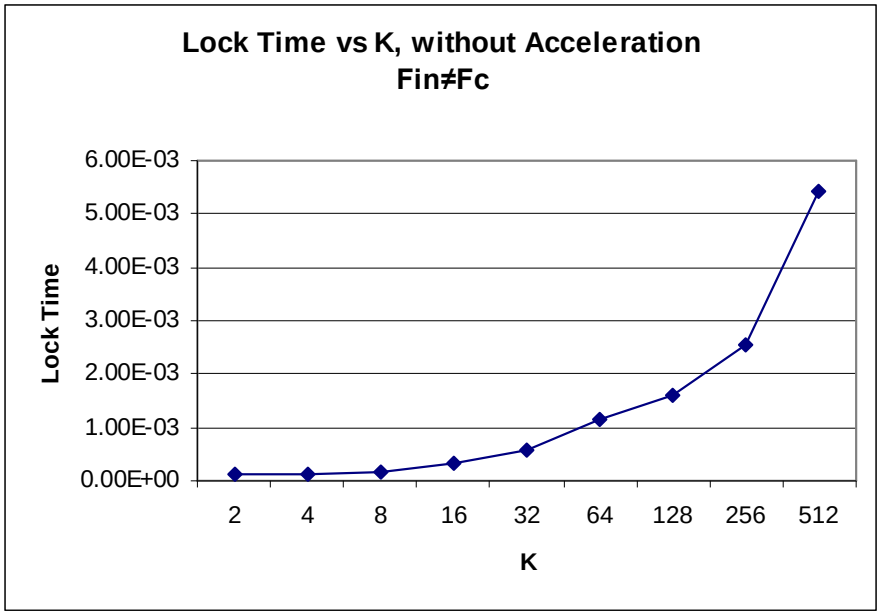


Figure 11.4 Measured Lock Time versus K w/o Acceleration, $f_{in} \neq f_c$.

Measured lock times for various values of K are listed in Table 11.2 and charted in Figure 11.5 for the case of $f_{in}=f_c=62500$Hz.

Table 11.2 Measured Lock Times without Acceleration, $f_{in}=f_c$.

				Lock time (sec)		
K	K dcba	N43210	LatchDelay	min	max	avg
2	0001	01101	0ns	62.00E-06	124.00E-06	93.00E-06
4	0010	01101	0ns	56.00E-06	228.00E-06	142.00E-06
8	0011	11101	400ns	88.00E-06	197.00E-06	142.50E-06
16	0100	11101	0ns	192.00E-06	604.00E-06	398.00E-06
32	0101	00011	400ns	310.00E-06	1.43E-03	870.00E-06
64	0110	00011	200ns	700.00E-06	2.16E-03	1.43E-03
128	0111	00011	200ns	1.98E-03	3.78E-03	2.88E-03
256	1000	00011	200ns	3.90E-03	9.90E-03	6.90E-03
512	1001	00011	200ns	10.50E-03	18.70E-03	14.60E-03
1024	1010	00011	200ns	24.00E-03	40.00E-03	32.00E-03
2048	1011	00011	200ns	39.60E-03	78.40E-03	59.00E-03
4096	1100	00011	200ns	94.40E-03	122.00E-03	108.20E-03
8192	1101	00011	200ns	206.00E-03	230.00E-03	218.00E-03
16384	1110	00011	200ns	415.00E-03	455.00E-03	435.00E-03
32768	1111	00011	200ns	848.00E-03	1.11E+00	979.00E-03

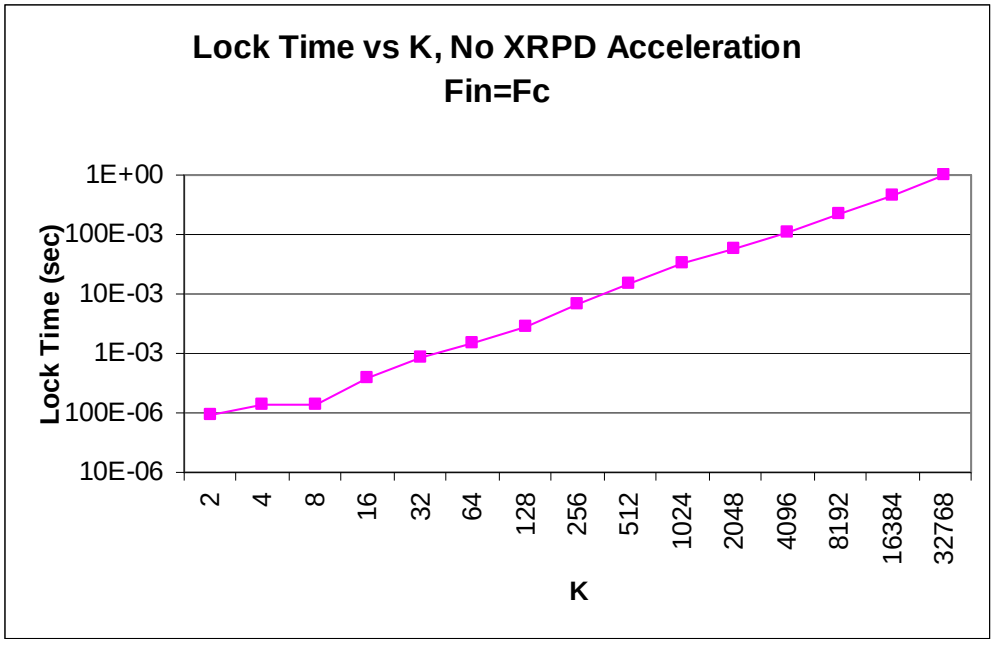


Figure 11.5 Measured Lock Time versus K w/o Acceleration, $f_{in}=f_c$.

11.2 Lock Range Time Unmodified DPLL

Also measured were the times to get into lock range of the EXOR phase detector as illustrated earlier in Figure 8.1. This can be done by latching f_{out} using the rising edge of f_{in}. This is illustrated in Figure 11.6 for the case of wide lock range with a K value of 16. The time to reach lock range is 88µs to 364µs in this figure.

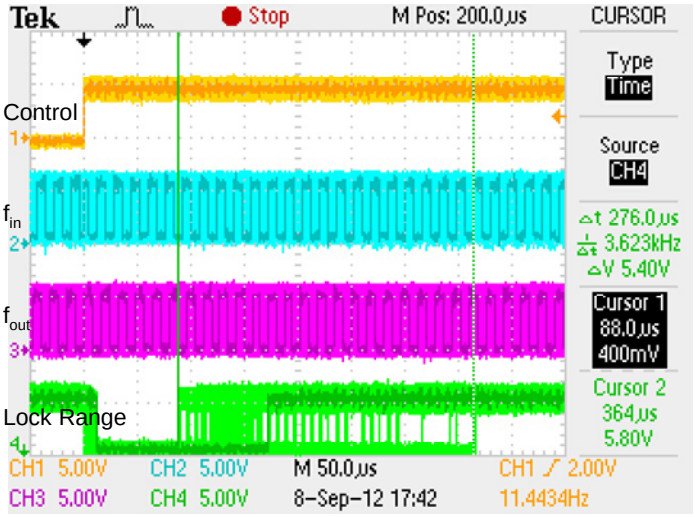


Figure 11.6 Time to reach XRPD lock range, K=16, $f_{in} \neq f_c$.

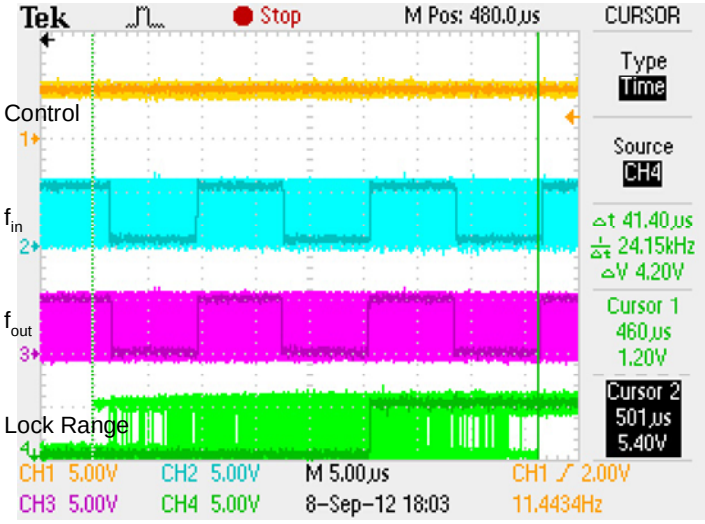


Figure 11.7 Time to reach XRPD lock range, K=512, $f_{in} \neq f_c$.

Figure 11.7 illustrates the case of narrow lock range with a K value of 512. The time to reach lock range is about 460µs to 501µs.

Measured lock range times for various values of K are listed in Table 11.3 and charted in Figure 11.8 for the case of f_{in}=62400Hz and f_c=62500Hz. Generally, the time to reach lock range increases with K. However when f_{in} is not equal to f_c, at higher values of K, the steady state phase error $\varphi_e(\infty)$ is off-center, so the time to reach lock range peaks out at K=256 then decreases at K=512.

Table 11.3 Measured Lock Range Times without Acceleration, $f_{in} \neq f_c$.

				Lock range time (sec)			Phase Error
K	K dcba	N43210	LatchDelay	min	max	avg	$\varphi_e(\infty)$
2	0001	01101	0ns	16.00E-06	117.00E-06	66.50E-06	0.25
4	0010	01101	0ns	16.00E-06	133.00E-06	74.50E-06	0.25
8	0011	11101	400ns	32.00E-06	140.00E-06	86.00E-06	0.25
16	0100	11101	0ns	96.00E-06	324.00E-06	210.00E-06	0.24
32	0101	00011	200ns	222.00E-06	506.00E-06	364.00E-06	0.24
64	0110	00011	0ns	340.00E-06	432.00E-06	386.00E-06	0.23
128	0111	10011	200ns	470.00E-06	528.00E-06	499.00E-06	0.22
256	1000	01011	200ns	572.00E-06	610.00E-06	591.00E-06	0.18
512	1001	00111	0ns	462.00E-06	502.00E-06	482.00E-06	0.11

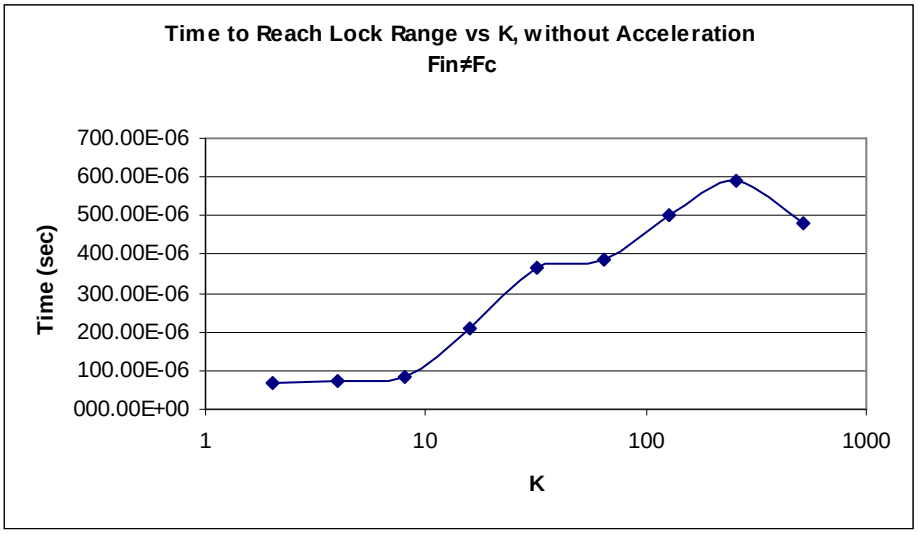


Figure 11.8 Measured lock range time versus K w/o acceleration, $f_{in} \neq f_c$.

The steady state phase error $\varphi_e(\infty)$ is illustrated for two values of K in Figure 11.9 and Figure 11.10. At a low value of K, the loop locks up with a nearly 50% duty cycle on the output of the phase detector. At a higher value of K, the duty cycle of the phase detector output deviates from 50%.

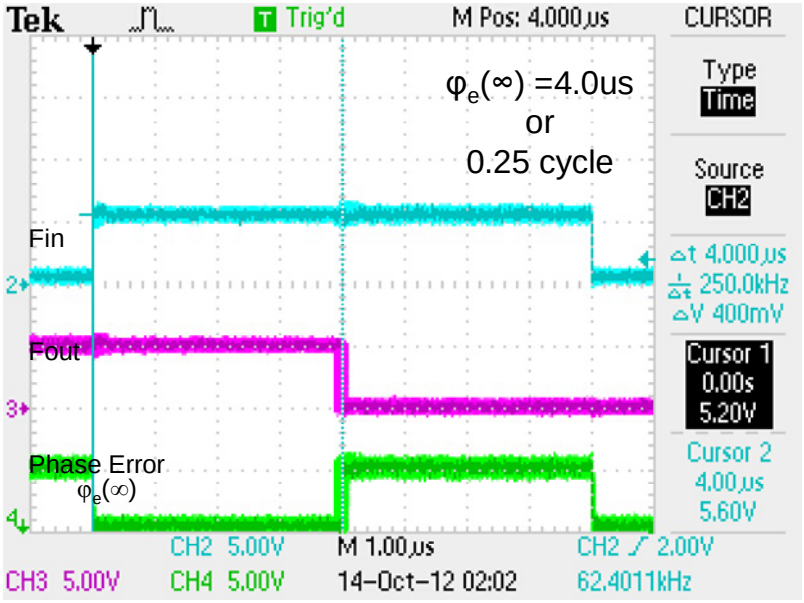


Figure 11.9 Steady state phase error for K=2, $f_{in} \neq f_c$.

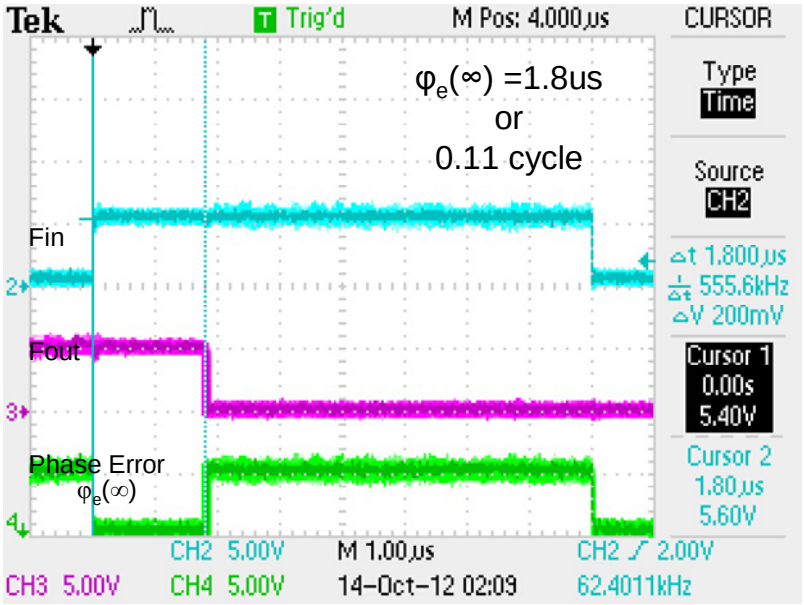


Figure 11.10 state phase error for K=512, $f_{in} \neq f_c$.

Variation of the steady state phase error $\varphi_e(\infty)$ versus K-counter modulus is charted in Figure 11.11. At low values of K, the phase error is near 0.25 cycle and the loop will have the maximum phase error to adjust when the input signal is inverted. But lock time is relatively fast at low values of K. At high values of K, the phase error is off-center and the loop will not require as much adjustment to get the loop back into lock range when the input signal is inverted. This tends to negate the effect of the higher lock times at high values of K.

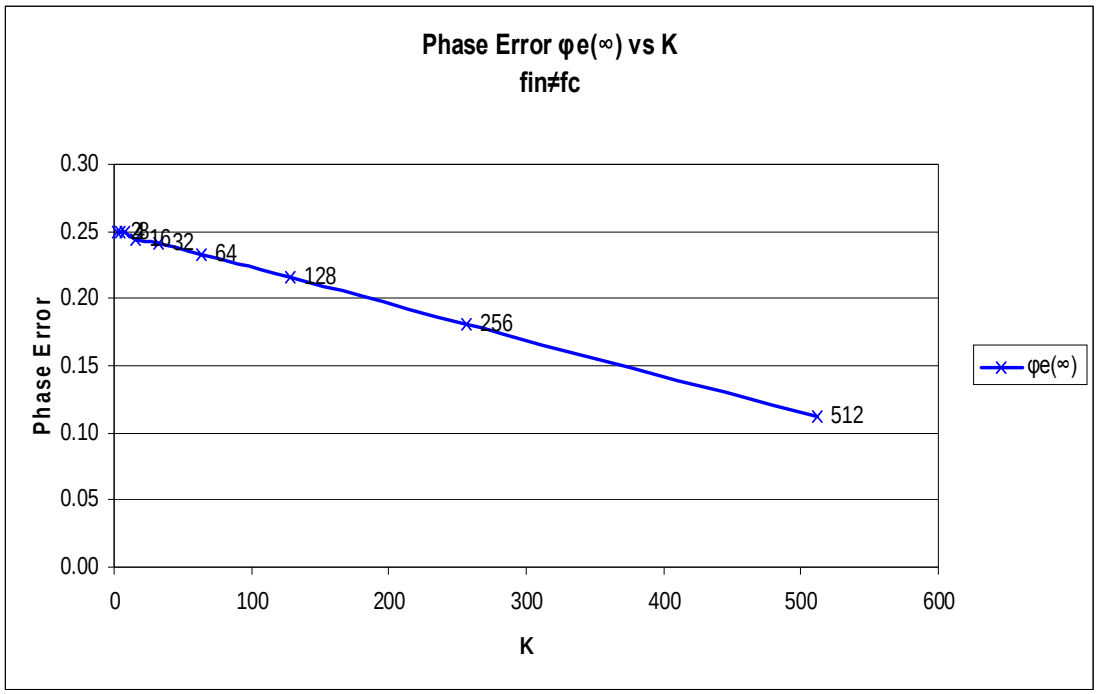


Figure 11.11 Phase Error $\varphi_e(\infty)$ versus K.

Measured lock range times for various values of K are listed in Table 11.4 and charted in Figure 11.12 for the case of $f_{in}=f_c=62500$Hz. Lock range times are longer in this case than for the case of $f_{in}\neq f_c$. The reason for this is that f_{in}/f_{out} locks up with the maximum phase error generating a 50% duty cycle on the EXOR phase detector output. When input signal is inverted to take it out of lock,

the f_{out} signal has the maximum distance to travel to get back to a locked condition.

Table 11.4 Measured Lock Range Times without Acceleration, $f_{in}=f_c$.

				Lock range time (sec)		
K	K dcba	N43210	LatchDelay	min	max	avg
2	0001	01101	0ns	23.00E-06	69.00E-06	46.00E-06
4	0010	01101	0ns	24.00E-06	125.00E-06	74.50E-06
8	0011	11101	400ns	31.00E-06	132.00E-06	81.50E-06
16	0100	11101	0ns	96.00E-06	348.00E-06	222.00E-06
32	0101	00011	400ns	212.00E-06	572.00E-06	392.00E-06
64	0110	00011	200ns	550.00E-06	1.74E-03	1.15E-03
128	0111	00011	200ns	1.24E-03	2.48E-03	1.86E-03
256	1000	00011	200ns	3.08E-03	6.28E-03	4.68E-03
512	1001	00011	200ns	6.40E-03	15.90E-03	11.15E-03
1024	1010	00011	200ns	16.20E-03	28.80E-03	22.50E-03
2048	1011	00011	200ns	21.60E-03	67.60E-03	44.60E-03
4096	1100	00011	200ns	72.00E-03	95.00E-03	83.50E-03
8192	1101	00011	200ns	145.00E-03	163.00E-03	154.00E-03
16384	1110	00011	200ns	290.00E-03	307.00E-03	298.50E-03
32768	1111	00011	200ns	390.00E-03	768.00E-03	579.00E-03

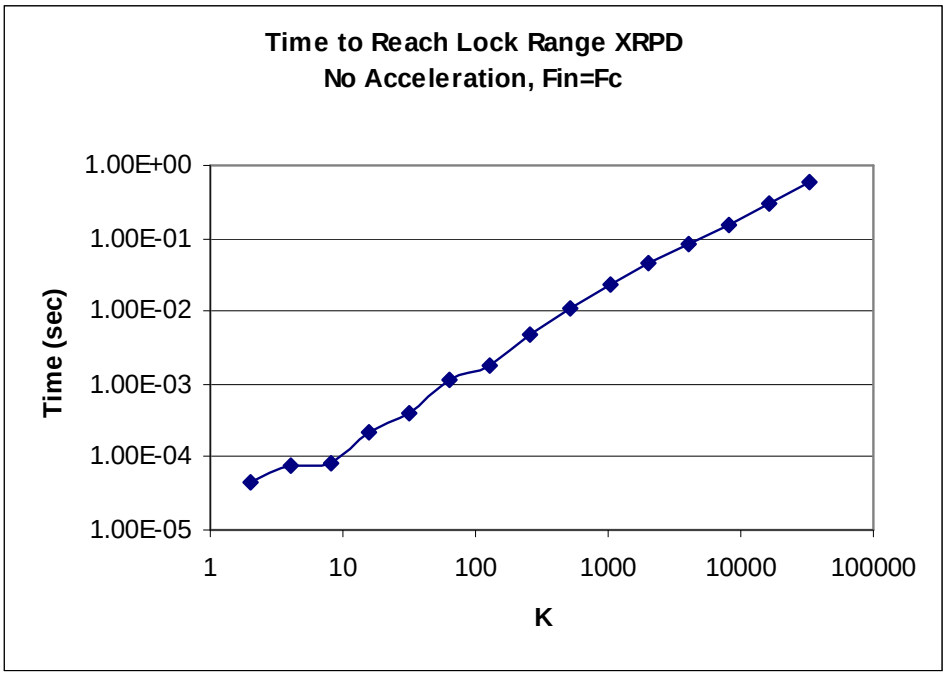


Figure 11.12 Time to reach lock range XRPD, no acceleration, $f_{in}=f_c$.

11.3 Lock Range Time with Modified XRPD

Next, the latch/mux circuit was added to the EXOR phase detector to speed up the lock time for out of lock range situations. The diagram was shown in Figure 8.6 and is repeated here in Figure 11.13. Improvement in lock time is minimal under the condition of $f_{in} \neq f_c$ because the phase error is off-center in a locked condition and not much adjustment is needed to get the f_{out} signal back in lock range when the input f_{in} is inverted.

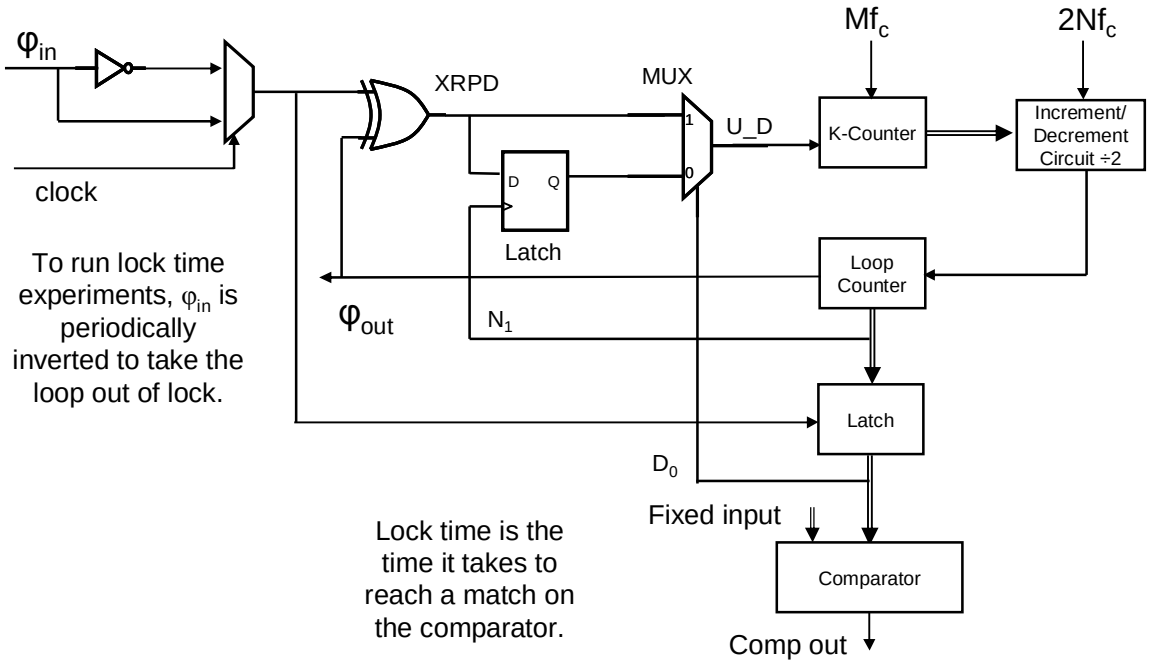


Figure 11.13 Latch/mux with XRPD phase detector to speed up lock time.

Measured lock range times with the latch/mux circuit for various values of K are listed in Table 11.5 and charted in Figure 11.14 for the case of f_{in}=62400Hz and f_c=62500Hz. The time to reach lock range reaches a peak and flattens out at K=256 and K=512. Higher values of K are out of the lock range of the loop.

Table 11.5 Lock Range Times with Acceleration, $f_{in} \neq f_c$.

				Lock range time		
K	K dcba	N43210	LatchDelay	min	max	avg
2	0001	01101	0ns	15.40E-06	33.60E-06	24.50E-06
4	0010	01101	0ns	15.40E-06	43.00E-06	29.20E-06
8	0011	11101	400ns	23.80E-06	44.00E-06	33.90E-06
16	0100	11101	0ns	44.60E-06	60.40E-06	52.50E-06
32	0101	00011	200ns	82.00E-06	106.00E-06	94.00E-06
64	0110	00011	0ns	149.00E-06	177.00E-06	163.00E-06
128	0111	10011	200ns	259.00E-06	289.00E-06	274.00E-06
256	1000	01011	200ns	386.00E-06	418.00E-06	402.00E-06
512	1001	00111	0ns	389.00E-06	426.00E-06	407.50E-06

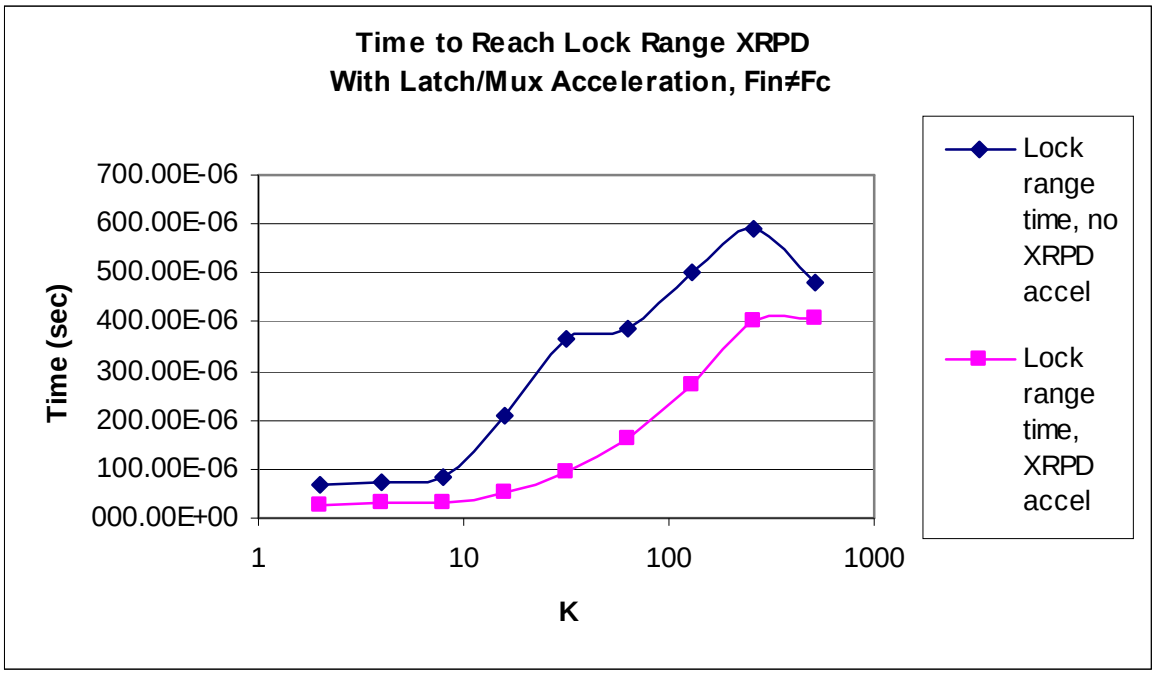


Figure 11.14 Lock range time with latch/mux acceleration, $f_{in} \neq f_{out}$.

Measured lock range times with the latch/mux circuit for various values of K are listed in Table 11.6 and charted in Figure 11.15 for the case of $f_{in}=f_c=62500$Hz. The improvement in the time it takes to get into lock range is substantial at all values of K.

Table 11.6 Lock Range Times with Acceleration, $f_{in}=f_c$.

				Lock range time (sec)		
K	K dcba	N43210	LatchDelay	min	max	avg
2	0001	01101	0ns	16.00E-06	34.40E-06	25.20E-06
4	0010	01101	0ns	16.00E-06	43.60E-06	29.80E-06
8	0011	11101	400ns	20.40E-06	44.80E-06	32.60E-06
16	0100	11101	0ns	43.60E-06	59.60E-06	51.60E-06
32	0101	00011	400ns	77.00E-06	106.00E-06	91.50E-06
64	0110	00011	200ns	164.00E-06	201.00E-06	182.50E-06
128	0111	00011	200ns	344.00E-06	369.00E-06	356.50E-06
256	1000	00011	200ns	654.00E-06	704.00E-06	679.00E-06
512	1001	00011	200ns	1.30E-03	1.34E-03	1.32E-03
1024	1010	00011	200ns	2.59E-03	2.66E-03	2.63E-03
2048	1011	00011	200ns	5.15E-03	5.23E-03	5.19E-03
4096	1100	00011	200ns	10.30E-03	10.40E-03	10.35E-03
8192	1101	00011	200ns	21.80E-03	22.20E-03	22.00E-03
16384	1110	00011	200ns	33.60E-03	33.90E-03	33.75E-03
32768	1111	00011	200ns	41.50E-03	42.70E-03	42.10E-03

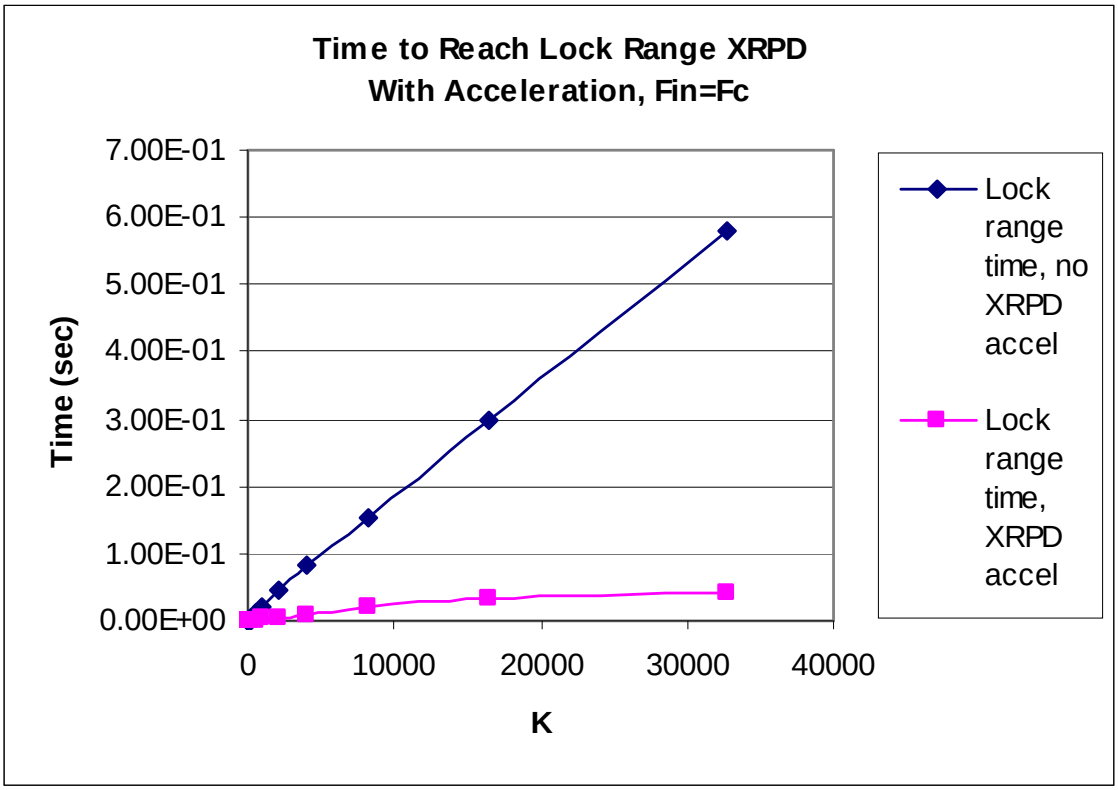


Figure 11.15 Lock Range Times with/without Acceleration, $f_{in}=f_c$.

11.4 Lock Time with Modified XRPD

Measured lock times with the latch/mux lock time acceleration circuit for various values of K are listed in Table 11.7 and charted in Figure 11.16 for the case of f_{in}=62400Hz and f_c=62500Hz. For comparison, graphs of lock time are shown with and without the XRPD acceleration in Figure 11.16. The graph shows marginal improvement in lock time with the phase detector modifications.

Table 11.7 Measured Lock Times with Acceleration, $f_{in} \neq f_c$.

				Lock time, with XRPD acceleration		
K	K dcba	N43210	LatchDelay	min	max	avg
2	0001	01101	0ns	28.40E-06	100.00E-06	64.20E-06
4	0010	01101	0ns	27.00E-06	130.00E-06	78.50E-06
8	0011	11101	400ns	60.40E-06	122.00E-06	91.20E-06
16	0100	11101	0ns	147.00E-06	201.00E-06	174.00E-06
32	0101	00011	200ns	172.00E-06	824.00E-06	498.00E-06
64	0110	00011	0ns	540.00E-06	1.10E-03	820.00E-06
128	0111	10011	200ns	1.15E-03	2.07E-03	1.61E-03
256	1000	01011	200ns	2.07E-03	2.49E-03	2.28E-03
512	1001	00111	0ns	4.74E-03	5.58E-03	5.16E-03

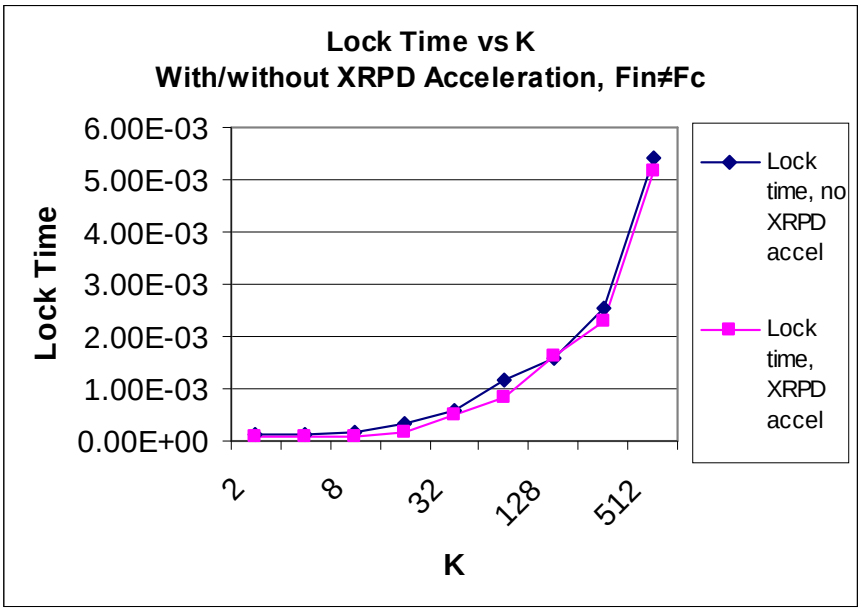


Figure 11.16 Measured lock times with/without XRPD acceleration, $f_{in} \neq f_c$.

To better visualize of the lock time improvement with the XRPD latch/mux circuit, delta lock times were calculated with and without the phase detector modification. These are listed in Table 11.8 in both absolute and percent change. Figure 11.17 illustrates the delta time in units of seconds and Figure 11.18 illustrates the improvement in lock times as a delta percent. The percent improvement is in the 40-50% range at low values of K and diminishes at higher values of K.

Table 11.8 Delta Lock Times with XRPD Acceleration, $f_{in} \neq f_c$.

				Lock Time Delta Improvement	
K	K dcba	N43210	LatchDelay	Δ	% Δ
2	0001	01101	0ns	60.80E-06	48.6%
4	0010	01101	0ns	36.50E-06	31.7%
8	0011	11101	400ns	62.80E-06	40.8%
16	0100	11101	0ns	146.00E-06	45.6%
32	0101	00011	200ns	82.00E-06	14.1%
64	0110	00011	0ns	350.00E-06	29.9%
128	0111	00011	200ns	-10.00E-06	-0.6%
256	1000	00011	200ns	260.00E-06	10.2%
512	1001	00011	0ns	260.00E-06	4.8%

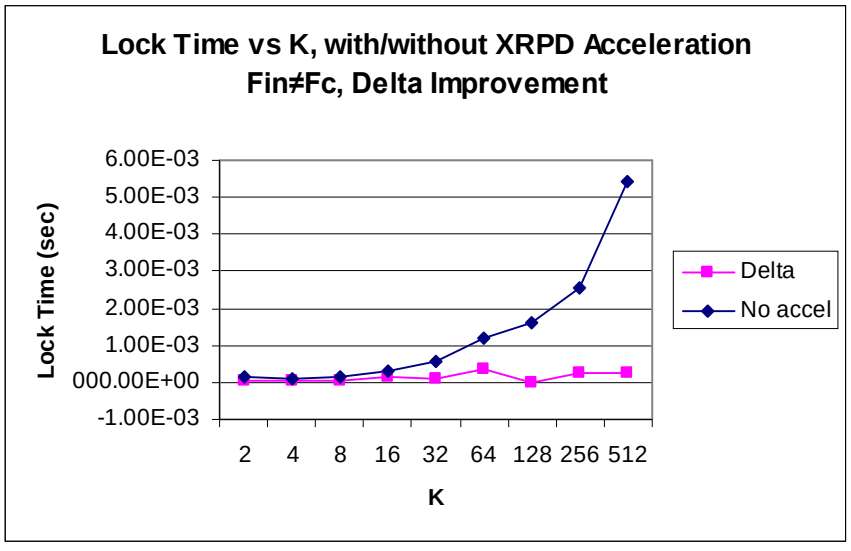


Figure 11.17 Delta lock range times with XRPD acceleration, $f_{in} \neq f_c$.

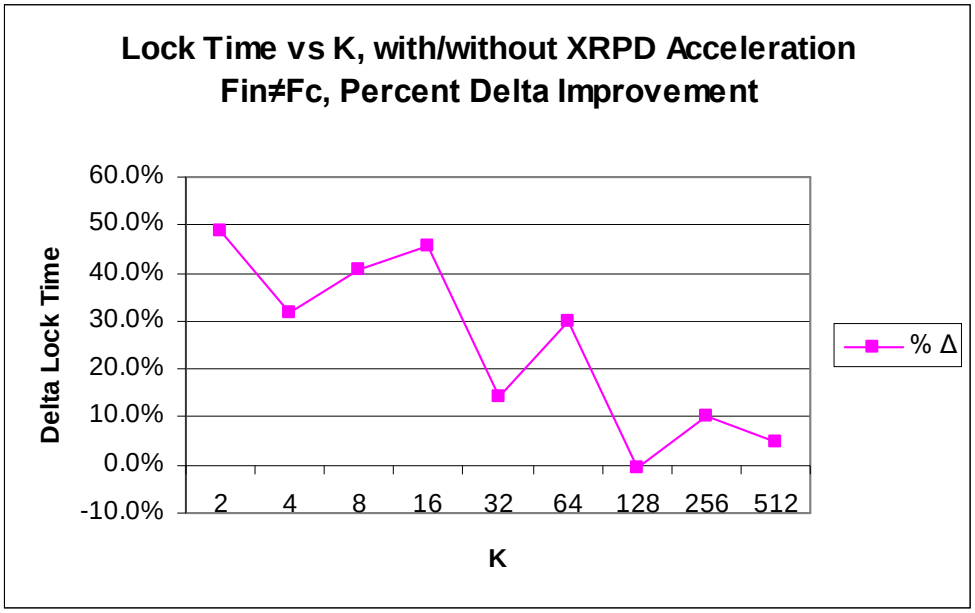


Figure 11.18 Percent delta lock range time improvement with XRPD acceleration, $f_{in} \neq f_c$.

Measured lock times with the latch/mux circuit for various values of K are listed in Table 11.9 and charted in Figure 11.19 for the case of $f_{in}=f_c=62500$Hz. The time to reach lock range is substantially better with the acceleration circuit.

Table 11.9 Measured Lock Times with Acceleration, $f_{in}=f_c$.

				Lock time (sec)		
K	K dcba	N43210	LatchDelay	min	max	avg
2	0001	01101	0ns	28.40E-06	83.20E-06	55.80E-06
4	0010	01101	0ns	28.00E-06	91.00E-06	59.50E-06
8	0011	11101	400ns	67.00E-06	108.00E-06	87.50E-06
16	0100	11101	0ns	156.00E-06	191.00E-06	173.50E-06
32	0101	00011	400ns	276.00E-06	442.00E-06	359.00E-06
64	0110	00011	200ns	592.00E-06	764.00E-06	678.00E-06
128	0111	00011	200ns	1.20E-03	1.47E-03	1.34E-03
256	1000	00011	200ns	2.50E-03	2.69E-03	2.60E-03
512	1001	00011	200ns	4.96E-03	5.39E-03	5.18E-03
1024	1010	00011	200ns	9.86E-03	10.80E-03	10.33E-03
2048	1011	00011	200ns	19.70E-03	21.60E-03	20.65E-03
4096	1100	00011	200ns	39.70E-03	42.90E-03	41.30E-03
8192	1101	00011	200ns	79.00E-03	86.30E-03	82.65E-03
16384	1110	00011	200ns	157.00E-03	172.00E-03	164.50E-03
32768	1111	00011	200ns	316.00E-03	343.00E-03	329.50E-03

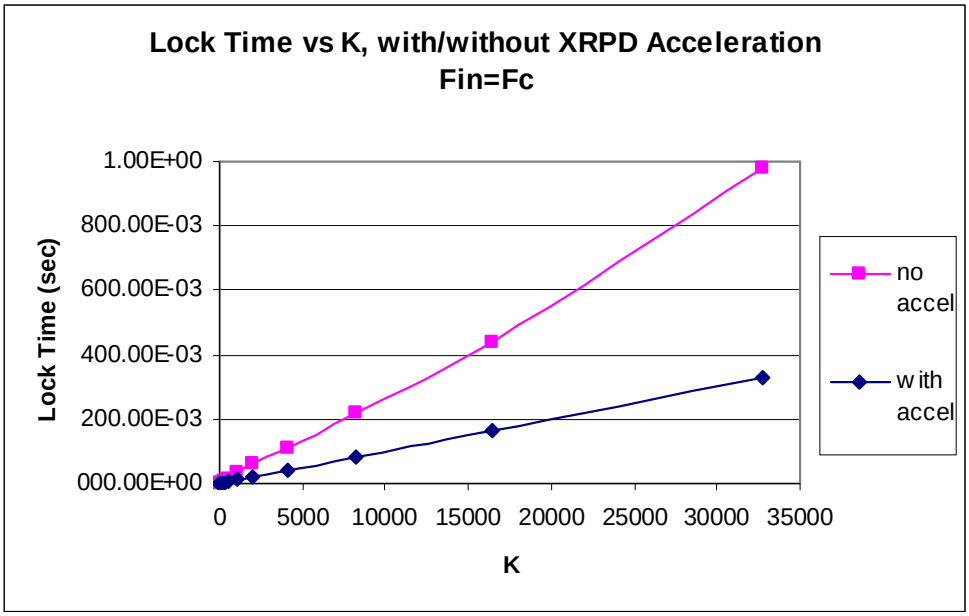


Figure 11.19 Measured lock times with/without acceleration, $f_{in}=f_c$.

For the case of $f_{in}=f_c$ with the XRPD acceleration circuit, the delta lock times are listed in Table 11.10. Figure 11.20 illustrates the delta percent improvement in lock times versus K. The percent improvement is in the 40-65% range over all values of K.

Table 11.10 Delta lock times with XRPD acceleration, $f_{in}=f_c$.

K	K dcba	N43210	LatchDelay	Δ	% Δ
2	0001	01101	0ns	37.20E-06	40.0%
4	0010	01101	0ns	82.50E-06	58.1%
8	0011	11101	400ns	55.00E-06	38.6%
16	0100	11101	0ns	224.50E-06	56.4%
32	0101	00011	400ns	511.00E-06	58.7%
64	0110	00011	200ns	752.00E-06	52.6%
128	0111	00011	200ns	1.55E-03	53.6%
256	1000	00011	200ns	4.31E-03	62.4%
512	1001	00011	200ns	9.43E-03	64.6%
1024	1010	00011	200ns	21.67E-03	67.7%
2048	1011	00011	200ns	38.35E-03	65.0%
4096	1100	00011	200ns	66.90E-03	61.8%
8192	1101	00011	200ns	135.35E-03	62.1%
16384	1110	00011	200ns	270.50E-03	62.2%
32768	1111	00011	200ns	649.50E-03	66.3%

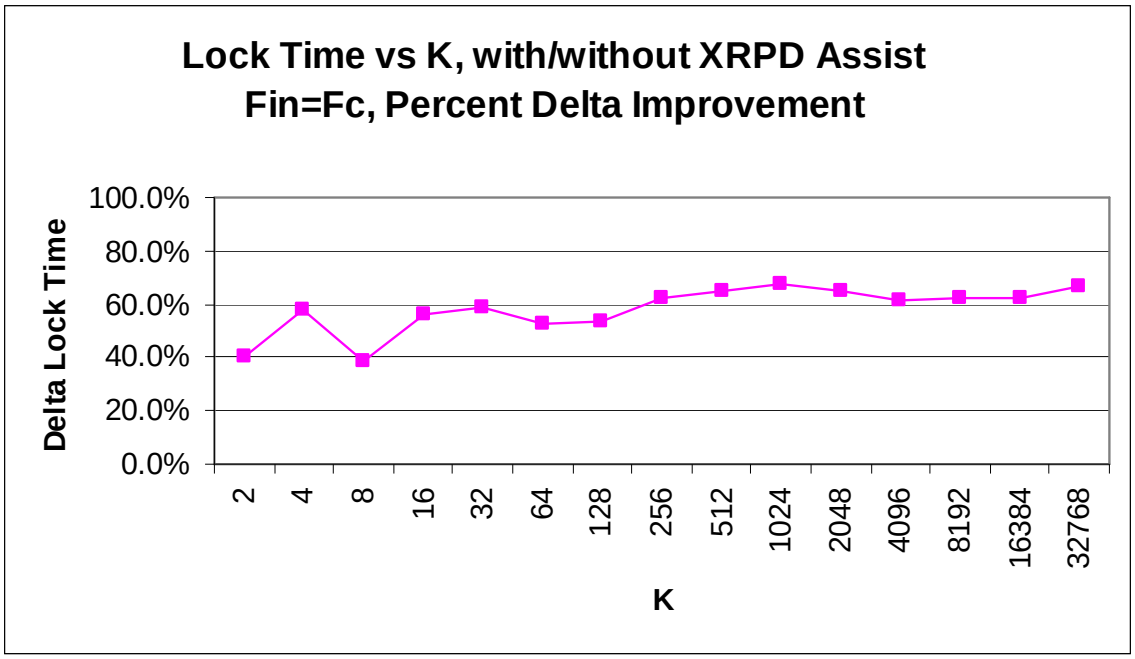


Figure 11.20 Percent delta lock time improvement with XRPD acceleration, $f_{in}=f_c$.

11.5 Lock Time with K State Machine Controller Circuit

The next breadboard experiment was evaluation and checkout of the state machine circuit. This was done for two values of K. For the case of $f_{in}=f_c$, the final phase error in a locked state is always 0.25 cycle which produces a duty cycle of 50% at the output of the EXOR phase detector. Due to this, the latched value of the N-counter will be the same for both the locked-wide and locked-narrow condition. This in effect simplifies the state machine from four states to three: unlocked, locked, and reset.

Two sets of data were collected. Data was collected with K1 fixed and K2 varying, and a second set of data was collected with K2 fixed and K1 varying. Data was collected for K values of 64 through 32768. This simplified the data

collection because a latch delay of 200ns could be used for all of the measurements. Data for K2 varying and K1 Fixed at 64 is listed in Table 11.11 and charted in Figure 11.21. Data for K1 varying and K2 Fixed at 32768 is listed in Table 11.12 and charted in Figure 11.22.

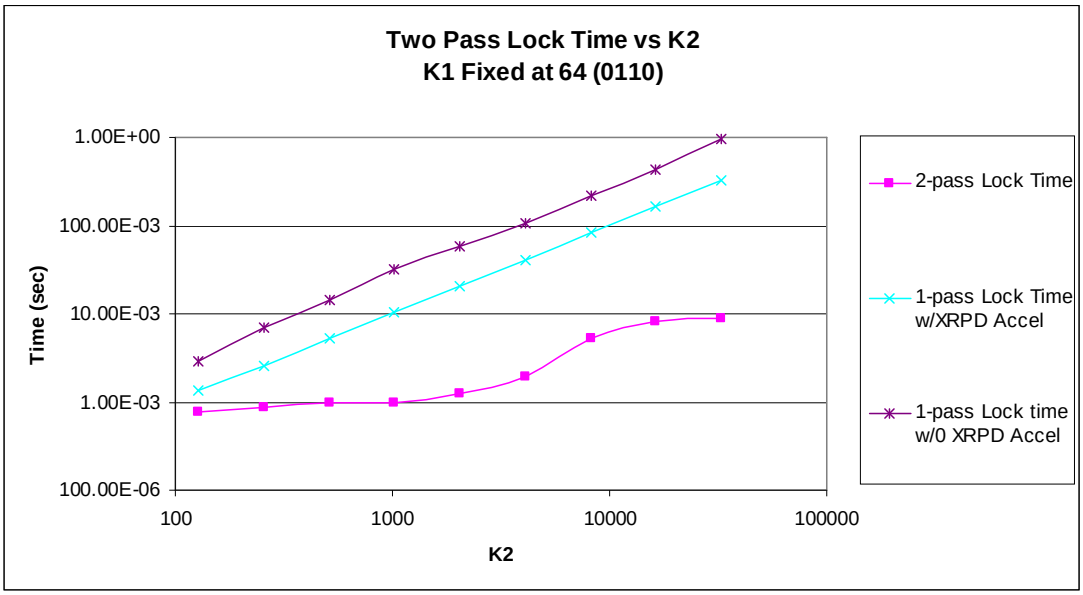


Figure 11.21 Two Pass Lock Time versus K2, K1 Fixed at 64 (0110).

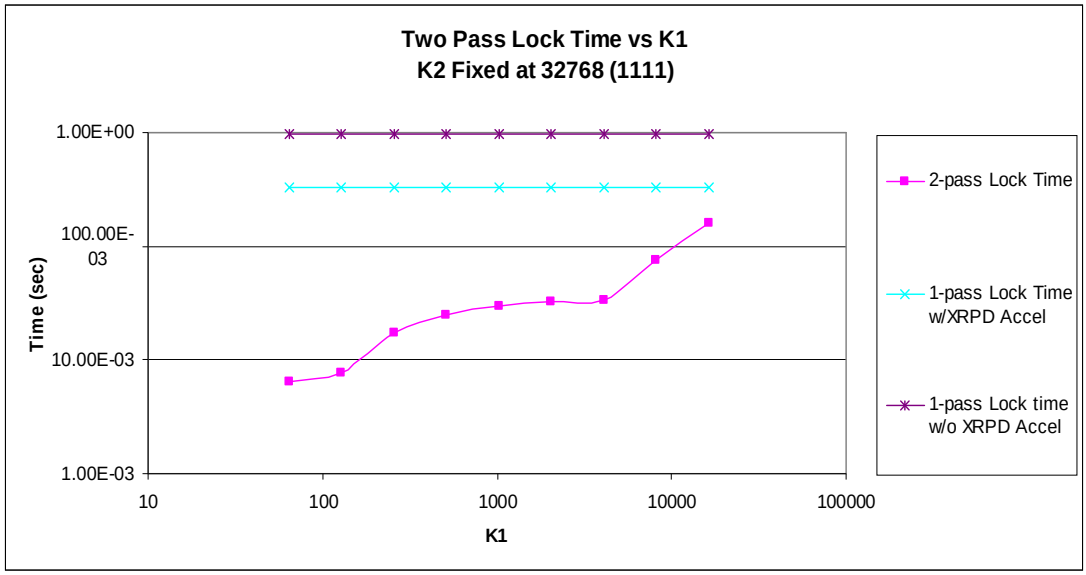


Figure 11.22 Two Pass Lock Time versus K1, K2 Fixed at 32768 (1111).

Table 11.11 Two Pass Lock Time versus K2, K1 Fixed at 64 (0110).

K1	K1 dcba	K2	K2 dcba	N-wide	N-narrow	LatchDelay	2-pass Time to Lock Range	2-pass Lock Time	1-pass Time to Lock Range with XRPD Accel.	1-pass Lock Time with XRPD Accel.	1-pass Lock Time, No XRPD Accel.
64	0110	128	0111	00011	00011	200ns/200ns	254.00E-06	780.00E-06	356.50E-06	1.34E-03	2.88E-03
64	0110	256	1000	00011	00011	200ns/200ns	254.00E-06	870.00E-06	679.00E-06	2.60E-03	6.90E-03
64	0110	512	1001	00011	00011	200ns/200ns	254.00E-06	965.00E-06	1.32E-03	5.18E-03	14.60E-03
64	0110	1024	1010	00011	00011	200ns/200ns	254.00E-06	985.00E-06	2.63E-03	10.33E-03	32.00E-03
64	0110	2048	1011	00011	00011	200ns/200ns	254.00E-06	1.23E-03	5.19E-03	20.65E-03	59.00E-03
64	0110	4096	1100	00011	00011	200ns/200ns	254.00E-06	1.91E-03	10.35E-03	41.30E-03	108.20E-03
64	0110	8192	1101	00011	00011	200ns/200ns	254.00E-06	5.20E-03	22.00E-03	82.65E-03	218.00E-03
64	0110	16384	1110	00011	00011	200ns/200ns	254.00E-06	8.30E-03	33.75E-03	164.50E-03	435.00E-03
64	0110	32768	1111	00011	00011	200ns/200ns	254.00E-06	9.00E-03	42.10E-03	329.50E-03	979.00E-03

Table 11.12 Two Pass Lock Time versus K1, K2 Fixed at 32768 (1111).

K1	K1 dcba	K2	K2 dcba	N-wide	N-narrow	LatchDelay	2-pass Time to Lock Range	2-pass Lock Time	1-pass Time to Lock Range with XRPD Accel.	1-pass Lock Time with XRPD Accel.	1-pass Lock Time, No XRPD Accel.
64	0110	32768	1111	00011	00011	200ns/200ns	261.50E-06	6.35E-03	182.50E-06	329.50E-03	979.00E-03
128	0111	32768	1111	00011	00011	200ns/200ns	428.00E-06	7.80E-03	356.50E-06	329.50E-03	979.00E-03
256	1000	32768	1111	00011	00011	200ns/200ns	760.00E-06	17.20E-03	679.00E-06	329.50E-03	979.00E-03
512	1001	32768	1111	00011	00011	200ns/200ns	1.35E-03	24.60E-03	1.32E-03	329.50E-03	979.00E-03
1024	1010	32768	1111	00011	00011	200ns/200ns	2.91E-03	29.40E-03	2.63E-03	329.50E-03	979.00E-03
2048	1011	32768	1111	00011	00011	200ns/200ns	5.49E-03	33.00E-03	5.19E-03	329.50E-03	979.00E-03
4096	1100	32768	1111	00011	00011	200ns/200ns	11.00E-03	34.00E-03	10.35E-03	329.50E-03	979.00E-03
8192	1101	32768	1111	00011	00011	200ns/200ns	21.85E-03	76.50E-03	22.00E-03	329.50E-03	979.00E-03
16384	1110	32768	1111	00011	00011	200ns/200ns	43.20E-03	161.00E-03	33.75E-03	329.50E-03	979.00E-03

For the previous set of data, delta lock times were calculated and are listed in Table 11.13 and Table 11.14. The percentage improvement in lock time is charted in Figure 11.23 and Figure 11.24. The combination of the XRPD latch/mux acceleration circuit and the state machine circuit produces lock time improvements in excess of 90% for higher values of K.

Table 11.13 Delta Lock Time, $f_{in}=f_c$, K2 Varying, K1 Fixed at 64.
Two Pass Lock Time to One Pass Lock Time.

K2	Δ Lock Time 1-pass Accel to 2-pass	% Δ Lock Time 1-pass Accel to 2-pass	Δ Lock Time 1-pass No Accel to 2-pass	% Δ Lock Time 1-pass No Accel to 2-pass
128	555.00E-06	41.57%	2.10E-03	72.92%
256	1.73E-03	66.47%	6.03E-03	87.39%
512	4.21E-03	81.35%	13.64E-03	93.39%
1024	9.35E-03	90.46%	31.02E-03	96.92%
2048	19.43E-03	94.07%	57.78E-03	97.92%
4096	39.39E-03	95.38%	106.29E-03	98.23%
8192	77.45E-03	93.71%	212.80E-03	97.61%
16384	156.20E-03	94.95%	426.70E-03	98.09%
32768	320.50E-03	97.27%	970.00E-03	99.08%

Table 11.14 Delta Lock Time, $f_{in}=f_c$, K1 Varying, K2 Fixed at 32768.
Two Pass Lock Time to One Pass Lock Time.

K1	Δ Lock Time 1-pass Accel to 2-pass	% Δ Lock Time 1-pass Accel to 2-pass	Δ Lock Time 1-pass No Accel to 2-pass	% Δ Lock Time 1-pass No Accel to 2-pass
64	323.15E-03	98.07%	972.65E-03	99.35%
128	321.70E-03	97.63%	971.20E-03	99.20%
256	312.30E-03	94.78%	961.80E-03	98.24%
512	304.90E-03	92.53%	954.40E-03	97.49%
1024	300.10E-03	91.08%	949.60E-03	97.00%
2048	296.50E-03	89.98%	946.00E-03	96.63%
4096	295.50E-03	89.68%	945.00E-03	96.53%
8192	253.00E-03	76.78%	902.50E-03	92.19%
16384	168.50E-03	51.14%	818.00E-03	83.55%

For the next breadboard experiment lock times were evaluated for the case of $f_{in}\neq f_c$. As with the case of $f_{in}=f_c$, two sets of data were collected: one set of data with K1 fixed and K2 varying, and a second set of data with K2 fixed and

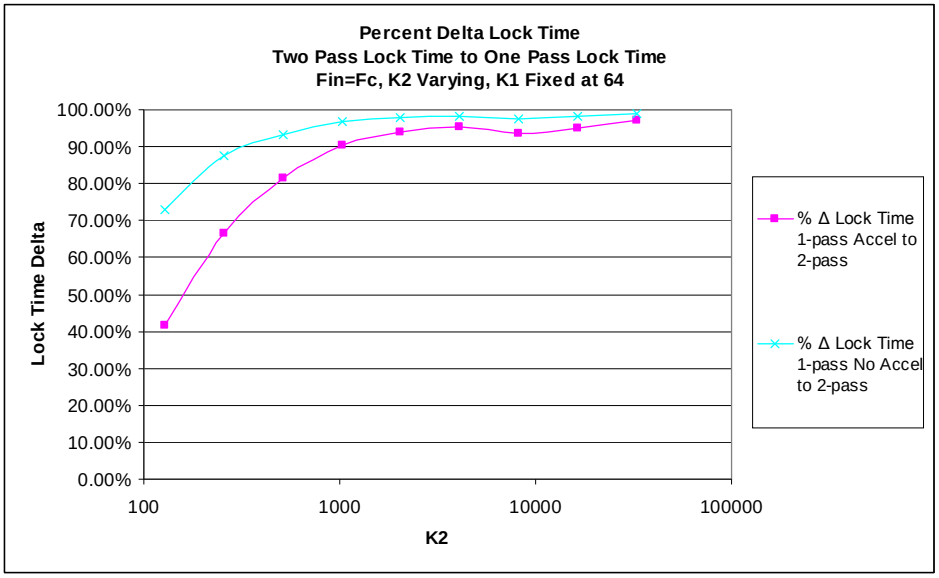


Figure 11.23 Percent delta lock time, 2-pass lock time to 1-pass lock time, $f_{in}=f_c$, K2 varying, K1 fixed.

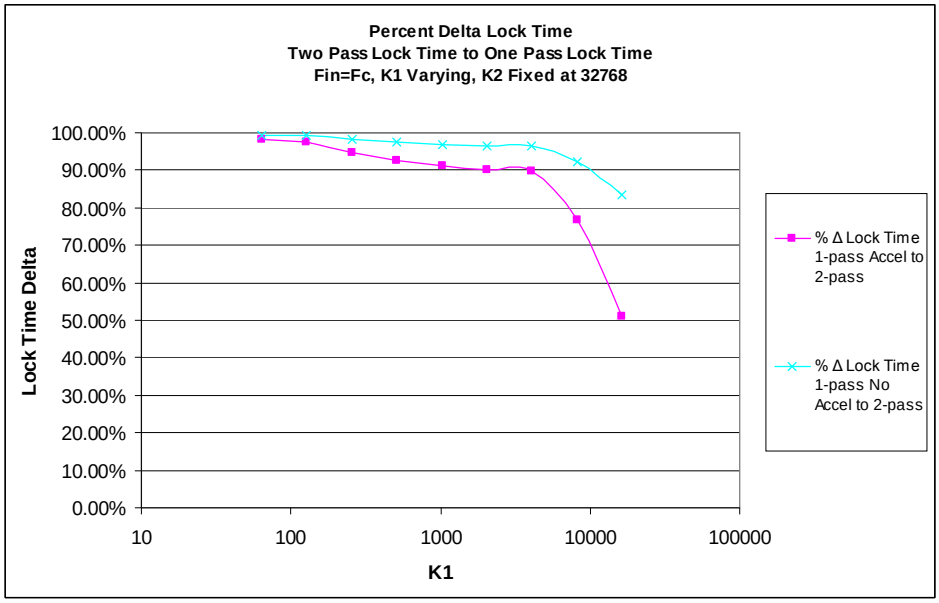


Figure 11.24 Percent delta lock time 2-pass lock time to 1-pass lock time, $f_{in}=f_c$, K1 varying, K2 fixed.

K1 varying. To simplify the data collection, data was collected for K values of 2, 4, 16, 64, and 512 because a latch delay of 0ns could be used for all of the measurements. Data for K1 varying and K2 Fixed at 32768 is listed in Table

11.15 and charted in Figure 11.25. Data for K2 varying and K1 Fixed at 64 is listed in Table 11.16 and charted in Figure 11.26.

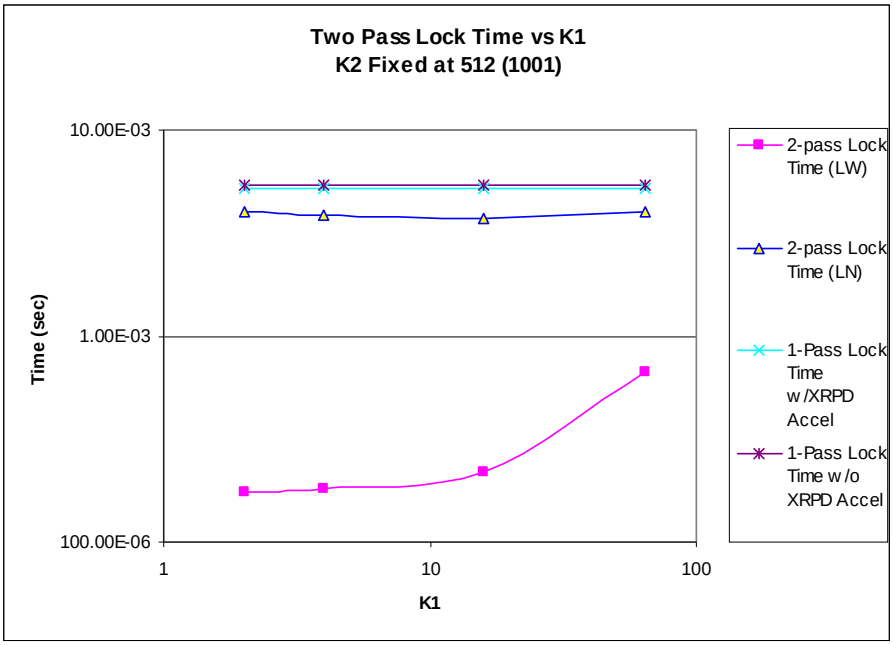


Figure 11.25 Two Pass Lock Time versus K1, K2 Fixed at 512 (1001), $f_{in} \neq f_c$.

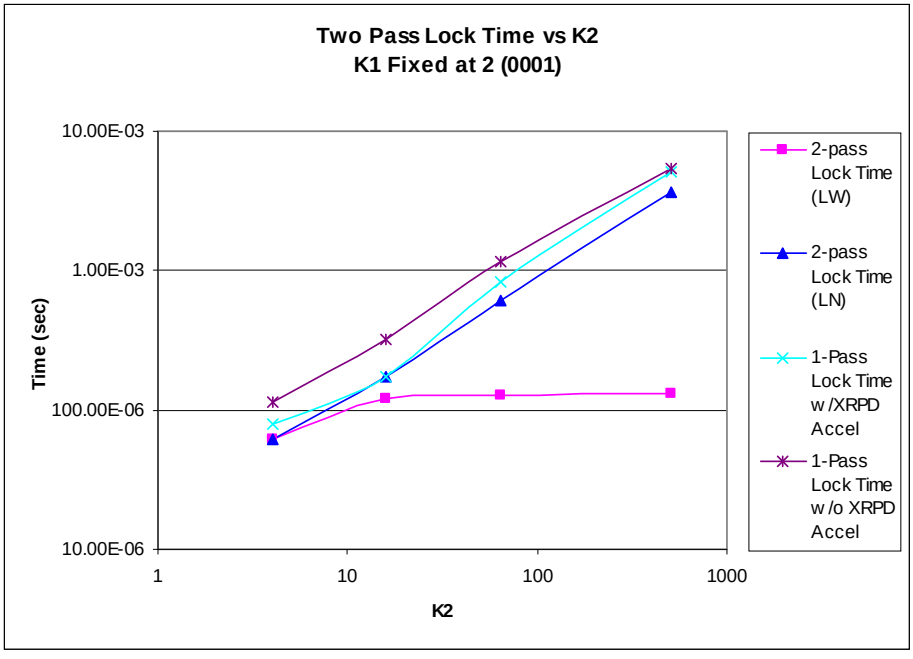


Figure 11.26 Two pass lock time versus K2, K1 fixed at 2 (0001), $f_{in} \neq f_c$.

Table 11.15 Two Pass Lock Time versus K1, K2 Fixed at 512, $f_{in} \neq f_c$.

K1	K1 dcba	K2	K2 dcba	N-wide	N-narrow	LatchDelay	2-pass Time to LR	2-pass Lock Time (LW)	2-pass Lock Time (LN)	1-pass Lock Time with XRPD Accel.	1-pass Lock Time, No XRPD Accel.
2	0001	512	1001	01101	00111	0ns/0ns	100.40E-06	176.50E-06	3.98E-03	5.16E-03	5.42E-03
4	0010	512	1001	01101	00111	0ns/0ns	101.10E-06	181.00E-06	3.90E-03	5.16E-03	5.42E-03
16	0100	512	1001	11101	00111	0ns/0ns	108.00E-06	218.00E-06	3.73E-03	5.16E-03	5.42E-03
64	0110	512	1001	00011	00111	0ns/0ns	151.50E-06	675.00E-06	4.01E-03	5.16E-03	5.42E-03

Table 11.16 Two Pass Lock Time versus K2, K1 Fixed at 2, $f_{in} \neq f_c$.

K1	K1 dcba	K2	K2 dcba	N-wide	N-narrow	LatchDelay	2-pass Time to LR	2-pass Lock Time (LW)	2-pass Lock Time (LN)	1-pass Lock Time with XRPD Accel.	1-pass Lock Time, No XRPD Accel.
2	0001	4	0010	01101	01101	0ns/0ns	28.60E-06	62.20E-06	62.20E-06	78.50E-06	115.00E-06
2	0001	16	0100	01101	11101	0ns/0ns	52.00E-06	120.00E-06	171.50E-06	174.00E-06	320.00E-06
2	0001	64	0110	01101	00011	0ns/0ns	100.20E-06	128.00E-06	610.00E-06	820.00E-06	1.17E-03
2	0001	512	1001	01101	00111	0ns/0ns	99.10E-06	132.00E-06	3.71E-03	5.16E-03	5.42E-03

Table 11.17 Two Pass Lock Time Delta versus K1, K2 Fixed at 512, $f_{in} \neq f_c$.

K1	2-pass Lock Time (LN)	1-pass Lock Time with XRPD Accel.	1-pass Lock Time, No XRPD Accel.	Delta LT 1-pass xa to 1pass nxa	% Delta LT 1-pass xa to 1pass nxa	xrpd accel	Delta LT 2-pass to 1-pass nxa	%Delta LT 2-pass to 1-pass nxa
2	3.98E-03	5.16E-03	5.42E-03	260.00E-06	4.80%	n	1.45E-03	26.66%
4	3.90E-03	5.16E-03	5.42E-03	260.00E-06	4.80%	n	1.52E-03	28.04%
16	3.73E-03	5.16E-03	5.42E-03	260.00E-06	4.80%	y	1.70E-03	31.27%
64	4.01E-03	5.16E-03	5.42E-03	260.00E-06	4.80%	y	1.41E-03	26.01%

Table 11.18 Two Pass Lock Time Delta versus K2, K1 Fixed at 2, $f_{in} \neq f_c$.

K2	2-pass Lock Time (LN)	1-pass Lock Time with XRPD Accel.	1-pass Lock Time, No XRPD Accel.	Delta LT 1-pass xa to 1pass nxa	% Delta LT 1-pass xa to 1pass nxa	xrpd accel	Delta LT 2-pass to 1-pass nxa	%Delta LT 2-pass to 1-pass nxa
4	62.20E-06	78.50E-06	115.00E-06	36.50E-06	31.74%	y	52.80E-06	45.91%
16	171.50E-06	174.00E-06	320.00E-06	146.00E-06	45.63%	y	148.50E-06	46.41%
64	610.00E-06	820.00E-06	1.17E-03	350.00E-06	29.91%	y	560.00E-06	47.86%
512	3.71E-03	5.16E-03	5.42E-03	260.00E-06	4.80%	y	1.72E-03	31.64%

For the previous set of data, delta lock times were calculated and the percentage improvements in lock times are charted in Figure 11.27 and Figure 11.28. The combination of the XRPD latch/mux acceleration circuit and the state machine circuit produces lock time improvements in the range of 30-45%.

Figure 11.27 Two pass lock time % delta versus K1, K2 fixed at 512, $f_{in} \neq f_c$.

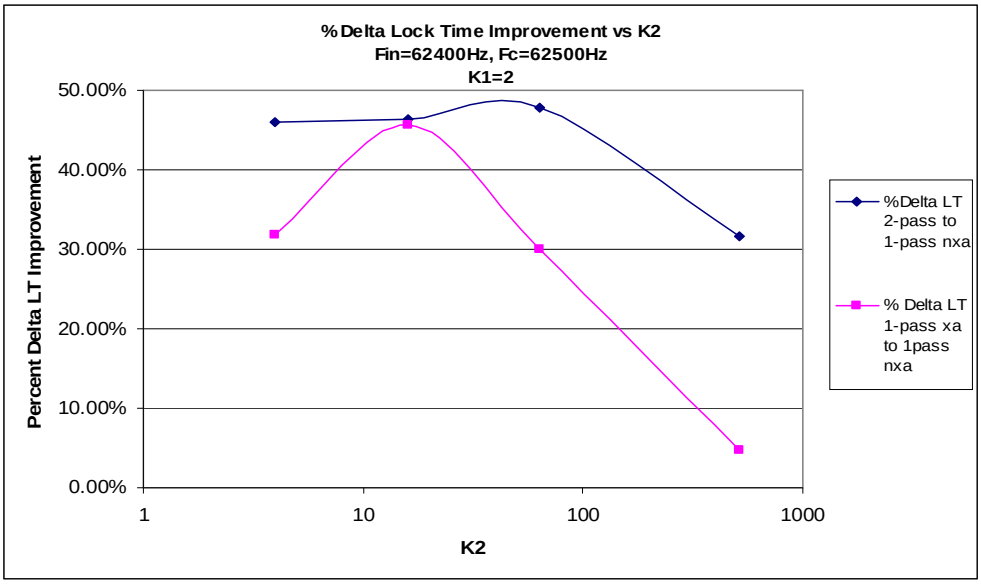


Figure 11.28 Two pass lock time delta versus K2, K1 fixed at 2, $f_{in} \neq f_c$.

Chapter 12 Measured versus Predicted Results

To gauge the accuracy of the lock time predictions from the equations, lock times were tabulated and charted. Lock time measurements were calculated by subtracting the time to reach lock range from the total lock time. This was done for measurements on a loop without controller circuits. These measurements are compared with predicted lock time 2.08τ. The numbers are listed in Table 12.1 and charted in Figure 12.1 and Figure 12.2. Charting on a log scale, the measured lock times follow the predicted numbers reasonably well. Charting on a linear scale however shows some deviation from predicted lock times at higher values of K.

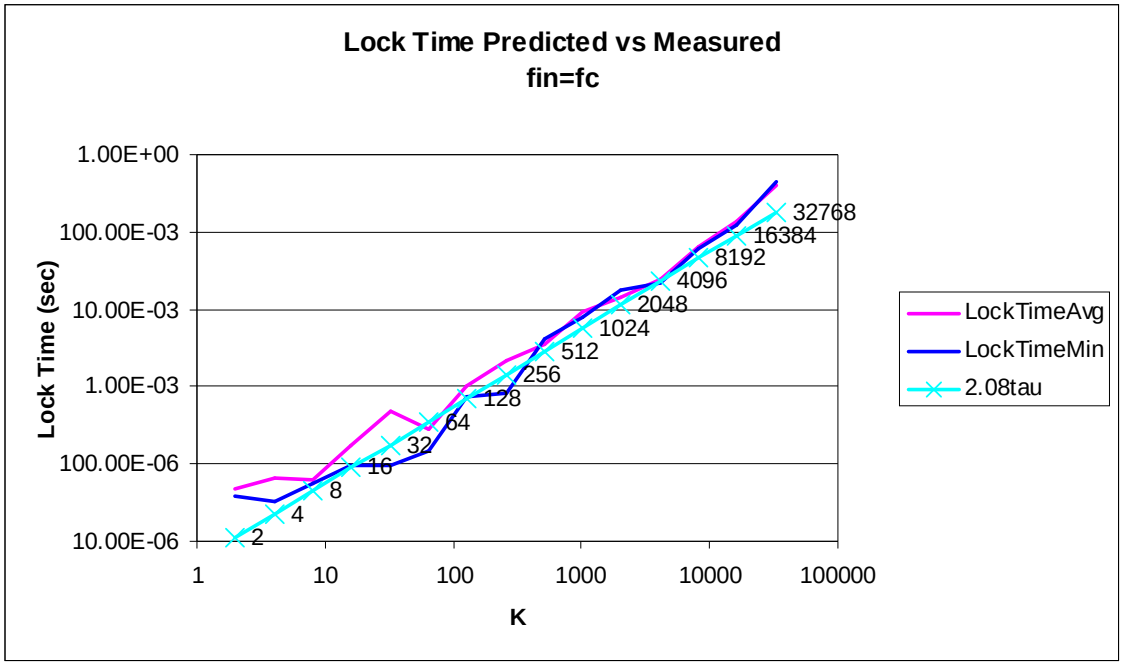


Figure 12.1 Lock time predicted versus measured, log scale.

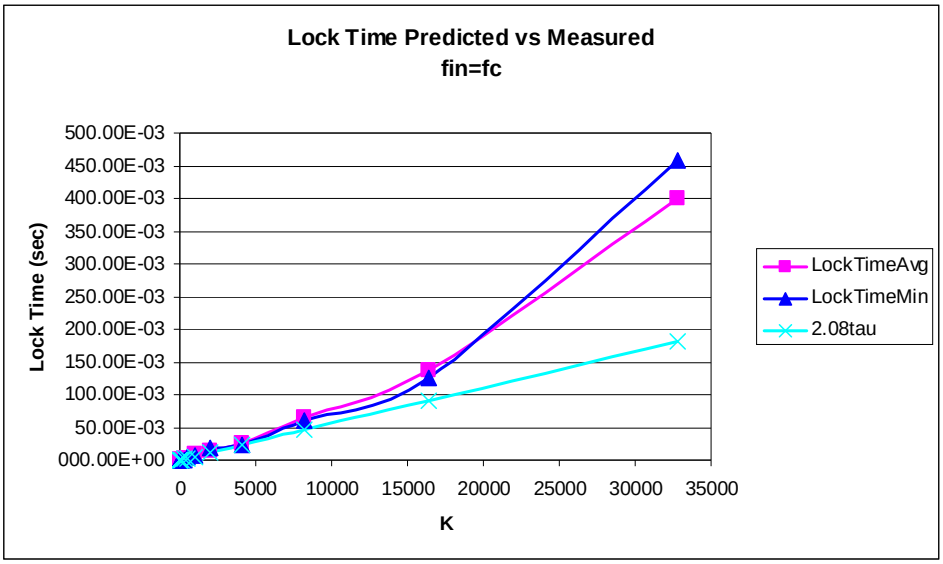


Figure 12.2 Lock time predicted versus measured, linear scale.

Table 12.1 Time to lock after reaching lock range, $f_{in}=f_c$.

K	avg	min	2.08tau
2	47.00E-06	39.00E-06	11.09E-06
4	67.50E-06	32.00E-06	22.19E-06
8	61.00E-06	57.00E-06	44.37E-06
16	176.00E-06	96.00E-06	88.75E-06
32	478.00E-06	98.00E-06	177.49E-06
64	285.00E-06	150.00E-06	354.99E-06
128	1.02E-03	740.00E-06	709.97E-06
256	2.22E-03	820.00E-06	1.42E-03
512	3.45E-03	4.10E-03	2.84E-03
1024	9.50E-03	7.80E-03	5.68E-03
2048	14.40E-03	18.00E-03	11.36E-03
4096	24.70E-03	22.40E-03	22.72E-03
8192	64.00E-03	61.00E-03	45.44E-03
16384	136.50E-03	125.00E-03	90.88E-03
32768	400.00E-03	458.00E-03	181.75E-03

The next set of data analyzes the measured versus predicted time to reach lock range after the input signal is inverted. Given a sufficient amount of lock time, the output signal f_{out} will reach a phase error of zero plus or minus a jitter of 1/2N or 1/256. When the signal is inverted the phase error will be moved to 0.5 cycles plus or minus 1/256 cycles. To get back into lock range, the phase

error must traverse back to 0.25 cycles and it will do so in an inverse exponential path as shown earlier in Figure 8.2. The time taken to accomplish this is equivalent to a normal exponential from 0.25 cycles to 1/256 or 0.0039 cycles. Using equation (5) with a starting phase error of 0.25 and an ending phase error of 0.0039, we arrive at a time of 4.16τ , or

$$t = -\tau \ln \frac{\phi_e(t)}{\phi_e(0)} = -\tau \ln \frac{1/256}{1/4} = 4.16\tau . \qquad (6)$$

Calculated values of 4.16τ for various values of K are shown in the last column of Table 12.2. Also included in the table are the average and minimum measured times to achieve lock range. These are charted for visual comparison in Figure 12.3 and Figure 12.4. The measured and calculated values track reasonably well as viewed on a log scale chart as shown in Figure 12.3. Some deviation is apparent at higher values of K if the data is charted on a linear scale as shown in Figure 12.4.

Table 12.2 Time to reach lock range, unmodified XRPD, $f_{in}=f_c$.
Unmodified XRPD.

	Lock range time (sec)		
K	min	avg	4.159tau
2	23.00E-06	46.00E-06	22.18E-06
4	24.00E-06	74.50E-06	44.36E-06
8	31.00E-06	81.50E-06	88.73E-06
16	96.00E-06	222.00E-06	177.45E-06
32	212.00E-06	392.00E-06	354.90E-06
64	550.00E-06	1.15E-03	709.80E-06
128	1.24E-03	1.86E-03	1.42E-03
256	3.08E-03	4.68E-03	2.84E-03
512	6.40E-03	11.15E-03	5.68E-03
1024	16.20E-03	22.50E-03	11.36E-03
2048	21.60E-03	44.60E-03	22.71E-03
4096	72.00E-03	83.50E-03	45.43E-03
8192	145.00E-03	154.00E-03	90.85E-03
16384	290.00E-03	298.50E-03	181.71E-03
32768	390.00E-03	579.00E-03	363.42E-03

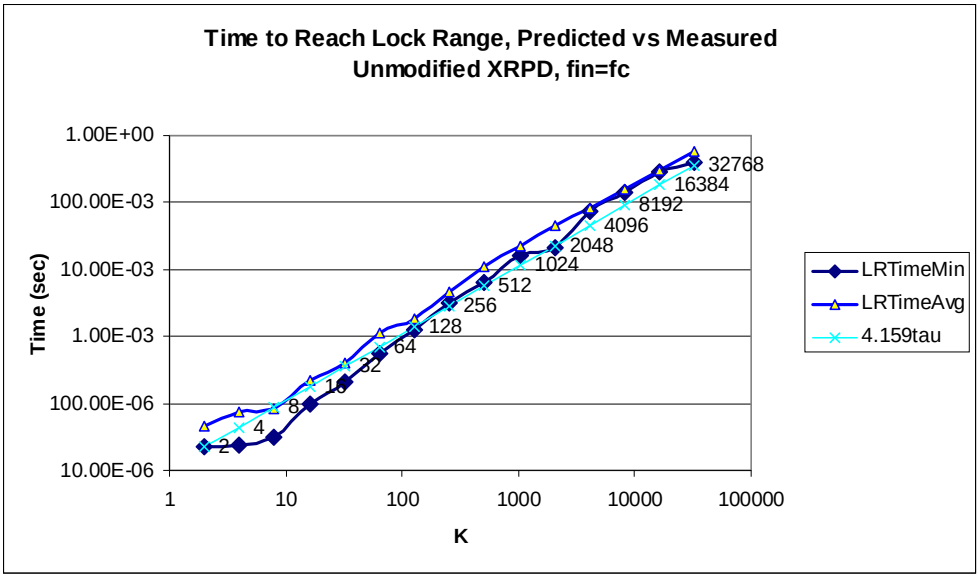


Figure 12.3 Time to reach lock range, unmodified XRPD, $f_{in}=f_c$, log scale.

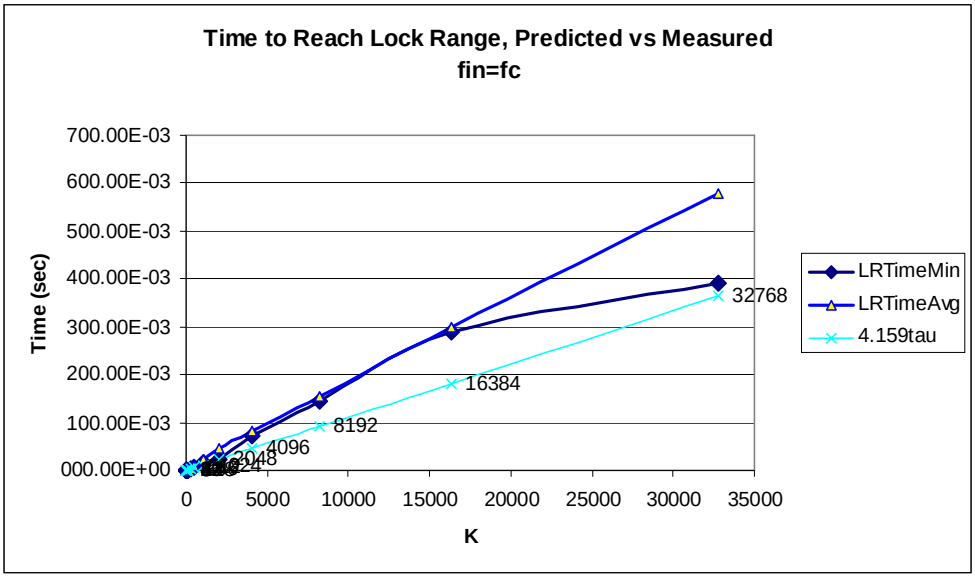


Figure 12.4 Time to reach lock range, unmodified XRPD, $f_{in}=f_c$, linear scale.

The next analysis is the measured versus calculated time to reach lock range with the modified phase detector. With the phase detector bypassed, the K-counter and ID circuit will make phase adjustments in a linear manner at a rate of $2KN/Mf_c$. An equation which satisfies this is

$$\phi_e(t) = \phi_e(0)\left[1 - \frac{Mf_c}{2KN}\right]t. \tag{7}$$

Solving the previous equation for t,

$$t = \frac{2KN}{Mf_c}\left[1 - \frac{\phi_e(t)}{\phi_e(0)}\right]. \tag{8}$$

When the input signal is inverted the phase error will be shifted to ½ cycle minus 1/256 cycles or 0.4961 cycles. The phase error will adjust linearly down to 0.25 cycles to return to lock range. The time to reach lock range is 0.2461 times $2KN/Mf_c$. This is calculated for various values of K in the last column of Table 12.3. Also included in the table are the average and minimum measured times to achieve lock range. These are charted in Figure 12.5 and Figure 12.6. The measured and calculated values track reasonably well at mid-range values of K with some deviation apparent at extreme high and low values of K. The deviation at the high end is more apparent when graphed on a linear scale.

Table 12.3 Time to reach lock range, with modified XRPD, $f_{in}=f_c$.
With Modified XRPD.

	Lock range time (sec)		
K	min	avg	0.2461(2KN/MFc)
2	16.00E-06	16.00E-06	5.25E-06
4	16.00E-06	16.00E-06	10.50E-06
8	20.40E-06	20.40E-06	21.00E-06
16	43.60E-06	43.60E-06	42.00E-06
32	77.00E-06	77.00E-06	84.00E-06
64	164.00E-06	164.00E-06	168.00E-06
128	344.00E-06	344.00E-06	336.01E-06
256	654.00E-06	654.00E-06	672.02E-06
512	1.30E-03	1.30E-03	1.34E-03
1024	2.59E-03	2.59E-03	2.69E-03
2048	5.15E-03	5.15E-03	5.38E-03
4096	10.30E-03	10.30E-03	10.75E-03
8192	21.80E-03	21.80E-03	21.50E-03
16384	33.60E-03	33.60E-03	43.01E-03
32768	41.50E-03	41.50E-03	86.02E-03

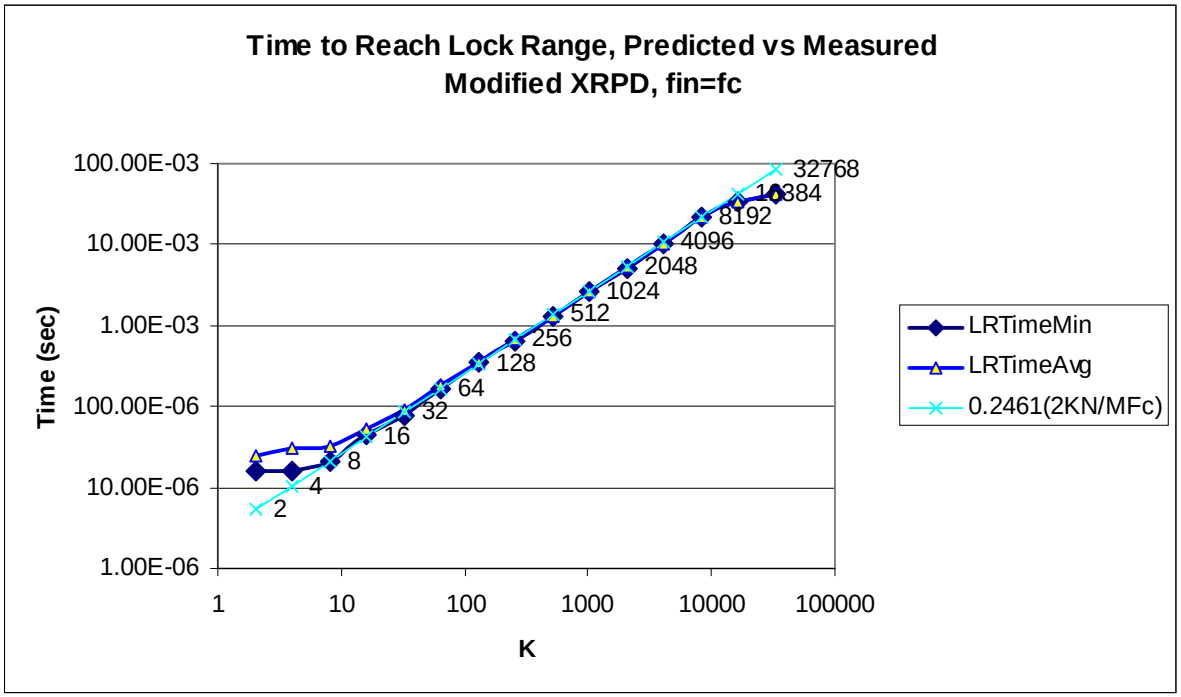


Figure 12.5 Time to reach lock range, modified XRPD, $f_{in}=f_c$, log scale.

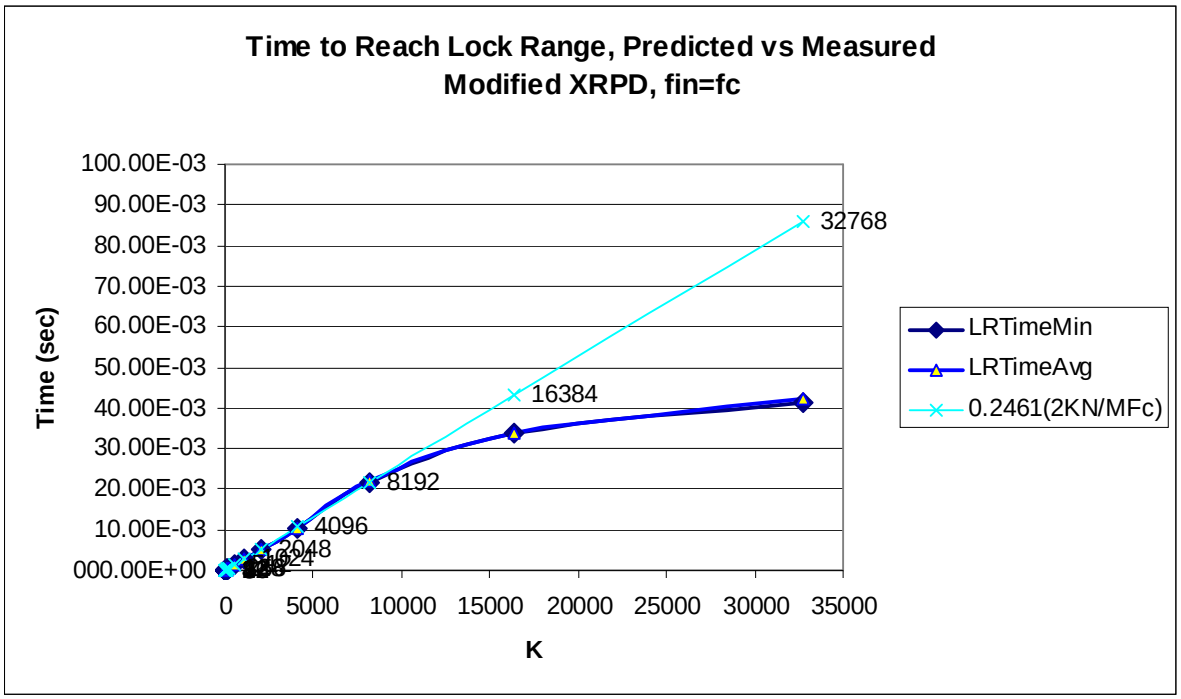


Figure 12.6 Time to reach lock range, modified XRPD, $f_{in}=f_c$, linear scale.

Chapter 13 Discussion

The breadboard prototype circuit performed as expected. For loop applications where the incoming signal deviates from the center frequency ($f_{in} \neq f_c$), it is beneficial to perform a wide lock followed by a narrow lock. Frequency shift key (FSK) is an example application where incoming signal frequencies may deviate from the center frequency. The 4-state state machine (unlocked, wide lock, narrow lock, reset) would help accelerate the lock time when changing between different frequencies.

For applications where the input signal is always equal to the center frequency, the comparator value is the same for both wide lock and narrow lock. In this case the state machine could be simplified to three states (unlocked, locked, reset). This might be a good match for a phase shift key (PSK) application where the incoming signal frequency f_{in} is constant, but the phase of the signal changes over time.

The exclusive-OR phase detector has a lock range of ±¼ cycle (±90°). The loop will take extra time to lock onto an incoming signal with a phase that is out of this range. This could be a performance limiter for PSK or other applications that are continually changing phase by more than ±¼ cycle. The latch/mux modification to the exclusive-OR could improve the performance of these applications by accelerating the re-lock time on sudden phase changes. This modification would improve initial signal acquisition lock time in all applications.

Advantages of the all digital phase locked loop include the ability to digitally select parameters, and the parameters are not subject to factors such as device tolerances, temperature, component aging, and power supply variations. Digitally programmable parameters can be modified dynamically, an advantage over analog loops which require analog components for establishing loop parameters. All digital phase locked loops can be designed with standard CMOS tools and fabricated on a standard CMOS process [6,14].

This style of DPLL however has some disadvantages which limit its usage. Jitter exists in the output signal f_{out} which can be minimized but not eliminated. Jitter minimization requires a high clock rate resulting in high power consumption. Further, the loop requires an input clock frequency which is much higher than the center frequency of the loop [14]. Another disadvantage of the DPLL is the lock time versus bandwidth issue which is addressed by this controller design.

For this project, the DPLL and the controller were designed as a two-chip set for manufacturing of prototype units. The maximum pin count for dual in-line packages from Mosis is 40 pins. Two 40-pin devices were needed to accomplish the goals of the design. The entire DPLL and controller design could be put on a single chip with a pin count of approximately 80 pins. Alternative package options such as pin grid array or chip carrier would be required for this pin count.

Chapter 14 Summary and Conclusions

The DPLL analyzed in this report is a first order system. Fast lock time and narrow bandwidth cannot be achieved simultaneously. The comparator and state machine circuit presented here can dynamically change the loop parameters (K modulus) to switch between wide bandwidth and narrow bandwidth. In applications where $f_{in} \neq f_c$ the steady state phase error of the loop will be different for different K values. Therefore the proposed circuit was designed to accommodate two different lock states, wide and narrow.

While performing lock time experiments, it was found when the incoming signal was periodically inverted (the PSK application for example), it was taking excessive time to relock. This is because the signal was being thrown outside the XRPD phase lock range of ±¼ cycle. A fix for this was also proposed.

Circuits to perform these functions were designed, laid out, and simulated using Cadence design tools. Two circuits were submitted for fabrication through the Mosis service and were received in April 2012. These circuits turned out to be non-functional. Analysis of the failing devices revealed that a data entry error in the project request resulted in incorrect mask sets used to process the circuits. A second submission was done for the circuits with a correction for the processing masks. The circuits were submitted in July 2012 for the Mosis V27K fabrication run and are due at publication time.

A prototype of the overall circuit was assembled on a breadboard and evaluated. Performance data was collected, analyzed, and presented.

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