USE OF TAPPED DELAY LINE FILTER IN DIGITAL TRANSMISSION SYSTEMS

A THESIS

PRESENTED TO THE

FACULTY OF THE DEPARTMENT OF ELECTRICAL ENGINEERING

UNIVERSITY OF HOUSTON

IN PARTIAL FULFILLMENT

OF THE REQUIREMENTS FOR THE DEGREE

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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by

Howard W. Louie

December, 1973

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ABSTRACT

The probability of error was found analytically by the averaging method for a PCM/NRZ digital transmission system under the influence of intersymbol interference and additive Gaussian noise. Two receiver structures were studied; an integrate-and-dump detector receiver and an intergrate-and-dump with tapped delay line filtering. The two receivers were implemented in order to obtain experimental results for comparison with calculated results. The analytical and experimental results were also compared to results for other receiver structures suggested by other investigators.

The receiver structure that was found to give near optimum performance consisted of an integrate-and-dump detector with a one-tap tapped delay line filter operating at a bandwidth-time duration product equal to 0.8.

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INTRODUCTION

In digital communication systems, there are two main sources of detection errors; intersymbol interference and additive random noise. For high bit rate transmission systems operating at high signal-to-noise ratios, intersymbol interference is often the main source of detection errors.

One source of intersymbol interference is bandwidth limiting of the system. Bandwidth limiting occurs through transmitter filtering, channel bandwidth restrictions, and receiver filtering. Bandlimiting of the signal produces not only degradation of the signal through energy loss, but also a time overlapping of the symbols into adjacent bit spaces. This overlapping of signals is called intersymbol interference. Thus intersymbol interference is the dependence of the amplitude of the desired signal upon other signals that precede or follow the signal under detection.

Chapter I will discuss the baseband model and receiver structures to be used in this thesis. Intersymbol interference and the use of a tapped delay line filter to eliminate the intersymbol interference will be covered. A modified tapped delay line filter will be introduced.

The error performance of the receiver structures will analyzed in Chapter II. Conclusions will be made from the analysis.

Chapter III will describe the experimental model of the digital transmission system. The experimental results will be discussed in Chapter IV.

In Chapter V, a comparison of the tapped delay line filter will be made with other receiver structures proposed by other investigators.

I. DIGITAL TRANSMISSION SYSTEM

1.1 Baseband Model

A baseband model of a PCM/NRZ digital transmission system is shown in Fig. 1. The transmitter consists of a binary source that generates a random sequence of binary bits, "1" and "0", and an encoder that produces the NRZ (non-return-to-zero) pulse sequence $\sum_{n=-\infty}^{\infty} a_n(t)$. The pulse $a_n(t)$ is of amplitude A or -A with pulse width T and corresponds to the binary "1" or "0" respectively.

The channel consists of additive white Gaussian noise and an ideal low pass filter. The Gaussian noise is zero mean with a spectral density of $\frac{N_o}{2}$. The filter has a transfer function

$$H(f) = \begin{cases} 1 & -B \le f \le B \\ 0 & \text{elsewhere} \end{cases}$$

The received signal is

$$r(t) = \sum_{n=-\infty}^{\infty} \Big(a_n(t) * h(t) \Big) + n_1(t) \ .$$

which is the transmitted sequence $\sum a_n(t)$ convolved with the low pass filter impulse reponse h(t) and the filtered noise $n_1(t)$.

The receiver consists of an integrate-and-dump detector, a sampler, a threshold detector, and a decoder. This is the optimum receiver structure for detecting the NRZ signal when the noise is white Gaussian and the bandwidth of the system is infinite. However, as the transmitted signal

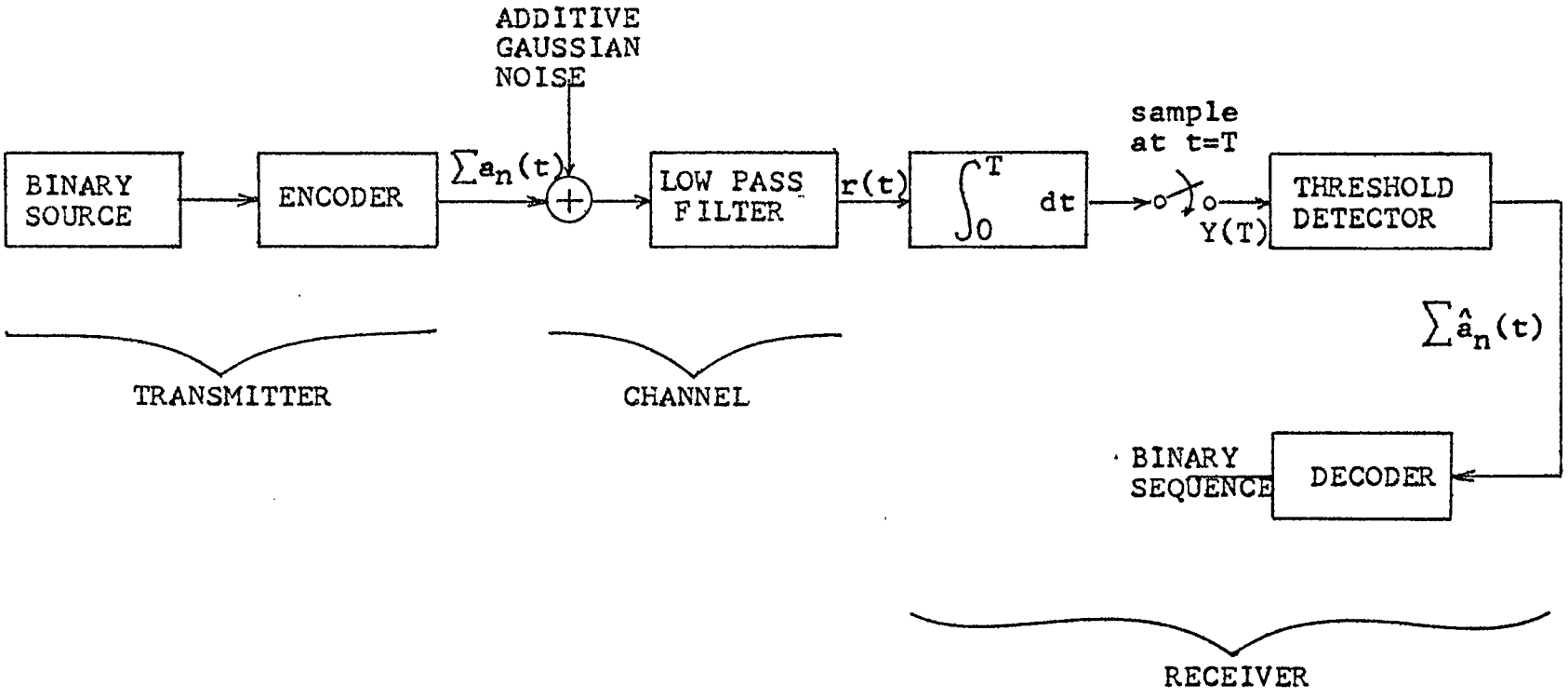


Figure 1 Baseband Model for PCM/NRZ Digital Transmission system

passes through the bandlimited channel, intersymbol interference is introduced by the low pass filter, H(f). This occurs as a "time smearing" of the individual bits into the adjacent bit periods. The interference is non Gaussian and is correlated with the sequence $\sum a_n(t)$. The integrate-and-dump detector is no longer the optimum receiver structure and the performance of the system is degraded, [1].

1.2 Intersymbol Interference

The output of the integrate-and-dump, Y(T) in Fig. 1, is

$$Y(T) = A_0 T\, J(BT,0) + \sum_{n=1}^{\infty} (A_n + A_{-n}) T\, J(BT,n) + n_2(T) \qquad (1)$$

where

$$J(BT,n) = \frac{2}{\pi} \int_0^{\pi BT} \frac{\sin^2 x}{x^2} \cos nx\, dx, \text{ [2]}. \qquad (2)$$

B is the bandwidth of the lowpass filter, T is the bit time duration of the pulse, and A_n equals +A or -A depending on which message was sent. The term J(BT,n) represents the output of the integrator from the sequence of pulses transmitted. The term $n_2(T)$ is the output of the integrator of the filtered noise $n_1(t)$.

Table 1 shows some values of J(BT,n) for various bandwidth-bit duration products (BT) and n's. J(BT,0) represents the integrator output of the bit under detection. For positive n's, J(BT,n) represents the the contribution to the output from future bits. For negative n's, J(BT,n) represents the contribution to the output from the past bits. Note that as BT approaches infinity, J(BT,n) for n not zero, becomes zero. This is expected since there is no intersymbol

TABLE 1

Some Values of J(BT,n)

BT	J(BT,0)	J(BT,1)	J(BT,2)	J(BT,3)
.5	0.7737	0.1291	-0.0222	0.0094
.6	0.8393	0.0673	0.0292	-0.0271
.7	0.8776	0.0441	0.0204	0.0030
.8	0.8960	0.0433	0.0033	0.0054
.9	0.9021	0.0464	0.0007	0.0001
1.0	0.9028	0.0471	0.0011	0.0002
1.2	0.9060	0.0493	0.0002	0.0024
1.5	0.9311	0.0353	-0.0113	0.0004
2.5	0.9592	0.0206	-0.0003	0.0001

interference when the bandwidth of the system is infinite.

Thus in (1), the first term represents the bit under detection. The second term is the intersymbol interference. And the third term is the additive Gaussian noise. The performance of the receiver can be improved if the second term or the intersymbol interference can be eliminated.

1.3 Tapped Delay Line Filtering

Various papers have been written on the use of tapped delay line (TDL) filters for eliminating the effects of in-intersymbol interference [3], [4], [5]. The basic tapped delay line filter is shown in Fig. 2. The output of the tegrator (from the system in Fig. 1) is normalized by the gain $\frac{1}{AT}$. The normalized intergrator samples are stored in an analog delay line with (2N+1) taps spaced T seconds apart. Thus the bit under detection with N adjacent past bits and N adjacent future bits ate stored in the delay line for every bit undergoing detection. In theory, the number of taps required would be infinite in order to obtain an optimum system. However, in most practical systems the number of interfering bits would be limited to a finite number and the number of taps required would also be finite.

The output of the taps are fed into a sign detector, SGN, in Fig. 2. The sign detector decides on whether the bit being sampled is positive or negative corresponding to A or -A being transmitted. The output of the sign detector is -1 if the bit was A or +1 if the bit was -A. This is multiplied by the tap gain J(BT,n) for n equal $\pm 1, \pm 2, \ldots \pm N$.

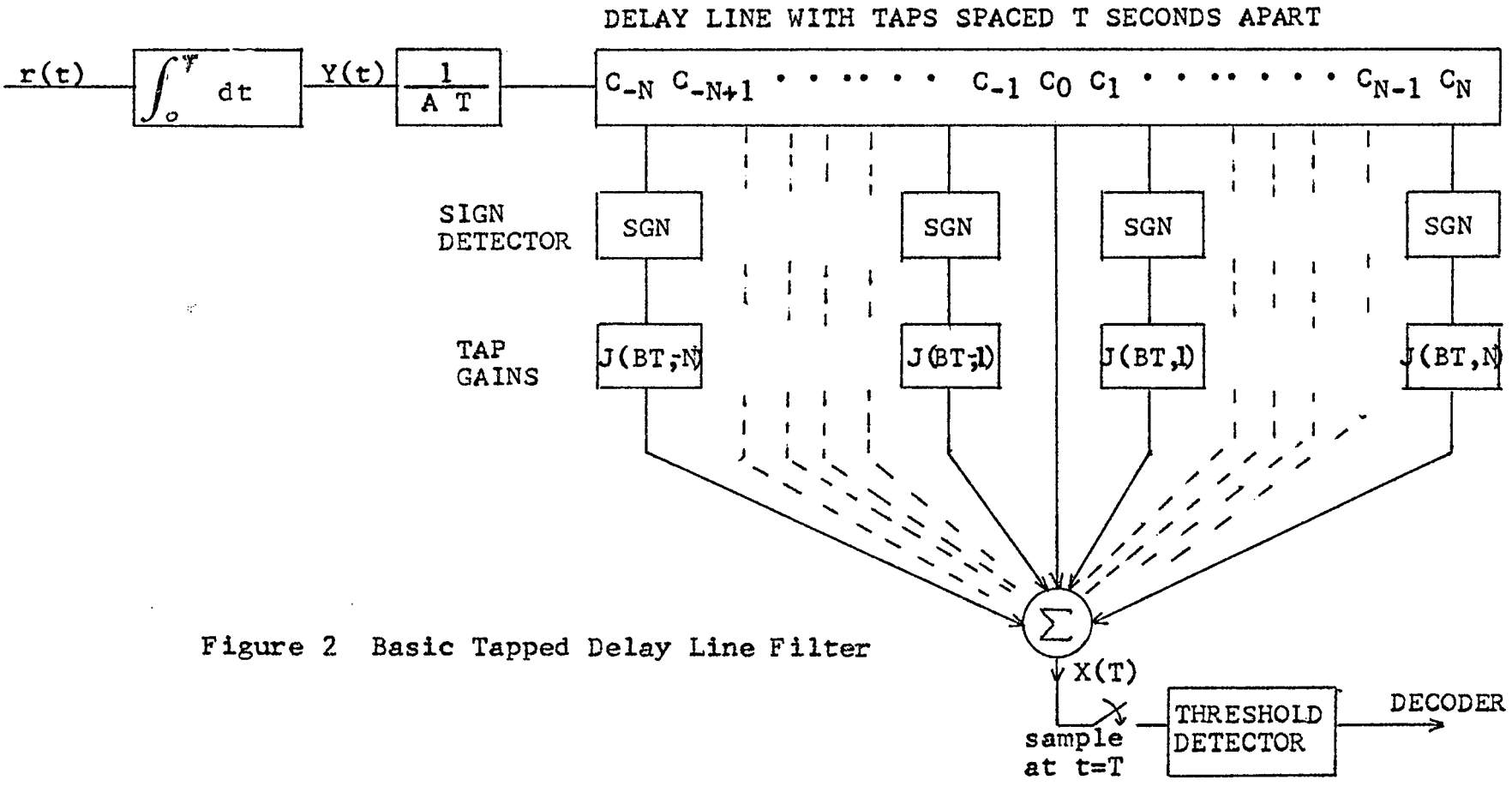


Figure 2 Basic Tapped Delay Line Filter

The 2N tap gains and C_0 are added together in the summer and sampled at t=T seconds. The output at X(T) will then be

$$X(T) = J(BT,0) + \sum_{n=1}^{N}\left[J(BT,n) + J(BT,-n)\right] + n_2(T) + \sum_{n=1}^{N}\left[(SGN)\ J(BT,n) + (SGN)\ J(BT,-n)\right] \qquad (3)$$

where SGN is either +1 or -1.

The first three terms are the sample stored in C_0 consisting of the normalized bit under detection, the intersymbol interference, and the Gaussian noise. The fourth term is the output of the 2N adjacent bits multiplied by the tap gains J(BT, n). Therefore, if all the signs of the adjacent interfering bits were detected correctly, the output X(T) would be

$$X(T) = J(BT,0) + n_2(T)$$

as the intersymbol interference is eliminated. This receiver structure would be near optimum (the SNR is reduced since J(BT,0) is not unity when the bandwidth is restriced). The performance is degraded since there will be errors produced in the sign detectors.

1.4 Modified Tapped Delay Line Filter

A modified tapped delay line filter is to be implemented in this thesis. This is shown in Fig. 3. It will be assummed that the intersymbol interference is limited to two bits preceding the one under detection. Assumming that the intersymbol interference is limited to past bits only can be justified by the fact that causal filters have no output previous to the arrival of the input. It has been determined experimentally that only two past bits need be considered

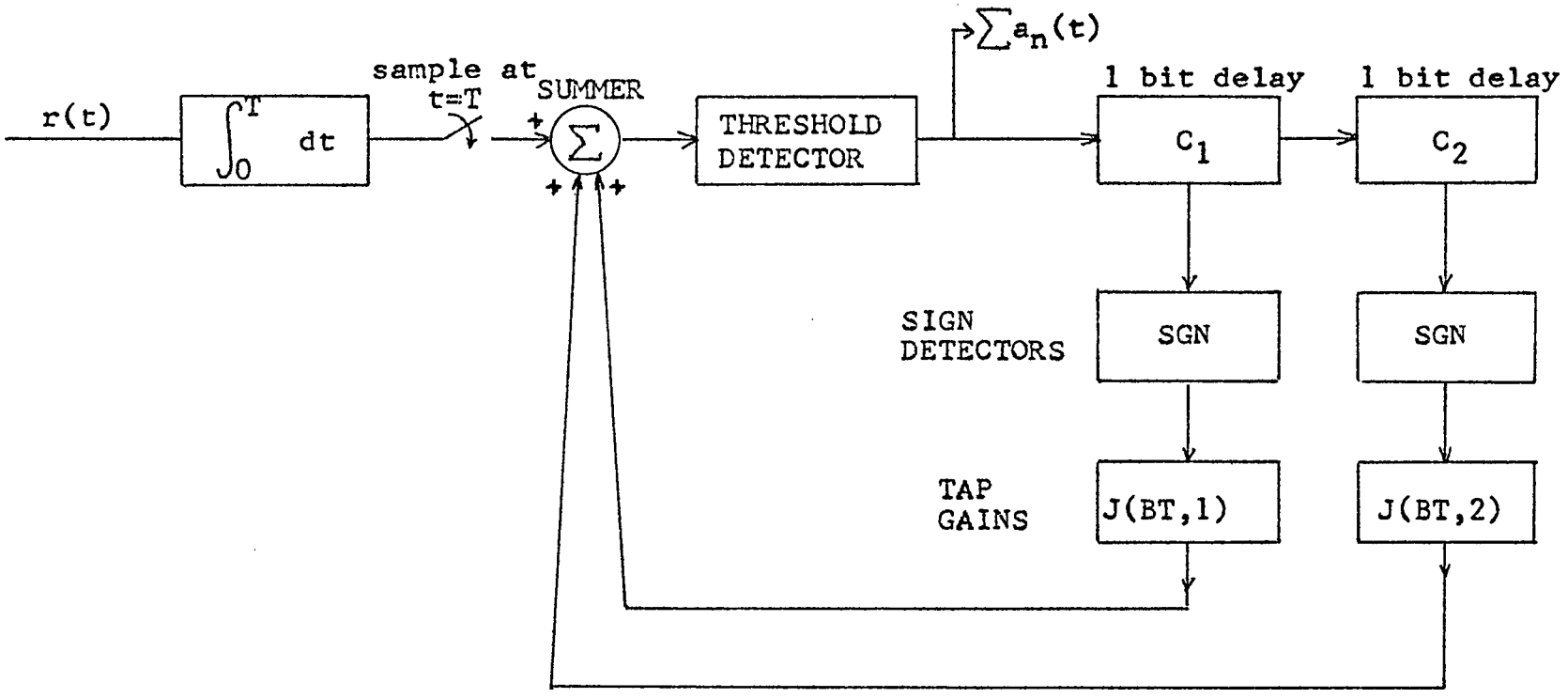


Figure 3 Modified Tapped Delay Line Filter

for analysis of the receiver performance.

In the modified tapped delay line filter, the output of the threshold detector is fed into a digital delay line. This simplified construction since only a shift register is required and an analog delay line is not required. The delay line taps, C_1 and C_2, store the bits after detection has been made. The output of the sign detectors, SGN, and tap gains J(BT,1) and J(BT,2) should represent the influence of the intersymbol interference from the past two bits on the bit under detection. This influence is then subtracted from the bit under detection at the summer.

The major difference between the system in Fig. 2 and the modified system in Fig. 3 occurs in how the signs of the past two bits are determined. Looking back at Fig. 2, we see that the output of the integrator is stored in an analog delay line. If the sign detector is a threshold detector, then the sign detector output would be the same as the integrate-and-dump detector in Fig. 1. The probability of error for the sign detector would be the same as that of the integrate-and-dump detector operating in the presence of intersymbol interference.

Looking at the system in Fig. 3, the sign detectors operate on bits that had been previously processed. That is, the bits would hopefully have had the intersymbol interference eliminated before being decided on by the threshold detector. The probability of error for the sign detectors in this system will be lower than the probability of error

for the sign detectors in Fig. 2. This can be considered as decision feedback since past decisions will be used in making present decisions.

Since there is feedback in the modified tapped delay line, an error in the decision of $a_n(t)$ will affect the decision of $a_{n+1}(t)$ and $a_{n+2}(t)$. The incorrect bit $\hat{a}_n(t)$ is kept for two bit periods. The sign detectors will therefore be incorrect for two decisions. If an error occurs in detecting $a_{n+1}(t)$ because of error in $\hat{a}_n(t)$, the first error will also affect the decision on $a_{n+3}(t)$. This is error propagation in the system and will be analyzed in a later section of this thesis.

II. PERFORMANCE ANALYSIS OF MODIFIED TAPPED DELAY LINE FILTER

An analysis of the performance of the modified tapped delay line filter will be made using one and two taps in the delay line. The analytical performance of this system will be used to compare it with other systems for eliminating intersymbol interference and will be compared with the experimental results from the implemented system. The most commonly used parameter for measuring the performance of digital systems is the bit error rate probability. The bit error rate (probability of error) versus signal-to-noise energy ratio (SNR) for various BT's will be plotted.

2.1 Assumptions Used in Analysis

The assumptions used in analyzing the PCM/NRZ system

are:

1) The transmitter and receiver will be in perfect synchronization.
2) The baseband channel will consists of an ideal lowpass filter. This assumption will simplify calculations.
3) The intersymbol interference will be limited to the two preceding bits before the bit under detection.
4) The noise is additive white Gaussian with zero mean and variance of $\frac{N_o}{2}$.
5) A random sequence of equiprobable binary bits is transmitted.

Figure 4a shows the two NRZ signals, A and -A. These two pulses are the antipodal signals s(t) and -s(t) in Fig. 4b multiplied by the amplitude A. Figure 4c shows the channel response to a single pulse, $s_p(t)$. The pulse, $s_p(t)$ is s(t) "time smeared" into the adjacent bits. Figure 4d shows a binary sequence of "1" 's and "0" 's and their corresponding NRZ sequence. Figure 4e shows the NRZ sequence after it has passed through a lowpass channel without noise. There is intersymbol interference introduced into the sequence by the "smearing" of the individual bits in the channel.

2.2 Operation of the Tapped Delay Line Filter

A simplified block diagram of the modified tapped delay line filter is shown in Fig. 5 and this will be used for the analysis. The intergrate-and-dump detector has an impulse response

$$h(t) = s(T-t)$$

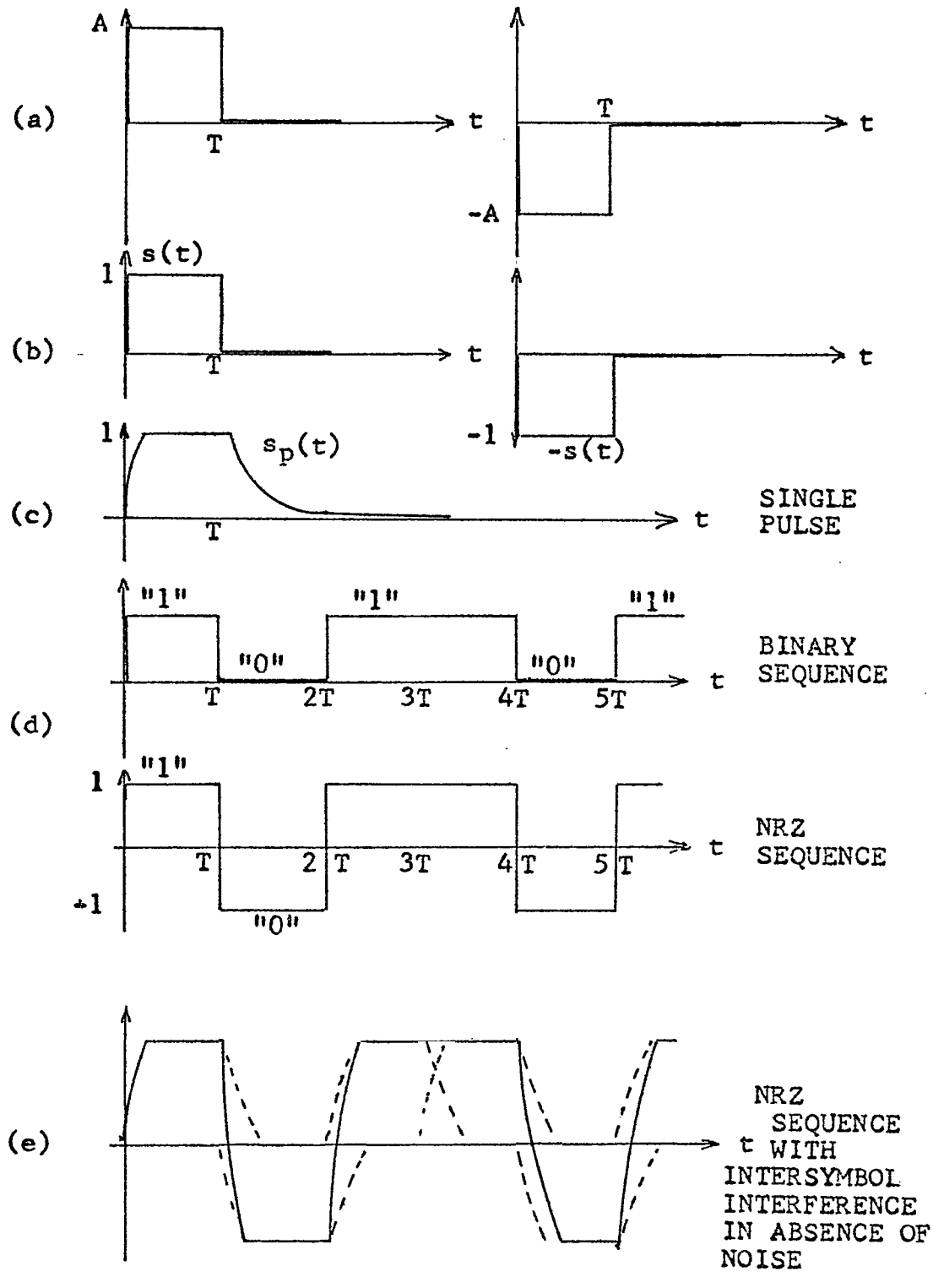


Figure 4 Examples of Pulses in Digital Systems

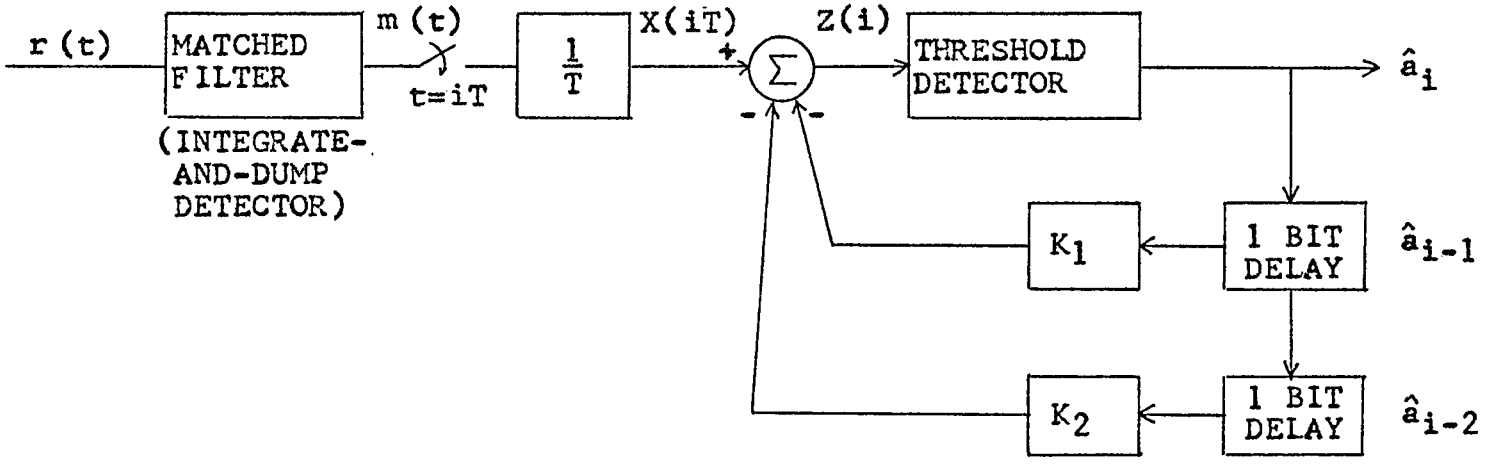


Figure 5 Simplified Form of Modified Delay Line

where T is the bit period length. This is a matched filter which is matched to the transmitted pulse rather than the received pulse. The transmitter transmits an infinite sequence of NRZ pulses $\sum_n a_n A\, s(t-nT)$, where a_n is +1 or -1 depending on the message sent.

The receiver input is

$$r(t) = \sum_{n=-\infty}^{\infty} a_n A\, s_p(t-nT) + n_1(t) \tag{4}$$

where $s_p(t-nT)$ is the response of and ideal lowpass filter with the input $s(t-nT)$ and $n_1(t)$ is the response of the filter to the noise $n(t)$ alone.

The output of the integrator can be written as

$$m(t) = \left\{ \sum_{n=-\infty}^{\infty} \left[a_n A\, s_p(t-nT) \right] + n_1(t) \right\} * s(T-t) \tag{5}$$

Or, expanding in terms of integrals

$$m(t) = \int_0^T \sum_{n=-\infty}^{\infty} \left[a_n A\, s_p(t-nT) \right] dt + \int_0^T n_1(t)\, dt \tag{6}$$

Integrating and sampling at $t=iT$, where i is the i-th bit under detection, the output of the sampler is

$$X(iT) = K_0\, a_i + K_1\, a_{i-1} + K_2\, a_{i-2} + n_2 \tag{7}$$

where

$$K_0 = \int_0^T A\, s_p(t)\, dt \tag{8}$$

$$K_1 = \int_0^T A\, s_p(t-T)\, dt \tag{9}$$

$$K_2 = \int_0^T A\, s_p(t-2T)\, dt \tag{10}$$

$$n_2 = \int_0^T n_1(t)\, dt \tag{11}$$

K_0 corresponds to the output of the integrator from bit a_i. K_1 corresponds to the output from the interference caused by

bit a_{i-1}. K_2 corresponds to the integrator output from the interference caused by bit a_{i-2}.

The noise component n_2 is still a random variable with a zero mean Gaussian distribution with variance

$$\begin{aligned}\sigma^2 &= E\{n_2{}^2\} \\ &= E\left\{\int_0^T n_1(t)\,dt \int_0^T n_1(\tau)\,d\tau\right\} \\ &= \int_0^T\int_0^T E\{n_1(t)\,n_1(\tau)\}\,dt\,d\tau \\ &= \frac{N_oT}{2}\int_0^{\pi BT}\frac{\sin^2 x}{x^2}\,dx \end{aligned} \tag{11}$$

This can be expressed in terms of J(BT,0) as

$$\sigma^2 = \frac{N_oT}{2}\,J(BT,0) \tag{13}$$

Since ideal lowpass filtering is assummed, (8) - (9) can be simplified using (2)

$$K_0 = AT\,J(BT,0) \tag{14}$$

$$K_1 = AT\,J(BT,1) \tag{15}$$

$$K_2 = AT\,J(BT,2) \tag{16}$$

The input of the threshold detector Z(i) is

$$\begin{aligned} Z(i) &= X(iT) - K_1\,\hat{a}_{i-1} - K_2\,\hat{a}_{i-2} \\ &= K_0\,a_i + K_1\,a_{i-1} + K_2\,a_{i-2} + n_2 \\ &\quad - K_1\,\hat{a}_{i-1} - K_2\,\hat{a}_{i-2} \\ &= K_0\,a_i + K_1(a_{i-1} - \hat{a}_{i-1}) + K_2(a_{i-2} - \hat{a}_{i-2}) + n_2 \end{aligned} \tag{17}$$

where $\hat{a}_{i-1}$ and $\hat{a}_{i-2}$ are the detected signals corresponding to a_{i-1} and a_{i-2}. The threshold detector must make the decision from

$$K_0a_i + K_1(a_{i-1} - \hat{a}_{i-1}) + K_2(a_{i-2} - \hat{a}_{i-2}) + n_2 \underset{-1}{\overset{1}{\gtrless}} 0 \tag{18}$$

Let

$$\lambda = K_0 a_i + K_1(a_{i-1} - \hat{a}_{i-1}) + K_2(a_{i-2} - \hat{a}_{i-2}) + n_2$$

The threshold detector then chooses +1 if λ is greater than zero, the threshold level, and chooses -1 if λ is less than zero.

2.3 Error Analysis

An error in detection is made when λ is less than zero given that +1 was transmitted or when λ is greater than zero given that -1 was transmitted. The probability of error for the detection of bit a_i is

$$P\{\mathcal{E}\} = \tfrac{1}{2} P\{\lambda<0 \,|\, a_i=+1\} + \tfrac{1}{2} P\{\lambda>0 \,|\, a_i=-1\} \qquad (19)$$

given that a_i is +1 or -1 with equal probability. Because of the intersymbol interference, the conditional probabilities in (19) are dependent on the previously transmitted bits a_{i-1} and a_{i-2} and the detected bits $\hat{a}_{i-1}$ and $\hat{a}_{i-2}$. The probability of error will be determined using the averaging method. Table 2 lists all possible sequences of a_i, $\hat{a}_{i-1}$, and $\hat{a}_{i-2}$.

The probability of error can be written as

$$\begin{aligned}
P_i = {} & \tfrac{1}{2} P\left\{\lambda<0 \,|\, a_i=1, \hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}=a_{i-2}\right\}(1-P_{i-1})(1-P_{i-2}) \\
& + \tfrac{1}{2} P\left\{\lambda<0 \,|\, a_i=1, \hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}=a_{i-2}\right\}(P_{i-1})(1-P_{i-2}) \\
& + \tfrac{1}{2} P\left\{\lambda<0 \,|\, a_i=1, \hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}\right\}(1-P_{i-1})(P_{i-2}) \\
& + \tfrac{1}{2} P\left\{\lambda<0 \,|\, a_i=1, \hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}\right\}(P_{i-1})(P_{i-2}) \\
& + \tfrac{1}{2} P\left\{\lambda>0 \,|\, a_i=-1, \hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}=a_{i-2}\right\}(1-P_{i-1})(1-P_{i-2}) \\
& + \tfrac{1}{2} P\left\{\lambda>0 \,|\, a_i=-1, \hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}=a_{i-2}\right\}(P_{i-1})(1-P_{i-2}) \\
& + \tfrac{1}{2} P\left\{\lambda>0 \,|\, a_i=-1, \hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}\right\}(1-P_{i-1})(P_{i-2}) \\
& + \tfrac{1}{2} P\left\{\lambda>0 \,|\, a_i=-1, \hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}\right\}(P_{i-1})(P_{i-2})
\end{aligned} \qquad (20)$$

Table 2 Possible Sequences of a_i, $\hat{a}_{i-1}$, and $\hat{a}_{i-2}$

a_i		$E\{Z(i)\} = m_i$	
1	$\hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}=a_{i-2}$	$m_1=K_0$	
1	$\hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}=a_{i-2}$	$m_2=K_0+2K_1\hat{a}_{i-1}$	$m_{2a}=K_0+2K_1$
			$m_{2b}=K_0-2K_1$
1	$\hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}$	$m_3=K_0+2K_2\hat{a}_{i-2}$	$m_{3a}=K_0+2K_2$
			$m_{3b}=K_0-2K_2$
1	$\hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}$	$m_4=K_0+2K_1\hat{a}_{i-1}$	$m_{4a}=K_0+2K_1+2K_2$
		$+2K_2\hat{a}_{i-2}$	$m_{4b}=K_0+2K_1-2K_2$
			$m_{4c}=K_0-2K_1+2K_2$
			$m_{4d}=K_0-2K_1-2K_2$
-1	$\hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}=a_{i-2}$	$m_5=-K_0$	
-1	$\hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}=a_{i-2}$	$m_6=-K_0+2K_1\hat{a}_{i-1}$	$m_{6a}=-K_0+2K_1$
			$m_{6b}=-K_0-2K_1$
-1	$\hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}$	$m_7=-K_0+2K_2\hat{a}_{i-2}$	$m_{7a}=-K_0+2K_2$
			$m_{7b}=-K_0-2K_2$
-1	$\hat{a}_{i-1}\neq a_{i-1}, \hat{a}_{i-2}\neq a_{i-2}$	$m_8=-K_0+2K_1\hat{a}_{i-1}$	$m_{8a}=-K_0+2K_1+2K_2$
		$+2K_2\hat{a}_{i-2}$	$m_{8b}=-K_0-2K_1+2K_2$
			$m_{8c}=-K_0+2K_1-2K_2$
			$m_{8d}=-K_0-2K_1-2K_2$

where P_{i-1} and P_{i-2} are the the probability of error in the detection of bits a_{i-1} and a_{i-2} respectively. The probability of error, P_i, is the sum of the conditional probabilities of error for all possible sequences that can occur.

The conditional probabilities are random variables that are Gaussian distributed functions with the mean equal to the expected value of Z(i) and the variance σ^2 of the noised n_2. The means of the sequences are shown in the second column of Table 2. Note that the means m_2, m_3, m_6, and m_7 can have two different values and the means m_4 and m_8 can have four different values depending on the value of a_{i-1} and a_{i-2}. This is shown in the last column of Table 2.

The conditional probability in the first term in (20) can be written as

$$P\left\{\lambda<0 \middle| a_i=1, \hat{a}_{i-1}=a_{i-1}, \hat{a}_{i-2}=a_{i-2}\right\} = \int_{-\infty}^{0} N(m_1,\sigma^2)\, dt \qquad (21)$$

where

$$N(m_j,\sigma^2) = \frac{1}{\sqrt{2\pi}\,\sigma} \exp\left\{-\frac{(x-m_j)^2}{2\sigma^2}\right\}, \quad j=1,2, \ldots 8$$

and

$$m_j = E\left\{Z(i)\right\}$$

This can be expressed in the form of the tabulated function

$$Q(a) = \int_{-\infty}^{a} \frac{1}{\sqrt{2\pi}} \exp\left\{-\frac{x^2}{2}\right\} dx \qquad (22)$$

Noting that the conditional probabilities for $P\{\lambda<0 | a_i=1\}$ are equal to $P\{\lambda>0 | a_i=-1\}$ due to the symmetry of the signals and message patterns, (20) can be rewritten as

$$P_i = Q\left(\frac{m_1}{\sigma}\right)(1-P_{i-1})(1-P_{i-2}) + \tfrac{1}{2}\left[Q\left(\frac{m_{2a}}{\sigma}\right) + Q\left(\frac{m_{2b}}{\sigma}\right)\right](P_{i-1})(1-P_{i-2})$$

$$+ \tfrac{1}{2}\left[Q\left(\frac{m_{3a}}{\sigma}\right) + Q\left(\frac{m_{3b}}{\sigma}\right)\right](1-P_{i-1})(P_{i-2})$$
$$+ \tfrac{1}{4}\left[Q\left(\frac{m_{4a}}{\sigma}\right) + Q\left(\frac{m_{4b}}{\sigma}\right) + Q\left(\frac{m_{4c}}{\sigma}\right) + Q\ \frac{m_{4d}}{\sigma}\right](P_{i-1})(P_{i-2}) \quad (23)$$

Looking at the first term in (23) the argument of Q is $\frac{m_1}{\sigma}$. This can be written as

$$\frac{m_1}{\sigma} = \frac{AT\ J(BT,0)}{\sqrt{\frac{N_o}{2}\,T\,J(BT,0)}} \quad (24)$$

Multipling the numerator and denominator by $\frac{1}{AT}$

$$\frac{m_1}{\sigma} = \frac{J(BT,0)}{\sqrt{\frac{N_o}{2A^2T}\,J(BT,0)}} \quad (25)$$

Let $E = A^2T$, the energy in the transmitted signal, then

$$\frac{m_1}{\sigma} = \sqrt{\frac{E}{2N_o}}\sqrt{\frac{1}{J(BT,0)}}\ J(BT,0) \quad (26)$$

Similarly for $Q\left(\frac{m_{2a}}{\sigma}\right)$

$$\frac{m_{2a}}{\sigma} = \sqrt{\frac{E}{2N_o}}\sqrt{\frac{1}{J(BT,0)}}\ \left(J(BT,0) + 2\,J(BT,1)\right) \quad (27)$$

The arguments of Q in the other terms follow readily. Thus The probability of error (bit error rate) can now be expressed in terms of the signal-to-noise ratio, $\frac{E}{N_o}$, and BT.

Notice for the case of infinite bandwidth, J(BT,0) equals 1 and J(BT,n) for n not zero equals 0. The terms $Q\left(\frac{m_j}{\sigma}\right)$, j=1,2, ...8, all reduce to $Q\left(\sqrt{E/2N_o}\right)$. Letting the probability

$$P_i = P_{i-1} = P_{i-2} = P$$

Equation (23) reduces to

$$P = Q\left(\sqrt{\frac{E}{2N_o}}\right) \quad (28)$$

which is the probability of error for the detection of antipodal signals with additive white Gaussian noise using a matched filter receiver (an integrate-and-dump detector is a matched filter for the case of infinite bandwidth).

We would expect the average probabilities P_i, P_{i-1}, and P_{i-2} to be equal since the average probability of error should be the same from bit to bit. However, (23) cannot be found in closed form by letting $P_i = P_{i-1} = P_{i-2}$ because a quadratic equation would result from this substitution. The probability of error for this system was calculated in a recursive manner by the use of a computer program. The program used is shown in Appendix 1. The probabilities P_1 and P_2 were set equal to zero and the probability for bit i=10 was found. Setting P_1 and P_2 equal to zero would correspond to starting the system with a known channel input or having the state of the channel known. The results of the computer calculations are tabulated in Table 5.

If the probabilities P_1 and P_2 are set equal to one in the computer program, this would correspond to having two errors in a row. P_3 would then correspond to the worst case error rate when two incorrect decisions are made in sequence. The results of this analysis are also shown in Table 5.

An analysis was also made for a tapped delay line filter using only one tap. It is still assummed that the intersymbol interference is limited to the two preceding bits. The averaging method for determining the probability of error is still used. All possible sequences of a_i, $\hat{a}_{i-1}$,

and a_{i-2} are shown in Table 3 along with the $E\{Z(i)\}$. The probability of error can be expressed as

$$\begin{aligned} P_i' &= P\left\{\lambda'<0 \,\middle|\, a_i=1, a_{i-1}=a_{i-1}, a_{i-2}=1\right\}\tfrac{1}{4}(1-P_{i-1}') \\ &+ P\left\{\lambda'<0 \,\middle|\, a_i=1, a_{i-1}=a_{i-1}, a_{i-2}=-1\right\}\tfrac{1}{4}(1-P_{i-1}') \\ &+ P\left\{\lambda'<0 \,\middle|\, a_i=1, a_{i-1}\neq a_{i-1}, a_{i-2}=1\right\}\tfrac{1}{4}(P_{i-1}') \\ &+ P\left\{\lambda'<0 \,\middle|\, a_i=1, a_{i-1}\neq a_{i-1}, a_{i-2}=-1\right\}\tfrac{1}{4}(P_{i-1}') \\ &+ \text{four terms for } P\left\{\lambda'>0 \,\middle|\, a_i=-1\right\} \end{aligned} \tag{29}$$

where P_i' and P_{i-1}' are the probabilities of error for a one-tap tapped delay line filter. Since the probability of error for the sequence when $P\{a_i=1\}$ are the same as those for $P\{a_i=-1\}$, P_i' can be written as

$$\begin{aligned} P_i' &= \tfrac{1}{2}\, Q\left(\frac{m1}{\sigma}\right)(1-P_{i-1}') + \tfrac{1}{2}\, Q\left(\frac{m2}{\sigma}\right)(i-P_{i-1}') \\ &+ \tfrac{1}{4}\left[Q\left(\frac{m3a}{\sigma}\right) + Q\left(\frac{m3b}{\sigma}\right)\right] P_{i-1}' \\ &+ \tfrac{1}{4}\left[Q\left(\frac{m4a}{\sigma}\right) + Q\left(\frac{m4b}{\sigma}\right)\right] P_{i-1}' \end{aligned} \tag{30}$$

The probability of error was calculated using a computer program similar to the program in Appendix 1. The error rate was calculated for the known channel case and for the case when an incorrect decision is in the delay line. The results are tabulated in Table 5.

Finally, the probability of error was calculated for the integrate-and-dump detector. It is still assumed that the intersymbol interference is limited to the two past bits. All possible sequences of a_i, a_{i-1}, and a_{i-2} are shown in Table 4. The probability of error can be expressed as

$$P\{\mathcal{E}\} = \tfrac{1}{4}\left[Q\left(\frac{m1}{\sigma}\right) + Q\left(\frac{m2}{\sigma}\right) + Q\left(\frac{m3}{\sigma}\right) + Q\left(\frac{m4}{\sigma}\right)\right] \tag{31}$$

The results are also shown in Table 5 along with the results for the one- and two-tap tapped delay line filter.

TABLE 3

Possible Sequences of

a_i, $\hat{a}_{i-1}$, and a_{i-2}

a_i	a_{i-1}	a_{i-2}	$E\{Z(i)\}$	
+1	$\hat{a}_{i-1} = a_{i-1}$	+1	$m_1 = K_0 + K_2$	
+1	$\hat{a}_{i-1} = a_{i-1}$	-1	$m_2 = K_0 + K_2$	
+1	$\hat{a}_{i-1} \neq a_{i-1}$	+1	$m_{3a} = K_0 + 2K_1 + K_2$	$m_{3b} = K_0 - 2K_1 + K_2$
+1	$\hat{a}_{i-1} \neq a_{i-1}$	-1	$m_{4a} = K_0 + 2K_1 - K_2$	$m_{4b} = K_0 - 2K_1 - K_2$
-1	$\hat{a}_{i-1} = a_{i-1}$	+1	$m_5 = -K_0 + K_2$	
-1	$\hat{a}_{i-1} = a_{i-1}$	-1	$m_6 = -K_0 - K_2$	
-1	$\hat{a}_{i-1} \neq a_{i-1}$	+1	$m_{7a} = -K_0 + 2K_1 + K_2$	$m_{7b} = -K_0 - 2K_1 + K_2$
-1	$\hat{a}_{i-1} \neq a_{1-1}$	-1	$m_{8a} = -K_0 + 2K_1 - K_2$	$m_{8b} = -K_0 - 2K_1 - K_2$

TABLE 4

Possible Sequences of

a_i, a_{i-1}, and a_{i-2}

a_i	a_{i-1}	a_{i-2}	$E\{Z(i)\}$
+1	+1	+1	$m_1 = K_0 + K_1 + K_2$
+1	-1	+1	$m_2 = K_0 - K_1 + K_2$
+1	+1	-1	$m_3 = K_0 + K_1 - K_2$
+1	-1	-1	$m_4 = K_0 - K_1 - K_2$
-1	-1	-1	$m_5 = -K_0 - K_1 - K_2$
-1	+1	-1	$m_6 = -K_0 + K_1 - K_2$
-1	-1	+1	$m_7 = -K_0 - K_1 + K_2$
-1	+1	+1	$m_8 = -K_0 + K_1 + K_2$

TABLE 5

Analytical Results

BT	SNR (DB)	INTEGRATE AND DUMP DETECTOR (IDD) LOG P(E)	ONE-TAP TAPPED DELAY LINE		TWO-TAP TAPPED DELAY LINE	
			LOG P(E)	WORST CASE LOG P(E)	LOG P(E)	WORST CASE LOG P(E)
0.5	3	-1.337	-1.392	-1.185	-1.386	-1.184
	6	-1.973	-2.175	-1.605	-2.175	-1.603
	8	-2.621	-3.043	-2.027	-3.046	-2.023
	10	-3.574	-4.369	-2.655	-4.377	-2.644
	12	-5.020	-6.415	-3.606	-6.435	-3.580
	14	-7.255	-9.596	-5.065	-9.644	-5.003
	16	-10.729	-14.564	-7.318	-14.677	-7.180
	18	-16.151	-22.345	-10.814	-21.005	-10.534
0.6	3	-1.451	-1.467	-1.400	-1.466	-1.390
	6	-2.234	-2.298	-2.077	-2.310	-2.048
	8	-3.069	-3.214	-2.769	-3.244	-2.705
	10	-4.297	-4.606	-3.782	-4.679	-3.645
	12	-6.130	-6.735	-5.305	-6.903	-5.033
	14	-8.917	-10.016	-7.631	-10.377	-7.142
	16	-13.228	-15.119	-11.220	-15.828	-10.415
	18	-19.979	-23.127	-16.822	-24.414	-15.544
0.7	3	-1.503	-1.510	-1.480	-1.510	-1.475
	6	-2.351	-2.379	-2.273	-2.385	-2.257
	8	-3.276	-3.343	-3.110	-3.358	-3.073
	10	-4.664	-4.817	-4.345	-4.854	-4.263
	12	-6.760	-7.088	-6.207	-7.176	-6.030

TABLE 5 (CONT.)

BT	SNR (DB)	IDD	ONE-TAP		TWO-TAP	
			TDL	W.C.	TDL	W.C.
		LOG P(E)	LOG P(E)	LOG P(E)	LOG P(E)	LOG P(E)
0.7	14	-9.950	-10.605	-9.067	-10.804	-8.723
	16	-14.903	-16.078	-13.502	-16.500	-12.901
	18	-22.634	-24.656	-20.431	-25.473	-19.457
0.8	3	-1.525	-1.531	-1.502	-1.529	-1.502
	6	-2.394	-2.421	-2.317	-2.421	-2.317
	8	-3.347	-3.412	-3.184	-3.413	-3.183
	10	-4.786	-4.937	-4.471	-4.938	-4.469
	12	-6.979	-7.304	-6.428	-7.301	-6.422
	14	-10.357	-11.003	-9.465	-11.009	-9.450
	16	-15.628	-16.808	-14.219	-16.823	-14.183
	18	-23.912	-25.944	-21.692	-25.981	-21.609
0.9	3	-1.530	-1.538	-1.504	-1.535	-1.504
	6	-2.402	-2.433	-2.316	-2.433	-2.316
	8	-3.356	-3.431	-3.175	-3.431	-3.175
	10	-4.796	-4.966	-4.451	-4.966	-4.451
	12	-6.987	-7.350	-6.394	-7.350	-6.394
	14	-10.366	-11.077	-9.412	-11.077	-9.411
	16	-15.644	-16.929	-14.140	-16.929	-14.139
	18	-23.949	-26.148	-21.579	-26.150	-21.575
1.0	3	-1.530	-1.538	-1.504	-1.536	-1.504
	6	-2.402	-2.434	-2.314	-2.434	-2.314
	8	-3.356	-3.433	-3.171	-3.433	-3.171
	10	-4.794	-4.969	-4.443	-4.969	-4.443
	12	-6.983	-7.355	-6.381	-7.355	-6.380

TABLE 5 (CONT.)

BT	SNR (DB)	IDD	ONE-TAP		TWO-TAP	
		LOG P(E)	TDL LOG P(E)	W.C. LOG P(E)	TDL LOG P(E)	W.C. LOG P(E)
1.0	14	-10.358	-11.084	-9.391	-11.085	-9.390
	16	-15.632	-16.940	-14.108	-16.942	-14.103
	18	-23.930	-26.165	-21.527	-26.169	-21.517
1.2	3	-1.533	-1.542	-1.505	-1.540	-1.505
	6	-2.406	-2.442	-2.311	-2.441	-2.311
	8	-3.360	-3.444	-3.162	-3.444	-3.162
	10	-4.797	-4.986	-4.426	-4.986	-4.426
	12	-6.983	-7.382	-6.352	-7.382	-6.352
	14	-10.356	-11.127	-9.346	-11.127	-9.346
	16	-15.627	-17.008	-14.037	-17.008	-14.037
	18	-23.923	-16.274	-21.416	-26.274	-21.416
1.5	3	-1.563	-1.568	-1.548	-1.567	-1.547
	6	-2.469	-2.487	-2.416	-2.489	-2.411
	8	-3.467	-3.511	-3.351	-3.416	-3.339
	10	-4.983	-5.087	-4.746	-5.098	-4.717
	12	-7.297	-7.528	-6.861	-7.556	-6.794
	14	-10.854	-11.332	-10.127	-11.400	-9.978
	16	-16.376	-17.280	-15.220	-17.438	-14.919
	18	-25.015	-26.608	-23.194	-26.951	-22.654
2.5	3	-1.596	-1.598	-1.591	-1.597	-1.591
	6	-2.537	-2.543	-2.078	-2.543	-2.518
	8	-3.583	-3.599	-3.539	-3.599	-3.539
	10	-5.189	-5.226	-5.088	-5.226	-5.088
	12	-7.667	-7.756	-7.455	-7.756	-7.455

TABLE 5 (CONT.)

BT	SNR (DB)	IDD	ONE-TAP		TWO-TAP	
		LOG P(E)	TDL LOG P(E)	W.C. LOG P(E)	TDL LOG P(E)	W.C. LOG P(E)
2.5	14	-11.510	-11.712	-11.109	-11.713	-11.109
	16	-17.501	-17.930	-16.817	-17.930	-16.817
	18	-26.900	-27.727	-25.800	-27.728	-25.799
∞	3	-1.640				
	6	-2.621				
	8	-3.719				
	10	-5.412				
	12	-8.045				
	14	-12.166				
	16	-18.644				
	18	-28.855				

2.4 Conclusions Obtained From Analysis

Various performance curves are shown in Figs. 6, 7, 8, and 9. Some conclusions that can be drawn from these calculations are:

1) At low signal-to-noise ratios, the Gaussian noise is the predominant source of errors.
2) At high signal-to-noise ratios, intersymbol interference is the predominant source of errors.
3) Intersymbol interference increases as BT is decreased.
4) There is little or no difference in performance between the one- and two-tap tapped delay line except when operating at low BT's ($BT<0.8$) with high signal-to-noise ratios ($SNR\geq 18dB$).
5) The probability of error after a detection error has been made in the tapped delay line does not increase significantly when operating at low SNR's. At high SNR's, the probability of error may be increased by several orders of magnitude, but this is not serious since the probability of error is still less than 10^{-12} at these levels. Thus there is no problem of severe error propagation where the receiver could get into a situation where errors keep producing more errors.
6) For all systems, as BT increases above BT equal to 0.8, the performance of the system improves by an insignificant amount except at very high SNR's ($SNR\geq 18dB$). Thus the performance is near optimum at BT equal to 0.8.
7) From the above conclusions, a fixed digital channel

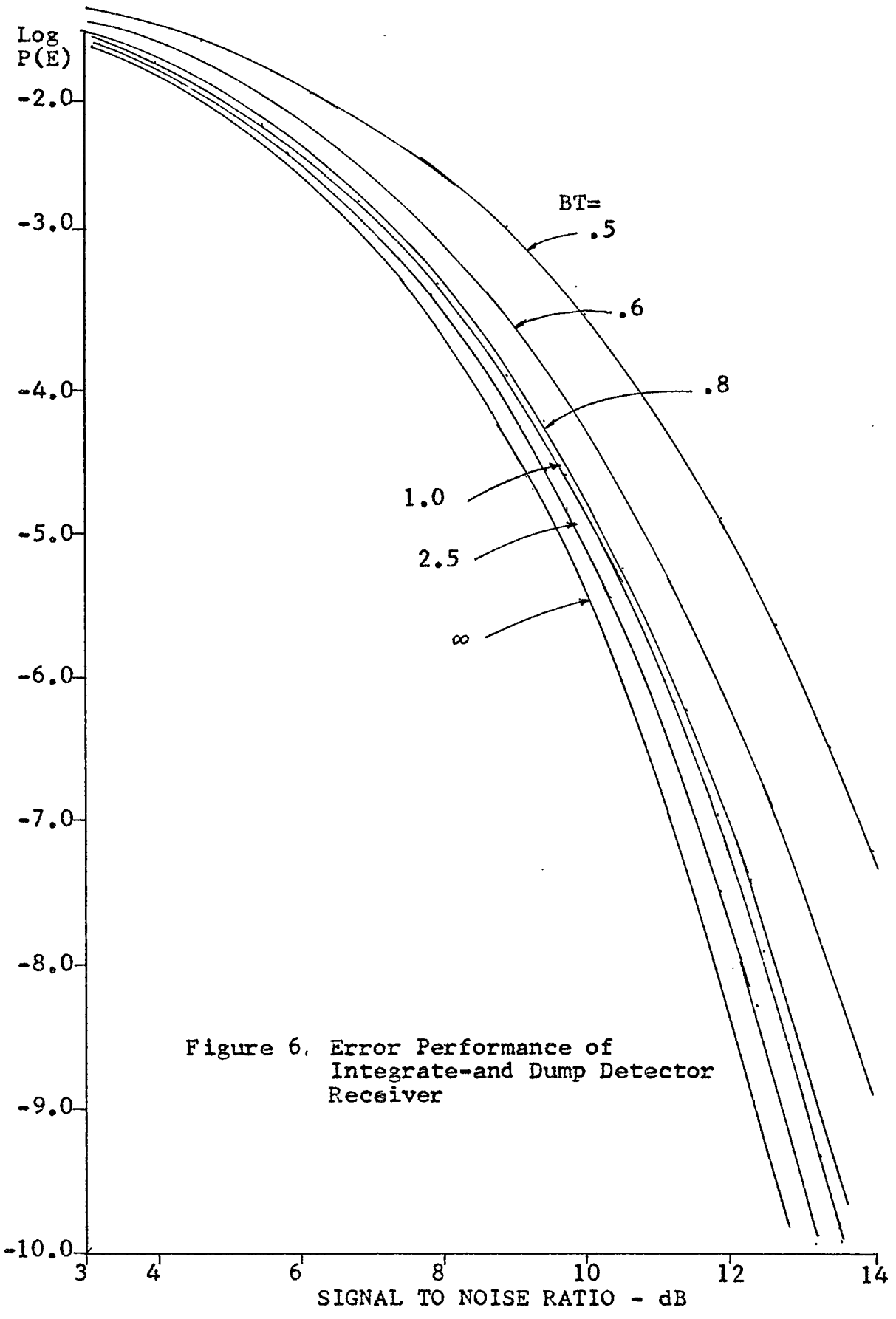


Figure 6. Error Performance of Integrate-and Dump Detector Receiver

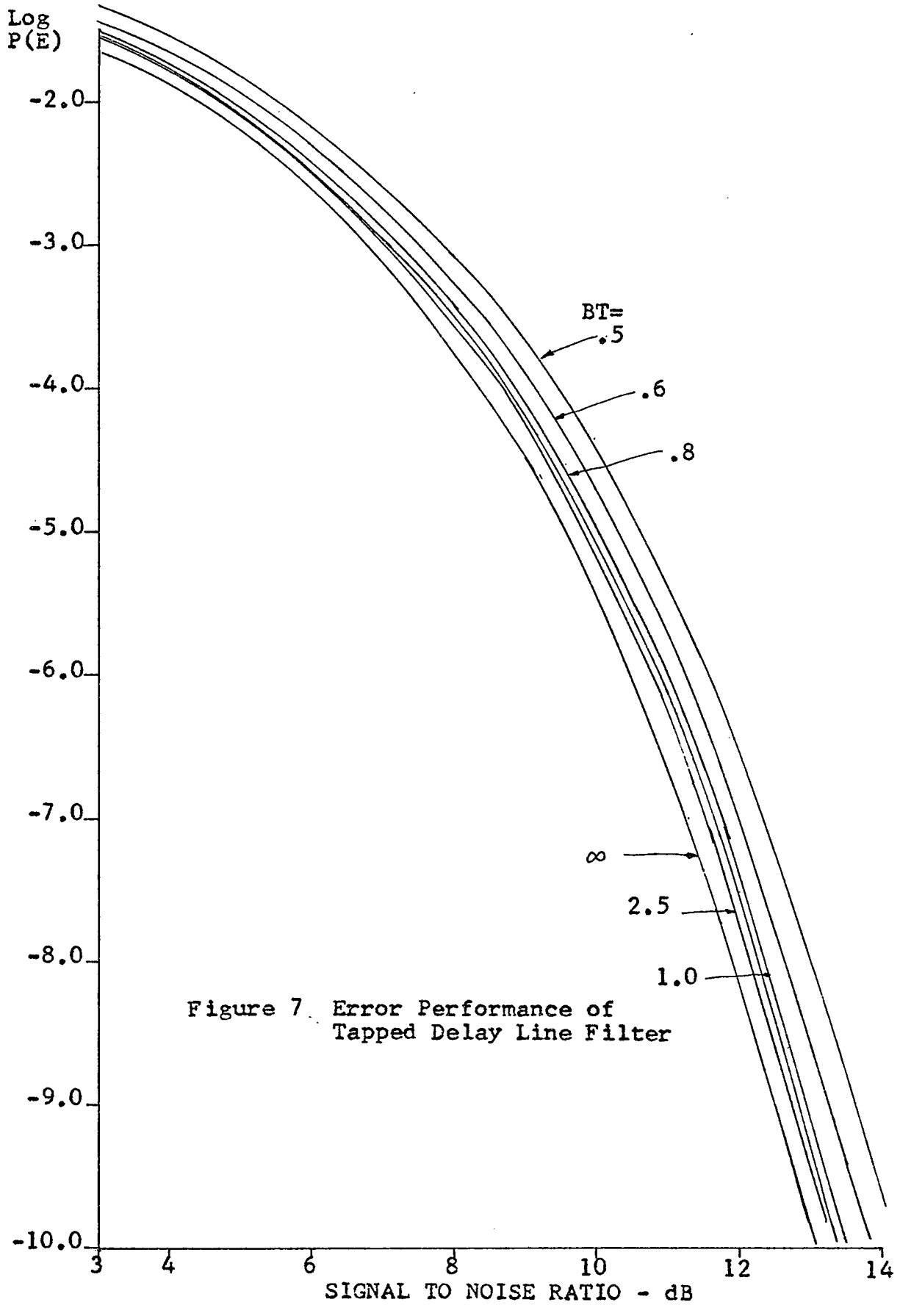


Figure 7. Error Performance of Tapped Delay Line Filter

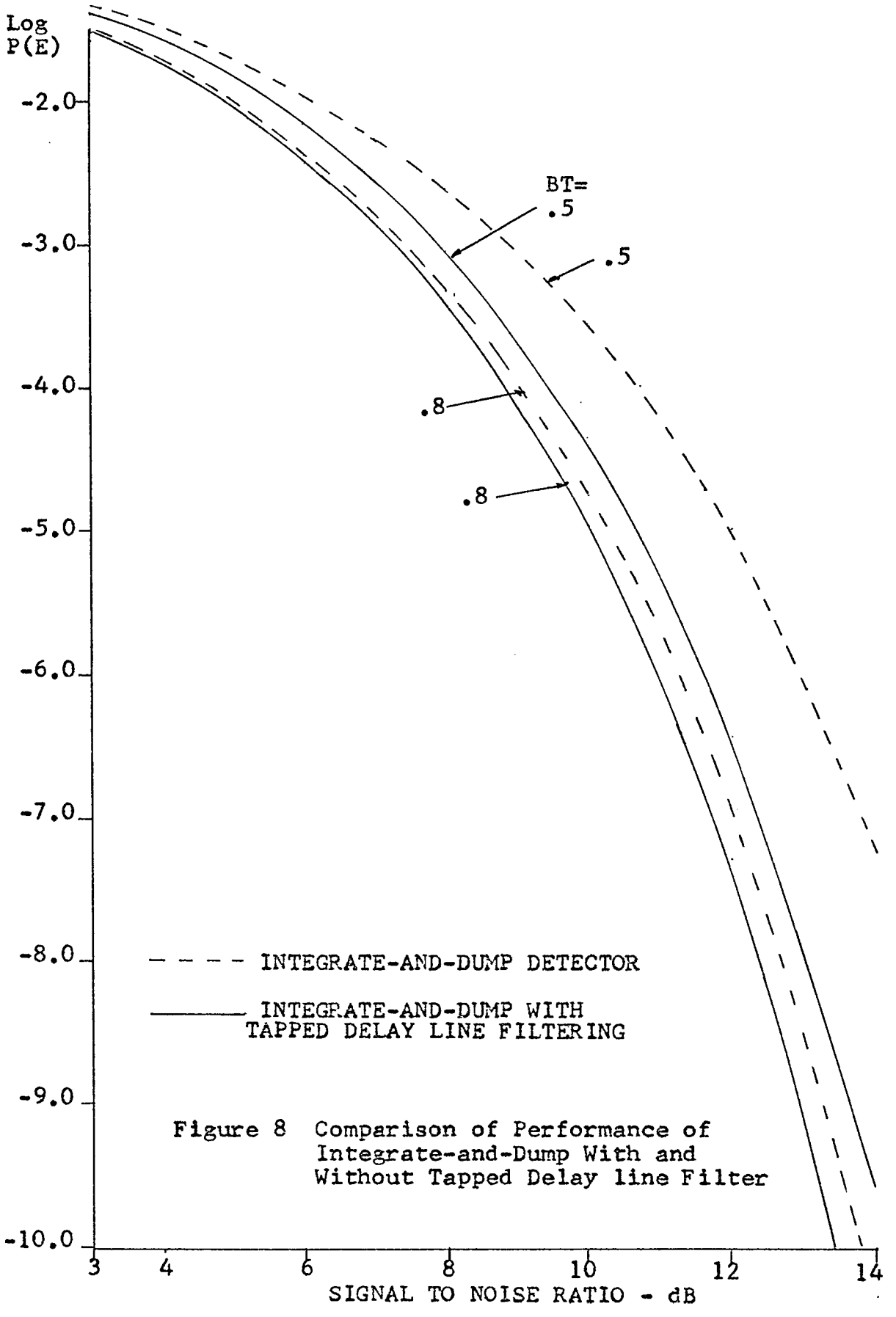


Figure 8 Comparison of Performance of Integrate-and-Dump With and Without Tapped Delay line Filter

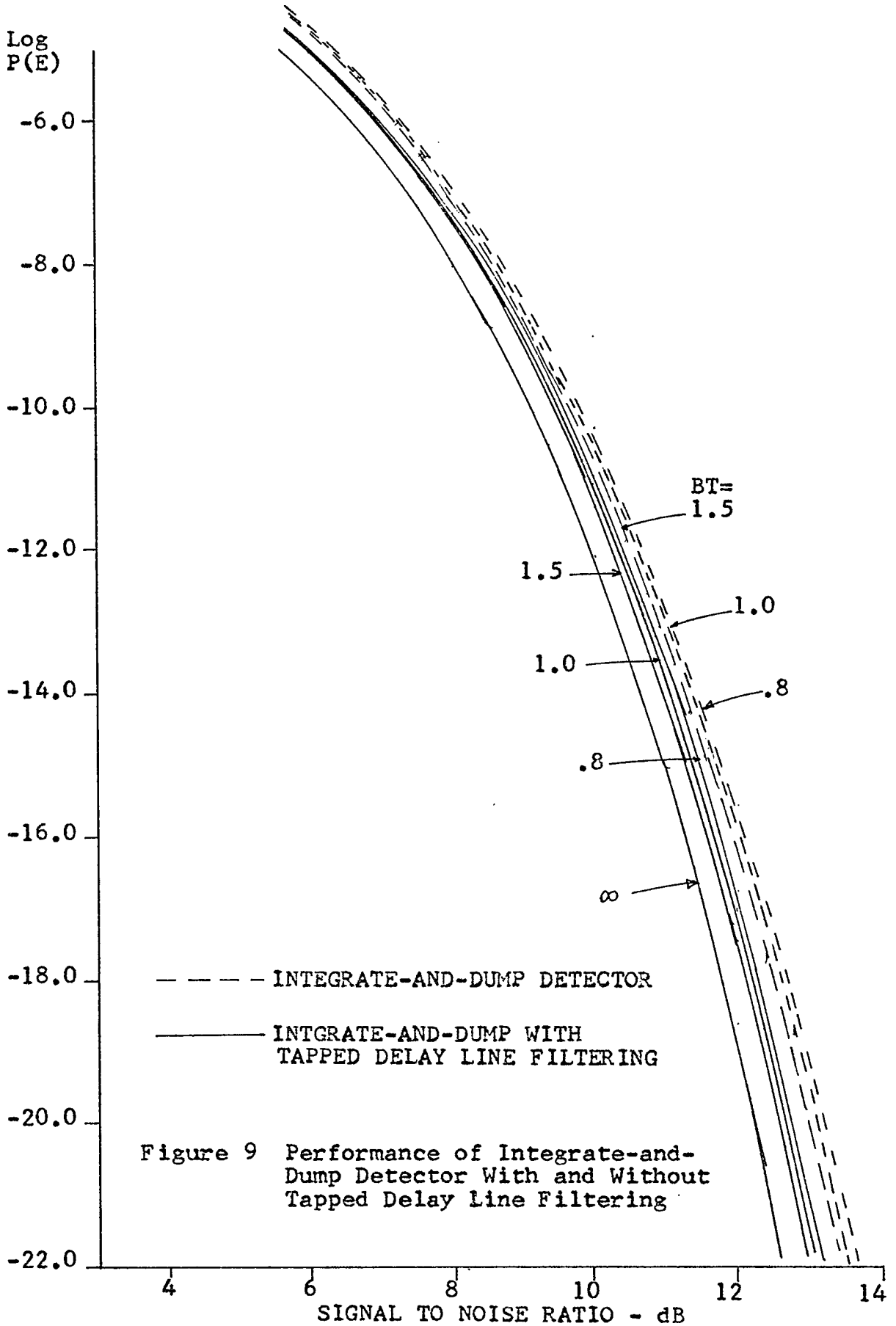


Figure 9 Performance of Integrate-and-Dump Detector With and Without Tapped Delay Line Filtering

operating at moderate SNR (10 to 18 dB) provides near optimum performance when using an integrate-and-dump detector with a one-tap tapped delay line filter and with the system operating at a bit rate such that BT equals 0.8. Any increase in BT would produce an insignificant improvement in performance and a decrease in BT would produce a significant degradation of performance. The use of two instead of one tap would also produce an insignificant improvement in performance.

III. SYSTEM IMPLEMENTATION

A PCM/NRZ baseband digital transmission system was implemented in order to obtain experimental results. The system was implemented using commerically available integrated circuits to simplify construction. A block diagram of the system is shown in Fig. 10. The receiver can be operated as an integrate-and-dump detector or an integrate-and-dump with tapped delay line filtering. Note, that there are two seperate threshold detectors and that dual integrators are used.

The experimental system operates at 10 kilobits per second. The bit period is therefore 100 μsec. The bandwidth bit duration (BT) of the system is changed by varying the bandwidth of the lowpass filter. A commerical lowpass filter was used. The filter had a -24 dB/octave attenuation slope.

As the transmitted signal passes through the filter, a time lag will occur between the transmitter output and the integrator input. This time lag will range between 150 μsec at BT=2.0 to 225 μsec at BT=0.5. Therefore a variable time delay was provided in order to properly synchronize the transmitter and the receiver in this system for different BT's.

The system clock is shown in Fig. 11. A pulse generator provides a 500 KHz square wave. The 500 KHz is divided by 50 to obtain a 10 KHz square wave. The 10 KHz clock pulse provides the time base for the pseudo random sequence generator and the integrator control. A Run/Reset switch

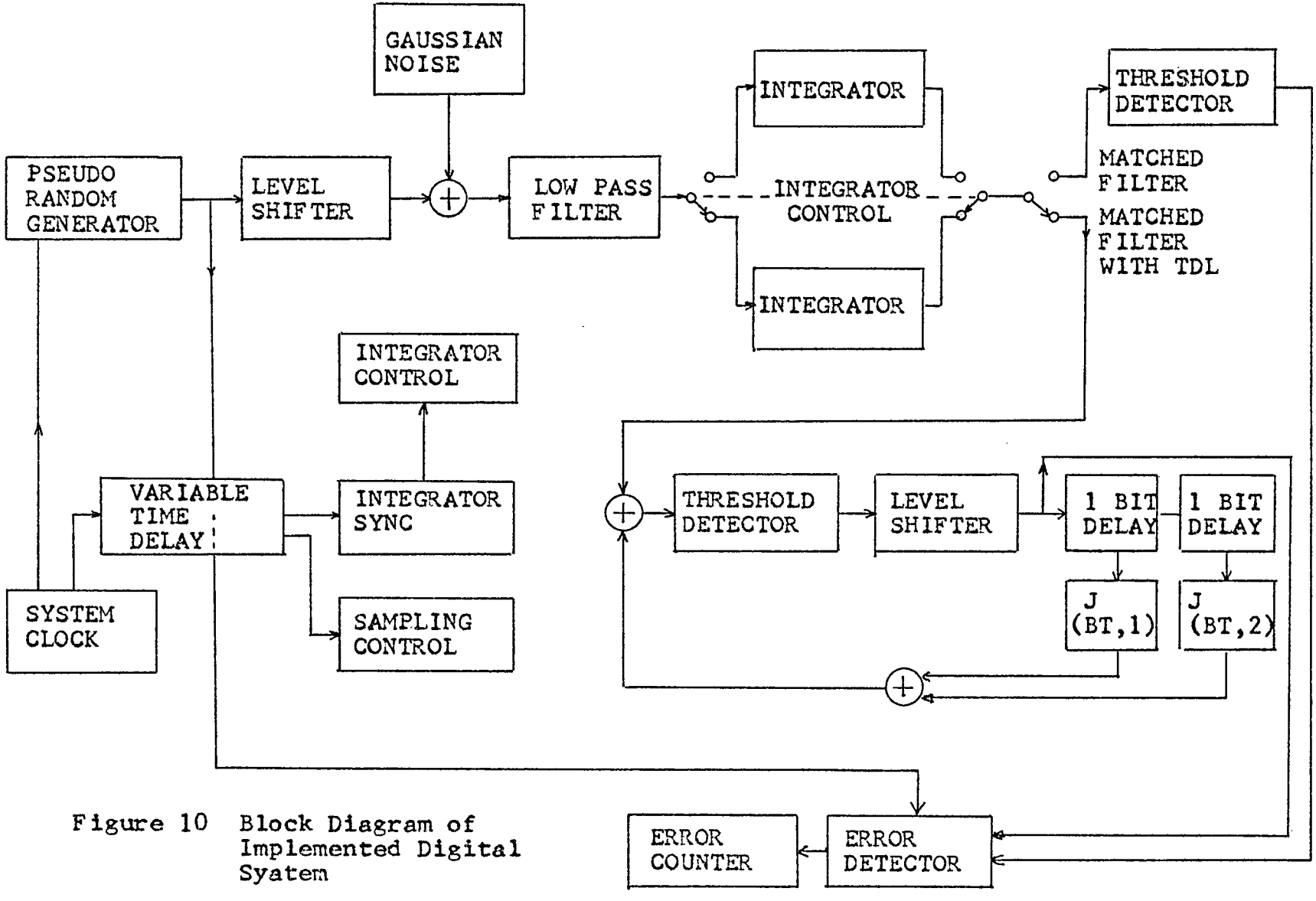
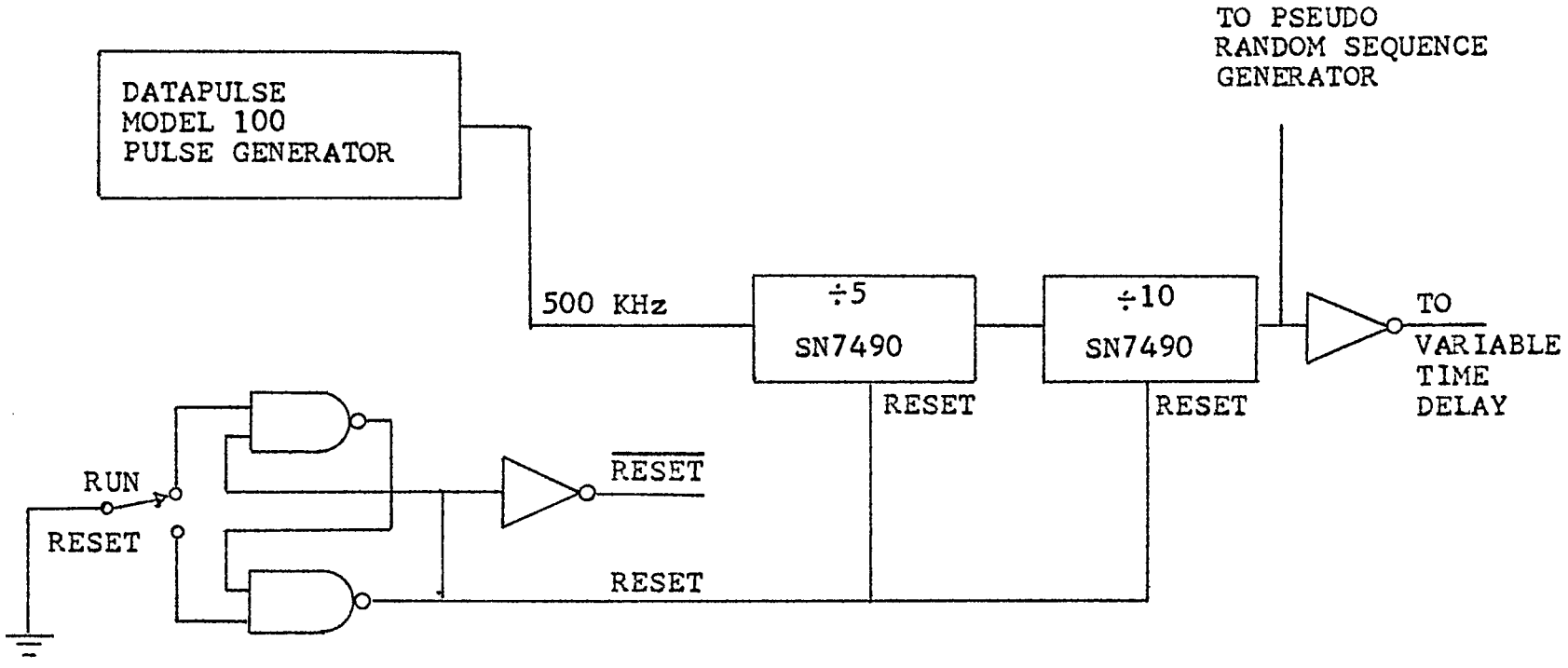


Figure 10 Block Diagram of Implemented Digital Syatem



ALL 2-INPUT NAND -- 946
ALL INVERTERS -- 932

Figure 11 System Clock with Reset Control

has been provided for resetting the system to a known starting point.

A pseudo random sequence generator (also known as PN (pseudo noise) sequence) is shown in Fig. 12 and Fig. 13. It consists of an eleven stage shift register, SR1-11, with exclusive-or gate (modulo-2 addition) feedback from stages one, two, three, eight, ten and eleven. This is shown in block diagram form in Fig. 14.

Pseudo random sequences possess three basic properties [6] which are:

1) Cycle-and-add - The modulo-2 sum of a given PN code and any cyclic permutation of the same PN code is another cyclic permutation of the PN code. Example: In this system the PN length is 11. A code permutation, 1101110 0001, and another permutation, 01110110010, form a modulo-2 sum, 10101010011, which is another permutation of the PN code.
2) Balance - For any cyclic permutation of the PN code, the total number of "1" 's differs from the total number of "0" 's by one. In the above example, there are six "1" 's and five "0" 's in any of the PN code permutations.
3) Run - The number of runs of length N is defined as the number of N consecutive bits of the same state having adjacent bits of the opposite states. In a period, the number of funs of length one is half the number of "1" 's or "0" 's. The number of runs of length greater than one, N, is equal to $1/2^{N-1}$ of that of length N-1.

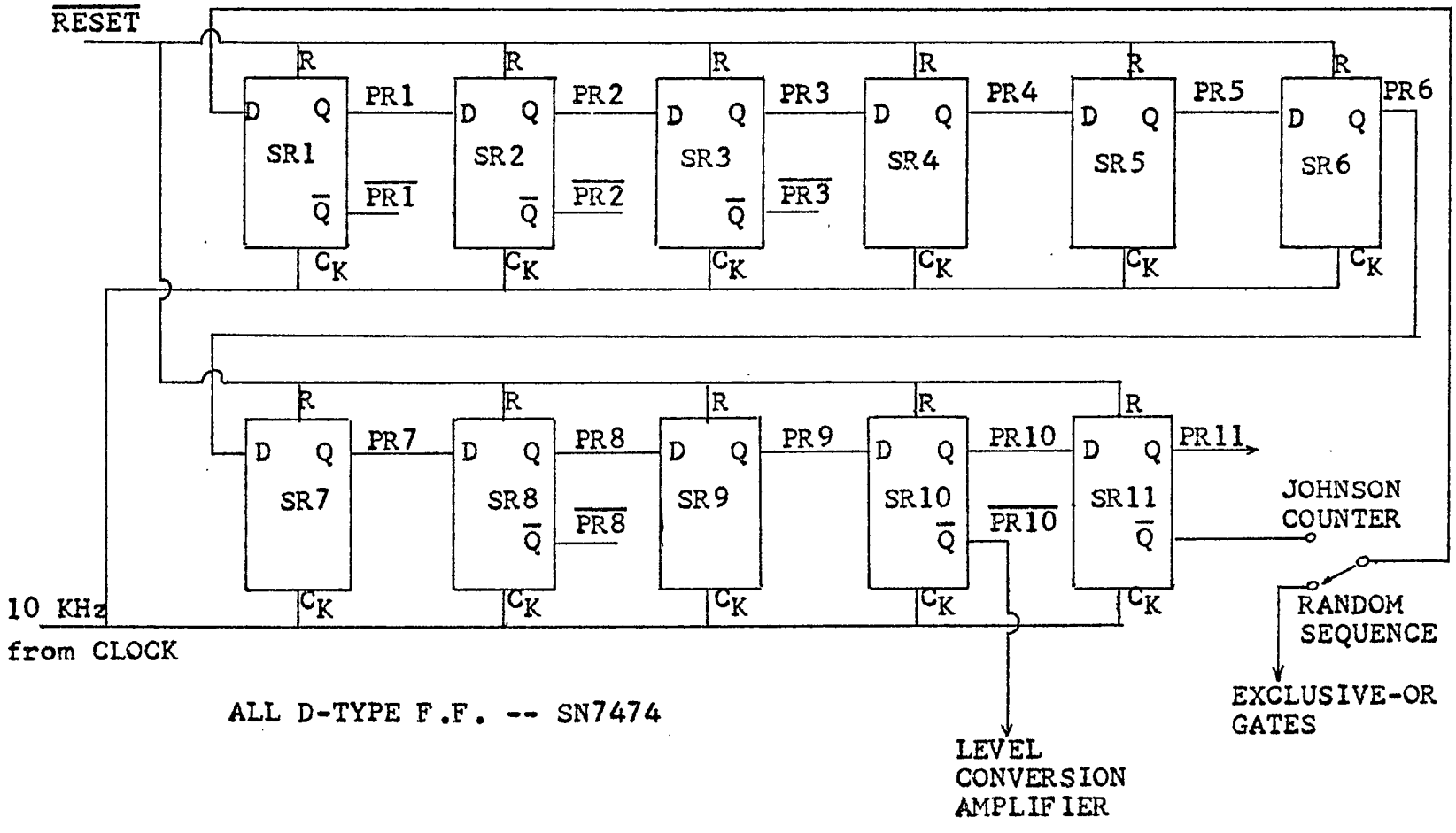


Figure 12 Psuedo Random Sequence Generator - Shift Registers

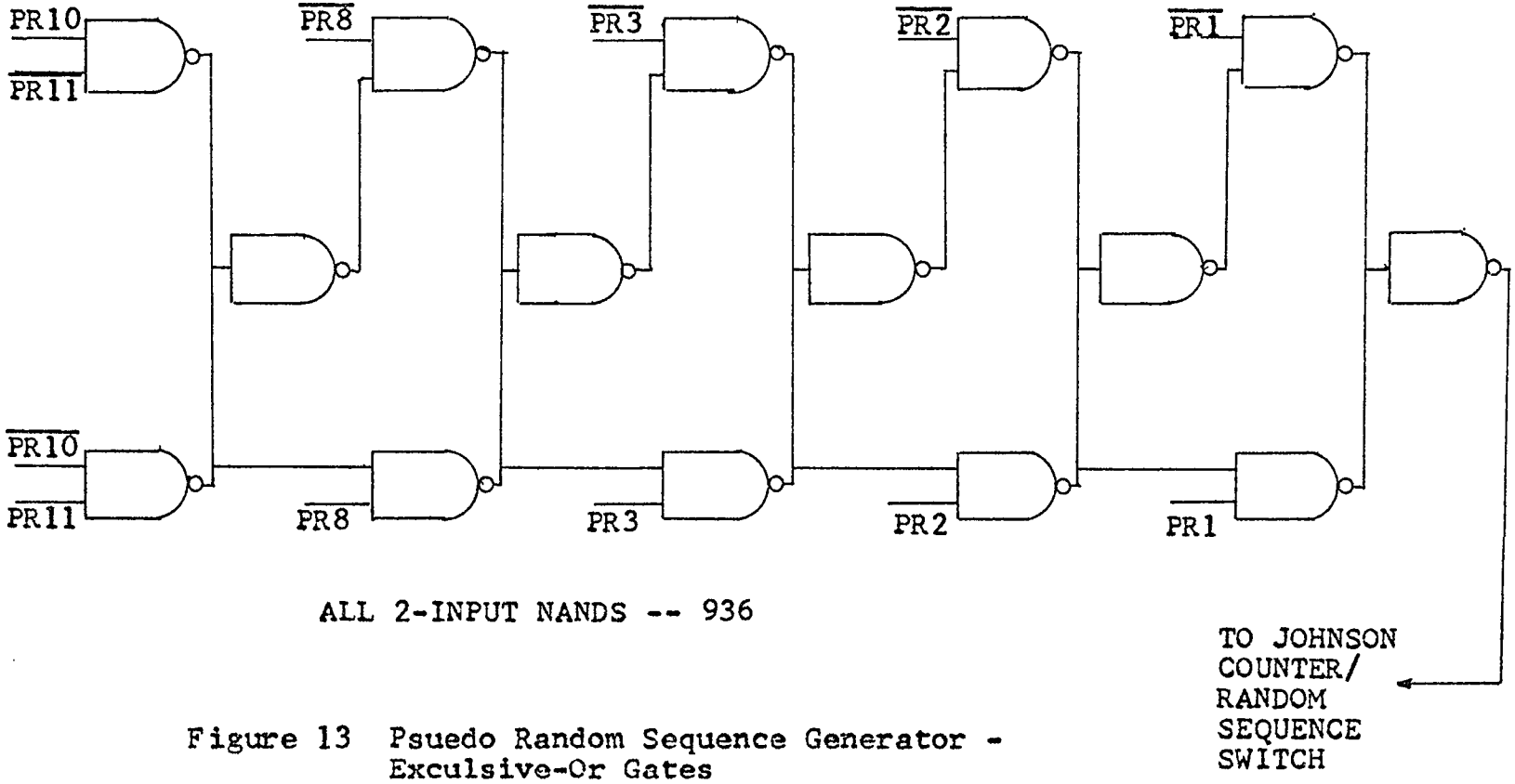
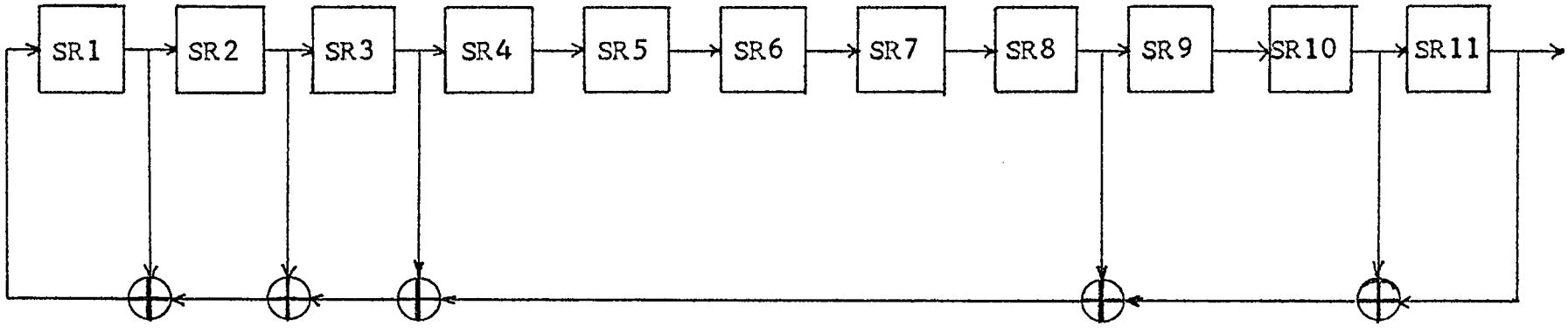


Figure 13 Psuedo Random Sequence Generator - Exculsive-Or Gates



⊕ DENOTES MODULO-2 ADDITION

Figure 14 Block Diagram of Pseudo Random Sequence Generator

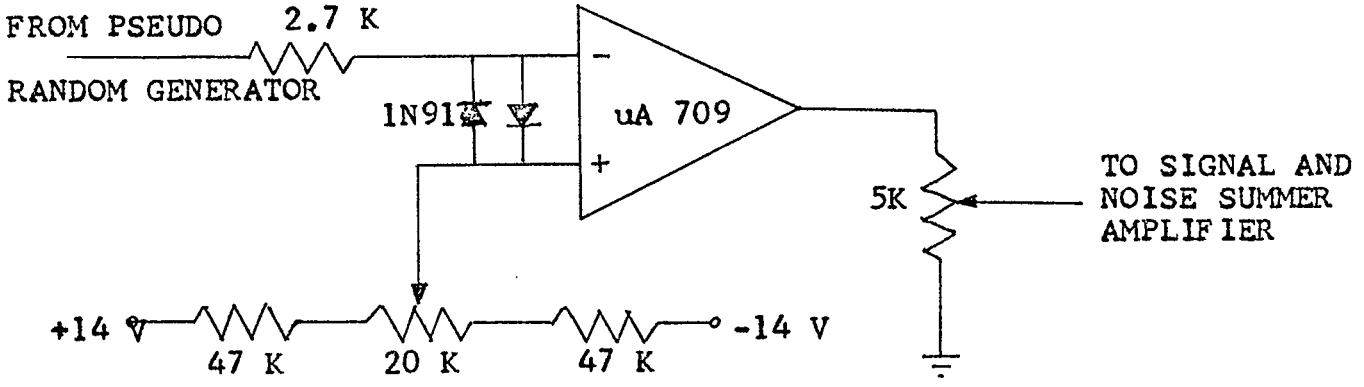


Figure 15 Level Conversion Amplifier

The output of the pseudo random sequence generator is taken from stage ten (SR10) and fed into a level conversion amplifier shown in Fig. 15. The amplifier converts the 0 V and +5 V levels of the TTL digital logic to a -14/+14 V level (NRZ signals). These voltage levels correspond to "0" and "1" repectively. The level conversion amplifier consists of a uA 709 operational amplifier operating at open loop gain. The threshold level is set so that the amplifier saturates at either +14 or -14 V depending on whether the input is above or below the threshold level.

The NRZ signals are summed with white additive Gaussian noise in the summing amplifier shown in Fig. 16. The summer output is passed through a Krohn-Hite lowpass filter which serves as the channel. The lowpass filter can be adjusted to provide any bandwidth required.

The lowpass filter output is connected to the integrator input FET (field effect transistor) switches shown in Fig. 17. The switches direct the input signal to the two integrators alternately. Two integrators are required since the discharge of the integrator capacitor requires a finite amount of time. An integrator is shown in Fig. 18. The FET discharge switch across the capacitor discharges the integrator between alternate integrations. The output of the integrators are connected to the integrator output FET switch shown in Fig. 19. These switches select the proper integra- output.

For the integrate-and-dump without tapped delay line

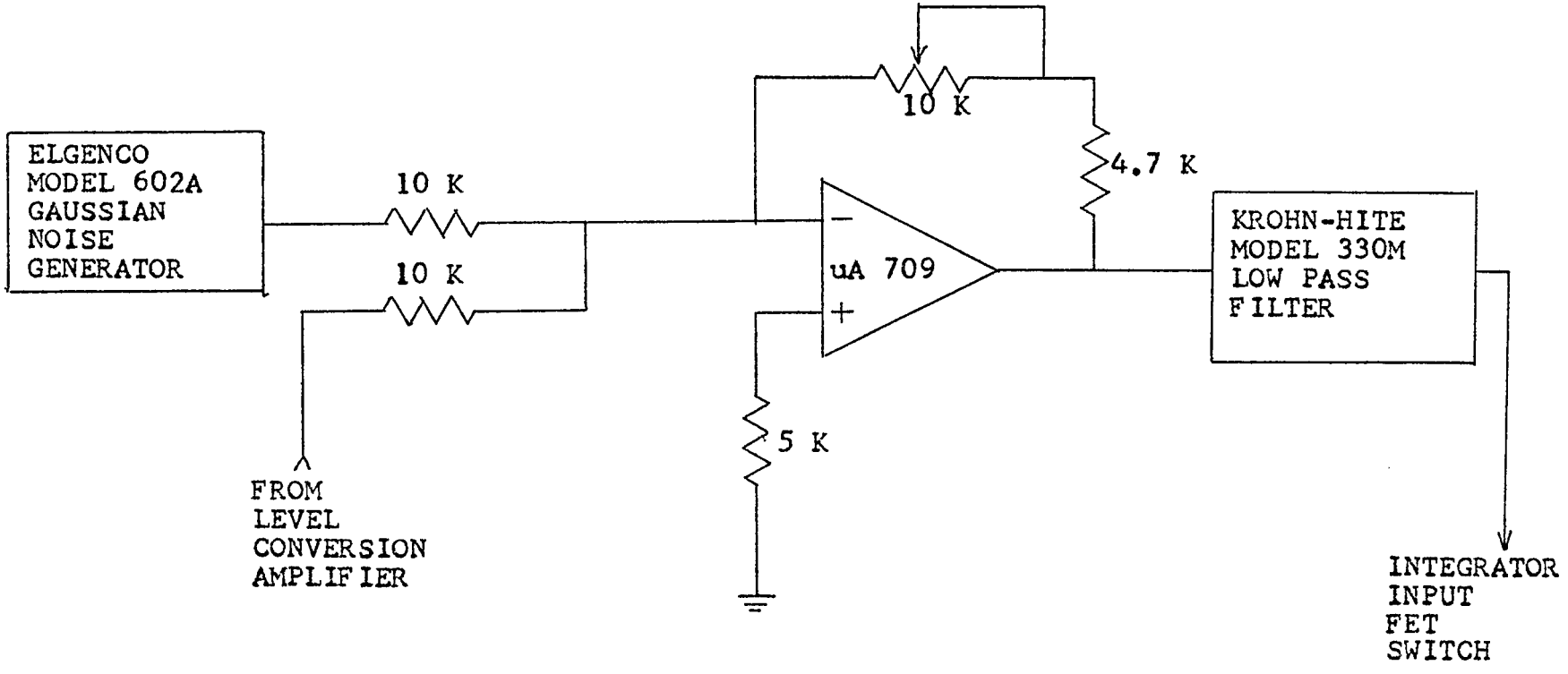


Figure 16 Signal and Noise Summer

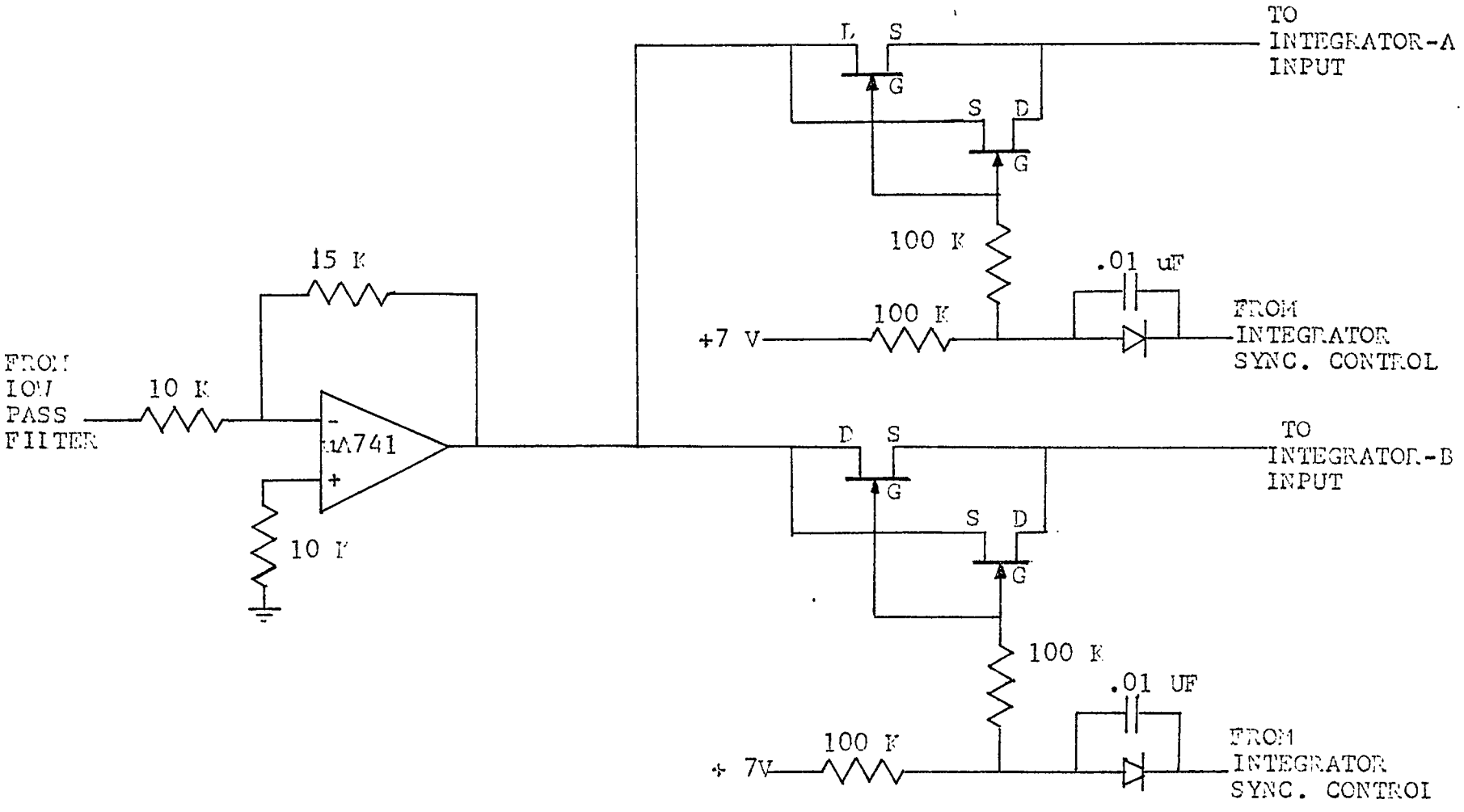


Figure 17 Integrator Input FET Switches

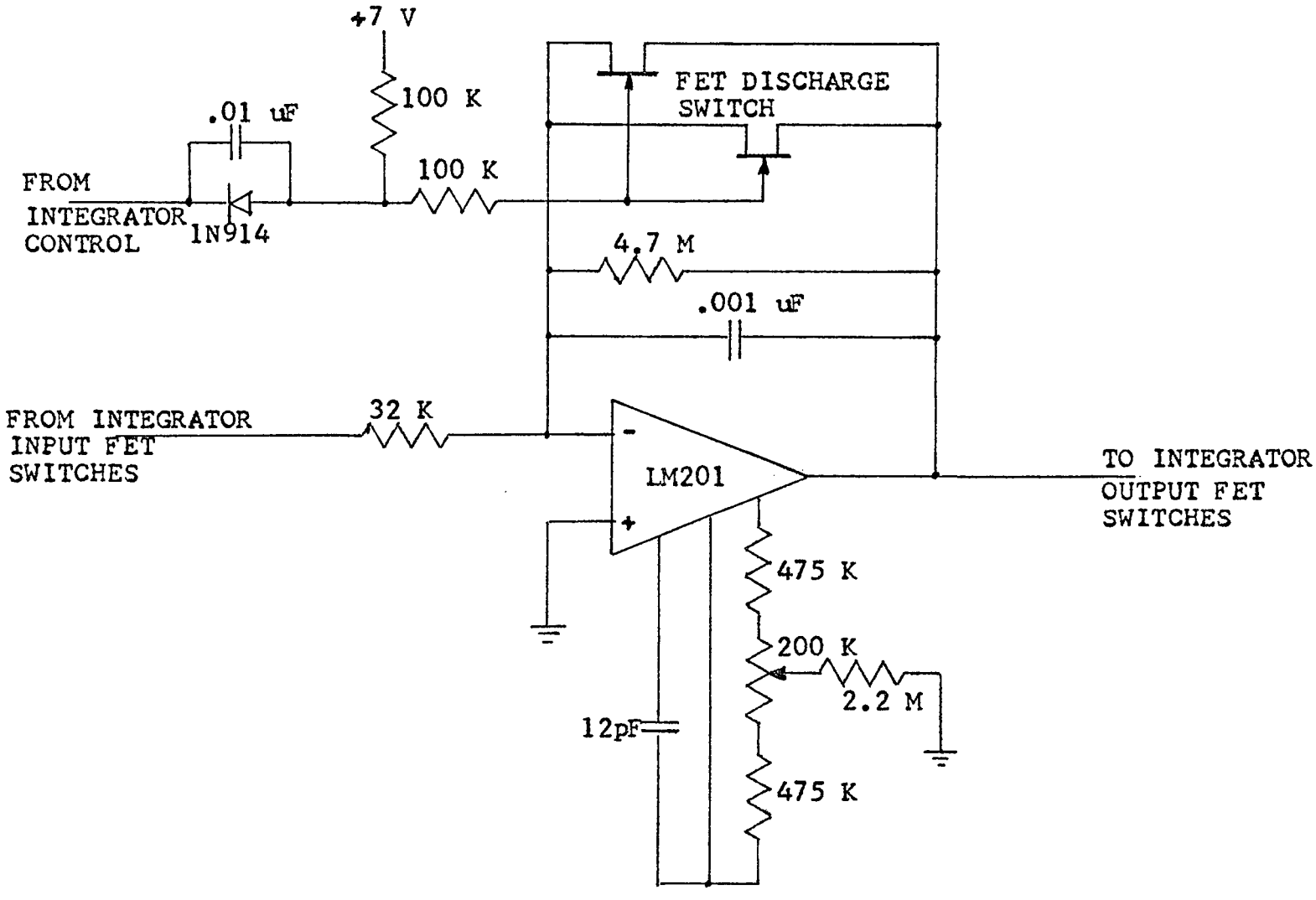


Figure 18 Integrator A (Same as for B)

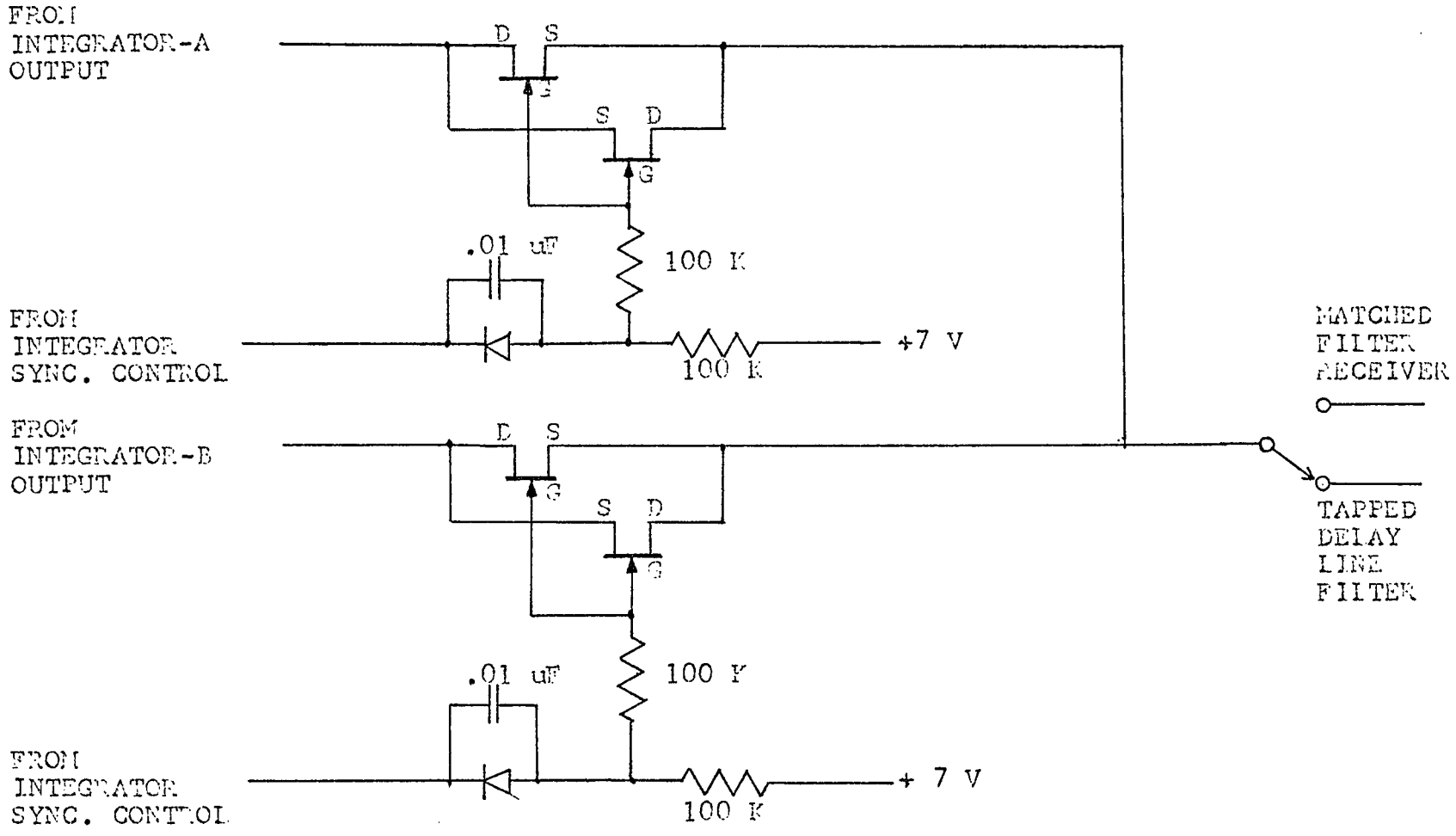


Figure 19 Integrator Output FET Switches

filtering, a threshold detector is used. This is shown in Fig. 20. A μA 741 operational amplifier is operated at open loop gain (~60 dB). Thus, with the offset input voltage of the operational amplifier adjusted to zero, the output is +14 V if the input is negative and -14 V if the input is positive. The transistor and diode convert the output to +5 or 0 V and is compatible with the TTL logic of the error detector.

The integrate-and-dump with tapped delay line filtering is shown in Fig. 21. The integrator output is summed along with the tap gain outputs (μA 709 summer). A seperate threshold detector is used (μA 741). After the threshold detector output levels are converted to binary signals compatible with the TTL logic, the binary bits are stored in the digital delay line. The delay line is formed from D-type flip-flops used as shift registers. The bit in SR12 is the first bit preceding the one under detection. The bit in SR 13 is the second bit preceding the one under detection.

The output of the taps in the delay line are connected to the tap gain amplifier in Fig. 22. The tap gain amplifier converts the 0/+5 V levels to -14/+14 V levels. The output of the tap gain can be adjusted to whatever gain is required by the bandwidth of the system by the 100 K potentiometer. The outputs of the tap gains are summed together as shown in Fig. 23 before being added to the integrator signal.

The variable time delay and integrator synchronization circuits are shown in Fig. 24. The time delay circuit con-

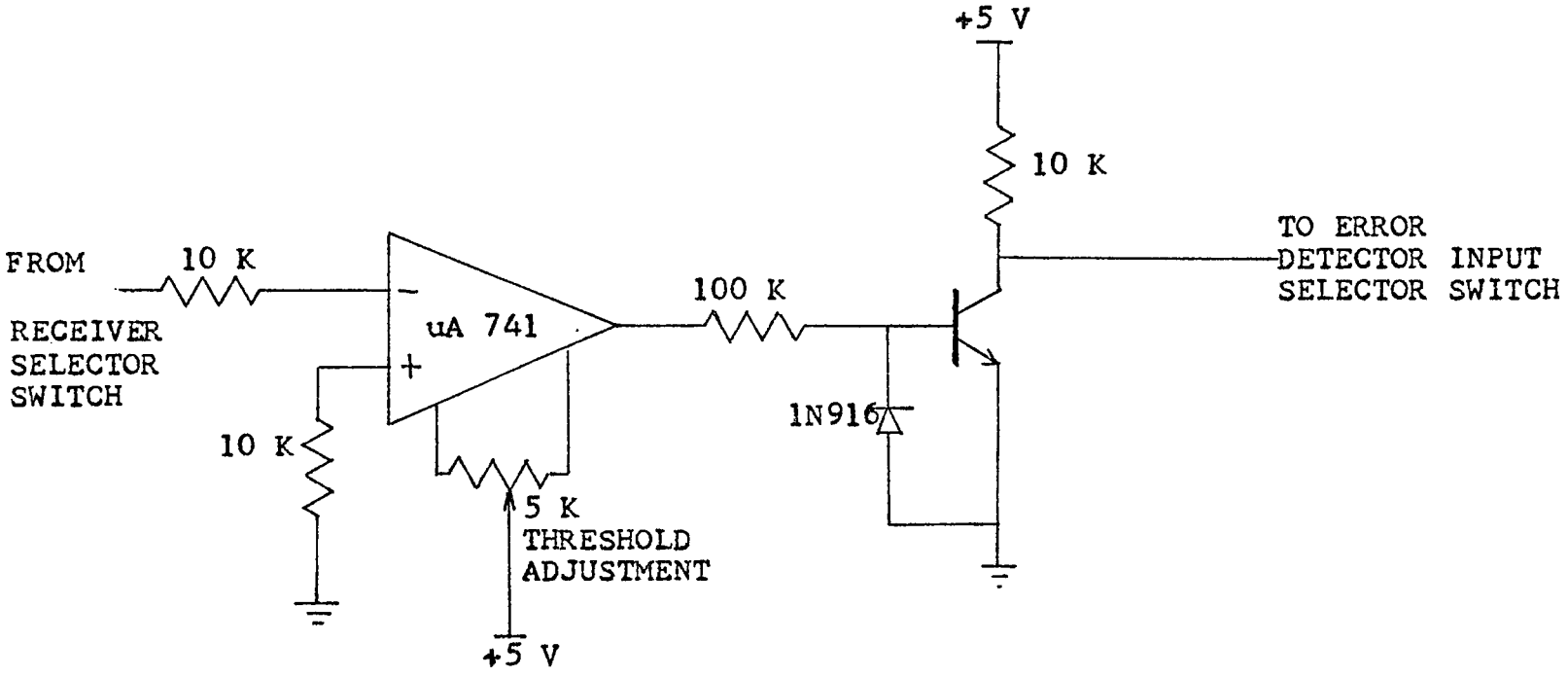


Figure 20 Threshold Detector for Integrate-and-Dump Detector Receiver

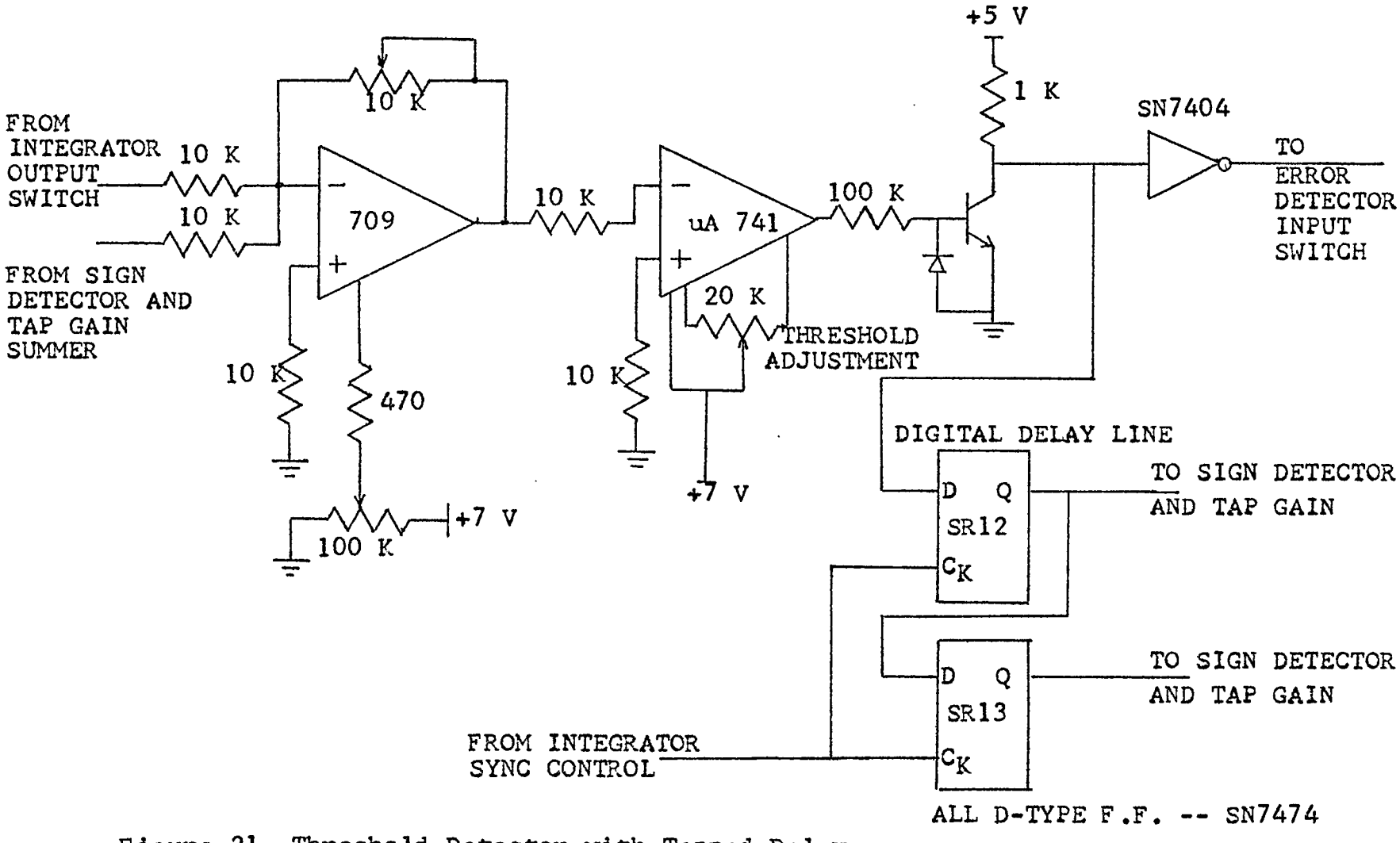


Figure 21 Threshold Detector with Tapped Delay Line Filter

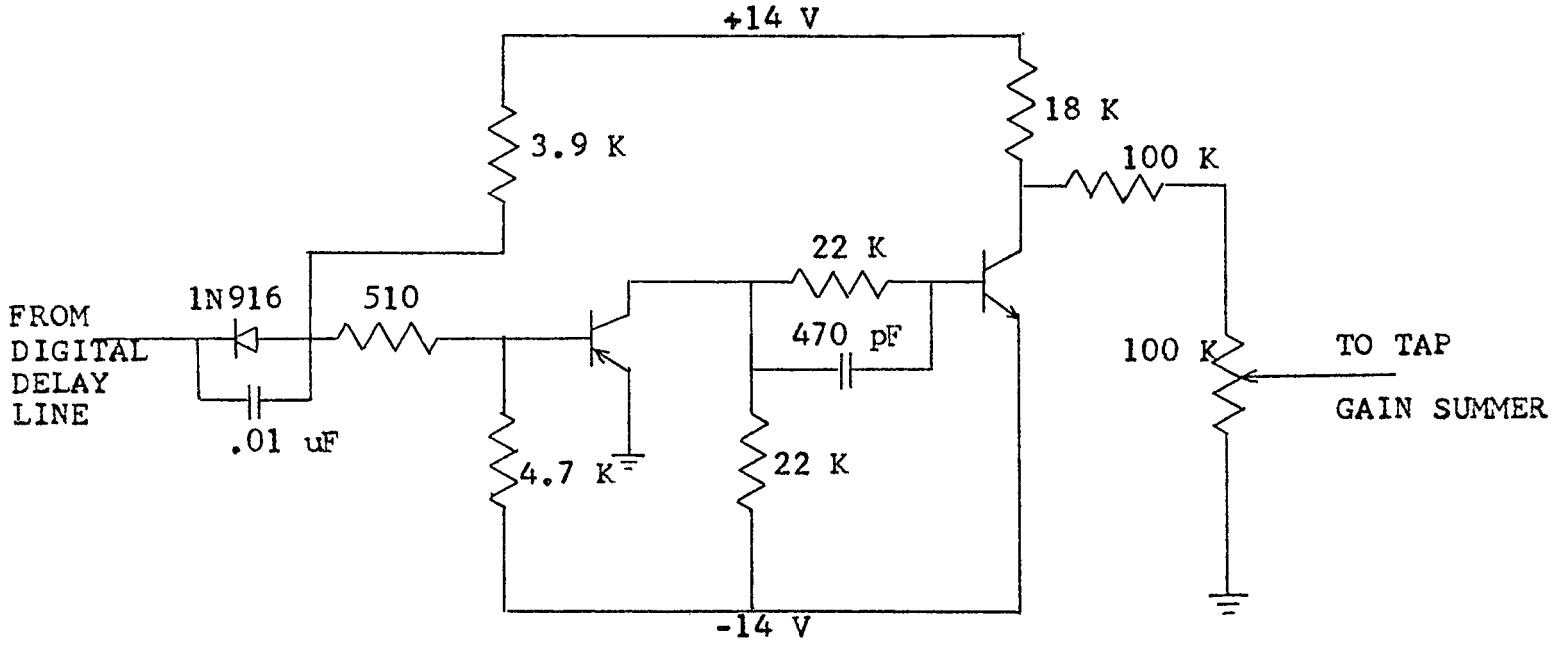


Figure 22 Tap Gain Amplifier (Two Used)

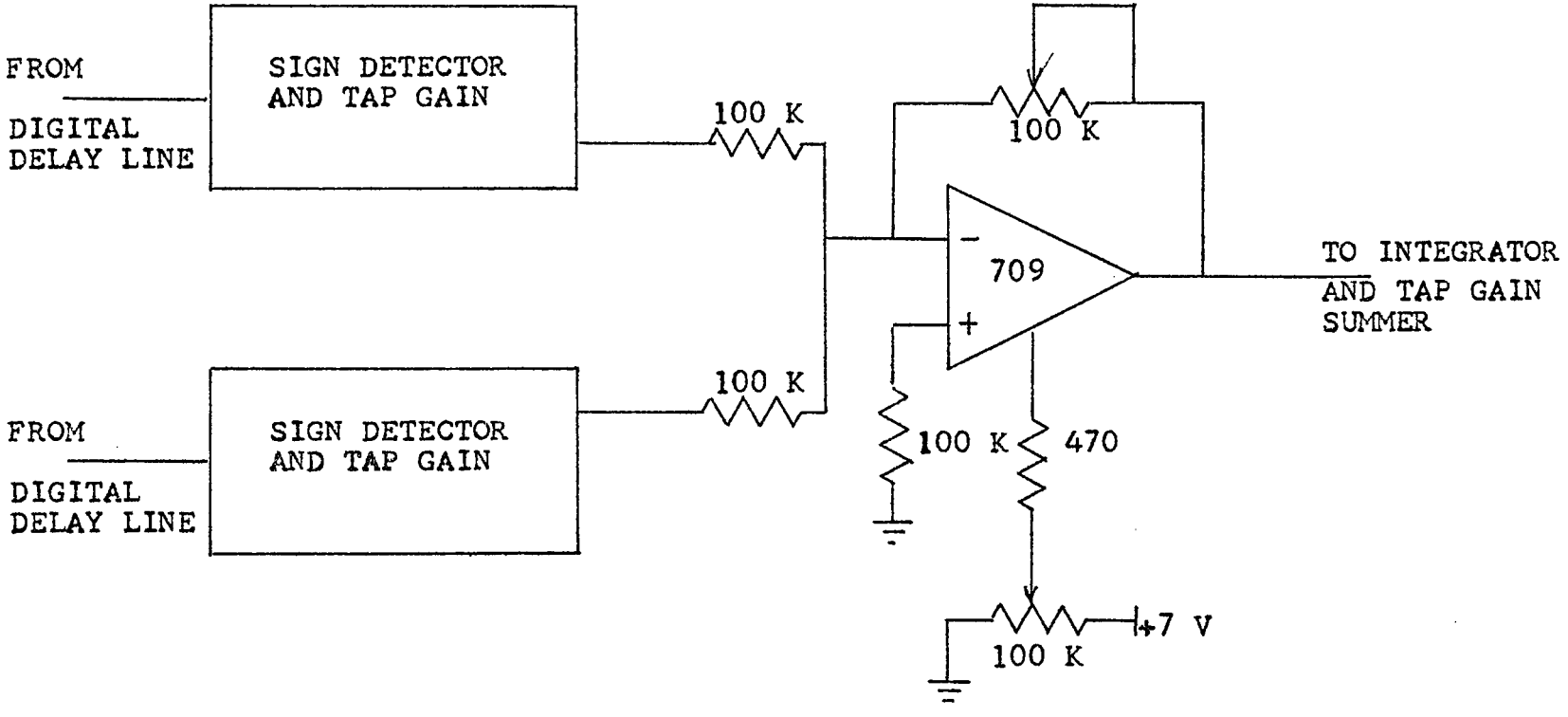


Figure 23 Tap Gain Summer

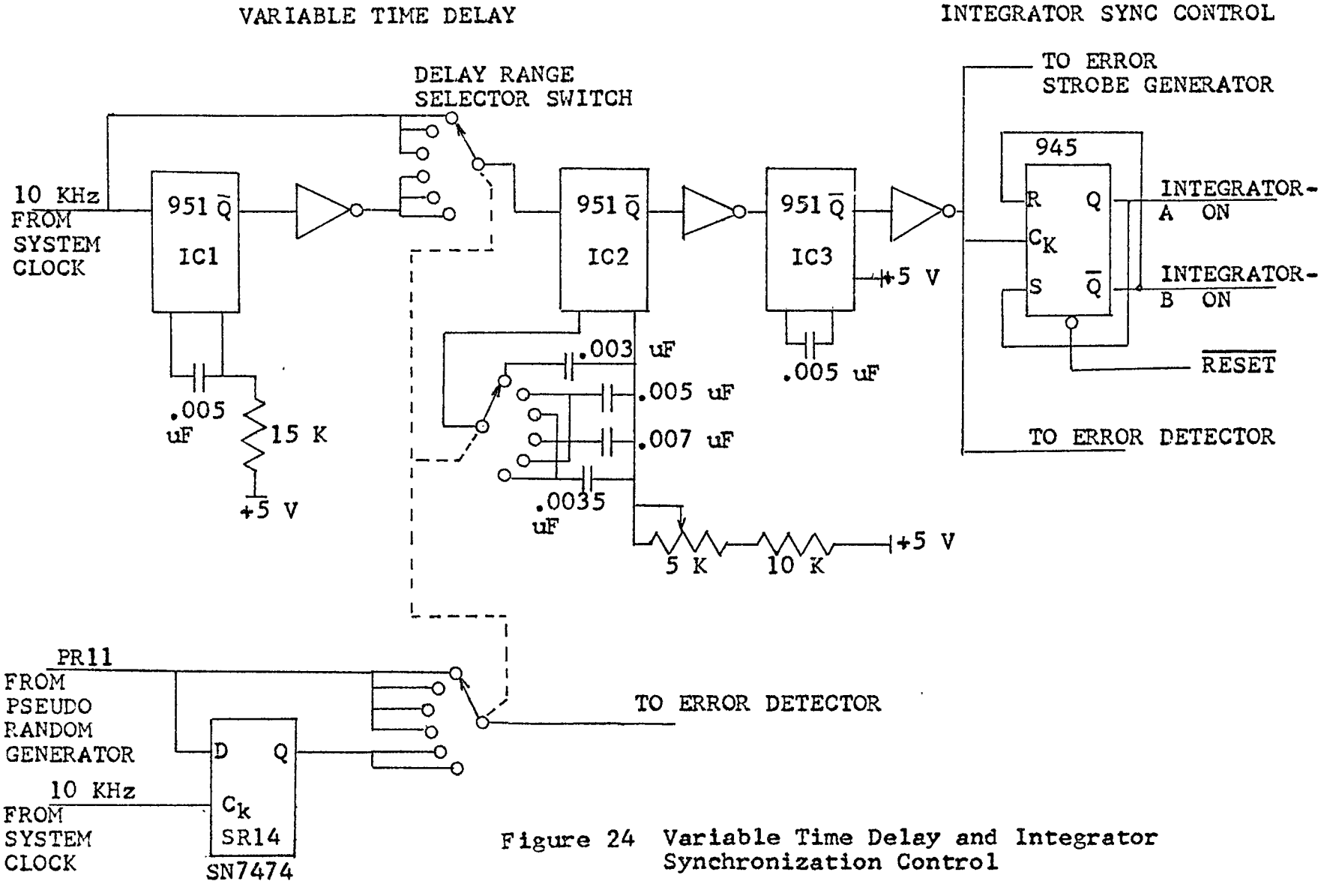


Figure 24 Variable Time Delay and Integrator Synchronization Control

sists of three μL 951 monostable multivibrators. The multivibrators are connected such that the output of IC3 is a delayed version of the system clock pulse. The timing capacitor of IC2 can be switch selected and the timing potentiometer can be adjusted to provide continuous time delays. An additional fixed time delay can be added to the variable delay by switching in IC1. Since the binary bit to the error detector is taken from SR11 (Fig. 12), it will be delayed by 100 μsec from the transmitted bit. An additional 100 μsec delay can be added to the bit entering the error detector by switching in SR14 (Fig. 24).

The integrator synchronization control is driven directly by the delayed clocked pulse from the variable time delay circuit. The control circuit consists of a R-S flip-flop connected to change states with each clock pulse, i.e., a toggle flip-flop. The state of the R-S flip-flop switches the received signal from one integrator to the other through the intergrator control.

The integrator control is shown in Fig. 25. It consists of six inverters and six level converters. The inputs, Integrator A-On and Integrator B-On, are always of opposite states since they are connected to the Q and $\overline{Q}$ outputs of the R-S flip-flop. The Q and $\overline{Q}$ outputs change states at a 5 KHz rate. When the Integrator A-On input is "high", the input signal is connected to integrator A input and the integrator output is connected to the input of the receiver selector switch through the input FET switches (Fig. 17). At the

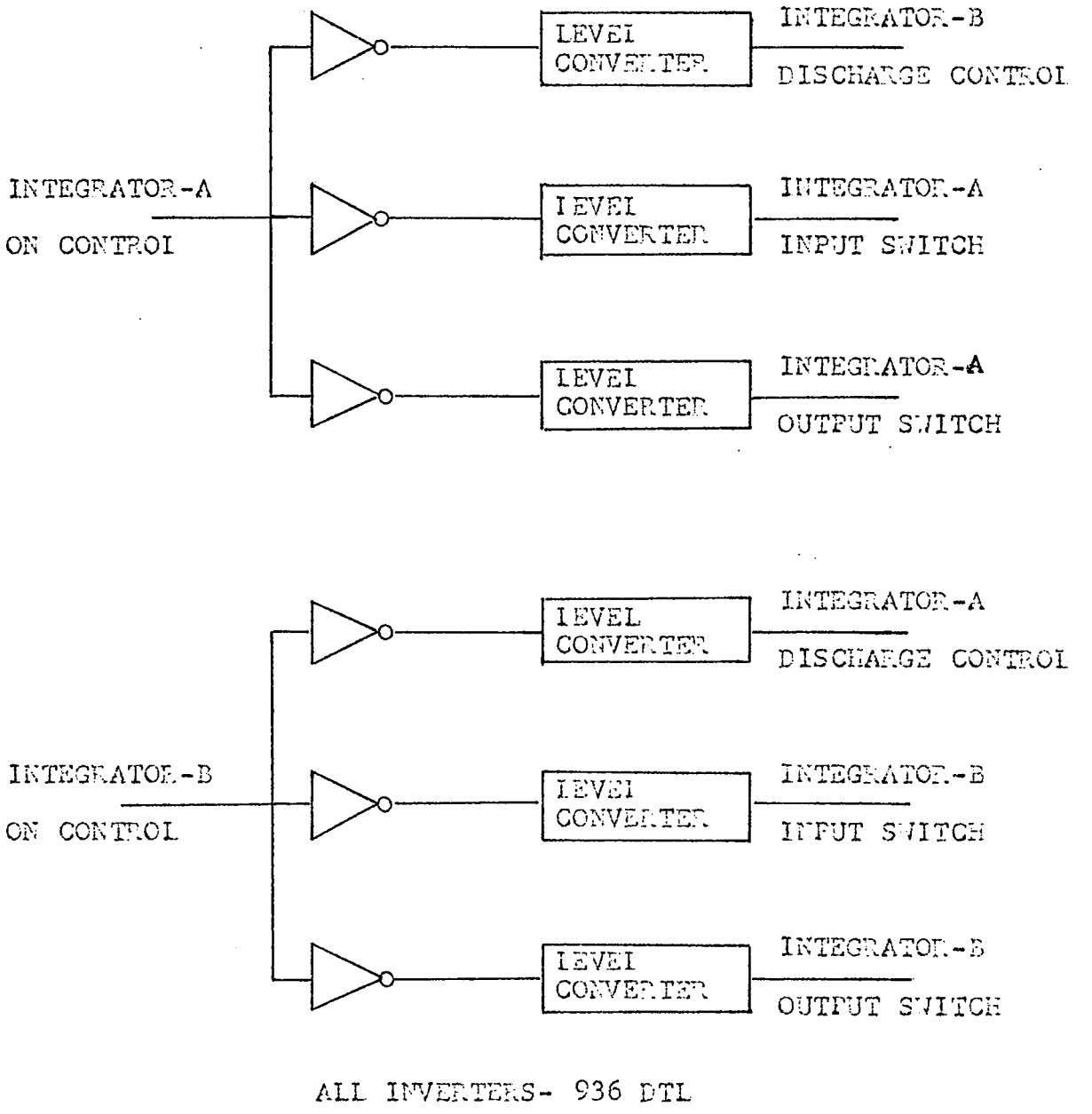


Figure 25 Integrator Switch Control

same time, integrator B is discharged through its discharge control switch (Fig. 18). When the R-S flip-flop changes states, the Integrator A-On Control goes "low" and the Integrator B-On Control goes "high". The received signal is switched from Integrator A to Integrator B. Integrator A is is discharged at this time. Thus the integrators intergrate the received signal on alternating bits and are discharged between the bits being integrated.

The level converters are shown in Fig. 26. The level converters change the input voltage levels of 0 and +5 V to -14 and +14 V respectively. The -14 and +14 V levels are required to switch the FET's in the integrator input, output, and discharge switches on and off.

The error detector is shwon in Fig. 27. The two D-type flip-flops, SR15 and SR16, store the two bits from the transmitted signal and the detector output. Since there was a time lag between the transmission of a bit and the detector output, the variable time delay circuit accounts for this lag and the bits in the flip-flops are from the same bit period. The three 2-input NAND's and inverter form a coincidence detector. The output of the coincidence detector is zero whenever the states of the flip-flops are the same. When the states of the flip-flop are not the same, corresponding to an error in detection, a pulse is generated at the output by the error strobe generator. These pulses are then counted by a digital counter.

The error strobe generator is shown in Fig. 28. It

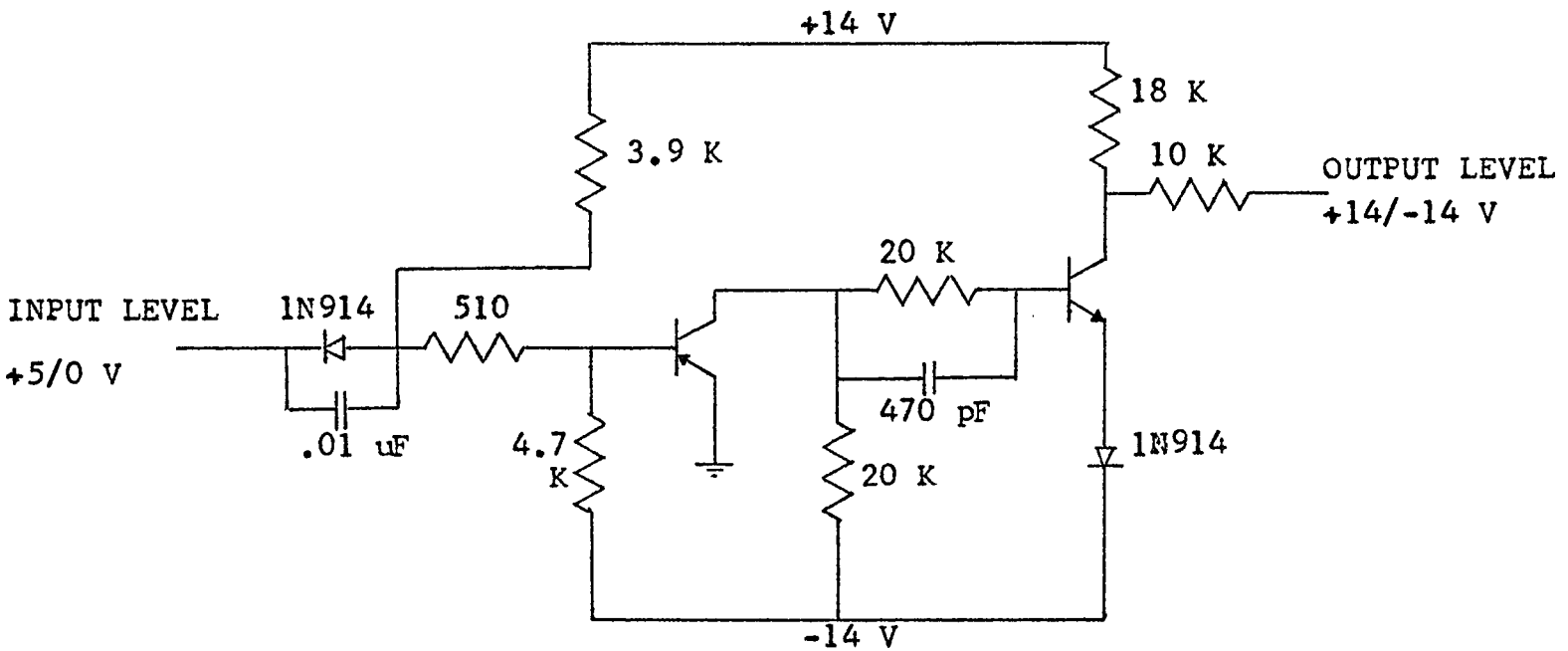


Figure 26 Typical Level Converter

ALL D-TYPE F.F. -- SN7474
ALL 2-INPUT NAND -- 946
ALL INVERTERS -- 936

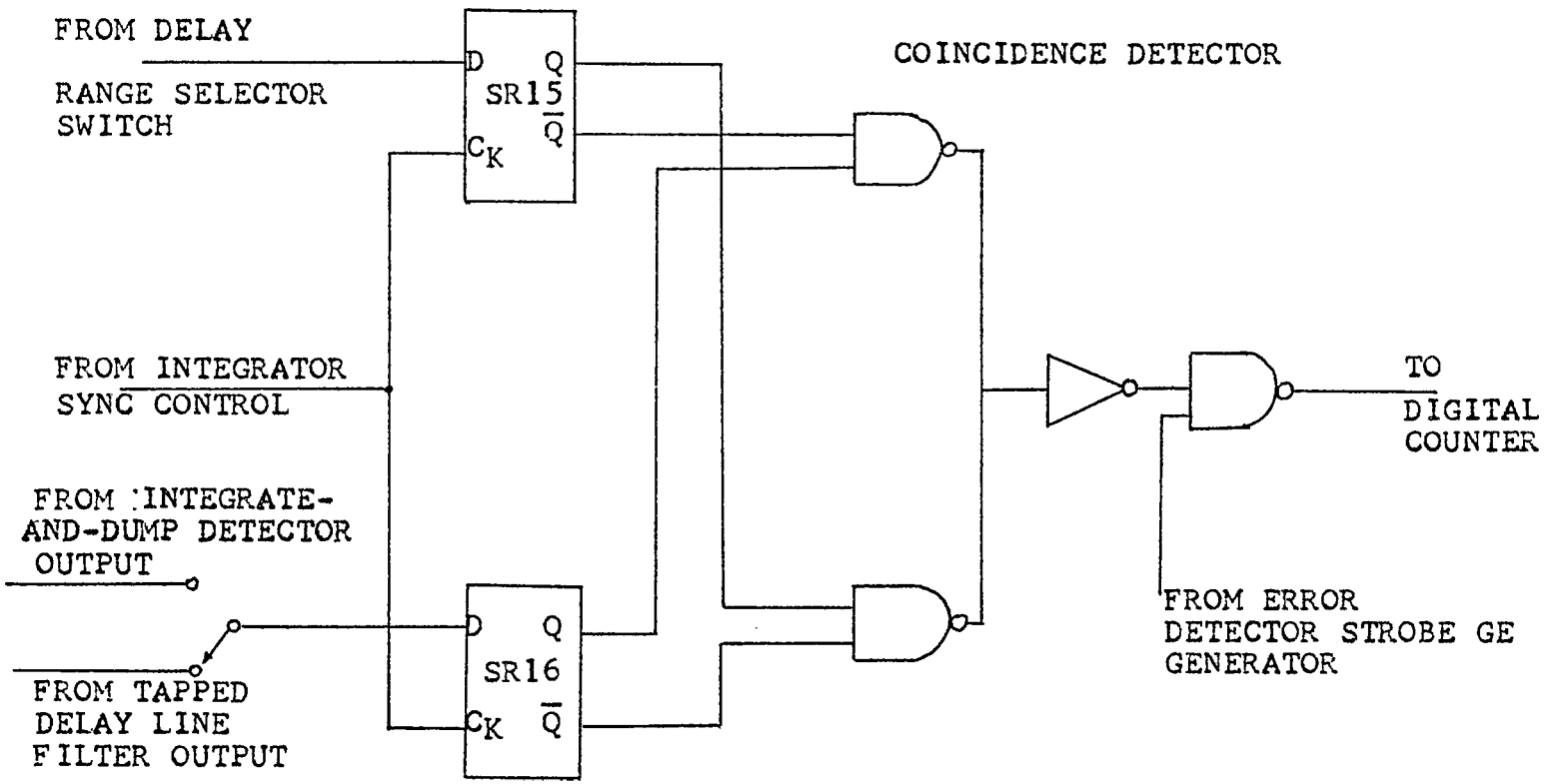


Figure 27 Error Detector and Counter

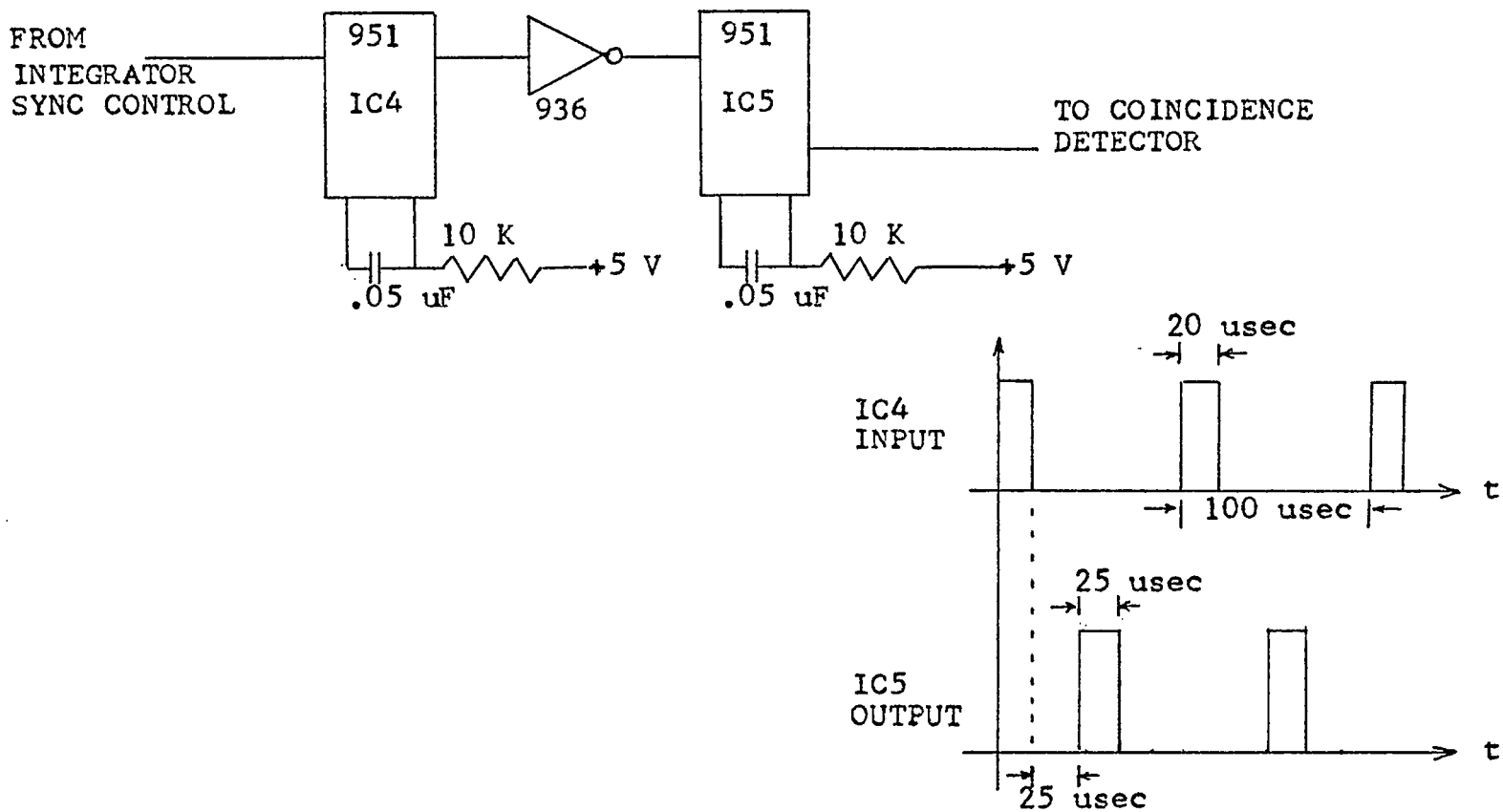


Figure 28 Error Strobe Generator

consists of two μL 951 monstable multivibrators. The timing capacitor and resistor are chosen such that a 25 μsec pulse is generated whenever IC4 is triggered by the integrator synchronization pulse from the variable time delay circuit. The output of IC5 is a 25 μsec wide pulse that appears in the middle of the integration timing period as shown in the timing diagram.

A synchronization and timing diagram of the clock and control pulses is shown in Fig. 29. The system clock pulse is shown in Fig. 29a. It consists of a 20 μsec wide pulse every 100 μsec. The positive going edge (point A in the diagram) of the pulse controls the D-type flip-flops used in the pseudo random sequence generator. The D-type flip-flops assume the input state during the positive going edge of the clock pulse. Thus the bit period of the binary signal starts at point A.

The μL 951 used in the variable time delay circuit is triggered on the negative going edge of the pulse (point B in Fig. 29b). The output of IC1 triggered by the inverted system clock is shown in Fig. 29b and 29c. The pulse width, t_1 in Fig. 29c, is fixed at 35 μsec. This is inverted and can be used to increase the time delay range of the variable time delay circuit. IC2 can also be triggered from the inverted system clock or it can be triggered from the inverted IC1. The output pulse width, t_2 in Fig. 29e, is variable between 35 and 75 μsec. IC3 is triggered by IC2 and provides a 20 μsec wide pulse. This pulse is inverted (Fig. 29h) and

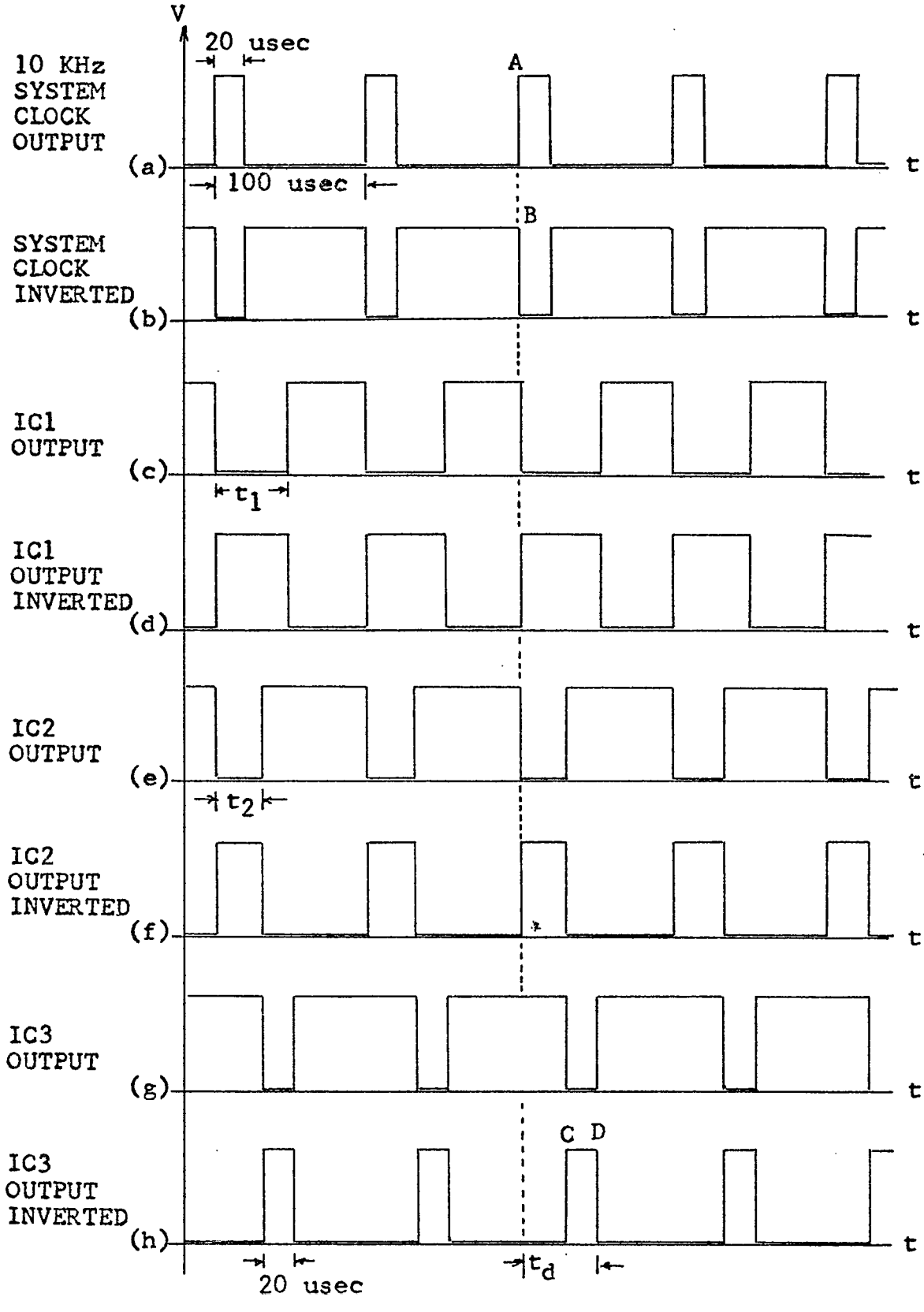


Figure 29 Synchronization and Timing Pulses in System

is used for integrator synchronization and sampling control.

The R-S flip-flop in the integrator synchronization control is clocked by the inverted output of IC3. The flip-flop changes state on the negative going edge of its clock pulse (point D in Fig. 29h). At the time it changes states, the integration period occurs between the negative going edges of the integrator synchronization pulses. The time delay between the transmitted pulse and the intergrator input is t_d. This time delay is given by

$$t_d = t_2 + 20\ \mu sec$$

or

$$t_d = t_1 + t_2 + 20\ \mu sec$$

depending on whether t_1 is connected by the range selector switch. Along with the bit period delay provided by SR13 and SR14, a time delay of 155 μsec to 225 μsec is obtained.

As noted before, the D-type flip-flop assumes the state at its input terminal only during the positive going edge of the clock pulse. The flip-flop SR16 in the error detector (Fig. 27) has its input connected to the threshold detectors of the tow recivers through a selector switch. The clock input of this flip-flop is connected to the integrator synchronization control.

The flip-flop therefore takes a sample of the threshold detector's output at the point C of the pulse in Fig. 29h. This point is 20 μsec before the end of the of the integration period at which time the integrator is discharged. The flip-flop therefore performs the operation of the samp-

ler. Note that the sampler in this system follows the threshold detectors rather than preceding it as in Fig. 3. The results are the same in either case.

IV. EXPERIMENTAL RESULTS

4.1 Measurements

The signal-to-noise ratio was determined at the summer where the transmitted signal and the Gaussian noise were added together. This occurs before filtering by the channel. The signal-to-noise ratio is given by

$$SNR = 10 \log \frac{E}{N_o}$$

where E is the energy in the transmitted signal and N_o is the noise spectral power density.

The energy of a NRZ signal is

$$E = V_s^2 \, T \ (V^2\text{-sec})$$

where V_s is the amplitude of the pulse and T is the bit time duration. For this experiment V_s is 0.1 V and T is 10^{-4} sec.

The noise spectral density is given by

$$N_o = (5.0 \times 10^{-3} \times V_n)^2 \ (V^2/Hz)$$

where V_n is the rms value of the noise generator output. This was obtained from the operating manual for the noise generator.

The probability of error was obtained by counting the number of errors in the detection of 10^6 bits transmitted. The probability of error would then be

$$P\{\mathcal{E}\} = \frac{N}{10^6}$$

where N is the number of errors. Ten readings were made and

the results averaged in order to obtain the probability of error.

The tap gains in the delay line were determined experimentally by adjusting the gains until the error rate was minimized. It was found that optimim performance was obtained using only the first tap of the delay line. The second tap produced only a very small improvement in the performance of the receiver. This improvement was obtainable only for BT equal 0.5. This verified the calculated results that a single tap produced near optimum performance. Therefore, the performance was measured for the one-tap tapped delay line filter only.

4.2 Results and Conclusions

The error performance was found for the integrate-and-dump detector with and without the tapped delay line filter. The receiver was operated at BT=0.5, 0.6, 0.7, 0.8, 1.0, 1.5, and 2.0 with the SNR=6, 8, 10, and 12 dB. The results are listed in Table 6. These results are shown in graphical form in Fig. 30.

The results in Fig. 30 verified that near optimum results are obtained at BT=.8 for either system since little improvement was obtained as BT was increased above 0.8. The addition of the tapped delay line filter improved the performance of the integrate-and-dump detector at all values of BT except 2.0. However, the improvement was insignificant for BT≥1.0 as was predicted by the analytical results obtained eariler.

TABLE 6

EXPERIMENTAL RESULTS

BT	SNR (DB)	INTEGRATE-AND-DUMP DETECTOR LOG P(E)	INTEGRATE-AND-DUMP WITH TAPPED DELAY LINE FILTER LOG P(E)
0.5	6	-1.716	-1.838
	8	-2.157	-2.273
	10	-2.740	-3.056
	12	-3.22	-3.886
0.6	6	-1.850	-1.889
	8	-2.374	-2.475
	10	-3.230	-3.553
	12	-4.097	-4.398
0.7	6	-1.996	-2.005
	8	-2.582	-2.600
	10	-3.606	-3.620
	12	-4.523	-4.602
0.8	6	-2.112	-2.200
	8	-2.949	-3.022
	10	-4.097	-4.398
	12	-6.000	
1.0	6	-2.132	-2.200
	8	-3.066	-3.097
	10	-4.222	-4.398
1.5	6	-2.158	-2.163
	8	-3.056	-3.060
	10	-4.523	-4.290

TABLE 6 (CONT.)

BT	SNR (DB)	INTEGRATE-AND-DUMP DETECTOR LOG P(E)	INTEGRATE-AND-DUMP WITH TAPPED DELAY LINE FILTER LOG P(E)
2.0	6	-2.188	-2.188
	8	-3.075	-3.075
	10	-4.523	-4.523

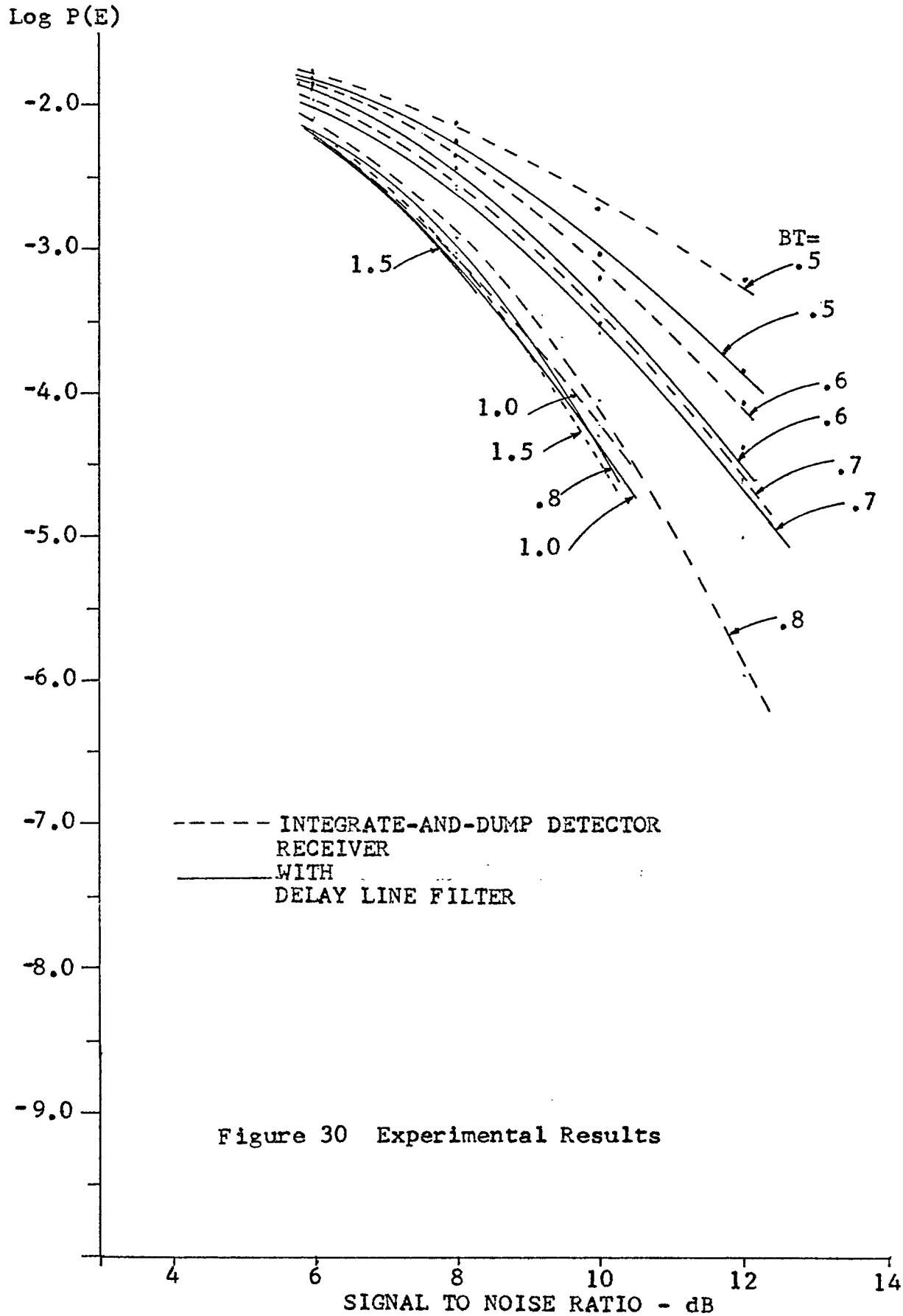


Figure 30 Experimental Results

Figure 31 shows the experimental results for BT=0.5 and 0.8 along with the calculated performance from the analysis. There is about 2 dB difference in performance between the experimental and calculated results for BT=0.5 and less than 1 dB difference for BT=0.8. The calculated results do not predict the performance of the experimental system with much accuracy. However, it does predict accurately, the amount of improvement in the performance of the integrate-and-dump detector by the addition of the tapped delay line filter. There is a 1 dB improvement for BT=0.5 and a 0.2 dB improvement for BT=0.8.

The differences in performance between the experimental and calculated results occur because of several factors. The physical lowpass filter does not give the same values for $J(BT,n)$ and σ^2 as was obtained by using an ideal filter in the analysis. The physical system was not accurately modeled in the analysis. The noise in the actual receiver was not accounted for. Since the sampling was made at 0.8T rather than at T, some energy in the received signal is lost.

The experimental results does verify that an optimum system can be obtained using an integrate-and-dump detector with a one-tap tapped delay line operating at BT=0.8. An increase in BT does not improve the performance significantly and a decrease in BT degrades the performance significantly.

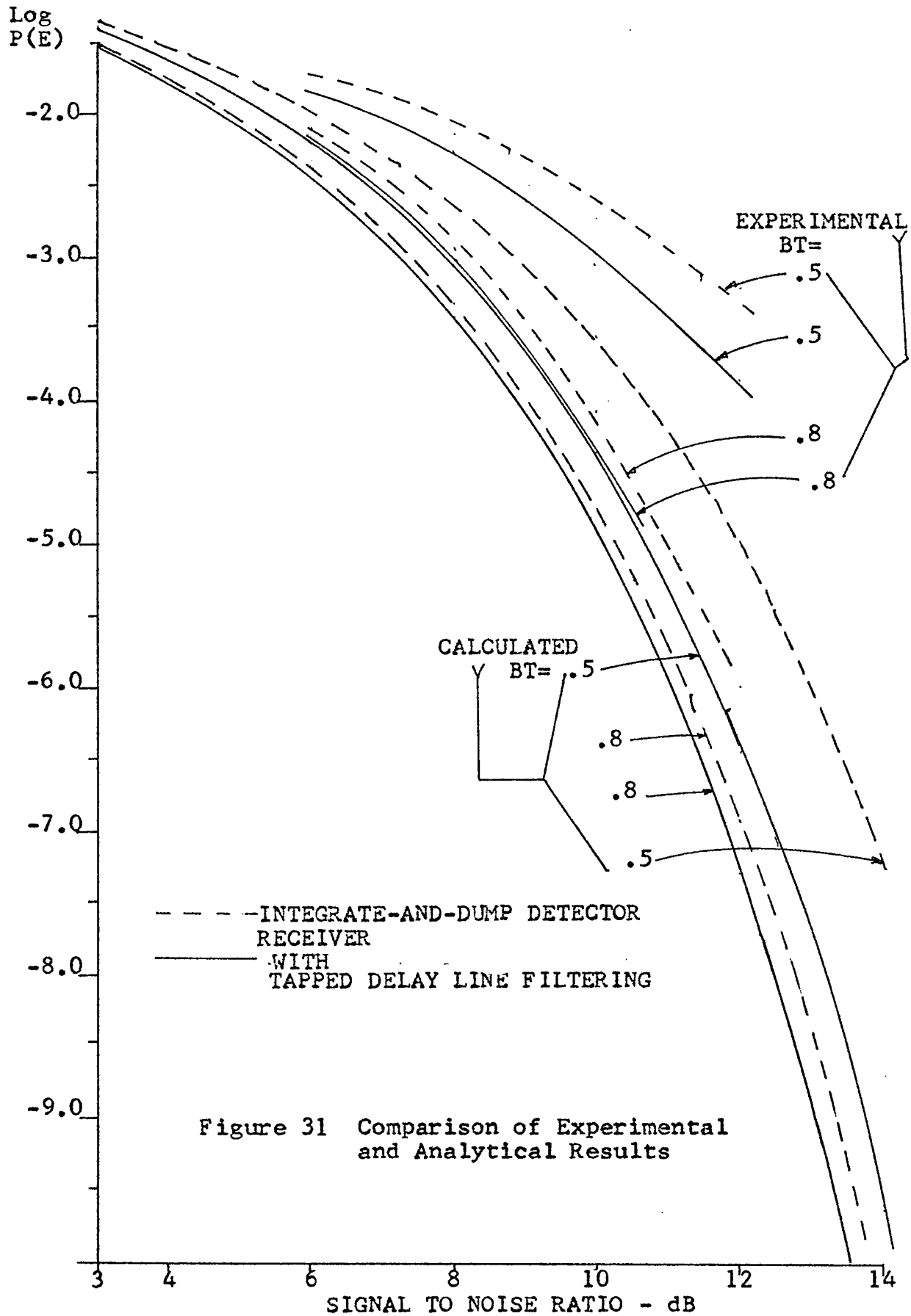


Figure 31 Comparison of Experimental and Analytical Results

V. COMPARISON OF OTHER RECEIVER STRUCTURES

5.1 Tu - Tapped Delay Line Filter

Kwei Tu [2] analyzed a tapped delay line of the form shown in Fig. 2. Tu analyzed the system assumming that the intersymbol interference was limited to the ten nearest bits; five bits preceding and five bits following the bit under detection. The delay line had three taps: C_{-1}, C_0, and C_1. There was no decision feedback used in this receiver structure. An analysis was also made for the integrate-and-dump detector.

The results from Tu's paper are shown in Fig. 32 along with the calculated results of this thesis. The performance of Tu's analysis was poorer as would be expected since interference from both future and past bits was considered. Also, the interference was not limited to only two bits but was extended to ten bits.

There is a 2 dB difference in performance for the integrate-and-dump detectors at BT=0.5 and a 0.2 dB difference at BT=0.8. For tapped delay line filtering, there is a 0.8 dB difference at BT=0.5 and a 0.1 dB difference at BT=0.8. The reason for the large differences in results for BT=0.5 is due to larger values of J(0.5,n) for n>2. Tu considered the increase of energy in the bits beyond the second bit from the bit under detection. This is shown somewhat by the experimental model. The second tap did improve the performance of the system. This improvement was limited to BT=0.5

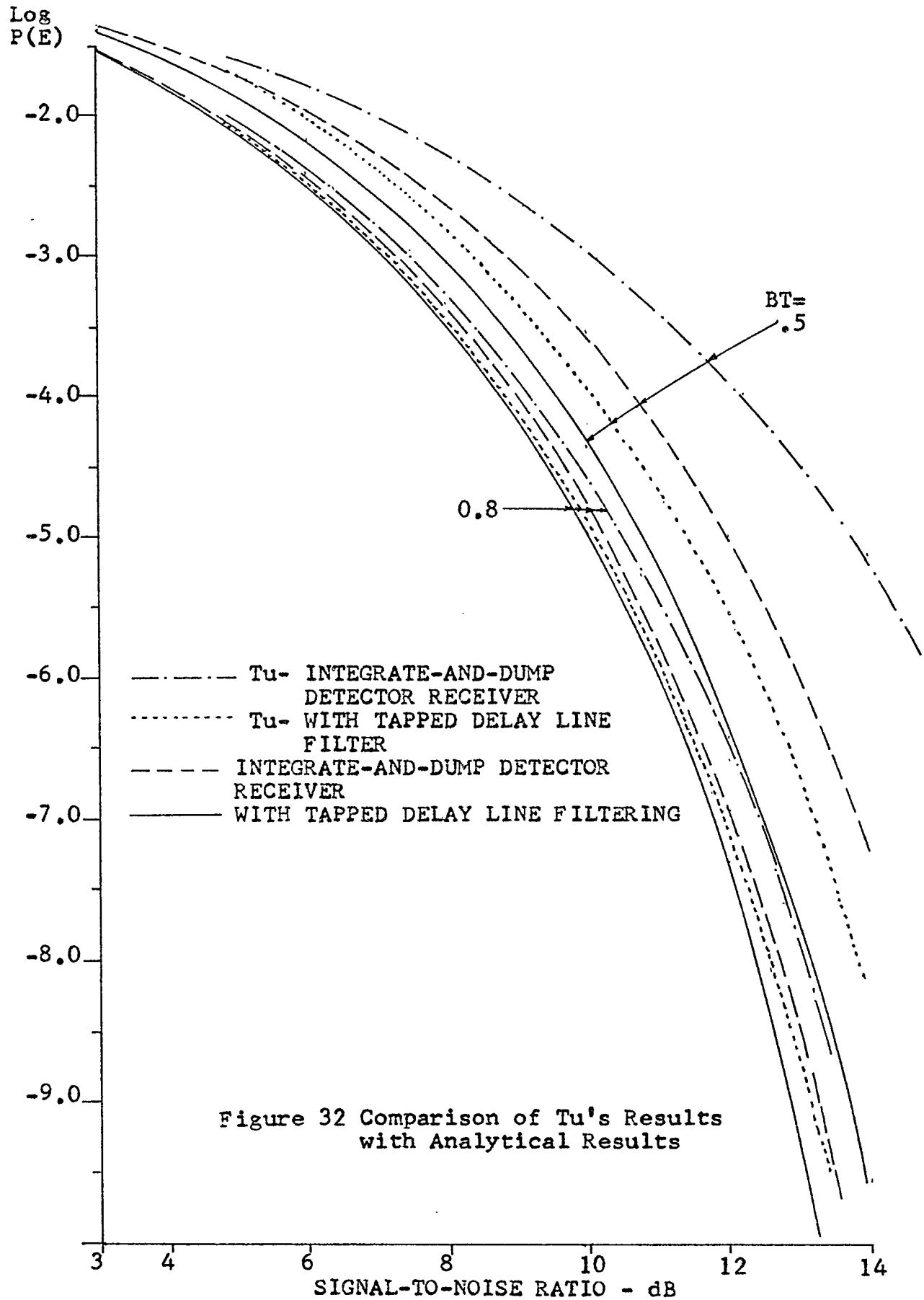


Figure 32 Comparison of Tu's Results with Analytical Results

and was small.

The experimental results was also compared to Tu's calculations in Fig. 33. Tu's results gave a tighter lower bound on the experimental results. However, Tu's calculations showed about a 2 dB improvement in the performance of the tapped delay line filter over the integrate-and-dump detector at BT=0.5. There was only about a 1 dB improvement in the experiemtal model which was also the amount predicted by the calculations in this thesis. At BT=0.8, there was only a slight difference in the amount of improvement predicted and the amount obtained experimentally.

5.2 Bershad and Vena - Channel State Estimation Receiver

Bershad and Vena[7] proposed a channel state estimation receiver using decision feedback for elimination of intersymbol interference. The receiver structure is shown in Fig. 34. It consists of an optimum linear filter, a conditional maximim-likelihood decision box that is conditioned on the previous receiver decisions, a conditional maximum-likelihood estimate of the channel state, and a variable threshold whose motion is controlled by the channel state estimate.

The receiver operates as follows; assume that a decision has been made on the last bit transmitted and the present bit (the bit to be detected) appears at the input of the optimum linear filter along with additive Gaussian noise. A conditional maximum likelihood estimate of the channel state is made from the decision made on the previous bit.

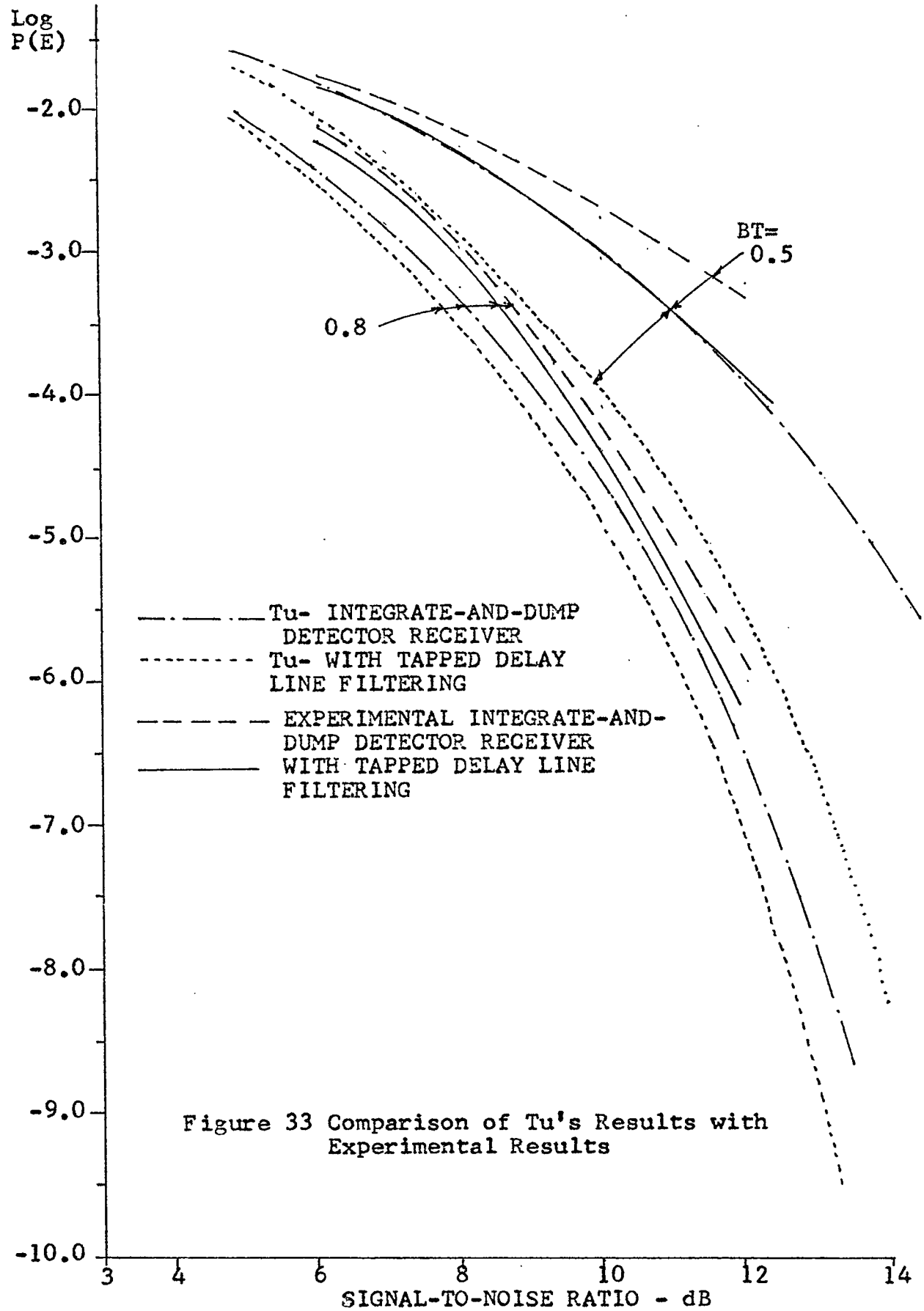


Figure 33 Comparison of Tu's Results with Experimental Results

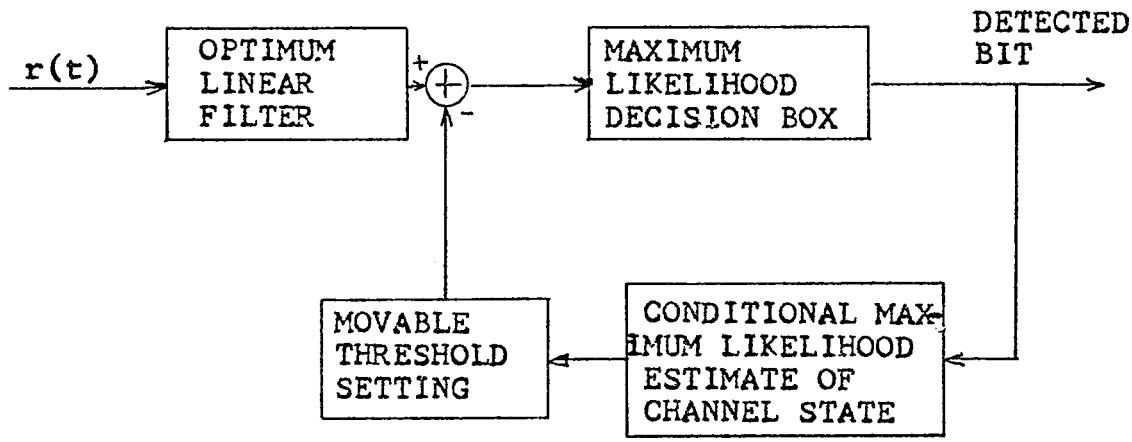


Figure 34 Structure of Bershad-Vena
Channel-State Estimation Receiver

If the last bit was detected correctly, the state estimate of the channel is perfect. The effect of the channel (transient response) is translated into a non zero threshold setting that compensates for the transient response of the channel from the past bit. The present bit will then appear at the maximum likelihood decision box with the intersymbol interference removed. As long as the receiver makes correct decisions, the tails of the past bits do not affect the present decisions. However, when an error is made in the decision, the channel state estimate will be in error. This in turn causes an error in the setting of the threshold.

This receiver structure can be shown to be equivalent to the tapped delay line. Bershad and Vena designated the optimum linear filter to be a matched filter matched to the received signal. This is very difficult to physically realize. The conditional maximum likelihood estimate of the channel state is obtained by driving a replica of the channel impulse response with the detedted pulse train. This and the movable threshold setting corresponds to the function of the sign detectors and tap gains in the tapped delay line filter. The tap gains effectively change the threshold of the threshold detector. By using a threshold detector for the maximum likelihood decision box and an integrate-and-dump detector for the matched filter, the two receiver structures become equivalent.

Bershad and Vena approached the analysis of the error performance by studing the statistics of the dynamic behavi-

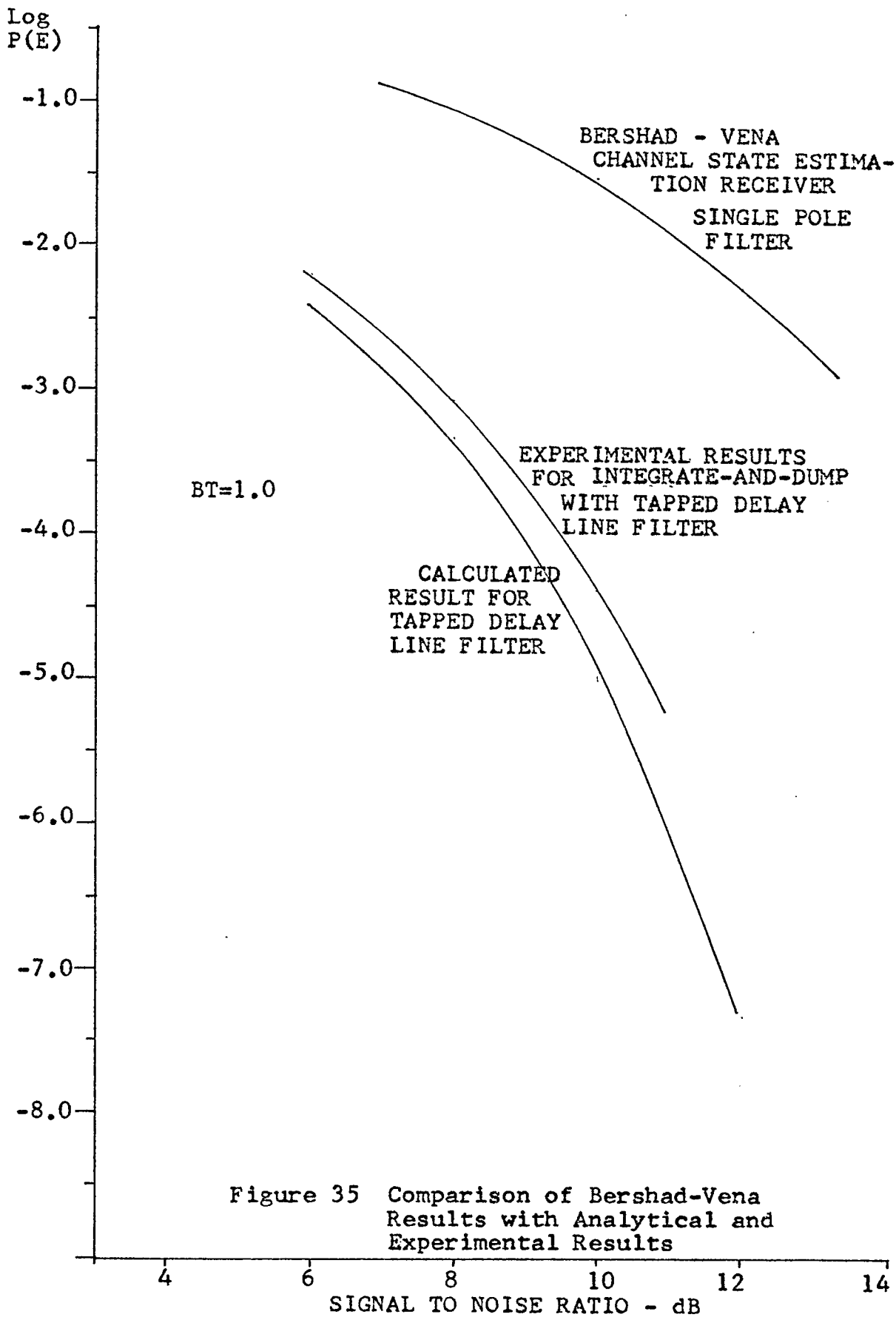


Figure 35 Comparison of Bershad-Vena Results with Analytical and Experimental Results

or of the threshold error. The threshold error was approximated using techniques used in the study of threshold learning systems. The receiver performance was then found as a function of the threshold setting error. The performance was analyzed for one- and two-pole channels.

Figure 35 shows the results of the channel-state estimation receiver with a one-pole filter at BT=1.0. The experimental and analytical results from this thesis is also shown. Since Bershad and Vena used a one-pole filter, a direct comparison cannot be made. There is a 6 dB difference in performance between the experimental results and Bershad and Vena's calculations.

5.3 Korn - Analysis for Causal Filters

Korn [8] analyzed intersymbol interference for causal filters with emphasis on Butterworth filters. A sampling detector and an integrate-and-dump detector were used as the receivers. Korn also analyzed the integrate-and-dump detector using feedback network to remove the intersymbol interference from the past bits. However, Korn does not elaborate on the structure of the feedback network. Only the correct detection of the past bits were considered when eliminating the intersymbol interference. Therefore, only a lower bound was given on the performance of the feedback system.

The probability of error was calculated by finding tight upper and lower bounds on the probability of error. It was assummed that the intersymbol interference was limited to finite number of bits. The nummber of interfering bits

was reached by making calculations of the probability of error bounds with increasing numbers of interfering bits considered until there was an insignificant change in the fourth significant figure of the bound.

The Butterworth filter has the transfer function

$$G_N\left|(j2\pi f)\right|^2 = \left[1 + (f/f_o)^{2N}\right]^{-1}$$

where f_o is the 3 dB cutoff frequency and N is the order of the filter. The filter used in the experiment had a -24 dB/octave attenuation slope at cutoff. This corresponds approximately to a Butterworth filter of order N=3. The graphs of the probability of error versus signal-to-noise ratio for Korn's calculations are shown in Fig. 36 and 37. Since Korn considered only causal filters and only an ideal filter was used for the calculations in this thesis, there will be a difference in the calculated values of J(BT,n) and σ^2. These differences will give different values of performance for the two systems.

Figure 36 shows the calculated performance from this thesis along with Korn's for BT=0.5 and 1.0. The results are very close to each other. At BT=0.5, there is less than 0.3 dB difference in the performance curves. For BT=1.0, the difference is less than 0.2 dB. Thus the assumption of using the ideal filter instea of a causal filter did not affect the calculations by a significant amount.

Figure 37 shows the experimental performance curves along with Korn's calculations. There is a considerable difference between the experimental results and Korn's results.

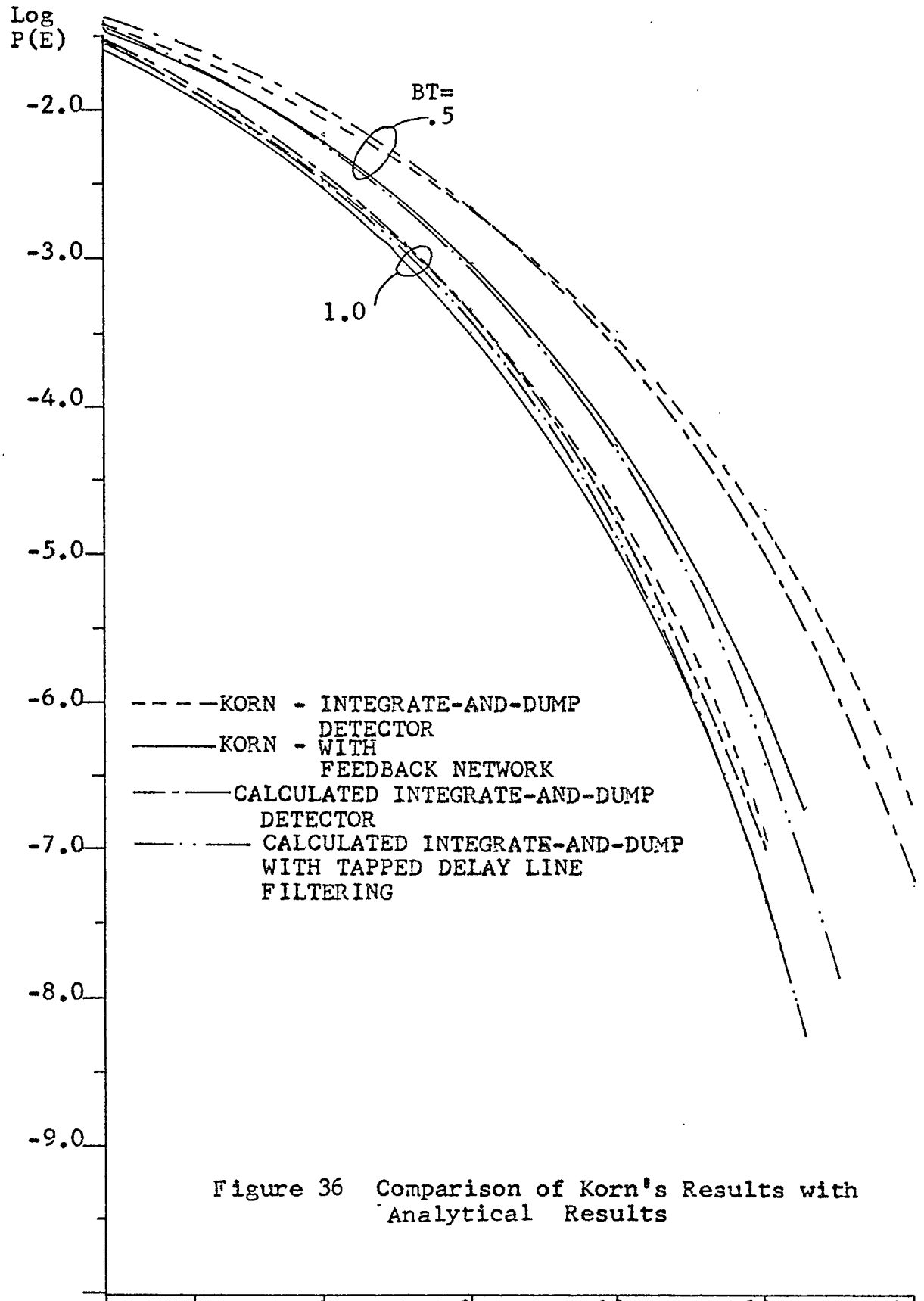


Figure 36 Comparison of Korn's Results with Analytical Results

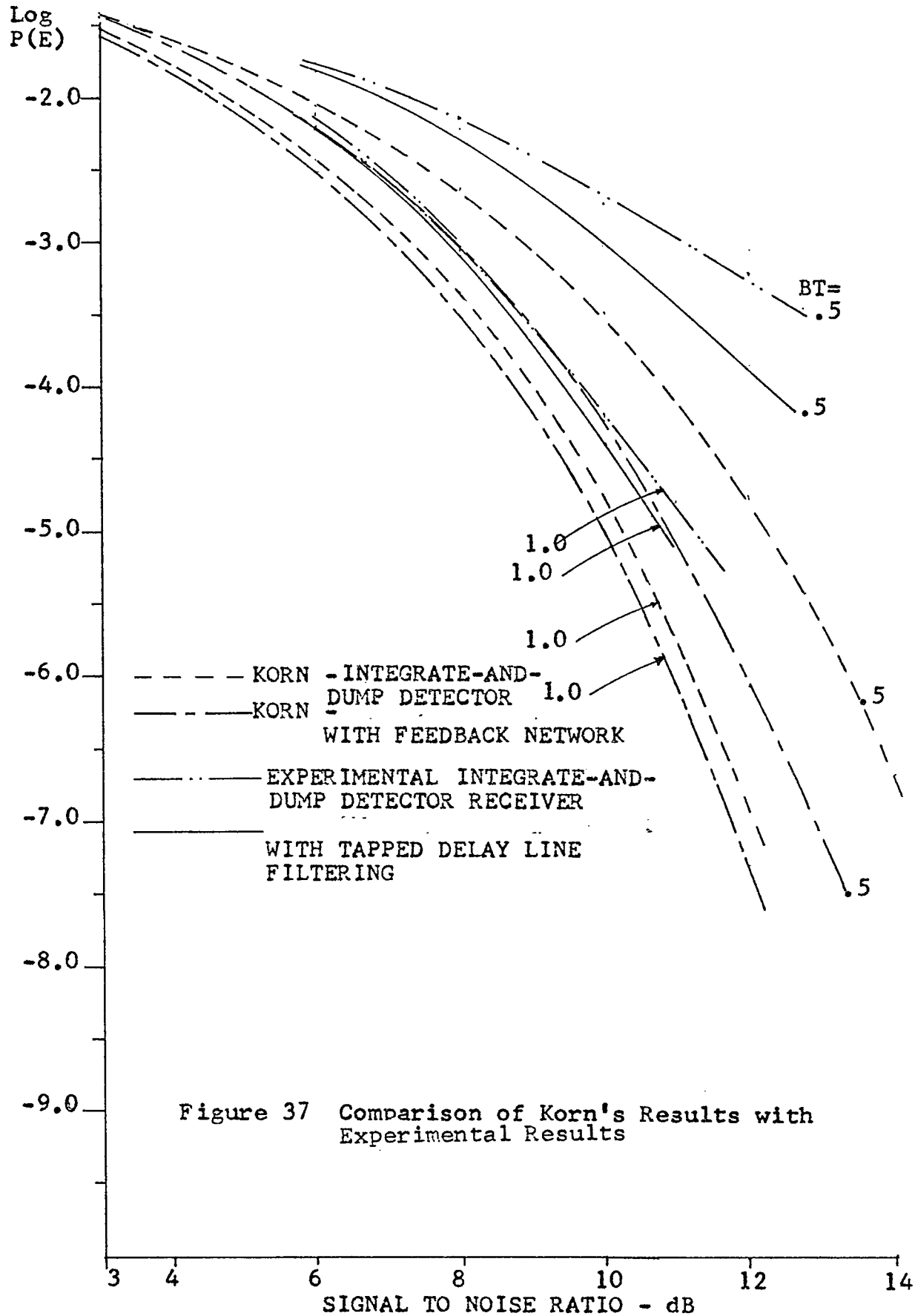


Figure 37 Comparison of Korn's Results with Experimental Results

This difference is the same as that compared with the calculations of this thesis.

5.4 Gonsalves - Maximum Likelihood Receiver

Gonsalves [9] suggested a maximum-likelihood receiver for eliminating intersymbol interference. The receiver structure is shown in Fig. 38. This is the simplest form of the maximum-likelihood receiver shown by Gonsalves. The receiver cnsists of a matched filter, a summer, a unit delay, a saturated amplifier, Z_R, a sampler, and a threshold detector. This receiver resembles the except that there is no decision feedback loop. The saturated amplifier is defined by

$$Z_R = \begin{cases} R & u>0 \\ -R & u<0 \end{cases}$$

where u is the output of the matched filter and R is defined as

$$R = \frac{4}{N_o} \int_0^T s_p(t)\, s_p(t+T)\, dt$$

where $s_p(t)$ is defined as in Chapter II. The sign of Z_R is determined by a threshold detection of the last bit. Thus the intersymbol interference is removed from the bit under detection if the the last bit was detected correctly.

Gonsalves assummed that intersymbol interference was limited to only one bit preceding the bit under detection. An upper bound on the probability of error was given for this receiver structure as

$$P\{\mathcal{E}\}(\text{upper}) = S^2\, Q(\sqrt{\rho}) + SP\left[Q(\sqrt{\rho}(1+2r) + Q(\sqrt{\rho}(1-2r)\right] + P^2\left[\tfrac{1}{2}\, Q(\sqrt{\rho}) + \tfrac{1}{4}\,\left(Q(\sqrt{\rho}(1+4r) + Q(\sqrt{\rho}(1-4r)\right)\right]$$

where

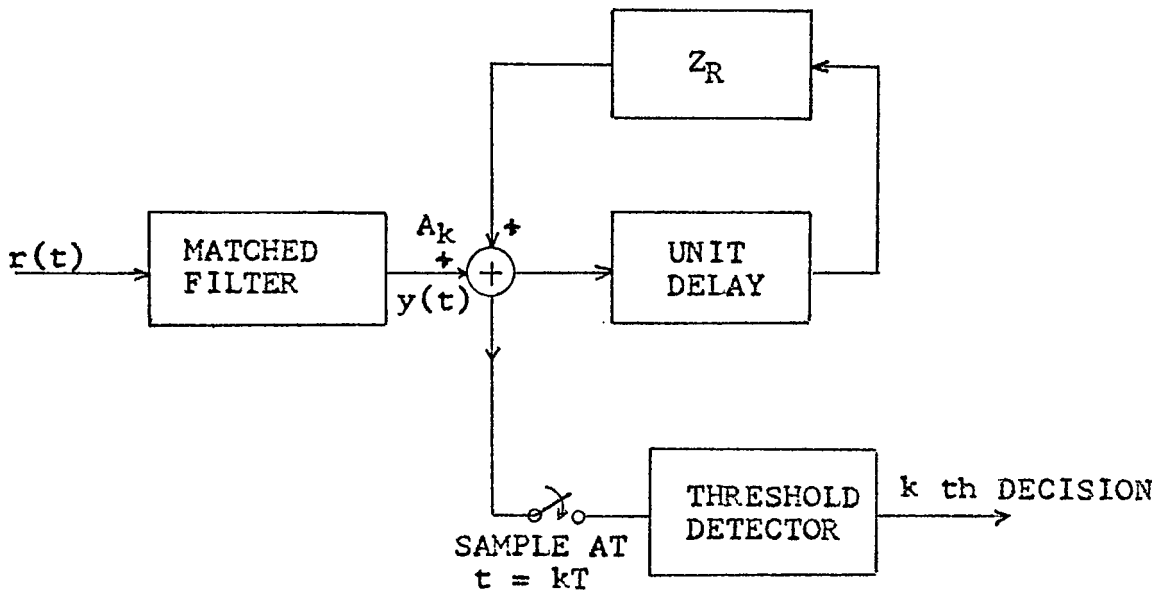


Figure 38 Structure of Gonsalves' Maximum-Likelihood Receiver

$$\rho = \frac{2}{N_o} \int_0^{2T} s_p^2(t)\, dt$$

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} \exp\left\{-\frac{t^2}{2}\right\} dt$$

$$P = \frac{Q(\sqrt{\rho/2})}{1 + Q(\sqrt{\rho/2}) - \frac{1}{2} Q(\sqrt{\rho/2}(1-4r) - \frac{1}{2} Q(\sqrt{\rho/2}(1+4r))}$$

$$S = 1-P$$

$$r = \frac{\int_0^{2T} s_p(t)\, s_p(t+T)\, dt}{\int_0^{2T} s_p^2(t)\, dt}$$

where P is the probability of error for a tail cancelation receiver.

Gonsalves defined $s_p(t)$ as the received pulse with width 2T. The matched filter was assummed to bo matched to the received pulse $s_p(t)$. This is not the same as tthe integrate-and-dump detector, which was matched to the transmitted pulse rather than the received pulse. A filter matched to the the received signal would give better performance. However, it is very difficult to physically realize a filter what would be matched to the received pulse.

Gonsalves' equations must be modified in order to make a comparison. Let s(t) be the transmitted pulse, then s(T-t) is the impulse response of the integrate-and-dump. Gonsalves' equations can be rewritten as

$$r = \frac{\int_0^{T} s_p(t)\, dt}{\int_T^{2T} s_p(t)\, dt}$$

$$= \frac{J(BT,1)}{J(BT,0)}$$

$$= \frac{2}{N_o} \int_0^{T} s_p(t)\, dt = \frac{2}{N_o} J(BT,0)$$

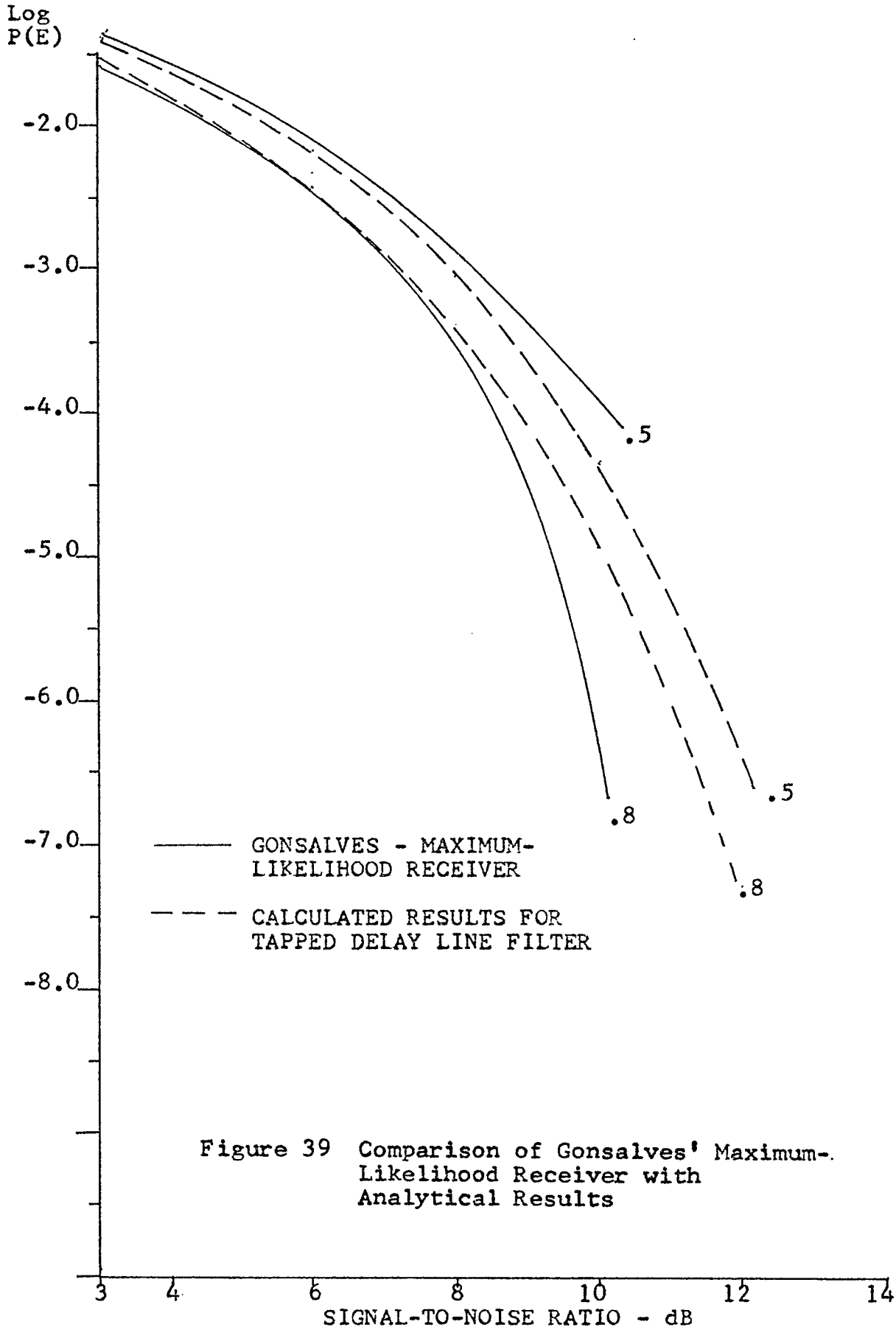


Figure 39 Comparison of Gonsalves' Maximum-Likelihood Receiver with Analytical Results

$$R = \frac{4}{N_o} J(BT,1)$$

Since A_k in Fig. 38 is given by

$$A_k = \frac{N_o}{4} \int_{kT}^{(k+1)T} r(t)\, s(t-kT)\, dt$$

the factor $4/N_o$ will be cancelled at the output of Z_R. Thus Z_R is equivalent to the tap gains in the tapped delay line filter.

The performance for Gonsalves' maximum-likelihood receiver using an integrate-and-dump detector was calculated using the modified equations. The results are shown in Fig. 39. For BT=0.5, Gonsalves' calculations does provide an upper bound. However, at BT=0.8, the upper bound fails.

5.5 Wang and Noack - Decision Directed Detector

Wang and Noack [10] suggested a decision-deirected detector for eliminating intersymbol interference. The receiver structure is shown in Fig. 40. Ignoring the part in the dashed line box, the decision-directed detector is identical to the one-tap tapped delay line except for the matched filter. K_2 is the contribution of the past bit's interference and is subtracted from the present bit being detected. Feedback is used in this receiver structure. Note that the unit delay used in the past bit detector can be a digital shift register but the unit delay in the future bit detector must be an analog delay line.

Wang and Noack assummed that intersymbol interference was limited to one bit preceding and one bit following the bit under detection. The received pulse was assummed to be

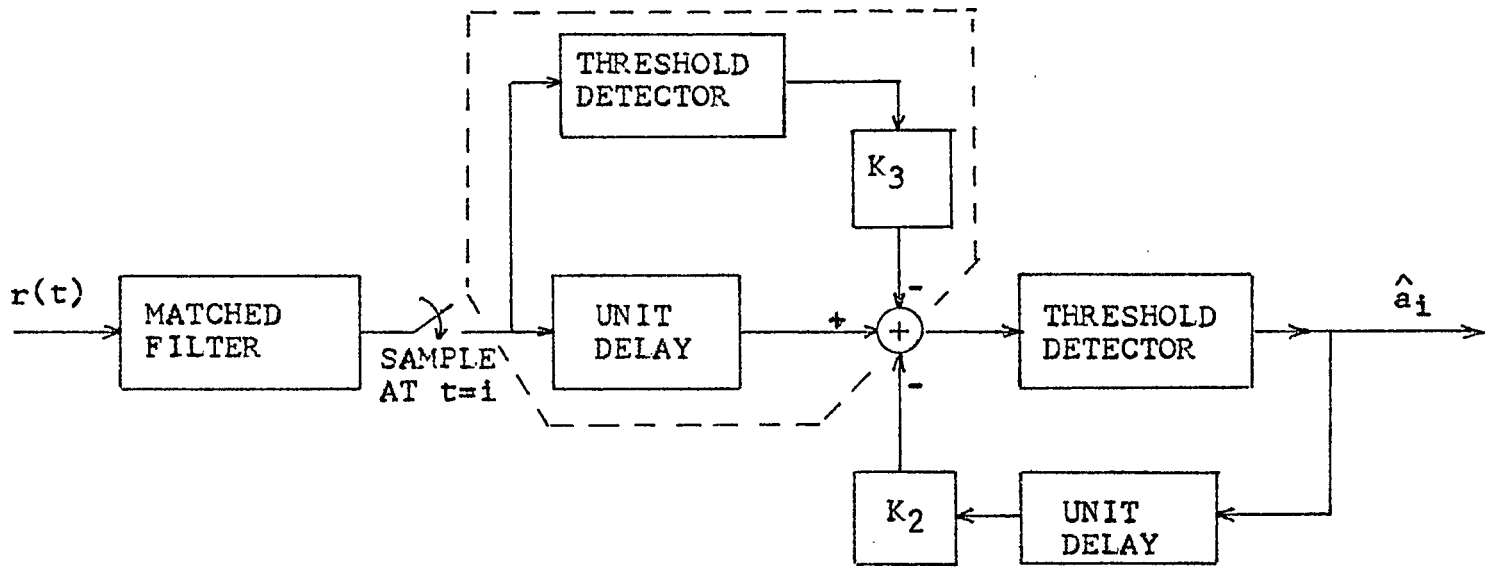


Figure 40 Structure of Wang-Noack Decision-Directed Detector

piecewise linear as shown in Fig. 41. $S_p(t)$ and $-S_p(t)$ are the received pulses. The matched filter was matched to the received pulses rather than to the transmitted pulses.

Wang and Noack used the averaging method in the analysis of the performance of the decision-directed detector. Substituting an integrate-and-dump detector for the matched filter, using an ideal filter channel, and ignoring the interference from future bits would only lead to the same analysis performed in this thesis. The matched filter specified by Wang and Noack would be difficult to physically realize. This is of little concern as the actual received pulse in a digital system does not resemble the piecewise linear model used by Wang and Noack.

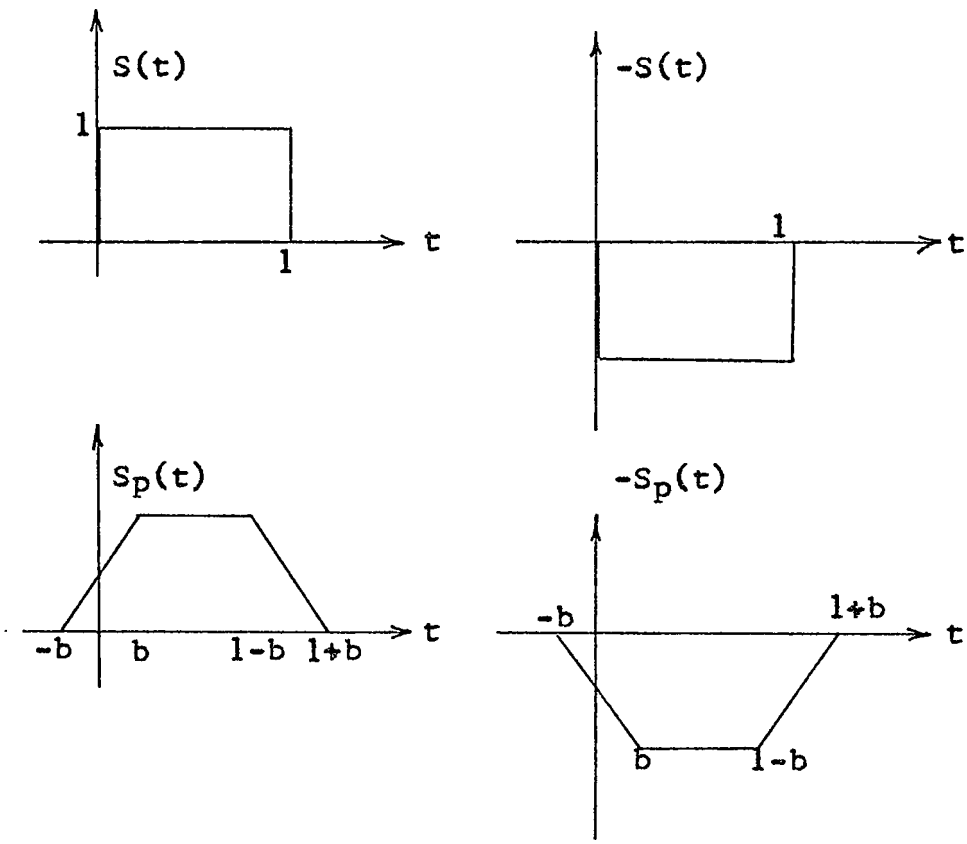


Figure 41 Pulse Shape Used by Wang-Noack

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APPENDIX I

COMPUTER PROGRAM FOR CALCULATING ERROR PERFORMANCE OF TWO-TAP TAPPED DELAY LINE

```
C     R'S CORRESPOND TO SNR OF 3,6,8,10,12,14,16,18 DB
C     U'S CORRESPOND TO MEANS OF SEQUENCES
C     T0=J(BT,0), T1=2*J(BT,1), T2=2*J(BT,2)
      IMPLICT REAL*8(A-H,O-Z)
      DIMENSION R(8),P(25),PE(25)
      R(1)=10.**.3
      R(2)=10.**.6
      R(3)=10.**.8
      R(4)=10.**1.0
      R(5)=10.**1.2
      R(6)=10.**1.4
      R(7)=10.**1.6
      R(8)=10.**1.8
      DO 30 L=1,10
      READ (5,1300) T0,T1,T2
1200  FORMAT (3F7.4)
      DO 20 K=1,8
      WRITE (6,1100) T0,T1,T2
1100  FORMAT (3(F7.4,5X))
      S=DSQRT(R(K)/T0)
      P(1)=1.0
      P(2)=1.0
      U1=T0
      U2=T0+T1
      U3=T0-T1
      U4=T0+T2
      U5=T0-T2
      U6=T0+T1+T2
      U7=T0-T1+T2
      U8=T0+T1-T2
      U9=T0-T1-T2
      DO 10 I=3,25
      P(I)=(1.0-P(I-1))*(1.-P(I-2))*DERFC(S*U1)*.5
     1 +P(I-1)*(1.-P(I-2)*.5*((DERFC(S*U2)+DERFC(S*U3))*.5
     2 +P(I-2)*(1.-P(I-1)*.5*((DERFC(S*U4)+DERFC(S*U5))*.5
     3 +P(I-1)*P(I-2)*.25*((DERFC(S*U6)+DERFC(S*U7)+
     4 +DERFC(S*U8)+DERFC(S*U9))
      PE(I)=DLOG10(P(I))
      WRITE (6,1000) I, P(I),PE(I)
1000  FORMAT (I3,5X,F16.12,5X,F10.5)
   10 CONTINUE
   20 CONTINUE
   30 CONTINUE
      CALL EXIT
      END
```