THE SIMULATION OF DEDICATED DEMAND COMPUTER SYSTEMS

A Thesis

Presented to

the Faculty of

the Department of Computer Science

The University of Houston

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

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by

Robert N. Wright

December 1979

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ABSTRACT

System performance analysis is an area of interest affecting most everyone associated with computer systems. However, it is an area which is often neglected by many analysts responsible for system development and maintenance.

Simulation is one of the most powerful and flexible tools available for system performance evaluation, which has seen limited use in the applications environment. Today a very important product class which is marketed by many small and large system houses and OEM firms are dedicated demand interactive systems. Simulation of these type systems would be a powerful development tool for these companies, and in addition provide them with a marketing and customer support bonus.

This thesis will present a structured approach to dedicated demand system simulation that will be flexible enough to 'grow' with a target system both in hardware and software configuration.

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1.0 INTRODUCTION

Modeling and simulation are, and have been, important tools in the computer industry for designers of hardware and software systems. However, systems users and applications analysts, being production rather than development oriented, often do not have the familiarity with the techniques necessary for the effective utilization of these valuable tools in the evaluation of their system's performance. Modeling and simulation are also becoming increasingly more important as system managers become aware of benefits which can be realized through modeling and simulation in the area of maximizing their investment in hardware and personnel through increased performance. It is in this area that a system's wasted potential can be explored and brought to light.

A neglected but perhaps just as important advantage derived from modeling and simulation is that it can be very useful and sometimes necessary in helping an applications analyst grasp a better understanding of the basic interactions of the system for which he is responsible(4,30). This understanding, in turn, will give him the insight required to more effectively judge the capacity of the system and its future potential for expansion.

Most dedicated demand systems are not developed by the end user. The user normally contracts with a systems or OEM company to develop the particular system capabilities he requires. Therefore, while simulation may be a valuable tool

for a user, it would probably not be practical to assume that he would have the resources available for simulator development if he did not have the resources necessary for system development. However, the systems and OEM companies most likely do have the necessary resources to develop the simulation tools necessary to aid in the development and optimization of their products. In addition, since many of these product systems have similar applications, a flexible simulator should be able to model the performance of a broad range of their system applications with only minor modifications.

Such a simulation capability could also offer these companies additional benefits. Simulation can be used as a marketing tool to provide a potential customer with performance data on a system configuration he may be considering for his application. It can also provide customers with continuing simulation support which they probably otherwise could not obtain.

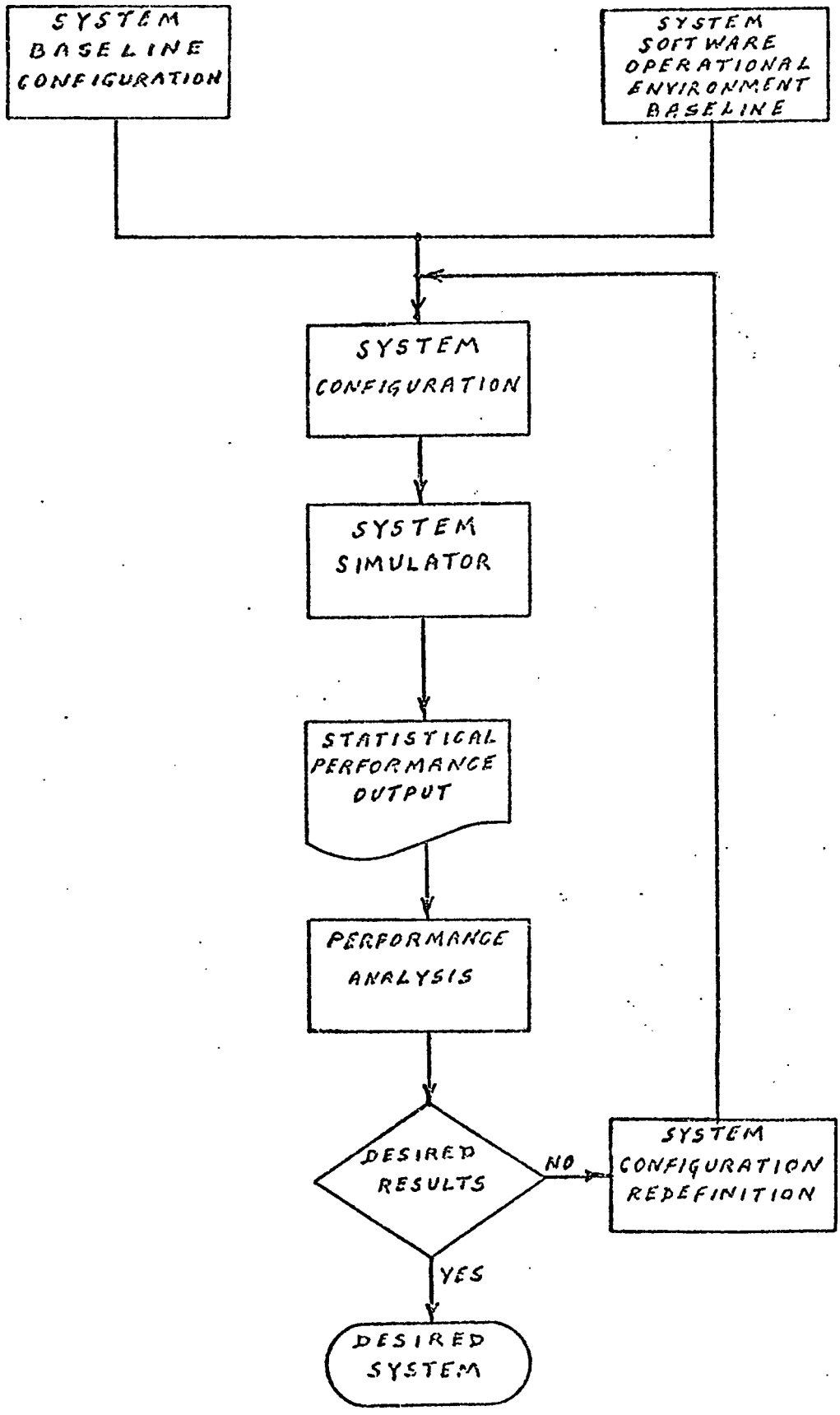
This thesis will present a technique for producing a flexible simulator for dedicated demand timesharing systems typically those utilizing a common data base. This simulator will be designed to 'grow' with the target system's hardware or software. Therefore, the initial investment in producing such a simulator can be amortized over the life of the target system since the simulator can then be maintained as an analysis and management tool.

An additional stumbling block to the use of system performance evaluation techniques is the conviction most system users have that today's hardware and software systems are too complex to be modeled by any simple technique. This thesis will further demonstrate that a relatively simple simulator can effectively evaluate the performance of a modern computer system.

In such a simulator, each system resource is represented by a modular simulation routine and each software application program or task is represented by a simulation function which can then closely depict the actual operational environment of the system. Through this function, the various possible simulation transactions are mapped into the required sequence of system services.

A requirement of this simulator is that all of the pertinent system variables which may be the source of increased system performance through their modification must be external to the main body of the simulator in order that they may be readily modified. The desired simulation analysis flow is shown in figure 1, and any simulator should be designed tc operate readily in such a manner.

The next section will further discuss simulation and why it has been chosen over analytical modeling for this application.



SIMULATION OPERATIONAL FLOW

FIGURE 1

2.0 MODELING AND SIMULATION

Modeling and simulation are the two most common methods of predicting computer system performance. The question of which performance evaluation method, modeling or simulation, is best suited for use by the typical applications analyst in the evaluation of the capabilities of a system configuration leads to the following observations.

Modeling, a mathematical presentation of a system, has the advantage in system evaluation of conceptual simplicity and flexibility. However, these attributes tend to break down when a model is viewed outside a controlled microcosm. The disadvantage of analytical modeling is that the mechanism and results of the model are often incomprehensible to those for which they are designed, and models often rely on oversimplified assumptions that may not accurately reflect the complexities of the target system. In contrast, simulation has the advantage of being comprehensible to a wider variety of uses and allowing realistic detail in a wider variety of applications. However, on the negative side, simulation has the disadvantages of being time consuming and subject to random programming errors (8,29).

There are many similarities between analytical modeling and simulation both in terms of the steps one has to go through to derive the required results and in the possible sources of errors in the techniques.

While an analytical model must be formulated, and the required equations depicting the system's interactions derived, a simulator must be written to depict a system. An analytical model must be solved for a given configuration (when a solution is possible) and a simulator must be run and the results analyzed. Both the results of an analytical model and a simulator must be verified, and no proven 100% accurated procedures for model validation are available. Verification can sometimes be the most difficult step especially if the target system is in the conceptual stage and doesn't actually exist.

Simulation and analytical modeling also share many analogous pitfalls. While simulation models are subject to programming errors, analytical models are subject to errors in the mathematical manipulation of the parameters. Therefore simple programming errors in simulation are paralleled by the possibility of perhaps dropping a sign in an analytical modeling equation. Poor selection or specification of system parameters will have an equally detrimental effect on analytical and simulation modeling, as will the poor specification of work-load characteristics.

2.1 DETERMINISTIC MODELS

Analytical models are usually classified as being either deterministic or probablistic models. Deterministic models are relatively simple models which are limited in their utility by their inability to model systems which cannot be characterized by a set of deterministic parameters.

One type of deterministic model is the mean-value model. In this type model all of the random system variables are replaced with their mean-values as are other factors such as job arrival rates. It should be noted that this is not the same as selecting an average of observed values of a parameter which is known to have a fixed value. Since this type model by definition, depicts the average case, worst case system conflicts are ignored and the results of such a model can be optimistic and misleading.

2.2 PROBABLISTIC MODELS

As mentioned previously, probablistic models are much more capable of depicting real system interactions than are deterministic models. One such model which is sometimes used is the Markov model. A Markov chain is a stochastic process consisting of states in which the probability of transition from one state to the next at time t_i depends only on the state the process was in at time t_{i-1}. Therefore, a system can be depicted as a system of state-to-state transitions, considering only the current state and the available next states.

2.3 QUEUING MODELS

Perhaps the most frequently used analytical model for the evaluation of computer system performance is the queuing model. In this model system resources are depicted as servers and a model is derived with users requesting an activity by a server and if the server is busy a wait queue will be formed which is occupied by the user's awaiting service. Queuing theory has had many applications outside computer system performance since the basic work was done in 1909 by Erlang. It has been used extensively in industrial engineering applications and the concepts have been applied with some success to computer system performance evaluation.

It is fairly easy to see how a queuing model of a check-out line at a store can be analogous to a computer disk access just as customers would wait in line for the cashier. With a known mean arrival rate and a known mean service time one can calculate the average number of users awaiting service. However the disk subsystem model in real life is not so simple, and the input to one queue is not an independent entity but part of a larger and more complex system. The input to a queue may not be at a known rate but rather it may be fed by the output of several other queuing systems.

2.4 BENCHMARKS

Benchmarks are a simulation technique which are commonly used in the comparative studies of computer systems. A benchmark involves running a workload simulation program on one or more systems or configurations and comparing the results. This technique is often useful in computer selection studies, but the results are often misleading or incomplete since the benchmark programs often give only simple results such as response time and job throughput rate. There are usually no internal system statistics available for analysis; therefore, it is difficult to determine why a system configuration performs at an observed level, since there is no data available on the internal performance of the target system. This makes decisions as to how to best improve the performance of a system configuration very difficult since no data is available on the performance of the components of the system configuartion under study.

Benchmarks may not be the best technique for the evaluation of system performance, but they are very valuable in the evaluation of the performance of system resources. Because of this, benchmarks are a valuable source of performance parameters which may be used for system simulation.

2.5 SIMULATION

Simulation modeling is simply the creation of a simulation program model of a target system which when provided with the workload characteristics of the target system will provide the user with statistical data which represents how the target system would respond were it to process the same workload. If it is so simple why not just run the workload on the target system?

Simulation is used for much the same reasons as are analytical models. Often the target system does not yet exist and data is required to validate design decisions. If the target system does exist, it may not have the same configuration as the one which is to be simulated. Even if the exact configuration does exist those charged with the task of analyzing the system may not have sufficient access to the system.

In addition to the above mentioned availability problems, most systems do not have the ability to collect data on internal performance indices. Therefore, as in benchmark simulation there is difficulty in obtaining data on the cause of an observed level of system performance.

Simulation is therefore often a readily available modeling technique which is used to evaluate system configurations. For example, INTEL used simulation techniques to

analyze various conceptual internal hardware configurations of the 16-bit 8086 microprocessor. From the simulation data various decisions were made such as the determination of the length of the CPU instruction processing pipeline. This is typical of an application of conceptual design simulation.

2.6 MODELING OR SIMULATION?

The choice of simulation or analytical modeling ultimately will be a user's choice. However, analytical and simulation modeling each have their place and each are better suited for certain applications.

Analytical modeling is a powerful tool for the study of smaller system problems, such as a disk queuing discipline. In this type of application, analytical models are generally superior to simulation techniques, since an analytical model can provide formulas which give the relationships between the subsystem workload demands, resources, and scheduling algorithm. In addition, the methodology of the performance measurement will be backed by mathematical proof. However, most real world system problems are not so simple, and while analytical models can provide performance measurements for some system configurations, most real world system problems and many performance measurements normally desired cannot be formulated using existing analytical methods (14).

When a complex system problem cannot readily be solved by analytical methods, often simplifying assumptions must be

made in order to obtain a solvable model. Decomposition is a technique which can be used to subdivide a more complex system problem into smaller subsystems which can be simplified and formulated into analytical models. These simplifications naturally will affect a model's accuracy and applicability to a performance analysis problem.

While some analytical models have exact solutions, in simulation some error always exists since the simulator is not an exact reproduction of the target system. Nevertheless simulators are well suited to real world system analysis problems and the inaccuracies which normally arise form a selected level of simulation detail and time resolution are usually considered acceptable. So while analytical models can only be applied to a relatively limited number of real world system performance problems, benchmarks and simulation techniques are most frequently used for the more involved real world system modeling tasks.

2.7 WORKLOAD SIMULATION

There are many techniques for representing a model of the target system's workload to the system simulator or model. One of the most basic is a distribution driven workload simulator. This technique can utilize sampled data on resource utilization from a target system to determine a stochastic sequence of simulation states.

A distribution driven workload simulation often provides for a very compact representation of the workload. However, it is impossible to accuractely depict any but the simplest of workloads with this technique.

Another method of workload characterization is one in which the workload is divided into identifiable tasks and each task is separately characterized. This technique is very popular and commonly used. A task can be characterized to any degree of detail that the user finds necessary to provide for the level of accuracy and flexibility required by his application.

Workload data on the target system can be compiled in various ways. Workload on a system can be characterized by information collected in operating system accounting logs; this technique is simple but usually does not provide the model with a detailed enough characterization of the system workload. Another technique which can provide detailed information on the system is trace-driven modeling. This technique collects trace data with a system probe and these data are later analyzed and translated into a workload model. This technique can provide the system with very detailed data on the workload; however, there are problems in that often the trace probe is not a standard component of the target system, and therefore the probe interferes with the system to some extent. This interference generally will become more pronounced as the detail of the trace probe is

increased. Another problem which must be considered in any workload model is that the workload model must be compatible with the system model. Therefore, any collection of trace data must be reduced and transformed into a format acceptable to the system model, and generally a system probe of sufficient detail will collect a large amount of data. The interpretation and reduction of these data are non-trivial tasks (29).

In systems where the character of the workload is known and does not vary appreciably from measurement interval to measurement interval, another technique is to characterize workload as sequences of system resource demands. Each sequence represents a known task in the target system and is in effect a psuedo-program which drives the simulator. Today, there are many system applications for which this technique is well suited since many medium and small computer systems are functionally dedicated. Therefore, it is known that the system workload will not change in character significantly from one observed interval to the next. That is not to say that the system may not be busier at certain times, but that the tasks the system will be performing will remain essentially unchanged.

3.0 ESSENTIAL ELEMENTS OF SIMULATION

For many years systems managers have had no better means for evaluating a prospective system than the application of Grosch's Law, which maintains that manufacturers price their equipment so as to make performance proportional to the square of the cost - $P = kC^2$. Therefore, if one wanted a system with four times the throughput, one would expect to pay twice as much for it (21). As crude and generalized as this 'law' appears, it has until recently proven a fairly accurate measure on the industry's pricing practices.

Today, tools are available which remove to a great extent the users dependency on the manufacturer for sole source information on system requirements and performance. The following are the elements which need to be considered and included in a simulator if it is to be constructed at a minimal cost, grow with the target system and maintain a close correlation with the target system's performance and capabilities.

3.1 EVALUATION CRITERIA

The first consideration in system performance evaluation is selecting the system characteristics which are to be used as the measure of improved system performance. Many different measures are available--throughput, resource utilization, and response time to mention only a few, but for the interactive processing application, response time is

usually considered the major performance goal.

Response time is selected as the performance goal in demand systems such as:

a) point-of-sale terminal systems

b) reservation services

c) banking services

d) inventory control

In these types of systems productivity can almost always be improved by the reduction in the amount of time the terminal user has to spend waiting for the system to respond to an input from the terminal. Therefore, for this application, a system which can process 750 tasks with a response time of 500 milliseconds would be preferred to a system which could process 1000 tasks with a 2500 millisecond response time. While the second system is capable of processing more tasks, it does so at the expense of user wait time, and therefore it is not responding to the requirements of the operational environment.

3.2 SYSTEM VARIABLES

Another factor in the building of a model or a simulator is the selection of the important system variables which are to be used to depict the structure of the system, and which further will be used to modify the system configuration to study alternatives of system design.

Typical examples of these system variables are:

a) The size of main storage.

b) The number and type of peripheral storage devices.

c) The peripheral storage access times and data transfer rates.

d) The direct memory access (DMA) channels and configurations.

e) The assignment of task priorities.

3.3 SYSTEM STRUCTURES

A computer hardware system is modular by design, being a collection of system components such as the central processor, the memory system, peripheral storage devices, and input/output communications devices. These system components interact with each other in a known manner decided by the basic system architecture to provide the system services necessary to accomplish the tasks required of the system. Therefore, if a simulator is to be built, it will be easier for the user to understand, use, and modify if it is designed in a modular manner also. The modules of the simulator can then carry a close one-to-one relationship with the target system components and if one wishes to change the specifications of the target system's disc drive, then likewise one need only to go to the routines in the simulator which emulates the operations of the systems disc drives and change the parameters which define these specifications for the simulator.

3.4 REALISTIC DETAIL

An important consideration in system simulation is the decision concerning how much detail is to be designed into the model. The typical solution to this question is "the more detail the better"; the justification being that a computer executes instructions in the microsecond range. Therefore, the simulator should also operate in this range (26). However, it is a well known fact that normally the events which take place in the millisecond range are those which place the bound on system performance. Therefore, excessive detail, as advocated by Nielsen (33), will serve no other purpose in a small system simulator than to instill in the user a false sense of simulation accuracy. For example, in an imaginary system, a routine to establish a request in the I/O queue could optimally be 25 instructions long, but through inefficient programming the software is written in 50 instructions. The average instruction execution time for this system is 5 microseconds; therefore, the routine which should take 125 microseconds, actually takes 250 microseconds and is 50% inefficient wasting 125 microseconds. To process this I/O request, optimally it would take 4 disk accesses, however, through inefficient data structures and programming it will take 5 disk accesses. The average time required for each access/read is 23 milliseconds, therefore, the procedure should take 92 milliseconds, but actually takes 105 milliseconds and is 20% inefficient, wasting 23 milliseconds. This example

demonstrates that while 50% programming inefficiency could waste 125 microseconds, poor utilization of the peripherial storage, while only 20% inefficient, would waste 23 milliseconds or 184 times as much system time. While it must be noted that this example deals with different system resources, either resource when wasted will result in degraded system performance.

3.5 LANGUAGE SELECTION

There are innumerable considerations which can influence the choice of a simulation language for the simulation of a demand interactive system. The selection of a special purpose simulation language will carry with it benefits which should well outweigh the problems of availability and longer run times.

The arguements for the use of a special purpose simulation language rather than FORTRAN or ALGOL are similar to the arguements given by Denning for the use of a higher level language rather than assembly language for system programming (8). That is, a simulation language will be more understandable to other programmers, involves less programming time, and most important, has extensive measurement and statistical gathering capabilities included which are available with little or no additional programming.

3.6 OPERATIONAL ENVIRONMENT

One of the major problems encountered in all types of simulation is providing the simulator with valid representation of the actual required work the system will be processing.

Many simulators have been constructed for many purposes, and the techniques are varied but basically similar in their objectives. The problem all of these techniques have in common is providing the simulator with an accurate representation of the target system's operating environment. In other words, the workload presented to the simulator must accurately reflect the expected workload of the system being simulated.

The most common method of providing a simulator with input is by means of a random work generator. This generator will produce work for the simulator according to some predetermined distribution of the types of system services which will be required. This method has one obvious drawback, which is that known high-demand jobs which are regularly required of a system will tend to be averaged out by the statistical distribution. Another problem encountered is that the validity of the simulator is difficult to establish since the input to the simulator bears no close correlation to the actual work requirements which will be or are being made of the system.

A technique which solves most of the problems of a random work generator is trace-driven simulation (40). With this technique, a trace-driver is derived from a probe placed in the system to be simulated which then gathers data from the operational system on workload and at the same time gathers data on system performance and resource utilization. These data in turn must be interpreted and reduced into a usable form for input into the simulator. Therefore, the input into the simulator is derived from the actual workload of the target system, and at the same time data on the system's performance have been gathered which in turn can be used to validate the performance of the simulator. As mentioned earlier, this technique provides an answer to many of the problems inherent in a random work generator; however, trace-driven simulation has two primary drawbacks which tend to limit its applicability. The first and most obvious drawback is that the target system must exist, and must be operating with a predictable degree of reliability in order to gather the trace data. Secondly, the volume of trace data collected can be a non-trivial consideration when it comes to reducing it into a useable form and interpreting its applicability to the simulation (29). The degree of difficulty naturally depends on the system since some systems have extensive hardware or software data gathering facilities which can greatly reduce the size of the data collection task (36). Nevertheless, whatever data gathering technique

is used, the amount of time involved in the interpretation and analysis of the data will greatly increase the cost of the simulator and require skills which may not be readily available.

This thesis will approach the problem of providing the simulator with a valid operating environment by providing a very flexible task generator which can accurately depict a typical task as a string of system services that the target system normally would be required to provide. This task generator must have a high correlation to the actual environment and therefore, a prior knowledge of the system's existing or proposed operating requirements must exist.

4.0 DEMAND INTERACTIVE SYSTEMS

The wide-spread application of demand real-time processing today makes the field of system evaluation an even more important area of research. Today one can purchase a powerful 'mini'-computer with all the peripherials necessary for real-time demand processing for a fraction of what it would have cost seven years ago. Because of this drastic reduction in hardware costs, more and more users are using demand interactive systems for their various processing requirements.

Typical examples of today's spreading demand processing applications are:

a). airline reservations and ticket services

b). shipping and transportation control

c). billing and accounting services

d). inventory control

e). banking services

f). process control systems

g). point-of-sale terminal systems

h). word processing systems

The above mentioned systems are characteristically utilized by a number of users working on a common data base toward related goals.

Users of these systems will naturally be primarily concerned in the applications areas and they will not have

the familiarity with the performance evaluation tools, which they might require to effectively 'tune' their systems for optimum performance. They would probably also lack the means whereby they might evaluate various modifications or extensions to their systems and the effect these changes might have on their overall system performance. This lack of insight into a system's capabilities, along with vendor encouragement, often lead users to the assumption that any system expansion will necessarily require a capital investment in new hardware.

A means is therefore needed whereby the user of a system can evaluate its strengths and weaknesses and through this evaluation of the system's capabilities gain the knowledge necessary to efficiently increase the system capability to meet any expanded system requirements.

Dedicated demand systems as defined here, lend themselves to simulation techniques which should result in a close correlation of the simulation data to actual system performance. These systems, since they are dedicated to a function, can be given a depictive simulation workload without being concerned with the random occurance of unusual job types or mixes. In addition since these systems are normally not heavily involved in computation,the simulator will be less sensitive to the type of computer used, and the emphasis can be placed on the system interactions and

the functioning of the system peripherals, which will normally be the limiting factor in the systems performance.

5.0 SYSTEM EVALUATION

The area of system configuration evaluation always involves trade-offs. The problem generally is obtaining sufficient valid data to allow an analyst to make an effective cost-performance trade-off analysis.

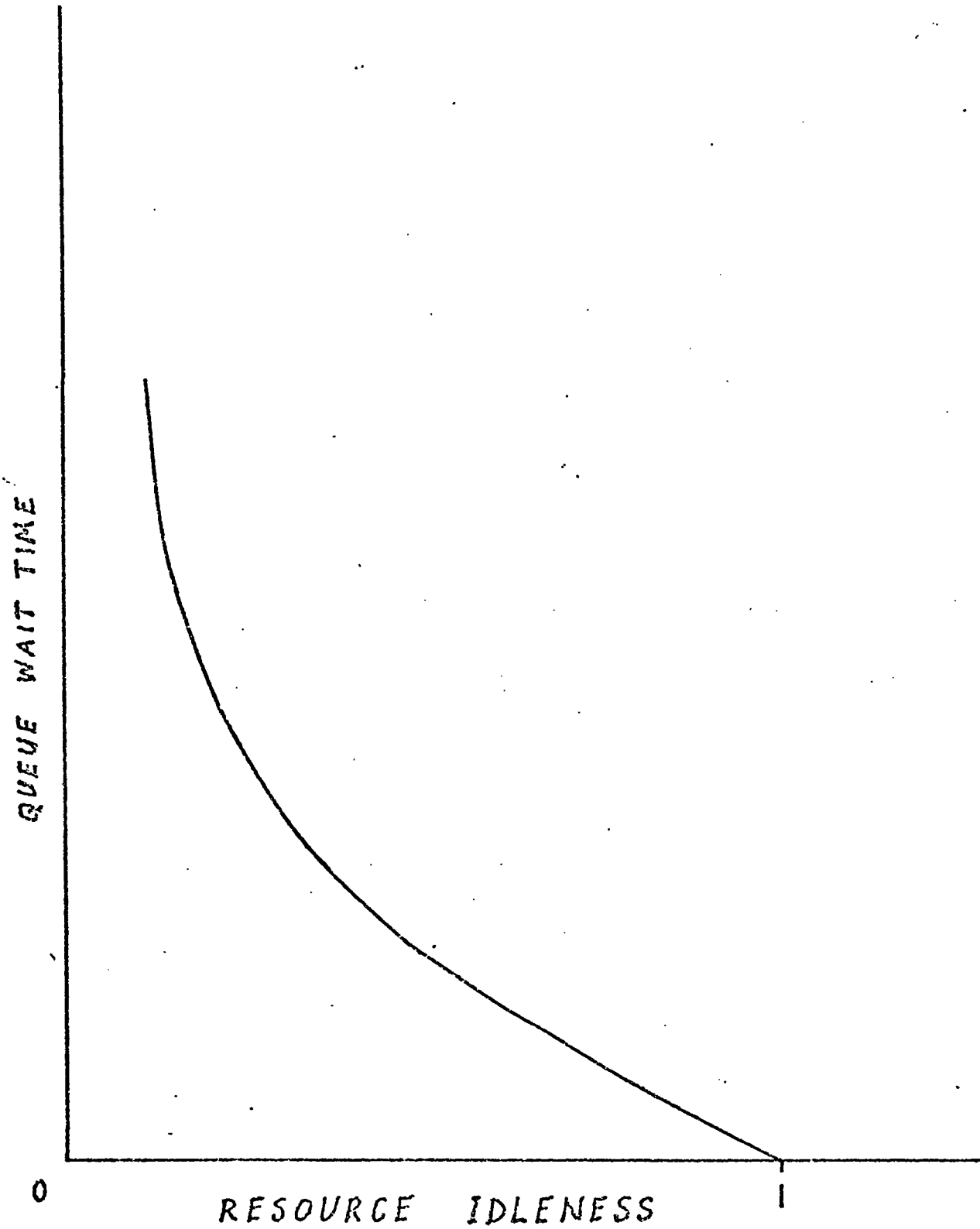
A typical systems analysis problem is in the area of mass storage performance evaluation. For example, a moving-head disk can be considered slow as compared to a head-per-track disk/drum using a "shortest-access-time-first" hardware queuing mechanism (1), which is nearly optimal with respect to service wait-time minimization. The problem can then be taken a step further, for if a "shortest-access-time-first" drum can be justified through static performance specifications, then one must conclude that core or semiconductor mass storage can be justified on the same basis. So the questions that must be answered are--has the need for additional speed been demonstrated and can the additional expense be justified? Even if the cost can be justified, will the expected performance differential be realized in a dynamic operational system environment if no input/output channel queuing problem or congestion has previously been observed? Simulation is therefore a necessary tool which can be effective in gathering the required data for effective decision-making.

5.1 DEDICATED DEMAND SYSTEM EVALUATION

The usual goals of systems design are especially conflicting in the dedicated demand processing situation. Balancing system efficiency against user satisfaction, which in this case is normally expressed as fast system response, will usually require some compromise. That is not to say that these are not the goals of other types of systems; however, in the dedicated demand system if there is a conflict between resource utilization and system response, a decision is normally made in favor of response, while in many other system applications, one would normally consider resource utilization and system effeciency paramount.

This precarious balance between system response and system utilization is expressed in queuing theory as: the more likely it is that a facility or resource queue is non-empty (and therefore, the facility or resource is not idle), the more likely it is that the queue wait time is long (and therefore, a user must wait longer for service). If X is the idleness of a facility or resource, the expected wait time in queue is proportional to (1-X)/X. In other words, this means that if a queue exists for a facility's service, there is a high probability that the queue wait time will be long--see figure 2 (8).

In simple terms, this means that the more likely it is a resource is utilized, the more likely it is that a long



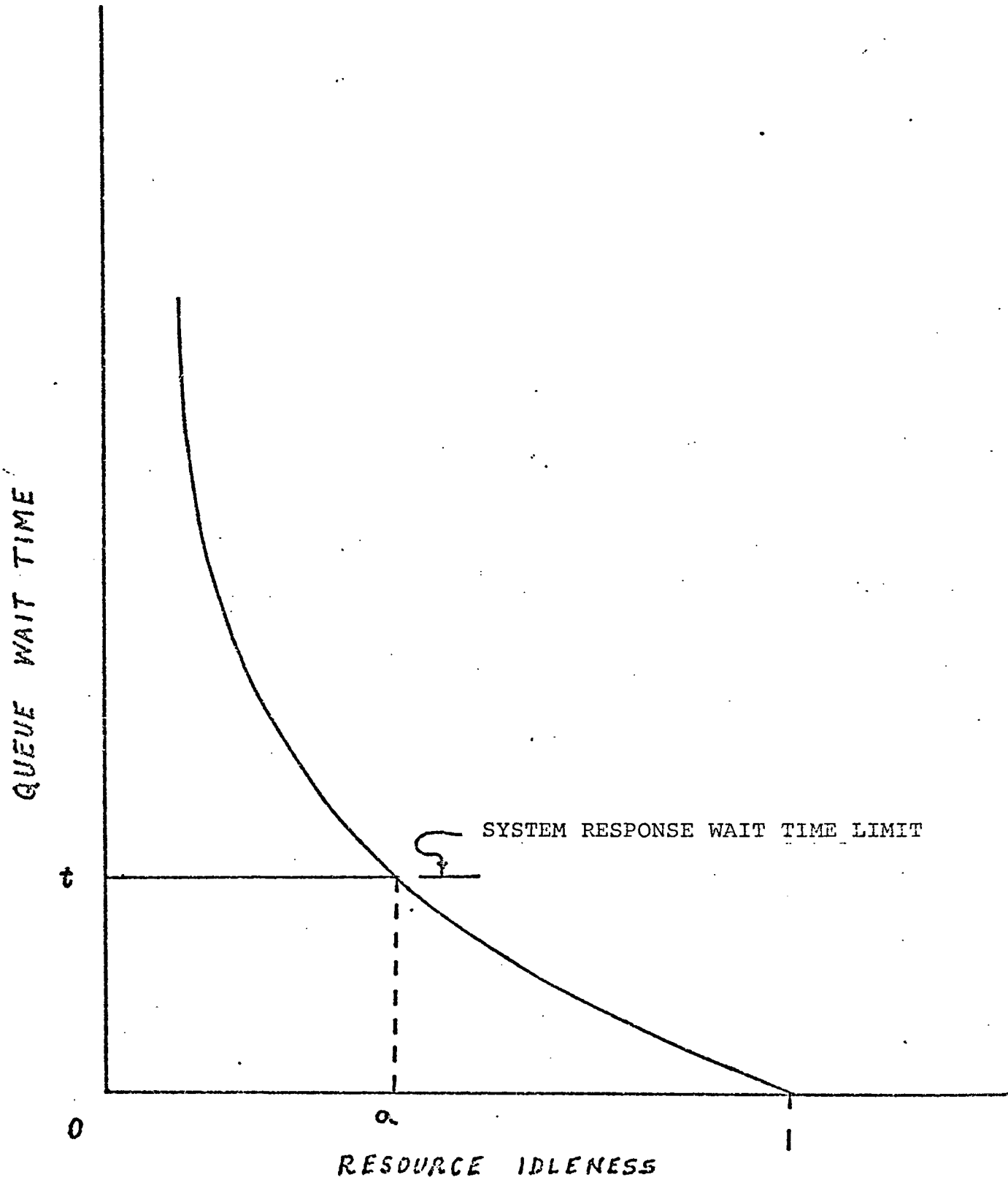
QUEUE WAIT TIME vs. RESOURCE UTILIZATION

FIGURE 2

queue will exist for that utility's service. As a common example, from experience it can be seen in most any large grocery store, that there are either idle checkers or there are long lines at each available register. It is unusual to see each available register occupied by only one customer. Therefore, in order to provide a "customer" with prompt service, a resource must be prepared to accept a certain amount of idle time.

The typical dedicated demand interactive system with multiple input terminals will usually have more than one task, or process, resident in the system at any one time. However, since only one can be occupying the central processor, all other tasks will either be idle, queued for system services or perhaps occupying an input/output channel. The evaluation of these times spent in queues, or system wait times, is always an area of prime interest in system evaluation.

The basic assumption underlying demand system evaluation and 'tuning' is that the minimization of system wait times and thereby the minimization of the system response time will be the areas of prime concern. Unfortunately, as previously mentioned, placing a constraint on 'wait time' will result in a loss of system efficiency. This loss is shown graphically in Figure 3 and equals 'a'. While processing efficiency is certainly important for system efficiency, the results gained are rarely of the necessary magnitude to significantly



QUEUE WAIT TIME vs. RESOURCE UTILIZATION - TRADEOFF

FIGURE 3

increase system performance. Nevertheless, one area related to processing efficiency which should be considered in system evaluation is the priority levels assigned to different types of transactions in the system; this can have a decided effect on performance, especially if some of the transactions in the system are lengthly.

The previously mentioned characteristics of dedicated demand interactive systems are very similar to the functional requirements of an operating system; therefore, many of the solutions to operating system problems are applicable on a smaller scale in dedicated demand interactive systems.

5.2 SIMULATION LANGUAGE SELECTION

There are many simulation languages to chose from in order to construct a system simulator; however, the three languages that are probably most commonly used in discrete system simulation are GPSS, SIMSCRIPT, and FORTRAN. FORTRAN, while not a special purpose simulation language, is often used either because the user feels more comfortable with a language they know, or because they feel their simulator is 'too complex' to adequately be portrayed by a general purpose simulation language (33). GPSS is a language that is most often used for small to medium scale simulation models, while for larger simulation models and those which may require a higher level of computational complexity than GPSS can effectively provide, SIMSCRIPT is usually found to be more effective.

The simulation language selected for this simulator is GPSS, General Purpose Simulation system, or more specifically GPSS/360 (24,25); this language is a transaction oriented simulation language which has found widespread applications due to GPSS's availability in many IBM and Univac installations (30).

GPSS was selected as the simulation language for several reasons; the main ones being the language's availability and that it is probably the best known simulation language, with broad simulation capabilities. Another important point is that the language has a comprehensive statistical package which can provide the user with statistical data on any area of the simulator under investigation. GPSS was designed with the non-programmer in mind, and because of this a simulator written in GPSS is usually comprehensible and easily learned by a wider range of potential users. It is hoped that this factor will give the potential users of this type of simulator clearer insight into its operation and thereby the operation of the simulator's target system. This insight should prove valuable, if not mandatory, if various modifications are to be made to a simulator to implement functional system differences, or perhaps to implement a different statistical gathering technique.

5.3 A DEDICATED DEMAND SYSTEM SIMULATOR

The simulator to be used must be designed to study the

interaction between the many system variables under typical operational conditions. The goal of this simulator is to aid in the evaluation of the various possible system configurations in order to derive the most effective configuration with a minimal loss in system efficiency. The areas of primary interest will be terminal wait for input time and system response time once input is accepted.

Items such as CPU utilization will necessarily be of secondary importance, as mentioned previously. For this simulator, the maximization of system potential, measured as response time, should be accomplished without any major system design modifications. The goal actually will be to 'tune' the system to extend its designed performance rather than to redesign another 'better' system. This is a situation one is often faced with when expected to do the best with what one has rather than purchasing new equipment.

Some of the primary system performance parameters which will be considered in the system evaluation are:

a). Terminal input wait time

b). System response time

c). Queues for system services

d). System resource utilization

These parameters were chosen because, as mentioned previously, the prime areas of system bottlenecks are waits for system resources. These bottlenecks are displayed as long system queues and excessive wait times for a system

resource. System resources with long wait queues will usually have a relatively high utilization and be suspect of having a detrimental effect on overall system response.

Typical system design variables to be included in a system simulator are:

a). Peripherial storage access times

b). Peripherial storage data transfer rates

c). System services scheduling and priorities

d). Input/output DMA channel utilization

e). Processor task capacity

f). Buffer quantities

g). Operational environment and workload

The simulator designed will have to be flexible enough to depict various system configurations in order to make valid comparisons of system performances and trade-offs. However, it must be realized that flexibility should only be carried so far, at some point the simulator will become so complex that only the designer of the simulator would be able to use it effectively. Therefore, a simulator should not be designed to cover all possible configurations of a system's hardware no matter how impractical they may be. Rather, the simulator should be designed to cover only the practical alternatives in the design of the target system, utilizing the simplified system components and interactions which will have to be considered in the dedicated demand system simulator.

Therefore this simulator will be used to examine the target system's performance without changing the basic system components, but only how they are utilized. Nevertheless, to accomodate possible future requirements of such a simulator, it must be capable of being easily changed to reflect actual or proposed modifications to the components of the simulator's target system.

In the evaluation of the simulation results, many facets of the system must be considered along with the performance figures. Since the goal is the maximization of design potential and not the redesign of the system, careful consideration must be made as to the effect any change will have on the overall system. For example, in most systems that use disc storage the selection of a faster disc or drum could be expected to have a pronounced effect on the overall system performance;however, this fact may be overshadowed by the pronounced effect the selection may have on the system's cost.

The simulator given as an example will be required to simulate to a limited extent several of the various functions of a typical operating system, that is it will:

a). create and terminate transactions.

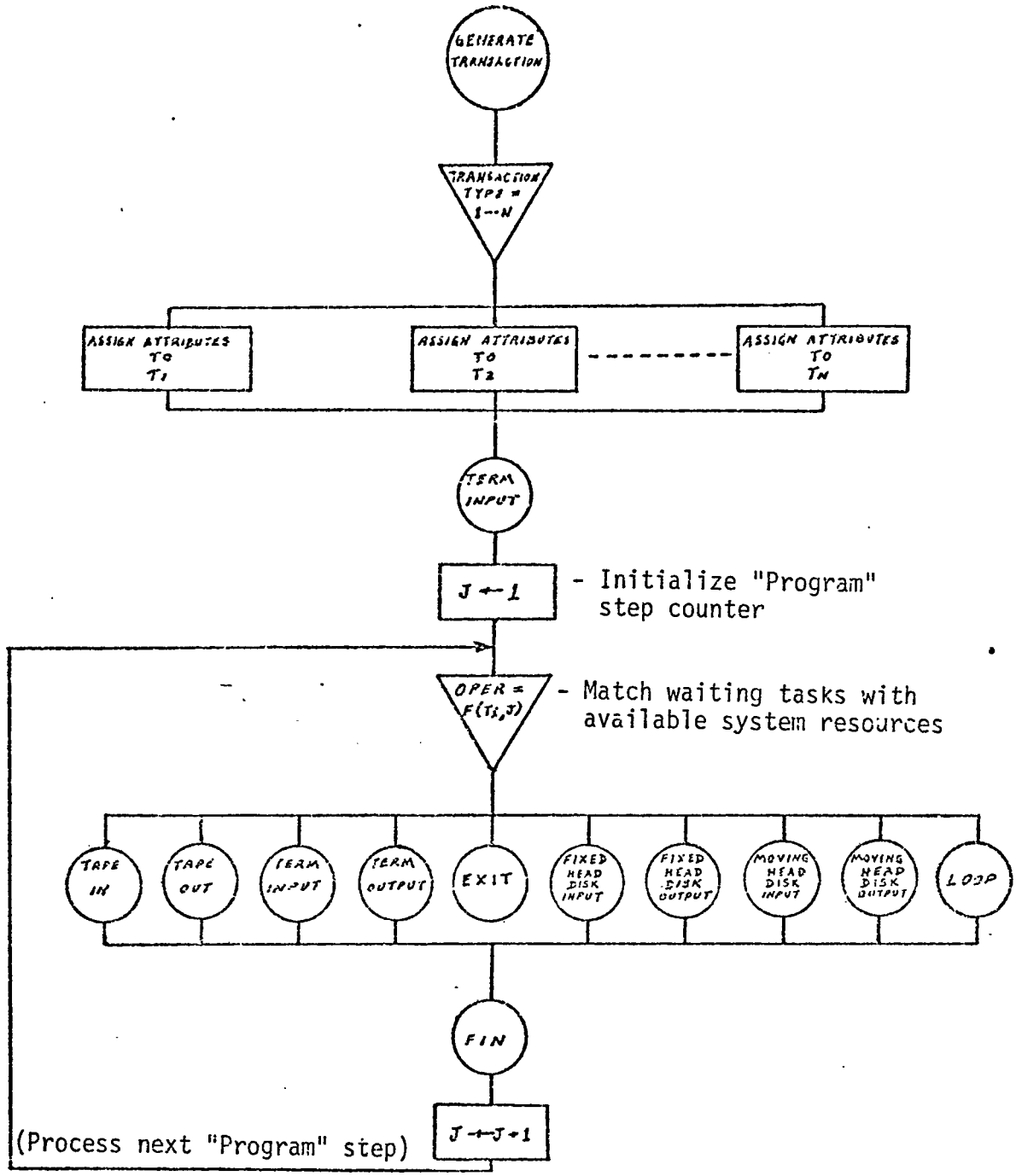
b). control the progress of all processes in the system.

c). allocate system resources such as-- input/output devices and routines, storage and processor time.

Any errors which might be expected to occur in normal system development and operation (27) will not be introduced into the simulation. However, this area should not be ignored in systems where common operations errors have been identified since simulation can prove beneficial in devising recovery techniques. Using simulation techniques one can evaluate alternative and degraded modes of system operation which might be used in the event of a system hardware failure, and in this way try to solve operational problems before they occur.

The simulator will consider 'operating system' resource preemption time as an unscheduled random preemption of selected system resources. Active transactions will be considered preemptable only by the 'operating system' or the various system hardware interrupts.

As mentioned previously, in the development of a system simulator it is useful to create a one-to-one correspondence between the elements of the simulator and the basic required events being simulated in the system, such as the input/output functions, transaction routing, and even the routine names. This correspondence is shown in the general simulator flow diagram, Figure 4. This diagram shows the routing of transactions from the time they are created; shows where the transactions are devided into separate tasks; and gives the general flow path each task will follow until it exits the simulator. A more complete description of the various segments of the simulator is provided in Section 6.



SIMULATOR FLOW DIAGRAM

FIGURE 4

This simulator is not designed to answer all possible questions about the target system. Certain information concerning the target system is assumed to be valid. Primarily, it is assumed that the user knows that the system will work. The simulator is not intended to determine whether a selected computer has sufficient I/O bus speed to accommodate a selected high speed disk, or if there is enough disk space available for the system's data base. Therefore, the simulator assumes that the specified system will accomplish the tasks required of it and the simulator will then provide data on the performance of the specified configuration.

6.0 THE SIMULATOR

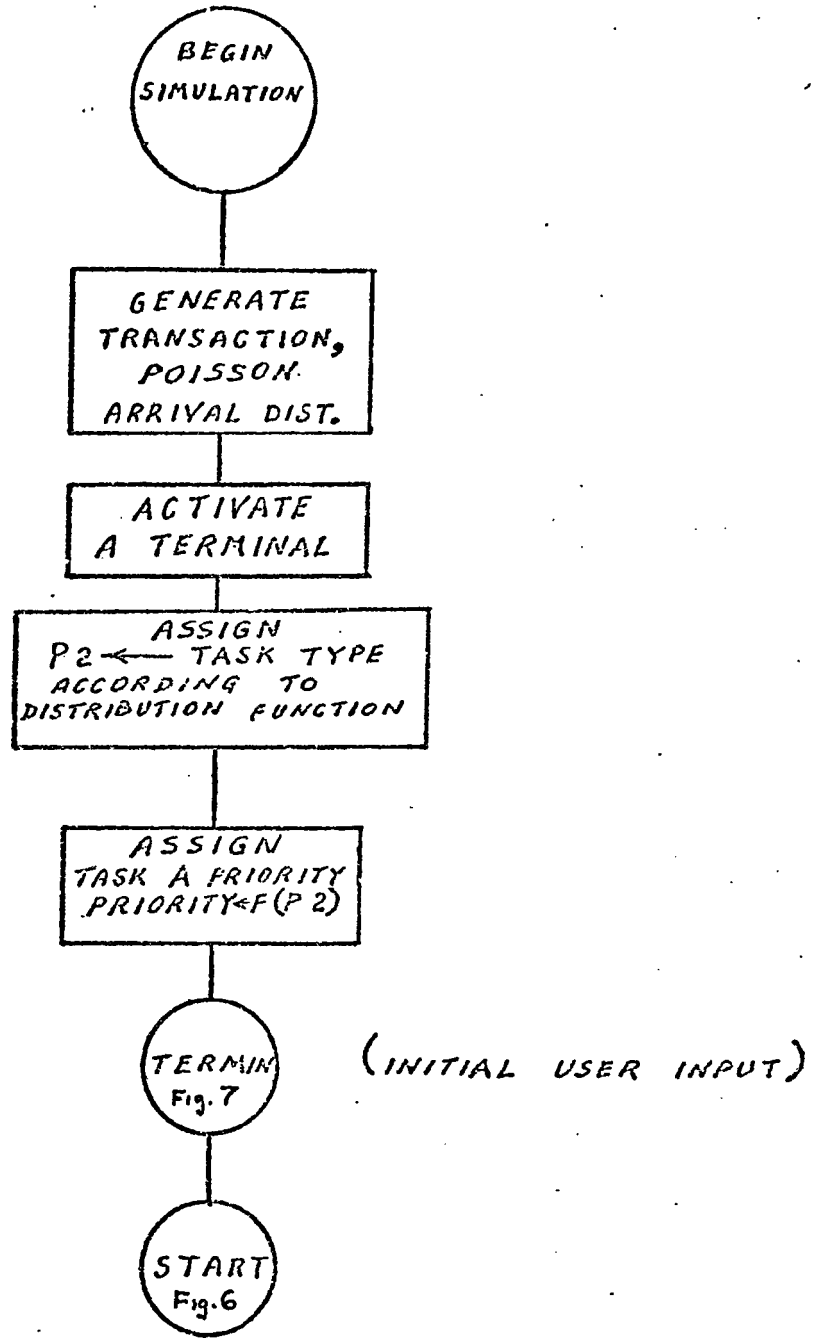
There are commercially available computer system simulators which can be used in much the same way as the simulator presented here. These simulators however are usually quite large and expensive and are supported by a data base which maintains the system definitions of a selection of popular computer systems. The systems supported are usually large "mainframe" type systems since it is probably felt that these are the type systems for which such an expensive tool might be justified.

The simulator presented here is not so powerful a tool as some of the large commercially available simulators. However, it is powerful enough and generalized enough to simulate a relatively wide range of "minicomputer" type applications. In fact in this way, the simulator which will be used to evaluate the performance of a conceptual system design will be partially validated by the simulation of a multitasking benchmark which will be run on an existing system with similar peripherals.

The simulator assembled for this example can be described as being comprised of two main sections. The first section serves as a 'Central Dispatcher'; this section of the simulator receives the initial input from a random exponential task generator and divides this input into one of the several user defined pseudo-process types, according to a user prescribed distribution, Figure 5. The Central Dispatcher, Figure 6, then

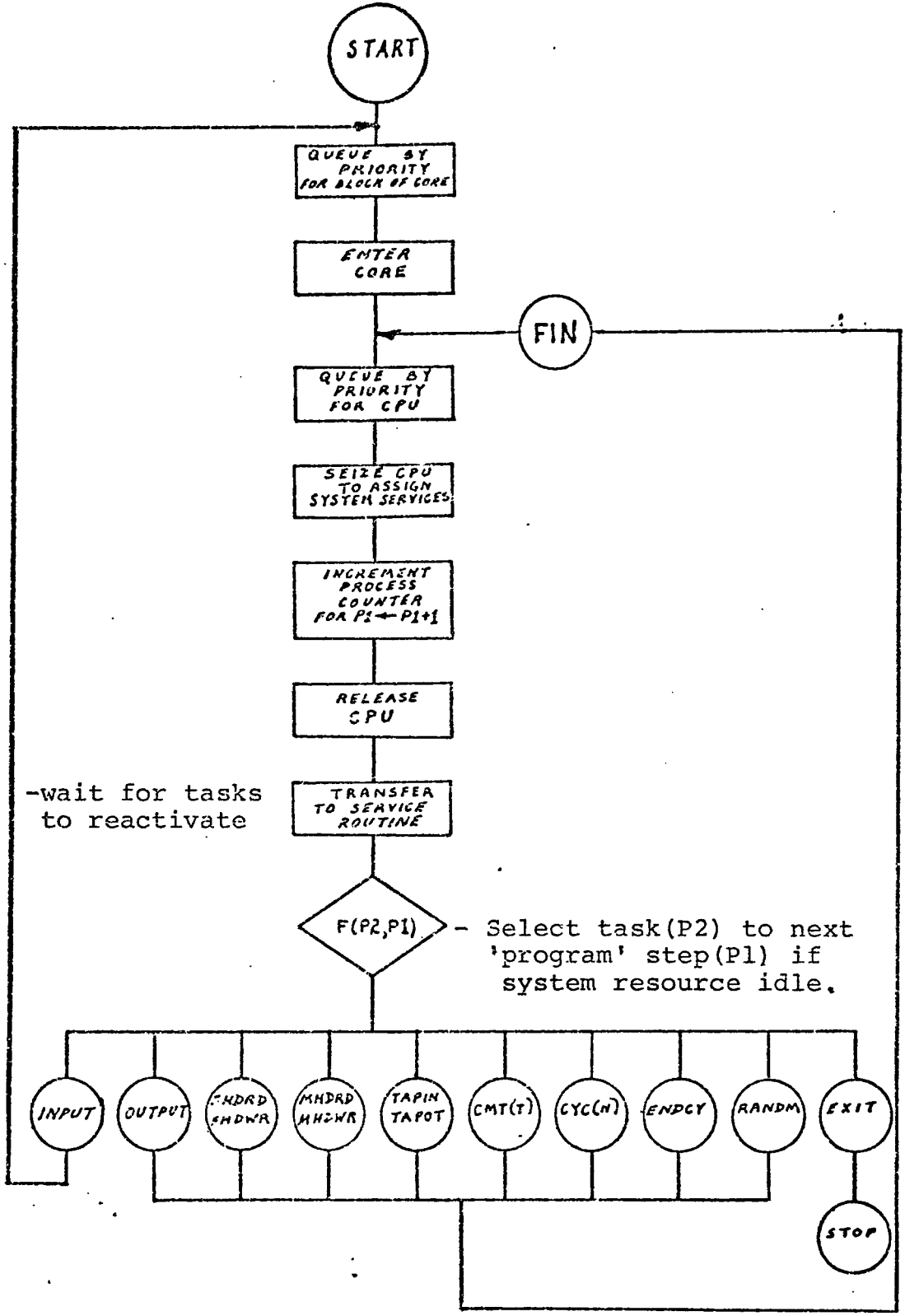
routes the tasks to the various system service routines according to the task priorities, which are also user assigned. The tasks are routed through the required system services in a sequence determined by the pseudo-process functions which define the system processing requirements of each task, Figure 6. These functions are explained further in Section 8.2.

The second main section of the simulator is comprised of the various system service routines through which the Central Dispatcher will route the tasks. These routines, or modules, and their functions are explained further in the following sections. Variables to the simulator which are used to define the target system's configuration are shown enclosed in parenthesis in the following sections and the use is described further in Section 8.1.



TASK GENERATOR

FIGURE 5

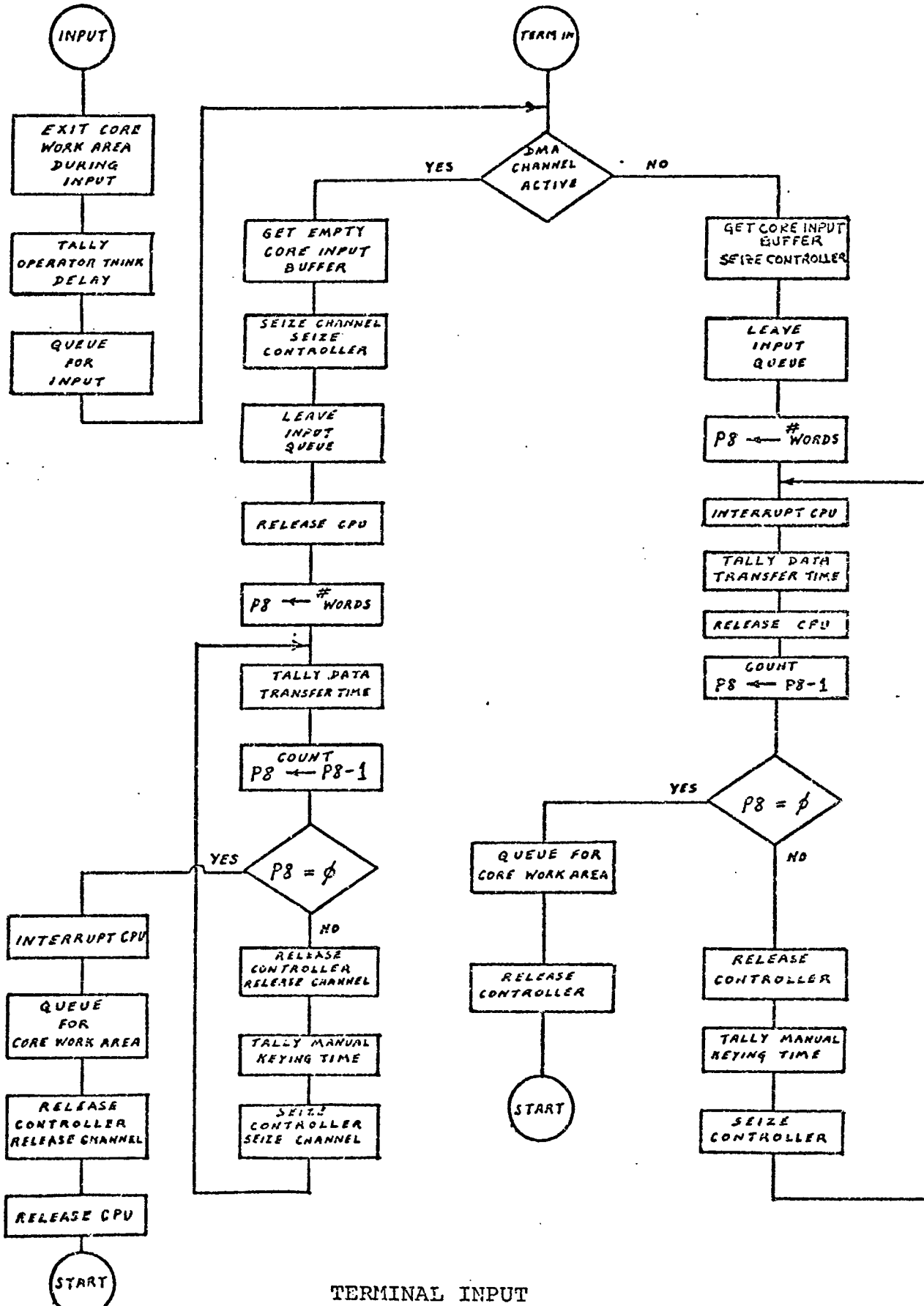


CENTRAL DISPATCHER

FIGURE 6

6.1 TERMINAL INPUT ROUTINE - INPUT

The INPUT routine, Figure 7, is used to simulate the input of data from a terminal user to the system. INPUT first will free this transaction's core work area, since it is unknown how long it will take the user to input data. INPUT then tallies an operator's think delay (THINK), or how long it may take the user to respond to the information the system may have sent him. INPUT will then obtain an input buffer, and transfer a specified number of words (WORDI) to the computer, as this transfer occurs INPUT will tally the data transfer time (CPUTM) and the time necessary for the operator to hit the terminal keys (TYPE) for each word transferred. When the transfer is complete, the CPU is interrupted and notified; INPUT then queues for a transaction core work area, releases the terminal devices, and transfers to the START routine, Figure 6, where the input buffer will be released.

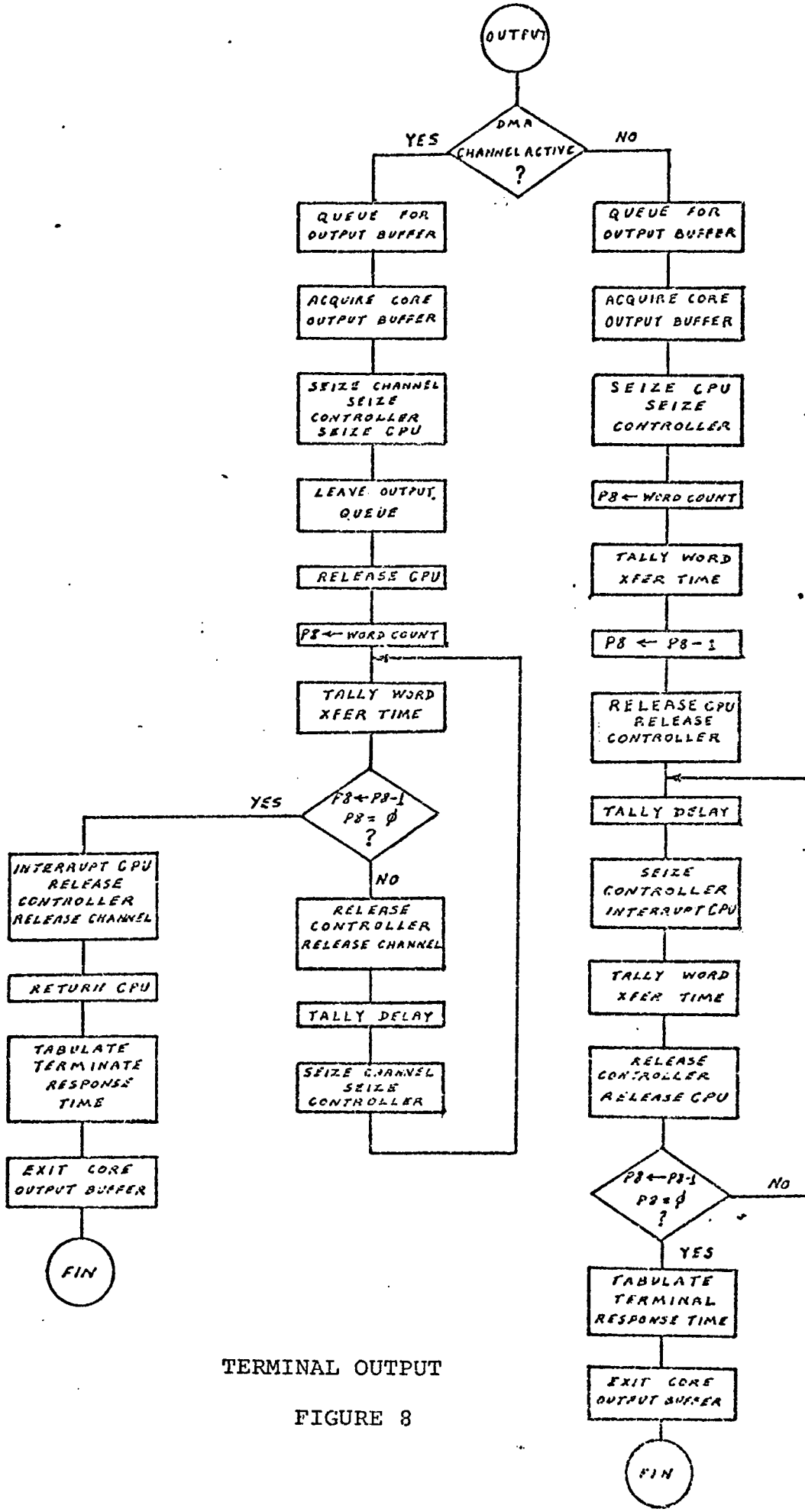


TERMINAL INPUT

FIGURE 7

6.2 TERMINAL OUTPUT ROUTINE - OTPUT

The OTPUT routine, Figure 8, is used to simulate the transmission of data from the system to an operator's terminal and tally the terminal response time which will be the amount of time since the last operator input for this transaction. OTPUT first obtains an output buffer, and then will transmit a number of words (WORDO) to an operator's terminal. OTPUT will tally the data transfer time for each word (CPUTM) and an interword delay (TRATE) for the transfer. When the transfer is complete OTPUT will release the terminal devices, notify the CPU of the transfer, tabulate the terminal response time, and exit the output buffer. Control is then transferred to FIN, Figure 6.

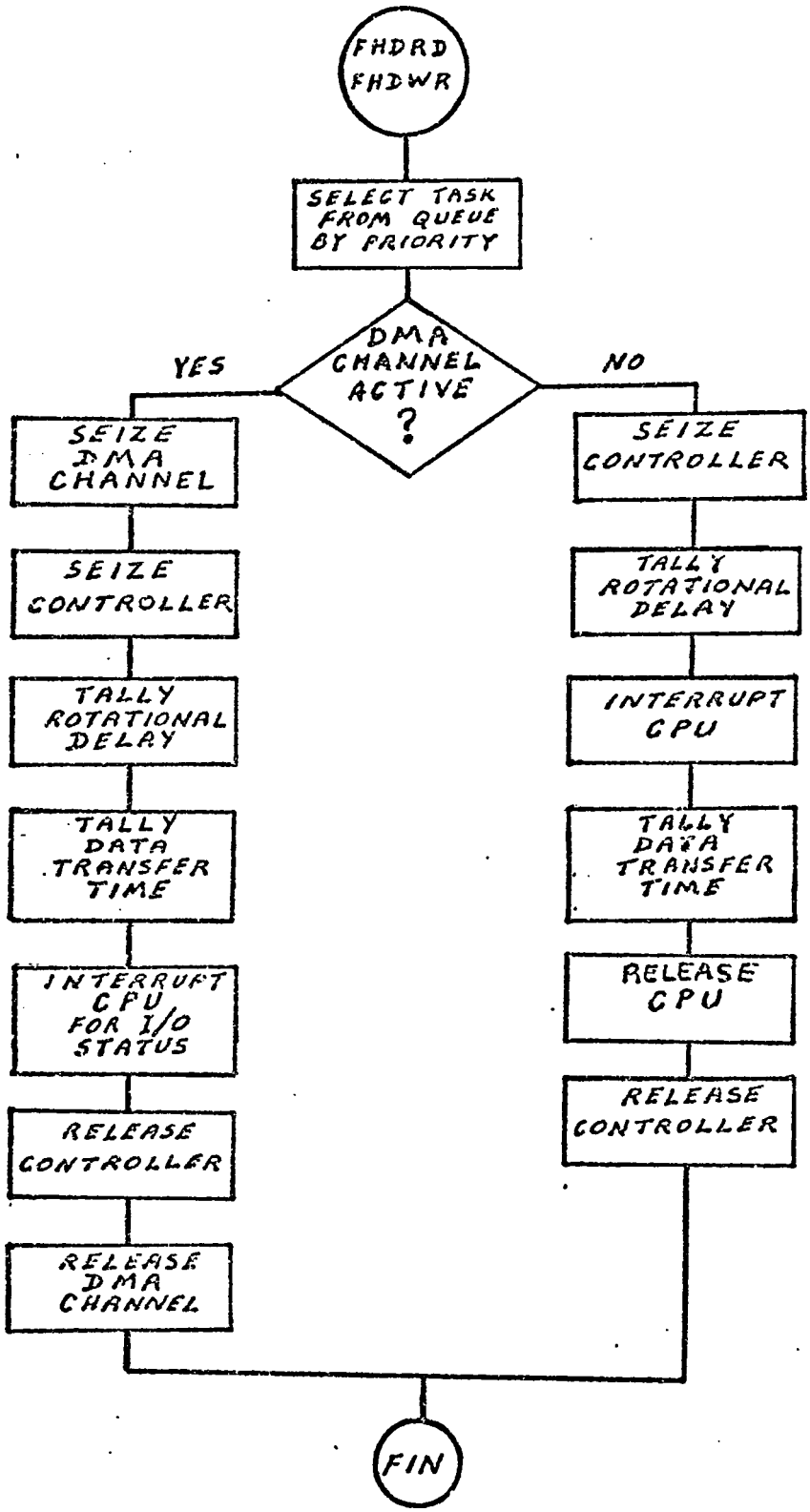


TERMINAL OUTPUT

FIGURE 8

6.3 FIXED-HEAD DISK READ/WRITE ROUTINES - FHDRD/FHDWR

The FHDRD/FHDWR routines, Figure 9, are used to simulate a read or write of one sector of the fixed-head disk. The routine will select the next transaction from its wait queue by priority and transfer one disk sector. The routine will tally the sector rotational delay (FROT) and the sector transfer time (READF). When the transfer is complete the CPU is interrupted and notified of the completion of the transfer. The disk devices are released and control is transferred to FIN, Figure 6.

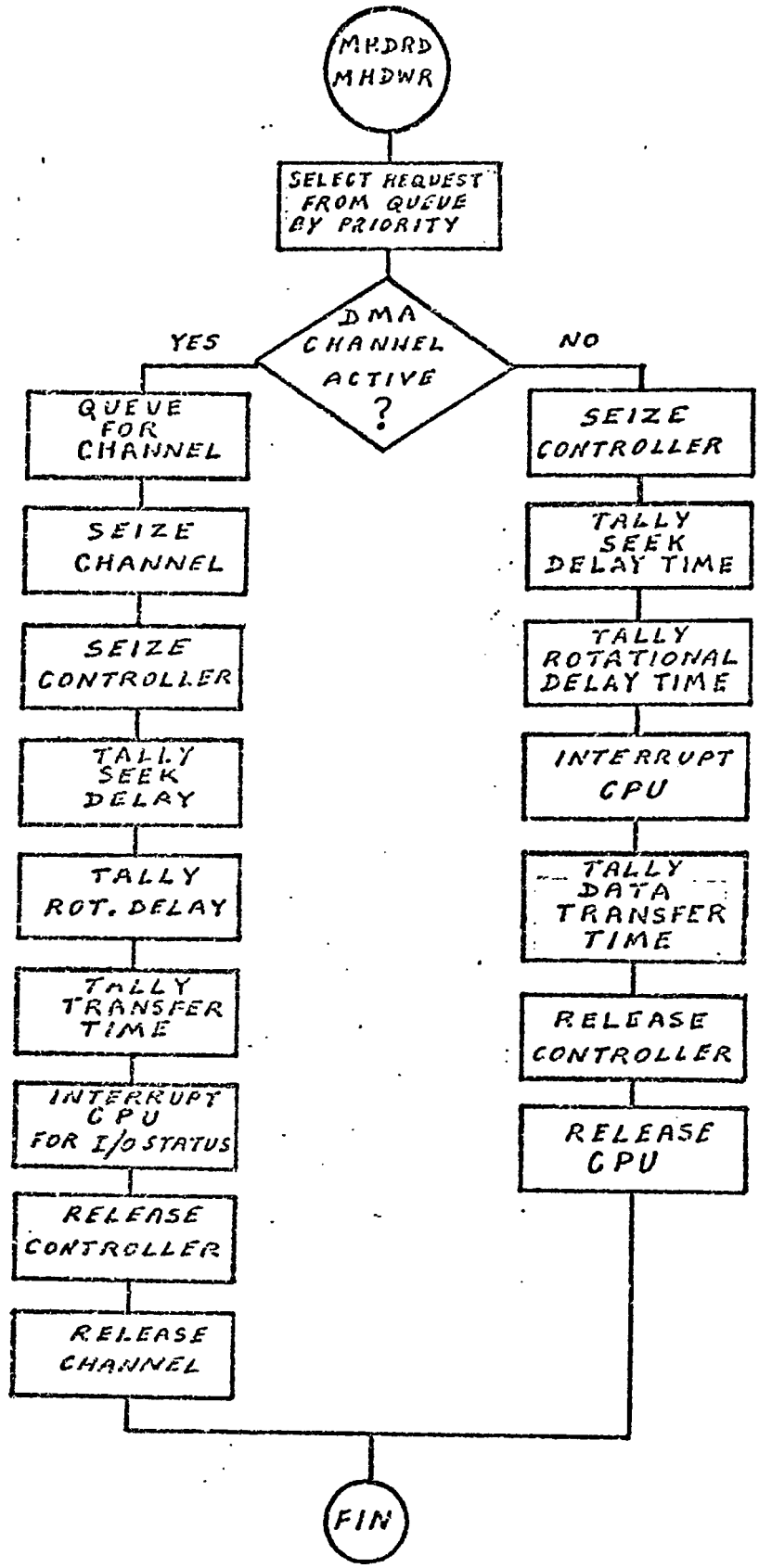


FIXED HEAD DISK READ/WRITE ROUTINE

FIGURE 9

6.4 MOVING-HEAD DISK READ/WRITE ROUTINES - MHDRD/MHDWR

The MHDRD/MHDWR routines, Figure 10, are used to simulate the read or write of one sector of the moving-head disk. The routine will select the next transaction from its wait queue by priority and transfer one disk sector. The routine will tally the sector seek (LATRL) and rotational (MROT) delay and the sector transfer time (READM). When the transfer is complete the CPU is interrupted and notified and the disk devices are released. Control then transfers back to FIN, Figure 6.

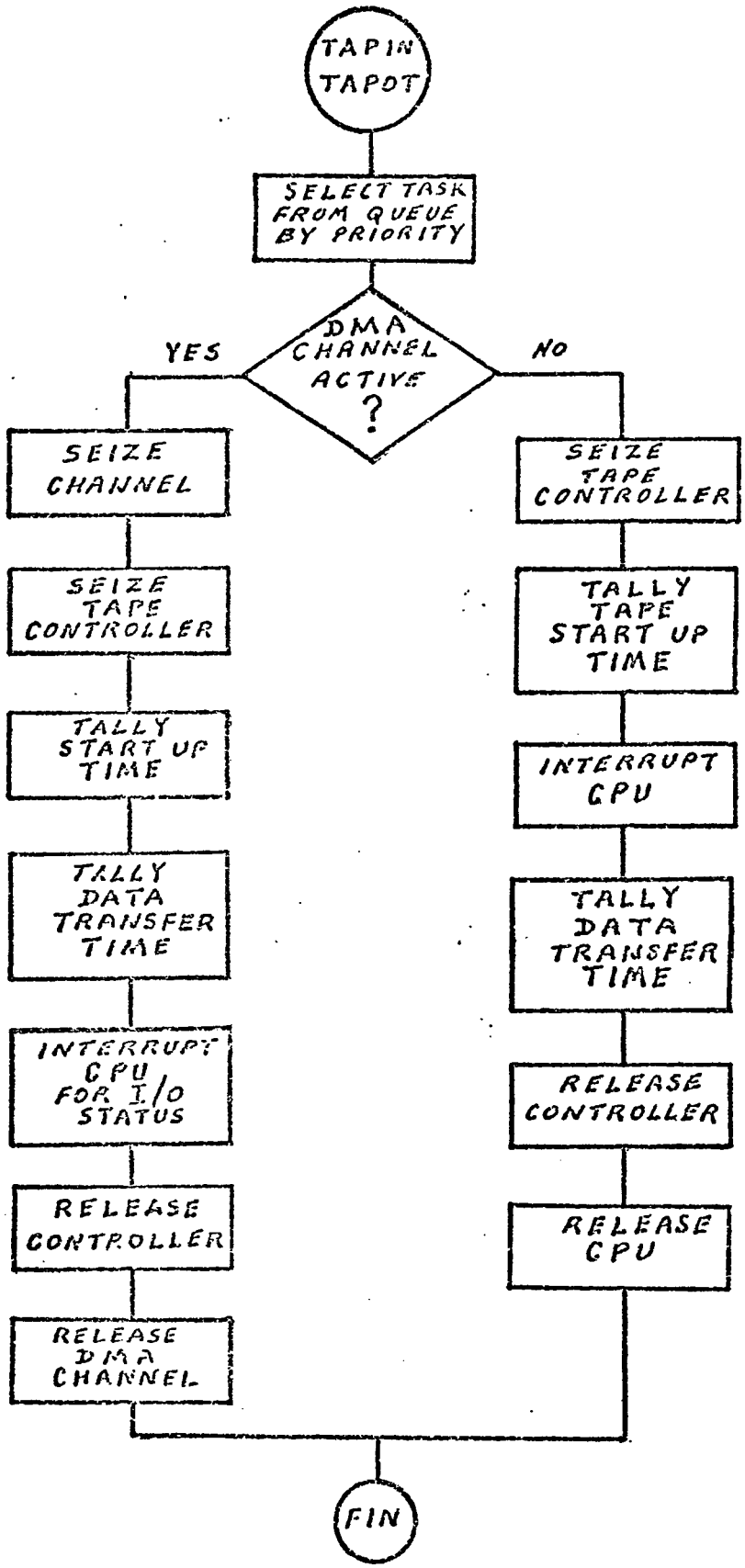


MOVING HEAD DISK READ/WRITE ROUTINE

FIGURE 10

6.5 MAGNETIC TAPE READ/WRITE ROUTINES - TAPIN/TAPOT

The TAPIN/TAPOT routines, Figure 11, are used to simulate a read or write of one record to the magnetic tape drive. The routine will select the next transaction from its wait queue by priority and transfer one record. The routine will tally the tape access time (TPACC) and the time required to transfer one record (RDTAP). When the transfer is complete the CPU is interrupted and notified, and the tape devices are released. Control then transfers back to FIN, Figure 6.

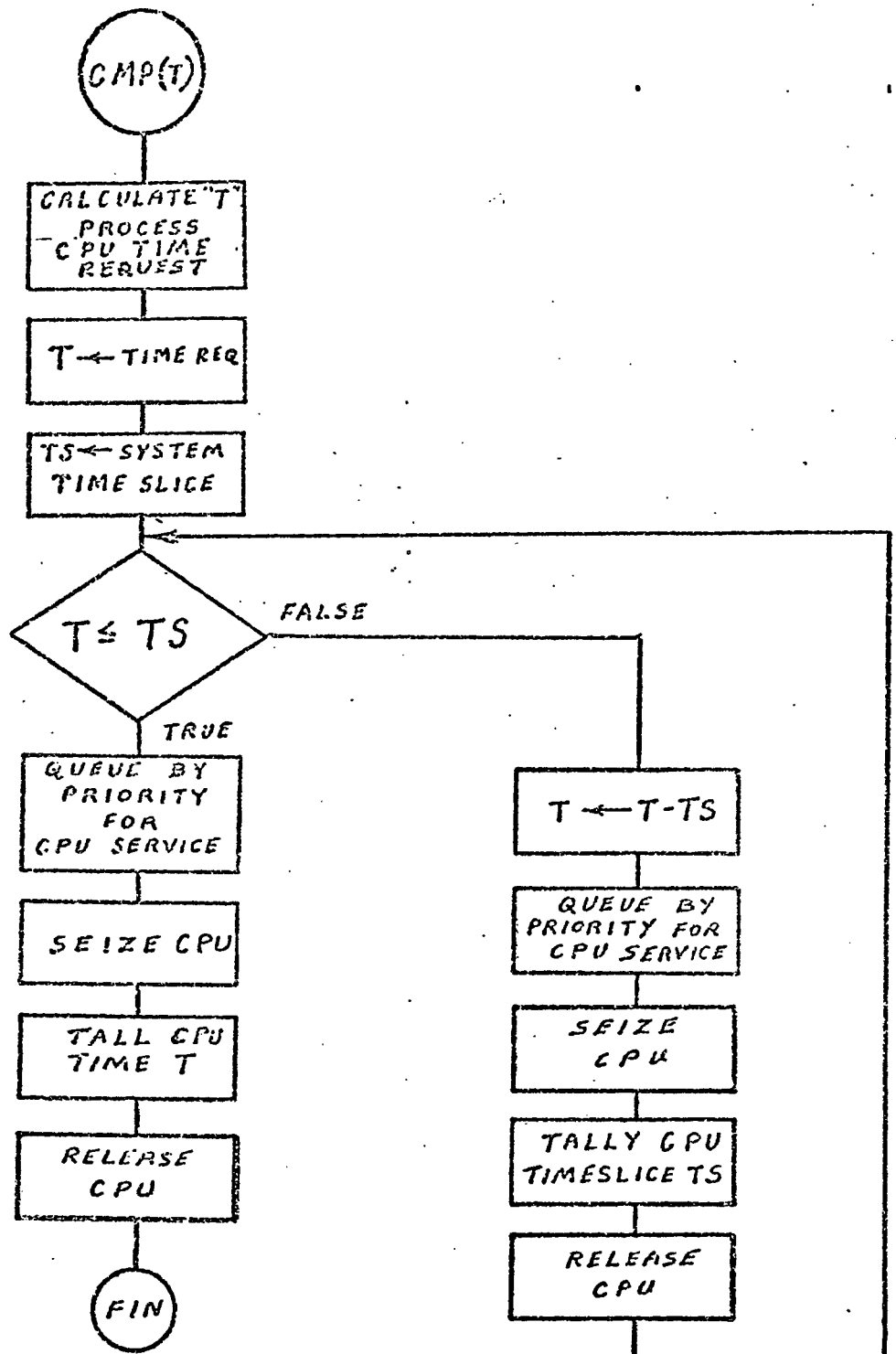


MAGNETIC TAPE READ/WRITE ROUTINE

FIGURE 11

6.6 COMPUTATION TIME ROUTINE - CMP(T)

The CMP(T) routine is used to tally the amount of time a transaction is utilizing the CPU. The entry point into the CMP(T) routine determines the amount of time requested (T) by the transaction. The routine will then seize the CPU if it is available and decrement (T) while tallying the CPU utilization time by a given system timeslice (SLICE). At the end of a timeslice the CPU is released, and if a higher priority transaction is queued for service, the CPU will then be seized by the higher priority transaction. If no higher priority transaction is queued for service, (T) is again decremented and the amount tallied until (T) equals zero. The CPU is then released and control is transferred to FIN, Figure 6.



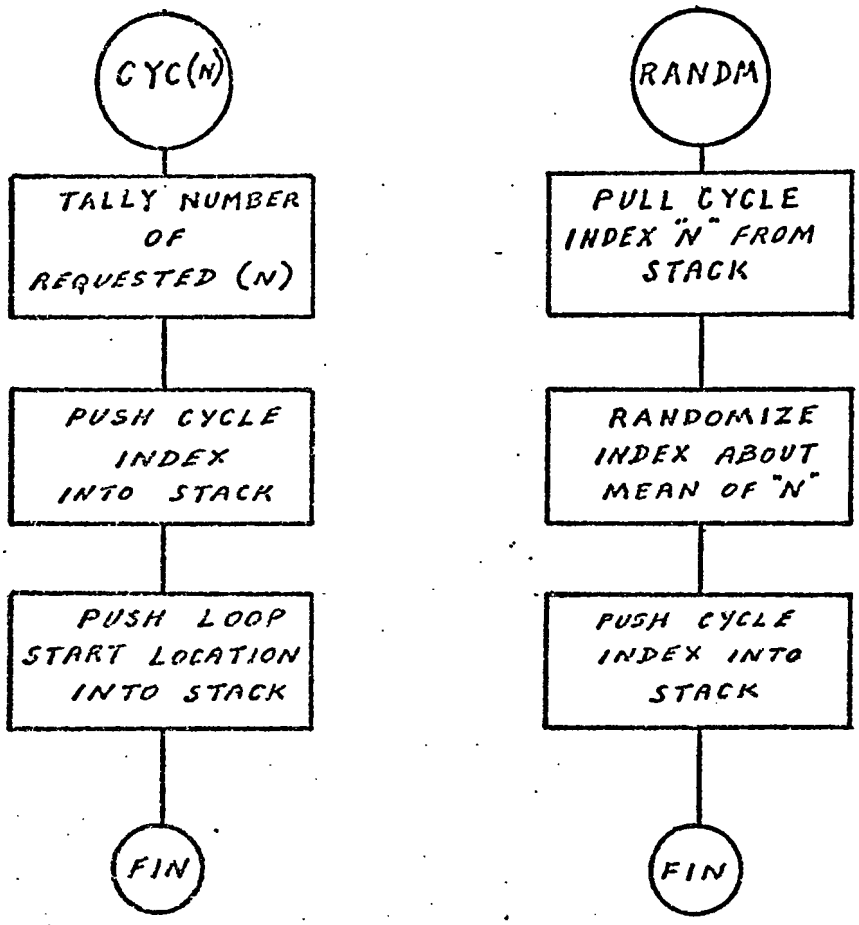
COMPUTE TIME ROUTINE

FIGURE 12

6.7 LOOP CONTROL ROUTINES - CYC(N), RANDM, ENDCY

The routine CYC(N), Figure 13, is used to initiate a loop sequence through a segment of the software simulation function; these loops can be nested 5 deep. The CYC(N) first calculates the number of cycles of this loop (N) and then pushes this number into the transaction's loop counter stack which is kept in parameters 16-20 of the transaction, with parameter 5 used as the stack pointer. The starting location of the loop is then stored in a return location stack which is kept in parameters 11-15 of the transaction, with parameter 4 used as the stack pointer. Control then transfers to FIN, Figure 6, to proceed with the steps internal to the loop.

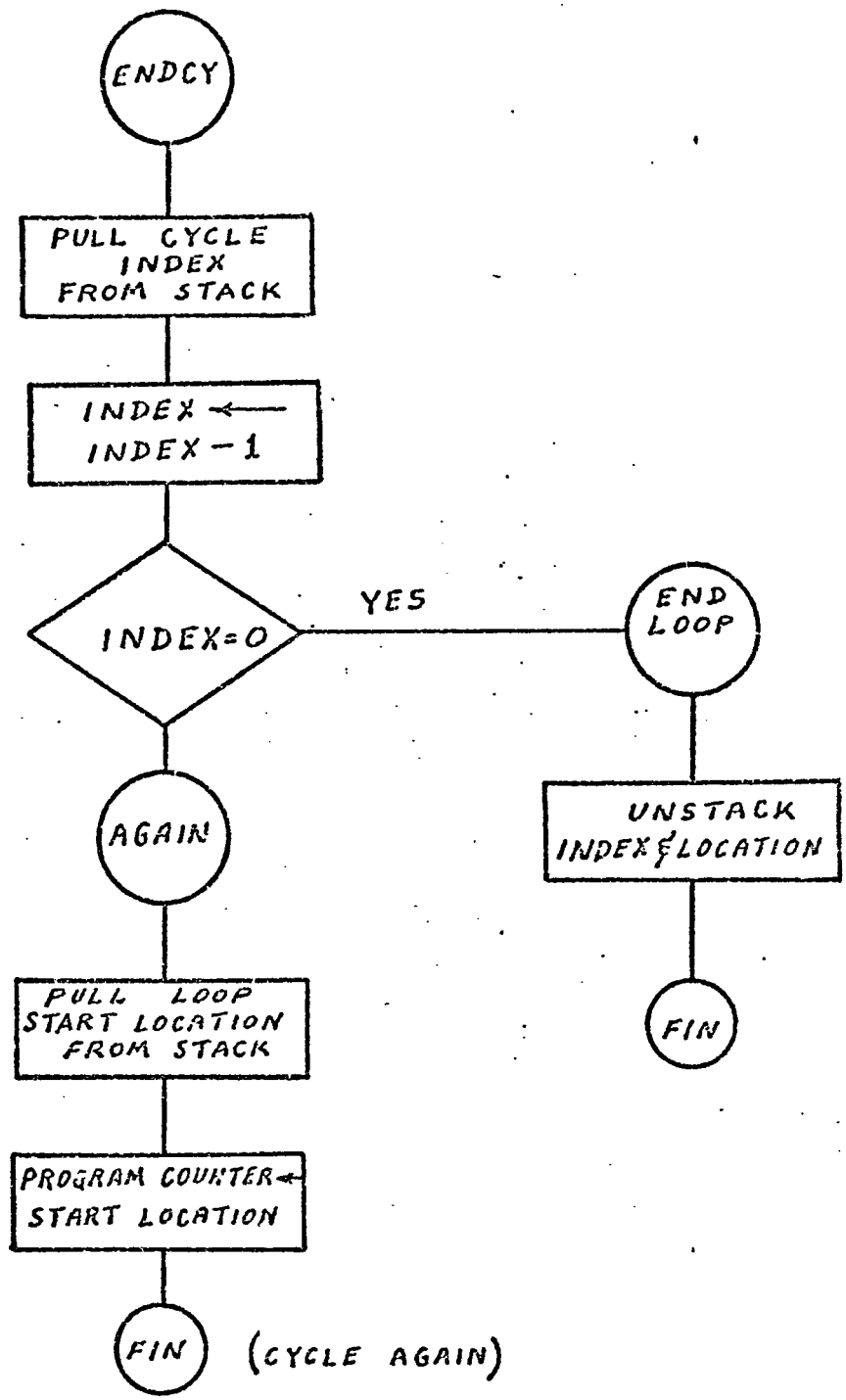
The routine RANDM, Figure 13, can be used to randomize the number of cycles a loop routine will make. RANDM will randomize the cycle index (N) about a mean of (N). This routine call, when used, must follow the CYC(N) call immediately in the software simulation function, and it will pull the cycle index (N) from the stack, randomize the number and return it to the stack. Control is then passed to FIN, Figure 6.



LOOP DESIGNATOR ROUTINES

FIGURE 13

The routine ENDCY, Figure 14, marks the end of a loop sequence; it decrements the cycle index and then will continue or loop if the cycle index is not zero. This routine pulls the cycle index and decrements the number; if the index is zero the index and starting location are pulled from the stacks and control is then passed to FIN, Figure 6. If the decremented cycle index is not equal to zero the loop start pointer is pulled from the stack and placed in the operation designator, parameter 1 of the transaction. Control is then passed to FIN, Figure 6.

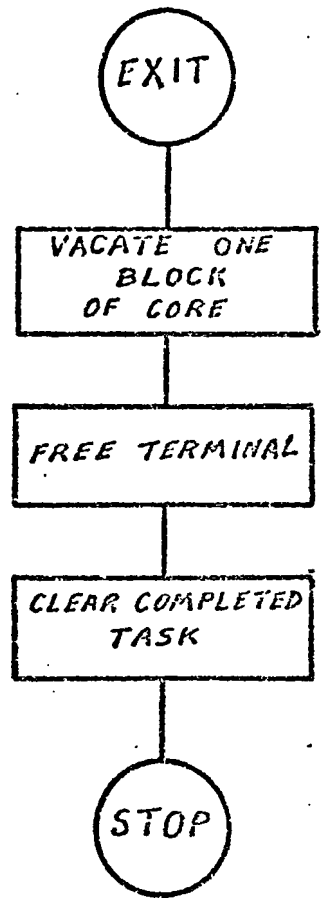


LOOP CONTROL ROUTINE

FIGURE 14

6.8 EXIT - EXIT

The EXIT routine, Figure 15, marks the end of a software simulation function. This routine deallocates core if required, frees the terminal and terminates the transaction.



EXIT ROUTINE

FIGURE 15

7.0 A TARGET SYSTEM

The type of dedicated demand processing system selected for a simulation example was a department store type point-of-sale real-time accounting system. This system would be responsible for all on-the-floor sales, credit accounts, and inventory control. The basic four system transactions, or tasks, the simulator will be required to process are:

a). cash sales

b). credit verification and sales

c). payments on customer accounts

d). inventory receiving and control

These transactions will all be processed in real-time from remote terminals. The basic system will utilize the following hardware for interactive processing:

a). central processor

b). direct memory access (DMA) channels

c). fixed and moving-head disks

d). tape drive

e). remote terminals

A more complete description of the target system's configuration used for the simulation will be found in Appendix A; at the end of the simulator listing where the system hardware and software specifications are listed.

8.0 SIMULATION OPERATING ENVIRONMENT

8.1 HARDWARE DEFINITIONS

The simulator is defined, as to the system hardware configuration, by a collection of variables or parameters. These variables can readily be changed, even in the middle of a simulation run. Because of this , system configurations can easily be compared by changing the variables which define the system component of interest.

The basic GPSS statements which are used to define the hardware environment are the VARIABLE and STORAGE statements. The VARIABLE statement introduces a constant or an arithemetic expression into the simulation model; the introduction of a VARIABLE statement into a GPSS model will provide that variable value for use throughout the simulator. Furthermore, should a variable be redefined, the last value of the variable introduced into the simulator will be the only valid value from the time it is introduced. Therefore, by redefining a variable which represents an equipment attribute, the hardware configuration of the system can be changed.

The STORAGE statement assigns a quantity of storage to a GPSS storage entity. In this manner storage, units of equipment, and buffers can be defined. The STORAGE statement, like the VARIABLE statement, once defined is valid throughout the GPSS simulator, and once a STORAGE statement redefines a storage entity, the redefined value will then supercede

the initial storage value. This is also the method used to redefine a simulation model in mid-run. However, when a run is modified a RESET or CLEAR card is inserted into the simulator in order to clear the statistics gathered to date.

CPU and Central System Parameters

The simulator input parameters defining the central system are as follows:

*2	8	..	1 9	
WDSIZ	VARIABLE		XX	Computer word size in bits
SLICE	VARIABLE		XXX	CPU sharing time-slice in milliseconds
TASKS	VARIABLE		XXX	Task capacity of system
BUFFI	STORAGE		XXX	Number of terminal input buffers
BUFFO	STORAGE		XXX	Number of terminal output buffers
SYCPU	VARIABLE		XXX	CPU system overhead percentage
SYCHN	VARIABLE		XXX	System disk storage overhead percentage
SYSCH	VARIABLE		XXX	CPU system scheduling overhead, time required to "schedule" each system event, in milliseconds

* Indicates card columns for GPSS.

Terminal Operating Definitions

The following GPSS statements define the terminal characteristics, operating constraints, and data transfer rates.

*2	8	19	
MUXCH	VARIABLE	X	A 1 in column 19 indicates a mux channel is used, and a 0 indicates CPU controlled transfers.
BAUD	VARIABLE	XXXX	Terminal baud rate.
TYPE	VARIABLE	XXXX	Estimated time delay between input character, milliseconds.
THINK	VARIABLE	XXXXX	Average time between computer response and operator reply, milliseconds.
CPUTM	VARIABLE	XX	Time required by CPU to process one character to/from a terminal in the non-channel mode, milliseconds.
WDTRN	VARIABLE	XX	Time required by channel to transfer one character to/from terminal, milliseconds.
WORDI	VARIABLE	XX	Average number of characters input from a terminal.
WORDO	VARIABLE	XX	Average number of characters output to a terminal.
TERMS	STORAGE	XXX	Number of terminals in the system.

* Indicates card column for GPSS input.

Disk Storage System Definitions

The following GPSS variables define the operation of the target system's disk storage system.

```
                          1
*2      8          ...9
```

CHANA	VARIABLE	X	A 1 in column 19 indicates that channel A is used, and a 0 that the CPU is controlling the data transfers. This is for the fixed head disk
CHANB	VARIABLE	X	A 1 in column 19 indicates that channel B is used, and a 0 that the CPU is controlling the data transfers. This is for the moving head disk.
LATRL	VARIABLE	XXX	Average lateral positioning time for moving head disk, milliseconds.
MROT	VARIABLE	XXX	Average rotational access time for moving head disk, milliseconds.
READM	VARIABLE	XXX	Transfer time for one sector to/ from the moving head disk, milliseconds.
FROT	VARIABLE	XXX	Average rotational access time for the fixed head disk, milliseconds.
READF	VARIABLE	XXX	Transfer time for one sector to/ from the fixed head disk, milliseconds.

Tape Storage Definitions

The following GPSS variables define the magnetic tape storage peripheral.

```
                      1
*2      8        .. 9
```

CHANC	VARIABLE	X	A 1 in column 19 indicates that channel C is used, a 0 that the CPU is controlling transfers.

* Indicates the card column for GPSS input.

*2	8	.. 1 9	
TPACC	VARIABLE	XXX	Tape drive start-up time, milliseconds.
RDTAP	VARIABLE	XXX	Time required to read/write one tape record, milliseconds.

8.2 OPERATIONAL SOFTWARE ENVIRONMENT DEFINITIONS

The operational environment of the simulator is defined using a series of GPSS "functions". These functions provide the simulator with the information necessary to create an accurate simulation work environment. These functions like the hardware definition statements may be redefined at any time during a simulation in order to modify the system work characteristics or task mixes. The three basic functions used are described in the following sections.

Task Distribution Function

This function takes a GPSS random number input that ranges from 0 to .999 and will assign a pseudo-process (or task) number to a newly created transaction according to the distribution defined by the function. Transaction type is determined by the function input variable, which for the task distribution function is a random number (RN2). The following are typical task distribution functions.

* Indicates the card column for GPSS input.

```
                    1
*2      8       ..  9
 DISTR FUNCTION     RN2,D2   50/50 distribution of two tasks.
.25,1/.75/2
```

Any random number generated from 0 to .499 will result in the selection of task type 1; random numbers in the range .50 to .999 will select task type 2.

```
                    1
*2      8       ..  9
 DISTR FUNCTION     RN2,D3   25/25/50 distribution of three
.125,1/.375,2/.75,3          tasks.
```

Any random number generated between 0 and .249 will result in the selection of task type 1; random numbers in the range .25 to .499 will select task type 2; and task type three is selected by a random number between .5 and .999.

Priority Assignment Function

This function will assign a priority level to each of the pseude-processes (or tasks). GPSS provides for 128 priority levels; the higher the numerical priority the higher the priority level. The following is a typical priority function; the input parameter is the task type (P2) which then selects a priority level from the list.

```
                    1
*2      8       ..  9
 PRITY FUNCTION     P2,L4    Priority assignments for four tasks.
1,4/2,3/3,2/4,1
```

The above function will make the following priority

* Indicates the card column for GPSS input.

assignments according to the input variable (P2) which is the task type stored in parameter 2 of the transaction.

task 1 - priority 4
task 2 - priority 3
task 3 - priority 2
task 4 - priority 1

Pseudo-process Definition Functions

The pseudo-process functions are built similar to a typical program and define the various system services required by a task and the sequence in which these services are required. These functions also have a looping feature and can cycle through and section of the function. The loop control index can be randomized if desired. The system services controlled through the pseudo-process functions are:

CMPxx	This is a request for xx milliseconds of CPU processing time. xx can range from 5 to 95 milliseconds in 5 millisecond increments.
CYCxx	This is the statement which begins a looping sequence. xx denotes the number of cycles. The loop segment is delimited by an ENDCY statement. Loops can be nested to 5 levels providing an inner loop is completely contained by all outer loops.
ENDCY	This statement is the delimiter for a loop.
RANDM	This statement will randomize the loop index of the preceeding CYCxx statement. The RANDM statement must follow the CYCxx statement immediately.
FHDRD/ FHDWR	This is a request for the system to read or write one sector on the fixed head disk.

MHDRD/ MHDWR	This is a request for the system to read or write one sector on the moving head disk.
TAPIN/ TAPOT	This is a request to read or write one record on the magnetic tape unit(s).
INPUT	This is a request for input from a user terminal. The task is then dormant awaiting user response.
OTPUT	This is a request for a message to be sent to a user terminal.
EXIT	This statement identifies the end of a Pseudo-process (or task).

The Pseudo-process function is used in the following manner. The task type, stored in parameter 2 of the transaction, directs the simulator to choose the pseudo-process function of the same number. Progress of the task through the function is then controlled by the input to the function which is parameter 1 of the transaction. Parameter 1 of the transaction therefore serves as a "program counter" for the pseudo-process. This counter is incremented or modified as required until the task progresses through to completion (EXIT).

A typical pseudo-process function is constructed in the following example.

```
                    1
*2      8       ..  9
 2      FUNCTION    P1,L10  Task #2, input P1, 10 statements
1,CYC4                      Loop 4 times for account search
2,RANDM                     Randomize above loop index
3,FHDRD                     Read account directory
4,CMP10                     Check directory
5,ENDCY                     End of loop
6,MHDRD                     Read required account record
7,CMP15                     Update account for payment
8,OTPUT                     Acknowledge payment to terminal
9,TAPOT                     Write transaction record to tape
10,EXIT                     End of task
```

The above example is used in the simulator to depict a task which might be used to update a customer's account when payments are received. Note that there is no initial terminal input shown, since this is a dedicated demand system it is assumed that all tasks, or transactions, originate with a user terminal input request.

* Indicates the card column for GPSS input.

9.0 THE SIMULATION OF A DEMAND SYSTEM

Simulation experiments were run to predict the performance of the hypothetical target system defined in section 7.0. The results of these experiments were examined and the the system configuration was modified accordingly. The experiments were comprised of four simulation runs to accommodate for any statistical anomalies which might arise when evaluating a single simulation run. The first simulation run of each experiment was first initialized with system transactions to remove the simulation start-up bias. The initialization run lasted for 2 minutes of simulated time and the four simulation runs lasted 5 minutes each. This series of simulation runs of the target system, the baseline of which is defined at the end of Appendix A, produced the following results when interpreted as suggested by Figure 1.

9.1 EXPERIMENT #1 - BASELINE

System Performance

Tasks initialized	700
Tasks completed	631
System/terminal interactions	1988
Input wait time	23700 ms.
System response time	23997 ms.

Output Analysis

Analysis of experiment 1 shows the utilization of all resources to be below 25% (for a summary of the results of the experiments see Appendix C); therefore; no system overload conditions seem to exist. The system response time is very good, yet there is a long wait for terminal input. Examination of the input buffers showed a 100% utilization factor, and that the buffers were saturated at the end of the simulation. Therefore a bottleneck existed which degraded overall system performance; resulting in a long wait for input time.

System Configuration Redefinition

Since analysis showed input queue congestion, the number of input buffers will be increased by 10.

9.2 EXPERIMENT #2

System Performance

Tasks initiated	809
Tasks completed	822
System/terminal interactions	2487
Input wait time	186 ms.
System response time	504 ms.

Output Analysis

Analysis of the results show a significant improvement in turnaround time, which brings the user wait time within acceptable limits. It can also be seen that the system response time was slightly longer indicating a higher level of utilization of the system resources, and this can also be observed as the number of tasks completed increased by 30%.

System Configuration Redefinition

The baseline simulator services tasks using a one priority first-in-first-out (FIFO) technique. Response will next be evaluated using a FIFO technique with different priority levels assigned to the tasks. For the next experiment, long transactions with the highest number of system/terminal interactions will be given the highest priority.

9.3. EXPERIMENT #3

System Performance

Tasks initialized	804
Tasks completed	818
System/terminal interactions	2537
Input wait time	250 ms.
System response time	571 ms.

Output Analysis

Analysis of experiment 3 shows that while there was a slight increase in throughput, the system suffered an increase in turnaround time of 13%. This is most likely due to the fact that long jobs which are given the highest priority are also the most common system tasks. Therefore, the system would tend to always be processing these tasks, leaving the shorter tasks partially blocked by the system. This would also account for the 34% increase in input wait time.

System Configuration Redefinition

The next experiment will evaluate a priority scheme designed to penalize the longer tasks by giving them the lower priorities.

9.4 EXPERIMENT #4

System Performance

Tasks initialized	790
Tasks completed	794
System/terminal interactions	2603
Input wait time	75 ms.
System response time	396 ms.

Output Analysis

Analysis of this experiment shows that while system throughput is greater than in some of the previous experiments, the system response time and input wait times are greatly improved by this configuration and should provide the user with quick responses to input requests.

The correctness of one's analysis of the experimental results naturally is directly dependent on the correctness of the simulator and its ability to predict changes in system performance based on differing system configurations. Therefore, before one can act on the simulation data, some means of verifying the simulator's correctness is required. The next section deals with the validation of the simulator.

10.0 SIMULATOR VALIDATION

Simulator or model validation is one of the more difficult aspects of performance evaluation. There is no established 100% accurate technique for evaluating the correctness of a simulator or model. Therefore, any technique employed must involve compromises, and common sense is one of the most valuable assets in the evaluation of the validation data. A system model (whether analytical or simulation) is rarely expected to represent an accurate 1 to 1 mirror image of the target system's performance. The user is not normally interested in whether selecting a faster peripheral device will change the system response time from 8.934ms to 7.594ms., but rather that the change in the system should give approximately a 15% improvement in system response time in that particular application. Performance data should be interpreted this way since typically a simulator's accuracy in predicting a target system's performance can be as good as 5% or as bad as 50%. Even a model "proven" accurate under one specified operating environment may prove not nearly so accurate under a differing environment. This discrepancy in a model's (analytical or simulation) performance is due to various trade-off decisions which must be made in order to create the model.

Some common modeling trade-offs which can affect the accuracy of the results are:

- The amount of detail in an analytical or simulation model will affect the model's accuracy.
- In analytical modeling, simplifications of the system and certain assumptions must often be made so that the analytical model will have a solution.
- The amount of detail and correctness of the workload characterization of the target system will also affect the accuracy of the results.

The validation of the simulator will be in two parts. First the basic simulator will be validated by comparing simulation results with pencil and paper calculations of expected results from selected portions of the simulator. In this way, the modules which represent the various system resources, such as the disks, tape drives, etc. can be verified to see if they perform as expected.

Additionally, the simulator will be validated by configuring it to model and existing system with a known workload. This system will be a ROLM 1602A system with floppy disks and 75 ips tape transports. Various workloads will be run on the target system and the simulation model, and the results will then be correlated.

The results of the validation experiments must be analyzed to determine whether the simulator is performing satisfactorily. The statistical analysis of the validation

experiment results should give the user of the simulator confidence in the ability of the simulator to predict the target system's performance. Furthermore, it should give an estimate of the accuracy of these predictions.

The results of the validation experiments will therefore be correlated and analyzed as follows. In each case it will be assumed that the simulation results bear a linear one-to-one relationship to the target results, such that:

$$X = aY + c$$

Where: X represents the simulation results
Y represents the target results
a = 1
c = 0

Therefore, if the simulator bears a perfect one-to-one relationship with a target system, this relationship would naturally be represented by -

$$X = Y$$

To verify the linear correlation between the simulation results and the target results, the product-moment formula will be used to determine the linear correllation, r.

$$r = \frac{\Sigma xy}{((\Sigma X^2)(\Sigma y^2))^{\frac{1}{2}}}$$

This coefficient will reflect the degree to which the linear relationship X = aY + c can be considered an accurate representation.

We can go one step further and determine the standard error of estimate, $S_{x,y}$. This will reflect the accuracy of the assumption X = Y, and can give a 95% confidence interval for which the results should be valid. The properties of the standard error of estimate are analogous to those of the standard deviation. From this, lines constructed at a horizontal distance from the X = Y curve, as shown in Figure 16, should include all the samples within the confidence limits given below.

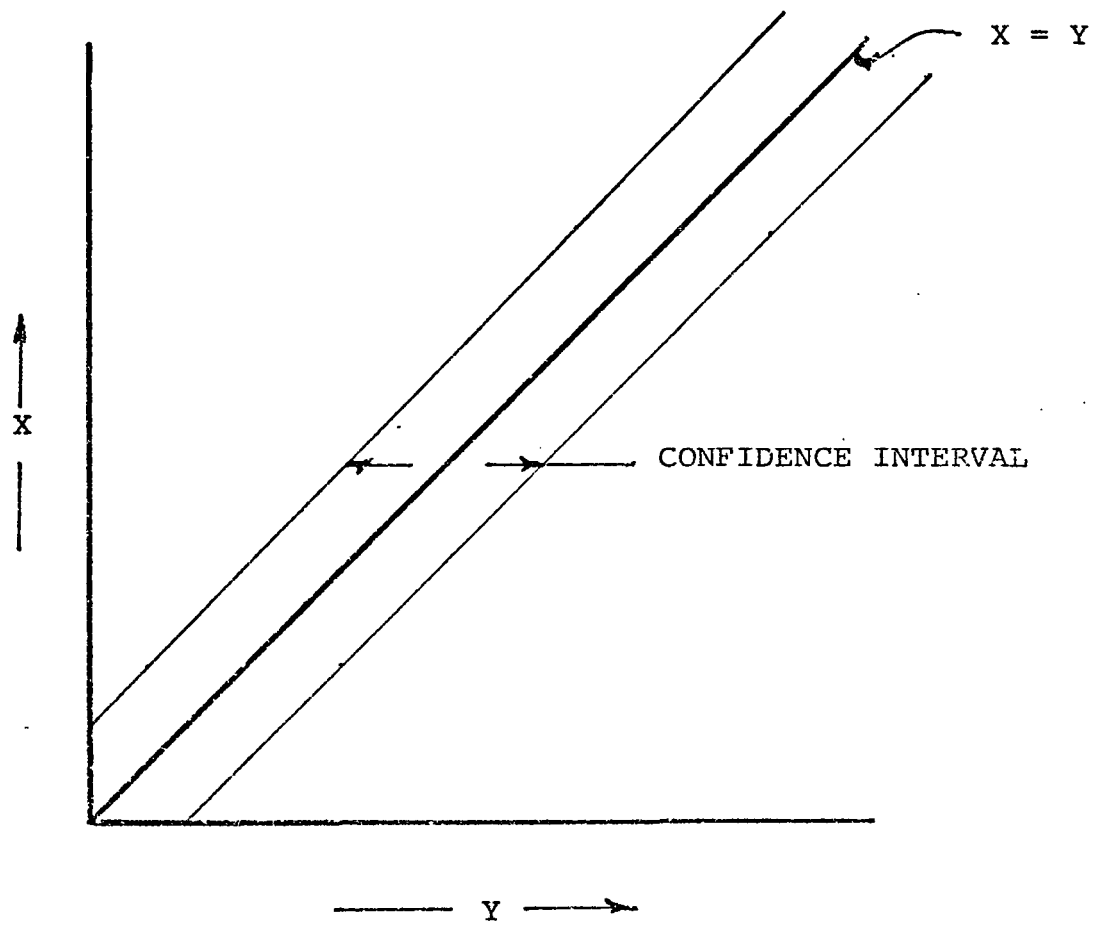
$$S_{x,y} = 68\%$$
$$2(S_{x,y}) = 95\%$$
$$3(S_{x,y}) = 99.7\%$$

Therefore, from the validation experiment results the standard error of estimate $S_{x,y}$ will be calculated by--

$$S_{x,y} = \left(\frac{\Sigma (X - X_{est.})^2}{N} \right)^{\frac{1}{2}}$$

Using this value, $S_{x,y}$, a 95% confidence interval for any value X will be given by $X \pm 2*(S_{x,y})$.

As mentioned previously in Section 3.6, the validation of a system simulator is a relatively simple process if the target system exists and is operational. If the target system is operational one can devise test runs of the system and its simulator and by comparing results the simulator can be verified and fine-tuned. For this simulator, however, the target



PLOT OF TYPICAL SIMULATION VERSUS TARGET RESULTS

FIGURE 16

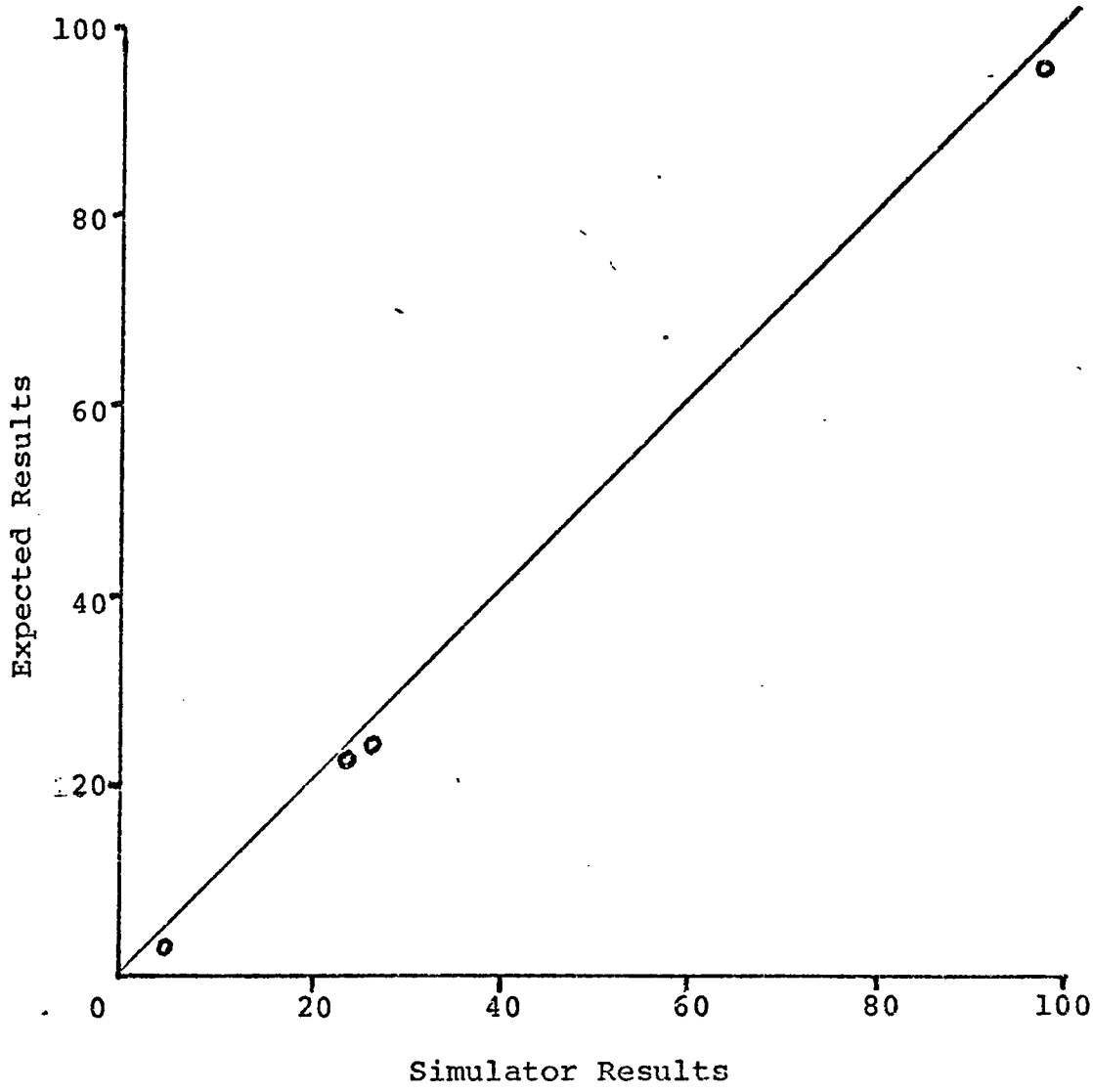
system does not exist and some other means must be found for testing the validity of the simulator.

In Section 3.3 it was stated that a simulator should be constructed with modular simulation routines which would represent the various system resources or components available in the target system. A computer system is a collection of these resources or components which perform, it is assumed, in a manner consistent with the manufacturer's specifications, and interact with each other in a known manner determined by the basic system architecture. Therefore, if the basic rules and protocol of the target system architecture are followed in the interaction of the independent simulation modules which correspond to the various system components, then a test of the simulator validity would be to make requests of these system services (read disc, write to magnetic tape, etc.) and compare the simulator's response data with the specifications provided to the simulator defining these system services. A benefit which is derived from the use of a simulation language is that statistical data is available on almost every element of the simulation. Using the last simulation run in Appendix B, the following analysis is available on the expected vs. the actual performance of the simulator.

RESOURCE	EXPECTED	ACTUAL	% differ.
FIXED-DISK	25.00 ms.	26.39 ms.	5.56%
MOVING-DISK	97.00 ms.	98.11 ms.	1.14%
MAG TAPE	24.00 ms.	24.38 ms.	1.58%
TERMINAL XFER	5.00 ms.	5.23 ms.	4.6%

From the above data it can be seen that the simulator's actual performance is following the expected performance closely. When these results are plotted and correlated, Figure 17, a very high degree of linear correlation is observed. When the linear correlation is calculated from the formula given previously, it is found to be .9995. While this shows an obvious correlation of the data, the standard error of estimate when calculated gives a value of .84. This will give a 95% confidence interval for the simulation results of 1.68. Therefore one can be confident that 95% of the simulation results fall in the range of $\bar{x} \pm 1.68$.

While the above indicates the simulator accurately simulates the specified functions of the given system resources, it only shows the operations of small portions of the simulator. In order to test how well the simulator can predict the performance of a system running a known workload, the following test was run. The second step in the validation of the simulator was to run several simulation test benchmarks of a ROLM 1602A computer system and correlate the



PERFORMANCE OF SIMULATOR SYSTEM RESOURCES

FIGURE 17

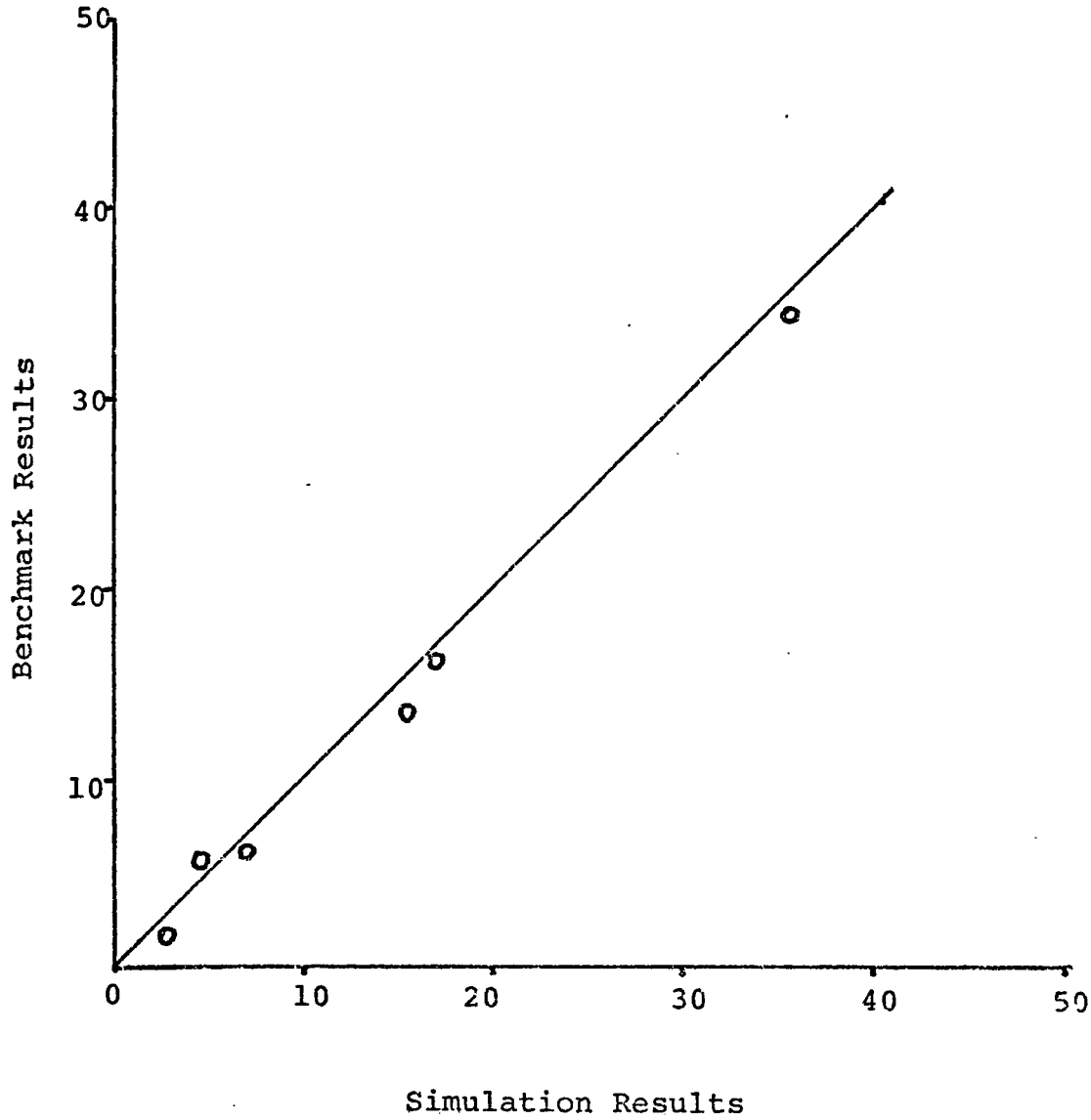
results with the actual observed performance of the ROLM system.

The ROLM system consists of a 1602A computer, a floppy disk, and a 75 ips tape transport. Three Fortran tasks were written, each utilizing the above mentioned system resources. These tasks were all run on the ROLM system; each task was timed by itself in a single-tasking environment, and in a three task multitasking environment. These benchmarks were then simulated and the results of these runs are plotted in figure 18, and given below.

ROLM/SIMULATOR TASKING BENCHMARKS

	ROLM	SIMULATION	% diff
Task 1 single tasking	2.13 ms.	2.24 ms.	5.1%
Task 2 single tasking	6.12 ms.	6.79 ms.	10.9%
Task 3 single tasking	13.43 ms.	15.04 ms.	11.9%
Task 1 multi-tasking	5.44 ms.	5.32 ms.	2.2%
Task 2 multi-tasking	16.64 ms.	16.77 ms.	0.7%
Task 3 multi-tasking	34.80 ms.	35.63 ms.	2.3%

A linear correlation calculated on these results gives a linear correlation coefficient of .9994. The standard error of estimate calculated for these results gives a value of .63. This value gives a 95% confidence interval of $\pm$ 1.26.



SIMULATION OF ROLM BENCHMARKS

FIGURE 18

The validation of the simulator in this case should give one a high degree of confidence in the ability of the simulator to provide performance data on the operation of of a specified system. While the accuracy of the simulator will vary with the target system and with the accuracy of the input specifications, there is no reason to assume that the simulator will be significantly less accurate in other similar applications. Especially since the simulator was never designed to simulate the ROLM system specifically, nor was this particular machine available when the simulator was first designed.

11.0 SIMULATOR GROWTH POTENTIAL

Few systems are designed and built for static applications with zero growth potential; therefore, a simulator designed to be easily modified in order to grow with a target system will provide the user with a greater return on his initial investment in the simulator.

The simulator described in the previous sections is an example of a simulator which, once designed and operational, is easily modified to match changes which may develop in the target system. All of the possible changes which could be made in the target system are too numerous to mention, however several possible changes are:

a) A change in a system task

b) A change in the specifications of a hardware resource

c) The addition of a new hardware device

11.1 A SOFTWARE CHANGE

In the simulator, the target system software tasks are defined using GPSS functions, which are built to represent a string of system services that the target system would require to accomplish a task. An example of one of these GPSS pseudo-process functions is given in Section 8.2. It is:

```
2     FUNCTION    P1,L10    Task #2, input P1, 10 statements
1,CYC4                      Loop 4 times for account search
2,RANDM                     Randomize above loop index
3,FHDRD                     Read account directory
4,CMP10                     Check directory for customer
5,ENDCY                     End of loop
6,MHDRD                     Read the required account record
7,CMP15                     Update the account for payment
8,OTPUT                     Acknowledge payment to terminal
9,TAPOT                     Write transaction record
10,EXIT                     End of task
```

Assume that in the above task the following changes are required:

a) It will take an average of 5 accesses of the fixed head disk to find the account directory entry.

b) To speed up operations the account records will be located on the fixed head disk.

c) The task should only allow 10 milliseconds for the update of the account for payment.

To accomplish the above changes in the simulator the following three changes are required in the GPSS pseudo-process function.

a) item 1 becomes 1,CYC5

b) item 6 becomes 6,FHDRD

c) item 7 becomes 7,CMP10

The complete updated pseudo-process then becomes:

```
 2     FUNCTION   P1,L10  Task #2,input P1, 10 statements
1,CYC5                   Loop 5 times for account search
2,RANDM                  Randomize above loop index
3,FHDRD                  Read account directory for customer
4,CMP10                  Check directory
5,ENDCY                  End of loop
6,FHDRD                  Read required account record
7,CMP10                  Update the account for payment
8,OTPUT                  Acknowledge payment to terminal
9,TAPOT                  Write transaction record
10,EXIT                  End of task
```

11.2 A CHANGE IN HARDWARE SPECIFICATIONS

In the simulator, the target system's hardware is defined by GPSS variables; if these variables are changed, the hardware definitions are also changed. In the baseline system the moving head disk is defined as having a lateral access time of 75 milliseconds, and an average rotational access time of 13 milliseconds with a sector transfer time of 7 milliseconds. Assume the original disk were replaced with a new disk having the following specifications - average lateral access time of 34 milliseconds, rotational access time of 8 milliseconds, and a sector read time of 1 millisecond. The GPSS VARIABLE statements used to define the moving head disk in the baseline simulator are:

```
LATRL VARIABLE      75
MROT  VARIABLE      13
READM VARIABLE       7
```

In order to implement the required changes these statements would be changed to read:

```
LATRL VARIABLE      34
MROT  VARIABLE       8
READM VARIABLE       1
```

These three changes are all that would be required to modify the simulator to accommodate a change in the moving head disk.

11.3 THE ADDITION OF NEW HARDWARE

Additional hardware, or system resources, in this simulator are incorporated into the simulator by the addition of a simulation routine which will depict the function of the new hardware. Assume that for the test simulator a peripheral real-time clock device is to be added to the system. This clock is read by the CPU; the data transfer takes 1 millisecond and the clock can be read by any task in the system. A routine for the test simulator to implement this clock might look like this:

```
                                1
*2      8           ..          9
CLOCK   QUEUE           CLOKQ       Wait queue for clock routine
        BUFFER                      Allow task priority alignment
        SEIZE           CPU         Acquire CPU when availiable
        SEIZE           CLOK        Acquire clock when availiable
        DEPART          CLOKQ       Leave the wait queue
        ADVANCE         CLKTIC      Tally clock read time
        RELEASE         CLOK        free the clock
        RELEASE         CPU         Free the CPU
        TRANSFER        ,FIN        Return to dispatcher
```

To have a task access the clock, the term "CLOCK" must be included in a pseudo-process function defining that task. In addition the GPSS variable CLKTIC must be defined as 1. That is all that is required to add a new system resource to the simulator.

12.0 CONCLUSIONS

Of the initial goals set for this thesis, most were met by the simulator constructed for this project and the simulation and validation experiments which were run. One of the primary goals was the construction of a structured simulator, which would be easy to implement and configure for a given target system. It has been shown that the simulator's structure is such that any change to one module of the simulator,resulting from a change in the target system, will have little if any effect on any other portion of the simulator. This modular constuction and the "pseudo-process" technique used to emulate the system workload characteristics, allow the simulator to be easily and quickly reconfigured, which is an important feature when the performance of several system configurations are to be evaluated.

The utility of the simulator in the area of system performance evaluation was demonstrated through the analysis of the simulation data on the hypothetical target dedicated demand system. The simulation experiments resulted in significant improvements in system response through the detection of a system bottleneck, which was made evident by long queue wait times in the simulation results. While system throughput was not a prime consideration in the evaluation of the target system, the system throughput was increased by 24% overall. This increase was due in part

to the evaluation of the effect of priority assignments on the overall system performance. The utility of simulation as a performance evaluation tool would seem to be self-evident from these results. Nevertheless, there are many other areas in which simulation can be applied for the solution of computer system problems, areas such as - deadlock detection, error recovery optimization, and hardware failure effect on system performance, just to mention a few.

The level of detail of the simulator was shown to be sufficient by the results of the simulation experiments. It was assumed that in dedicated demand computer systems, the performance of the peripheral devices would be the bounding factor on system performance, and that the internal functional characteristics of any one resource, most notably the CPU, would not significantly impact overall system performance. Therefore, the functional characteristics of the CPU were not considered as impacting system performance; however, it was assumed that the CPU was functionally able to accomplish the assigned tasks. The validation experiments did show that the simulator had sufficient detail to predict the performance of a computer system with a high degree of accuracy.

The one remaining problem of simulation is that it is not usually available as a resource for use by the typical applications analyst. Until the resources for simulation become as available as some of the more common programming

languages, most system evaluation will remain a mixture of manufacturer's data, trial-and-error, and guesswork. However, it is hoped that the availability and use of simulation will increase in the future to provide the applications analyst with a much needed tool for system performance forecasting.

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APPENDIX - A

Listing of the Baseline Simulator

```
BLOCK NO.   *LOC   NAME        A,B,C,D,E,F,G,H,I             COMMENTS                               CARD NO.

                   SIMULATE    ,,,,PF                                                                  1
                   REALLOCATE  BLO,400,VAR,30                                                          2
            POIS   FUNCTION    RN1,C24                 POISSON ARRIVAL DISTRIBUTION                    3
            .0,.0/.1,.104/.2,.222/.3,.355/.4,.50/.5,.6                                                 4
            .6,.915/.7,1.2/.75,1.33/.8,1.6/.84,1.83/.88,2.12                                           5
            .9,2.3/.92,2.52/.94,2.81/.95,2.99/.96,3.2/.97,3.5                                          6
            .98,3.9/.99,4.6/.995,5.3/.998,6.2/.999,7./.9997,8.                                         7
   1               GENERATE    1500,FN$POIS,,,,20PF    SYSTEM INPUT TRANSACTIONS                       8
   2               ENTER       TERMS                   ACTIVATE TERMINAL                               9
   3               ASSIGN      2,FN$DISTR,,PF          TRANSACTION TYPE DISTRIBUTION                  10
   4               ASSIGN      4,K10,,PF               INITIALIZE LOOP RETURN POINTER                 11
   5               ASSIGN      5,K15,,PF               LOOP CONTROL STACK                             12
   6               PRIORITY    FN$PRITY                ASSIGN TRANSACTION PRIORITY                    13
   7               QUEUE       INPUT                   TERMINAL INPUT WAIT QUEUE                      14
   8               BUFFER                                                                             15
   9               TRANSFER    ,TRMIN                  INITIAL TERMINAL INPUT                         16
  10        START  GATE SNF    TASKS                   TASK SPACE AVAILABLE                           17
  11               ENTER       TASKS                   STORE TASK IN MEMORY (ALLOCATE)                18
  12               ASSIGN      10,K1,,PF               IN CORE FLAG                                   19
  13               DEPART      COREQ                   EXIT CORE WAIT QUEUE                           20
  14               LEAVE       BUFFI                   EXIT INPUT BUFFER                              21
  15        NEXT   QUEUE       CPU                     CPU SERVICE QUEUE                              22
  16               SEIZE       CPU                     ENTER CPU                                      23
  17               DEPART      CPU                     EXIT QUEUE                                     24
  18               ASSIGN      1+,K1,,PF               INCREMENT OPERATION DESIGNATOR                 25
  19               ADVANCE     V$SYSCH                 SETUP TIME - SCHEDULING OVERHEAD               26
  20               RELEASE     CPU                                                                    27
  21               TRANSFER    ,FN*2                   SELECT OPERATION                               28
  22        FIN    TRANSFER    ,NEXT                                                                  29
            *****                                                                                     30
            *****                                                                                     31
            *****                                                                                     32
            *****                   TERMINAL INPUT SWAP-OUT AND DELAY ROUTINE                         33
            *****                                                                                     34
            *****                                                                                     35
            *****                                                                                     36
  23        INPUT  LEAVE       TASKS                   EXIT CORE TO AWAIT INPUT                       37
  24               ASSIGN      10,K0,,PF               OUT OF CORE FLAG                               38
  25               ADVANCE     V$THINK,V$THINK         TERMINAL USER THINK DELAY                      39
  26               QUEUE       INPUT                   TERMINAL INPUT WAIT QUEUE                      40
  27               TRANSFER    ,TRMIN                  GO TO INPUT ROUTINE                            41
            *****                                                                                     42
            *****                   TERMINATION OF PROCESS                                            43
            *****                                                                                     44
  28        EXIT   TEST E      P10,K1,TMOUT            IS TASK IN CORE?                               45
  29               LEAVE       TASKS                   TASK OVER, LEAVE CORE.                         46
  30        TMOUT  LEAVE       TERMS                   TASK ENDED RELEASE TERMINAL                    47
  31               TABULATE    TTIME                                                                  48
  32               TERMINATE   0                                                                      49
            TTIME  TABLE       M1,0,5000,25            TOTAL TURNAROUND TIME                          50
```

```
BLOCK NO.      *LOC   NAME         A,B,C,D,E,F,G,H,I              COMMENTS                          CARD NO.
                      *****                                                                          51
                      *****                                                                          52
                      *****                                                                          53
                      *****                        RANDOM OVERHEAD GENERATOR                         54
                      *****                                                                          55
                      *****                                                                          56
                      *****                                                                          57
                      20     VARIABLE    1000                          SYSTEM TIME SLICE BASE       58
                      21     FVARIABLE   V20*(V$SYCPU/100)             CPU SYSTEM OVERHEAD          59
                      22     FVARIABLE   V20*(V$SYCHN/100)             SYSTEM I/O CHANNEL OVERHEAD  60
          33                 GENERATE    V20,V20,,,60                  GENERATE RANDOM SYSTEM WORK  61
          34                 PREEMPT     CPU                                                        62
          35                 ADVANCE     V21                           OCCUPY CPU                   63
          36                 RETURN      CPU                                                        64
          37                 SEIZE       CHANA                         DISK OVERHEAD                65
          38                 SEIZE       CONTA                         OCCUPY CONTROLLER            66
          39                 SEIZE       CHANB                         DISK OVERHEAD                67
          40                 SEIZE       CONTB                         OCCUPY CONTROLLER            68
          41                 ADVANCE     V22                                                        69
          42                 RELEASE     CONTB                                                      70
          43                 RELEASE     CHANB                                                      71
          44                 RELEASE     CONTA                                                      72
          45                 RELEASE     CHANA                                                      73
          46                 TERMINATE   0                                                          74
                      *****                                                                          75
                      *****                                                                          76
                      *****                                                                          77
                      *****                        LOOP CONTRCL AND NESTING ROUTINE                  78
                      *****                                                                          79
                      *****                                                                          80
                      *****                                                                          81
          47          CYC10  ASSIGN      3+,K1,,PF                     LOOP 10 TIMES                82
          48          CYC9   ASSIGN      3+,K1,,PF                     LOOP 9 TIMES                 83
          49          CYC8   ASSIGN      3+,K1,,PF                     LOOP 8 TIMES                 84
          50          CYC7   ASSIGN      3+,K1,,PF                     LOOP 7 TIMES                 85
          51          CYC6   ASSIGN      3+,K1,,PF                     LOOP 6 TIMES                 86
          52          CYC5   ASSIGN      3+,K1,,PF                     LOOP 5 TIMES                 87
          53          CYC4   ASSIGN      3+,K1,,PF                     LOOP 4 TIMES                 88
          54          CYC3   ASSIGN      3+,K1,,PF                     LOOP 3 TIMES                 89
          55          CYC2   ASSIGN      3+,K1,,PF                     LOOP 2 TIMES                 90
          56          CYC1   ASSIGN      3+,K1,,PF                                                  91
          57                 ASSIGN      4+,K1,,PF                     POINTER TO NEST RETURN POINT 92
          58                 ASSIGN      *4,P1,,PF                     SAVE RETURN PCINT OF LOOP    93
          59                 ASSIGN      5+,K1,,PF                     INCREMENT STACK POINTER      94
          60                 ASSIGN      *5,P3,,PF                     STACK CYCLE COUNTER FOR LOOP 95
          61                 ASSIGN      3,K0,,PF                      CLEAR CYCLE COUNTER          96
          62                 TRANSFER    ,FIN                                                       97
          63          ENDCY  ASSIGN      7,P*5,,PF                     GET LOOP COUNTER             98
          64                 LOOP        7,AGAIN                       LOOP CONTROL                 99
          65                 ASSIGN      4-,K1,,PF                     UNSTACK RETURN LOCATION      100
```

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BLOCK NO.      *LOC   NAME        A,B,C,D,E,F,G,H,I              COMMENTS                                  CARD NO.
    66                ASSIGN      5-,K1,,PF                     UNSTACK CYCLE COUNTER                       101
    67                TRANSFER    ,FIN                                                                      102
    68                AGAIN ASSIGN 1,P*4,,PF                    RETRIEVE LOOP START LOCATION                103
    69                ASSIGN      *5,P7,,PF                     RETURN NEW DECREMENTED LOOP INDEX           104
    70                ASSIGN      7,K0,,PF                      CLEAR TO ZERO                               105
    71                TRANSFER    ,FIN                          RESTART LOOP                                106
                      *****                                                                                 107
                      *****                                                                                 108
                      *****                                                                                 109
                      *****                         ROUTINE RANDOMIZED PRECEEDING LOOP INDEX                110
                      *****                                                                                 111
                      *****                                                                                 112
                      *****                                                                                 113
    72                RANDM ASSIGN    7,P*5,,PF                 ASSIGN LOOP INDEX TO PARAMETER 7            114
    73                ASSIGN      *5,V$RAND,,PF                 REASSIGN RANDOMIZED LOOP INDEX              115
    74                ASSIGN      *4+,K1,,PF                    EXCLUDE RANDM FROM LOOPING                  116
    75                TRANSFER    ,FIN                          CONTINUE PROCESSING                         117
                      RAND  VARIABLE (RN3*(2*P7))/1000+1        RANDOMIZE PARAMETER 7                       118
                      *****                                                                                 119
                      *****                                                                                 120
                      *****                                                                                 121
                      *****                         COMPUTATION ROUTINE                                     122
                      *****                                                                                 123
                      *****                                                                                 124
                      *****                                                                                 125
    76                CMP95 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               126
    77                CMP90 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               127
    78                CMP85 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               128
    79                CMP80 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               129
    80                CMP75 ASSIGN    6+,K5 ,,PF                COMPUTE TIME INCREMENT IN MS.               130
    81                CMP70 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               131
    82                CMP65 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               132
    83                CMP60 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               133
    84                CMP55 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               134
    85                CMP50 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               135
    86                CMP45 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               136
    87                CMP40 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               137
    88                CMP35 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               138
    89                CMP30 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               139
    90                CMP25 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               140
    91                CMP20 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               141
    92                CMP15 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               142
    93                CMP10 ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               143
    94                CMP5  ASSIGN    6+,K5,,PF                 COMPUTE TIME INCREMENT IN MS.               144
    95                RECMP TEST.LE   P6,V$SLICE,SLICE          IS CPU TIME LESS THAN SLICE?                145
    96                BUFFER                                                                                146
    97                QUEUE       CPU                                                                       147
    98                SEIZE       CPU                           BEGIN PROCESSING                            148
    99                DEPART      CPU                                                                       149
   100                ADVANCE     P6                                                                        150
```

BLOCK NO.	*LOC	NAME	A,B,C,D,E,F,G,H,I	COMMENTS	CARD NO.
101		RELEASE	CPU		151
102		ASSIGN	6,K0,,PF	CLEAR PARAMETER TO 0	152
103		TRANSFER	,FIN	END PROCESSING	153
104	SLICE	ASSIGN	6-,V$SLICE,,PF	REDUCE CPU TIME BY SLICE SIZE	154
105		BUFFER			155
106		QUEUE	CPU		156
107		SEIZE	CPU	BEGIN PROCESSING	157
108		DEPART	CPU		158
109		ADVANCE	V$SLICE	PROCESS FOR ONE TIME-SLICE	159
110		RELEASE	CPU		160
111		TRANSFER	,RECMP	RETURN FOR FURTHER PROCESSING	161
	*****				162
	*****				163
	*****				164
	*****				165
	*****		TERMINAL I/O ROUTINE		166
	*****				167
	*****				168
	*****				169
112	TRMIN	BUFFER			170
113		TEST E	V$MUXCH,K1,CPUIN	CHAN OR CPU I/O	171
114		GATE SNF	BUFFI	TERMINAL I/O SATURATED	172
115		ENTER	BUFFI	ACQUIRE INPUT BLOCK	173
116		SEIZE	MUXCH	SEIZE TERMINAL MUX CHANNEL	174
117		SEIZE	TMCON	SEIZE CONTROLLER	175
118		PREEMPT	CPU	GET BUFFER	176
119		DEPART	INPUT	EXIT INPUT QUEUE	177
120		ADVANCE	K2		178
121		RETURN	CPU		179
122		ASSIGN	8,V$WORDI,,PF	NUMBER OF WORDS IN MESSAGE	180
123	TRWD	ADVANCE	V$WDTRN	PASS ONE WORD	181
124		LOOP	8,NXT	READ ANOTHER WORD?	182
125		QUEUE	COREQ	WAIT FOR CORE SPACE	183
126		MARK	9PF	MARK FOR THE RESPONSE MEASURE	184
127		PREEMPT	CPU	NOTIFY CPU OF I/O	185
128		RELEASE	TMCON		186
129		RELEASE	MUXCH		187
130		ADVANCE	K2		188
131		RETURN	CPU		189
132		TRANSFER	,START		190
133	NXT	RELEASE	TMCON	RELEASE CONTROLLER	191
134		RELEASE	MUXCH	RELEASE CHANNEL	192
135		ADVANCE	V$TYPE	MANUAL TYPE DELAY	193
136		SEIZE	MUXCH	SEIZE CHANNEL	194
137		SEIZE	TMCON	SEIZE CONTROLLER	195
138		TRANSFER	,TRWD		196
139	CPUIN	SEIZE	TMCON	SEIZE CONTROLLER	197
140		GATE SNF	BUFFI	TERMINAL I/O SATURATED	198
141		ENTER	BUFFI	ACQUIRE INPUT BLOCK	199
142		PREEMPT	CPU	GET BUFFER	200

BLOCK NO.	*LOC	NAME	A,B,C,D,E,F,G,H,I	COMMENTS	CARD NO.
143		DEPART	INPUT	DEPART INPUT QUEUE	201
144		ADVANCE	K2		202
145		RETURN	CPU		203
146		ASSIGN	8,V$WORDI,,PF	NUMBER OF WORDS IN MESSAGE	204
147	RDWD	PREEMPT	CPU	INTERRUPT	205
148		ADVANCE	V$CPUTM	READ ONE WORD	206
149		RETURN	CPU		207
150		LOOP	8,NXTIN	READ ANOTHER WORD?	208
151		QUEUE	COREQ	WAIT FOR CORE SPACE	209
152		MARK	9PF	MARK FOR THE RESPONSE MEASURE	210
153		RELEASE	TMCON		211
154		TRANSFER	,START		212
155	NXTIN	RELEASE	TMCON	RELEASE CONTROLLER	213
156		ADVANCE	V$TYPE	MANUAL TYPE DELAY	214
157		SEIZE	TMCON	SEIZE CONTROLLER	215
158		TRANSFER	,RDWD		216
	*****				217
	*****				218
	*****				219
	*****		TERMINAL OUTPUT ROUTINE		220
	*****				221
	*****				222
	*****				223
	*****				224
159	OTPUT	BUFFER			225
	RESPN	TABLE	MP9,0,500,50	RESPONSE TABLE DEFINITION	226
	TRATE	VARIABLE	1000/(V$BAUD/V$WDSIZ)	MINIMAL TERMINAL WORD TRANS INTERVAL	227
160		TEST E	V$MUXCH,K1,CPUOT	CHAN OR CPU I/O	228
161		QUEUE	OTPUT	TERMINAL OUTPUT QUEUE	229
162		GATE SNF	BUFFO	TERMINAL I/O SATURATED	230
163		ENTER	BUFFO	ACQUIRE INPUT BLOCK	231
164		SEIZE	CPU	SETUP OUTPUT BUFFER	232
165		SEIZE	MUXCH	SEIZE TERMINAL MUX CHANNEL	233
166		SEIZE	TMCON	SEIZE CONTROLLER	234
167		DEPART	OTPUT		235
168		ADVANCE	K5		236
169		RELEASE	CPU		237
170		ASSIGN	8,V$WORDO,,PF	NUMBER OF WORDS IN MESSAGE	238
171	WDOUT	ADVANCE	V$WDTRN	PASS ONE WORD	239
172		LOOP	8,NXTO	READ ANOTHER WORD?	240
173		PREEMPT	CPU	NOTIFY CPU OF I/O	241
174		RELEASE	TMCON		242
175		RELEASE	MUXCH		243
176		ADVANCE	K2		244
177		RETURN	CPU		245
178		TEST NE	P9,K0,SKTAB	TEST FOR MARKED TIME	246
179		TABULATE	RESPN	TABULATE RESPONSE	247
180		ASSIGN	9,K0,,PF	ZERO THE MARK TIME	248
181	SKTAB	LEAVE	BUFFO	EXIT OUTPUT BUFFER	249
182		TRANSFER	,FIN		250
183	NXTO	RELEASE	TMCON	RELEASE CONTROLLER	

BLOCK NO.	*LOC	NAME	A,B,C,D,E,F,G,H,I	COMMENTS	CARD NO.
184		RELEASE	MUXCH	RELEASE CHANNEL	251
185		ADVANCE	V$TRATE	SYNCHRONIZING DELAY	252
186		SEIZE	MUXCH	SEIZE CHANNEL	253
187		SEIZE	TMCON	SEIZE CONTROLLER	254
188		TRANSFER	,WDOUT	NEXT WORD	255
189	CPUOT	QUEUE	OTPUT	TERMINAL OUTPUT QUEUE	256
190		GATE SNF	BUFFO	WAIT FOR EMPTY BUFFER	257
191		ENTER	BUFFO		258
192		SEIZE	CPU	SEIZE CPU FOR OUTPUT	259
193		SEIZE	TMCON	SEIZE CONTROLLER	260
194		DEPART	OTPUT		261
195		ADVANCE	K5	SETUP OUTPUT	262
196		ASSIGN	8,V$WORDO,,PF	NUMBER OF WORDS IN MESSAGE	263
197		ADVANCE	V$CPUTM	TRANSMIT FIRST WORD	264
198		ASSIGN	8-,K1,,PF	DECREMENT COUNT	265
199		RELEASE	CPU		266
200		RELEASE	TMCON		267
201		ADVANCE	V$TRATE	SYNCHRONIZING DELAY	268
202	WDOT	SEIZE	TMCON	TERMINAL SEIZES CONTROLLER	269
203		PREEMPT	CPU	INTERRUPT CPU	270
204		ADVANCE	V$CPUTM	TRANSMIT WORD	271
205		RETURN	CPU		272
206		RELEASE	TMCON		273
207		LOOP	8,NXTOT	SEND NEXT WORD	274
208		TEST NE	P9,K0,NOTAB	TEST FOR MARKED TIME	275
209		TABULATE	RESPN	TABULATE RESPONSE	276
210		ASSIGN	9,K0,,PF	ZERO THE MARK TIME	277
211	NOTAB	LEAVE	BUFFO	EXIT OUTPUT BUFFER	278
212		TRANSFER	,FIN	EXIT ROUTINE	279
213	NXTOT	ADVANCE	V$TRATE	SYNCHRONIZING DELAY	280
214		TRANSFER	,WDOT	SEND NEXT WORD	281
	*****				282
	*****				283
	*****				284
	*****		FIXED HEAD DISK READ ROUTINE		285
	*****				286
	*****				287
	*****				288
215	FHDRD	QUEUE	FHDRD	DISK WAIT QUEUE	289
216		BUFFER			290
217		TEST E	V$CHANA,K1,CPUFR	SELECT CHANNEL OR CPU MODE	291
218		SEIZE	CHANA	SEIZE CHANNEL AND CONTROLLER	292
219		SEIZE	CONTA	SEIZE CONTROLLER	293
220		DEPART	FHDRD		294
221		ADVANCE	V$FROT,V$FROT		295
222		ADVANCE	V$READF	FIXED HEAD READ TIME	296
223		PREEMPT	CPU	NOTIFY CPU OF TRANSFER	297
224		ADVANCE	K2		298
225		RETURN	CPU		299
226		RELEASE	CONTA	CONTROLLER	300

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BLOCK NO.      *LOC   NAME       A,B,C,D,E,F,G,H,I          COMMENTS                                  CARD NO.
    227                RELEASE    CHANA                     EXIT CHANNEL                                301
    228                TRANSFER   ,FIN                                                                   302
    229          CPUFR SEIZE      CONTA                     CONTROLLER                                  303
    230                DEPART     FHDRD                                                                 304
    231                GATE LR    CPUIO                     CPU I/O INTERFERENCE SEMAPHORE              305
    232                LOGIC S    CPUIO                     SET CPU I/O SEMAPHORE                       306
    233                ADVANCE    V$FROT,V$FROT                                                         307
    234                PREEMPT    CPU                       INTERRUPT CPU                               308
    235                ADVANCE    V$READF                   FIXED HEAD READ TIME                        309
    236                LOGIC R    CPUIO                     RESET CPU I/O SEMAPHORE                     310
    237                RETURN     CPU                       COMPLETE INTERRUPT                          311
    238                RELEASE    CONTA                     EXIT CONTROLLER                             312
    239                TRANSFER   ,FIN                      EXIT                                        313
                  *****                                                                                  314
                  *****                                                                                  315
                  *****                                                                                  316
                  *****                MOVING HEAD DISK READ ROUTINE                                     317
                  *****                                                                                  318
                  *****                                                                                  319
                  *****                                                                                  320
    240          MHDRD QUEUE      MHDRD                     DISK WAIT QUEUE                             321
    241                BUFFER                                                                            322
    242                TEST E     V$CHANB,K1,CPUMR          SELECT CHANNEL OR CPU MODE                  323
    243                SEIZE      CHANB                     SEIZE CHANNEL AND CONTROLLER                324
    244                SEIZE      CONTB                     SEIZE CONTROLLER                            325
    245                DEPART     MHDRD                                                                 326
    246                ADVANCE    V$LATRL,V$LATRL           POSITION HEAD ON TRACK                      327
    247                ADVANCE    V$MROT,V$MROT             ROTATIONAL ACCESS                           328
    248                ADVANCE    V$READM                   MOVING HEAD DISK READ                       329
    249                PREEMPT    CPU                       NOTIFY CPU OF TRANSFER                      330
    250                ADVANCE    K2                                                                    331
    251                RETURN     CPU                                                                   332
    252                RELEASE    CONTB                     CONTROLLER                                  333
    253                RELEASE    CHANB                     EXIT CHANNEL                                334
    254                TRANSFER   ,FIN                                                                   335
    255          CPUMR SEIZE      CONTB                     CONTROLLER                                  336
    256                DEPART     MHDRD                                                                 337
    257                ADVANCE    V$LATRL,V$LATRL           POSITION HEAD ON TRACK                      338
    258                GATE LR    CPUIO                     CPU I/O INTERFERENCE SEMAPHORE              339
    259                LOGIC S    CPUIO                     SET CPU I/O SEMAPHORE                       340
    260                ADVANCE    V$MROT,V$MROT             ROTATIONAL ACCESS                           341
    261                PREEMPT    CPU                       INTERRUPT CPU                               342
    262                ADVANCE    V$READM                   MOVING HEAD DISK READ                       343
    263                LOGIC R    CPUIO                     RESET CPU I/O SEMAPHORE                     344
    264                RETURN     CPU                       COMPLETE INTERRUPT                          345
    265                RELEASE    CONTB                     EXIT CONTROLLER                             346
    266                TRANSFER   ,FIN                      EXIT                                        347
                  *****                                                                                  348
                  *****                                                                                  349
                  *****                                                                                  350
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BLOCK NO.    *LOC   NAME      A,B,C,D,E,F,G,H,I          COMMENTS                              CARD NO.
                    *****                    FIXED HEAD WRITE ROUTINE                          351
                    *****                                                                      352
                    *****                                                                      353
                    *****                                                                      354
       267          FHDWR  QUEUE     FHDWR                DISK WAIT QUEUE                      355
       268                 BUFFER                                                              356
       269                 TEST E   V$CHANA,K1,CPUFW     SELECT CHANNEL OR CPU MODE           357
       270                 SEIZE    CHANA                SEIZE CHANNEL AND CONTROLLER         358
       271                 SEIZE    CONTA                SEIZE CONTROLLER                     359
       272                 DEPART   FHDWR                                                     360
       273                 ADVANCE  V$FROT,V$FROT                                             361
       274                 ADVANCE  V$READF              FIXED HEAD WRITE                     362
       275                 PREEMPT  CPU                  NOTIFY CPU OF TRANSFER               363
       276                 ADVANCE  K2                                                        364
       277                 RETURN   CPU                                                       365
       278                 RELEASE  CONTA                CONTROLLER                           366
       279                 RELEASE  CHANA                EXIT CHANNEL                         367
       280                 TRANSFER ,FIN                                                      368
       281          CPUFW  SEIZE    CONTA                CONTROLLER                           369
       282                 DEPART   FHDWR                                                     370
       283                 GATE LR  CPUIO                CPU I/O INTERFERENCE SEMAPHORE       371
       284                 LOGIC S  CPUIO                SET CPU I/O SEMAPHORE                372
       285                 ADVANCE  V$FROT,V$FROT                                             373
       286                 PREEMPT  CPU                  INTERRUPT CPU                        374
       287                 ADVANCE  V$READF              FIXED HEAD WRITE                     375
       288                 LOGIC R  CPUIO                RESET CPU I/O SEMAPHORE              376
       289                 RETURN   CPU                  COMPLETE INTERRUPT                   377
       290                 RELEASE  CONTA                EXIT CONTROLLER                      378
       291                 TRANSFER ,FIN                 EXIT                                 379
                    *****                                                                      380
                    *****                                                                      381
                    *****                                                                      382
                    *****                    MOVING HEAD DISK WRITE ROUTINE                    383
                    *****                                                                      384
                    *****                                                                      385
                    *****                                                                      386
       292          MHDWR  QUEUE     MHDWR                DISK WAIT QUEUE                      387
       293                 BUFFER                                                              388
       294                 TEST E   V$CHANB,K1,CPUMW     SELECT CHANNEL OR CPU MODE           389
       295                 SEIZE    CHANB                SEIZE CHANNEL AND CONTROLLER         390
       296                 SEIZE    CONTB                SEIZE CONTROLLER                     391
       297                 DEPART   MHDWR                                                     392
       298                 ADVANCE  V$LATRL,V$LATRL      POSITION HEAD ON TRACK               393
       299                 ADVANCE  V$MROT,V$MROT        ROTATIONAL ACCESS                    394
       300                 ADVANCE  V$READM              MOVING HEAD DISK WRITE               395
       301                 PREEMPT  CPU                  NOTIFY CPU OF TRANSFER               396
       302                 ADVANCE  K2                                                        397
       303                 RETURN   CPU                                                       398
       304                 RELEASE  CONTB                CONTROLLER                           399
       305                 RELEASE  CHANB                EXIT CHANNEL                         400
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BLOCK NO.      *LOC   NAME       A,B,C,D,E,F,G,H,I          COMMENTS                          CARD NO.

       306            TRANSFER   ,FIN                                                          401
       307    CPUMW   SEIZE      CONTB                      CONTROLLER                         402
       308            DEPART     MHDWR                                                         403
       309            ADVANCE    V$LATRL,V$LATRL            POSITION HEAD ON TRACK             404
       310            GATE LR    CPUIO                      CPU I/O INTERFERENCE SEMAPHORE     405
       311            LOGIC S    CPUIO                      SET CPU I/O SEMAPHORE              406
       312            ADVANCE    V$MROT,V$MROT              ROTATIONAL ACCESS                  407
       313            PREEMPT    CPU                        INTERRUPT CPU                      408
       314            ADVANCE    V$READM                    MOVING HEAD DISK WRITE             409
       315            LOGIC R    CPUIO                      RESET CPU I/O SEMAPHORE            410
       316            RETURN     CPU                        COMPLETE INTERRUPT                 411
       317            RELEASE    CONTB                      EXIT CONTROLLER                    412
       318            TRANSFER   ,FIN                       EXIT                               413
                 *****                                                                         414
                 *****                                                                         415
                 *****                                                                         416
                 *****                  INPUT FROM TAPE ROUTINE                                417
                 *****                                                                         418
                 *****                                                                         419
                 *****                                                                         420
       319    TAPIN   QUEUE      TAPIN                      ENTER QUEUE                        421
       320            BUFFER                                                                   422
       321            TEST E     V$CHANC,K1,CPUTI           CPU OR CHANNEL I/O?                423
       322            SEIZE      CHANC                      SEIZE IO CHANNEL                   424
       323            SEIZE      TAPCN                      SEIZE TAPE CONTROLLER              425
       324            DEPART     TAPIN                                                         426
       325            ADVANCE    V$TPACC                    ACCESS WAIT                        427
       326            ADVANCE    V$RDTAP                    READ TIME ONE BLOCK                428
       327            PREEMPT    CPU                                                           429
       328            ADVANCE    K2                         NOTIFY CPU OF IO                   430
       329            RETURN     CPU                                                           431
       330            RELEASE    TAPCN                                                         432
       331            RELEASE    CHANC                                                         433
       332            TRANSFER   ,FIN                                                          434
       333    CPUTI   SEIZE      CPU                        INITIALIZE INPUT                   435
       334            ADVANCE    K2                                                            436
       335            SEIZE      TAPCN                      SEIZE CONTROLLER                   437
       336            DEPART     TAPIN                                                         438
       337            RELEASE    CPU                                                           439
       338            GATE LR    CPUIO                      CPU I/O INTERFERENCE SEMAPHORE     440
       339            LOGIC S    CPUIO                      SET CPU I/O SEMAPHORE              441
       340            ADVANCE    V$TPACC                    ACCESS TAPE                        442
       341            PREEMPT    CPU                        INTERRUPT CPU FOR INPUT            443
       342            ADVANCE    V$RDTAP                    READ TAPE RECORD                   444
       343            LOGIC R    CPUIO                      RESET CPU I/O SEMAPHORE            445
       344            RELEASE    TAPCN                                                         446
       345            RETURN     CPU                                                           447
       346            TRANSFER   ,FIN                       EXIT                               448
                 *****                                                                         449
                 *****                                                                         450
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BLOCK NO.    *LOC   NAME       A,B,C,D,E,F,G,H,I          COMMENTS                                  CARD NO.
                    *****
                    *****                          OUTPUT TO TAPE ROUTINE                          451
                    *****                                                                          452
                    *****                                                                          453
                    *****                                                                          454
                    *****                                                                          455
      347           TAPOT  QUEUE      TAPOT                      ENTER QUEUE                       456
      348                  BUFFER                                                                   457
      349                  TEST E     V$CHANC,K1,CPUTO          CPU OR CHANNEL I/O?               458
      350                  SEIZE      CHANC                     SEIZE IO CHANNEL                  459
      351                  SEIZE      TAPCN                     SEIZE TAPE CONTROLLER             460
      352                  DEPART     TAPOT                                                       461
      353                  ADVANCE    V$TPACC                   ACCESS WAIT                       462
      354                  ADVANCE    V$RDTAP                   READ TIME ONE RECORD              463
      355                  PREEMPT    CPU                                                         464
      356                  ADVANCE    K2                        NOTIFY CPU OF IO                  465
      357                  RETURN     CPU                                                         466
      358                  RELEASE    TAPCN                                                       467
      359                  RELEASE    CHANC                                                       468
      360                  TRANSFER   ,FIN                                                        469
      361           CPUTO  SEIZE      CPU                       INITIALIZE OUTPUT                 470
      362                  ADVANCE    K2                                                          471
      363                  SEIZE      TAPCN                     SEIZE CONTROLLER                  472
      364                  DEPART     TAPOT                                                       473
      365                  RELEASE    CPU                                                         474
      366                  GATE LR    CPUIO                     CPU I/O INTERFERENCE SEMAPHORE    475
      367                  LOGIC S    CPUIO                     SET CPU I/O SEMAPHORE             476
      368                  ADVANCE    V$TPACC                   ACCESS TAPE                       477
      369                  PREEMPT    CPU                       INTERRUPT CPU FOR OUTPUT          478
      370                  ADVANCE    V$RDTAP                   WRITE ONE BLOCK                   479
      371                  LOGIC R    CPUIO                     RESET CPU I/O SEMAPHORE           480
      372                  RELEASE    TAPCN                                                       481
      373                  RETURN     CPU                                                         482
      374                  TRANSFER   ,FIN                      EXIT                              483
                    ********************  SYSTEM AND SIMULATION PARAMETERS FOLLOW  ********************  484
                    ********************  ALL TIMES ARE EXPRESSED IN MILLISECONDS  ************       485
                    *****                                                                          486
                    *****                          CPU AND CORE DEFINITIONS                        487
                    *****                                                                          488
                    WDSIZ  VARIABLE   16                        WORD SIZE IN BITS                 489
                           STORAGE    S$TASKS,5                 MAXIMUM TASK CAPACITY OF CORE     490
                           STORAGE    S$BUFFI,15                NUMBER OF INPUT BUFFERS           491
                           STORAGE    S$BUFFO,5                 TERMINAL OUTPUT BUFFERS AVAILIABLE 492
                    SLICE  VARIABLE   25                        MS. COMPUTATION TIME-SLICE        493
                    SYCPU  VARIABLE   5                         CPU SYSTEM OVERHEAD PERCENTAGE    494
                    SYCHN  VARIABLE   5                         CHANNEL SYSTEM OVERHEAD PERCENTAGE 495
                    SYSCH  VARIABLE   5                         TASK SWITCHING OVERHEAD           496
                    *****                                                                          497
                    *****                          USER PROCESSING DEFINITIONS                     498
                    *****                                                                          499
                    DISTR  FUNCTION   RN2,D4                    TRANSACTION DISTRUBUTION          500
```

```
BLOCK NO.      *LOC   NAME        A,B,C,D,E,F,G,H,I          COMMENTS                                        CARD NO.
               .15,1/.40,2/.65,3/.9,4                        1=30%,2=20%,3=30%,4=20%                          501
               PRITY  FUNCTION    P2,L4                      TRANSACTION PRIORITY ASSIGNMENT                  502
               1,1/2,1/3,1/4,1                                                                               503
               1      FUNCTION    P1,L23     TRANS #1 CREDIT PURCHASE TRANSACTION                           504
               1,CYC4                        LOOP FOR CREDIT SEARCH                                         505
               2,RANDM                       RANDOMIZE SEARCH                                               506
               3,FHDRD                       READ CREDIT DIRECTORY                                          507
               4,CMP10                       CHECK DIRECTORY                                                508
               5,ENDCY                       END OF LOOP                                                    509
               6,MHDRD                       READ ACCOUNT                                                   510
               7,OTPUT                       OUTPUT TO TERMINAL FOR CREDIT OK                               511
               8,CYC5                        REGISTER PURCHASES                                             512
               9,RANDM                       RANDOMIZE PURCHASES                                            513
               10,FHDWR                      SWAP OUT TO SCRATCH FOR INPUT WAIT                             514
               11,INPUT                      RECEIVE FIRST PURCHASE                                         515
               12,FHDRD                      READ FROM SCRATCH                                              516
               13,CMP5                       LOCATE INVENTORY RECORD                                        517
               14,MHDRD                      READ INVENTORY RECORD                                          518
               15,CMP10                      TALLY PURCHASE                                                 519
               16,OTPUT                      ACKNOWLEDGE TALLY AND PURCHASE                                 520
               17,ENDCY                      END OF LOOP                                                    521
               18,CMP25                      TOTAL AND SET UP OUTPUT                                        522
               19,OTPUT                      SUBTOTAL                                                       523
               20,OTPUT                      TAX                                                            524
               21,OTPUT                      TOTAL                                                          525
               22,TAPOT                      OUTPUT TRANSACTION RECORD                                      526
               23,EXIT                       END OF PROCESS                                                 527
               2      FUNCTION    P1,L10     TRANS #2 PAYMENT ON ACCOUNT TRANSACTION                        528
               1,CYC4                        LOOP FOR ACCOUNT SEARCH                                        529
               2,RANDM                       RANDOMIZE SEARCH LENGTH                                        530
               3,FHDRD                       READ ACCOUNT DIRECTORY                                         531
               4,CMP10                       CHECK DIRECTORY                                                532
               5,ENDCY                       END OF LOOP                                                    533
               6,MHDRD                       READ ACCOUNT                                                   534
               7,CMP25                       TALLY PAYMENT                                                  535
               8,OTPUT                       ACKNOWLEDGE PAYMENT TO TERMINAL                                536
               9,TAPOT                       WRITE TRANSACTION RECORD                                       537
               10,EXIT                       END OF PROCESS                                                 538
               3      FUNCTION    P1,L18     TRANS #3 CASH PURCHASES TRANSACTION                            539
               1,OTPUT                       ACKNOWLEDGE READY FOR PURCHASES                                540
               2,CYC5                        REGISTER MEAN OF 5 PURCHASES                                   541
               3,RANDM                       RANDOMIZE PURCHASES                                            542
               4,CMP15                       SET-UP RECORD                                                  543
               5,FHDWR                       SWAP OUT TO SCRATCH FOR INPUT WAIT                             544
               6,INPUT                       INPUT PURCHASE                                                 545
               7,FHDRD                       READ BACK FROM SCRATCH                                         546
               8,CMP5                        LOCATE INVENTORY RECORD                                        547
               9,MHDRD                       READ INVENTORY RECORD                                          548
               10,CMP25                      TALLY PURCHASE                                                 549
               11,OTPUT                      ACKNOWLEDGE AND TALLY PURCHASE                                 550
```

```
BLOCK NO.      *LOC    NAME        A,B,C,D,E,F,G,H,I          COMMENTS                                        CARD NO.
                       12,ENDCY                               END OF LOOP                                       551
                       13,CMP25                               TOTAL AND PREPARE OUTPUT                          552
                       14,OTPUT                               SUBTOTAL                                          553
                       15,OTPUT                               TAX                                               554
                       16,OTPUT                               TOTAL                                             555
                       17,TAPOT                               OUTPUT TRANSACTION RECORD                         556
                       18,EXIT                                END OF PROCESS                                    557
                       4       FUNCTION    P1,L6              TRANS #4 RECEIVING INVENTORY UPDATE               558
                       1,CMP5                                 LOCATE INVENTORY RECORD                           559
                       2,MHDRD                                READ INVENTORY RECORD                             560
                       3,CMP25                                UPDATE INVENTORY RECORD                           561
                       4,TAPOT                                CREATE TRANSACTION RECORD                         562
                       5,OTPUT                                RESPOND TO TERMINAL                               563
                       6,EXIT                                 END OF PROCESS                                    564
                       *****                                                                                    565
                       *****                                  DISK/DRUM STORAGE DEFINITIONS                     566
                       *****                                                                                    567
                       CHANA   VARIABLE    1                          CHANNEL = 1, CPU = 0                      568
                       CHANB   VARIABLE    1                          CHANNEL = 1, CPU = 0                      569
                       LATRL   VARIABLE    75                         POSITION HEAD LATERALLY                   570
                       MROT    VARIABLE    13                         MOVING HEAD DISK ROTATIONAL ACCESS        571
                       READM   VARIABLE    7                          MOVING HEAD DISK READ/WRITE TIME          572
                       FROT    VARIABLE    16                         FIXED DISK ROTATIONAL ACCESS              573
                       READF   VARIABLE    7                          FIXED HEAD DISK READ/WRITE TIME           574
                       *****                                                                                    575
                       *****                                  TERMINAL OPERATIONS DEFINITIONS                   576
                       *****                                                                                    577
                       MUXCH   VARIABLE    1                          CHANNEL = 1, CPU = 0                      578
                       BAUD    VARIABLE    1200                       TERMINAL TRANSMISSION RATE                579
                       TYPE    VARIABLE    1000                       TIME REQUIRED TO TYPE ONE WORD            580
                       THINK   VARIABLE    2500                       TERMINAL USER THINK TIME                  581
                       CPUTM   VARIABLE    1                          CPU SPEDD/CHAR                            582
                       WDTRN   VARIABLE    5                          MS. TO TRANSFER ONE WORD                  583
                               STORAGE     S$TERMS,100                                                          584
                       WORDI   VARIABLE    10                 AVERAGE NUMBER OF WORDS INPUT                     585
                       WORDO   VARIABLE    5                  AVERAGE NUMBER OF WORDS OUTPUT                    586
                       *****                                                                                    587
                       *****                                  TAPE I/O DEFINITIONS                              588
                       *****                                                                                    589
                       CHANC   VARIABLE    1                  CHANNEL = 1, CPU = 0                              590
                       TPACC   VARIABLE    10                         MS. TO ACCESS TAPE RECORD                 591
                       RDTAP   VARIABLE    12                         MS. TO READ ONE TAPE RECORD               592
                       ****************************       RUN PARAMETERS FOR GPSS  ********************         593
375                            GENERATE    60000                      ONE MINUTE TIMER                          594
376                            TERMINATE   1                                                                       595
                               START       2,NP                       INITIALIZE THE SIMULATOR                  596
                               RESET                                                                            597
                               START       5,,,1                                                                598
                               RESET                                                                            599
                               START       5,,,1                                                                600
```

```
      BLOCK NO.      *LOC   NAME       A,B,C,D,E,F,G,H,I            COMMENTS                    CARD NO.

                            RESET                                                                 601
                            START      5,,,1                                                      602
                            RESET                                                                 603
                            START      5,,,1                                                      604
                            STORAGE    S$BUFFI,25          NUMBER OF INPUT BUFFERS                605
                            CLEAR                                                                 606
                            START      2,NP                INITIALIZE THE SIMULATOR               607
                            RESET                                                                 608
                            START      5,,,1                                                      609
                            RESET                                                                 610
                            START      5,,,1                                                      611
                            RESET                                                                 612
                            START      5,,,1                                                      613
                            RESET                                                                 614
                            START      5,,,1                                                      615
                     PRITY  FUNCTION   P2,L4                                                      616
ERROR IN ABOVE CARD * * * * * MULTIPLE DEFINED ENTITY SYMBOL (NON-FATAL)       <<<<<

                     1,4/2,2/3,3/4,1                       LONG JOB BENEFIT                       617
                            CLEAR                                                                 618
                            START      2,NP                INITIALIZE THE SIMULATOR               619
                            RESET                                                                 620
                            START      5,,,1                                                      621
                            RESET                                                                 622
                            START      5,,,1                                                      623
                            RESET                                                                 624
                            START      5,,,1                                                      625
                            RESET                                                                 626
                            START      5,,,1                                                      627
                     PRITY  FUNCTION   P2,L4                                                      628
ERROR IN ABOVE CARD * * * * * MULTIPLE DEFINED ENTITY SYMBOL (NON-FATAL)       <<<<<

                     1,1/2,3/3,2/4,4                       SHORT JOB BENEFIT                      629
                            CLEAR                                                                 630
                            START      2,NP                INITIALIZE THE SIMULATOR               631
                            RESET                                                                 632
                            START      5,,,1                                                      633
                            RESET                                                                 634
                            START      5,,,1                                                      635
                            RESET                                                                 636
                            START      5,,,1                                                      637
                            RESET                                                                 638
                            START      5,,,1                                                      639
                            END                                                                   640
```

SYMBOL	NUMBER	REFERENCES BY CARD NO.
AGAIN	68	99
CMP10	93	508 519 532
CMP15	92	543
CMP20	91	
CMP25	90	522 535 549 552 561
CMP30	89	
CMP35	88	
CMP40	87	
CMP45	86	
CMP50	85	
CMP55	84	
CMP5	94	517 547 559
CMP60	83	
CMP65	82	
CMP70	81	
CMP75	80	
CMP80	79	
CMP85	78	
CMP90	77	
CMP95	76	
CPUFR	229	291
CPUFW	281	357
CPUIN	139	171
CPUMR	255	323
CPUMW	307	389
CPUOT	189	227
CPUTI	333	423
CPUTO	361	458
CYC10	47	
CYC1	56	
CYC2	55	
CYC3	54	
CYC4	53	505 529
CYC5	52	512 541
CYC6	51	
CYC7	50	
CYC8	49	
CYC9	48	
ENDCY	63	509 521 533 551
EXIT	28	527 538 557 564
FHDRD	215	507 516 531 546
FHDWR	267	514 544
FIN	22	97 102 106 117 153 249 279 302 313 335 347 368 379 401 413 434 448 469 483
INPUT	23	515 545
MHDRD	240	510 518 534 548 560
MHDWR	292	
NEXT	15	29
NOTAB	211	275

SYMBOL	NUMBER	REFERENCES BY CARD NO.											
NXT	133	182											
NXTIN	155	208											
NXTO	183	239											
NXTOT	213	274											
OTPUT	159	511	520	523	524	525	536	540	550	553	554	555	563
RANDM	72	506	513	530	542								
RDWD	147	216											
RECMP	95	161											
SKTAB	181	245											
SLICE	104	145											
START	10	190	212										
TAPIN	319												
TAPOT	347	526	537	556	562								
TMOUT	30	45											
TRMIN	112	16	41										
TRWD	123	196											
WDOT	202	281											
WDOUT	171	255											

SYMBOL	NUMBER	REFERENCES BY CARD NO.																
CHANA	2	65	73	292	301	358	367											
CHANB	4	67	71	324	334	390	400											
CHANC	8	424	433	459	468													
CONTA	3	66	72	293	300	303	312	359	366	369	378							
CONTB	5	68	70	325	333	336	346	391	399	402	412							
CPU	1	23	27	62	64	148	151	157	160	176	179	185	189	200	203	205	207	231
		236	240	244	259	266	270	272	297	299	308	311	330	332	342	345	363	365
		374	377	396	398	408	411	429	431	435	439	443	447	464	466	470	474	478
		482																
MUXCH	6	174	187	192	194	232	242	251	253									
TAPCN	9	425	432	437	446	460	467	472	481									
TMCON	7	175	186	191	195	197	211	213	215	233	241	250	254	260	267	269	273	

SYMBOL	NUMBER	REFERENCES BY CARD NO.						
BUFFI	3	21	172	173	198	199	491	605
BUFFO	4	229	230	248	257	258	278	492
TASKS	2	17	18	37	46	490		
TERMS	1	9	47	584				

SYMBOL	NUMBER	REFERENCES BY CARD NO.					
COREQ	2	20	183	209			
CPU	3	22	24	147	149	156	158
FHDRD	5	289	294	304			
FHDWR	7	355	360	370			
INPUT	1	14	40	177	201		
MHDRD	6	321	326	337			
MHDWR	8	387	392	403			
OTPUT	4	228	234	256	261		
TAPIN	9	421	426	438			
TAPOT	10	456	461	473			

SYMBOL	NUMBER	REFERENCES BY CARD NO.
CPUIO	1	305 306 310 339 340 344 371 372 376 405 406 410 440 441 445 475 476 480

SYMBOL	NUMBER	REFERENCES BY CARD NO.
RESPN	2	225 246 276
TTIME	1	48 50

SYMBOL	NUMBER	REFERENCES BY CARD NO.
DISTR	6	10 500
POIS	5	3 8
PRITY	7	13 502 616 628

SYMBOL	NUMBER	REFERENCES BY CARD NO.								
BAUD	13	226	579							
CHANA	16	291	357	568						
CHANB	19	323	389	569						
CHANC	26	423	458	590						
CPUTM	11	206	264	271	582					
FROT	17	295	295	307	307	361	361	373	373	573
LATRL	23	327	327	338	338	393	393	404	404	570
MROT	24	328	328	341	341	394	394	407	407	571
MUXCH	7	171	227	578						
RAND	5	115	118							
RDTAP	28	428	444	463	479	592				
READF	18	296	309	362	375	574				
READM	25	329	343	395	409	572				
SLICE	6	145	154	159	493					
SYCHN	4	60	495							
SYCPU	3	59	494							
SYSCH	1	26	496							
THINK	2	39	39	581						
TPACC	27	427	442	462	477	591				
TRATE	12	226	252	268	280					
TYPE	10	193	214	580						
WDSIZ	14	226	489							
WDTRN	9	181	238	583						
WORDI	8	180	204	585						
WORDO	15	237	263	586						

APPENDIX - B

Simulation Run Listings

```
                RESET                                                                   597
                START       5,,,1                                                       598
```

****

TERMINAL STATISTICS * ABSOLUTE CLOCK = 420000 RELATIVE CLOCK = 300000

****

****
BLOCK COUNTS
****

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	164	2# ENTER	0	164	3# ASSIGN	0	164	4# ASSIGN	0	164	5# ASSIGN	0	164
6# PRIOR	0	164	7# QUEUE	0	164	8# BUFFER	0	164	9# TRANSF	0	164	10# GATE	0	497
11# ENTER	0	497	12# ASSIGN	0	497	13# DEPART	0	497	14# LEAVE	0	497	15# QUEUE	0	4979
16# SEIZE	0	4979	17# DEPART	0	4979	18# ASSIGN	0	4979	19# ADVANC	0	4979	20# RELEAS	0	4979
21# TRANSF	0	4979	22# TRANSF	0	4482	23# LEAVE	0	337	24# ASSIGN	0	337	25# ADVANC	4	337
26# QUEUE	0	335	27# TRANSF	0	335	28# TEST	0	160	29# LEAVE	0	160	30# LEAVE	0	160
31# TABULT	0	160	32# TERM	0	160	33# GENERT	0	312	34# PREMPT	0	312	35# ADVANC	1	312
36# RETURN	0	311	37# SEIZE	0	311	38# SEIZE	0	311	39# SEIZE	0	311	40# SEIZE	0	311
41# ADVANC	0	311	42# RELEAS	0	311	43# RELEAS	0	311	44# RELEAS	0	311	45# RELEAS	0	311
46# TERM	0	311	52# ASSIGN	0	66	53# ASSIGN	0	124	54# ASSIGN	0	124	55# ASSIGN	0	124
56# ASSIGN	0	124	57# ASSIGN	0	124	58# ASSIGN	0	124	59# ASSIGN	0	124	60# ASSIGN	0	124
61# ASSIGN	0	124	62# TRANSF	0	124	63# ASSIGN	0	609	64# LOOP	0	609	65# ASSIGN	0	112
66# ASSIGN	0	112	67# TRANSF	0	112	68# ASSIGN	0	497	69# ASSIGN	0	497	70# ASSIGN	0	497
71# TRANSF	0	497	72# ASSIGN	0	124	73# ASSIGN	0	124	74# ASSIGN	0	124	75# TRANSF	0	124
90# ASSIGN	0	398	91# ASSIGN	0	398	92# ASSIGN	0	645	93# ASSIGN	0	1016	94# ASSIGN	0	1409
95# TEST	0	1409	96# BUFFER	0	1409	97# QUELE	0	1409	98# SEIZE	0	1409	99# DEPART	0	1409
100# ADVANC	0	1409	101# RELEAS	0	1409	102# ASSIGN	0	1409	103# TRANSF	0	1409	112# BUFFER	0	499
113# TEST	14	499	114# GATE	0	497	115# ENTER	0	497	116# SEIZE	0	497	117# SEIZE	0	497
118# PREMPT	0	497	119# DEPART	0	497	120# ADVANC	0	497	121# RETURN	0	497	122# ASSIGN	0	497
123# ADVANC	0	4967	124# LOOP	0	4967	125# QUEUE	0	497	126# MARK	0	497	127# PREMPT	0	497
128# RELEAS	0	497	129# RELEAS	0	497	130# ADVANC	0	497	131# RETURN	0	497	132# TRANSF	C	497
133# RELEAS	0	4470	134# RELEAS	0	4470	135# ADVANC	15	4470	136# SEIZE	0	4470	137# SEIZE	0	4470
138# TRANSF	0	4470	159# BUFFER	0	659	160# TEST	0	659	161# QUEUE	0	659	162# GATE	0	659
163# ENTER	0	659	164# SEIZE	0	659	165# SEIZE	0	659	166# SEIZE	0	659	167# DEPART	0	659
168# ADVANC	0	659	169# RELEAS	0	659	170# ASSIGN	0	659	171# ADVANC	0	3295	172# LOOP	0	3295
173# PREMPT	0	659	174# RELEAS	0	659	175# RELEAS	0	659	176# ADVANC	0	659	177# RETURN	0	659
178# TEST	0	659	179# TABULT	0	497	180# ASSIGN	0	497	181# LEAVE	0	659	182# TRANSF	0	659
183# RELEAS	0	2636	184# RELEAS	0	2636	185# ADVANC	C	2636	186# SEIZE	0	2636	187# SEIZE	C	2636
188# TRANSF	0	2636	215# QUEUE	0	609	216# BUFFER	C	609	217# TEST	0	609	218# SEIZE	0	609
219# SEIZE	0	609	220# DEPART	0	609	221# ADVANC	0	609	222# ADVANC	0	609	223# PREMPT	0	609
224# ADVANC	0	609	225# RETURN	0	609	226# RELEAS	0	609	227# RELEAS	0	609	228# TRANSF	0	609
240# QUEUE	0	451	241# BUFFER	0	451	242# TEST	0	451	243# SEIZE	0	451	244# SEIZE	0	451
245# DEPART	0	451	246# ADVANC	0	451	247# ADVANC	0	451	248# ADVANC	0	451	249# PREMPT	0	451
250# ADVANC	0	451	251# RETURN	0	451	252# RELEAS	0	451	253# RELEAS	0	451	254# TRANSF	0	451
267# QUEUE	0	337	268# BUFFER	0	337	269# TEST	0	337	270# SEIZE	0	337	271# SEIZE	C	337
272# DEPART	0	337	273# ADVANC	0	337	274# ADVANC	0	337	275# PREMPT	0	337	276# ADVANC	0	337
277# RETURN	0	337	278# RELEAS	0	337	279# RELEAS	0	337	280# TRANSF	0	337	347# QUEUE	0	160
348# BUFFER	0	160	349# TEST	0	160	350# SEIZE	0	160	351# SEIZE	0	160	352# DEPART	0	160
353# ADVANC	0	160	354# ADVANC	0	160	355# PREMPT	0	160	356# ADVANC	0	160	357# RETURN	0	160
358# RELEAS	0	160	359# RELEAS	0	160	360# TRANSF	0	160	375# GENERT	0	5	376# TERM	0	5

****
FACILITIES
****

REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	10569	6.57	0.2315	0.2315	0.	A	100.00	0	15
CHANA	1257	32.50	0.1362	0.1362	0.	A	100.00	0	0
CONTA	1257	32.50	0.1362	0.1362	0.	A	100.00	0	0
CHANB	762	76.68	0.1948	0.1948	0.	A	100.00	0	0
CONTB	762	76.68	0.1948	0.1948	0.	A	100.00	0	0
MUXCH	8262	5.75	0.1584	0.1584	0.	A	100.00	0	0
TMCON	8262	5.75	0.1584	0.1584	0.	A	100.00	0	0
CHANC	160	25.27	0.0135	0.0135	0.	A	100.00	0	0
TAPCN	160	25.27	0.0135	0.0135	0.	A	100.00	0	0

****
STORAGES
****

REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	33.29	193	51752.36	0.333	0.333	0.	A	100.00	33	44
TASKS	5	0.63	497	377.90	0.125	0.125	0.	A	100.00	0	3
BUFFI	15	15.00	512	8789.06	1.000	1.000	0.	A	100.00	15	15
BUFFO	5	0.19	659	88.36	0.039	0.039	0.	A	100.00	0	3

****
QUEUES
****

REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	27	14.72	511	0	0.	8640.49	8640.49	0	14
COREQ	1	0.01	497	0	0.	3.75	3.75	0	0
CPU	3	0.01	6388	6032	94.43	0.53	9.49	0	0
OTPUT	1	0.00	659	528	80.12	1.39	6.97	0	0
FHDRD	2	0.01	609	526	86.37	3.27	23.99	0	0
MHDRD	2	0.01	451	385	85.37	7.37	50.38	0	0
FHDWR	1	0.00	337	307	91.10	2.42	27.13	0	0
TAPOT	1	0.	160	160	100.00	0.	0.	0	0

****
TABLES
****

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	160	50801.637	55562.698	8128262.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.914
5000	0	0.	0.	100.00	0.098	-0.824
10000	0	0.	0.	100.00	0.197	-0.734
15000	5	3.13	3.13	96.88	0.295	-0.644
20000	80	50.00	53.13	46.88	0.394	-0.554
25000	20	12.50	65.63	34.38	0.492	-0.464
30000	1	0.62	66.25	33.75	0.591	-0.374
35000	1	0.62	66.87	33.13	0.689	-0.284
40000	6	3.75	70.62	29.38	0.787	-0.194
45000	2	1.25	71.88	28.13	0.886	-0.104
50000	2	1.25	73.12	26.88	0.984	-0.014
55000	0	0.	73.12	26.88	1.083	0.076
60000	1	0.62	73.75	26.25	1.181	0.166
65000	0	0.	73.75	26.25	1.279	0.256
70000	0	0.	73.75	26.25	1.378	0.346
75000	3	1.87	75.62	24.38	1.476	0.436
80000	2	1.25	76.87	23.13	1.575	0.526
85000	3	1.87	78.75	21.25	1.673	0.615
90000	0	0.	78.75	21.25	1.772	0.705
95000	1	0.62	79.37	20.63	1.870	0.795
100000	1	0.62	80.00	20.00	1.968	0.885
105000	1	0.62	80.62	19.38	2.067	0.975
110000	2	1.25	81.87	18.13	2.165	1.065
115000	1	0.62	82.50	17.50	2.264	1.155
120000	4	2.50	85.00	15.00	2.362	1.245
OVERFLOW	24	15.00	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 165727.541 MAXIMUM VALUE OF OVERFLOW = 225857

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	497	296.638	121.260	147429.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.446
500	462	92.96	92.96	7.04	1.686	1.677
1000	35	7.04	100.00	0.	3.371	5.800

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET
                START       5,,,1                                                599
                                                                                 600
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* TERMINAL STATISTICS * ABSOLUTE CLOCK = 720000 RELATIVE CLOCK = 300000

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BLOCK COUNTS
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	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	199	2# ENTER	0	199	3# ASSIGN	0	199	4# ASSIGN	0	199	5# ASSIGN	0	199
6# PRIOR	0	199	7# QUEUE	0	199	8# BUFFER	0	199	9# TRANSF	0	199	10# GATE	0	498
11# ENTER	0	498	12# ASSIGN	0	498	13# DEPART	0	498	14# LEAVE	0	498	15# QUEUE	0	5100
16# SEIZE	0	5100	17# DEPART	0	5100	18# ASSIGN	0	5100	19# ADVANC	0	5100	20# RELEAS	0	5100
21# TRANSF	0	5100	22# TRANSF	0	4602	23# LEAVE	0	330	24# ASSIGN	0	330	25# ADVANC	3	330
26# QUEUE	0	331	27# TRANSF	0	331	28# TEST	0	167	29# LEAVE	0	167	30# LEAVE	0	167
31# TABULT	0	167	32# TERM	0	167	33# GENERT	0	292	34# PREMPT	0	292	35# ADVANC	0	292
36# RETURN	0	293	37# SEIZE	0	293	38# SEIZE	0	293	39# SEIZE	0	293	40# SEIZE	0	293
41# ADVANC	1	293	42# RELEAS	0	292	43# RELEAS	0	292	44# RELEAS	0	292	45# RELEAS	0	292
46# TERM	0	292	52# ASSIGN	0	67	53# ASSIGN	0	137	54# ASSIGN	0	137	55# ASSIGN	0	137
56# ASSIGN	0	137	57# ASSIGN	0	137	58# ASSIGN	0	137	59# ASSIGN	0	137	60# ASSIGN	0	137
61# ASSIGN	0	137	62# TRANSF	0	137	63# ASSIGN	0	654	64# LOOP	0	654	65# ASSIGN	0	123
66# ASSIGN	0	123	67# TRANSF	0	123	68# ASSIGN	0	531	69# ASSIGN	0	531	70# ASSIGN	0	531
71# TRANSF	0	531	72# ASSIGN	0	137	73# ASSIGN	0	137	74# ASSIGN	0	137	75# TRANSF	0	137
90# ASSIGN	0	363	91# ASSIGN	0	363	92# ASSIGN	0	561	93# ASSIGN	0	1019	94# ASSIGN	0	1408
95# TEST	0	1408	96# BUFFER	0	1408	97# QUEUE	0	1408	98# SEIZE	0	1408	99# DEPART	0	1408
100# ADVANC	0	1408	101# RELEAS	0	1408	102# ASSIGN	0	1408	103# TRANSF	0	1408	112# BUFFER	0	530
113# TEST	46	530	114# GATE	0	498	115# ENTER	0	498	116# SEIZE	0	498	117# SEIZE	0	498
118# PREMPT	0	498	119# DEPART	0	498	120# ADVANC	0	498	121# RETURN	0	498	122# ASSIGN	0	498
123# ADVANC	0	4966	124# LOOP	0	4966	125# QUEUE	0	498	126# MARK	0	498	127# PREMPT	0	498
128# RELEAS	0	498	129# RELEAS	0	498	130# ADVANC	0	498	131# RETURN	0	498	132# TRANSF	0	498
133# RELEAS	0	4468	134# RELEAS	0	4468	135# ADVANC	15	4468	136# SEIZE	0	4468	137# SEIZE	0	4468
138# TRANSF	0	4468	159# BUFFER	0	656	160# TEST	0	656	161# QUEUE	0	656	162# GATE	0	656
163# ENTER	0	656	164# SEIZE	0	656	165# SEIZE	0	656	166# SEIZE	0	656	167# DEPART	0	656
168# ADVANC	0	656	169# RELEAS	0	656	17C# ASSIGN	C	656	171# ADVANC	0	3280	172# LOOP	0	3280
173# PREMPT	0	656	174# RELEAS	0	656	175# RELEAS	0	656	176# ADVANC	0	656	177# RETURN	0	656
178# TEST	0	656	179# TABULT	0	497	180# ASSIGN	0	497	181# LEAVE	0	656	182# TRANSF	0	656
183# RELEAS	0	2624	184# RELEAS	0	2624	185# ADVANC	0	2624	186# SEIZE	0	2624	187# SEIZE	0	2624
188# TRANSF	0	2624	215# QUEUE	0	655	216# BUFFER	0	655	217# TEST	1	655	218# SEIZE	0	654
219# SEIZE	0	654	220# DEPART	0	654	221# ADVANC	0	654	222# ADVANC	0	654	223# PREMPT	0	654
224# ADVANC	0	654	225# RETURN	0	654	226# RELEAS	0	654	227# RELEAS	0	654	228# TRANSF	0	654
240# QUEUE	0	459	241# BUFFER	0	459	242# TEST	C	459	243# SEIZE	0	459	244# SEIZE	0	459
245# DEPART	0	459	246# ADVANC	0	459	247# ADVANC	0	459	248# ADVANC	0	459	249# PREMPT	0	459
250# ADVANC	0	459	251# RETURN	0	459	252# RELEAS	0	459	253# RELEAS	0	459	254# TRANSF	0	459
267# QUEUE	0	330	268# BUFFER	0	330	269# TEST	0	330	270# SEIZE	0	330	271# SEIZE	0	330
272# DEPART	0	330	273# ADVANC	0	330	274# ADVANC	0	330	275# PREMPT	0	330	276# ADVANC	0	330
277# RETURN	0	330	278# RELEAS	0	330	279# RELEAS	0	330	280# TRANSF	0	330	347# QUEUE	C	167
348# BUFFER	0	167	349# TEST	0	167	350# SEIZE	0	167	351# SEIZE	0	167	352# DEPART	0	167
353# ADVANC	0	167	354# ADVANC	0	167	355# PREMPT	0	167	356# ADVANC	0	167	357# RETURN	0	167
358# RELEAS	0	167	359# RELEAS	0	167	360# TRANSF	0	167	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	10719	6.39	0.2283	0.2283	0.	A	100.00	0	0
CHANA	1277	31.77	0.1352	0.1352	0.	A	100.00	21	0
CONTA	1277	31.77	0.1352	0.1352	0.	A	100.00	21	0
CHANB	752	78.07	0.1957	0.1957	0.	A	100.00	21	0
CONTB	752	78.07	0.1957	0.1957	0.	A	100.00	21	0
MUXCH	8246	5.73	0.1575	0.1575	0.	A	100.00	0	0
TMCON	8246	5.73	0.1575	0.1575	0.	A	100.00	0	0
CHANC	167	24.51	0.0136	0.0136	0.	A	100.00	0	0
TAPCN	167	24.51	0.0136	0.0136	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	45.65	232	59035.94	0.457	0.457	0.	A	100.00	65	68
TASKS	5	0.62	498	376.48	0.125	0.125	0.	A	100.00	1	3
BUFFI	15	15.00	513	8771.93	1.000	1.000	0.	A	100.00	15	15
BUFFO	5	0.19	656	88.43	0.039	0.039	0.	A	100.00	0	2

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	51	27.23	544	0	0.	15014.69	15014.69	0	46
COREQ	1	0.01	498	0	C.	3.64	3.64	0	0
CPU	3	0.01	6508	6180	94.96	0.47	9.27	0	0
OTPUT	2	0.00	656	505	76.98	1.71	7.41	0	0
FHDRD	2	0.01	655	574	87.63	3.96	32.06	0	1
MHDRD	1	0.00	459	420	91.50	3.14	37.00	0	0
FHDWR	1	0.00	330	298	90.30	2.69	27.78	0	0
TAPOT	1	0.00	167	166	99.40	0.11	19.00	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATICN	SUM OF ARGUMENTS
TTIME	167	61003.407	63084.666	10187569.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.967
5000	0	0.	0.	100.00	0.082	-0.888
10000	0	0.	0.	100.00	0.164	-0.808
15000	0	0.	0.	100.00	0.246	-0.729
20000	41	24.55	24.55	75.45	0.328	-0.650
25000	32	19.16	43.71	56.29	0.410	-0.571
30000	17	10.18	53.89	46.11	0.492	-0.491
35000	15	8.98	62.87	37.13	0.574	-0.412
40000	9	5.39	68.26	31.74	0.656	-0.333
45000	3	1.80	70.06	29.94	0.738	-0.254
50000	1	0.60	70.66	29.34	0.820	-0.174
55000	0	0.	70.66	29.34	0.902	-0.095
60000	0	0.	70.66	29.34	0.984	-0.016
65000	3	1.80	72.46	27.54	1.066	0.063
70000	0	0.	72.46	27.54	1.147	0.143
75000	0	0.	72.46	27.54	1.229	0.222
80000	0	0.	72.46	27.54	1.311	0.301
85000	1	0.60	73.05	26.95	1.393	0.380
90000	2	1.20	74.25	25.75	1.475	0.460
95000	1	0.60	74.85	25.15	1.557	0.539
100000	2	1.20	76.05	23.95	1.639	0.618
105000	2	1.20	77.25	22.75	1.721	0.697
110000	4	2.40	79.64	20.36	1.803	0.777
115000	1	0.60	80.24	19.76	1.885	0.856
120000	2	1.20	81.44	18.56	1.967	0.935
OVERFLOW	31	18.56	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 179866.902 MAXIMUM VALUE OF OVERFLOW = 242186

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	497	297.376	119.107	147796.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.497
500	458	92.15	92.15	7.85	1.681	1.701
1000	39	7.85	100.00	0.	3.363	5.899

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET                                                    601
                START       5,,,1                                        602
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 1020000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	191	2# ENTER	0	191	3# ASSIGN	0	191	4# ASSIGN	0	191	5# ASSIGN	0	191
6# PRIOR	0	191	7# QUEUE	0	191	8# BUFFER	0	191	9# TRANSF	0	191	10# GATE	0	496
11# ENTER	0	496	12# ASSIGN	0	496	13# DEPART	0	496	14# LEAVE	0	496	15# QUEUE	0	4848
16# SEIZE	0	4848	17# DEPART	0	4848	18# ASSIGN	0	4848	19# ADVANC	0	4848	20# RELEAS	0	4848
21# TRANSF	0	4848	22# TRANSF	0	4352	23# LEAVE	0	324	24# ASSIGN	0	324	25# ADVANC	5	324
26# QUEUE	0	322	27# TRANSF	0	322	28# TEST	0	173	29# LEAVE	0	173	30# LEAVE	0	173
31# TABULT	0	173	32# TERM	0	173	33# GENERT	0	298	34# PREMPT	0	298	35# ADVANC	0	298
36# RETURN	0	298	37# SEIZE	0	298	38# SEIZE	0	298	39# SEIZE	0	298	40# SEIZE	0	298
41# ADVANC	0	298	42# RELEAS	0	299	43# RELEAS	0	299	44# RELEAS	0	299	45# RELEAS	0	299
46# TERM	0	299	52# ASSIGN	0	64	53# ASSIGN	0	123	54# ASSIGN	0	123	55# ASSIGN	0	123
56# ASSIGN	0	123	57# ASSIGN	0	123	58# ASSIGN	0	123	59# ASSIGN	0	123	60# ASSIGN	0	123
61# ASSIGN	0	123	62# TRANSF	0	123	63# ASSIGN	0	572	64# LOOP	0	572	65# ASSIGN	0	116
66# ASSIGN	0	116	67# TRANSF	0	116	68# ASSIGN	0	456	69# ASSIGN	0	456	70# ASSIGN	0	456
71# TRANSF	0	456	72# ASSIGN	0	123	73# ASSIGN	0	123	74# ASSIGN	0	123	75# TRANSF	0	123
90# ASSIGN	0	367	91# ASSIGN	0	367	92# ASSIGN	0	572	93# ASSIGN	0	950	94# ASSIGN	0	1344
95# TEST	0	1344	96# BUFFER	0	1344	97# QUEUE	0	1344	98# SEIZE	0	1344	99# DEPART	0	1344
100# ADVANC	0	1344	101# RELEAS	0	1344	102# ASSIGN	0	1344	103# TRANSF	0	1344	112# BUFFER	0	513
113# TEST	63	513	114# GATE	0	496	115# ENTER	0	496	116# SEIZE	0	496	117# SEIZE	0	496
118# PREMPT	0	496	119# DEPART	0	496	120# ADVANC	0	496	121# RETURN	0	496	122# ASSIGN	0	496
123# ADVANC	0	4965	124# LOOP	0	4965	125# QUEUE	0	496	126# MARK	0	496	127# PREMPT	0	496
128# RELEAS	0	496	129# RELEAS	0	496	130# ADVANC	0	496	131# RETURN	0	496	132# TRANSF	0	496
133# RELEAS	0	4469	134# RELEAS	0	4469	135# ADVANC	15	4469	136# SEIZE	0	4469	137# SEIZE	0	4469
138# TRANSF	0	4469	159# BUFFER	0	668	160# TEST	0	668	161# QUEUE	0	668	162# GATE	0	668
163# ENTER	0	668	164# SEIZE	0	668	165# SEIZE	0	668	166# SEIZE	0	668	167# DEPART	0	668
168# ADVANC	0	668	169# RELEAS	0	668	170# ASSIGN	0	668	171# ADVANC	0	3340	172# LOOP	0	3340
173# PREMPT	0	668	174# RELEAS	0	668	175# RELEAS	0	668	176# ADVANC	0	668	177# RETURN	0	668
178# TEST	0	668	179# TABULT	0	497	180# ASSIGN	0	497	181# LEAVE	0	668	182# TRANSF	0	668
183# RELEAS	0	2672	184# RELEAS	0	2672	185# ADVANC	0	2672	186# SEIZE	0	2672	187# SEIZE	0	2672
188# TRANSF	0	2672	215# QUEUE	0	571	216# BUFFER	0	571	217# TEST	0	571	218# SEIZE	0	572
219# SEIZE	0	572	220# DEPART	0	572	221# ADVANC	0	572	222# ADVANC	0	572	223# PREMPT	0	572
224# ADVANC	0	572	225# RETURN	0	572	226# RELEAS	0	572	227# RELEAS	0	572	228# TRANSF	0	572
240# QUEUE	0	453	241# BUFFER	0	453	242# TEST	0	453	243# SEIZE	0	453	244# SEIZE	0	453
245# DEPART	0	453	246# ADVANC	0	453	247# ADVANC	0	453	248# ADVANC	0	453	249# PREMPT	0	453
250# ADVANC	0	453	251# RETURN	0	453	252# RELEAS	0	453	253# RELEAS	0	453	254# TRANSF	0	453
267# QUEUE	0	324	268# BUFFER	0	324	269# TEST	0	324	270# SEIZE	0	324	271# SEIZE	0	324
272# DEPART	0	324	273# ADVANC	0	324	274# ADVANC	0	324	275# PREMPT	0	324	276# ADVANC	0	324
277# RETURN	0	324	278# RELEAS	0	324	279# RELEAS	0	324	280# TRANSF	0	324	347# QUEUE	0	173
348# BUFFER	0	173	349# TEST	0	173	350# SEIZE	0	173	351# SEIZE	0	173	352# DEPART	0	173
353# ADVANC	0	173	354# ADVANC	0	173	355# PREMPT	0	173	356# ADVANC	0	173	357# RETURN	0	173
358# RELEAS	0	173	359# RELEAS	0	173	360# TRANSF	0	173	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	10340	6.47	0.2229	0.2229	0.	A	100.00	0	0
CHANA	1195	32.44	0.1292	0.1292	0.	A	100.00	0	0
CONTA	1195	32.44	0.1292	0.1292	0.	A	100.00	0	0
CHANB	752	79.29	0.1987	0.1987	0.	A	100.00	0	0
CONTB	752	79.29	0.1987	0.1987	0.	A	100.00	0	0
MUXCH	8305	5.74	0.1589	0.1589	0.	A	100.00	0	0
TMCON	8305	5.74	0.1589	0.1589	0.	A	100.00	0	0
CHANC	173	25.03	0.0144	0.0144	0.	A	100.00	0	0
TAPCN	173	25.03	0.0144	0.0144	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	75.64	256	88644.86	0.756	0.756	0.	A	100.00	83	87
TASKS	5	0.62	497	375.77	0.125	0.125	0.	A	100.00	0	3
BUFFI	15	15.00	511	8806.26	1.000	1.000	0.	A	100.00	15	15
BUFFO	5	0.20	668	89.17	0.040	0.040	0.	A	100.00	0	2

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QLEUES
****

REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	70	57.15	559	0	0.	30671.84	30671.84	0	63
COREQ	1	0.01	496	0	0.	3.14	3.14	0	0
CPU	2	0.01	6192	5818	93.96	0.55	9.13	0	0
OTPUT	1	0.00	668	492	73.65	2.03	7.69	0	0
FHDRD	2	0.01	572	499	87.24	3.61	28.32	0	0
MHDRD	1	0.01	453	405	89.40	4.04	38.17	0	0
FHDWR	1	0.00	324	283	87.35	2.76	21.83	0	0
TAPOT	1	0.	173	173	100.00	0.	0.	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	173	105693.155	106624.928	18284916.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.991
5000	0	0.	0.	100.00	0.047	-0.944
10000	0	0.	0.	100.00	0.095	-0.897
15000	0	0.	0.	100.00	0.142	-0.851
20000	0	0.	0.	100.00	0.189	-0.804
25000	0	0.	0.	100.00	0.237	-0.757
30000	0	0.	0.	100.00	0.284	-0.710
35000	0	0.	0.	100.00	0.331	-0.663
40000	26	15.03	15.03	84.97	0.378	-0.616
45000	49	28.32	43.35	56.65	0.426	-0.569
50000	39	22.54	65.90	34.10	0.473	-0.522
55000	2	1.16	67.05	32.95	0.520	-0.475
60000	0	0.	67.05	32.95	0.568	-0.429
65000	0	0.	67.05	32.95	0.615	-0.382
70000	0	0.	67.05	32.95	0.662	-0.335
75000	1	0.58	67.63	32.37	0.710	-0.288
80000	0	0.	67.63	32.37	0.757	-0.241
85000	2	1.16	68.79	31.21	0.804	-0.194
90000	1	0.58	69.36	30.64	0.852	-0.147
95000	1	0.58	69.94	30.06	0.899	-0.100
100000	2	1.16	71.10	28.90	0.946	-0.053
105000	0	0.	71.10	28.90	0.993	-0.007
110000	1	0.58	71.68	28.32	1.041	0.040
115000	0	0.	71.68	28.32	1.088	0.087
120000	0	0.	71.68	28.32	1.135	0.134
OVERFLOW	49	28.32	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 255709.061 MAXIMUM VALUE OF OVERFLOW = 429107

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	497	293.125	109.836	145683.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.669
500	470	94.57	94.57	5.43	1.706	1.883
1000	27	5.43	100.00	0.	3.412	6.436

THE REMAINING FREQUENCIES ARE ALL ZERO

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RESET                                                          603
START      5,,,1                                               604
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 1320000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	146	2# ENTER	0	146	3# ASSIGN	0	146	4# ASSIGN	0	146	5# ASSIGN	0	146
6# PRIOR	0	146	7# QUEUE	0	146	8# BUFFER	0	146	9# TRANSF	0	146	10# GATE	0	497
11# ENTER	0	497	12# ASSIGN	0	497	13# DEPART	0	497	14# LEAVE	0	497	15# QUEUE	0	5222
16# SEIZE	0	5222	17# DEPART	0	5222	18# ASSIGN	0	5222	19# ADVANC	0	5222	20# RELEAS	0	5222
21# TRANSF	0	5222	22# TRANSF	0	4725	23# LEAVE	0	366	24# ASSIGN	0	366	25# ADVANC	3	366
26# QUEUE	0	368	27# TRANSF	0	368	28# TEST	0	131	29# LEAVE	0	131	30# LEAVE	0	131
31# TABULT	0	131	32# TERM	0	131	33# GENERT	0	309	34# PREMPT	0	309	35# ADVANC	0	309
36# RETURN	0	309	37# SEIZE	0	309	38# SEIZE	0	309	39# SEIZE	0	309	40# SEIZE	0	309
41# ADVANC	0	309	42# RELEAS	0	309	43# RELEAS	0	309	44# RELEAS	0	309	45# RELEAS	0	309
46# TERM	0	309	52# ASSIGN	0	75	53# ASSIGN	0	148	54# ASSIGN	0	148	55# ASSIGN	0	148
56# ASSIGN	0	148	57# ASSIGN	0	148	58# ASSIGN	0	148	59# ASSIGN	0	148	60# ASSIGN	0	148
61# ASSIGN	0	148	62# TRANSF	0	148	63# ASSIGN	0	702	64# LOOP	0	702	65# ASSIGN	0	122
66# ASSIGN	0	122	67# TRANSF	0	122	68# ASSIGN	0	580	69# ASSIGN	0	580	70# ASSIGN	0	580
71# TRANSF	0	580	72# ASSIGN	0	148	73# ASSIGN	0	148	74# ASSIGN	0	148	75# TRANSF	0	148
90# ASSIGN	0	333	91# ASSIGN	0	333	92# ASSIGN	0	541	93# ASSIGN	0	1041	94# ASSIGN	0	1426
95# TEST	0	1426	96# BUFFER	0	1426	97# QUEUE	0	1426	98# SEIZE	0	1426	99# DEPART	0	1426
100# ADVANC	0	1426	101# RELEAS	0	1426	102# ASSIGN	0	1426	103# TRANSF	0	1426	112# BUFFER	0	514
113# TEST	80	514	114# GATE	0	497	115# ENTER	0	497	116# SEIZE	0	497	117# SEIZE	0	497
118# PREMPT	0	497	119# DEPART	0	497	120# ADVANC	0	497	121# RETURN	0	497	122# ASSIGN	0	497
123# ADVANC	0	4968	124# LOOP	0	4968	125# QUEUE	0	497	126# MARK	0	497	127# PREMPT	0	497
128# RELEAS	0	497	129# RELEAS	0	497	130# ADVANC	0	497	131# RETURN	0	497	132# TRANSF	0	497
133# RELEAS	0	4471	134# RELEAS	0	4471	135# ADVANC	15	4471	136# SEIZE	0	4471	137# SEIZE	0	4471
138# TRANSF	0	4471	159# BUFFER	0	644	160# TEST	0	644	161# QUEUE	0	644	162# GATE	0	644
163# ENTER	0	644	164# SEIZE	0	644	165# SEIZE	0	644	166# SEIZE	0	644	167# DEPART	0	644
168# ADVANC	0	644	169# RELEAS	0	644	170# ASSIGN	0	644	171# ADVANC	0	3220	172# LOOP	0	3220
173# PREMPT	0	644	174# RELEAS	0	644	175# RELEAS	0	644	176# ADVANC	0	644	177# RETURN	0	644
178# TEST	0	644	179# TABULT	0	497	180# ASSIGN	0	497	181# LEAVE	0	644	182# TRANSF	0	644
183# RELEAS	0	2576	184# RELEAS	0	2576	185# ADVANC	0	2576	186# SEIZE	0	2576	187# SEIZE	0	2576
188# TRANSF	0	2576	215# QUEUE	0	702	216# BUFFER	0	702	217# TEST	0	702	218# SEIZE	0	702
219# SEIZE	0	702	220# DEPART	0	702	221# ADVANC	0	702	222# ADVANC	0	702	223# PREMPT	0	702
224# ADVANC	0	702	225# RETURN	0	702	226# RELEAS	0	702	227# RELEAS	0	702	228# TRANSF	0	702
240# QUEUE	0	458	241# BUFFER	0	458	242# TEST	0	458	243# SEIZE	0	458	244# SEIZE	0	458
245# DEPART	0	458	246# ADVANC	0	458	247# ADVANC	0	458	248# ADVANC	0	458	249# PREMPT	0	458
250# ADVANC	0	458	251# RETURN	0	458	252# RELEAS	0	458	253# RELEAS	0	458	254# TRANSF	0	458
267# QUEUE	0	366	268# BUFFER	0	366	269# TEST	0	366	270# SEIZE	0	366	271# SEIZE	0	366
272# DEPART	0	366	273# ADVANC	0	366	274# ADVANC	0	366	275# PREMPT	0	366	276# ADVANC	0	366
277# RETURN	0	366	278# RELEAS	0	366	279# RELEAS	0	366	280# TRANSF	0	366	347# QUEUE	0	131
348# BUFFER	0	131	349# TEST	0	131	350# SEIZE	0	131	351# SEIZE	0	131	352# DEPART	0	131
353# ADVANC	0	131	354# ADVANC	0	131	355# PREMPT	0	131	356# ADVANC	0	131	357# RETURN	0	131
358# RELEAS	0	131	359# RELEAS	0	131	360# TRANSF	0	131	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	10896	6.39	0.2322	0.2322	0.	A	100.00	0	0
CHANA	1377	32.21	0.1479	0.1479	0.	A	100.00	0	0
CONTA	1377	32.21	0.1479	0.1479	0.	A	100.00	0	0
CHANB	767	77.54	0.1983	0.1983	0.	A	100.00	0	0
CONTB	767	77.54	0.1983	0.1983	0.	A	100.00	0	0
MUXCH	8188	5.73	0.1565	0.1565	0.	A	100.00	0	0
TMCON	8188	5.73	0.1565	0.1565	0.	A	100.00	0	0
CHANC	131	26.15	0.0114	0.0114	0.	A	100.00	0	0
TAPCN	131	26.15	0.0114	0.0114	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	96.51	229	126435.49	0.965	0.965	0.	A	100.00	98	100
TASKS	5	0.63	497	381.57	0.126	0.126	0.	A	100.00	0	3
BUFFI	15	15.00	512	8789.06	1.000	1.000	0.	A	100.00	15	15
BUFFO	5	0.19	644	88.24	0.038	0.038	0.	A	100.00	0	2

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	85	77.84	577	0	0.	40470.44	40470.44	0	80
COREQ	1	0.01	497	0	0.	3.11	3.11	0	0
CPU	2	0.01	6648	6298	94.74	0.48	9.17	0	0
OTPUT	1	0.00	644	512	79.50	1.21	5.92	0	0
FHDRD	2	0.01	702	622	88.60	3.33	29.19	0	0
MHDRD	2	0.01	458	409	89.30	5.00	46.69	0	0
FHDWR	2	0.00	366	322	87.98	3.16	26.27	0	0
TAPOT	1	0.00	131	130	99.24	0.08	10.00	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	131	160113.098	158786.967	20974816.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-1.008
5000	0	0.	0.	100.00	0.031	-0.977
10000	0	0.	0.	100.00	0.062	-0.945
15000	0	0.	0.	100.00	0.094	-0.914
20000	0	0.	0.	100.00	0.125	-0.882
25000	0	0.	0.	100.00	0.156	-0.851
30000	0	0.	0.	100.00	0.187	-0.819
35000	0	0.	0.	100.00	0.219	-0.788
40000	0	0.	0.	100.00	0.250	-0.756
45000	10	7.63	7.63	92.37	0.281	-0.725
50000	15	11.45	19.08	80.92	0.312	-0.693
55000	17	12.98	32.06	67.94	0.344	-0.662
60000	38	29.01	61.07	38.93	0.375	-0.630
65000	2	1.53	62.60	37.40	0.406	-0.599
70000	0	0.	62.60	37.40	0.437	-0.568
75000	0	0.	62.60	37.40	0.468	-0.536
80000	0	0.	62.60	37.40	0.500	-0.505
85000	0	0.	62.60	37.40	0.531	-0.473
90000	0	0.	62.60	37.40	0.562	-0.442
95000	0	0.	62.60	37.40	0.593	-0.410
100000	0	0.	62.60	37.40	0.625	-0.379
105000	1	0.76	63.36	36.64	0.656	-0.347
110000	0	0.	63.36	36.64	0.687	-0.316
115000	1	0.76	64.12	35.88	0.718	-0.284
120000	0	0.	64.12	35.88	0.749	-0.253
OVERFLOW	47	35.88	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 348941.273 MAXIMUM VALUE OF OVERFLOW = 536956

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	497	301.614	127.789	149902.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.360
500	457	91.95	91.95	8.05	1.658	1.552
1000	40	8.05	100.00	0.	3.315	5.465

THE REMAINING FREQUENCIES ARE ALL ZERO

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                STORAGE     S3,25                                          605
                CLEAR                                                      606
                START       2,NP                                           607
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                RESET
                START       5,,,1                                                608
                                                                                 609
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 420000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	195	2# ENTER	0	195	3# ASSIGN	0	195	4# ASSIGN	0	195	5# ASSIGN	0	195
6# PRIOR	0	195	7# QUEUE	0	195	8# BUFFER	0	195	9# TRANSF	0	195	10# GATE	0	588
11# ENTER	0	588	12# ASSIGN	0	588	13# DEPART	0	588	14# LEAVE	0	588	15# QUEUE	0	5824
16# SEIZE	0	5824	17# DEPART	0	5824	18# ASSIGN	0	5824	19# ADVANC	1	5824	20# RELEAS	0	5823
21# TRANSF	0	5823	22# TRANSF	0	5236	23# LEAVE	0	382	24# ASSIGN	0	382	25# ADVANC	1	382
26# QUEUE	0	384	27# TRANSF	0	384	28# TEST	0	206	29# LEAVE	0	206	30# LEAVE	0	206
31# TABULT	0	206	32# TERM	0	206	33# GENERT	0	305	34# PREMPT	0	305	35# ADVANC	0	305
36# RETURN	0	305	37# SEIZE	0	305	38# SEIZE	0	305	39# SEIZE	0	305	40# SEIZE	0	305
41# ADVANC	0	305	42# RELEAS	0	305	43# RELEAS	0	305	44# RELEAS	0	305	45# RELEAS	0	305
46# TERM	0	305	52# ASSIGN	0	76	53# ASSIGN	0	158	54# ASSIGN	0	158	55# ASSIGN	0	158
56# ASSIGN	0	158	57# ASSIGN	0	158	58# ASSIGN	0	158	59# ASSIGN	0	158	60# ASSIGN	0	158
61# ASSIGN	0	158	62# TRANSF	0	158	63# ASSIGN	0	696	64# LOOP	0	696	65# ASSIGN	0	160
66# ASSIGN	0	160	67# TRANSF	0	160	68# ASSIGN	0	536	69# ASSIGN	0	536	70# ASSIGN	0	536
71# TRANSF	0	536	72# ASSIGN	0	158	73# ASSIGN	0	158	74# ASSIGN	0	158	75# TRANSF	0	158
90# ASSIGN	0	416	91# ASSIGN	0	416	92# ASSIGN	0	621	93# ASSIGN	0	1108	94# ASSIGN	0	1571
95# TEST	0	1571	96# BUFFER	0	1571	97# QUEUE	0	1571	98# SEIZE	0	1571	99# DEPART	0	1571
100# ADVANC	0	1571	101# RELEAS	0	1571	102# ASSIGN	0	1571	103# TRANSF	0	1571	112# BUFFER	0	579
113# TEST	0	579	114# GATE	0	579	115# ENTER	0	579	116# SEIZE	0	579	117# SEIZE	0	579
118# PREMPT	0	579	119# DEPART	0	579	120# ADVANC	0	579	121# RETURN	0	579	122# ASSIGN	0	579
123# ADVANC	0	5823	124# LOOP	0	5824	125# QUEUE	0	588	126# MARK	0	588	127# PREMPT	0	588
128# RELEAS	0	588	129# RELEAS	0	588	130# ADVANC	0	588	131# RETURN	0	588	132# TRANSF	0	588
133# RELEAS	0	5236	134# RELEAS	0	5236	135# ADVANC	15	5236	136# SEIZE	0	5244	137# SEIZE	0	5244
138# TRANSF	0	5244	159# BUFFER	0	823	160# TEST	0	823	161# QUEUE	0	823	162# GATE	0	823
163# ENTER	0	823	164# SEIZE	0	823	165# SEIZE	0	823	166# SEIZE	0	823	167# DEPART	0	823
168# ADVANC	0	823	169# RELEAS	0	823	170# ASSIGN	0	823	171# ADVANC	0	4115	172# LOOP	0	4115
173# PREMPT	0	823	174# RELEAS	0	823	175# RELEAS	0	823	176# ADVANC	0	823	177# RETURN	0	823
178# TEST	0	823	179# TABULT	0	589	180# ASSIGN	0	589	181# LEAVE	0	823	182# TRANSF	0	823
183# RELEAS	0	3292	184# RELEAS	0	3292	185# ADVANC	0	3292	186# SEIZE	0	3292	187# SEIZE	0	3292
188# TRANSF	0	3292	215# QUEUE	0	695	216# BUFFER	0	695	217# TEST	0	695	218# SEIZE	0	695
219# SEIZE	0	695	220# DEPART	0	695	221# ADVANC	0	695	222# ADVANC	0	696	223# PREMPT	0	696
224# ADVANC	0	696	225# RETURN	0	696	226# RELEAS	0	696	227# RELEAS	0	696	228# TRANSF	0	696
240# QUEUE	0	545	241# BUFFER	0	545	242# TEST	0	545	243# SEIZE	0	545	244# SEIZE	0	545
245# DEPART	0	545	246# ADVANC	0	545	247# ADVANC	0	545	248# ADVANC	0	545	249# PREMPT	0	545
250# ADVANC	0	545	251# RETURN	0	545	252# RELEAS	0	545	253# RELEAS	0	545	254# TRANSF	0	545
267# QUEUE	0	382	268# BUFFER	0	382	269# TEST	0	382	270# SEIZE	0	382	271# SEIZE	0	382
272# DEPART	0	382	273# ADVANC	0	382	274# ADVANC	0	382	275# PREMPT	0	382	276# ADVANC	0	382
277# RETURN	0	382	278# RELEAS	0	382	279# RELEAS	0	382	280# TRANSF	0	382	347# QUEUE	0	207
348# BUFFER	0	207	349# TEST	0	207	350# SEIZE	0	207	351# SEIZE	0	207	352# DEPART	0	207
353# ADVANC	0	207	354# ADVANC	0	207	355# PREMPT	0	207	356# ADVANC	0	207	357# RETURN	0	207
358# RELEAS	0	207	359# RELEAS	0	207	360# TRANSF	0	207	375# GENERT	0	5	376# TERM	0	5

FACILITIES

REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	12343	6.24	0.2568	0.2568	0.	A	100.00	97	0
CHANA	1383	31.89	0.1470	0.1470	0.	A	100.00	0	0
CONTA	1383	31.89	0.1470	0.1470	0.	A	100.00	0	0
CHANB	850	79.35	0.2248	0.2248	0.	A	100.00	0	0
CONTB	850	79.35	0.2248	0.2248	0.	A	100.00	0	0
MUXCH	9939	5.85	0.1938	0.1938	0.	A	100.00	0	0
TMCON	9939	5.85	0.1938	0.1938	0.	A	100.00	0	0
CHANC	207	24.73	0.0171	0.0171	0.	A	100.00	0	0
TAPCN	207	24.73	0.0171	0.0171	0.	A	100.00	0	0

STORAGES

REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	21.65	223	29132.26	0.217	0.217	0.	A	100.00	17	31
TASKS	5	0.79	589	400.50	0.157	0.157	0.	A	100.00	1	5
BUFFI	25	17.59	603	8749.23	0.703	0.703	0.	A	100.00	15	25
BUFFO	5	0.25	823	91.85	0.050	0.050	0.	A	100.00	0	4

QUEUES

REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	2	0.01	579	448	77.37	5.88	25.97	0	0
COREQ	1	0.01	588	0	0.	3.58	3.58	0	0
CPU	4	0.03	7395	6551	88.59	1.22	10.72	0	0
OTPUT	2	0.01	823	521	63.30	3.15	8.59	0	0
FHDRD	2	0.01	695	582	83.74	5.05	31.04	0	0
MHDRD	2	0.02	545	434	79.63	13.52	66.37	0	0
FHDWR	1	0.00	382	324	84.82	3.80	25.02	0	0
TAPOT	1	0.00	207	204	98.55	0.23	15.67	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	206	32043.602	37189.901	6600982.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.862
5000	0	0.	0.	100.00	0.156	-0.727
10000	128	62.14	62.14	37.86	0.312	-0.593
15000	0	0.	62.14	37.86	0.468	-0.458
20000	1	0.49	62.62	37.38	0.624	-0.324
25000	11	5.34	67.96	32.04	0.780	-0.189
30000	0	0.	67.96	32.04	0.936	-0.055
35000	11	5.34	73.30	26.70	1.092	0.079
40000	3	1.46	74.76	25.24	1.248	0.214
45000	2	0.97	75.73	24.27	1.404	0.348
50000	8	3.88	79.61	20.39	1.560	0.483
55000	1	0.49	80.10	19.90	1.716	0.617
60000	3	1.46	81.55	18.45	1.872	0.752
65000	1	0.49	82.04	17.96	2.028	0.886
70000	0	0.	82.04	17.96	2.185	1.021
75000	2	0.97	83.01	16.99	2.341	1.155
80000	1	0.49	83.50	16.50	2.497	1.290
85000	4	1.94	85.44	14.56	2.653	1.424
90000	0	0.	85.44	14.56	2.809	1.558
95000	1	0.49	85.92	14.08	2.965	1.693
100000	5	2.43	88.35	11.65	3.121	1.827
105000	6	2.91	91.26	8.74	3.277	1.962
110000	4	1.94	93.20	6.80	3.433	2.096
115000	3	1.46	94.66	5.34	3.589	2.231
120000	4	1.94	96.60	3.40	3.745	2.365
OVERFLOW	7	3.40	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 131064.000 MAXIMUM VALUE OF OVERFLOW = 138697

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	589	308.560	113.428	181742.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.720
500	551	93.55	93.55	6.45	1.620	1.688
1000	38	6.45	100.00	0.	3.241	6.096

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET                                                                610
                START       5,,,1                                                    611
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 720000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	225	2# ENTER	0	225	3# ASSIGN	0	225	4# ASSIGN	0	225	5# ASSIGN	0	225
6# PRIOR	0	225	7# QUEUE	0	225	8# BUFFER	0	225	9# TRANSF	0	225	10# GATE	0	671
11# ENTER	0	671	12# ASSIGN	0	671	13# DEPART	0	671	14# LEAVE	0	671	15# QUEUE	0	7039
16# SEIZE	0	7039	17# DEPART	0	7039	18# ASSIGN	0	7039	19# ADVANC	0	7039	20# RELEAS	0	7040
21# TRANSF	0	7040	22# TRANSF	0	6368	23# LEAVE	0	451	24# ASSIGN	0	451	25# ADVANC	3	451
26# QUEUE	0	449	27# TRANSF	0	449	28# TEST	0	220	29# LEAVE	0	220	30# LEAVE	0	220
31# TABULT	0	220	32# TERM	0	220	33# GENERT	0	306	34# PREMPT	0	306	35# ADVANC	0	306
36# RETURN	0	306	37# SEIZE	0	306	38# SEIZE	0	306	39# SEIZE	0	306	40# SEIZE	0	306
41# ADVANC	0	306	42# RELEAS	0	306	43# RELEAS	0	306	44# RELEAS	0	306	45# RELEAS	0	306
46# TERM	0	306	52# ASSIGN	0	82	53# ASSIGN	0	192	54# ASSIGN	0	192	55# ASSIGN	0	192
56# ASSIGN	0	192	57# ASSIGN	0	192	58# ASSIGN	0	192	59# ASSIGN	0	192	60# ASSIGN	0	192
61# ASSIGN	0	192	62# TRANSF	0	192	63# ASSIGN	0	935	64# LOOP	0	935	65# ASSIGN	0	189
66# ASSIGN	0	189	67# TRANSF	0	189	68# ASSIGN	0	746	69# ASSIGN	0	746	70# ASSIGN	0	746
71# TRANSF	0	746	72# ASSIGN	0	192	73# ASSIGN	0	192	74# ASSIGN	0	192	75# TRANSF	0	192
90# ASSIGN	0	457	91# ASSIGN	0	457	92# ASSIGN	0	696	93# ASSIGN	0	1393	94# ASSIGN	0	1910
95# TEST	0	1910	96# BUFFER	0	1910	97# QUEUE	0	1910	98# SEIZE	0	1910	99# DEPART	0	1910
100# ADVANC	0	1910	101# RELEAS	0	1910	102# ASSIGN	0	1910	103# TRANSF	0	1910	112# BUFFER	0	674
113# TEST	0	674	114# GATE	0	674	115# ENTER	0	674	116# SEIZE	0	674	117# SEIZE	0	674
118# PREMPT	0	674	119# DEPART	0	674	120# ADVANC	0	674	121# RETURN	0	674	122# ASSIGN	0	674
123# ADVANC	0	6687	124# LOOP	0	6687	125# QLELE	0	671	126# MARK	0	671	127# PREMPT	0	671
128# RELEAS	0	671	129# RELEAS	0	671	130# ADVANC	0	671	131# RETURN	0	671	132# TRANSF	0	671
133# RELEAS	0	6016	134# RELEAS	0	6016	135# ADVANC	18	6016	136# SEIZE	0	6013	137# SEIZE	0	6013
138# TRANSF	0	6013	159# BUFFER	0	907	160# TEST	0	907	161# QUEUE	0	907	162# GATE	0	907
163# ENTER	0	907	164# SEIZE	0	907	165# SEIZE	0	907	166# SEIZE	0	907	167# DEPART	0	907
168# ADVANC	0	907	169# RELEAS	0	907	170# ASSIGN	0	907	171# ADVANC	0	4535	172# LOOP	0	4535
173# PREMPT	0	907	174# RELEAS	0	907	175# RELEAS	0	907	176# ADVANC	0	907	177# RETURN	0	907
178# TEST	0	907	179# TABULT	0	670	180# ASSIGN	0	670	181# LEAVE	0	907	182# TRANSF	0	907
183# RELEAS	0	3628	184# RELEAS	0	3628	185# ADVANC	0	3628	186# SEIZE	0	3628	187# SEIZE	0	3628
188# TRANSF	0	3628	215# QUEUE	0	936	216# BUFFER	0	936	217# TEST	0	936	218# SEIZE	0	936
219# SEIZE	0	936	220# DEPART	0	936	221# ADVANC	0	936	222# ADVANC	0	936	223# PREMPT	0	936
224# ADVANC	0	936	225# RETURN	0	936	226# RELEAS	0	936	227# RELEAS	0	936	228# TRANSF	0	936
240# QUEUE	0	627	241# BUFFER	0	627	242# TEST	0	627	243# SEIZE	0	627	244# SEIZE	0	627
245# DEPART	0	627	246# ADVANC	1	627	247# ADVANC	0	626	248# ADVANC	0	626	249# PREMPT	0	626
250# ADVANC	0	626	251# RETURN	0	626	252# RELEAS	0	626	253# RELEAS	0	626	254# TRANSF	0	626
267# QUEUE	0	451	268# BUFFER	0	451	269# TEST	0	451	270# SEIZE	0	451	271# SEIZE	0	451
272# DEPART	0	451	273# ADVANC	0	451	274# ADVANC	0	451	275# PREMPT	0	451	276# ADVANC	0	451
277# RETURN	0	451	278# RELEAS	0	451	279# RELEAS	0	451	280# TRANSF	0	451	347# QUEUE	0	219
348# BUFFER	0	219	349# TEST	0	219	350# SEIZE	0	219	351# SEIZE	0	219	352# DEPART	0	219
353# ADVANC	0	219	354# ADVANC	0	219	355# PREMPT	0	219	356# ADVANC	0	219	357# RETURN	0	219
358# RELEAS	0	219	359# RELEAS	0	219	360# TRANSF	0	219	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	14647	6.07	0.2964	0.2964	0.	A	100.00	0	0
CHANA	1693	30.70	0.1733	0.1733	0.	A	100.00	0	0
CONTA	1693	30.70	0.1733	0.1733	0.	A	100.00	0	0
CHANB	933	82.89	0.2578	0.2578	0.	A	100.00	72	0
CONTB	933	82.89	0.2578	0.2578	0.	A	100.00	72	0
MUXCH	11222	5.79	0.2166	0.2166	0.	A	100.00	0	0
TMCON	11222	5.79	0.2166	0.2166	0.	A	100.00	0	0
CHANC	219	25.59	0.0187	0.0187	0.	A	100.00	0	0
TAPCN	219	25.59	0.0187	0.0187	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	- - AVERAGE UTILIZATION - - AVERAGE TIME/UNIT	TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	25.10	242	31114.21	0.251	0.251	0.	A	100.00	22	33
TASKS	5	0.95	672	423.70	0.190	0.190	0.	A	100.00	1	5
BUFFI	25	20.19	689	8792.40	0.808	0.808	0.	A	100.00	18	25
BUFFO	5	0.28	907	92.71	0.056	0.056	0.	A	100.00	0	4

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	5	0.19	674	449	66.62	84.96	254.49	0	0
COREQ	1	0.01	671	0	0.	3.99	3.99	0	0
CPU	5	0.05	8949	7628	85.24	1.69	11.47	0	0
OTPUT	3	0.01	907	517	57.00	4.31	10.01	0	0
FHDRD	2	0.02	936	753	80.45	5.03	25.73	0	0
MHDRD	2	0.03	627	496	79.11	16.04	76.76	0	0
FHDWR	2	0.01	451	370	82.04	4.56	25.37	0	0
TAPOT	1	0.00	219	218	99.54	0.07	16.00	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	220	34271.541	39416.311	7539739.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.869
5000	0	0.	0.	100.00	0.146	-0.743
10000	125	56.82	56.82	43.18	0.292	-0.616
15000	16	7.27	64.09	35.91	0.438	-0.489
20000	3	1.36	65.45	34.55	0.584	-0.362
25000	6	2.73	68.18	31.82	0.729	-0.235
30000	0	0.	68.18	31.82	0.875	-0.108
35000	5	2.27	70.45	29.55	1.021	0.018
40000	3	1.36	71.82	28.18	1.167	0.145
45000	0	0.	71.82	28.18	1.313	0.272
50000	2	0.91	72.73	27.27	1.459	0.399
55000	4	1.82	74.55	25.45	1.605	0.526
60000	7	3.18	77.73	22.27	1.751	0.653
65000	2	0.91	78.64	21.36	1.897	0.780
70000	2	0.91	79.55	20.45	2.043	0.906
75000	2	0.91	80.45	19.55	2.188	1.033
80000	1	0.45	80.91	19.09	2.334	1.160
85000	7	3.18	84.09	15.91	2.480	1.287
90000	4	1.82	85.91	14.09	2.626	1.414
95000	0	0.	85.91	14.09	2.772	1.541
100000	2	0.91	86.82	13.18	2.918	1.668
105000	7	3.18	90.00	10.00	3.064	1.794
110000	3	1.36	91.36	8.64	3.210	1.921
115000	3	1.36	92.73	7.27	3.356	2.048
120000	2	0.91	93.64	6.36	3.501	2.175
OVERFLOW	14	6.36	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 127639.214 MAXIMUM VALUE OF OVERFLOW = 139697

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	670	333.001	146.268	223111.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.277
500	598	89.25	89.25	10.75	1.501	1.142
1000	71	10.60	99.85	0.15	3.003	4.560
1500	1	0.15	100.00	0.	4.504	7.978

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET                                                          612
                START       5,,,1                                              613
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 1020000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	221	2# ENTER	0	221	3# ASSIGN	0	221	4# ASSIGN	0	221	5# ASSIGN	0	221
6# PRIOR	0	221	7# QUEUE	0	221	8# BUFFER	0	221	9# TRANSF	0	221	10# GATE	0	722
11# ENTER	0	722	12# ASSIGN	0	722	13# DEPART	0	722	14# LEAVE	0	722	15# QUEUE	0	7124
16# SEIZE	0	7124	17# DEPART	0	7124	18# ASSIGN	0	7124	19# ADVANC	0	7124	20# RELEAS	0	7124
21# TRANSF	0	7124	22# TRANSF	0	6402	23# LEAVE	0	503	24# ASSIGN	0	503	25# ADVANC	4	503
26# QUEUE	0	502	27# TRANSF	0	502	28# TEST	0	220	29# LEAVE	0	220	30# LEAVE	0	220
31# TABULT	0	220	32# TERM	0	220	33# GENERT	0	306	34# PREMPT	0	306	35# ADVANC	0	306
36# RETURN	0	306	37# SEIZE	0	306	38# SEIZE	0	306	39# SEIZE	0	306	40# SEIZE	0	306
41# ADVANC	0	306	42# RELEAS	0	306	43# RELEAS	0	306	44# RELEAS	0	306	45# RELEAS	0	306
46# TERM	0	306	52# ASSIGN	0	88	53# ASSIGN	0	176	54# ASSIGN	0	176	55# ASSIGN	0	176
56# ASSIGN	0	176	57# ASSIGN	0	176	58# ASSIGN	0	176	59# ASSIGN	0	176	60# ASSIGN	0	176
61# ASSIGN	0	176	62# TRANSF	0	176	63# ASSIGN	0	851	64# LOOP	0	851	65# ASSIGN	0	177
66# ASSIGN	0	177	67# TRANSF	0	177	68# ASSIGN	0	674	69# ASSIGN	0	674	70# ASSIGN	0	674
71# TRANSF	0	674	72# ASSIGN	0	176	73# ASSIGN	0	176	74# ASSIGN	0	176	75# TRANSF	0	176
90# ASSIGN	0	546	91# ASSIGN	0	546	92# ASSIGN	0	874	93# ASSIGN	0	1399	94# ASSIGN	0	1973
95# TEST	0	1973	96# BUFFER	0	1973	97# QUEUE	0	1973	98# SEIZE	0	1973	99# DEPART	0	1973
100# ADVANC	0	1973	101# RELEAS	0	1973	102# ASSIGN	0	1973	103# TRANSF	0	1973	112# BUFFER	0	723
113# TEST	0	723	114# GATE	0	723	115# ENTER	0	723	116# SEIZE	0	723	117# SEIZE	0	723
118# PREMPT	0	723	119# DEPART	0	723	120# ADVANC	0	723	121# RETURN	0	723	122# ASSIGN	0	723
123# ADVANC	0	7262	124# LOOP	0	7262	125# QUEUE	0	722	126# MARK	0	722	127# PREMPT	0	722
128# RELEAS	0	722	129# RELEAS	0	722	130# ADVANC	0	722	131# RETURN	0	722	132# TRANSF	0	722
133# RELEAS	0	6540	134# RELEAS	0	6540	135# ADVANC	19	6540	136# SEIZE	0	6539	137# SEIZE	0	6539
138# TRANSF	0	6539	159# BUFFER	0	990	160# TEST	0	990	161# QUEUE	0	990	162# GATE	0	990
163# ENTER	0	990	164# SEIZE	0	990	165# SEIZE	0	990	166# SEIZE	0	990	167# DEPART	0	990
168# ADVANC	0	990	169# RELEAS	0	990	170# ASSIGN	0	990	171# ADVANC	0	4950	172# LOOP	0	4950
173# PREMPT	0	990	174# RELEAS	0	990	175# RELEAS	0	990	176# ADVANC	0	990	177# RETURN	0	990
178# TEST	0	990	179# TABULT	0	723	180# ASSIGN	0	723	181# LEAVE	0	990	182# TRANSF	0	990
183# RELEAS	0	3960	184# RELEAS	0	3960	185# ADVANC	0	3960	186# SEIZE	0	3960	187# SEIZE	0	3960
188# TRANSF	0	3960	215# QUEUE	0	850	216# BUFFER	0	850	217# TEST	0	850	218# SEIZE	0	850
219# SEIZE	0	850	220# DEPART	0	850	221# ADVANC	0	850	222# ADVANC	0	850	223# PREMPT	0	850
224# ADVANC	0	850	225# RETURN	0	850	226# RELEAS	0	850	227# RELEAS	0	850	228# TRANSF	0	850
240# QUEUE	0	662	241# BUFFER	0	662	242# TEST	0	662	243# SEIZE	0	662	244# SEIZE	0	662
245# DEPART	0	662	246# ADVANC	0	662	247# ADVANC	0	663	248# ADVANC	0	663	249# PREMPT	0	663
250# ADVANC	0	663	251# RETURN	0	663	252# RELEAS	0	663	253# RELEAS	0	663	254# TRANSF	0	663
267# QUEUE	0	503	268# BUFFER	0	503	269# TEST	0	503	270# SEIZE	0	503	271# SEIZE	0	503
272# DEPART	0	503	273# ADVANC	0	503	274# ADVANC	0	503	275# PREMPT	0	503	276# ADVANC	0	503
277# RETURN	0	503	278# RELEAS	0	503	279# RELEAS	0	503	280# TRANSF	0	503	347# QUEUE	0	220
348# BUFFER	0	220	349# TEST	0	220	350# SEIZE	0	220	351# SEIZE	0	220	352# DEPART	0	220
353# ADVANC	0	220	354# ADVANC	0	220	355# PREMPT	0	220	356# ADVANC	0	220	357# RETURN	0	220
358# RELEAS	0	220	359# RELEAS	0	220	360# TRANSF	0	220	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	15064	6.13	0.3077	0.3077	0.	A	100.00	0	0
CHANA	1659	31.03	0.1716	0.1716	0.	A	100.00	0	0
CONTA	1659	31.03	0.1716	0.1716	0.	A	100.00	0	0
CHANB	969	82.20	0.2655	0.2655	0.	A	100.00	C	0
CONTB	969	82.20	0.2655	0.2655	0.	A	100.00	0	0
MUXCH	12212	5.79	0.2358	0.2358	0.	A	100.00	0	0
TMCON	12212	5.79	0.2358	0.2358	0.	A	100.00	0	0
CHANC	220	24.55	0.0180	0.0180	0.	A	100.00	0	0
TAPCN	220	24.55	0.0180	0.0180	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	- - AVERAGE UTILIZATION - - AVERAGE TIME/UNIT	TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	28.65	243	35369.81	C.286	0.286	0.	A	100.00	23	39
TASKS	5	1.00	723	415.86	C.200	0.200	0.	A	100.00	0	5
BUFFI	25	21.96	741	8888.95	C.878	0.878	0.	A	100.00	19	25
BUFFO	5	0.31	990	93.23	0.062	0.062	0.	A	100.00	0	4

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	11	1.54	723	283	39.14	638.54	1049.23	0	0
COREQ	1	0.01	722	0	0.	3.18	3.18	0	0
CPU	4	0.05	9097	7731	84.98	1.70	11.30	0	0
OTPUT	2	0.01	990	581	58.69	3.80	9.19	0	0
FHDRD	3	0.01	850	669	78.71	5.22	24.53	0	0
MHDRD	2	0.04	662	484	73.11	19.05	70.85	0	0
FHDWR	2	0.01	503	438	87.08	3.55	27.49	0	0
TAPOT	1	0.00	220	215	97.73	0.30	13.20	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	220	39414.527	43375.779	8671196.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.909
5000	0	0.	0.	100.00	0.127	-0.793
10000	84	38.18	38.18	61.82	0.254	-0.678
15000	47	21.36	59.55	40.45	0.381	-0.563
20000	2	0.91	60.45	39.55	0.507	-0.448
25000	10	4.55	65.00	35.00	0.634	-0.332
30000	0	0.	65.00	35.00	0.761	-0.217
35000	2	0.91	65.91	34.09	0.888	-0.102
40000	4	1.82	67.73	32.27	1.015	0.013
45000	4	1.82	69.55	30.45	1.142	0.129
50000	4	1.82	71.36	28.64	1.269	0.244
55000	3	1.36	72.73	27.27	1.395	0.359
60000	1	0.45	73.18	26.82	1.522	0.475
65000	0	0.	73.18	26.82	1.649	0.590
70000	3	1.36	74.55	25.45	1.776	0.705
75000	4	1.82	76.36	23.64	1.903	0.820
80000	0	0.	76.36	23.64	2.030	0.936
85000	5	2.27	78.64	21.36	2.157	1.051
90000	4	1.82	80.45	19.55	2.283	1.166
95000	1	0.45	80.91	19.09	2.410	1.281
100000	2	0.91	81.82	18.18	2.537	1.397
105000	8	3.64	85.45	14.55	2.664	1.512
110000	5	2.27	87.73	12.27	2.791	1.627
115000	4	1.82	89.55	10.45	2.918	1.743
120000	8	3.64	93.18	6.82	3.045	1.858
OVERFLOW	15	6.82	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 133552.666 MAXIMUM VALUE OF OVERFLOW = 148390

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	723	319.433	128.100	230950.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.494
500	663	91.70	91.70	8.30	1.565	1.410
1000	58	8.02	99.72	0.28	3.131	5.313
1500	2	0.28	100.00	0.	4.696	9.216

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET
                START       5,,,1                                          614
                                                                           615
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 1320000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	168	2# ENTER	0	168	3# ASSIGN	0	168	4# ASSIGN	0	168	5# ASSIGN	0	168
6# PRIOR	0	168	7# QUEUE	0	168	8# BUFFER	0	168	9# TRANSF	0	168	10# GATE	0	505
11# ENTER	0	505	12# ASSIGN	0	505	13# DEPART	0	505	14# LEAVE	0	505	15# QUEUE	0	5055
16# SEIZE	0	5055	17# DEPART	0	5055	18# ASSIGN	0	5055	19# ADVANC	0	5055	20# RELEAS	0	5055
21# TRANSF	0	5055	22# TRANSF	0	4550	23# LEAVE	0	329	24# ASSIGN	0	329	25# ADVANC	0	329
26# QUEUE	0	333	27# TRANSF	0	333	28# TEST	0	176	29# LEAVE	0	176	30# LEAVE	0	176
31# TABULT	0	176	32# TERM	0	176	33# GENERT	0	302	34# PREMPT	0	302	35# ADVANC	0	302
36# RETURN	0	302	37# SEIZE	0	302	38# SEIZE	0	302	39# SEIZE	0	302	40# SEIZE	0	302
41# ADVANC	0	302	42# RELEAS	0	302	43# RELEAS	0	302	44# RELEAS	0	302	45# RELEAS	0	302
46# TERM	0	302	52# ASSIGN	0	61	53# ASSIGN	0	123	54# ASSIGN	0	123	55# ASSIGN	0	123
56# ASSIGN	0	123	57# ASSIGN	0	123	58# ASSIGN	0	123	59# ASSIGN	0	123	60# ASSIGN	0	123
61# ASSIGN	0	123	62# TRANSF	0	123	63# ASSIGN	0	610	64# LOOP	0	610	65# ASSIGN	0	132
66# ASSIGN	0	132	67# TRANSF	0	132	68# ASSIGN	0	478	69# ASSIGN	0	478	70# ASSIGN	0	478
71# TRANSF	0	478	72# ASSIGN	0	123	73# ASSIGN	0	123	74# ASSIGN	0	123	75# TRANSF	0	123
90# ASSIGN	0	385	91# ASSIGN	0	385	92# ASSIGN	0	589	93# ASSIGN	0	990	94# ASSIGN	0	1396
95# TEST	0	1396	96# BUFFER	0	1396	97# QUEUE	0	1396	98# SEIZE	0	1396	99# DEPART	0	1396
100# ADVANC	0	1396	101# RELEAS	0	1396	102# ASSIGN	0	1396	103# TRANSF	0	1396	112# BUFFER	0	501
113# TEST	0	501	114# GATE	0	501	115# ENTER	0	501	116# SEIZE	0	501	117# SEIZE	0	501
118# PREMPT	0	501	119# DEPART	0	501	120# ADVANC	0	501	121# RETURN	0	501	122# ASSIGN	0	501
123# ADVANC	1	5013	124# LOOP	0	5012	125# QUEUE	0	505	126# MARK	0	505	127# PREMPT	0	505
128# RELEAS	0	505	129# RELEAS	0	505	130# ADVANC	0	505	131# RETURN	0	505	132# TRANSF	0	505
133# RELEAS	0	4507	134# RELEAS	0	4507	135# ADVANC	14	4507	136# SEIZE	0	4512	137# SEIZE	0	4512
138# TRANSF	0	4512	159# BUFFER	0	715	160# TEST	0	715	161# QUEUE	0	715	162# GATE	0	715
163# ENTER	0	715	164# SEIZE	0	715	165# SEIZE	0	715	166# SEIZE	0	715	167# DEPART	0	715
168# ADVANC	0	715	169# RELEAS	0	715	170# ASSIGN	0	715	171# ADVANC	0	3575	172# LOOP	0	3575
173# PREMPT	0	715	174# RELEAS	0	715	175# RELEAS	0	715	176# ADVANC	0	715	177# RETURN	0	715
178# TEST	0	715	179# TABULT	0	505	180# ASSIGN	0	505	181# LEAVE	0	715	182# TRANSF	0	715
183# RELEAS	0	2860	184# RELEAS	0	2860	185# ADVANC	0	2860	186# SEIZE	0	2860	187# SEIZE	0	2860
188# TRANSF	0	2860	215# QUEUE	0	610	216# BUFFER	0	610	217# TEST	0	610	218# SEIZE	0	610
219# SEIZE	0	610	220# DEPART	0	610	221# ADVANC	0	610	222# ADVANC	0	610	223# PREMPT	0	610
224# ADVANC	0	610	225# RETURN	0	610	226# RELEAS	0	610	227# RELEAS	0	610	228# TRANSF	0	610
240# QUEUE	0	468	241# BUFFER	0	468	242# TEST	0	468	243# SEIZE	0	468	244# SEIZE	0	468
245# DEPART	0	468	246# ADVANC	0	468	247# ADVANC	0	468	248# ADVANC	0	468	249# PREMPT	0	468
250# ADVANC	0	468	251# RETURN	0	468	252# RELEAS	0	468	253# RELEAS	0	468	254# TRANSF	0	468
267# QUEUE	0	329	268# BUFFER	0	329	269# TEST	0	329	270# SEIZE	0	329	271# SEIZE	0	329
272# DEPART	0	329	273# ADVANC	0	329	274# ADVANC	0	329	275# PREMPT	0	329	276# ADVANC	0	329
277# RETURN	0	329	278# RELEAS	0	329	279# RELEAS	0	329	280# TRANSF	0	329	347# QUEUE	0	176
348# BUFFER	0	176	349# TEST	0	176	350# SEIZE	0	176	351# SEIZE	0	176	352# DEPART	0	176
353# ADVANC	0	176	354# ADVANC	0	176	355# PREMPT	0	176	356# ADVANC	0	176	357# RETURN	0	176
358# RELEAS	0	176	359# RELEAS	0	176	360# TRANSF	0	176	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	10772	6.44	0.2314	0.2314	0.	A	100.00	0	0
CHANA	1241	32.96	0.1364	0.1364	0.	A	100.00	0	0
CONTA	1241	32.96	0.1364	0.1364	0.	A	100.00	0	0
CHANB	770	79.48	0.2040	0.2040	0.	A	100.00	0	0
CONTB	770	79.48	0.2040	0.2040	0.	A	100.00	0	0
MUXCH	8588	5.76	0.1650	0.1650	0.	A	100.00	63	0
TMCON	8588	5.76	0.1650	0.1650	0.	A	100.00	63	0
CHANC	176	24.64	0.0145	0.0145	0.	A	100.00	0	0
TAPCN	176	24.64	0.0145	0.0145	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	18.69	191	29359.92	0.187	0.187	0.	A	100.00	15	30
TASKS	5	0.69	505	408.35	0.137	0.137	0.	A	100.00	0	5
BUFFI	25	15.13	520	8730.88	0.605	0.605	0.	A	100.00	15	25
BUFFO	5	0.22	715	90.95	0.043	0.043	0.	A	100.00	0	3

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	3	0.02	501	388	77.45	13.63	60.44	0	0
COREQ	1	0.00	505	0	0.	2.85	2.85	0	0
CPU	4	0.03	6451	5698	88.33	1.34	11.45	0	0
OTPUT	2	0.01	715	433	60.56	3.35	8.48	0	0
FHDRD	2	0.01	610	517	84.75	3.98	26.12	0	0
MHDRD	2	0.02	468	372	79.49	13.39	65.28	0	0
FHDWR	2	0.00	329	286	86.93	3.37	25.77	0	0
TAPOT	1	0.00	176	170	96.59	0.41	12.17	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	176	33896.432	37545.978	5965772.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.903
5000	0	0.	C.	100.00	0.148	-0.770
10000	106	60.23	60.23	39.77	0.295	-0.636
15000	0	0.	60.23	39.77	0.443	-0.503
20000	0	0.	60.23	39.77	0.590	-0.370
25000	7	3.98	64.20	35.80	0.738	-0.237
30000	1	0.57	64.77	35.23	0.885	-0.104
35000	3	1.70	66.48	33.52	1.033	0.029
40000	7	3.98	70.45	29.55	1.180	0.163
45000	3	1.70	72.16	27.84	1.328	0.296
50000	11	6.25	78.41	21.59	1.475	0.429
55000	2	1.14	79.55	20.45	1.623	0.562
60000	1	0.57	80.11	19.89	1.770	0.695
65000	0	0.	80.11	19.89	1.918	0.828
70000	4	2.27	82.39	17.61	2.065	0.962
75000	1	0.57	82.95	17.05	2.213	1.095
80000	0	0.	82.95	17.05	2.360	1.228
85000	2	1.14	84.09	15.91	2.508	1.361
90000	1	0.57	84.66	15.34	2.655	1.494
95000	4	2.27	86.93	13.07	2.803	1.627
100000	3	1.70	88.64	11.36	2.950	1.761
105000	2	1.14	89.77	10.23	3.098	1.894
110000	2	1.14	90.91	9.09	3.245	2.027
115000	6	3.41	94.32	5.68	3.393	2.160
120000	2	1.14	95.45	4.55	3.540	2.293
OVERFLOW	8	4.55	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 125824.125 MAXIMUM VALUE OF OVERFLOW = 131806

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	505	311.436	118.556	157275.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.627
500	469	92.87	92.87	7.13	1.605	1.591
1000	36	7.13	100.00	0.	3.211	5.808

THE REMAINING FREQUENCIES ARE ALL ZERO

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7       FUNCTION    P2,L4                                          616
1,4/2,2/3,3/4,1                      LONG JOB BENEFIT              617
        CLEAR                                                      618
        START       2,NP                                           619
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                RESET
                START       5,,,1                                                    620
                                                                                     621
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 420000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	191	2# ENTER	0	191	3# ASSIGN	0	191	4# ASSIGN	0	191	5# ASSIGN	0	191
6# PRIOR	0	191	7# QUEUE	0	191	8# BUFFER	0	191	9# TRANSF	0	191	10# GATE	0	660
11# ENTER	0	660	12# ASSIGN	0	660	13# DEPART	C	660	14# LEAVE	0	660	15# QUEUE	0	6539
16# SEIZE	0	6539	17# DEPART	0	6539	18# ASSIGN	C	6539	19# ADVANC	1	6539	20# RELEAS	0	6538
21# TRANSF	0	6538	22# TRANSF	0	5879	23# LEAVE	0	454	24# ASSIGN	0	454	25# ADVANC	1	454
26# QUEUE	0	456	27# TRANSF	0	456	28# TEST	0	203	29# LEAVE	0	203	30# LEAVE	0	203
31# TABULT	0	203	32# TERM	0	203	33# GENERT	0	310	34# PREMPT	0	310	35# ADVANC	0	310
36# RETURN	0	310	37# SEIZE	0	310	38# SEIZE	0	310	39# SEIZE	0	310	40# SEIZE	0	310
41# ADVANC	0	310	42# RELEAS	0	310	43# RELEAS	0	310	44# RELEAS	0	310	45# RELEAS	0	310
46# TERM	0	310	52# ASSIGN	0	71	53# ASSIGN	0	145	54# ASSIGN	0	145	55# ASSIGN	0	145
56# ASSIGN	0	145	57# ASSIGN	0	145	58# ASSIGN	0	145	59# ASSIGN	0	145	60# ASSIGN	0	145
61# ASSIGN	0	145	62# TRANSF	0	145	63# ASSIGN	0	784	64# LOOP	0	784	65# ASSIGN	0	156
66# ASSIGN	0	156	67# TRANSF	0	156	68# ASSIGN	0	628	69# ASSIGN	0	628	70# ASSIGN	0	628
71# TRANSF	0	628	72# ASSIGN	0	145	73# ASSIGN	0	145	74# ASSIGN	0	145	75# TRANSF	0	145
90# ASSIGN	0	536	91# ASSIGN	0	536	92# ASSIGN	0	859	93# ASSIGN	0	1312	94# ASSIGN	0	1848
95# TEST	0	1848	96# BUFFER	0	1848	97# QLELE	0	1848	98# SEIZE	0	1848	99# DEPART	C	1848
100# ADVANC	0	1848	101# RELEAS	0	1848	102# ASSIGN	0	1848	103# TRANSF	0	1848	112# BUFFER	0	647
113# TEST	0	647	114# GATE	0	651	115# ENTER	0	651	116# SEIZE	0	651	117# SEIZE	0	651
118# PREMPT	0	651	119# DEPART	0	651	120# ADVANC	0	651	121# RETURN	0	651	122# ASSIGN	0	651
123# ADVANC	0	6542	124# LOOP	0	6542	125# QUEUE	0	660	126# MARK	0	660	127# PREMPT	0	660
128# RELEAS	0	660	129# RELEAS	0	660	130# ADVANC	0	660	131# RETURN	0	660	132# TRANSF	0	660
133# RELEAS	0	5882	134# RELEAS	0	5882	135# ADVANC	16	5882	136# SEIZE	0	5891	137# SEIZE	0	5891
138# TRANSF	0	5891	159# BUFFER	0	907	16C# TEST	C	907	161# QUEUE	0	907	162# GATE	0	907
163# ENTER	0	907	164# SEIZE	0	907	165# SEIZE	0	907	166# SEIZE	0	907	167# DEPART	0	907
168# ADVANC	0	907	169# RELEAS	0	907	170# ASSIGN	0	907	171# ADVANC	0	4531	172# LOOP	0	4531
173# PREMPT	0	906	174# RELEAS	0	906	175# RELEAS	C	906	176# ADVANC	0	906	177# RETURN	0	906
178# TEST	0	906	179# TABULT	0	658	180# ASSIGN	0	658	181# LEAVE	0	906	182# TRANSF	0	906
183# RELEAS	0	3625	184# RELEAS	0	3625	185# ADVANC	1	3625	186# SEIZE	0	3624	187# SEIZE	0	3624
188# TRANSF	0	3624	215# QUEUE	0	786	216# BUFFER	C	786	217# TEST	0	786	218# SEIZE	0	786
219# SEIZE	0	786	220# DEPART	0	786	221# ADVANC	C	786	222# ADVANC	0	786	223# PREMPT	0	786
224# ADVANC	0	786	225# RETURN	0	786	226# RELEAS	C	786	227# RELEAS	0	786	228# TRANSF	0	786
240# QUEUE	0	609	241# BUFFER	0	609	242# TEST	0	609	243# SEIZE	0	609	244# SEIZE	0	609
245# DEPART	0	609	246# ADVANC	1	609	247# ADVANC	0	608	248# ADVANC	0	608	249# PREMPT	0	608
250# ADVANC	0	608	251# RETURN	0	608	252# RELEAS	0	608	253# RELEAS	0	608	254# TRANSF	0	608
267# QUEUE	0	454	268# BUFFER	0	454	269# TEST	C	454	270# SEIZE	0	454	271# SEIZE	0	454
272# DEPART	0	454	273# ADVANC	0	454	274# ADVANC	C	454	275# PREMPT	0	454	276# ADVANC	0	454
277# RETURN	0	454	278# RELEAS	0	454	279# RELEAS	0	454	280# TRANSF	0	454	347# QUEUE	0	203
348# BUFFER	0	203	349# TEST	0	203	350# SEIZE	0	203	351# SEIZE	0	203	352# DEPART	0	203
353# ADVANC	0	203	354# ADVANC	0	203	355# PREMPT	0	203	356# ADVANC	0	203	357# RETURN	0	203
358# RELEAS	0	203	359# RELEAS	0	203	360# TRANSF	0	203	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	13872	6.27	0.2898	0.2898	0.	A	100.00	94	0
CHANA	1550	31.98	0.1653	0.1653	0.	A	100.00	0	0
CONTA	1550	31.98	0.1653	0.1653	0.	A	100.00	0	0
CHANB	919	81.97	0.2511	0.2511	0.	A	100.00	69	0
CONTB	919	81.97	0.2511	0.2511	0.	A	100.00	69	0
MUXCH	11073	5.79	0.2138	0.2138	0.	A	100.00	0	0
TMCON	11073	5.79	0.2138	0.2138	0.	A	100.00	0	0
CHANC	203	25.68	0.0174	0.0174	0.	A	100.00	0	0
TAPCN	203	25.68	0.0174	0.0174	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	24.54	223	33011.34	0.245	0.245	0.	A	100.00	20	35
TASKS	5	0.92	660	417.11	0.184	0.184	0.	A	100.00	3	5
BUFFI	25	19.76	676	8771.33	0.791	0.791	0.	A	100.00	16	25
BUFFO	5	0.28	907	91.37	0.055	0.055	0.	A	100.00	1	4

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	6	0.19	651	419	64.36	87.98	246.88	0	0
COREQ	2	0.01	660	0	0.	4.12	4.12	0	0
CPU	5	0.05	8387	7349	87.62	1.73	14.02	0	0
OTPUT	2	0.01	907	636	70.12	2.93	9.82	0	0
FHDRD	3	0.02	786	635	80.79	5.87	30.58	0	0
MHDRD	3	0.03	609	464	76.19	17.07	71.70	0	0
FHDWR	2	0.01	454	382	84.14	4.88	30.75	0	0
TAPOT	1	0.	203	203	100.00	0.	0.	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	203	37024.325	39391.417	7515938.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.940
5000	0	0.	0.	100.00	0.135	-0.813
10000	102	50.25	50.25	49.75	0.270	-0.686
15000	19	9.36	59.61	40.39	0.405	-0.559
20000	1	0.49	60.10	39.90	0.540	-0.432
25000	4	1.97	62.07	37.93	0.675	-0.305
30000	2	0.99	63.05	36.95	0.810	-0.178
35000	3	1.48	64.53	35.47	0.945	-0.051
40000	2	0.99	65.52	34.48	1.080	0.076
45000	8	3.94	69.46	30.54	1.215	0.202
50000	1	0.49	69.95	30.05	1.350	0.329
55000	3	1.48	71.43	28.57	1.486	0.456
60000	4	1.97	73.40	26.60	1.621	0.583
65000	3	1.48	74.88	25.12	1.756	0.710
70000	4	1.97	76.85	23.15	1.891	0.837
75000	6	2.96	79.80	20.20	2.026	0.964
80000	4	1.97	81.77	18.23	2.161	1.091
85000	3	1.48	83.25	16.75	2.296	1.218
90000	4	1.97	85.22	14.78	2.431	1.345
95000	3	1.48	86.70	13.30	2.566	1.472
100000	2	0.99	87.68	12.32	2.701	1.599
105000	5	2.46	90.15	9.85	2.836	1.726
110000	4	1.97	92.12	7.88	2.971	1.853
115000	2	0.99	93.10	6.90	3.106	1.980
120000	4	1.97	95.07	4.93	3.241	2.106
OVERFLOW	10	4.93	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 130036.000 MAXIMUM VALUE OF OVERFLOW = 137280

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	658	322.766	139.664	212380.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.311
500	602	91.49	91.49	8.51	1.549	1.269
1000	55	8.36	99.85	0.15	3.098	4.849
1500	1	0.15	100.00	0.	4.647	8.429

THE REMAINING FREQUENCIES ARE ALL ZERO

```
                RESET
                START       5,,,1                                                622
                                                                                 623
```

TERMINAL STATISTICS * ABSOLUTE CLOCK = 720000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	220	2# ENTER	0	220	3# ASSIGN	0	220	4# ASSIGN	0	220	5# ASSIGN	0	220
6# PRIOR	0	220	7# QUEUE	0	220	8# BUFFER	0	220	9# TRANSF	0	220	10# GATE	0	694
11# ENTER	0	694	12# ASSIGN	0	694	13# DEPART	0	694	14# LEAVE	0	694	15# QUEUE	0	7067
16# SEIZE	0	7067	17# DEPART	0	7067	18# ASSIGN	0	7067	19# ADVANC	0	7067	20# RELEAS	0	7068
21# TRANSF	0	7068	22# TRANSF	0	6373	23# LEAVE	0	482	24# ASSIGN	0	482	25# ADVANC	3	482
26# QUEUE	0	480	27# TRANSF	0	480	28# TEST	0	213	29# LEAVE	0	213	30# LEAVE	0	213
31# TABULT	0	213	32# TERM	0	213	33# GENERT	0	310	34# PREMPT	0	310	35# ADVANC	0	310
36# RETURN	0	310	37# SEIZE	0	310	38# SEIZE	0	310	39# SEIZE	0	310	40# SEIZE	0	310
41# ADVANC	0	310	42# RELEAS	0	310	43# RELEAS	0	310	44# RELEAS	0	310	45# RELEAS	0	310
46# TERM	0	310	52# ASSIGN	0	92	53# ASSIGN	0	176	54# ASSIGN	0	176	55# ASSIGN	0	176
56# ASSIGN	0	176	57# ASSIGN	0	176	58# ASSIGN	0	176	59# ASSIGN	0	176	60# ASSIGN	0	176
61# ASSIGN	0	176	62# TRANSF	0	176	63# ASSIGN	0	894	64# LOOP	0	894	65# ASSIGN	0	169
66# ASSIGN	0	169	67# TRANSF	0	169	68# ASSIGN	0	725	69# ASSIGN	0	725	70# ASSIGN	0	725
71# TRANSF	0	725	72# ASSIGN	0	176	73# ASSIGN	0	176	74# ASSIGN	0	176	75# TRANSF	0	176
90# ASSIGN	0	500	91# ASSIGN	0	500	92# ASSIGN	0	793	93# ASSIGN	0	1398	94# ASSIGN	0	1953
95# TEST	0	1953	96# BUFFER	0	1953	97# QUEUE	0	1953	98# SEIZE	0	1953	99# DEPART	0	1953
100# ADVANC	0	1953	101# RELEAS	0	1953	102# ASSIGN	0	1953	103# TRANSF	0	1953	112# BUFFER	0	700
113# TEST	0	700	114# GATE	0	700	115# ENTER	0	700	116# SEIZE	0	700	117# SEIZE	0	700
118# PREMPT	0	700	119# DEPART	0	700	120# ADVANC	0	700	121# RETURN	0	700	122# ASSIGN	0	700
123# ADVANC	0	6951	124# LOOP	0	6951	125# QUEUE	0	694	126# MARK	0	694	127# PREMPT	0	694
128# RELEAS	0	694	129# RELEAS	0	694	130# ADVANC	0	694	131# RETURN	0	694	132# TRANSF	0	694
133# RELEAS	0	6257	134# RELEAS	0	6257	135# ADVANC	22	6257	136# SEIZE	0	6251	137# SEIZE	0	6251
138# TRANSF	0	6251	159# BUFFER	0	947	160# TEST	0	947	161# QUEUE	0	947	162# GATE	0	947
163# ENTER	0	947	164# SEIZE	0	947	165# SEIZE	0	947	166# SEIZE	0	947	167# DEPART	0	947
168# ADVANC	0	947	169# RELEAS	0	947	170# ASSIGN	0	947	171# ADVANC	0	4737	172# LOOP	0	4737
173# PREMPT	0	947	174# RELEAS	0	947	175# RELEAS	0	947	176# ADVANC	0	947	177# RETURN	0	947
178# TEST	0	947	179# TABULT	0	694	180# ASSIGN	0	694	181# LEAVE	0	947	182# TRANSF	0	947
183# RELEAS	0	3790	184# RELEAS	0	3790	185# ADVANC	1	3790	186# SEIZE	0	3790	187# SEIZE	0	3790
188# TRANSF	0	3790	215# QUEUE	0	892	216# BUFFER	0	892	217# TEST	0	892	218# SEIZE	0	892
219# SEIZE	0	892	220# DEPART	0	892	221# ADVANC	0	892	222# ADVANC	0	892	223# PREMPT	0	892
224# ADVANC	0	892	225# RETURN	0	892	226# RELEAS	0	892	227# RELEAS	0	892	228# TRANSF	0	892
240# QUEUE	0	640	241# BUFFER	0	640	242# TEST	0	640	243# SEIZE	0	640	244# SEIZE	0	640
245# DEPART	0	640	246# ADVANC	1	640	247# ADVANC	0	640	248# ADVANC	0	640	249# PREMPT	0	640
250# ADVANC	0	640	251# RETURN	0	640	252# RELEAS	0	640	253# RELEAS	0	640	254# TRANSF	0	640
267# QUEUE	0	482	268# BUFFER	0	482	269# TEST	0	482	270# SEIZE	0	482	271# SEIZE	0	482
272# DEPART	0	482	273# ADVANC	0	482	274# ADVANC	0	482	275# PREMPT	0	482	276# ADVANC	0	482
277# RETURN	0	482	278# RELEAS	0	482	279# RELEAS	0	482	280# TRANSF	0	482	347# QUEUE	0	213
348# BUFFER	0	213	349# TEST	0	213	350# SEIZE	0	213	351# SEIZE	0	213	352# DEPART	0	213
353# ADVANC	0	213	354# ADVANC	0	213	355# PREMPT	0	213	356# ADVANC	0	213	357# RETURN	0	213
358# RELEAS	0	213	359# RELEAS	0	213	360# TRANSF	0	213	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	14846	6.11	0.3025	0.3025	0.	A	100.00	0	0
CHANA	1684	30.76	0.1727	0.1727	0.	A	100.00	0	0
CONTA	1684	30.76	0.1727	0.1727	0.	A	100.00	0	0
CHANB	951	81.04	0.2569	0.2569	0.	A	100.00	87	0
CONTB	951	81.04	0.2569	0.2569	0.	A	100.00	87	0
MUXCH	11688	5.78	0.2252	0.2252	0.	A	100.00	0	0
TMCON	11688	5.78	0.2252	0.2252	0.	A	100.00	0	0
CHANC	213	25.28	0.0179	0.0179	0.	A	100.00	0	0
TAPCN	213	25.28	0.0179	0.0179	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	27.92	240	34906.23	0.279	0.279	0.	A	100.00	27	45
TASKS	5	0.96	697	413.67	0.192	0.192	0.	A	100.00	2	5
BUFFI	25	21.00	716	8800.59	0.840	0.840	0.	A	100.00	22	25
BUFFO	5	0.29	948	91.18	0.058	0.058	0.	A	100.00	1	3

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	17	1.94	700	329	47.00	831.29	1568.47	0	0
COREQ	1	0.01	694	0	C.	3.65	3.65	0	0
CPU	5	0.06	9020	79C3	87.62	1.87	15.07	0	0
OTPUT	2	0.01	947	637	67.27	3.14	9.59	0	0
FHDRD	2	0.02	892	715	80.16	5.27	26.57	0	0
MHDRD	3	0.03	640	490	76.56	14.82	63.22	0	0
FHDWR	2	0.01	482	411	85.27	3.45	23.41	0	0
TAPOT	1	0.00	213	211	99.06	0.18	19.00	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	213	39065.896	39066.745	8321036.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-1.000
5000	0	0.	0.	100.00	0.128	-0.872
10000	79	37.09	37.09	62.91	0.256	-0.744
15000	28	13.15	50.23	49.77	0.384	-0.616
20000	6	2.82	53.05	46.95	0.512	-0.488
25000	7	3.29	56.34	43.66	0.640	-0.360
30000	7	3.29	59.62	40.38	0.768	-0.232
35000	8	3.76	63.38	36.62	0.896	-0.104
40000	8	3.76	67.14	32.86	1.024	0.024
45000	2	0.94	68.08	31.92	1.152	0.152
50000	4	1.88	69.95	30.05	1.280	0.280
55000	2	0.94	70.89	29.11	1.408	0.408
60000	6	2.82	73.71	26.29	1.536	0.536
65000	5	2.35	76.06	23.94	1.664	0.664
70000	3	1.41	77.46	22.54	1.792	0.792
75000	1	0.47	77.93	22.07	1.920	0.920
80000	5	2.35	80.28	19.72	2.048	1.048
85000	5	2.35	82.63	17.37	2.176	1.176
90000	2	0.94	83.57	16.43	2.304	1.304
95000	6	2.82	86.38	13.62	2.432	1.432
100000	2	0.94	87.32	12.68	2.560	1.560
105000	4	1.88	89.20	10.80	2.688	1.688
110000	4	1.88	91.08	8.92	2.816	1.816
115000	4	1.88	92.96	7.04	2.944	1.944
120000	3	1.41	94.37	5.63	3.072	2.072
OVERFLOW	12	5.63	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 129666.916 MAXIMUM VALUE OF OVERFLOW = 137460

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	694	322.455	152.360	223784.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.116
500	628	90.49	90.49	9.51	1.551	1.165
1000	63	9.08	99.57	0.43	3.101	4.447
1500	3	0.43	100.00	0.	4.652	7.729

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET                                                    624
                START       5,,,1                                        625
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* TERMINAL STATISTICS * ABSOLUTE CLOCK = 1020000 RELATIVE CLOCK = 300000 *

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BLOCK COUNTS
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	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	196	2# ENTER	0	196	3# ASSIGN	0	196	4# ASSIGN	0	196	5# ASSIGN	0	196
6# PRIOR	0	196	7# QUEUE	0	196	8# BUFFER	0	196	9# TRANSF	0	196	10# GATE	0	636
11# ENTER	0	636	12# ASSIGN	0	636	13# DEPART	0	636	14# LEAVE	0	636	15# QUEUE	0	6493
16# SEIZE	0	6493	17# DEPART	0	6493	18# ASSIGN	0	6493	19# ADVANC	0	6493	20# RELEAS	0	6493
21# TRANSF	0	6493	22# TRANSF	0	5857	23# LEAVE	0	435	24# ASSIGN	0	435	25# ADVANC	4	435
26# QUEUE	0	434	27# TRANSF	0	434	28# TEST	0	202	29# LEAVE	0	202	30# LEAVE	0	202
31# TABULT	0	202	32# TERM	0	202	33# GENERT	0	302	34# PREMPT	0	302	35# ADVANC	0	302
36# RETURN	0	302	37# SEIZE	0	302	38# SEIZE	0	302	39# SEIZE	0	302	40# SEIZE	0	302
41# ADVANC	0	302	42# RELEAS	0	302	43# RELEAS	0	302	44# RELEAS	0	302	45# RELEAS	0	302
46# TERM	0	302	52# ASSIGN	0	70	53# ASSIGN	0	151	54# ASSIGN	0	151	55# ASSIGN	0	151
56# ASSIGN	0	151	57# ASSIGN	0	151	58# ASSIGN	0	151	59# ASSIGN	0	151	60# ASSIGN	0	151
61# ASSIGN	0	151	62# TRANSF	0	151	63# ASSIGN	0	829	64# LOOP	0	829	65# ASSIGN	0	156
66# ASSIGN	0	156	67# TRANSF	0	156	68# ASSIGN	0	673	69# ASSIGN	0	673	70# ASSIGN	0	673
71# TRANSF	0	673	72# ASSIGN	0	151	73# ASSIGN	0	151	74# ASSIGN	0	151	75# TRANSF	0	151
90# ASSIGN	0	466	91# ASSIGN	0	466	92# ASSIGN	0	724	93# ASSIGN	0	1290	94# ASSIGN	0	1803
95# TEST	0	1803	96# BUFFER	0	1803	97# QUEUE	0	1803	98# SEIZE	0	1803	99# DEPART	0	1803
100# ADVANC	0	1803	101# RELEAS	0	1803	102# ASSIGN	0	1803	103# TRANSF	0	1803	112# BUFFER	0	630
113# TEST	0	630	114# GATE	0	630	115# ENTER	0	630	116# SEIZE	0	630	117# SEIZE	0	630
118# PREMPT	0	630	119# DEPART	0	630	120# ADVANC	0	630	121# RETURN	0	630	122# ASSIGN	0	630
123# ADVANC	0	6335	124# LOOP	0	6335	125# QUEUE	0	636	126# MARK	0	636	127# PREMPT	0	636
128# RELEAS	0	636	129# RELEAS	0	636	130# ADVANC	0	636	131# RETURN	0	636	132# TRANSF	0	636
133# RELEAS	0	5699	134# RELEAS	0	5699	135# ADVANC	16	5699	136# SEIZE	0	5705	137# SEIZE	0	5705
138# TRANSF	0	5705	159# BUFFER	0	862	160# TEST	0	862	161# QUEUE	0	862	162# GATE	0	862
163# ENTER	0	862	164# SEIZE	0	862	165# SEIZE	0	862	166# SEIZE	0	862	167# DEPART	0	862
168# ADVANC	0	862	169# RELEAS	0	862	170# ASSIGN	0	862	171# ADVANC	1	4309	172# LOOP	0	4308
173# PREMPT	0	862	174# RELEAS	0	862	175# RELEAS	0	862	176# ADVANC	0	862	177# RETURN	0	862
178# TEST	0	862	179# TABULT	0	638	180# ASSIGN	0	638	181# LEAVE	0	862	182# TRANSF	0	862
183# RELEAS	0	3446	184# RELEAS	0	3446	185# ADVANC	0	3446	186# SEIZE	0	3447	187# SEIZE	0	3447
188# TRANSF	0	3447	215# QUEUE	0	829	216# BUFFER	0	829	217# TEST	0	829	218# SEIZE	0	829
219# SEIZE	0	829	220# DEPART	0	829	221# ADVANC	0	829	222# ADVANC	0	829	223# PREMPT	0	829
224# ADVANC	0	829	225# RETURN	0	829	226# RELEAS	0	829	227# RELEAS	0	829	228# TRANSF	0	829
240# QUEUE	0	594	241# BUFFER	0	594	242# TEST	0	594	243# SEIZE	0	594	244# SEIZE	0	594
245# DEPART	0	594	246# ADVANC	0	594	247# ADVANC	0	595	248# ADVANC	0	595	249# PREMPT	0	595
250# ADVANC	0	595	251# RETURN	0	595	252# RELEAS	0	595	253# RELEAS	0	595	254# TRANSF	0	595
267# QUEUE	0	435	268# BUFFER	0	435	269# TEST	0	435	270# SEIZE	0	435	271# SEIZE	0	435
272# DEPART	0	435	273# ADVANC	0	435	274# ADVANC	0	435	275# PREMPT	0	435	276# ADVANC	0	435
277# RETURN	0	435	278# RELEAS	0	435	279# RELEAS	0	435	280# TRANSF	0	435	347# QUEUE	0	202
348# BUFFER	0	202	349# TEST	0	202	350# SEIZE	0	202	351# SEIZE	0	202	352# DEPART	0	202
353# ADVANC	0	202	354# ADVANC	0	202	355# PREMPT	0	202	356# ADVANC	0	202	357# RETURN	0	202
358# RELEAS	0	202	359# RELEAS	0	202	360# TRANSF	0	202	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
****

REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	13649	6.17	0.2806	0.2806	0.	A	100.00	0	0
CHANA	1566	31.26	0.1632	0.1632	0.	A	100.00	0	0
CONTA	1566	31.26	0.1632	0.1632	0.	A	100.00	0	0
CHANB	897	81.56	0.2439	0.2439	0.	A	100.00	0	0
CONTB	897	81.56	0.2439	0.2439	0.	A	100.00	0	0
MUXCH	10644	5.82	0.2066	0.2066	0.	A	100.00	93	0
TMCON	10644	5.82	0.2066	0.2066	0.	A	100.00	93	0
CHANC	202	26.07	0.0176	0.0176	0.	A	100.00	0	0
TAPCN	202	26.07	0.0176	0.0176	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	- - AVERAGE UTILIZATION - - AVERAGE TIME/UNIT	TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	23.93	223	32199.22	0.239	0.239	0.	A	100.00	21	36
TASKS	5	0.88	638	413.41	0.176	0.176	0.	A	100.00	1	5
BUFFI	25	19.14	652	8807.91	0.766	0.766	0.	A	100.00	16	25
BUFFO	5	0.26	863	91.35	0.053	0.053	0.	A	100.00	1	3

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	8	0.17	630	417	66.19	80.12	236.96	0	0
COREQ	1	0.01	636	0	0.	3.89	3.89	0	0
CPU	5	0.05	8296	7348	88.57	1.76	15.39	0	0
OTPUT	2	0.01	862	609	70.65	2.87	9.78	0	0
FHDRD	2	0.01	829	659	79.49	4.81	23.46	0	0
MHDRD	2	0.03	594	456	76.77	14.13	60.81	0	0
FHDWR	2	0.00	435	368	84.60	3.29	21.39	0	0
TAPOT	1	0.00	202	200	99.01	0.13	13.00	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	202	36516.812	41649.111	7376396.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.877
5000	0	0.	0.	100.00	0.137	-0.757
10000	113	55.94	55.94	44.06	0.274	-0.637
15000	15	7.43	63.37	36.63	0.411	-0.517
20000	1	0.50	63.86	36.14	0.548	-0.397
25000	4	1.98	65.84	34.16	0.685	-0.277
30000	0	0.	65.84	34.16	0.822	-0.156
35000	8	3.96	69.80	30.20	0.958	-0.036
40000	2	0.99	70.79	29.21	1.095	0.084
45000	0	0.	70.79	29.21	1.232	0.204
50000	4	1.98	72.77	27.23	1.369	0.324
55000	2	0.99	73.76	26.24	1.506	0.444
60000	3	1.49	75.25	24.75	1.643	0.564
65000	1	0.50	75.74	24.26	1.780	0.684
70000	1	0.50	76.24	23.76	1.917	0.804
75000	5	2.48	78.71	21.29	2.054	0.924
80000	1	0.50	79.21	20.79	2.191	1.044
85000	1	0.50	79.70	20.30	2.328	1.164
90000	4	1.98	81.68	18.32	2.465	1.284
95000	4	1.98	83.66	16.34	2.602	1.404
100000	6	2.97	86.63	13.37	2.738	1.524
105000	2	0.99	87.62	12.38	2.875	1.644
110000	5	2.48	90.10	9.90	3.012	1.764
115000	3	1.49	91.58	8.42	3.149	1.884
120000	2	0.99	92.57	7.43	3.286	2.004
OVERFLOW	15	7.43	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 130164.800 MAXIMUM VALUE OF OVERFLOW = 143269

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	638	323.824	146.079	206600.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.217
500	580	90.91	90.91	9.09	1.544	1.206
1000	55	8.62	99.53	0.47	3.088	4.629
1500	3	0.47	100.00	0.	4.632	8.052

THE REMAINING FREQUENCIES ARE ALL ZERO

```
                RESET                                                                626
                START       5,,,1                                                    627
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* TERMINAL STATISTICS * ABSOLUTE CLOCK = 1320000 RELATIVE CLOCK = 300000

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****
BLOCK COUNTS
****

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	197	2# ENTER	0	197	3# ASSIGN	0	197	4# ASSIGN	0	197	5# ASSIGN	0	197
6# PRIOR	0	197	7# QUEUE	0	197	8# BUFFER	0	197	9# TRANSF	0	197	10# GATE	0	549
11# ENTER	0	549	12# ASSIGN	0	549	13# DEPART	0	549	14# LEAVE	0	549	15# QUEUE	0	5598
16# SEIZE	0	5598	17# DEPART	0	5598	18# ASSIGN	0	5598	19# ADVANC	1	5598	20# RELEAS	0	5597
21# TRANSF	0	5597	22# TRANSF	0	5049	23# LEAVE	0	348	24# ASSIGN	0	348	25# ADVANC	5	348
26# QUEUE	0	347	27# TRANSF	0	347	28# TEST	0	200	29# LEAVE	0	200	30# LEAVE	0	200
31# TABULT	0	200	32# TERM	0	200	33# GENERT	0	294	34# PREMPT	0	294	35# ADVANC	0	294
36# RETURN	0	294	37# SEIZE	0	294	38# SEIZE	0	294	39# SEIZE	0	294	40# SEIZE	0	294
41# ADVANC	0	294	42# RELEAS	0	294	43# RELEAS	0	294	44# RELEAS	0	294	45# RELEAS	0	294
46# TERM	0	294	52# ASSIGN	0	64	53# ASSIGN	0	144	54# ASSIGN	0	144	55# ASSIGN	0	144
56# ASSIGN	0	144	57# ASSIGN	0	144	58# ASSIGN	0	144	59# ASSIGN	0	144	60# ASSIGN	0	144
61# ASSIGN	0	144	62# TRANSF	0	144	63# ASSIGN	0	703	64# LOOP	0	703	65# ASSIGN	0	146
66# ASSIGN	0	146	67# TRANSF	0	146	68# ASSIGN	0	557	69# ASSIGN	0	557	70# ASSIGN	0	557
71# TRANSF	0	557	72# ASSIGN	0	144	73# ASSIGN	0	144	74# ASSIGN	0	144	75# TRANSF	0	144
90# ASSIGN	0	418	91# ASSIGN	0	418	92# ASSIGN	0	634	93# ASSIGN	0	1118	94# ASSIGN	0	1550
95# TEST	0	1550	96# BUFFER	0	1550	97# QUEUE	0	1550	98# SEIZE	0	1550	99# DEPART	0	1550
100# ADVANC	0	1550	101# RELEAS	0	1550	102# ASSIGN	0	1550	103# TRANSF	0	1550	112# BUFFER	0	544
113# TEST	0	544	114# GATE	0	544	115# ENTER	0	544	116# SEIZE	0	544	117# SEIZE	0	544
118# PREMPT	0	544	119# DEPART	0	544	120# ADVANC	0	544	121# RETURN	0	544	122# ASSIGN	0	544
123# ADVANC	0	5472	124# LOOP	0	5472	125# QUEUE	0	549	126# MARK	0	549	127# PREMPT	0	549
128# RELEAS	0	549	129# RELEAS	0	549	130# ADVANC	0	549	131# RETURN	0	549	132# TRANSF	0	549
133# RELEAS	0	4923	134# RELEAS	0	4923	135# ADVANC	11	4923	136# SEIZE	0	4928	137# SEIZE	0	4928
138# TRANSF	0	4928	159# BUFFER	0	745	160# TEST	0	745	161# QUEUE	0	745	162# GATE	0	745
163# ENTER	0	745	164# SEIZE	0	745	165# SEIZE	0	745	166# SEIZE	0	745	167# DEPART	0	745
168# ADVANC	0	745	169# RELEAS	0	745	170# ASSIGN	0	745	171# ADVANC	0	3728	172# LOOP	0	3729
173# PREMPT	0	746	174# RELEAS	0	746	175# RELEAS	0	746	176# ADVANC	0	746	177# RETURN	0	746
178# TEST	0	746	179# TABULT	0	547	180# ASSIGN	0	547	181# LEAVE	0	746	182# TRANSF	0	746
183# RELEAS	0	2983	184# RELEAS	0	2983	185# ADVANC	0	2983	186# SEIZE	0	2983	187# SEIZE	0	2983
188# TRANSF	0	2983	215# QUEUE	0	704	216# BUFFER	0	704	217# TEST	0	704	218# SEIZE	0	704
219# SEIZE	0	704	220# DEPART	0	704	221# ADVANC	1	704	222# ADVANC	0	703	223# PREMPT	0	703
224# ADVANC	0	703	225# RETURN	0	703	226# RELEAS	0	703	227# RELEAS	0	703	228# TRANSF	0	703
240# QUEUE	0	511	241# BUFFER	0	511	242# TEST	0	511	243# SEIZE	0	511	244# SEIZE	0	511
245# DEPART	0	511	246# ADVANC	0	511	247# ADVANC	0	511	248# ADVANC	0	511	249# PREMPT	0	511
250# ADVANC	0	511	251# RETURN	0	511	252# RELEAS	0	511	253# RELEAS	0	511	254# TRANSF	0	511
267# QUEUE	0	348	268# BUFFER	0	348	269# TEST	0	348	270# SEIZE	0	348	271# SEIZE	0	348
272# DEPART	0	348	273# ADVANC	0	348	274# ADVANC	0	348	275# PREMPT	0	348	276# ADVANC	0	348
277# RETURN	0	348	278# RELEAS	0	348	279# RELEAS	0	348	280# TRANSF	0	348	347# QUEUE	0	200
348# BUFFER	0	200	349# TEST	0	200	350# SEIZE	0	200	351# SEIZE	0	200	352# DEPART	0	200
353# ADVANC	0	200	354# ADVANC	0	200	355# PREMPT	0	200	356# ADVANC	0	200	357# RETURN	0	200
358# RELEAS	0	200	359# RELEAS	0	200	360# TRANSF	0	200	375# GENERT	0	5	376# TERM	0	5

****
FACILITIES
****

REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	11788	6.31	0.2478	0.2478	0.	A	100.00	77	0
CHANA	1346	31.94	0.1433	0.1433	0.	A	100.00	81	0
CONTA	1346	31.94	0.1433	0.1433	0.	A	100.00	81	0
CHANB	805	79.74	0.2140	0.2140	0.	A	100.00	0	0
CONTB	805	79.74	0.2140	0.2140	0.	A	100.00	0	0
MUXCH	9201	5.76	0.1767	0.1767	0.	A	100.00	0	0
TMCON	9201	5.76	0.1767	0.1767	0.	A	100.00	0	0
CHANC	200	24.59	0.0164	0.0164	0.	A	100.00	0	0
TAPCN	200	24.59	0.0164	0.0164	0.	A	100.00	0	0

****
STORAGES
****

REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	20.18	218	27764.27	0.202	0.202	0.	A	100.00	18	29
TASKS	5	0.74	550	402.79	0.148	0.148	0.	A	100.00	2	5
BUFFI	25	16.53	560	8856.41	0.661	0.661	0.	A	100.00	11	25
BUFFO	5	0.22	746	89.88	0.045	0.045	0.	A	100.00	0	4

****
QUEUES
****

REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	2	0.00	544	433	79.60	1.66	8.15	0	0
COREQ	1	0.01	549	0	0.	3.17	3.17	0	0
CPU	5	0.03	7148	6495	90.86	1.19	12.98	0	0
OTPUT	2	0.01	745	570	76.51	2.26	9.63	0	0
FHDRD	2	0.01	704	603	85.65	3.91	27.27	0	0
MHDRD	3	0.02	511	401	78.47	14.25	66.22	0	0
FHDWR	2	0.00	348	295	84.77	4.18	27.43	0	0
TAPOT	1	0.00	200	199	99.50	0.03	5.00	0	0

****
TABLES
****

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	200	30578.785	35935.301	6115757.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.851
5000	0	0.	0.	100.00	0.164	-0.712
10000	133	66.50	66.50	33.50	0.327	-0.573
15000	0	0.	66.50	33.50	0.491	-0.434
20000	2	1.00	67.50	32.50	0.654	-0.294
25000	4	2.00	69.50	30.50	0.818	-0.155
30000	0	0.	69.50	30.50	0.981	-0.016
35000	12	6.00	75.50	24.50	1.145	0.123
40000	1	0.50	76.00	24.00	1.308	0.262
45000	1	0.50	76.50	23.50	1.472	0.401
50000	1	0.50	77.00	23.00	1.635	0.540
55000	0	0.	77.00	23.00	1.799	0.680
60000	7	3.50	80.50	19.50	1.962	0.819
65000	0	0.	80.50	19.50	2.126	0.958
70000	1	0.50	81.00	19.00	2.289	1.097
75000	5	2.50	83.50	16.50	2.453	1.236
80000	3	1.50	85.00	15.00	2.616	1.375
85000	6	3.00	88.00	12.00	2.780	1.514
90000	2	1.00	89.00	11.00	2.943	1.654
95000	5	2.50	91.50	8.50	3.107	1.793
100000	1	0.50	92.00	8.00	3.270	1.932
105000	1	0.50	92.50	7.50	3.434	2.071
110000	4	2.00	94.50	5.50	3.597	2.210
115000	1	0.50	95.00	5.00	3.761	2.349
120000	3	1.50	96.50	3.50	3.924	2.488
OVERFLOW	7	3.50	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 129982.000 MAXIMUM VALUE OF OVERFLOW = 137534

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	547	315.868	128.524	172780.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.458
500	492	89.95	89.95	10.05	1.583	1.433
1000	55	10.05	100.00	0.	3.166	5.323

THE REMAINING FREQUENCIES ARE ALL ZERO

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7       FUNCTION    P2,L4                                          628
1,1/2,3/3,2/4,4                      SHORT JOB BENEFIT             629
        CLEAR                                                      630
        START       2,NP                                           631
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                RESET
                START       5,,,1                                                632
                                                                                 633
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* TERMINAL STATISTICS * ABSOLUTE CLOCK = 420000 RELATIVE CLOCK = 300000

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BLOCK COUNTS
****

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	212	2# ENTER	0	212	3# ASSIGN	0	212	4# ASSIGN	0	212	5# ASSIGN	0	212
6# PRIOR	0	212	7# QUEUE	0	212	8# BUFFER	0	212	9# TRANSF	0	212	10# GATE	0	709
11# ENTER	0	709	12# ASSIGN	0	709	13# DEPART	0	709	14# LEAVE	0	709	15# QUEUE	0	7155
16# SEIZE	0	7155	17# DEPART	0	7155	18# ASSIGN	0	7155	19# ADVANC	0	7155	20# RELEAS	0	7155
21# TRANSF	0	7155	22# TRANSF	0	6446	23# LEAVE	0	497	24# ASSIGN	0	497	25# ADVANC	5	497
26# QUEUE	0	494	27# TRANSF	0	494	28# TEST	C	211	29# LEAVE	0	211	30# LEAVE	0	211
31# TABULT	0	211	32# TERM	0	211	33# GENERT	0	311	34# PREMPT	0	311	35# ADVANC	0	311
36# RETURN	0	311	37# SEIZE	0	311	38# SEIZE	0	311	39# SEIZE	0	311	40# SEIZE	0	311
41# ADVANC	0	311	42# RELEAS	0	311	43# RELEAS	0	311	44# RELEAS	0	311	45# RELEAS	0	311
46# TERM	0	311	52# ASSIGN	0	89	53# ASSIGN	0	182	54# ASSIGN	0	182	55# ASSIGN	0	182
56# ASSIGN	0	182	57# ASSIGN	0	182	58# ASSIGN	0	182	59# ASSIGN	0	182	60# ASSIGN	0	182
61# ASSIGN	0	182	62# TRANSF	0	182	63# ASSIGN	C	901	64# LOOP	0	901	65# ASSIGN	0	179
66# ASSIGN	0	179	67# TRANSF	0	179	68# ASSIGN	0	722	69# ASSIGN	0	722	70# ASSIGN	0	722
71# TRANSF	0	722	72# ASSIGN	0	182	73# ASSIGN	0	182	74# ASSIGN	0	182	75# TRANSF	0	182
90# ASSIGN	0	473	91# ASSIGN	0	473	92# ASSIGN	0	734	93# ASSIGN	0	1374	94# ASSIGN	0	1943
95# TEST	0	1943	96# BUFFER	0	1943	97# QUEUE	0	1943	98# SEIZE	0	1943	99# DEPART	0	1943
100# ADVANC	0	1943	101# RELEAS	0	1943	102# ASSIGN	0	1943	103# TRANSF	0	1943	112# BUFFER	0	706
113# TEST	0	706	114# GATE	0	706	115# ENTER	0	706	116# SEIZE	0	706	117# SEIZE	0	706
118# PREMPT	0	706	119# DEPART	0	706	120# ADVANC	0	706	121# RETURN	0	706	122# ASSIGN	0	706
123# ADVANC	0	7065	124# LOOP	0	7065	125# QUEUE	0	709	126# MARK	0	709	127# PREMPT	0	709
128# RELEAS	0	709	129# RELEAS	0	709	130# ADVANC	0	709	131# RETURN	0	709	132# TRANSF	0	709
133# RELEAS	0	6356	134# RELEAS	0	6356	135# ADVANC	16	6356	136# SEIZE	0	6359	137# SEIZE	0	6359
138# TRANSF	0	6359	159# BUFFER	0	967	160# TEST	0	967	161# QUEUE	0	967	162# GATE	0	967
163# ENTER	0	967	164# SEIZE	0	967	165# SEIZE	0	967	166# SEIZE	0	967	167# DEPART	0	967
168# ADVANC	0	967	169# RELEAS	0	967	170# ASSIGN	C	967	171# ADVANC	0	4834	172# LOOP	C	4834
173# PREMPT	0	966	174# RELEAS	0	966	175# RELEAS	0	966	176# ADVANC	0	966	177# RETURN	0	966
178# TEST	0	966	179# TABULT	0	708	180# ASSIGN	0	708	181# LEAVE	0	966	182# TRANSF	0	966
183# RELEAS	0	3868	184# RELEAS	0	3868	185# ADVANC	1	3868	186# SEIZE	0	3867	187# SEIZE	0	3867
188# TRANSF	0	3867	215# QUEUE	0	902	216# BUFFER	0	902	217# TEST	0	902	218# SEIZE	0	902
219# SEIZE	0	902	220# DEPART	0	902	221# ADVANC	0	902	222# ADVANC	0	902	223# PREMPT	0	902
224# ADVANC	0	902	225# RETURN	0	902	226# RELEAS	0	902	227# RELEAS	0	902	228# TRANSF	0	902
240# QUEUE	0	662	241# BUFFER	0	662	242# TEST	C	662	243# SEIZE	0	662	244# SEIZE	0	662
245# DEPART	0	662	246# ADVANC	0	662	247# ADVANC	0	662	248# ADVANC	0	662	249# PREMPT	0	662
250# ADVANC	0	662	251# RETURN	0	662	252# RELEAS	0	662	253# RELEAS	0	662	254# TRANSF	0	662
267# QUEUE	0	497	268# BUFFER	0	497	269# TEST	0	497	270# SEIZE	0	497	271# SEIZE	0	497
272# DEPART	0	497	273# ADVANC	0	497	274# ADVANC	0	497	275# PREMPT	0	497	276# ADVANC	0	497
277# RETURN	0	497	278# RELEAS	0	497	279# RELEAS	C	497	280# TRANSF	0	497	347# QUEUE	0	211
348# BUFFER	0	211	349# TEST	0	211	350# SEIZE	0	211	351# SEIZE	0	211	352# DEPART	0	211
353# ADVANC	0	211	354# ADVANC	0	211	355# PREMPT	0	211	356# ADVANC	0	211	357# RETURN	0	211
358# RELEAS	0	211	359# RELEAS	0	211	360# TRANSF	0	211	375# GENERT	0	5	376# TERM	0	5

****
FACILITIES
****

REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	15029	6.05	0.3028	0.3028	0.	A	100.00	0	0
CHANA	1710	31.16	0.1776	0.1776	0.	A	100.00	0	0
CONTA	1710	31.16	0.1776	0.1776	0.	A	100.00	0	0
CHANB	973	84.74	0.2748	0.2748	0.	A	100.00	0	0
CONTB	973	84.74	0.2748	0.2748	0.	A	100.00	0	0
MUXCH	11899	5.77	0.2287	0.2287	0.	A	100.00	0	0
TMCON	11899	5.77	0.2287	0.2287	0.	A	100.00	0	0
CHANC	211	25.65	0.0180	0.0180	0.	A	100.00	0	0
TAPCN	211	25.65	0.0180	0.0180	0.	A	100.00	0	0

****
STORAGES
****

REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	26.77	233	34470.84	0.268	0.268	0.	A	100.00	22	35
TASKS	5	0.98	709	416.63	0.197	0.197	0.	A	100.00	1	5
BUFFI	25	21.36	725	8838.18	0.854	0.854	0.	A	100.00	16	25
BUFFO	5	0.30	967	91.73	0.059	0.059	0.	A	100.00	1	4

****
QUEUES
****

REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	5	0.27	706	415	58.78	114.44	277.65	0	0
COREQ	1	0.01	709	0	0.	3.47	3.47	0	0
CPU	4	0.05	9098	8104	89.07	1.49	13.67	0	0
OTPUT	2	0.01	967	657	67.94	3.26	10.16	0	0
FHDRD	3	0.02	902	726	80.49	5.55	28.44	0	0
MHDRD	3	0.04	662	506	76.44	17.42	73.94	0	0
FHDWR	2	0.00	497	436	87.73	2.82	23.02	0	0
TAPOT	1	0.00	211	210	99.53	0.09	19.00	0	0

****
TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	211	38247.146	42036.519	8070148.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.910
5000	0	0.	0.	100.00	0.131	-0.791
10000	120	56.87	56.87	43.13	0.261	-0.672
15000	5	2.37	59.24	40.76	0.392	-0.553
20000	1	0.47	59.72	40.28	0.523	-0.434
25000	8	3.79	63.51	36.49	0.654	-0.315
30000	0	0.	63.51	36.49	0.784	-0.196
35000	6	2.84	66.35	33.65	0.915	-0.077
40000	6	2.84	69.19	30.81	1.046	0.042
45000	0	0.	69.19	30.81	1.177	0.161
50000	5	2.37	71.56	28.44	1.307	0.280
55000	2	0.95	72.51	27.49	1.438	0.399
60000	2	0.95	73.46	26.54	1.569	0.517
65000	0	0.	73.46	26.54	1.699	0.636
70000	1	0.47	73.93	26.07	1.830	0.755
75000	5	2.37	76.30	23.70	1.961	0.874
80000	3	1.42	77.73	22.27	2.092	0.993
85000	6	2.84	80.57	19.43	2.222	1.112
90000	3	1.42	81.99	18.01	2.353	1.231
95000	5	2.37	84.36	15.64	2.484	1.350
100000	2	0.95	85.31	14.69	2.615	1.469
105000	2	0.95	86.26	13.74	2.745	1.588
110000	2	0.95	87.20	12.80	2.876	1.707
115000	3	1.42	88.63	11.37	3.007	1.826
120000	8	3.79	92.42	7.58	3.137	1.945
OVERFLOW	16	7.58	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 126816.688 MAXIMUM VALUE OF OVERFLOW = 140476

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	708	324.685	134.541	229877.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.413
500	646	91.24	91.24	8.76	1.540	1.303
1000	61	8.62	99.86	0.14	3.080	5.019
1500	1	0.14	100.00	0.	4.620	8.736

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET                                                          634
                START       5,,,1                                              635
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 720000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	215	2# ENTER	0	215	3# ASSIGN	0	215	4# ASSIGN	0	215	5# ASSIGN	0	215
6# PRIOR	0	215	7# QUEUE	0	215	8# BUFFER	0	215	9# TRANSF	0	215	10# GATE	0	686
11# ENTER	0	686	12# ASSIGN	0	686	13# DEPART	0	686	14# LEAVE	0	686	15# QUEUE	0	6891
16# SEIZE	0	6891	17# DEPART	0	6891	18# ASSIGN	0	6891	19# ADVANC	0	6891	20# RELEAS	0	6891
21# TRANSF	0	6891	22# TRANSF	0	6205	23# LEAVE	0	475	24# ASSIGN	0	475	25# ADVANC	6	475
26# QUEUE	0	474	27# TRANSF	0	474	28# TEST	0	211	29# LEAVE	0	211	30# LEAVE	0	211
31# TABULT	0	211	32# TERM	0	211	33# GENERT	0	292	34# PREMPT	0	292	35# ADVANC	0	292
36# RETURN	0	292	37# SEIZE	0	292	38# SEIZE	0	292	39# SEIZE	0	292	40# SEIZE	0	292
41# ADVANC	0	292	42# RELEAS	0	292	43# RELEAS	0	292	44# RELEAS	0	292	45# RELEAS	0	292
46# TERM	0	292	52# ASSIGN	0	86	53# ASSIGN	0	163	54# ASSIGN	0	163	55# ASSIGN	0	163
56# ASSIGN	0	163	57# ASSIGN	0	163	58# ASSIGN	0	163	59# ASSIGN	0	163	60# ASSIGN	0	163
61# ASSIGN	0	163	62# TRANSF	0	163	63# ASSIGN	0	845	64# LOOP	0	845	65# ASSIGN	0	162
66# ASSIGN	0	162	67# TRANSF	0	162	68# ASSIGN	0	683	69# ASSIGN	0	683	70# ASSIGN	0	683
71# TRANSF	0	683	72# ASSIGN	0	163	73# ASSIGN	0	163	74# ASSIGN	0	163	75# TRANSF	0	163
90# ASSIGN	0	540	91# ASSIGN	0	540	92# ASSIGN	0	871	93# ASSIGN	0	1387	94# ASSIGN	C	1936
95# TEST	0	1936	96# BUFFER	0	1936	97# QUEUE	0	1936	98# SEIZE	0	1936	99# DEPART	0	1936
100# ADVANC	0	1936	101# RELEAS	0	1936	102# ASSIGN	0	1936	103# TRANSF	0	1936	112# BUFFER	0	689
113# TEST	0	689	114# GATE	0	689	115# ENTER	0	689	116# SEIZE	0	689	117# SEIZE	0	689
118# PREMPT	0	689	119# DEPART	0	689	120# ADVANC	0	689	121# RETURN	0	689	122# ASSIGN	0	689
123# ADVANC	1	6882	124# LOOP	0	6881	125# QUEUE	0	686	126# MARK	0	686	127# PREMPT	0	686
128# RELEAS	0	686	129# RELEAS	0	686	130# ADVANC	0	686	131# RETURN	0	686	132# TRANSF	0	686
133# RELEAS	0	6195	134# RELEAS	0	6195	135# ADVANC	18	6195	136# SEIZE	0	6193	137# SEIZE	C	6193
138# TRANSF	0	6193	159# BUFFER	0	941	160# TEST	0	941	161# QUEUE	0	941	162# GATE	0	941
163# ENTER	0	941	164# SEIZE	0	941	165# SEIZE	0	941	166# SEIZE	0	941	167# DEPART	0	941
168# ADVANC	0	941	169# RELEAS	0	941	170# ASSIGN	0	941	171# ADVANC	0	4702	172# LOOP	0	4702
173# PREMPT	0	941	174# RELEAS	0	941	175# RELEAS	0	941	176# ADVANC	0	941	177# RETURN	0	941
178# TEST	0	941	179# TABULT	0	686	180# ASSIGN	0	686	181# LEAVE	0	941	182# TRANSF	0	941
183# RELEAS	0	3761	184# RELEAS	0	3761	185# ADVANC	1	3761	186# SEIZE	0	3761	187# SEIZE	0	3761
188# TRANSF	0	3761	215# QUEUE	0	845	216# BUFFER	C	845	217# TEST	0	845	218# SEIZE	0	845
219# SEIZE	0	845	220# DEPART	0	845	221# ADVANC	0	845	222# ADVANC	0	845	223# PREMPT	0	845
224# ADVANC	0	845	225# RETURN	0	845	226# RELEAS	0	845	227# RELEAS	0	845	228# TRANSF	0	845
240# QUEUE	0	626	241# BUFFER	0	626	242# TEST	0	626	243# SEIZE	0	626	244# SEIZE	0	626
245# DEPART	0	626	246# ADVANC	0	626	247# ADVANC	0	626	248# ADVANC	0	626	249# PREMPT	0	626
250# ADVANC	0	626	251# RETURN	0	626	252# RELEAS	0	626	253# RELEAS	0	626	254# TRANSF	0	626
267# QUEUE	0	475	268# BUFFER	0	475	269# TEST	0	475	270# SEIZE	0	475	271# SEIZE	0	475
272# DEPART	0	475	273# ADVANC	0	475	274# ADVANC	0	475	275# PREMPT	0	475	276# ADVANC	0	475
277# RETURN	0	475	278# RELEAS	0	475	279# RELEAS	0	475	280# TRANSF	0	475	347# QUEUE	0	211
348# BUFFER	0	211	349# TEST	0	211	350# SEIZE	0	211	351# SEIZE	0	211	352# DEPART	0	211
353# ADVANC	0	211	354# ADVANC	0	211	355# PREMPT	0	211	356# ADVANC	0	211	357# RETURN	0	211
358# RELEAS	0	211	359# RELEAS	0	211	360# TRANSF	0	211	375# GENERT	0	5	376# TERM	C	5

****
FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	14533	6.16	0.2982	0.2982	0.	A	100.00	0	0
CHANA	1612	31.25	0.1679	0.1679	0.	A	100.00	0	0
CONTA	1612	31.25	0.1679	0.1679	0.	A	100.00	0	0
CHANB	918	80.75	0.2471	0.2471	0.	A	100.00	0	0
CONTB	918	80.75	0.2471	0.2471	0.	A	100.00	0	0
MUXCH	11584	5.75	0.2219	0.2219	0.	A	100.00	85	0
TMCON	11584	5.75	0.2219	0.2219	0.	A	100.00	85	0
CHANC	211	25.05	0.0176	0.0176	0.	A	100.00	0	0
TAPCN	211	25.05	0.0176	0.0176	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	- - AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	25.98	237	32887.14	C.260	0.260	0.	A	100.00	26	37
TASKS	5	0.95	687	415.86	C.190	0.190	0.	A	100.00	1	5
BUFFI	25	20.79	705	8845.80	C.832	0.832	0.	A	100.00	19	25
BUFFO	5	0.29	942	92.57	C.058	0.058	0.	A	100.00	1	4

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	7	0.30	689	438	63.57	129.53	355.55	0	0
COREQ	2	0.01	686	0	0.	4.17	4.17	0	0
CPU	5	0.05	8827	7678	86.98	1.86	14.32	0	0
OTPUT	2	0.01	941	611	64.93	4.14	11.81	0	0
FHDRD	2	0.02	845	669	79.17	6.00	28.78	0	0
MHDRD	3	0.04	626	469	74.92	17.14	68.36	0	0
FHDWR	1	0.00	475	416	87.58	2.01	16.15	0	0
TAPOT	1	0.00	211	208	98.58	0.24	16.67	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	211	35741.355	38248.323	7541426.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.934
5000	0	0.	0.	100.00	0.140	-0.804
10000	125	59.24	59.24	40.76	0.280	-0.673
15000	1	0.47	59.72	40.28	0.420	-0.542
20000	0	0.	59.72	40.28	0.560	-0.412
25000	5	2.37	62.09	37.91	0.699	-0.281
30000	2	0.95	63.03	36.97	0.839	-0.150
35000	6	2.84	65.88	34.12	0.979	-0.019
40000	2	0.95	66.82	33.18	1.119	0.111
45000	3	1.42	68.25	31.75	1.259	0.242
50000	8	3.79	72.04	27.96	1.399	0.373
55000	3	1.42	73.46	26.54	1.539	0.504
60000	6	2.84	76.30	23.70	1.679	0.634
65000	1	0.47	76.78	23.22	1.819	0.765
70000	3	1.42	78.20	21.80	1.959	0.896
75000	2	0.95	79.15	20.85	2.098	1.026
80000	3	1.42	80.57	19.43	2.238	1.157
85000	10	4.74	85.31	14.69	2.378	1.288
90000	2	0.95	86.26	13.74	2.518	1.419
95000	2	0.95	87.20	12.80	2.658	1.549
100000	4	1.90	89.10	10.90	2.798	1.680
105000	4	1.90	91.00	9.00	2.938	1.811
110000	4	1.90	92.89	7.11	3.078	1.941
115000	4	1.90	94.79	5.21	3.218	2.072
120000	1	0.47	95.26	4.74	3.357	2.203
OVERFLOW	10	4.74	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 128027.000 MAXIMUM VALUE OF OVERFLOW = 137785

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	686	320.159	140.158	219629.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.284
500	625	91.11	91.11	8.89	1.562	1.283
1000	60	8.75	99.85	0.15	3.123	4.851
1500	1	0.15	100.00	0.	4.685	8.418

THE REMAINING FREQUENCIES ARE ALL ZERO.

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                RESET
                START       5,,,1                                          636
                                                                           637
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 1020000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	178	2# ENTER	0	178	3# ASSIGN	0	178	4# ASSIGN	0	178	5# ASSIGN	0	178
6# PRIOR	0	178	7# QUEUE	0	178	8# BUFFER	0	178	9# TRANSF	0	178	10# GATE	0	575
11# ENTER	0	575	12# ASSIGN	0	575	13# DEPART	0	575	14# LEAVE	0	575	15# QUEUE	0	5996
16# SEIZE	0	5996	17# DEPART	0	5996	18# ASSIGN	0	5996	19# ADVANC	0	5996	20# RELEAS	0	5996
21# TRANSF	0	5996	22# TRANSF	0	5421	23# LEAVE	0	397	24# ASSIGN	0	397	25# ADVANC	4	397
26# QUEUE	0	399	27# TRANSF	0	399	28# TEST	C	178	29# LEAVE	0	178	30# LEAVE	0	178
31# TABULT	0	178	32# TERM	0	178	33# GENERT	C	305	34# PREMPT	0	305	35# ADVANC	0	305
36# RETURN	0	305	37# SEIZE	0	305	38# SEIZE	0	305	39# SEIZE	0	305	40# SEIZE	0	305
41# ADVANC	0	305	42# RELEAS	0	305	43# RELEAS	0	305	44# RELEAS	0	305	45# RELEAS	0	305
46# TERM	0	305	52# ASSIGN	0	80	53# ASSIGN	0	162	54# ASSIGN	0	162	55# ASSIGN	0	162
56# ASSIGN	0	162	57# ASSIGN	0	162	58# ASSIGN	0	162	59# ASSIGN	0	162	60# ASSIGN	0	162
61# ASSIGN	0	162	62# TRANSF	0	162	63# ASSIGN	0	787	64# LOOP	0	787	65# ASSIGN	0	161
66# ASSIGN	0	161	67# TRANSF	0	161	68# ASSIGN	0	626	69# ASSIGN	0	626	70# ASSIGN	0	626
71# TRANSF	0	626	72# ASSIGN	0	162	73# ASSIGN	0	162	74# ASSIGN	0	162	75# TRANSF	0	162
90# ASSIGN	0	364	91# ASSIGN	0	364	92# ASSIGN	0	555	93# ASSIGN	0	1156	94# ASSIGN	0	1605
95# TEST	0	1605	96# BUFFER	0	1605	97# QUEUE	0	1605	98# SEIZE	0	1605	99# DEPART	0	1605
100# ADVANC	0	1605	101# RELEAS	0	1605	102# ASSIGN	0	1605	103# TRANSF	0	1605	112# BUFFER	0	577
113# TEST	0	577	114# GATE	0	577	115# ENTER	0	577	116# SEIZE	0	577	117# SEIZE	0	577
118# PREMPT	0	577	119# DEPART	0	577	120# ADVANC	0	577	121# RETURN	0	577	122# ASSIGN	0	577
123# ADVANC	0	5774	124# LOOP	0	5775	125# QUEUE	0	575	126# MARK	0	575	127# PREMPT	0	575
128# RELEAS	0	575	129# RELEAS	0	575	130# ADVANC	0	575	131# RETURN	0	575	132# TRANSF	0	575
133# RELEAS	0	5200	134# RELEAS	0	5200	135# ADVANC	21	5200	136# SEIZE	0	5197	137# SEIZE	0	5197
138# TRANSF	0	5197	159# BUFFER	0	812	160# TEST	0	812	161# QUEUE	0	812	162# GATE	0	812
163# ENTER	0	812	164# SEIZE	0	812	165# SEIZE	0	812	166# SEIZE	0	812	167# DEPART	0	812
168# ADVANC	0	812	169# RELEAS	0	812	17C# ASSIGN	C	812	171# ADVANC	0	4062	172# LOOP	0	4062
173# PREMPT	0	812	174# RELEAS	0	812	175# RELEAS	0	812	176# ADVANC	0	812	177# RETURN	0	812
178# TEST	0	812	179# TABULT	0	575	180# ASSIGN	0	575	181# LEAVE	0	812	182# TRANSF	0	812
183# RELEAS	0	3250	184# RELEAS	0	3250	185# ADVANC	1	3250	186# SEIZE	0	3250	187# SEIZE	0	3250
188# TRANSF	0	3250	215# QUEUE	0	786	216# BUFFER	0	786	217# TEST	0	786	218# SEIZE	0	786
219# SEIZE	0	786	220# DEPART	0	786	221# ADVANC	0	786	222# ADVANC	0	786	223# PREMPT	0	786
224# ADVANC	0	786	225# RETURN	0	786	226# RELEAS	C	786	227# RELEAS	0	786	228# TRANSF	C	786
240# QUEUE	0	531	241# BUFFER	0	531	242# TEST	0	531	243# SEIZE	0	531	244# SEIZE	0	531
245# DEPART	0	531	246# ADVANC	0	531	247# ADVANC	0	531	248# ADVANC	0	531	249# PREMPT	0	531
250# ADVANC	0	531	251# RETURN	0	531	252# RELEAS	0	531	253# RELEAS	0	531	254# TRANSF	0	531
267# QUEUE	0	397	268# BUFFER	0	397	269# TEST	0	397	270# SEIZE	0	397	271# SEIZE	0	397
272# DEPART	0	397	273# ADVANC	0	397	274# ADVANC	0	397	275# PREMPT	0	397	276# ADVANC	0	397
277# RETURN	0	397	278# RELEAS	0	397	279# RELEAS	0	397	280# TRANSF	0	397	347# QUEUE	C	179
348# BUFFER	0	179	349# TEST	0	179	35C# SEIZE	0	179	351# SEIZE	0	179	352# DEPART	0	179
353# ADVANC	0	179	354# ADVANC	0	179	355# PREMPT	0	179	356# ADVANC	0	179	357# RETURN	0	179
358# RELEAS	0	179	359# RELEAS	0	179	360# TRANSF	0	179	375# GENERT	0	5	376# TERM	0	5

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FACILITIES
****

REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	12575	6.15	0.2579	0.2579	0.	A	100.00	0	0
CHANA	1488	31.43	0.1559	0.1559	0.	A	100.00	0	0
CONTA	1488	31.43	0.1559	0.1559	0.	A	100.00	0	0
CHANB	836	79.76	0.2223	0.2223	0.	A	100.00	0	0
CONTB	836	79.76	0.2223	0.2223	0.	A	100.00	0	0
MUXCH	9837	5.85	0.1917	0.1917	0.	A	100.00	0	0
TMCON	9837	5.85	0.1917	0.1917	0.	A	100.00	0	0
CHANC	179	25.25	0.0151	0.0151	0.	A	100.00	0	0
TAPCN	179	25.25	0.0151	0.0151	0.	A	100.00	0	0

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STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	21.68	204	31885.57	0.217	0.217	0.	A	100.00	26	33
TASKS	5	0.80	576	416.64	0.160	0.160	0.	A	100.00	1	5
BUFFI	25	17.44	596	8780.63	0.698	0.698	0.	A	100.00	21	25
BUFFO	5	0.25	813	91.55	0.050	0.050	0.	A	100.00	1	3

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	4	0.04	577	428	74.18	22.23	86.08	0	0
COREQ	1	0.01	575	0	0.	3.25	3.25	0	0
CPU	4	0.04	7601	6851	90.13	1.47	14.86	0	0
OTPUT	2	0.01	812	606	74.63	2.54	10.02	0	0
FHDRD	3	0.01	786	639	81.30	4.92	26.30	0	0
MHDRD	2	0.03	531	416	78.34	14.61	67.48	0	0
FHDWR	2	0.01	397	325	81.86	5.00	27.57	0	0
TAPOT	1	0.00	179	175	97.77	0.35	15.50	0	0

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TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	178	37052.443	39463.883	6595335.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.939
5000	0	0.	0.	100.00	0.135	-0.812
10000	97	54.49	54.49	45.51	0.270	-0.685
15000	2	1.12	55.62	44.38	0.405	-0.559
20000	4	2.25	57.87	42.13	0.540	-0.432
25000	7	3.93	61.80	38.20	0.675	-0.305
30000	0	0.	61.80	38.20	0.810	-0.179
35000	6	3.37	65.17	34.83	0.945	-0.052
40000	3	1.69	66.85	33.15	1.080	0.075
45000	4	2.25	69.10	30.90	1.214	0.201
50000	7	3.93	73.03	26.97	1.349	0.328
55000	2	1.12	74.16	25.84	1.484	0.455
60000	6	3.37	77.53	22.47	1.619	0.581
65000	1	0.56	78.09	21.91	1.754	0.708
70000	2	1.12	79.21	20.79	1.889	0.835
75000	3	1.69	80.90	19.10	2.024	0.962
80000	2	1.12	82.02	17.98	2.159	1.088
85000	0	0.	82.02	17.98	2.294	1.215
90000	0	0.	82.02	17.98	2.429	1.342
95000	3	1.69	83.71	16.29	2.564	1.468
100000	5	2.81	86.52	13.48	2.699	1.595
105000	2	1.12	87.64	12.36	2.834	1.722
110000	7	3.93	91.57	8.43	2.969	1.848
115000	3	1.69	93.26	6.74	3.104	1.975
120000	1	0.56	93.82	6.18	3.239	2.102
OVERFLOW	11	6.18	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 126689.545 MAXIMUM VALUE OF OVERFLOW = 135518

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	575	318.544	135.484	183163.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.351
500	520	90.43	90.43	9.57	1.570	1.339
1000	54	9.39	99.83	0.17	3.139	5.030
1500	1	0.17	100.00	0.	4.709	8.720

THE REMAINING FREQUENCIES ARE ALL ZERO

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                RESET
                START       5,,,1                                                    638
                                                                                     639
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TERMINAL STATISTICS * ABSOLUTE CLOCK = 1320000 RELATIVE CLOCK = 300000

BLOCK COUNTS

	CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL		CURRENT	TOTAL
1# GENERT	0	185	2# ENTER	0	185	3# ASSIGN	0	185	4# ASSIGN	0	185	5# ASSIGN	0	185
6# PRIOR	0	185	7# QUEUE	0	185	8# BUFFER	0	185	9# TRANSF	0	185	10# GATE	0	633
11# ENTER	0	633	12# ASSIGN	0	633	13# DEPART	0	633	14# LEAVE	0	633	15# QUEUE	0	6405
16# SEIZE	0	6405	17# DEPART	0	6405	18# ASSIGN	0	6405	19# ADVANC	1	6405	20# RELEAS	0	6404
21# TRANSF	0	6404	22# TRANSF	0	5772	23# LEAVE	0	439	24# ASSIGN	0	439	25# ADVANC	2	439
26# QUEUE	0	441	27# TRANSF	0	441	28# TEST	0	194	29# LEAVE	0	194	30# LEAVE	0	194
31# TABULT	0	194	32# TERM	0	194	33# GENERT	0	314	34# PREMPT	0	314	35# ADVANC	0	314
36# RETURN	0	314	37# SEIZE	0	314	38# SEIZE	0	314	39# SEIZE	0	314	40# SEIZE	0	314
41# ADVANC	1	314	42# RELEAS	0	313	43# RELEAS	0	313	44# RELEAS	0	313	45# RELEAS	0	313
46# TERM	0	313	52# ASSIGN	0	71	53# ASSIGN	0	144	54# ASSIGN	0	144	55# ASSIGN	0	144
56# ASSIGN	0	144	57# ASSIGN	0	144	58# ASSIGN	0	144	59# ASSIGN	0	144	60# ASSIGN	0	144
61# ASSIGN	0	144	62# TRANSF	0	144	63# ASSIGN	0	799	64# LOOP	0	799	65# ASSIGN	0	156
66# ASSIGN	0	156	67# TRANSF	0	156	68# ASSIGN	0	643	69# ASSIGN	0	643	70# ASSIGN	0	643
71# TRANSF	0	643	72# ASSIGN	0	144	73# ASSIGN	0	144	74# ASSIGN	0	144	75# TRANSF	0	144
90# ASSIGN	0	480	91# ASSIGN	0	480	92# ASSIGN	0	755	93# ASSIGN	0	1267	94# ASSIGN	0	1784
95# TEST	0	1784	96# BUFFER	0	1784	97# QUEUE	0	1784	98# SEIZE	0	1784	99# DEPART	0	1784
100# ADVANC	0	1784	101# RELEAS	0	1784	102# ASSIGN	0	1784	103# TRANSF	0	1784	112# BUFFER	0	626
113# TEST	0	626	114# GATE	0	626	115# ENTER	0	626	116# SEIZE	0	626	117# SEIZE	0	626
118# PREMPT	0	626	119# DEPART	0	626	120# ADVANC	0	626	121# RETURN	0	626	122# ASSIGN	0	626
123# ADVANC	0	6284	124# LOOP	0	6284	125# QUEUE	0	633	126# MARK	0	633	127# PREMPT	0	633
128# RELEAS	0	633	129# RELEAS	0	633	130# ADVANC	0	633	131# RETURN	0	633	132# TRANSF	0	633
133# RELEAS	0	5651	134# RELEAS	0	5651	135# ADVANC	14	5651	136# SEIZE	0	5658	137# SEIZE	0	5658
138# TRANSF	0	5658	159# BUFFER	0	879	160# TEST	0	879	161# QUEUE	0	879	162# GATE	0	879
163# ENTER	0	879	164# SEIZE	0	879	165# SEIZE	0	879	166# SEIZE	0	879	167# DEPART	0	879
168# ADVANC	0	879	169# RELEAS	0	879	170# ASSIGN	0	879	171# ADVANC	0	4397	172# LOOP	0	4397
173# PREMPT	0	880	174# RELEAS	0	880	175# RELEAS	0	880	176# ADVANC	0	880	177# RETURN	0	880
178# TEST	0	880	179# TABULT	0	634	180# ASSIGN	0	634	181# LEAVE	0	880	182# TRANSF	0	880
183# RELEAS	0	3517	184# RELEAS	0	3517	185# ADVANC	0	3517	186# SEIZE	0	3518	187# SEIZE	0	3518
188# TRANSF	0	3518	215# QUEUE	0	799	216# BUFFER	0	799	217# TEST	0	799	218# SEIZE	0	799
219# SEIZE	0	799	220# DEPART	0	799	221# ADVANC	0	799	222# ADVANC	0	799	223# PREMPT	0	799
224# ADVANC	0	799	225# RETURN	0	799	226# RELEAS	0	799	227# RELEAS	0	799	228# TRANSF	0	799
240# QUEUE	0	590	241# BUFFER	0	590	242# TEST	0	590	243# SEIZE	0	590	244# SEIZE	0	590
245# DEPART	0	590	246# ADVANC	0	590	247# ADVANC	0	590	248# ADVANC	0	590	249# PREMPT	0	590
250# ADVANC	0	590	251# RETURN	0	590	252# RELEAS	0	590	253# RELEAS	0	590	254# TRANSF	0	590
267# QUEUE	0	439	268# BUFFER	0	439	269# TEST	0	439	270# SEIZE	0	439	271# SEIZE	0	439
272# DEPART	0	439	273# ADVANC	0	439	274# ADVANC	0	439	275# PREMPT	0	439	276# ADVANC	0	439
277# RETURN	0	439	278# RELEAS	0	439	279# RELEAS	0	439	280# TRANSF	0	439	347# QUEUE	0	193
348# BUFFER	0	193	349# TEST	0	193	350# SEIZE	0	193	351# SEIZE	0	193	352# DEPART	0	193
353# ADVANC	0	193	354# ADVANC	0	193	355# PREMPT	0	193	356# ADVANC	0	193	357# RETURN	0	193
358# RELEAS	0	193	359# RELEAS	0	193	360# TRANSF	0	193	375# GENERT	0	5	376# TERM	0	5

****
FACILITIES
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REFERENCE	# OF ENTRIES	AVERAGE TIME/TRAN	AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	TRANSACTION NUMBER SEIZING	PREEMPTING
CPU	13542	6.24	0.2815	0.2815	0.	A	100.00	91	0
CHANA	1552	31.83	0.1647	0.1647	0.	A	100.00	83	0
CONTA	1552	31.83	0.1647	0.1647	0.	A	100.00	83	0
CHANB	904	81.76	0.2464	0.2464	0.	A	100.00	83	0
CONTB	904	81.76	0.2464	0.2464	0.	A	100.00	83	0
MUXCH	10681	5.81	0.2068	0.2068	0.	A	100.00	0	0
TMCON	10681	5.81	0.2068	0.2068	0.	A	100.00	0	0
CHANC	193	25.02	0.0161	0.0161	0.	A	100.00	0	0
TAPCN	193	25.02	0.0161	0.0161	0.	A	100.00	0	0

****
STORAGES
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REFERENCE	CAPACITY	AVERAGE CONTENTS	ENTRIES	AVERAGE TIME/UNIT	AVERAGE UTILIZATION - - TOTAL TIME	AVAIL. TIME	UNAVAIL. TIME	CURRENT STATUS	PERCENT AVAILABILITY	CURRENT CONTENTS	MAXIMUM CONTENTS
TERMS	100	23.64	211	33614.35	0.236	0.236	0.	A	100.00	17	33
TASKS	5	0.89	634	419.26	0.177	0.177	0.	A	100.00	1	5
BUFFI	25	18.98	647	8802.21	0.759	0.759	0.	A	100.00	14.	25
BUFFO	5	0.27	880	92.12	0.054	0.054	0.	A	100.00	0	3

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QUEUES
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REFERENCE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	TOTAL AVG. TIME/TRAN	NZERO AVG. TIME/TRAN	QTABLE NUMBER	CURRENT CONTENTS
INPUT	5	0.07	626	450	71.88	33.93	120.68	0	0
COREQ	1	0.01	633	0	0.	3.15	3.15	0	0
CPU	5	0.05	8189	7246	88.48	1.67	14.50	0	0
OTPUT	2	0.01	879	618	70.31	3.35	11.28	0	0
FHDRD	3	0.01	799	644	80.60	4.66	24.01	0	0
MHDRD	3	0.03	590	449	76.10	16.75	70.07	0	0
FHDWR	2	0.01	439	373	84.97	3.84	25.53	0	0
TAPOT	1	0.00	193	192	99.48	0.10	19.00	0	0

****
TABLES
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REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
TTIME	194	40246.392	43350.287	7807800.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-0.928
5000	0	0.	0.	100.00	0.124	-0.813
10000	109	56.19	56.19	43.81	0.248	-0.698
15000	3	1.55	57.73	42.27	0.373	-0.582
20000	1	0.52	58.25	41.75	0.497	-0.467
25000	8	4.12	62.37	37.63	0.621	-0.352
30000	0	0.	62.37	37.63	0.745	-0.236
35000	4	2.06	64.43	35.57	0.870	-0.121
40000	5	2.58	67.01	32.99	0.994	-0.006
45000	1	0.52	67.53	32.47	1.118	0.110
50000	1	0.52	68.04	31.96	1.242	0.225
55000	1	0.52	68.56	31.44	1.367	0.340
60000	5	2.58	71.13	28.87	1.491	0.456
65000	3	1.55	72.68	27.32	1.615	0.571
70000	3	1.55	74.23	25.77	1.739	0.686
75000	0	0.	74.23	25.77	1.864	0.802
80000	2	1.03	75.26	24.74	1.988	0.917
85000	7	3.61	78.87	21.13	2.112	1.032
90000	2	1.03	79.90	20.10	2.236	1.148
95000	4	2.06	81.96	18.04	2.360	1.263
100000	4	2.06	84.02	15.98	2.485	1.378
105000	4	2.06	86.08	13.92	2.609	1.494
110000	3	1.55	87.63	12.37	2.733	1.609
115000	2	1.03	88.66	11.34	2.857	1.724
120000	6	3.09	91.75	8.25	2.982	1.840
OVERFLOW	16	8.25	100.00	0.		

AVERAGE VALUE OF OVERFLOW = 130153.500 MAXIMUM VALUE OF OVERFLOW = 137325

REFERENCE	ENTRIES	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS
RESPN	634	322.021	132.421	204161.000

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	0.	0.	100.00	0.	-2.432
500	572	90.22	90.22	9.78	1.553	1.344
1000	62	9.78	100.00	0.	3.105	5.120

THE REMAINING FREQUENCIES ARE ALL ZERO

A P P E N D I X C

Experimental Results

Tabulation

Simulation Results

Experiment 1

	Run 1	Run 2	Run 3	Run 4	Combined
Tasks Started	164	199	191	146	700
Tasks Finished	160	167	173	131	631
Average Terms. Active	33.3	45.7	75.6	96.5	62.8
Maximum Terms. Active	44	68	87	100	100
Average Input Buffers	15	15	15	15	15
Maximum Input Buffers	15	15	15	15	15
Average Input Queve	14.7	27.2	57.2	77.8	44.2
Maximum Input Queve	27	51	70	85	85
Input Queve Wait Time	8641	15015	30672	40470	23700
System/Terminal Interactions	497	497	497	497	1988
Response Time	296.6	297.4	293.1	301.6	297.2
Total Task Turnaround	50802	61003	105693	160113	94403

NOTE: All time expressed in milliseconds

Simulation Results

Experiment 2

	Run 1	Run 2	Run 3	Run 4	Combined
Tasks Started	195	225	221	168	809
Tasks Finished	206	220	220	176	822
Average Terms. Active	21.6	25.1	28.7	18.7	23.5
Maximum Terms. Active	31	33	39	30	39
Average Input Buffers	17.6	20.2	22.0	15.1	18.7
Maximum Input Buffers	25	25	25	25	25
Average Input Queve	.01	.19	1.54	.02	.44
Maximum Input Queve	2	5	11	3	11
Input Queve Wait Time	5.9	85.0	638.5	13.6	185.8
System/Terminal Interactions	589	670	723	505	2487
Response Time	308.6	333.0	319.4	311.4	318.1
Total Task Turnaround	32044	34272	39415	33896	34907

NOTE: All time expressed in milliseconds

Simulation Results

Experiment 3

	Run 1	Run 2	Run 3	Run 4	Combined
Tasks Started	191	220	196	197	804
Tasks Finished	203	213	202	200	818
Average Terms. Active	24.5	27.9	23.9	20.2	24.1
Maximum Terms. Active	35	45	36	29	45
Average Input Buffers	19.8	21.0	19.1	16.5	19.1
Maximum Input Buffers	25	25	25	25	25
Average Input Queue	.19	1.94	.17	.0	.6
Maximum Input Queue	6	17	8	2	17
Input Queue Wait Time	88	831.3	80.1	1.76	250.3
System/Terminal Interactions	658	694	638	547	2537
Response Time	322.8	322.5	323.8	315.9	321.3
Total Task Turnaround	37024	39066	36517	30579	35797

NOTE: All times expressed in milliseconds

Simulation Results

Experiment 4

	Run 1	Run 2	Run 3	Run 4	Combined
Tasks Started	212	215	178	185	790
Tasks Finished	211	211	178	194	794
Average Terms. Active	26.8	26.0	21.7	23.6	24.5
Maximum Terms. Active	35	37	33	33	37
Average Input Buffers	21.7	20.8	17.4	19.0	19.7
Maximum Input Buffers	25	25	25	25	25
Average Input Queue	.27	.3	.03	.07	.17
Maximum Input Queue	5	7	4	5	7
Input Queue Wait Time	114.4	129.5	22.2	33.9	75.0
System/Terminal Interactions	708	686	575	634	2603
Response Time	324.7	320.2	318.5	322.0	321.4
Total Task Turnaround	38247	35741	37052	40246	37822

NOTE: All times are expressed in milliseconds.