Fault-Tolerant High-Density Power Converters and In-Situ Health Prediction for Offshore MVDC Distribution

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DEDICATION

I dedicate my dissertation work to my lovely family and my lovely wife for their endless love, support, and encouragement.

A special feeling of gratitude to my loving parents, ***Heidar*** and ***Pari,*** whose words of encouragement and push for tenacity ring in my ears. My brothers ***Ali*** and ***Ata*** and their wives (***Elham*** and ***Nastaran***) have never left my side and are very special. Ali encouraged me to start the graduate program and supported me during the new chapter of my life.

Last but not least, I dedicate this work and give special thanks to my best friend, best supporter, and my wonderful wife, ***Sadaf***, for being with me throughout the entire doctorate program and support me when I need her strong suggestions and warm emotions.

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ABSTRACT

A fault-tolerant solid-state transformer (SST) structure to combine the benefits of higher power density and robustness in medium-voltage DC (MVDC) electric distribution systems is proposed in this dissertation. A SiC-MOSFET-based 6 MW, 36/6 kV ISOSP (input series output series-parallel) modular stacked DC/DC SST is proposed using medium frequency (MF) transformer isolation. This structure renders the system with fault tolerance and the capability to operate normally even in a partial fault condition. Small-signal modeling, simulations, and Typhoon-HiL real-time system were performed to verify the operation of the converter. Experimental results from a scaled-down laboratory prototype prove the feasibility of the proposed isolated DC/DC structure and control system. While replacing a low frequency transformer (LFT) with an SST for a certain application, the design of the transformer must be primarily optimized for size and efficiency. In this work, the transient model of a single-phase E-core transformer using a Multi-Turn Coil Domain was used to analyze the electromagnetic field. A medium frequency (MF) transformer with a ferrite core is designed and simulated in COMSOL© based on hardware prototype specifications, and outcomes from 3-D finite element analysis (FEA) matched the 20 kHz MF transformer design used in the hardware. The model includes the analysis of the nonlinear B-H curve, including saturation effects in the core to simulate the magnetic behavior of the soft-iron core. A pulsating voltage, including with up to 7^{th} harmonic, to simulate the effects of a near-square wave is applied to the model. The FEA design was done before manufacturing and to confirm the behavior of the designed transformer, especially for

peak flux density. It was also possible to compare the volume of the proposed MF transformer with LF transformers using FEA simulation. Overall, the proposed system can lead to significant improvement in power density in mission-critical MVDC applications such as subsea electrification. The reliability prediction and survival indices calculation are required for the sensitive operation of the proposed fault-tolerant converter.

A better understanding of the failure mechanisms and barriers to the utilization of electronic devices in extreme environments leads to reliable power converters in offshore applications. It is well known that each component's reliability in a power converter affects the reliability of the overall system. Due to the advancements in computing infrastructure and sensor technologies, data-driven approaches for predicting the health of power converters in real-time are slowly becoming popular. This research proposes a new statistical approach using probability density functions (PDFs) and associated concepts in measure theory to predict the probability of system failure using individual components' degradation data. For this purpose, remaining-useful-life (RUL) is estimated for each power component (or sub-system) using qualification data, followed by an evaluation of a cumulative probability of survival for the converter. An artificial neural network (ANN) is then trained to quickly estimate in real-time the probability of survival of the power converter in the future. While the algorithm involves multiple computation steps, the RUL prediction accuracy using the proposed method will be high due to the data-driven approach. Moreover, the machine learning-based model resulting from this approach to predict the probability of survival is low on

memory utilization. It is envisioned that this approach can be used to create digital twins of power converters in practical circuits, optimize performance, and predict RUL. This dissertation explains the theory followed by scaled-down hardware of an isolated modular DC-DC converter. An experimental qualification setup for device degradation test and system-level RUL measurement methods are provided.

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CHAPTER 1.
INTRODUCTION

1.1. MVDC Configuration for Subsea Electrification

At present, the subsea power transmission and distribution architectures primarily follow high voltage AC (or HVAC), as shown in Figure 1-1 [1]. The subsea electrical power system components include motors, power electronic converters, step-up/down transformers, switchgear, uninterruptable power supplies (UPS), subsea control modules, power management systems, etc. Several of these components are used to drive compressors and pumps for artificial oil lifting.

Power converters are used in many sections of a subsea power system – such as Variable Frequency Drives (VFDs), switchgear, etc. Advanced topologies, as well as reliability analysis for non-isolated and isolated power converters, are available in the literature [2]–[7]. The main challenge is that transmission and distribution at high power and long distances require durable cables with proper insulation that can also sustain harmonics.

Using long tie-back systems also results in reactive power consumption along with the cables, which further leads to higher losses. Moreover, the isolation transformers used for step-up/step-down in subsea or offshore applications operate at low frequency (LF) – may range from 15 to 65 Hz. These transformers are usually bulky and present difficulties in terms of transportation and installation. The issue of reactive power consumption can be solved by using a high voltage DC (HVDC) or medium-voltage DC (MVDC) architecture. However, that brings some other challenges: (i) there

is no inherent ‘zero-crossing’ in DC as in AC; (ii) step-up or step-down in voltage is challenging as it requires power electronics along with transformer isolation. A loss comparison between AC and DC distribution systems is conducted in [8], where two models, AC and DC, for a large distribution system are considered for comparison.

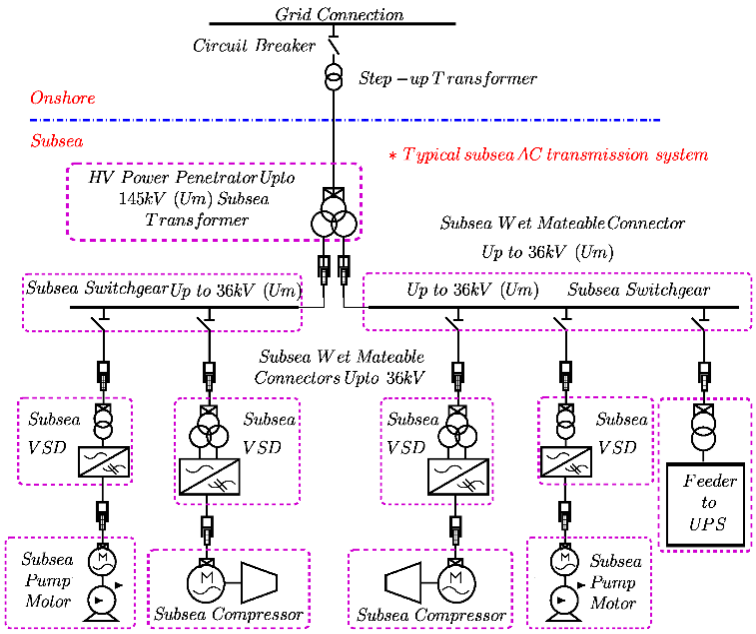


Figure 1-1 Conventional HVAC subsea power system block diagram [1]

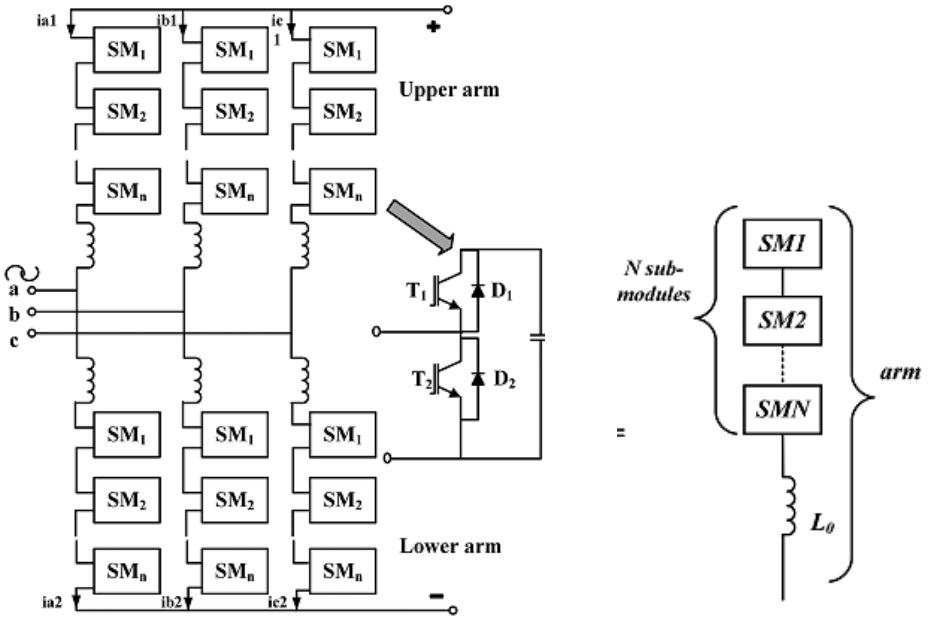
Due to the advantages provided by HVDC/MVDC transmission and distribution for longer tie-back lengths, there have been a few attempts to develop such architectures for subsea applications. The fundamental system components of MVDC grids, including an overview of power electronic converters and protection schemes against DC fault currents, is presented in [9]. Different MVDC collection systems with appropriate control modes for offshore wind plants are reviewed in [10]. For multi-phase multi-pulse supplies, different technologies for prime movers, electrical

generators, and rectifiers are discussed in [11]–[14]. To overcome the connection challenges between generated power by an offshore wind plant to the onshore electricity grids, an overview of the DC link development and evolution dedicated to HVDC structure is discussed in [15].

The most common circuits which provide isolation between primary and secondary side of the converter is Dual Active Bridge (DAB) structure. The DAB structure consists of DC/AC, step-down transformer, and AC/DC stages. The isolated topologies are classified into Two-Level DAB, Modular Multilevel DAB, and Multi-Module Cascaded DAB structures [16]. Several configurations of SSTs for DC power distribution are discussed in [17]–[20]. The two-level DAB converter is presented in [21], [22]. The basic structures of the multi-module cascaded DAB DC-DC converters are discussed in [23], [24]. A combination of different multi-module cascaded DAB DC-DC converters topologies can be assembled for specific HVDC applications [25], [26].

The Modular Multilevel Converter (MMC) is a structure used in high voltage adjustable speed drives, medium or high voltage grid interface applications, high-voltage direct current (HVDC), etc., for power conversion in an efficient and reliable manner. MMC structure presents many advantages such as modularity, the absence of a high voltage DC bus, and low switching frequency. It also presents some disadvantages, such as modeling complexity and control due to a large number of semiconductors. A review of different MMC topologies is discussed in [27]–[32]. While MMCs can provide fault tolerance with redundancy, they directly do not provide

galvanic isolation and hence cannot be used in the proposed application, especially with a high step down. Regarding MMC, this type of multilevel converter is gained a great deal of study in terms of various aspects as output performance improvement [33]–[36], reduced computational burden [37]–[39], power losses balancing among SMs [40]–[42], etc. The introduction summarized topologies and the operation characteristics of different kinds of DC/DC converters based on MMC along with their application is discussed in [16], [43], [44].



(a) (b)

Figure 1-2 Three-phase MMC circuit topology (a) MMC structure, (b) MMC converter arm (© 2018 IEEE [27]– Adapted with permission from the IEEE)

On the other hand, the primary function of solid-state transformers (or SSTs) is to provide galvanic isolation with sufficient step down as in the proposed application through the use of medium frequency transformers. SSTs can also provide additional

functionalities, compared to the classical low-frequency transformers (LFTs), such as bidirectional power flow control, an adaptation of both voltage and frequency levels, improvements of power quality indices through reactive compensation, active harmonic filtering, voltage drop compensation, and fault tolerance, among other aspects [45].

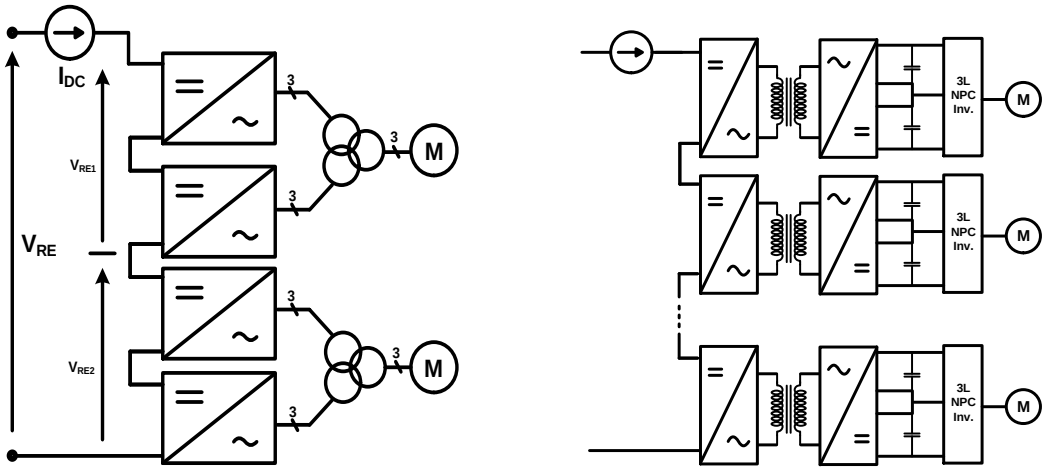
As described in [1] , a step-down transformer is the main interface between the subsea transmission line and the power distribution. It can be in multiple stages (HVDC/MVDC to LF AC conversion followed by an LF transformer and LF AC to MVDC conversion) or a single isolated DC-DC converter stage (using medium frequency transformer isolation) as a solid-state transformer (SST) are installed in a sealed, fluid-filled, and pressure-compensated unit, LF transformers will step down the voltage for VFDs of pump motors in subsea applications. To improve the power density of isolated converters, the use of medium frequency (MF) or high frequency (HF) transformers is a popular method. Efficiency and reliability are of utmost concern here.

As SSTs have a large number of power devices, it is important to enhance their reliability at high efficiency for subsea grids. Hence, the proposed SST structure combines the requirements of high-density power conversion (through medium frequency (MF) galvanic isolation and voltage step down) along with higher reliability and fault tolerance (via the in-built redundancy and cluster-level fault handling). In other words, the proposed SST structure can still operate normally even under faulty conditions (when some of the modules get bypassed) and generate the output without interrupting the operation of subsea electrification. This advantage can help in

significantly minimizing the costs and efforts by reducing the downtime in reliability-critical subsea or offshore operations.

To discuss how the proposed fault tolerant SST in this research differs from literature, a short comparison is provided here. A new approach using modular conversion and inductive filtering on the DC transmission line, also known as modular stacked direct current transmission (MSDC), is proposed in [46]. This structure uses modular multilevel converters at both sending and receiving end, which is connected in series to achieve high voltage DC operation, as shown in Figure 1-3(a).

A current-controlled mode of varying the sending end converter voltage is utilized to have a constant current along the cable as per load power demand. Having bulky low-frequency transformers on the load side increases the volume and mass of the whole system. Besides, the subsea loads are located far apart in this configuration; therefore, they require a large number of penetrators and wet-mate connectors, making the system quite expensive and potentially unreliable. Similarly, a current-fed modular stacked DC/DC converter is introduced in [47], as shown in Figure 1-3(b). Implementing the ZCS technique using a high frequency (HF) transformer is the benefit of the configuration used in the subsea environment. In [48], an input-series-output-parallel connection of only two ZVS full-bridge modules, with interleaved control for photovoltaic power conditioning systems, is introduced. The stacked modular power converter topology on the load side, as well as the topside (onshore) of the subsea power delivery system, is described in [49].



(a) (b)

Figure 1-3. (a) MSDC configuration proposed for subsea application (© 2014 IEEE [46]– Adapted with permission from the IEEE)
(b) Series-input parallel-output modular-phase DC-DC converter (© 2016 IEEE [47]– Adapted with permission from the IEEE)

Compared to the references [46]–[49], the configuration of the proposed fault-tolerant dc/dc topology in this research is different. The input ports of the converter modules are connected in series, but the output of each module is connected in series to another three modules to build a cluster (four series-connected modules in each cluster). Then, output ports of clusters are connected in parallel to carry load voltage/current requirements. A voltage-based zero-voltage-switching (ZVS) converter with switching frequency in the range of tens of kilohertz with redundancy is proposed in this work. The architecture proposed in [50] is employed to reduce the footprint and achieve modularity using a ring-based HVDC structure, which uses series-connected open-ended transformers at the distribution station, wherein each distribution transformer supplies power to the load individually, shown in Figure 1-4. The HVAC voltage converted at the inverter (DC/AC) stage is distributed among multiple transformers and achieves modularity. In the case of load fault, that particular section can be isolated by

using a bypass switch, which is connected across the primary winding of the transformer.

Many of the challenges and limitations involved in the power transmission, distribution, and electronic systems in subsea applications are discussed in [19]. To address the above-mentioned challenges, an MVDC distribution architecture with the concept of modular stacked medium frequency (MF) SST topology should be presented.

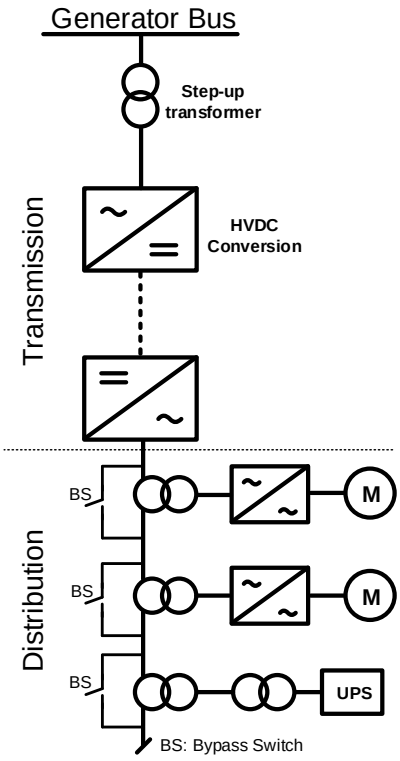


Figure 1-4. Single line diagrams of subsea power architectures (© 2010 IEEE [50]– Adapted with permission from the IEEE)

1.2. Reliability and Health-Monitoring in Power Converters

The reliability of power semiconductor switches is important when considering their vital role in power electronic converters for downhole subsea applications. Throughout the converter operation, power semiconductor devices may experience several unexpected and abnormal stresses due to environmental conditions, transients, and overload conditions, which can lead to severe degradation or even failure and ultimately interrupt the operation of the power converter. A better understanding of the failure mechanisms and barriers to the utilization of electronic devices in extreme environments leads to reliable power converters in offshore drilling applications. Due to the continuous emergence of SiC-MOSFETs in power electronic converters, many questions about their performance and reliability rise. According to a survey based on over 200 products from 80 companies, as shown in Figure 1-5, the semiconductor devices and capacitors are the two major components responsible for power electronic systems failure. With the increasing use of oil & gas sources, the number of power converters is increasing. Therefore, the reliability and efficiency of these converters are a significant concern.

Power semiconductors are one of the main components of power converters. Thus, the efficiency and reliability of these components are of great interest as they play a significant role in the power converters' overall reliability. With respect to technology advancements in material sciences, power MOSFETs with wide-band-gap materials have been proposed, such as silicon carbide (SiC) and gallium nitride (GaN), as an alternative to existing silicon (Si) based MOSFETs and IGBTs.

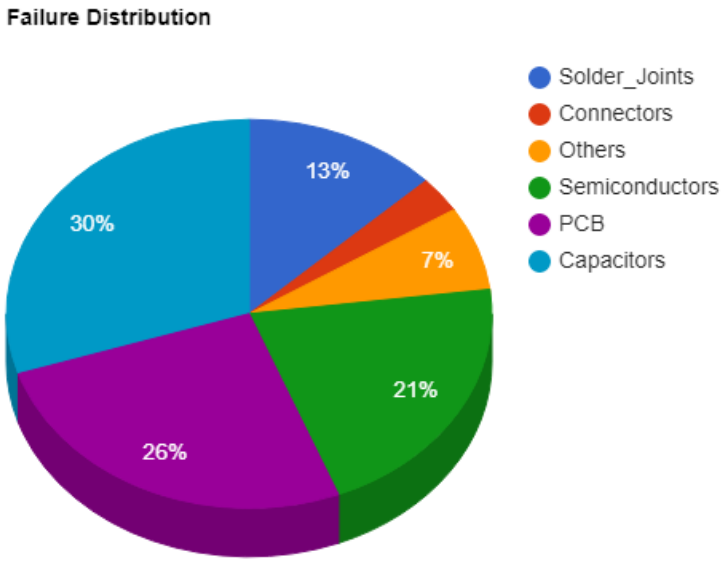


Figure 1-5. Failure distribution in power electronic system [27]

However, reliability analysis should be performed before substituting SiC-MOSFETs in the place of existing Si-MOSFETs and IGBTs [51]–[53]. A precise junction temperature estimation plays an essential role in the design and optimization of power devices. Power switches are extensively used in several mission-critical applications, such as subsea electrification [54], Electric Vehicle (EV) propulsion [55], and grid-connected power converters [56], where reliability is very important. The temperature of the semiconductor junction changes during the device operation with respect to the specific conditions. These variations induce thermo-mechanical stresses in the semiconductor packages or assemblies, which ultimately result in the failure of the entire application. A testing procedure for SiC power metal-oxide-semiconductor field-effect transistor (MOSFET) to determine its reliability model parameters is presented in [57]. The failure mechanisms of power electronics are complicated and are affected by many factors and discussed in [58]. It has been revealed that thermal cycling

(i.e., temperature swings inside or outside the devices) is a critical cause of failure in power electronic systems [59]. Any failure of these components may lead to shutting down of the whole system, which not only affects safety but also increases operational cost. The implementation issues of condition monitoring (CM) approaches are focused in [60].

Several model-based techniques have been presented in the literature to predict the reliability of power converters, including the use of analytics to interpret system characteristics and performance. An in situ SiC-MOSFET degradation monitoring method along with power-cycling tests is presented in [61]. The static device parameters are measured while aging the DUT, and the physical causes are discussed in detail. A custom accelerated aging platform for power MOSFETs was introduced in [62], which used a data-driven approach to estimate the remaining-useful-life (RUL) of a power device. A new method for reliability evaluation of power converters based on online monitoring of a parameter variation over time and deploying the Bayesian algorithm for data exploitation is presented in [63]. A study on degradation monitoring of silicon carbide MOSFETs and an early warning method to detect aging is presented in [64]. An RUL estimation technique for the critical component in a system was proposed in [65] and evaluated for motor bearings. A comprehensive review of the state-of-the-art in failure and lifetime predictions of power electronics devices was introduced in [66]. Different methods with component condition monitoring to improve the reliability of wind turbines are reviewed in [67]. Although the power semiconductor device reliability is reviewed systematically in [68], [69], the relation among techniques is not discussed.

Moreover, there are several limitations to existing approaches: (a) Once the failure data are collected from degradation tests, the actual RUL estimation using the monitoring process is usually based on the worst-case component failure time, which is often a conservative approach and will either result in underutilization of parts or in a large inventory; and (b) In order to assess the RUL of the complete system as a function of time and mission profile, it is not enough to address just one 'most critical' component, but the cumulative characteristics of all the components must be considered that can constitute a system failure. Considering the necessity of having a system-level health monitoring index, different methods and algorithms are applied to different datasets. The artificial neural network (ANN) is known as a universal function approximators, which can approximate any given nonlinear input/output data relationship with arbitrary precision.

1.3. Research Objectives

Subsea deep-water oil and gas production systems require long-distance power transmission and distribution. Until recently, the fossil fuel industry preferred placing the converters and power system equipment for supplying the subsea loads onshore or on the offshore vessels at the top side of the ocean. Because of the harsh environment at the seabed, the installation process of heavy equipment is challenging and expensive. The concept of placing power conversion systems near the loads often termed as 'Subsea Factory', is gaining more prominence. One of its main benefits is the cost reduction of power conversion systems with the same reliability index when converters and distribution systems are installed on the ocean floor. Hence, manufacturers are

producing more equipment suitable to work in harsh subsea environments [1], [70]. A study of the reliability of small and large offshore grids is done in [71]. Any failure in the subsea power system will be costly and will lead to repair or replacement in harsh conditions [1]. In response to this growing demand for smaller and less expensive energy conversion, this dissertation aims to propose a new configuration of MVDC distribution architecture along with isolated modular DC/DC converters for the subsea application. The concept lay on series stacked medium frequency (MF) SST topology with voltage-fed isolated DC/DC converters and presented the basic analysis with simulation results. Focusing on the subsea application, the detailed description, small-signal modeling, finite element analysis (FEA), along experimental results are presented.

Once the DC/DC converter is designed and implemented, the reliability evaluation procedure starts to measure the Remaining-Useful-Lifetime (RUL) of both components and the whole power converter. Therefore, a power cycling (PC) and thermal cycling (TC) test bench to perform accelerated life testing for reliability assessment of SiC-MOSFET in the harsh high-temperature offshore environment. The captured data from the Device-Under-Test (DUT) in different ambient temperatures are envisioned and provide critical information about the failure mechanisms and lifetime characteristics of power devices. The provided lifetime characteristics data of SiC-MOSFET will be used to statistically estimate the RUL of a component in a real application.

Besides, a new method for evaluating the survival index (system-level RUL) of power converters is also proposed. This method aims to address the issues by developing a statistical approach using probability density functions (PDFs) and associated concepts in measure theory to predict the probability of system failure using individual components' qualification data. An accelerated hardware setup for power and thermal cycling on DUT is implemented, and degradation data is captured for post-processing. A new H-bridge-based lifetime test setup is also proposed to degrade the DUT based on the thermal equilibrium index. Focusing on the system-level operation, this research proposes a new real-time reliability prediction approach using ANN-based for power FET devices and power converters.

1.4. Outline of Dissertation

This dissertation is organized into six chapters. CHAPTER 1 introduces the research background of subsea electrification along with HVAC system challenges in offshore electrification. Different MVDC/HVDC structures for voltage conversion are reviewed, and converter topologies are discussed, considering the benefits and drawbacks. Then, to investigate the necessity of having reliable and fault-tolerant topology is discussed, and different methods are introduced to understand RUL evaluation in power converters.

CHAPTER 2 proposes a radial MVDC distribution system for offshore applications, primarily subsea fossil extraction. An ISOSP (input series output series-parallel) isolated DC/DC converter is also proposed to convert desired MVDC voltage levels that benefit from fault-tolerance capability with SST configuration.

In order to evaluate reliability indices for the proposed DC/DC converter, a novel statistical methodology is introduced in CHAPTER 3 and CHAPTER 4. A power cycling (PC) and thermal cycling (TC) test bench to perform accelerated life testing for reliability assessment of SiC-MOSFET and Aluminum Electrolytic Capacitor (AEC) in the harsh high-temperature offshore environment is proposed in CHAPTER 3. In CHAPTER 4, a new method for evaluating the survival index (system-level RUL) of power converters is proposed. This method aims to address the issues of predicting RUL of component and power converters by developing a statistical approach using probability density functions (PDFs) and associated concepts in measure theory to predict the probability of system failure using individual components' qualification data.

Experimental results for the proposed system-level reliability evaluation of the proposed fault-tolerant DC/DC converter are discussed in CHAPTER 5. It is shown that the proposed online health monitoring procedure can measure the remaining time of operation in the future for the converter based on the present values of health indicators.

A summary of contributions introduced in this dissertation is covered in CHAPTER 6.

CHAPTER 2.

ISOLATED MULTILEVEL HVDC CONVERTER FOR OFF-SHORE DC DISTRIBUTION

2.1. MVDC Configuration for Subsea Electrification

The MVDC power transmission is gaining importance in subsea applications due to its advantage of operating with power networks with different frequencies, precise and instant control of power, and negligible reactive power consumption. Considering the benefits of sending DC power to the load for transmission distances over 550 km, the MVDC system overcomes high voltage AC transmission. However, in underground and subsea applications, a few studies have shown that the breakeven distance reduces to about 50 km, considering higher reactive power [1]. MVDC transmission shows improvements for step-out distances greater than 50 km, as cable capacitance in the subsea power umbilical is significant [72]. For long-distance subsea tieback, several power converter blocks can be stacked in series, both on the sending-end and at the receiving end, which is named MSDC in [49].

This research proposes an ISOSP (input series output series-parallel) isolated DC/DC converter as a fault-tolerant SST in MVDC configuration (Figure 2-1) for offshore applications, primarily subsea fossil extraction. It is assumed that AC power is generated offshore and then transferred to the desired DC level using an MVDC rectifier on a top-side vessel. The tieback is split into the different locations of loads by using an MVDC distribution hub. The load-side converters consist of isolated DC/DC converter

modules to form SSTs to step-down the voltage level from 36 kV to 6 kV, followed by a DC/AC inverter. The MVDC voltage levels may vary depending on the power and distance. The resulting voltage is fed to VFDs, which run the motors for pumps, compensators, etc. Wet-mate connectors and penetrators are significant barriers to subsea power transmission and distribution [1].

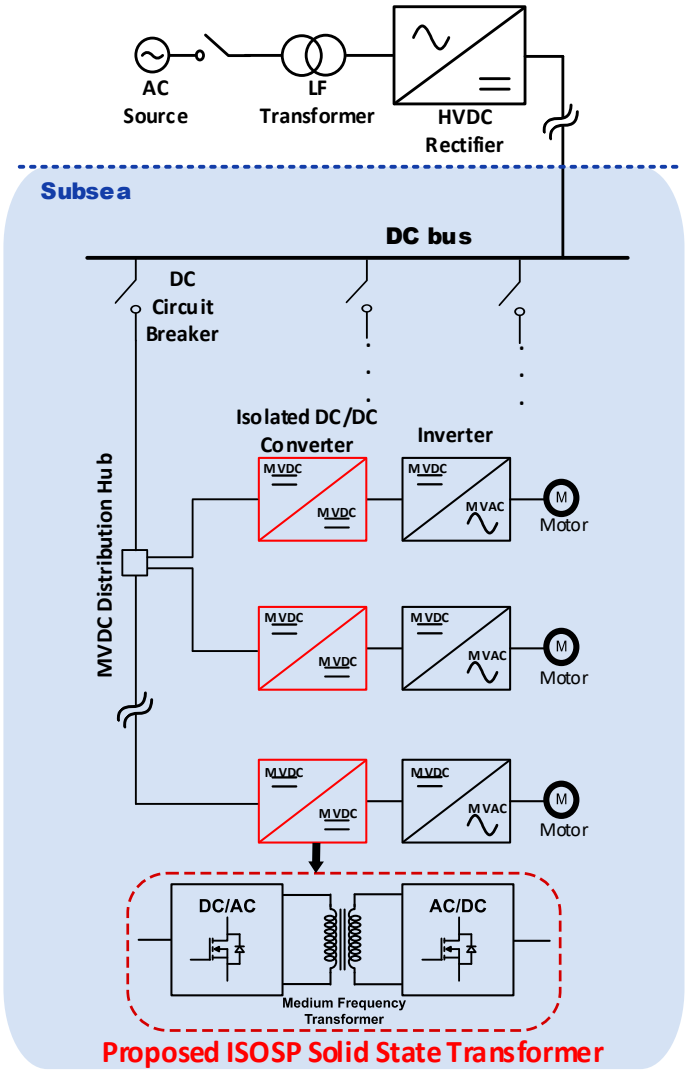


Figure 2-1. The proposed Radial DC distribution for subsea application with the proposed ISOSP SST converter

The use of the proposed power conversion configuration in subsea electrification will limit the number of penetrators and connectors, needing only one connector for input and one output connector for the load (motor, pump, etc.). This benefit is important in subsea applications since it can reduce the chance of failure for the whole system caused by any damage in penetrators. The main focus of this paper is the MVDC SSTs on the load-side. The proposed fault-tolerant SST structure has many advantages, which are listed below:

- High switching frequency is favored to minimize the size of passive components, especially isolation transformers addition with minimal size in footprint.
- Higher operational flexibility due to direct transmission from DC to DC without AC interference.
- The soft-switching technique helps to limit switching losses and increase further reduce system size.
- Closed-loop control guarantees constant output voltage with minimum ripple even under faulty operation mode.
- SiC-MOSFET-based converter results in lower losses and more efficiency.
- High reliability and fault-tolerance are possible with redundancy in modular DC/DC converter design.

2.2. Proposed Fault-tolerant Solid State Transformer (SST)

Isolated DC-DC SST must provide galvanic isolation from the MVDC transmission line and support a rigid DC link for motor drives. This paper assumes that the SST's primary DC voltage, secondary DC voltage, and peak load power are 36 kV,

6 kV, and 6 MW, respectively. The number of modules is decided considering voltage conversion ratio, switch blocking voltages, and load. The SST for the given specifications requires 24 isolated DC/DC converter modules using MF transformers, with the high voltage primary side cascaded in series and the lower voltage secondary side arranged in series-parallel configuration (ISOSP), as shown in Figure 2-2. Secondary side voltage is fed to a VFD, which is not studied in this research.

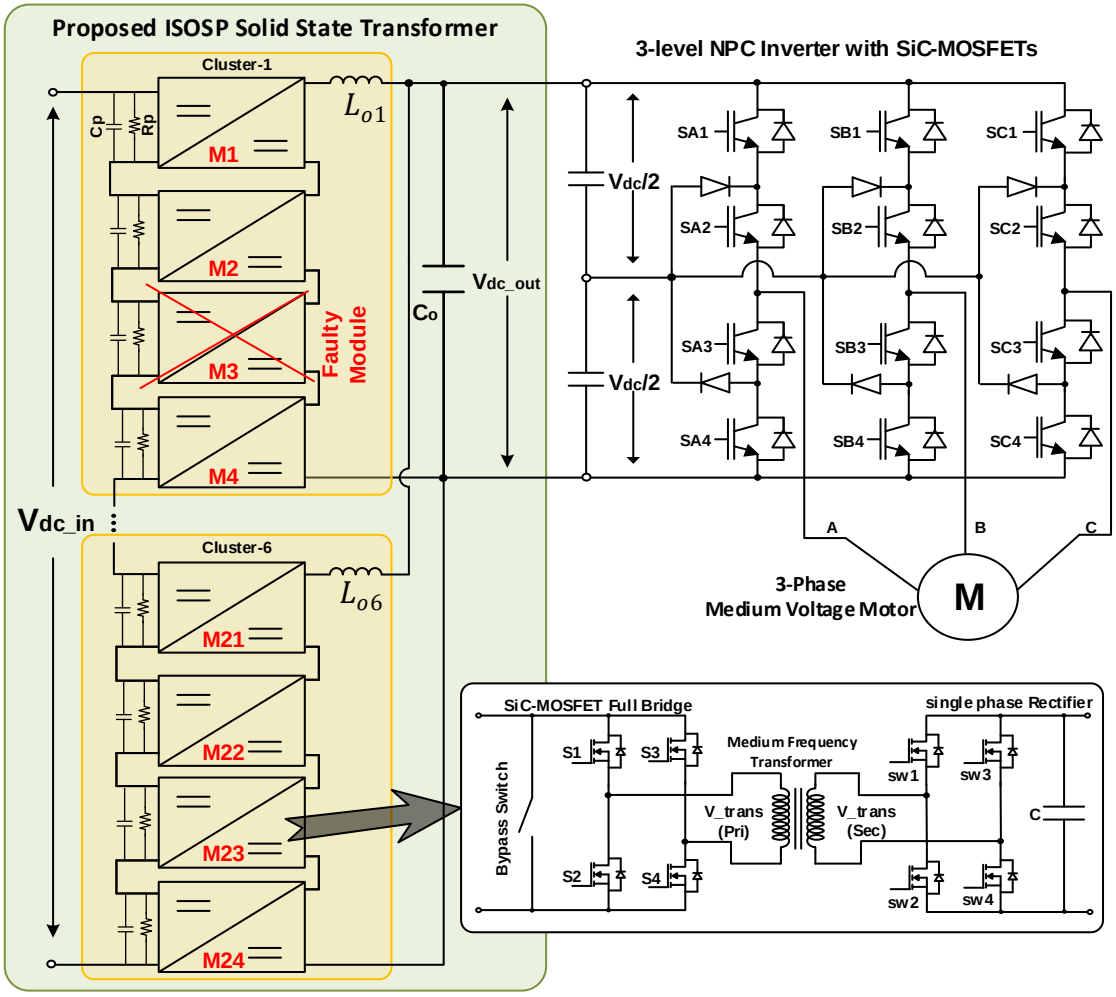


Figure 2-2. The proposed fault-tolerant ISOSP isolated DC/DC SST configuration using medium frequency transformer

The voltage on the primary side is divided among the individual 24-cascaded modules so that regular 3.3 kV rated SiC-MOSFETs introduced in [73] can be used. This SST can also be achieved by having only eighteen modules on the primary side, but to have redundancy, six additional modules are included to withstand higher voltage to enable post-fault regular operation. There are six clusters and four DC/DC modules in each cluster. Each cluster processes 1 MW of the total of 6 MW load power. In each cluster, four modules are series-connected to produce the desired 6 kV DC link voltage. Using SiC-MOSFETs, the higher switching frequency is favored to minimize the size of passives, especially isolation transformers.

High reliability and fault-tolerance are possible with redundancy in this design. In this work, the converter system faults are of primary consideration, where the power device (e.g., SiC-MOSFET, capacitor, gate driver, etc.) in a particular module fails during the operation. However, another benefit of the proposed topology is that it can also isolate faults outside the converter system when needed due to the in-built redundancy and the ISOSP architecture. Therefore, to isolate the occurred fault (fault detection is not focused in this research and is out of the scope), the bypass switch in the faulty module operates. That causes a sudden change in the voltages and currents in the modules. A methodology for fault detection and diagnosis is explained in [47], where currents of full-bridge switches are sensed, and the pulse duty ratio is estimated with a sampling frequency above switching frequency. Once the fault occurs, the current pulse duty ratio will not be 50 %, and it is hence possible to detect the faulty operation. Therefore, when there is a fault in one of the modules in a cluster (i.e., M3 in Figure

2-2), the faulty module will be bypassed using a relay and switches connected in parallel with the primary side of each module; while the other three modules will tolerate the higher voltage condition to produce the same output voltage when the fault has occurred. This advantage can help in significantly minimizing the costs and efforts by reducing the downtime in reliability-critical subsea or offshore operations. This capability is described in the next section.

Also, a resistor and a capacitor (R_p and C_p) are paralleled with each module to split input voltage equally among modules. Further, inductors (L_o) are used to balance currents among the clusters. Since the secondary sides of the cluster of modules are in parallel, the voltage of each cluster is fixed at 6 kV. Hence, if a module in a cluster fails, the secondary voltages of each of the other modules in the same cluster will re-organize to carry a proportionately higher voltage. This gets reflected back to the primary in a balanced manner with the presence of the near-identical MF transformers and voltage balancing R_p – C_p. The balancing resistance was calculated by analyzing the characteristics of the sub-module circuit. The following method is used to calculate the equalizing resistor [74]:

1. Determine the leakage current of the capacitor ($\mathrm{I}_{leakage\_capacitor} = 0.01 \times CV$).
2. Calculate the DC resistance value of the capacitor using the equation

$$R_{DC} = \frac{V_{rated}}{\mathrm{I}_{leakage}} = \frac{V}{0.01 \times CV} = \frac{100}{C}. \quad (2.1)$$

3. Balancing resistor value will be 10 % of the calculated DC resistance value

$$R_{balance} = 10\,\% \times R_{DC} = \frac{10}{C} = \frac{10}{600\mu F} = 17\ \mathrm{k\Omega} \quad (2.2)$$

where, for safety purposes, $R_{balance}$ = 22.5 kΩ.

The input voltage of each module in the hardware prototype is 50 VDC ($V_{module} = \frac{V_{input}}{\text{Number of modules}} = \frac{200}{4} = 50\,V$). Therefore, the loss of each balancing resistance would be as

$$P_{loss} = \frac{V^2}{R_{balance}} = \frac{50^2}{22.5\times10^3} \approx 112\,mW. \quad (2.3)$$

For the design of an actual 300 kW system with 24 total number of modules, a maximum 2.0 kV input voltage, and a 1200 μF input capacitor for each module, the same procedure is followed, and $R_{balance}$ is calculated to be 20 MΩ.

As it can be seen, the P_{loss} of equalizing resistors compare to three other major losses (switching, transformer, and power conduction) is very minimal; therefore, it is negligible to consider power loss of equalizing resistor in loss analysis. The calculated values of balancing resistors in both simulation and hardware setup are indicated in Table 2.1.

Table 2.1 The specification of the proposed converter

Parameter	Simulation	Hardware
Input Voltage	36 kV	200 V
Output voltage	6.0 kV	100 V
Maximum output power	6.0 MW	800 W
Number of modules	24	4
Switching frequency	20 kHz	20 kHz
Transformer magnetizing inductance	10 mH	3.84 mH
Transformer leakage inductance	2.8 μH	2.84 μH
Voltage balancing resistor	20 MΩ	22.5 kΩ

The bidirectional structure of the individual modules assists here in the voltage balancing, and the transformer turns ratio can be 1:1. The duty cycle of individual switches in each module will range between 0.375 and 0.5 to support transient and fault conditions.

In the proposed topology, the inputs of all modules are connected in series; it means that the primary current of all transformers would be of the same value. On top of that, using voltage balancing resistors (R_p) for all paralleled capacitors (C_p) secures nearly equal voltage division and results in equal power-sharing, thereby limiting the circulating currents in the modules. Therefore, there is hardly any change in the primary current of isolating transformers. All transformers are designed and built with the same specification and have an equal 1:1 turn ratio. As it is shown in Figure 2-3, if we consider output current (load current) as I_{out}, since we have two parallel clusters in the hardware setup (actual system with 24 modules and 6 clusters also would follow the same logic), each parallel cluster will have the same current value as $\frac{I_{out}}{2}$ by the above reasoning. Moreover, the proposed fault-tolerant DC/DC topology is based on voltage-fed input with closed-loop output voltage control. Therefore, the output voltage of each cluster is also regulated around the same value. Considering the same current and voltage for each cluster, power will be shared equally. Besides, when there is a fault in one of the modules in a cluster, the faulty module will be bypassed using a relay and switches connected in parallel with the primary side of each module; while other modules in the same cluster will tolerate higher voltage condition to produce the same output voltage. Further, inductors (L_o) are used to balance currents among the clusters. Hence, if a

module in a cluster fails, the secondary voltages of each of the other modules in the same cluster will re-organize to carry a proportionately higher voltage. This gets reflected back to the primary in a balanced manner with the presence of the near-identical MF transformers and voltage balancing.

In the worst-case scenario, the possibility of having a circulating current is more likely to happen for a very short period only during the transient time when one of the modules in one cluster is bypassed, and there is a mismatch output voltage among the clusters. The impedance of current in this situation is the sum of transformers leakage inductance ($L_{leakage}$) plus output filter inductance (L_o). The calculation of transient circulating current for hardware setup is as equation

$$I_{circulating_{transient}} = \frac{\Delta V}{2\times\omega L} = \frac{V_{out2}-V_{out1}}{2\times 2\pi f\times\left(L_{leakage}+L_o\right)} \tag{2.4}$$

$$= \frac{100-50}{2\times 2\pi\times 20\times 10^{3}\times(2.8\times 10^{-6}+600\times 10^{-6})} = 3.3\ mA.$$

This circulating current, compared to the output current of each cluster, is negligible, and it will be balanced when it reflects the primary side of the transformer. In any case, a separate cluster-level current sharing mechanism may be implemented in addition to the existing primary side voltage balancing technique for a practical application to further enhance the system resiliency.

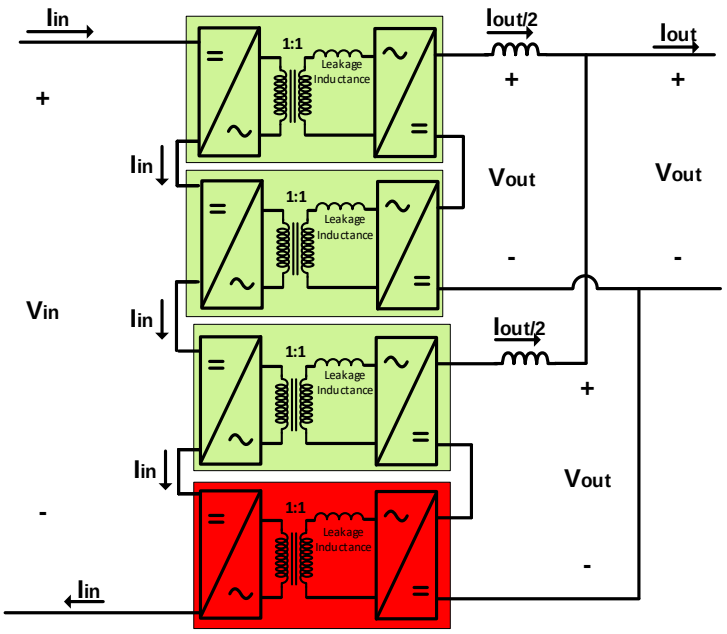


Figure 2-3. Power-sharing schematic for hardware setup (red module when it is bypassed)

2.3. Output Filter Design

To generate an output with minimum ripple in voltage and current, a low-pass LC-filter consisting of an inductor (L_0) and a capacitor (C_0) are used for the output of each cluster of modules. For the output filter capacitor, it is assumed that the peak-to-peak voltage ripple (ΔV) of the capacitor should be less than 5 % of the output voltage. The value of filter components is calculated based on the output voltage of the transformer. The variation of V_{sec_peak} is between 1.5 kV and 2.0 kV (details discussed in the following sections). Therefore, the operating duty cycle of the inverter will adjust to generate the desired output voltage. The maximum transformer secondary voltage (2.0 kV) is during steady-state operating conditions after fault occurrence.

The first step is to choose an output filter inductor. In the filter inductance calculation is assumed that the inductor current is not discontinuous. In Figure 2-4, the voltage and current of the inductor are shown, and based on the voltage across the inductor; the parameter L_0 can be calculated as

$$\frac{\Delta I}{2} = \mathrm{I}_{\mathrm{out}_{\mathrm{min}}} = \frac{V_L}{L_o} \times t_{on} = \frac{V_{sec-peak} - V_{out}}{L_o} \times t_{on}. \quad (2.5)$$

where ΔI is current ripple, I_{out_min} is minimum output current (5% of $I_{out_{nom}}$), V_L is the voltage across the inductor, L_o is filter inductance, t_{on} is switch on-state time and $V_{\mathrm{sec}_{peak}}$ is the peak value of transformer secondary voltage. The filter inductance can be calculated from (2.5) as

$$L_o = \frac{V_{\mathrm{sec}_{peak}} - V_{out}}{\Delta I} \times t_{on}. \quad (2.6)$$

The output voltage is defined as

$$V_o = \frac{2 \times t_{on}}{T} \times V_{\mathrm{sec}_{peak}}. \quad (2.7)$$

The value of filter components is calculated based on the output voltage of the transformer. The variation $V_{\mathrm{sec}_{peak}}$ is between 1500 and 2000 volts (details will be discussed in the next sections). Therefore, the operating duty cycle (D) of the inverter will change to generate the desired output voltage. The worst operating point is at maximum transformer secondary voltage with the minimum duty cycle.

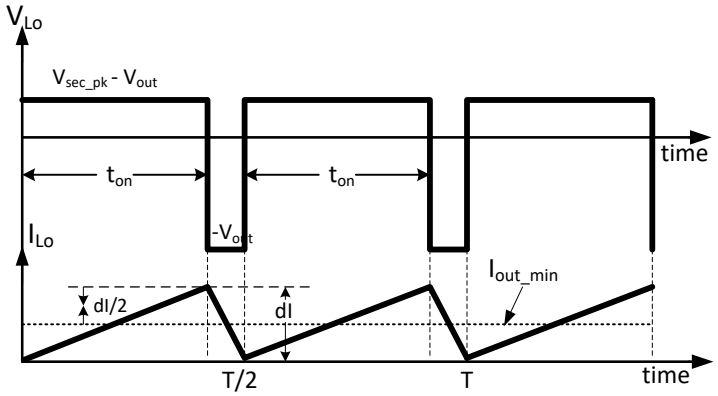


Figure 2-4. The voltage and current of the output filter inductor

The switch on-state time is

$$t_{on} = \frac{V_{out}}{V_{\sec_{peak}}} \times \frac{T}{2} = \frac{DT}{2}. \quad (2.8)$$

Therefore, the peak value of the transformer secondary voltage can be written as

$$V_{\sec_{peak}} = \frac{V_{out}}{D}. \quad (2.9)$$

By placing (2.8) and (2.9) in (2.5), the filter inductance equation would be

$$\Delta I = \frac{V_{\sec_{peak}} - V_{out}}{L_o} \times \frac{D}{2f} = 2 \times I_{out\_min}, \quad (2.10)$$

where, $f = \frac{1}{T}$ is switching frequency of the inverter.

The next step is choosing the output filter capacitor. It is assumed that the ripple voltage of the capacitor is 5% of the output voltage. Therefore, the capacitor value of the output filter can be calculated as

$$C_o = \frac{\Delta I \times t_{on}}{V_{ripple}} = \frac{\Delta I \times DT}{V_{ripple}} = \frac{\Delta I \times D}{f \times V_{ripple}}. \quad (2.11)$$

It is clear that filter components have a reverse relation with switching frequency, and working in high frequency will result in reducing the filter components value. The summary of the filter component calculation is provided in Table 2. 2. The

chosen values for the module's output filter for the worst-case ΔI of $\pm$ 20 % based on simulation voltage levels are $C_o = 10\ \mu F$ and $L_o = 13\ mH$.

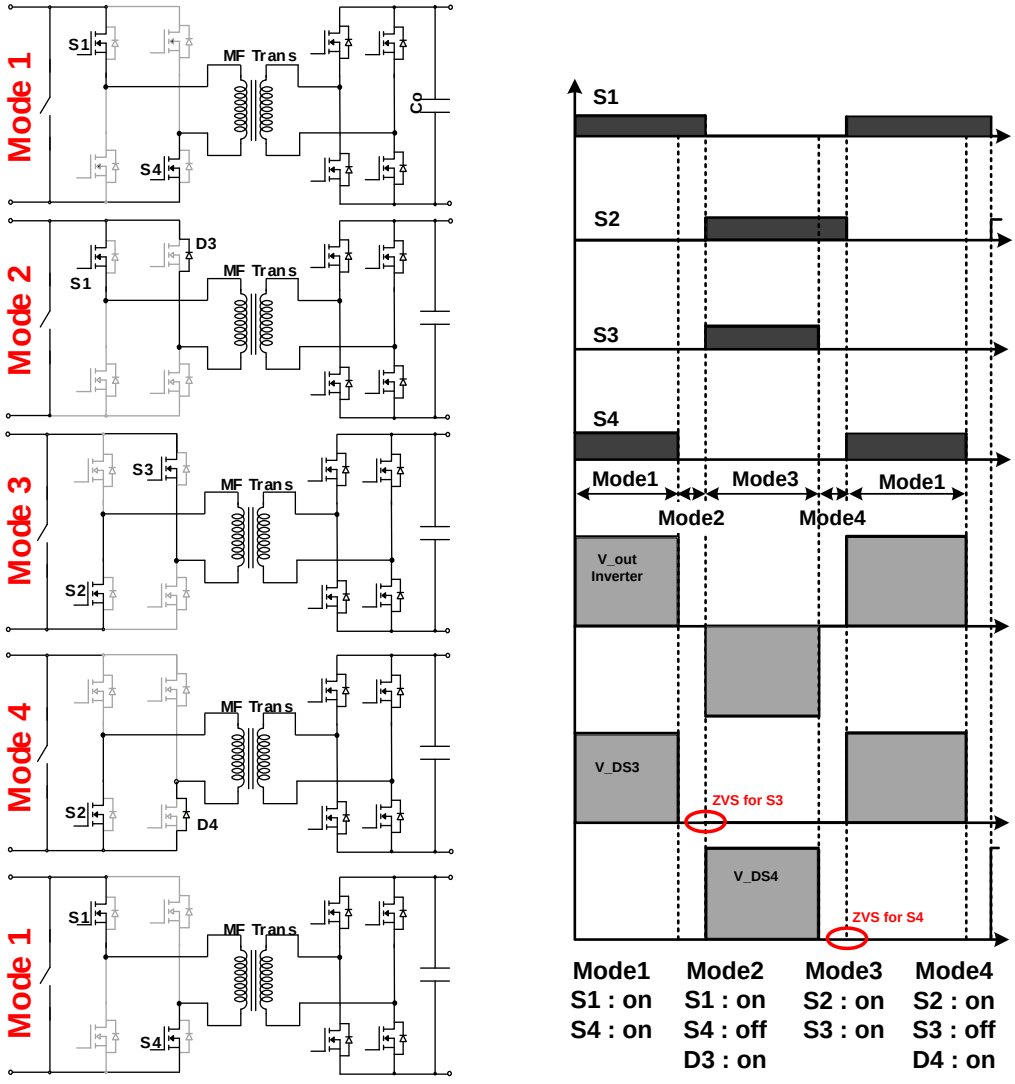
Table 2.2 Calculated filter components for different operating points

Amplitude value of V_{sec_eak}	1500 V	2000 V
Switch duty cycle (D)	$\frac{T}{2}$	$0.8 \times \frac{T}{2}$
Output Filter inductor (L_o)	1.125 *mH*	1.2 *mH*
Output Filter Capacitor (C_o)	8.9 µF	6.68 µF

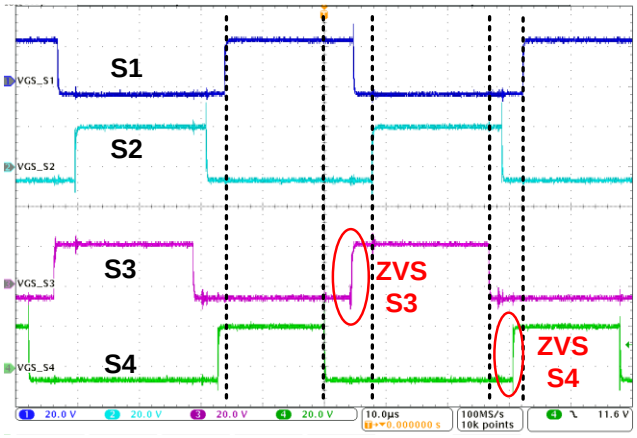
2.4. Zero Voltage Switching (ZVS)

To have zero voltage switching (ZVS) capability, an appropriate soft-switching technique is implemented, as described using Figure 2-5. There is a dead-time between S1 and S4 and also between S2 and S3 to ensure ZVS operation, described under Mode-2 and Mode-4, respectively. During this dead-time, i.e., Mode-2, S1 is still turn on, but S4 will be turned off. The transformer's primary current should find a path to flow. Therefore, D3 (diode across S3) will conduct. At the end of Mode-2 operation time, Mode-3 starts after the voltage across S3 has already become zero, enabling ZVS turn-on for S3. To keep the converter output voltage constant for the whole operating time, a traditional closed-loop PI voltage controller for hardware setup, as shown in Figure 2-6, is implemented in dSPACE-RTI1202. The gate pulses of switches are generated by the following procedure. First, the output voltage of the converter is measured by the LEM voltage sensor, and using ADC, the error signal between reference and the actual voltage goes to the controller, then the proper duty cycle is calculated. Using logical

AND gate, the duty cycle is compared with a fixed 20 kHz pulse, and then gate pulses of S3 and S4 switches are generated. The gate pulses for S1 and S2 are complementary ePWM with 20 kHz frequency. All gate pulses are sending to gate driver boards, and proper switching patterns are achieved. As per Figure 2-2, a 3-level Neutral Point Clamp (NPC) or a modular three-phase multilevel inverter presented in [75] can be connected at the output stage of the power conversion system to offer speed and torque control for MVAC motors.



(a) (b)



(c)

Figure 2-5. Gate signals and ZVS in each module (D1, D2, D3, and D4 are reverse diode connected to SiC-MOSFETs) (a) Operation modes (b) pulses and voltages (c) experimental gate pulses

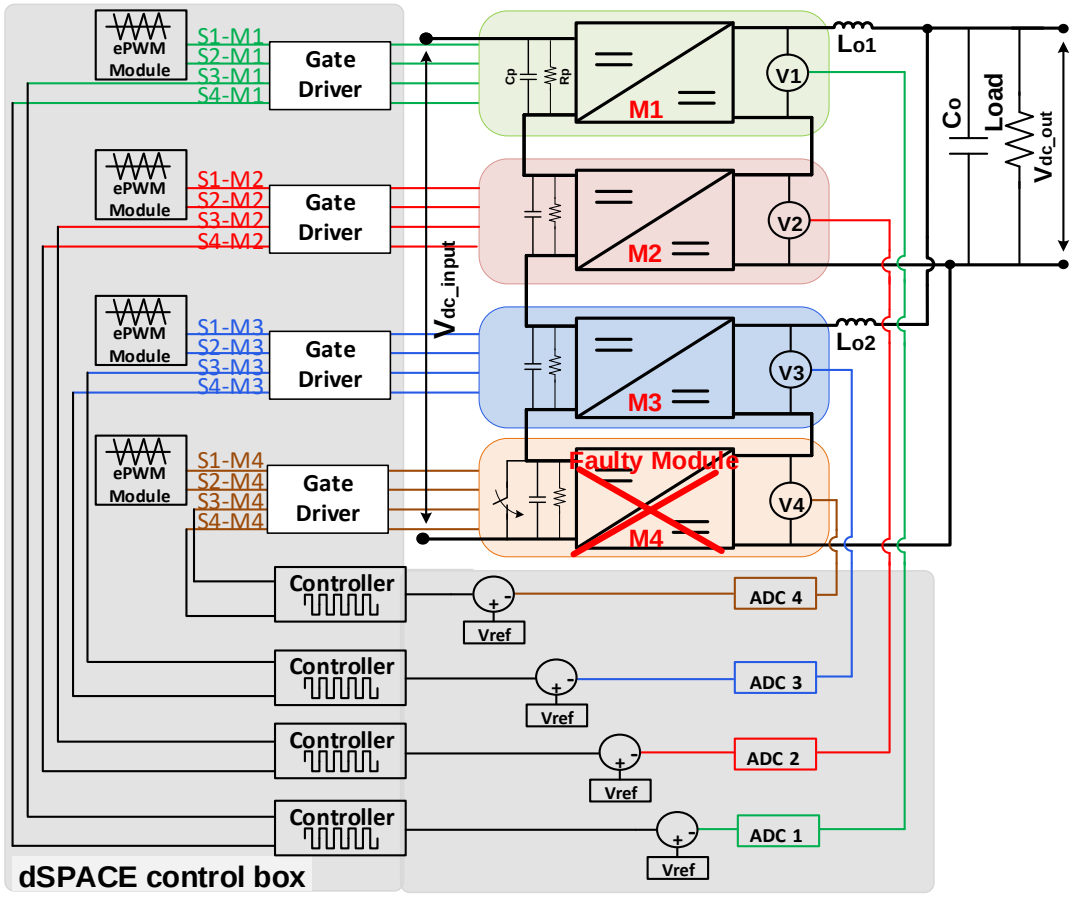


Figure 2-6. The schematic of the closed-loop voltage controllers implemented in dSPACE-RTI1202

2.5. Small Signal Model Derivation

In this sub-section, the small-signal equivalent circuit of the proposed fault-tolerant converter is discussed. An analytical model of the ISOP (input series output parallel) modular converter with a common input filter has been discussed in [76]. ISOSP configuration requires a more comprehensive equivalent circuit, as proposed in this paper (see Figure 2-7).

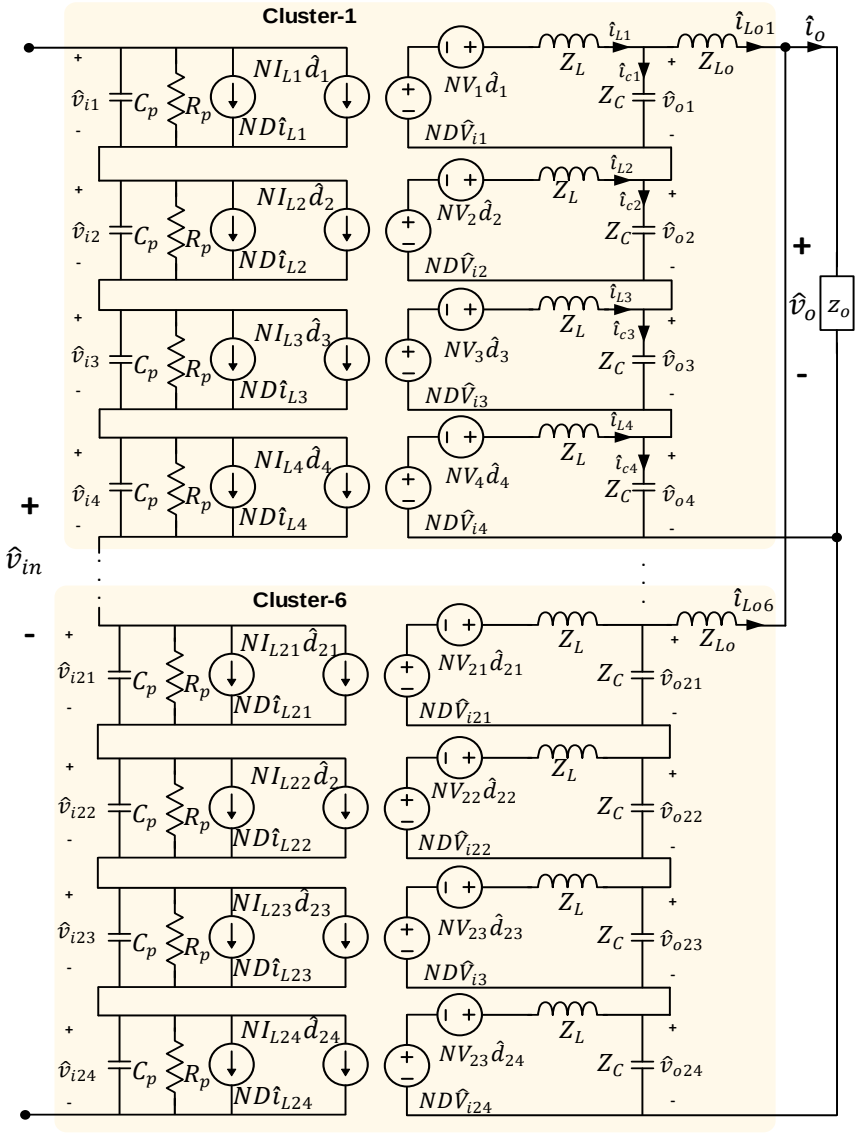


Figure 2-7. The small-signal modeling of the proposed fault-tolerant SST

A detailed model of the proposed SST consists of 'K' clusters in parallel, 'm' operational modules in a particular cluster, and '$K \times m$' total modules (here, 24). The effect of parasitic and parallel components is considered impedance. It is assumed that all modules have similar characteristics (equal impedances) and working at the same operating point (equal input voltage of $V_{i1} = V_{i2} = \cdots = V_{i24} = \frac{V_{in}}{K \times m}$, output current and duty cycle D). Magnetizing inductance is assumed to be high and excluded.

While [76] provided an equivalent model, it didn't consider the transformer leakage inductance, which can be critical in designing the control parameters. Several such models presented in the literature also exclude the leakage inductance. It is complex to arrive at a mathematical equivalent on the transformer side of the phase-shifted full-bridge converter module due to the negligible DC component and the presence of several higher frequency harmonic terms (present in quasi-square wave voltage and near-trapezoidal current).

In this research, a simple empirical analysis was performed on the 'output voltage to duty cycle' transfer function of the individual full-bridge module using the 'AC Sweep' feature of the PSIM software (Figure 2-8). The equivalent leakage inductance was added on the transformer secondary side (Figure 2-8(a)), and it was compared with the same inductance value placed on the DC side of the rectifier (Figure 2-8(b)). The simulation results, including the comparison of Bode plots, are shown in Figure 2-9. It can be seen that they are identical, as the effect of higher frequency terms on the impedance balance out. Hence, the small-signal model shown in Figure 2-7 can be justified. Considering the bode plot of the proposed small-signal model of full-bridge

converter, the K_p and K_i coefficients of the PI controller can be tuned to achieve a fast response with minimal overshoot.

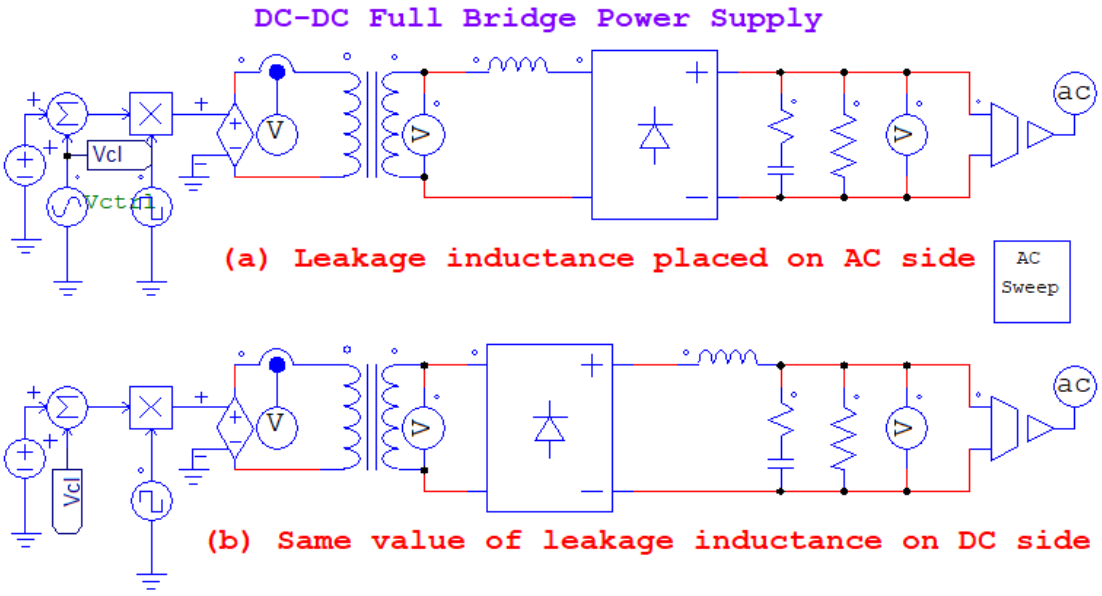


Figure 2-8. PSIM AC Sweep (Bode Plot) simulation set-up

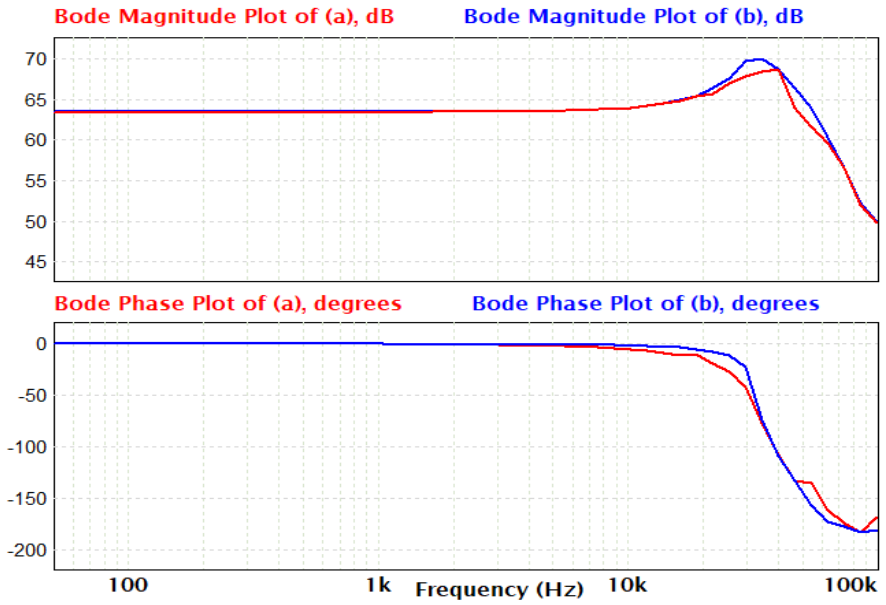


Figure 2-9. PSIM AC Sweep (Bode plot) results corresponding to Figure 2-8

The most important parameters for the mathematical model are:

$\hat{v}_{ij}$: Input voltage of module-*j* (*j*=1:24)

$\hat{v}_{oj}$: The output voltage of module-*j*

$\hat{d}_j$: The duty cycle of module-*j*

ω : Frequency of perturbation

$Z_L \cong j\omega L$: Transformer parasitic impedance

$Z_{Lo} = R_{Lo} + j\omega L_o$: Cluster's output filter impedance

$Z_c = \frac{1}{j\omega C}$: Each module parallel capacitor impedance

$Z_o = R_o \,||\, Z_{co}$

$Z_{co} = \frac{1}{j\omega C_o}$: Total output impedance

$\hat{\imath}_{Lok}$: The output current of cluster-*k* (here, *k*=1:6)

$\hat{\imath}_{Lj}$: The output current of module-*j*

$\hat{\imath}_{cj}$: The current of output parallel capacitor in module-*j*

N : Transformer turn ratio (here 1:1)

The output voltage of each module can be expressed as:

$$\hat{v}_{o1} = ND(\hat{v}_{i1}) + NV_{i1}(\hat{d}_1) - Z_L\hat{\imath}_{L1}. \quad (2.12)$$

$$\hat{v}_{o2} = ND(\hat{v}_{i2}) + NV_{i2}(\hat{d}_2) - Z_L\hat{\imath}_{L2}. \quad (2.13)$$

$$\hat{v}_{o3} = ND(\hat{v}_{i3}) + NV_{i3}(\hat{d}_3) - Z_L\hat{\imath}_{L3}. \quad (2.14)$$

$$\hat{v}_{o4} = ND(\hat{v}_{i4}) + NV_{i4}(\hat{d}_4) - Z_L \hat{\imath}_{L4} \tag{2.15}$$

where

$$\hat{\imath}_{L1} = \hat{\imath}_{Lo1} + \hat{\imath}_{c1} \quad ; \quad \hat{\imath}_{c1} = \frac{\hat{v}_{o1}}{Z_C} \tag{2.16}$$

$$\hat{\imath}_{L2} = \hat{\imath}_{Lo1} + \hat{\imath}_{c2} \quad ; \quad \hat{\imath}_{c2} = \frac{\hat{v}_{o2}}{Z_C} \tag{2.17}$$

$$\hat{\imath}_{L3} = \hat{\imath}_{Lo1} + \hat{\imath}_{c3} \quad ; \quad \hat{\imath}_{c3} = \frac{\hat{v}_{o3}}{Z_C} \tag{2.18}$$

$$\hat{\imath}_{L4} = \hat{\imath}_{Lo1} + \hat{\imath}_{c4} \quad ; \quad \hat{\imath}_{c4} = \frac{\hat{v}_{o4}}{Z_C}. \tag{2.19}$$

Summation of equations (2.12 - 2.15) and operating with equations (2.16 - 2.19) result in equation

$$(\hat{v}_{o1} + \cdots + v_{o4}) = ND(\hat{v}_{i1} + \cdots + v_{i4}) + \frac{NV_{in}}{K \times m}(\hat{d}_1 + \cdots + \hat{d}_4) - Z_L \Bigg(4\hat{\imath}_{Lo1} + \frac{1}{Z_C}(\hat{v}_{o1} + \cdots + \hat{v}_{o4}) \Bigg). \tag{2.20}$$

The same calculation can be derived for other clusters, e.g., for cluster-6

$$(\hat{v}_{o21} + \cdots + v_{o24}) = ND(\hat{v}_{i21} + \cdots + \hat{v}_{i24}) + \frac{NV_{in}}{M}(\hat{d}_{21} + \cdots + \hat{d}_{24}) - Z_L \Bigg(4\hat{\imath}_{Lo6} + \frac{1}{Z_C}(\hat{v}_{o21} + \cdots + \hat{v}_{o24}) \Bigg). \tag{2.21}$$

Considering calculation for all 24-modules, the modules output voltage can be described as follow

$$(\hat{v}_{o1} + \cdots + \hat{v}_{o24}) = ND(\hat{v}_{i1} + \cdots + \hat{v}_{i24}) + \frac{NV_{in}}{K \times m}(\hat{d}_1 + \cdots + \hat{d}_{24}) - 4Z_L \Bigg(\underbrace{\hat{\imath}_{Lo1} + \cdots + \hat{\imath}_{Lo6}}_{\hat{\imath}_o = \frac{\hat{V}_o}{Z_o}} \Bigg) - \frac{Z_L}{Z_C}(\hat{v}_{o1} + \cdots + \hat{v}_{o24}) \tag{2.22}$$

and

$$\left(1+\frac{Z_L}{Z_C}\right)\left(\underbrace{\hat{v}_{o1}+\cdots+\hat{v}_{o24}}\right)=ND(\hat{v}_{i1}+\cdots+\hat{v}_{i24})+\frac{NV_{in}}{K\times m}\left(\hat{d}_1+\cdots+\hat{d}_{24}\right)-4\frac{Z_L}{Z_C}\hat{v}_o. \tag{2.23}$$

The outer voltage loop in each cluster can be derived as:

$$(\hat{v}_{o1}+\cdots+\hat{v}_{o4})-Z_{Lo}\hat{\imath}_{Lo1}=\hat{v}_o, \tag{2.24}$$

$$(\hat{v}_{o5}+\cdots+v_{o8})-Z_{Lo}\hat{\imath}_{Lo2}=\hat{v}_o, \tag{2.25}$$

…

$$(\hat{v}_{o21}+\cdots+\hat{v}_{o24})-Z_{Lo}\hat{\imath}_{Lo6}=\hat{v}_o. \tag{2.26}$$

Summation of equations (2.23 - 2.25) for all 6 clusters results in

$$(\hat{v}_{o1}+\cdots+v_{o24})-Z_{Lo}\left(\underbrace{\hat{\imath}_{Lo1}+\cdots+\hat{\imath}_{Lo6}}_{\hat{\imath}_o=\frac{\hat{V}_o}{Z_o}}\right)=6\hat{v}_o. \tag{2.27}$$

Therefore, the total output voltage based on each module output voltage can be derived as

$$(\hat{v}_{o1}+\cdots+\hat{v}_{o24})=\left(6+\frac{Z_{Lo}}{Z_o}\right)\hat{v}_o. \tag{2.28}$$

Substituting equation (2.28) in equation (2.23) can give the total equation as

$$\left(1+\frac{Z_L}{Z_C}\right)\left(\underbrace{\hat{v}_{o1}+\cdots+\hat{v}_{o24}}_{eq.\ (17)}\right)=ND(\hat{v}_{i1}+\cdots+\hat{v}_{i24})+\frac{NV_{in}}{K\times m}\left(\hat{d}_1+\cdots+\hat{d}_{24}\right)-4\frac{Z_L}{Z_C}\hat{v}_o \tag{2.29}$$

where

$$\hat{v}_o = \frac{ND(\hat{v}_{i1}+\cdots+\hat{v}_{i24})+\frac{NV_{in}}{K\times m}(\hat{d}_1+\cdots+\hat{d}_{24})}{\frac{1}{Z_O}\left(6Z_O+Z_{Lo}+\frac{Z_L Z_O}{Z_C}+\frac{Z_L Z_{Lo}}{Z_C}+4Z_L\right)}. \quad (2.30)$$

As a generalized form of equation (2.30) for any compatible extension in the number of modules or clusters can be represented as

$$\hat{v}_o = \frac{ND(\hat{v}_{i1}+\cdots+\hat{v}_{iM})+\frac{NV_{in}}{K\times m}\left(\hat{d}_1+\cdots+\hat{d}_M\right)}{\left(K+\frac{Z_{Lo}}{Z_o}+\frac{Z_L * Z_o}{Z_o * Z_C}+\frac{Z_L * Z_{Lo}}{Z_o * Z_C}+m\frac{Z_L}{Z_o}\right)}. \quad (2.31)$$

To analyze the behavior of the proposed model, the derived transfer function in S-domain considering the perturbation of the duty cycle in output voltage is described in equation (2.32). As expected from the equivalent circuit, it is a fourth-order equation.

$$\hat{V}_o(s) = \frac{NV_{in}}{A_4S^4+A_3S^3+A_2S^2+A_1S+A_0}\times\frac{\left(\hat{d}_1(s)+\cdots+\hat{d}_M(s)\right)}{K\times m} \quad (2.32)$$

where:

$A_4 = (l * C * C_o * L)$

$A_3 = \left((R_{Lo} * C * l * C_o)+(L * l * C)\right)$

$A_2 = \left((C_o * L)+(l * C)+\left(\frac{R_{Lo}}{R_o} * l * C\right)+(m * l * C_o)\right)$

$A_1 = \left((R_{Lo} * C_o)+\left(\frac{L}{R_o}\right)+\left(\frac{ml}{R_o}\right)\right)$

$A_0 = \left(K+\frac{R_{Lo}}{R_o}\right).$

The bode plot of the transfer function for the whole 24-module configuration is shown in Figure 2-10. Since four modules are connected in series in each cluster during normal operation, the effective DC gain of the plot in Figure 2-10 is expected to be higher than that of each module (63.5 dB as in Figure 2-9) by $20 \times log(4) \approx 12\ dB$. This value can be easily verified by comparing the bode plots, helping to validate the mathematical model in equation (2.32).

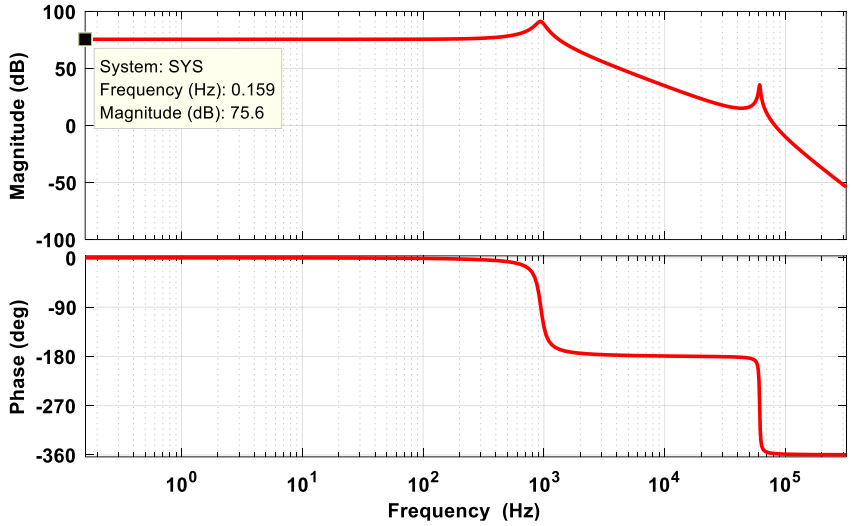


Figure 2-10. The bode plot of the transfer function for the whole 24-module configuration (DC gain value and the two resonant frequencies can be clearly identified)

2.6. Simulation and Real-time HIL Results

The proposed ISOSP DC/DC SST is simulated in MATLAB/Simulink, and the results are presented in this section. Converter simulation parameters are summarized in Table 2.1. The primary purpose is to show how the proposed SST will work under normal operation mode and also can handle an increment in the primary voltage of series-connected modules when one of the modules becomes faulty.

The voltage of each module and the total output DC link voltage of the proposed converter are shown in Figure 2-11. By using a digital closed-loop voltage controller, the output voltage of each module is stabilized at 1.5 kV, and the desired output DC-link voltage is achieved at 6.0 kV. To analyze the fault-tolerant capability of the proposed structure, it is assumed that there is an internal fault in module number 3 (M3) at t=0.005 seconds; therefore, M3 is bypassed.

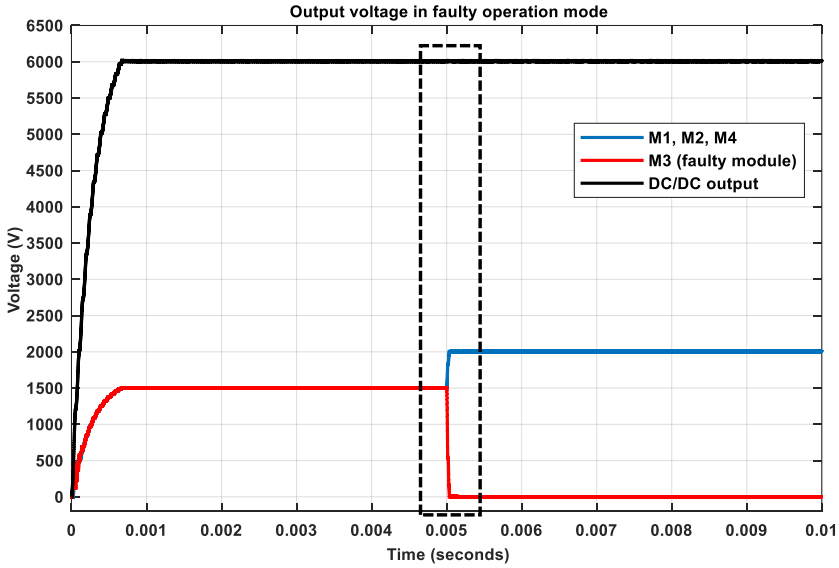
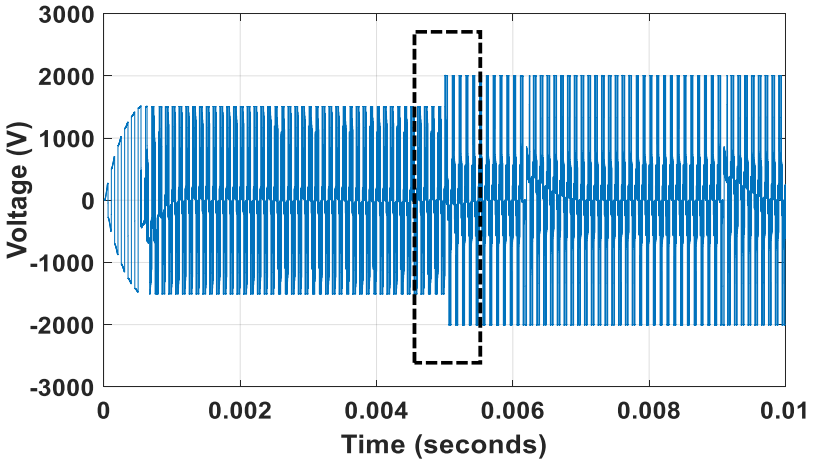


Figure 2-11. The output voltage of DC/DC converter and modules, when there is a fault and M3 is bypassed @ t=0.005 seconds

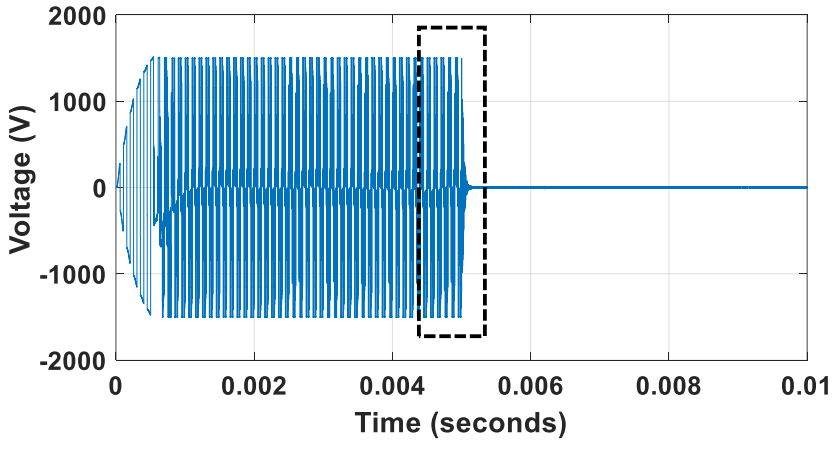
From Figure 2-11, it can be seen that before a fault occurs, the output voltages of series-connected modules within a cluster share the same voltage of 1.5 kV. At t=0.005 s, by turning on the parallel-connected bypass switch, M3 is bypassed. Its voltage then drops to zero, and there are only three modules to produce 6.0 kV at the DC link in the same cluster. Therefore, voltages rise to 2.0 kV for the other three modules (M1, M2, and M4), which is not significantly detrimental for the system's

health or performance considering 3.3 kV SiC-MOSFETs [73]. It means that cluster-level fault-tolerance is achieved, and redundancy is possible in this proposed ISOSP structure.

In this research, each MF transformer is designed to have a 1:1 turn ratio to reduce the losses and minimize the corona effect at high frequencies and voltages. The secondary voltage of transformers in regular and faulty operation modes is shown in Figure 2-12.



(a)



(b)

Figure 2-12. The secondary voltage of transformer in faulty operation mode in (a) module-1 (b) module-3 (when module-3 is bypassed @ *t=0.005*)

Before the fault occurrence, the secondary voltage of transformers is 1.5 kV. At t=0.005 s, when M3 is bypassed, other transformers' voltages go up to 2.0 kV without any interruption in system performance. The voltage of SiC-MOSFET in M1 is shown in Figure 2-13. It is clear that over-voltage on switches, even in faulty operation mode, is up to 2.0 kV, which is tolerable, and no breakdown will happen for 3.3 kV rated power switches.

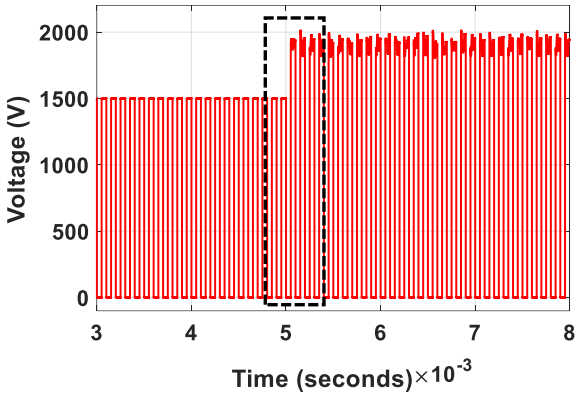
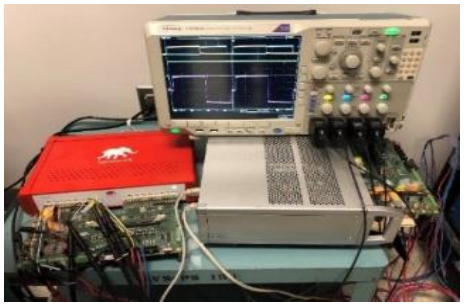
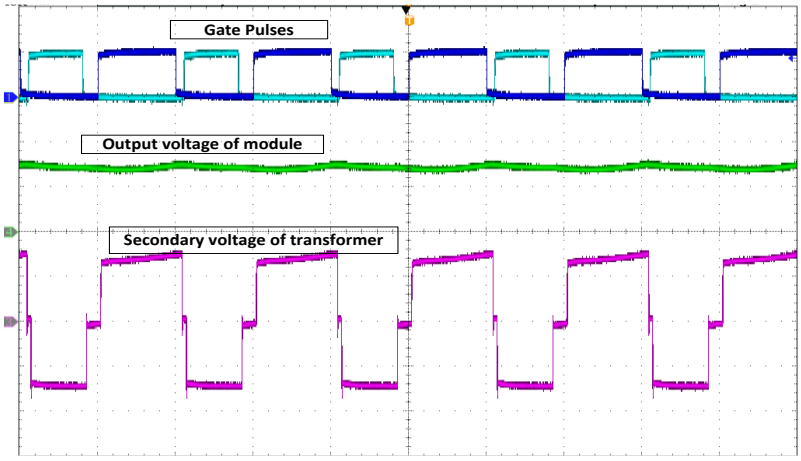


Figure 2-13. The voltage of SiC-MOSFET in M1 when module-3 (M3) is bypassed @ t=0.005

In order to prove the capability of the proposed structure and the control system, the operation of one module in normal and faulty modes was simulated in Typhoon Hardware-in-Loop (HiL, Figure 2-14(a)) before testing on real hardware. As shown in Figure 2-14(b), in normal operation mode, 1.5 kV is applied to the inverter, and a similar rectified output voltage is achieved. The output voltage ripple is less than 5 %, which is acceptable. The secondary voltage of the transformer has a peak value of 1.5 kV. In order to simulate the faulty operation mode of the module, a step change is applied to the input voltage of the inverter to increase from the voltage to 2.0 kV. An increase in the amplitude of transformer secondary voltage and the output voltage is shown in Figure 2-14(c).



(a)



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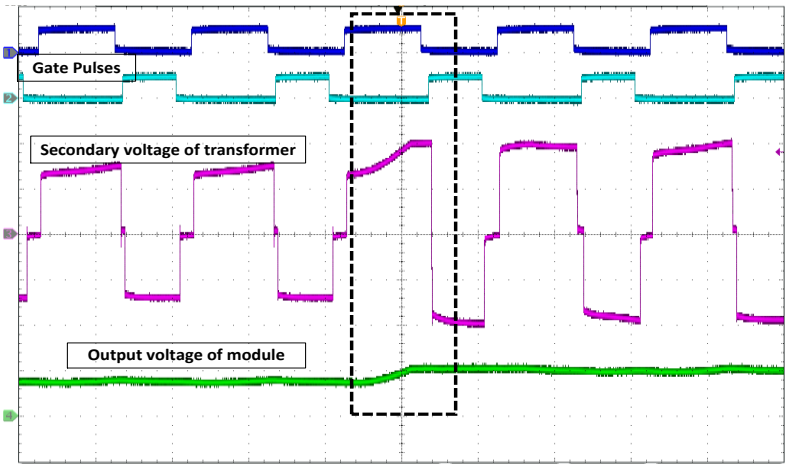


(c)

Figure 2-14. (a) Real-time simulation platform, Typhoon HIL (b) Waveforms of one module in normal operation mode. (i) Gate pulses (1V/div) (ii) Output voltage of module (1000 V/div) (iii) The secondary voltage of the transformer (1000 V/div) (c) Waveforms of one module in faulty operation mode. (i) Gate pulses (1/div) (ii) Secondary voltage of transformer (1000 V/div) (iii) The output voltage of module (2000 V/div)

2.7. Experimental Results

To further prove the capability and feasibility of the proposed SST, a scaled-down prototype hardware setup with 4-modules (divided into 2 clusters) is developed, as shown in Figure 2-15. The details of the experimental setup and results are provided in this section. The specification of the hardware setup is provided in Table 2.1. The details of the major components have been listed in Table 2. 3. The input voltage is 200 V (DC), and the output voltage is regulated at 100 V. An electric load with a maximum power of 800 W is connected to the converter. To consider faulty operation mode, module-4 (M4) in Figure 2-6 was bypassed with a mechanical switch. The output voltage of the converter (V_{out_total}) along with V_M3 and V_M4 (faulty module) is shown in Figure 2-16. As expected, the controller regulates the total output voltage at the reference value. The rise in the amplitude of M3 voltage is visible, which is done to compensate for the zero voltage of M4 when it is bypassed.

Table 2.3 The Experimental Hardware Components

Component	Model
SiC-MOSFET full bridge module	SEMIKRON - SK45MH120TSCp (Engineering Sample)
MF transformer	(Custom design-build at E-Craftsmen©) Input voltage = 150 V, Output Voltage = 150 V, Output Current = 15 A_{pk}, Frequency = 20 kHz
Voltage Sensor	LEM - LV25-p
Controller platform	dSPACE - RTI1202

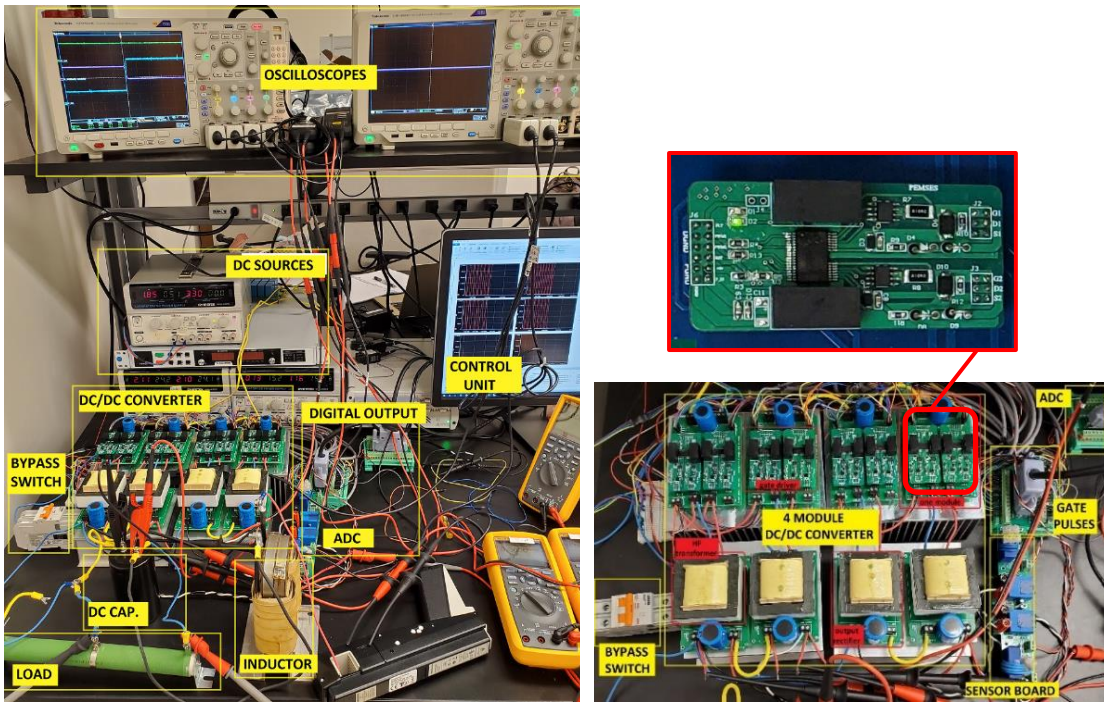


Figure 2-15. The scaled-down laboratory experimental test setup

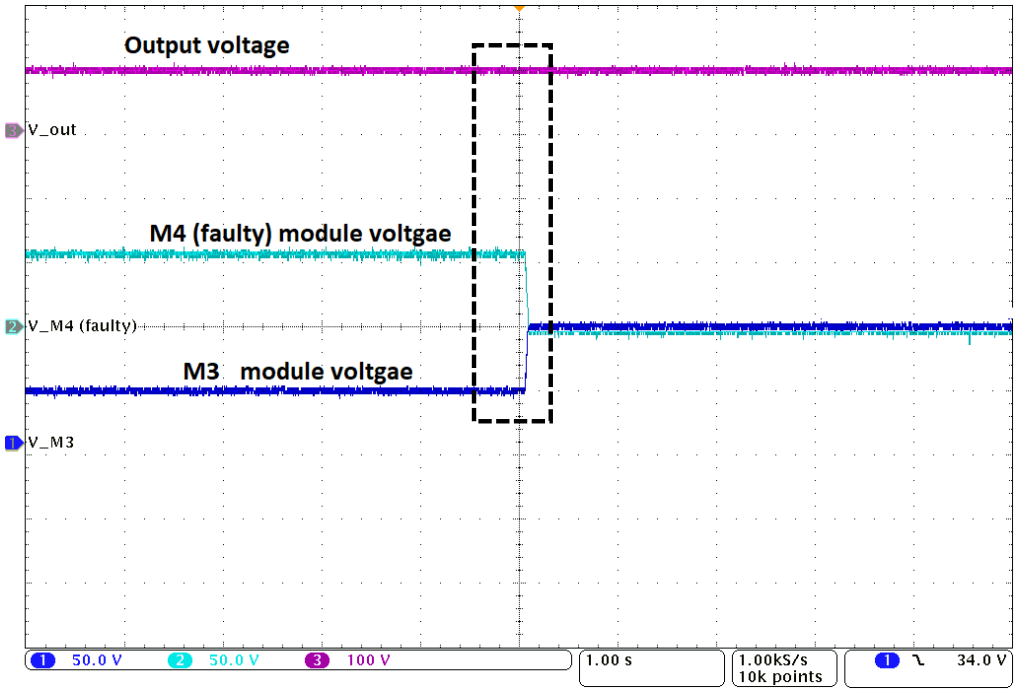


Figure 2-16. (i) The output voltage of converter (ii) M4 output voltage (iii) M3 output voltage, when there is a fault and M4 is bypassed in fault occurrence

The secondary voltage of transformers is shown in Figure 2-17 for hardware setup (similar to Figure 2-12). The voltage rise in power switches, VDS_M3, is captured for S3 in M3 and shown in Figure 2-18. To show the robustness of the control system, one more test with step changes in the load current was carried out; the first step-change is from 2 A to 4 A, followed by increasing the load current to 6 A and back to 2 A.

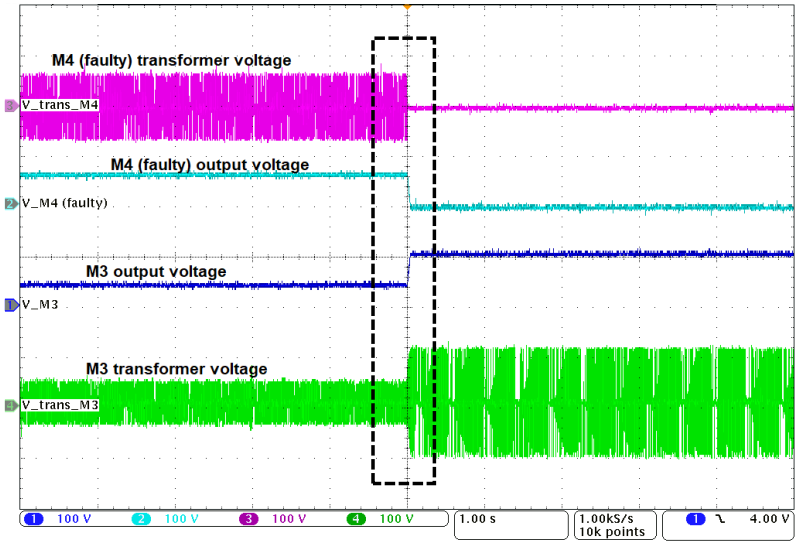


Figure 2-17. (i) M4 Secondary voltage of transformers (ii) M4 output voltage (iii) M3 output voltage (iv) M4 Secondary voltage of transformers, when there is a fault and M4 is bypassed in fault occurrence

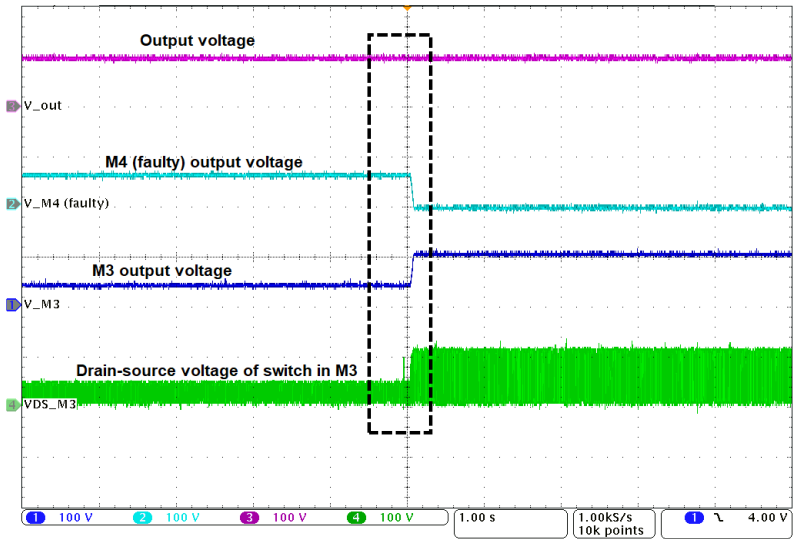


Figure 2-18. (i) The output voltage of converter (ii) M4 output voltage (iii) M3 output voltage (iv) V_{DS} of SiC-MOSFET in M3, when there is a fault and M4 is bypassed in fault occurrence

As can be seen from Figure 2-19, the closed-loop voltage control can handle the step changes, and there are no fluctuations in the voltages. The efficiency of the unoptimized lab-scale hardware prototype was calculated to be 92.3 % using measured output/input currents and voltages of each module separately at a maximum 8 A load current and 100 V DC output voltage. However, the efficiency in a full-scale practical system is expected to be much higher when using optimized SiC-MOSFET-based power converters [77]. In current practical HVAC subsea electrification systems with a similar specification for voltage and power levels provided in the context, the net losses are usually significantly higher than 5 % (or 180 kW). LF transformers, converters (such as adjustable speed drives), etc., generate a lot of heat due to the losses and are currently being addressed effectively.

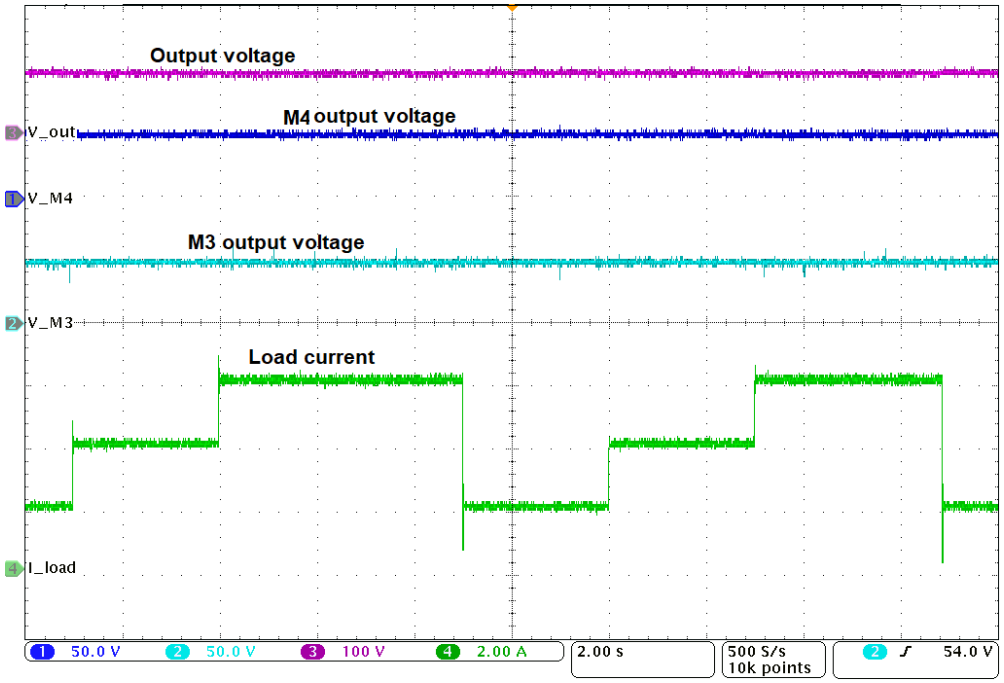


Figure 2-19. (i) The output voltage of converter (ii) M4 output voltage (iii) M3 output voltage (iv) load current, during step changes

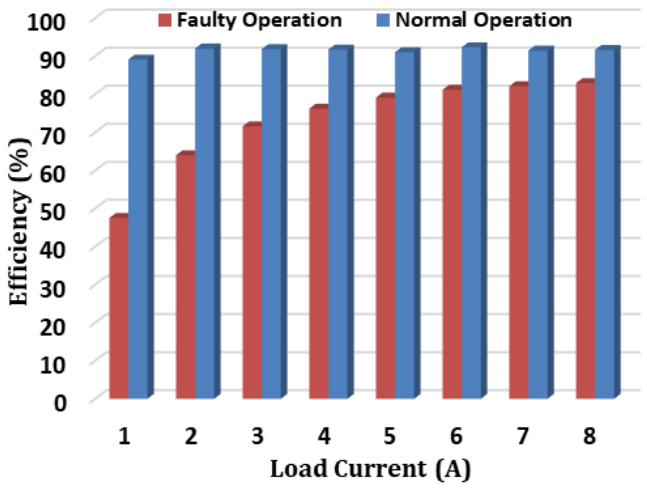


Figure 2-20. The loss chart for normal and faulty operation of hardware setup

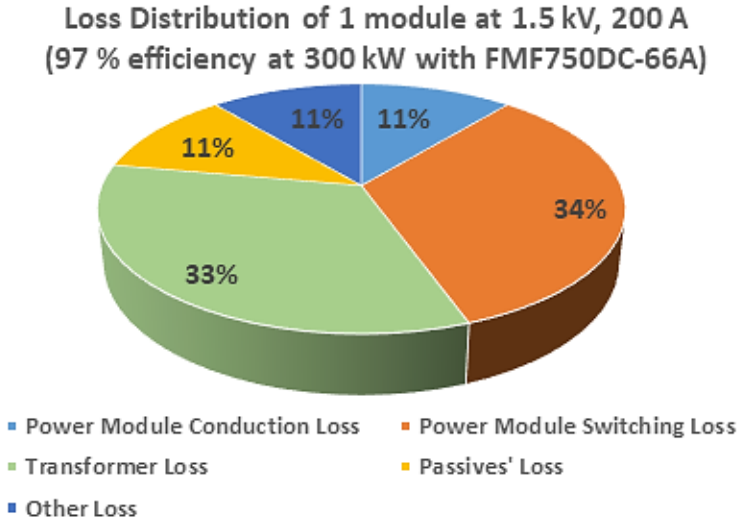


Figure 2-21. The loss analysis for the components of one module

The loss and efficiency analyses for the proposed hardware setup are investigated and summarized in Figure 2-20. It may be surprising to learn that lower-power converters generally have lower efficiencies than higher-power converters, especially considering the higher RI^2 losses that arise at higher output currents. However, almost constant internal power consumption of the switching controllers,

shunt regulators, and optocouplers (the "housekeeping" consumption) plays a significant role. The 92% efficiency in normal operation mode and 82% efficiency in faulty operation mode under 8 Amps load current is achieved, which in comparison to the literature is valuable [47]. The analytical loss calculation for one module is investigated and shown in Figure 2-21. At 300 kW per module, 3 kW converter switching loss, 1 kW conduction loss, 3 kW transformer loss, 1 kW passives' loss, and a rough estimate of 1 kW for other miscellaneous losses are achieved.

2.7.1. MF Transformer Design

The subsea transformer must be designed to withstand the pressure levels imposed by seawater at depths of 3000 m. Also, it should be able to operate well without maintenance for a long duration. As explained earlier, the MF transformer forms one of the most important components of the proposed topology. While replacing an LF transformer with a medium switching frequency SST for a certain application, the design of the transformer must be primarily optimized for size, losses, and cost using an appropriate core material. Different factors influencing these parameters are the core material, operating frequency, magnetic flux density, etc. This section provides the design details of the MF transformer employed in the experimental prototype.

The 3-D finite element analysis (FEA) of the MF transformer was carried out in COMSOL© software, with the design parameters provided in Table 2.4 and Figure 2-22. The transformer design was done by following the procedure introduced in [78], [79], consistent with standard practices. The model incorporates the effect of a nonlinear B-H curve, including saturation in the soft-iron core, to simulate its magnetic behavior.

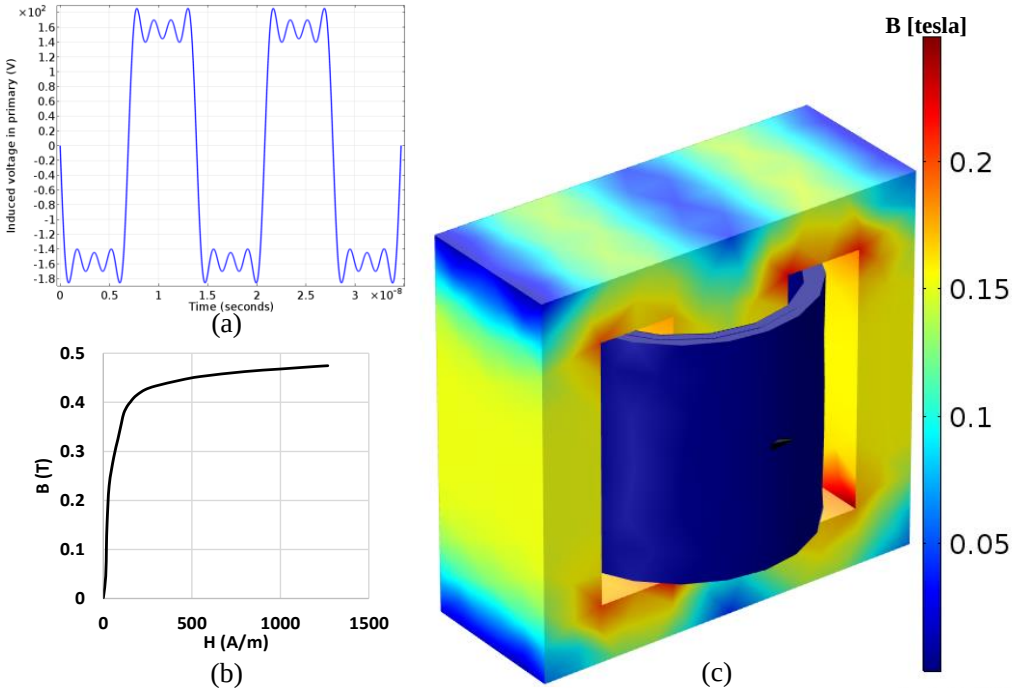


Figure 2-22. (a) Induced square wave primary voltage of the transformer as Taylor's series (b) The B-H curve for N67 (c) The core magnetic flux density distribution showing the peak flux density and leakages in COMSOL©

Table 2.4 Transformer Design Parameters in COMSOL©

Parameter	Value
Core material	Epcos N67
Primary inductance	3.84 mH
Primary / Secondary No. of turns	24/23
Primary/secondary resistance	15.98 mΩ
Core dimension	2.6" W × 2.1" H × 1" D
Transformer dimension	2.6" W × 2.1" H × 1.75" D

The FEA design was done before the transformer manufacturing to confirm the behavior of the designed transformer, especially for the peak flux density. The voltage in the primary winding of the transformer (shown in Figure 2-22(a)) was simulated with up to the 7th harmonic content for testing the effects of a near-square wave. The B-H curve for the N67 ferrite core is shown in Figure 2-22(b). The magnetic flux density for the MF transformer with 200 V amplitude, 15 A peak current, and 20 kHz frequency is shown in Figure 2-22(c). Compared to the 60 Hz transformer analyzed in [79], the MF transformer is less than 10 % of the volume, and the corresponding SST will result in the overall size reduction of up to 70 %, which will make it easier to install and maintain in a subsea setting. While the extent of reduction in volume or weight that can be achieved on a full-scale practical system may vary from the lab-scale experimental prototype (due to the differences in the impacts of partial discharge, *dv/dt* in the windings, cooling system, etc.), the assessment of the proposed MF transformer-based method versus an LF transformer approach provides a comparative insight for potential researchers.

The transformer design was done by following the below procedure, consistent with standard practices [36] and [37]:

1. Select an operating frequency for the transformer depending on the application and specifications (here is 10 kHz ~ 20 kHz)

2. Based on the power curves available for different cores, ferrite core is chosen. For a ferrite core B-H curve (as shown in Figure 2-22(b)), the saturating magnetic flux

density value and losses are much lower than silicon steel or amorphous core materials, so that they can be used for high operating frequencies in the range of kilohertz.

3. Once the core is decided, using the voltage, current, and peak flux density specifications, equation $V_{pri} = 4.44 \cdot f \cdot N_{pri} \cdot B_m \cdot A$ is used to determine the minimum '$A \times N$' value.

4. After that, a minimum value of magnetizing inductance, L is calculated for the selected frequency so that the magnetizing current, I_m (this is approximately "$I_{pri} - I_{sec}$" for a 1:1 transformer) is small with respect to (w.r.to) the transformer current rating. As per the usual design, from pure simulation model gave a similar value of less than 3 % leakage inductance

5. With the expected L value, choose a 'N_{pri}' value (here is 24). Then this value is used in $H_{net} = \frac{\text{Npri} \cdot \text{Ipri} - \text{Nsec} \cdot \text{Isec}}{\text{l}} = \frac{N \cdot Im}{l}$ to arrive at a minimum length of the core. A transformer window space factor of 25 % is assumed due to the 20 kHz frequency.

6. With the arrived dimensions, the total power loss, hence the efficiency of the transformer can be calculated. If it is either lower or higher than expected, the design steps are repeated with different values for the number of turns, magnetizing current, etc. until the final specification is met.

It should be mentioned that the design procedure used for the lab-scale prototype was the same as the 300 kW transformer. The transformer losses were estimated from both the FEA simulation as well as the hardware (by finding the difference between the average values of instantaneous $V \times I$ product on the primary and secondary sides). The maximum measured transformer loss during the experiment was 11 W, and the

corresponding temperature rise was around 45 degrees Celsius [80], without forced-air cooling. The requirement about the leakage inductance was that it must be less than 0.03 per unit (p.u.) per winding, calculated w.r.to the per unit impedance of the transformer at the designed medium frequency. It was used in the small-signal modeling and also later verified to be within the requirement. It may be noted that the same per unit impedance was chosen for the high-power system and the low power prototype to keep consistency in the analysis. While the transformer design is an important part, the primary focus of this research is about proposing fault-tolerant isolated DC/DC converter for subsea applications and on small-signal modeling/analysis of the proposed converter.

CHAPTER 3.

POWER CYCLE TEST BENCH FOR ACCELERATED LIFE TESTING OF SIC-MOSFETS TO ASSESS RELIABILITY

3.1. Power and Thermal Cycling in High-temperature Environment

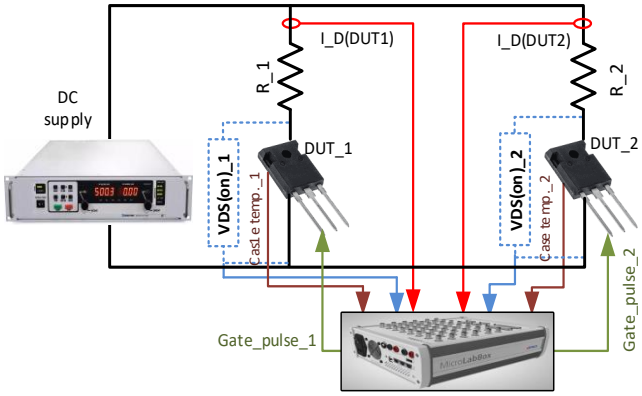
This chapter introduces a power cycling (PC) and thermal cycling (TC) test bench to perform accelerated life testing for reliability assessment of SiC-MOSFET in a harsh, high-temperature offshore environment. A degradation setup along with health monitoring of IGBTs in automotive power converter systems is well described in [81], which is modified for the SiC-MOSFET degradation procedure introduced in this research. The captured data from the Device-Under-Test (DUT) in different ambient temperatures are envisioned and provide critical information about the failure mechanisms and lifetime characteristics of power devices. The provided lifetime characteristics data of SiC-MOSFET will be used to statistically estimate the Remaining-Useful-Lifetime (RUL) of a component in a real application.

As mentioned earlier, SiC-MOSFETs are the most common component to fail due to stresses caused by the dissimilar coefficients of thermal expansion of the materials. During their lifetime, the device tolerates many temperature cycles, which causes damage until the device fails. The amount of damage each temperature cycle causes is influenced by the magnitude of the change in temperature and the rate at which the change occurs. Therefore, to accelerate the failure of the SiC devices, the large

temperature swing (ΔT) in a concise period in which temperature change occurs must be applied. A lifetime degradation test setup is designed and shown in

Figure 3-1. The proposed methodology's schematic provides a new, low-cost method of actively controlling the temperature of the SiC-MOSFETs power modules using thermoelectric coolers; see

Figure 3-1(a).



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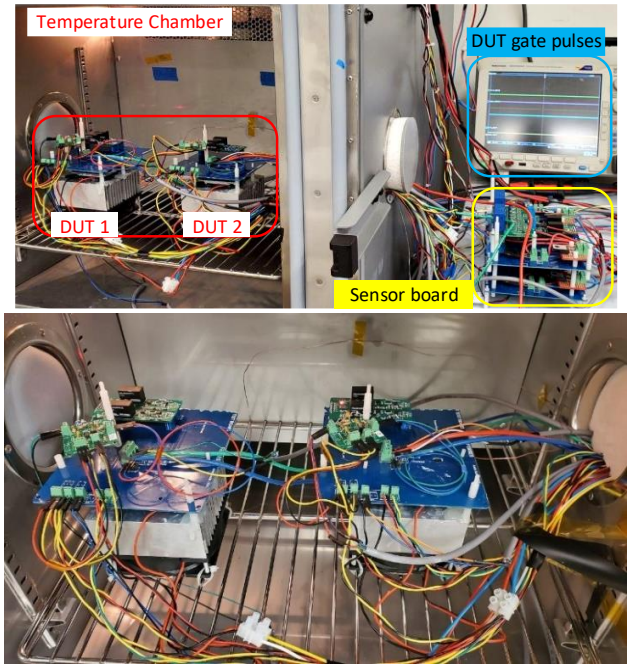
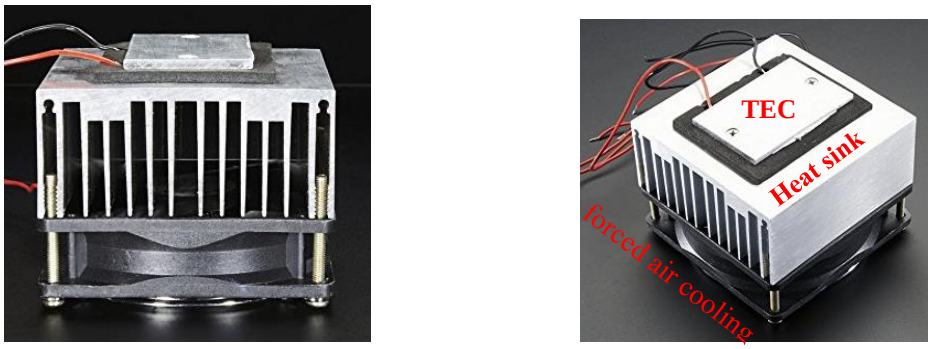


(b)

Figure 3-1. The test setup for SiC-MOSFET accelerated lifetime degradation (a) Schematic (b) Experimental hardware

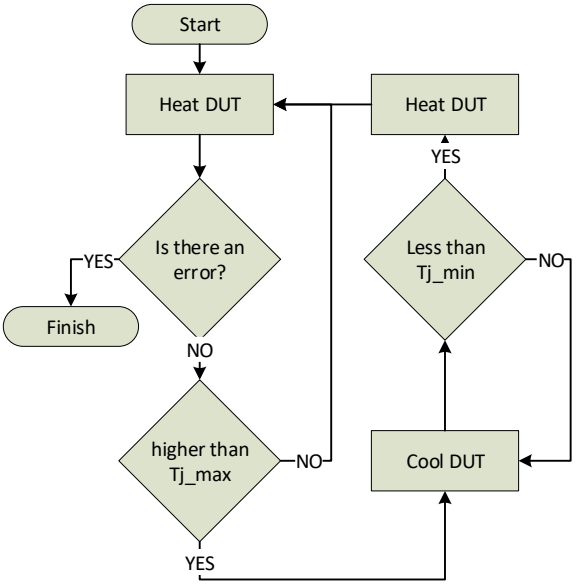
The SiC-MOSFET's temperature can be swept by controlling its case temperature fixed to a heat sink. This cycling is known as thermal cycling (TC). Therefore, if the temperature of the heat sink is reduced to a value that is lower than the DUT temperature, heat will flow out of the DUT into the heat sink. In the reverse operation, heat will flow to the DUT from the heat sink if the heat sink temperature is higher than that of the DUT temperature. Proportion to the temperature difference and conductivity of the heat path between the heat sink and the DUT, the rate at which the heat will flow out can be determined. To make a large temperature change in short period of time, a thermoelectric cooler (TEC) is attached to the DUT, and the other side has to be held at a constant temperature. This is achieved by using a large aluminum heat sink, which is held at a constant temperature by forced air cooling, see Figure 3-2. The thermoelectric cooler can then maintain a temperature either below or above the heat sink temperature. The thermal mass of TEC is very much smaller than that of the heat sink. Thus, the temperature of the cooler can be controlled accurately with a very rapid response time.



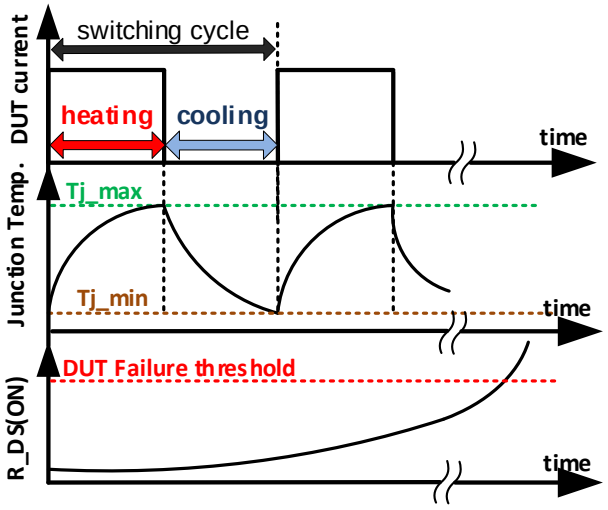
(a) (b)

Figure 3-2. The Adafruit 1335 Peltier Thermoelectric Cooler (TEC) Module with Heat Sink Assembly, 12 Volts, 5 Amps (a) side view (b) top view

The degradation cycle consists of two states, heating and cooling. The flowchart and the schematic of the DUT accelerated lifetime procedure are shown in Figure 3-3(a) and (b), respectively. In the heating state, the DUT is switched ON, and current flows through the DUT, causing its temperature to rise due to conduction losses. Simultaneously, the control system switches the current in the thermoelectric cooler (TEC), causing heat to flow into the DUT from the heatsink and blocking the device's heat flow. This results in a very fast junction temperature rise in the DUT. In the cooling state, the DUT is switched OFF, and the current stops flowing. At the same time, the current in the thermoelectric cooler is switched reverse so that heat flows out of the DUT into the heat sink. Using a TEC in this way greatly increases the cooling speed of the DUT. During each cycle, DUT junction temperature is monitored, and the controller moves from cooling state to heating state when junction temperature reaches its minimum threshold and returns to cooling state when the DUT maximum junction temperature is reached. These maximum and minimum junction temperature thresholds are set in the control system and can be modified for each test or even during a test to alter the DUT operating range. As shown in Figure 3-3(b), the switching cycle will continue until R_{DS_ON} passes its failure threshold.



(a)



(b)

Figure 3-3. (a) The flowchart of DUT accelerated degradation test (b) The schematic of degradation cycle

To measure the lifetime parameters of SiC-MOSFET under controlled operating conditions, a control system is designed in MATLAB/Simulink, see Figure 3-4, and programmed in dSPACE-RTI1202 to control the power and heat flowing in and out of the DUT along with data acquisition for post-processing purposes.

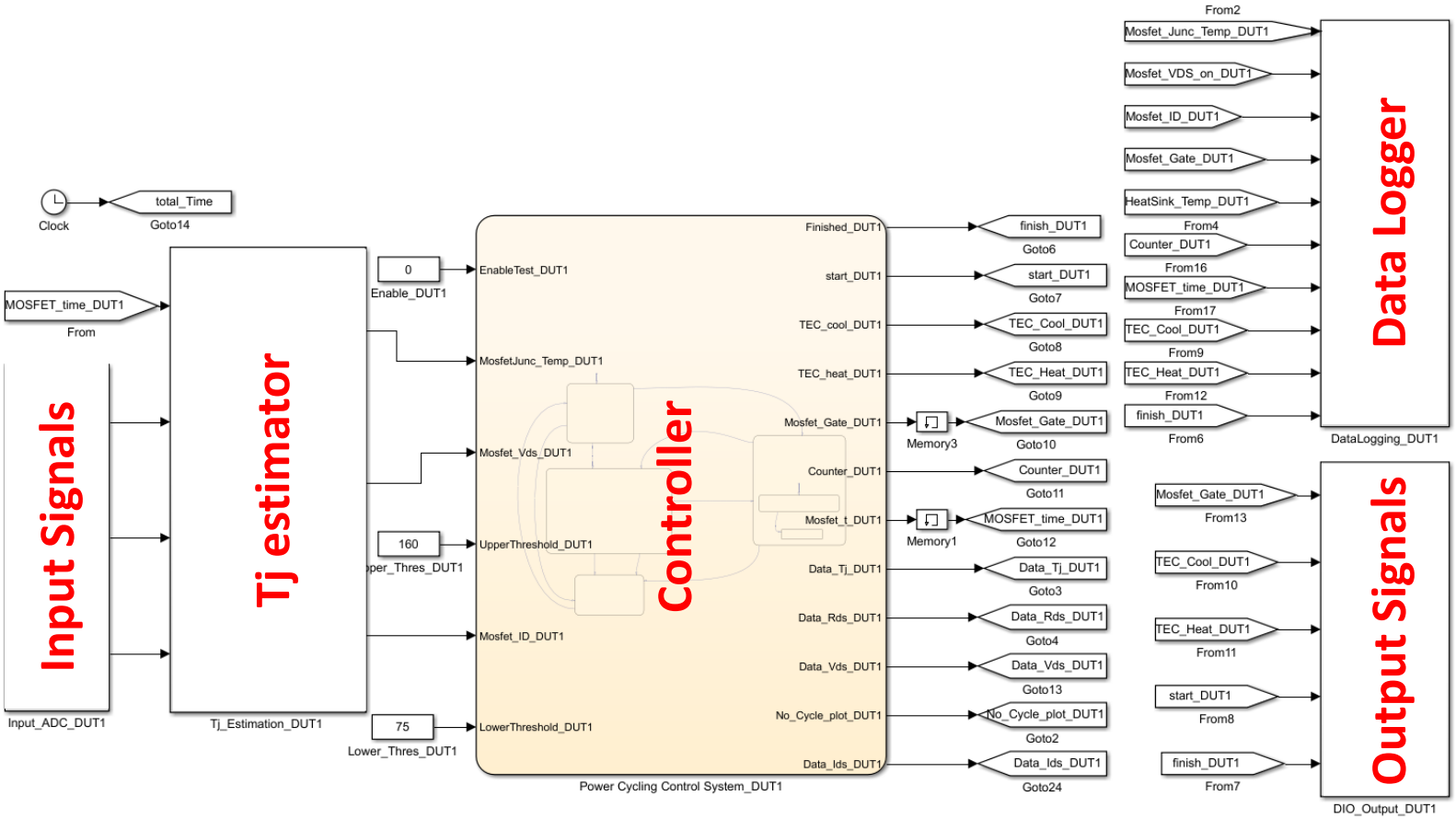


Figure 3-4. The accelerated lifetime experiment control system in MATLAB/Simulink

The control software unit is split into three sections: *inputs*, *outputs* & *data logging*, and *control system*. The input subsystem contains the control blocks to scale and offset the data for the various measurements like the voltage, current, and temperature. A second-order filter is used to reduce the noise of measurement for sensors.

The main control loop of the software is written in Stateflow and located in the *control system* subsystem in Figure 3-4. The Stateflow is a state or event-based program that takes input from Simulink and provides outputs to Simulink; see the Stateflow diagram in Figure 3-5. The first state in which the control software enters is labeled start. The experiment will remain in this state until the Enable variable is TRUE. When the experiment is initiated, the control system enters to heating state and will remain in this state as long as two conditions are satisfied; First, the junction temperature of DUT is less than the upper threshold, and second, $V_{DS(on)}$ value is less than failure threshold, and the number of heating cycles is not more than 1000. If the first condition comes to action, the control system will enter the Cooling state, and if the second conditions pass, the system will enter to Finish state, and the experiment will stop working. In the Cooling state, the device will cool down to its minimum threshold value where the cooling state condition is. After that, the control system will enter the heating mode until the device fails. The detailed mode of operation for the degradation cycle is described here.

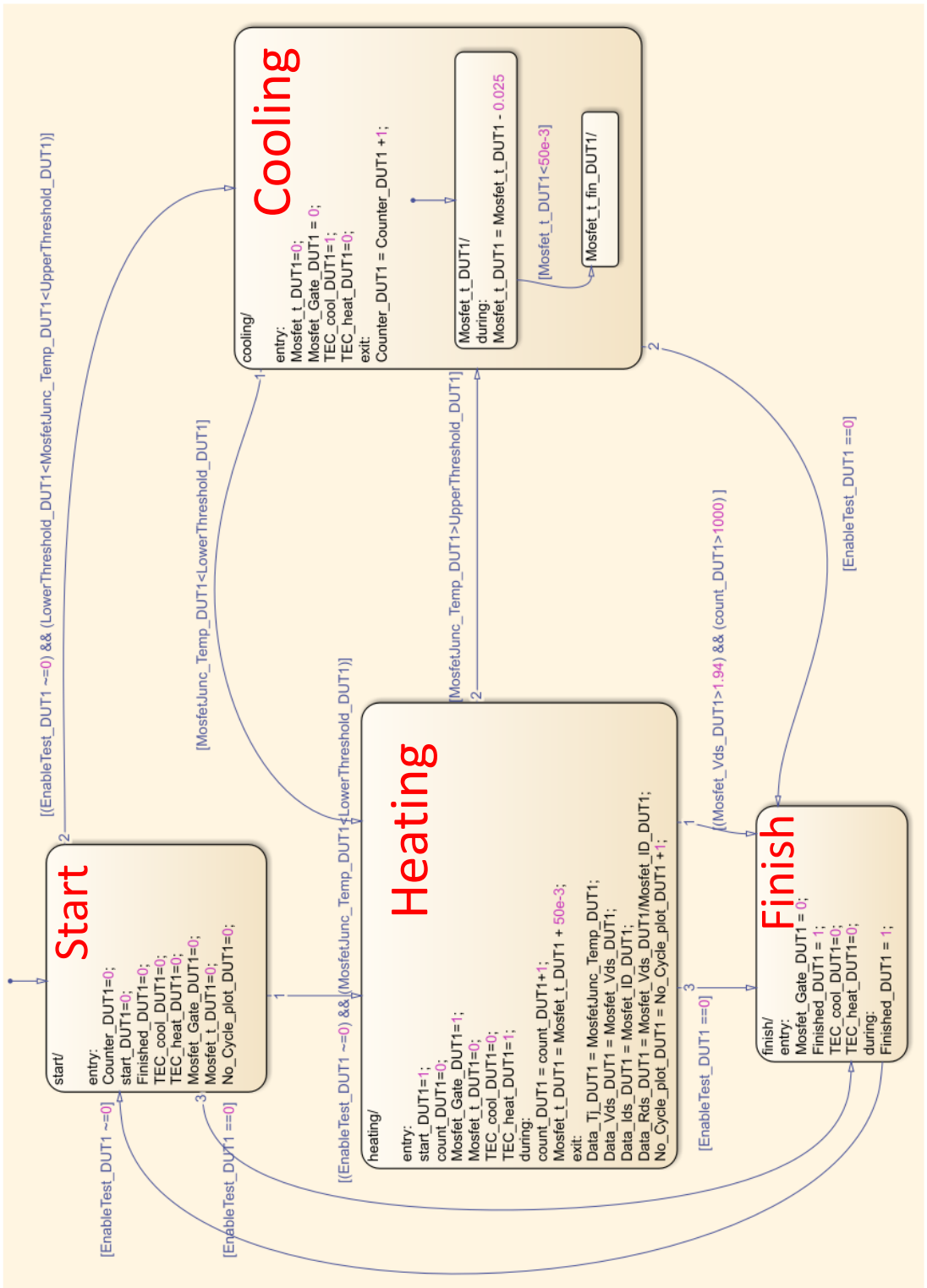


Figure 3-5. The Stateflow diagram of the main control system

The output subsystem uses different blocks to convert the output gate pulses of DUTs and relays to the values that drive the device appropriately. Using the digital outputs of dSPACE, the gate signals are sent to the gate driver of SiC-MOSFETs, which is attached on top of the degradation PCB, see Figure 3-6.

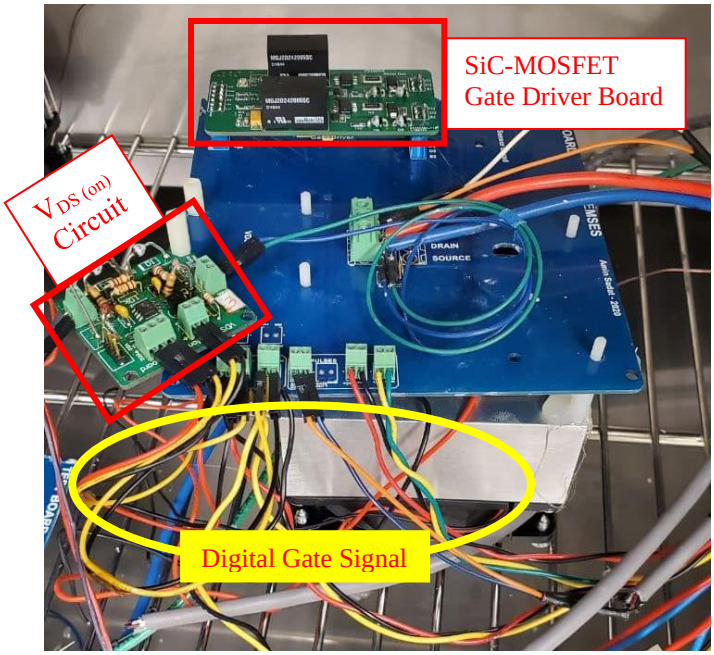
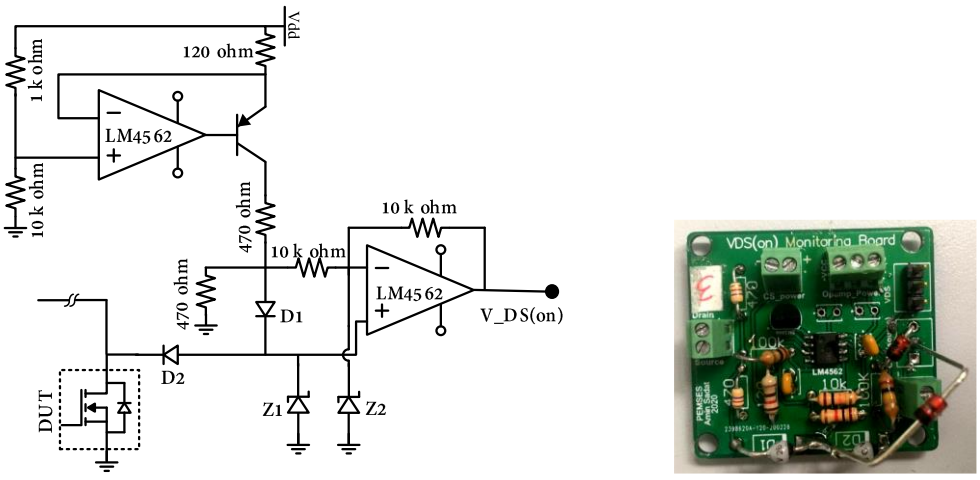


Figure 3-6. The experimental hardware including gate driver, $V_{DS\ (on)}$, and digital gate pulses from the control unit

SCT2450KEC SiC-MOSFET is chosen as the power DUT, but the method itself can be applied for other types of power devices. For power switches, the junction temperature and $R_{DS(ON)}$ of DUT are usually the temperature-sensitive-electrical parameters (TSEP) or health indicators to represent the device's degradation.

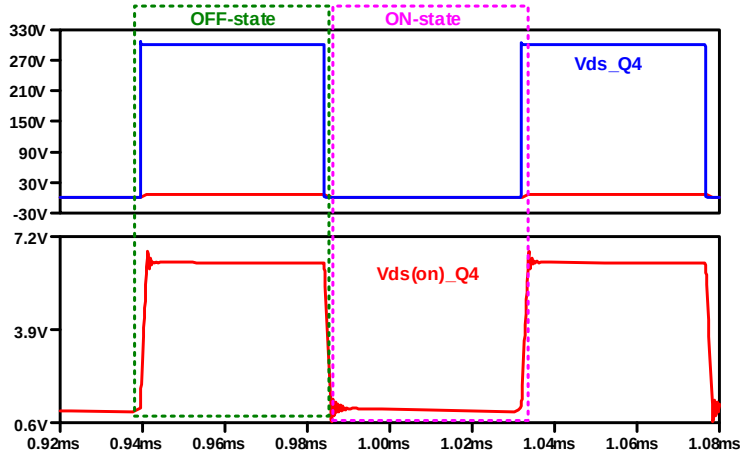
To estimate $R_{DS(ON)}$ during the degradation test, the $V_{DS(ON)}$ is monitored and captured using an improved measurement circuit. A V_{CE} measurement circuit for IGBT

devices is presented in [82], which cannot be used for SiC devices practically due to faster switching speeds. The diode D_2 (see Figure 3-7(a)) should turn off faster than DUT to protect op-amp from overvoltage during DUT off-time operation. The turn-off time for SiC-MOSFETs and Schottky diodes is in the range of nanoseconds, which means both will turn off at the same time. Therefore, for SiC-MOSFET $R_{DS(ON)}$ estimation, over-voltage protection via two Zener diodes with inverting and non-inverting pins of the op-amp are added to clamp pin voltages at constant levels (~7 V). The experimental prototype of the modified circuit is shown in Figure 3-7(b). The proposed algorithm, which will be described in the chapter, is based on calculating the RUL for each component with captured data during the degradation process. The simulation results of the proposed circuit and device drain-source voltage are shown in Figure 3-8 to prove the capability of voltage tracking of DUT during on-time operation. A 10 kHz pulse is applied to the device, and its drain-source voltage is monitored and measure for post-processing in the degradation algorithm.

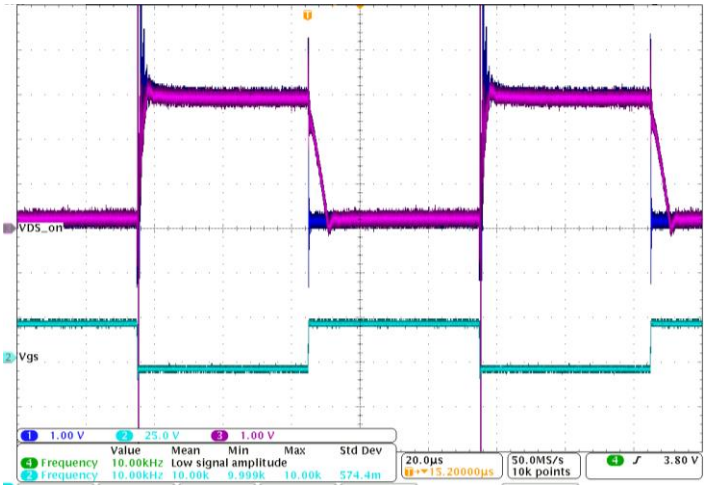


(a) (b)

Figure 3-7. The $V_{DS(ON)}$ measurement circuit (a) schematic (b) prototype



(a)



(b)

Figure 3-8. (a) The simulation results of (i) Drain-source voltage of DUT (blue) and $V_{DS(ON)}$ circuit (red) (ii) The $V_{DS(ON)}$ circuit voltage tracking (zoom-in view)
(b) The experimental results of (i) on-state drain-source voltage (blue) and $V_{DS(ON)}$ (pink) (ii) gate pulse

Since the DUTs are regular 3-pin power devices, a temperature sensor for junction temperature measurement is not included in the packaging. Therefore, in the experiment control system, DUT's junction temperature is estimated precisely with knowing the power losses in the device, time, and heatsink temperature (case

temperature). The modified junction temperature estimation using equation (3.1) [83] is used considering both switching and conduction losses of DUT.

$$T_J = (P_s + P_c) * \sqrt{\frac{4t}{\pi R_\Theta C_s}} + T_a \quad (3.1)$$

where, T_J is the junction temperature and rise due to switching and conduction losses of the device, P_s and P_c respectively, R_Θ is thermal resistance, C_s is heat capacity, t is the time period which the device is ON and T_a is ambient temperature or the heat sink temperature on which the device is fixed.

To measure the power dissipated due to switching losses, a double-pulse-test (DPT) is carried out on the device based on operating voltage and current levels. The experimental test setup and the result of DPT are shown in Figure 3-9. The experimental results of the device degradation cycle are shown in Figure 3-10.

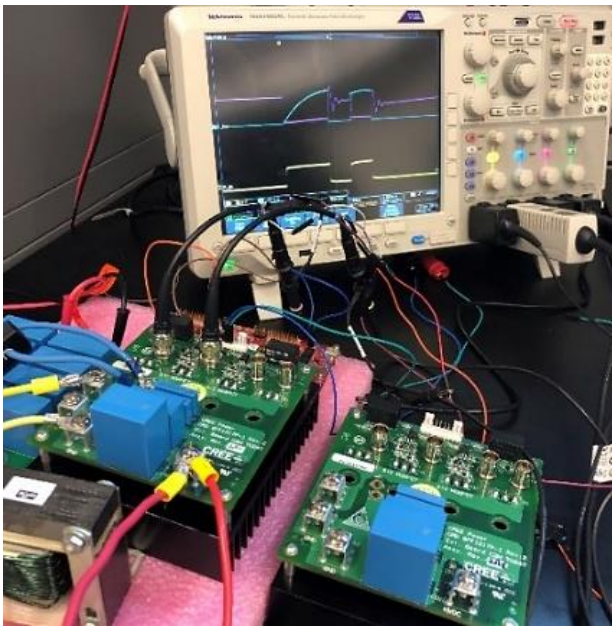


Figure 3-9. The Double-Pulse-Test setup

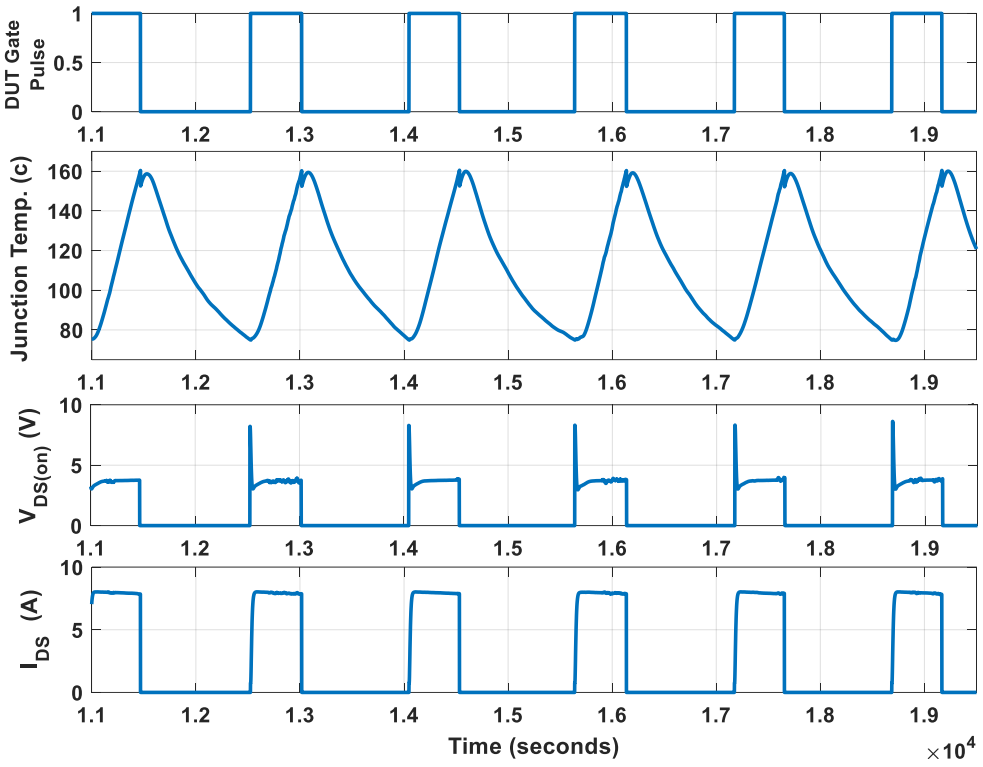
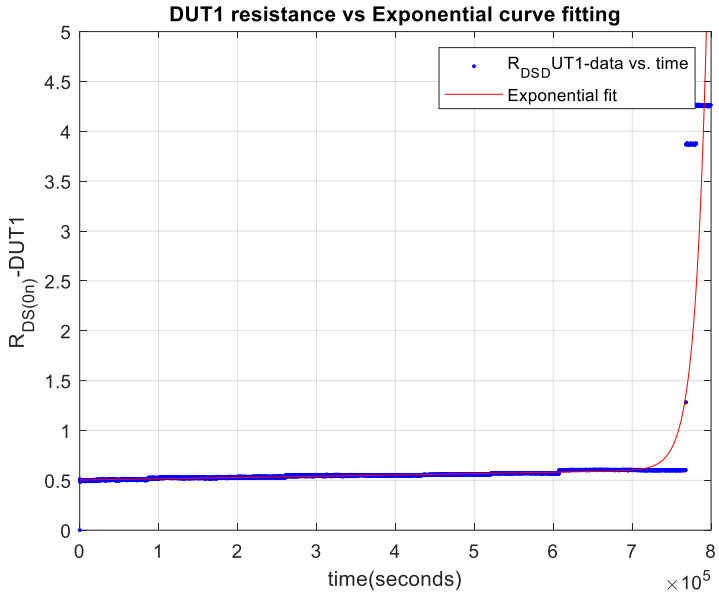


Figure 3-10. The experimental data at 75 °C ambient temperature for (i) DUT gate pulse (ii) DUT junction temperature (iii) $V_{DS(ON)}$ (iv) Drain-source current

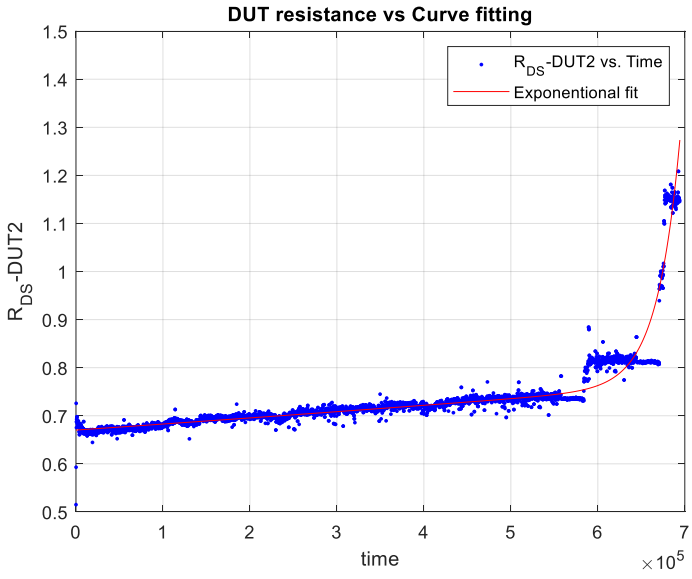
As described degradation procedure earlier, during the on-state operation, 8 A current will pass through the DUT, and drain-source voltage is recorded to calculate on-state resistance. The junction temperature starts from 75 °C and increases to 160 °C. Although the maximum junction temperature for the selected DUT is 175 °C, the upper threshold is kept at 160 °C for safety purposes and ignoring any unexpected failure caused by extra heating inside the device.

The accumulated estimated $R_{DS(ON)}$ for both two DUTs are shown in Figure 3-11. The initial value for $R_{DS(ON)}$ is almost 500 mΩ and 680 mΩ for both DUT1 and DUT2, respectively. Considering a 20 % increment in $R_{DS(ON)}$ as a failure threshold, both DUTs reach 720 mΩ and 830 mΩ at the end of the degradation test. For further component-

level reliability calculation, the degradation data of $R_{DS(ON)}$ is fitted to an exponential equation ($R_{DS\_ON} = a * e^{bt}$) to model the component behavior during the operational lifetime.

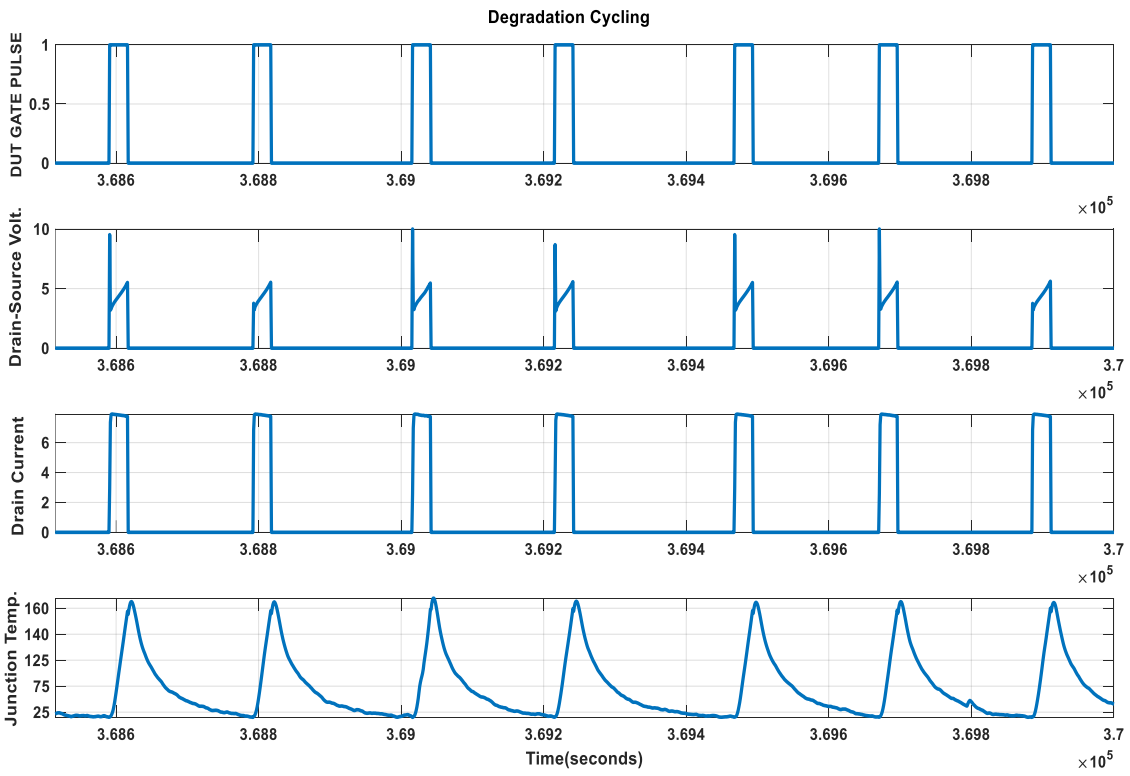


(a)

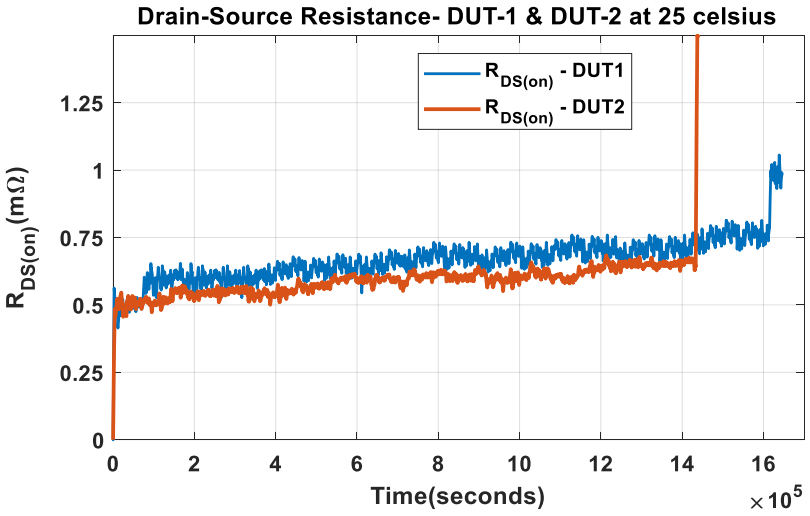


(b)

Figure 3-11. The accumulated estimated $R_{DS(ON)}$ at ambient temperature 75 °C (a) DUT1 (b) DUT2



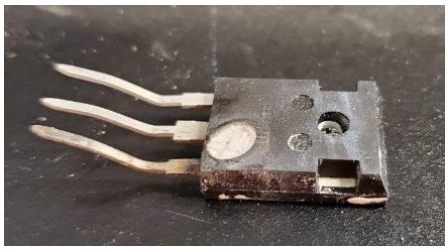
(a)



(b)

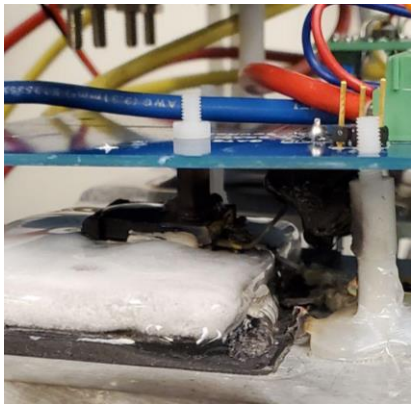
Figure 3-12. The experimental results of (a) degradation cycle (b) $R_{DS(ON)}$ variation for DUT1 and DUT2 at 25 °C ambient temperature

It can be inferred from Figure 3-11 and Figure 3-12 that the lifetime of DUT at 75 °C is almost half of that at 25 °C, which can be considered one of the main effects of the common failure of SiC-MOSFETs in high-temperature operating. The physical damage of DUTs due to accelerated degradation tests at 25 °C and 75 °C ambient temperature are shown in Figure 3-13(a) and Figure 3-13(b), respectively. Figure 3-13(c) indicates that the DUT is burnt after completing the accelerated lifetime test and damaged the hardware setup. The thermal IR camera snapshot of DUT during degradation cycling is shown in Figure 3-13(d). The ambient temperature is 75 °C, and the hottest spot, 150 °C, is the DUT's case temperature.

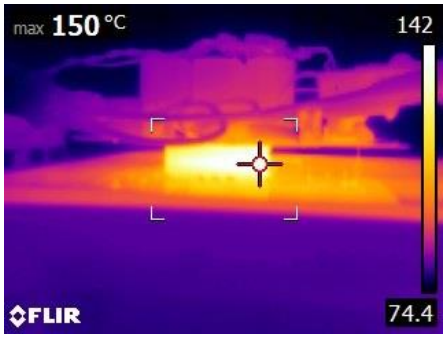


(a)

(b)



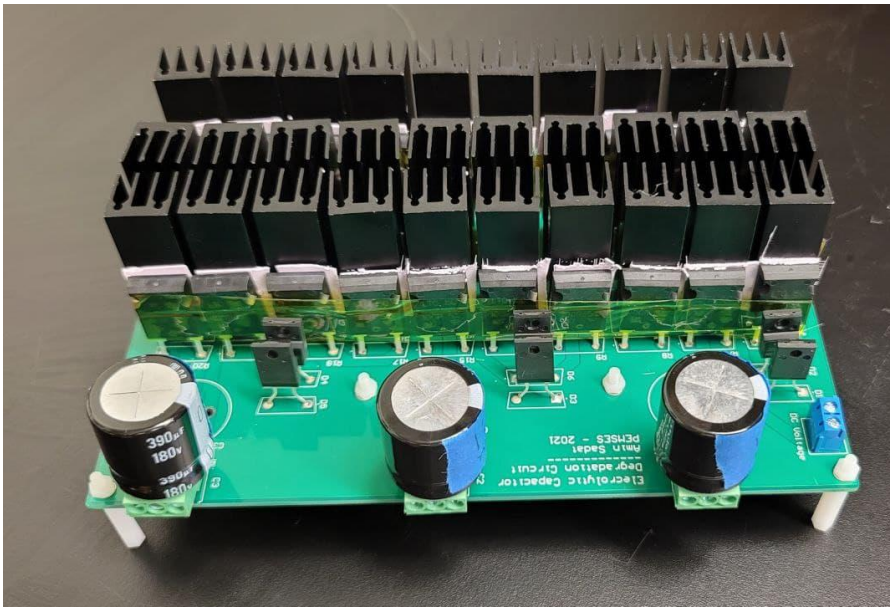
(c)



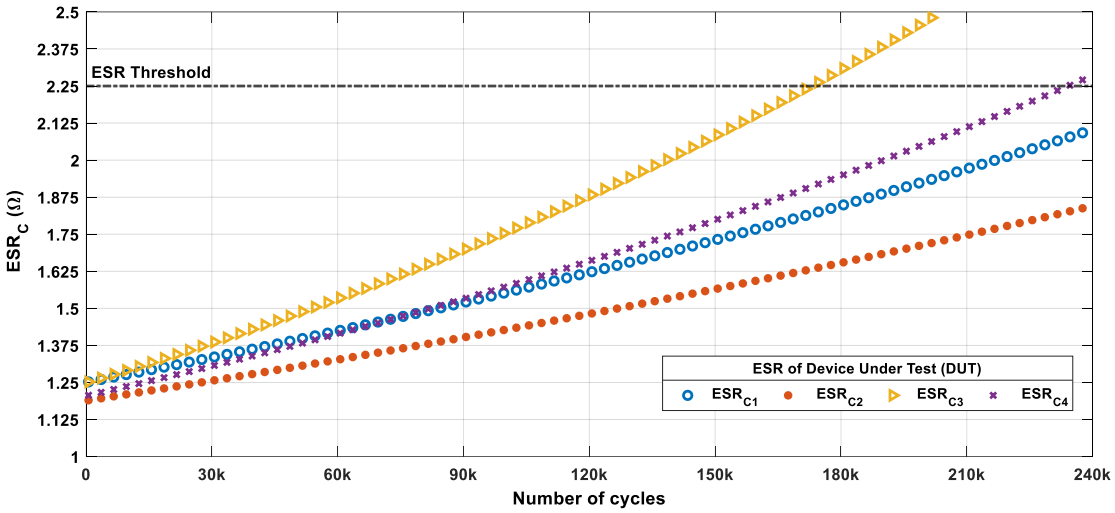
(d)

Figure 3-13.(a) DUT after completing degradation cycle at 25 °C ambient temperature (b) DUT after completing degradation cycle at 75 °C ambient temperature (c) The damage on hardware setup due to DUT failure at 75 °C ambient temperature (d) Thermal IR camera snapshot of DUT during degradation cycling at 75 °C ambient temperature

Capacitors, especially aluminum electrolytic (AECs), are some of the most age-affected components in power electronic converters. Since AECs are the primary cause for power electronics equipment breakdown, therefore their reliability is of major concern. Throughout the life of AECs, the equivalent series resistance (ESR) increases due to the loss of the electrolyte. Industry-defined standards specify the end-of-life threshold for an electrolytic capacitor as a 10 % decrement in capacitance and 250 % or more increment in the ESR_C value from its initial rated value [84]. The experimental and real-time techniques to determine the reactance and *ESR* intrinsic values of aluminum electrolytic capacitors are provided in [85]–[87]. An accelerated hardware setup is designed and implemented for AEC degradation, as shown in Figure 3-14(a). The degradation dataset based on charging and discharging of AEC with maximum rated voltage under 75 °C ambient temperature. The plot can be compared to the manufacturer's information, which mentions 3000 hours of operation at 105 °C temperature, with rated DC voltage and ripple current – for an effective ESR of 200 % of initial value. This means that every 10 hours of life during the performed degradation method at 75 °C temperature is equivalent to approximately 200 hours of life with the manufacturer's life test method at 105 °C temperature. Similarly, the life-time characteristics of capacitor can be extracted at different temperatures to get the appropriate distribution, considering that every 10 °C lower temperature will nearly double the life of the AECs, as suggested by the Arrhenius equation.



(a)



(b)

Figure 3-14. (a) The hardware setup for Aluminium Electrolytic Capacitors (AEC) degradation (b) Degradation dataset for AEC

3.2. Power FET Degradation based on Thermal Equilibrium during Mission-Profile Characterization

In order to precisely estimate problematic thermal behaviors in power devices, the thermal impedance derived from the datasheet or finite-element method (FEM) simulation alone may not be sufficient. It is important to consider power converters' practical operation, including ambient temperature variation, heat sinks, thermal dynamics of different components, and accurate thermal characterization [88], [89]. Hence, mapping the converter's mission profile into specific loading profiles of power electronic components is getting more important since it can simulate the practical behavior of power converters and components in real-time operation. Considering both the operational and environmental thermal stresses on bond wires in Silicon Carbide (SiC) MOSFET power modules, a mission-profile-based reliability analysis approach is proposed in [90]. A long-term mission profile-based reliability prediction method for modular multilevel converters considering analytical power loss models, system-level, and component-level thermal modeling is introduced in [91]. In [92], a long-term mission profile is used to estimate a converter-level reliability metric. A fast mission-profile-based simulation strategy for a SiC power module in a photovoltaic inverter topology is described in [93]. This approach relies on a fast condition-mapping simulation structure and the detailed electro-thermal modeling of the module topology and devices. Knowing the precise thermal dynamics of the power device is a fundamental step to understand the degradation of the DUT and predict the reliability or Remaining-Useful-Lifetime (RUL) of devices. In [89] and [94], an approach to

extract thermal characteristics of (insulated gate bipolar transistors) IGBT operation, under the switching mode, by using an H-bridge testing circuit is proposed.

This subsection presents a precise power FET degradation method based on thermal equilibrium characteristics during mission-profile qualification. The proposed technique is tested in an H-bridge-based setup to capture the junction temperature changes for analyzing power devices' thermal behavior during operational life. The mission profile is based on current levels variation and then applied to the H-bridge degradation test setup.

The proposed thermal model of the H-bridge-based degradation setup using four SiC-MOSFET is shown in Figure 3-15. All the four SiC-MOSFET DUTs (numbered from Q1 to Q4) and their antiparallel diodes are identical with the same part number. The inductive load is large enough to maintain load current with minimum ripple and assume as constant current. The gate pulses for switches in the same leg, Q1/Q2, and Q3/Q4, are complimentary with a 10 kHz switching frequency, but it can be increased to the actual operating frequency of the power device. There is a specific phase shift between gate pulses of Q1/Q3 to generate desired voltage and current levels on the inductor (See Figure 3-16). Using this topology, when two upper/lower switches are ON, the freewheeling load current will pass through the DUT. During the operation of Q1/Q4 and Q2/Q4, the diagonal device will conduct the same level of current and will have similar thermal behavior during the degradation process. Therefore, it is possible to degrade four devices at the same time, which saves energy and time. As shown in Figure 3-16, the current of Q4 is the same as the inductor current when Q1/Q4 are

conducting and will be used for device thermal characterization. A closed-loop current controller keeps the current at the desired value, but since there is no soft-switching technique applied to the DUTs, the maximum switching losses will be generated at the present current level.

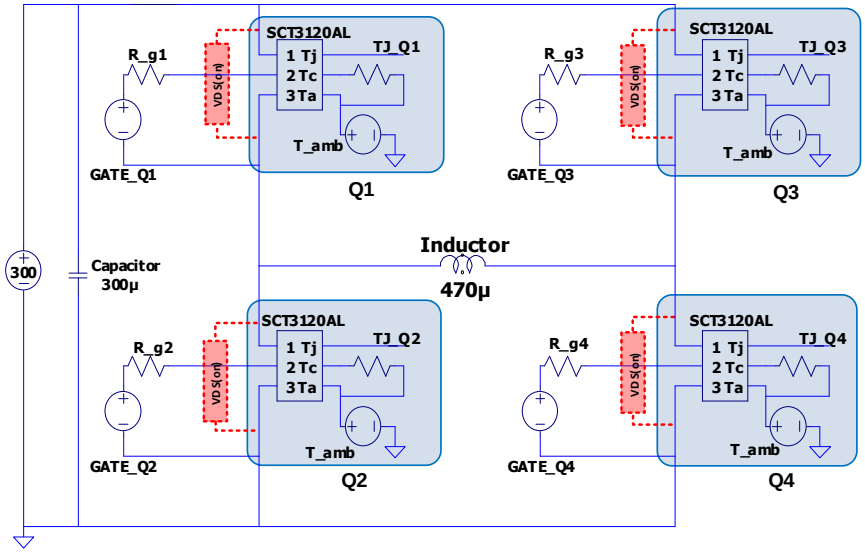


Figure 3-15. The H-bridge degradation test setup in LTspice

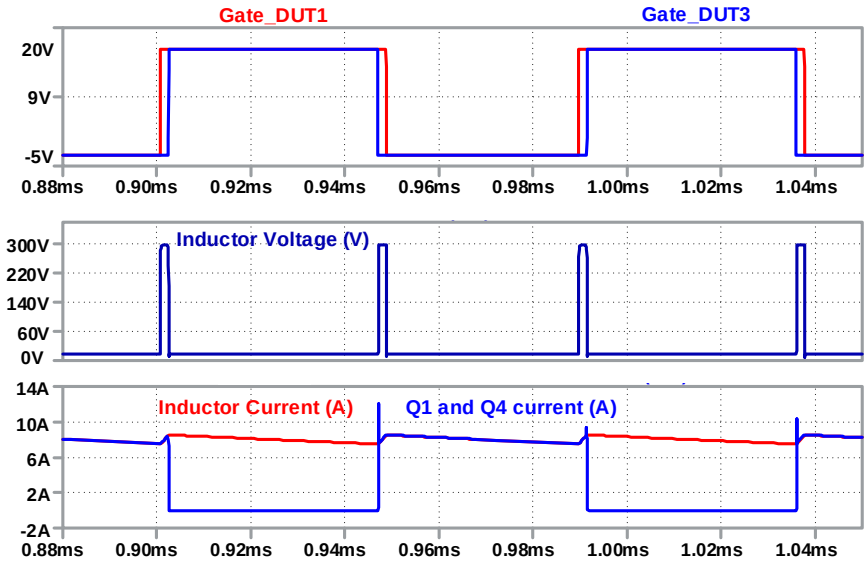


Figure 3-16.The gate pulses for Q1 and Q3 (ii) Inductor voltage (iii) Inductor current (red color) and Q1&Q4 current (blue color)

The proposed mission-profile-based degradation procedure utilizes three current steps in each cycle, 8 A, followed by 12 A, and then 16 A. As shown in Figure 3-17, during the device ON-state and due to conduction and switching losses, the device will heat up, and junction temperature will increase. When the switch is OFF, the junction temperature will drop, followed by another increment during the next ON-state operation. Having an almost constant current will help to degrade the power device with minimal usage of power.

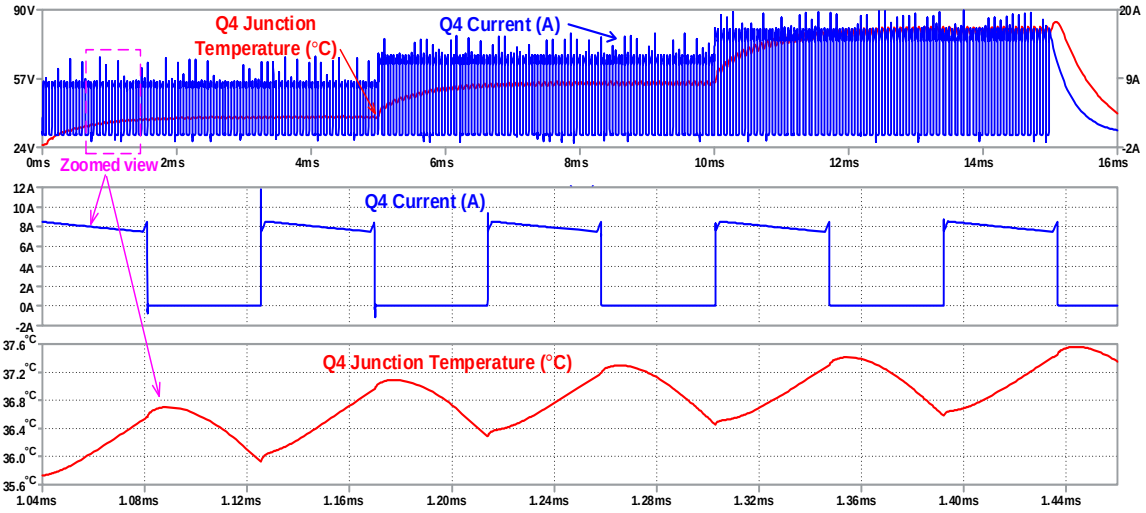


Figure 3-17. The current and junction temperature variations of Q4

For each step of heating mode, junction temperature will reach its equilibrium value and remain constant until the next stage of the current level applies to the DUT. Figure 3-18 and Figure 3-19 show the heating and cooling mode of the degradation test with two different ambient temperatures of 25 °C and 75 °C. In Figure 3-18, since each device pair is experiencing two different currents, Q1/Q4 and Q2/Q3 reach equilibrium at nearly 85 °C and 65 °C, respectively, with 25 °C ambient temperature. For T_{amb}= 75

°C, the equilibrium temperatures are about 145 °C and 115 °C for Q1/Q4 and Q2/Q3, respectively (see Figure 3-19).

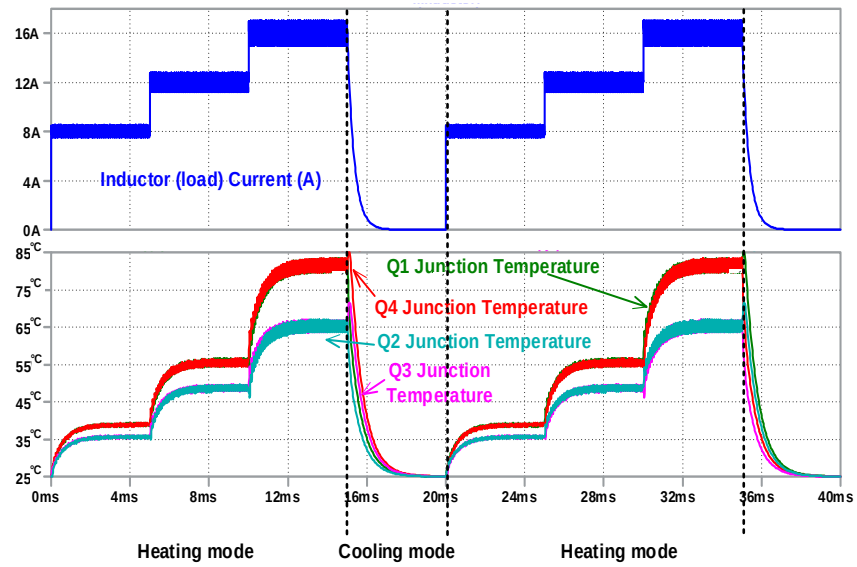


Figure 3-18.(i) Inductor load current (ii) Junction temperature of four DUTs at 25 °C ambient temperature

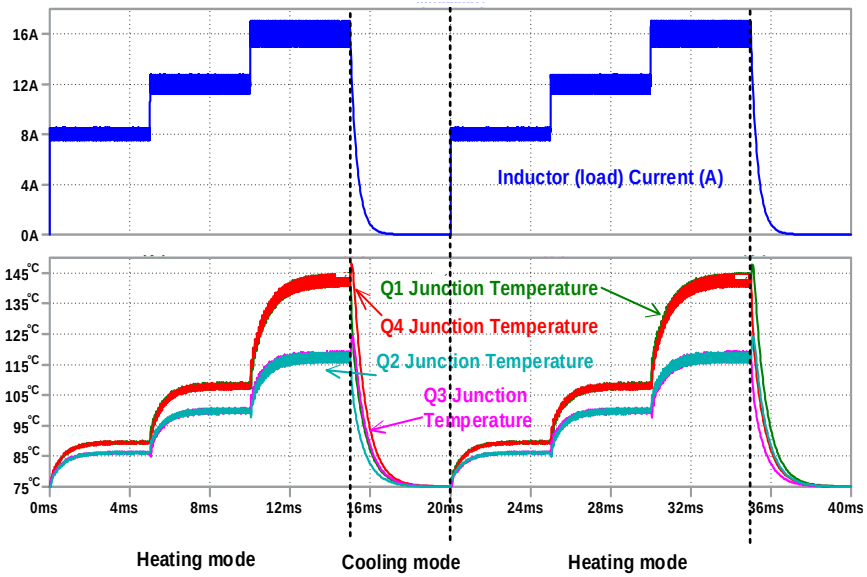


Figure 3-19. (i) Inductor load current (ii) Junction temperature of four DUTs at 75 °C ambient temperature

The difference between Q1/Q4 and Q2/Q3 equilibrium temperatures is 15 °C at T_{amb} =25 °C and 25 °C at T_{amb} =75 °C. The 10 °C variation (25 – 15 = 10 °C) at different ambient conditions is due to the impact of higher heat dissipated on device degradation performance even with the same mission profile. After completing several cycles (in the range of thousands of cycles), for each current step in the mission profile, at specific ambient temperatures, the equilibrium temperatures of the DUT will keep increasing until DUT fails. It means that the equilibrium temperature of DUT at the failure point would be different and increased compared to DUT's equilibrium temperature at the beginning of the test. Therefore, this increment in DUT's equilibrium junction temperature can be considered a new health indicator of power switches. Using $V_{DS(ON)}$ measurement circuit to estimate $R_{DS(ON)}$, a correlation between T_{equib} and $R_{DS(ON)}$ can be drawn during the degradation process. This advantage can help to interpret power devices' failure behavior under actual operation only by monitoring the case temperature or heatsink temperature. Temperature measurement is easier to implement and more reliable than implementing a separate $V_{DS(ON)}$ measurement circuit to calculate the ON-state device resistance.

It should be noted that to simulate the degradation cycle fast enough in LTspice, the thermal capacitance of DUT is reduced 1000 times in the thermal model. It is also possible to have various current mission profiles at different ambient temperatures based on SiC power device specifications. In the proposed thermal degradation setup, a thermoelectric cooler (TEC) with a current-based controller will be used to cool down the DUT to ambient temperature fast after cutting the load current from 16 A to 0 A

within 2 ms, as shown in Figure 3-20. Having a lower thermal time constant for the proposed procedure compared to that of conventional test setup results in reducing the cost of time and power usage to degrade the power devices.

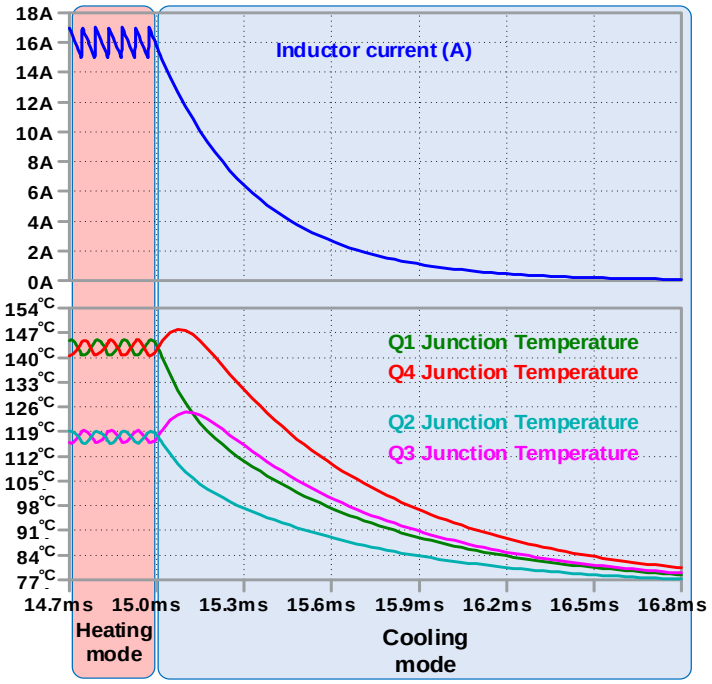
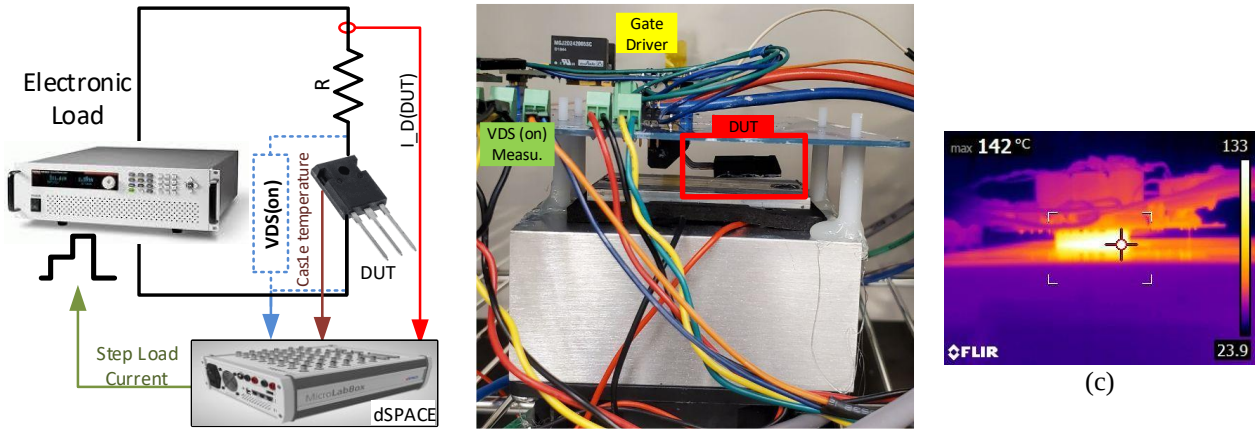


Figure 3-20. Fast turning off for cooling down the DUT up to the ambient temperature (i) Inductor (load) current (ii) DUTs junction temperature

3.2.1. The experimental results of the proposed test setup

In order to prove the feasibility and the capability of the proposed test procedure, an experimental hardware setup is designed and implemented to test the thermal equilibrium of SCT2450KEC SiC-MOSFET in the presence of step changes in load current. As shown in Figure 3-21, the power device with a maximum current of 10 A is connected to an electronic load that provides a step current waveform. The experiment starts with 4 A, then increases to 6 A, followed by 8 A load current. The $V_{DS(ON)}$ is also included with hardware setup to measure the $R_{DS(ON)}$ variation during the test; see Figure

3-21(b). A k-type thermocouple is attached to the case of SiC-MOSFET to measure its temperature and estimated the DUT's junction temperature. The whole setup is kept in the temperature chamber, and its temperature is set to 25 °C. The data are stored in, and control gate pulses come from dSPACE-RTI1202. The thermal IR camera snapshot of DUT during the test at 25 °C ambient temperature is captured. As shown in Figure 3-21(C), the lowest temperature is 23.9 °C, and the hottest spot is the DUT with a case temperature of 142 °C. Considering the generated heat by the device losses, this temperature is added to the case temperature and let the experiment run until T_J reaches its equilibrium value and then, the next step change will apply to the device. The experimental results of thermal equilibrium of the DUT under three-step changes are shown in Figure 3-22. The initial temperature of 25 °C is increased to 62.5 °C with 4 A current, then reaches 105 °C with 6 A and finally with 8 A current, the junction equilibrium temperature is stabilized at 170 °C.



(a) (b) (c)

Figure 3-21. (a) the schematic of the test setup (b) the hardware setup (c) thermal IR camera snapshot of DUT during the test at 25 °C ambient temperature

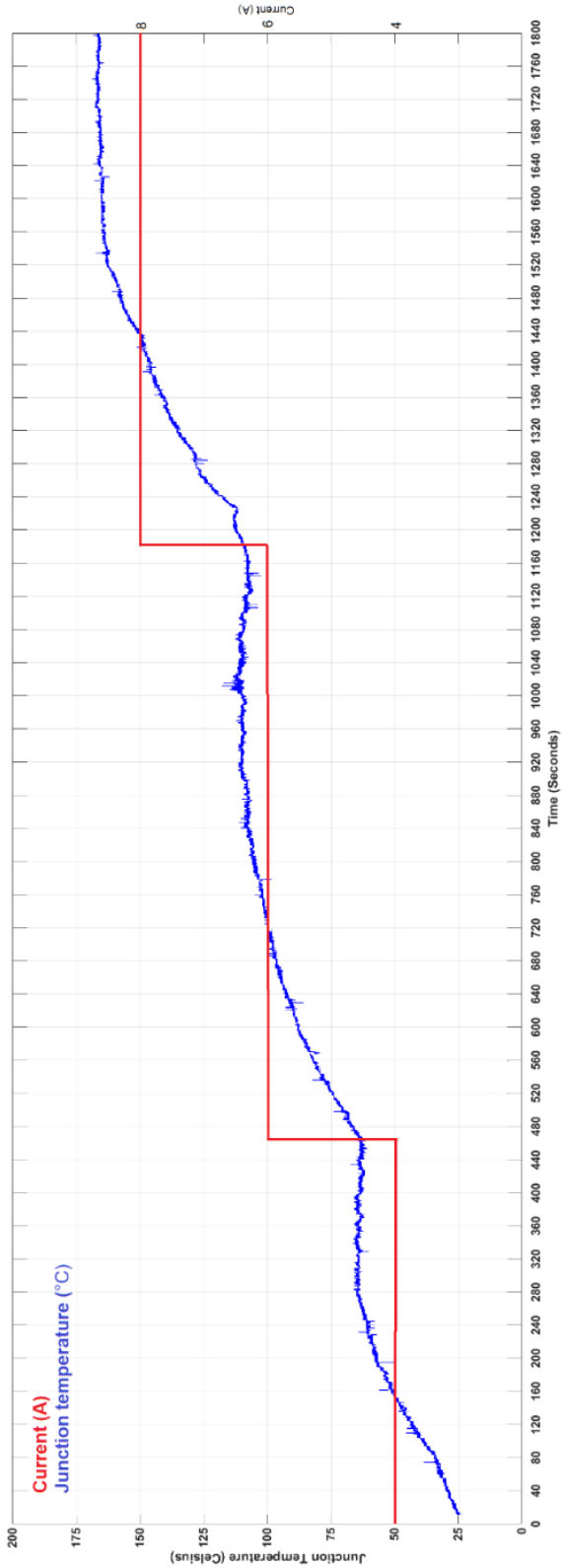


Figure 3-22. The experimental result of DUT equilibrium temperature at 25 °C ambient

CHAPTER 4.

MEASURE THEORY–BASED APPROACH FOR REMAINING USEFUL LIFETIME PREDICTION IN POWER CONVERTERS

In this chapter, a new method for evaluating the survival index (system-level RUL) of power converters is proposed. This method aims to address the issues of predicting RUL of component and power converters by developing a statistical approach using probability density functions (PDFs) and associated concepts in measure theory to predict the probability of system failure using individual components' qualification data. Focusing on the system-level operation, a new real-time reliability prediction approach using ANN-based for power FET devices and power converters is proposed in this chapter. The main advantages of the proposed method are:

- Measure theory-based algorithm uses data obtained via actual qualification of device samples, in various ambient temperatures and under different power levels.
- The proposed algorithm can be applied for other power converters or any general system, consisting of multiple critical sub-systems or components.
- Evaluating the probability of survival of power converters with online monitoring of health indicator variations over time using a machine-learning-based approach
- $R_{DS(ON)}$ value estimation considers the devices' fast switching performance during ON time via a $V_{DS(ON)}$ measurement circuit.
- Usage of component-level RUL indices for power FETs, capacitors and other critical components.

- The simple ANN model resulting from this approach to predict the probability of survival index is light in computational memory usage and can be implemented on graphics processing units (GPUs) or FPGAs.

4.1. Component-level RUL calculation algorithm

for further component-level reliability calculation, the experimental degradation data of $R_{DS(ON)}$ provided in CHAPTER 3 is fitted to an exponential equation ($R_{DS\_ON} = a * e^{bt}$) to model the component behavior during the operational lifetime [85], [95], as shown in Figure 4-1. For device RUL estimation, at any given point in the operation run time, the time (or the number of cycles) difference between the current values to the failure value of the respective health indicators in each of the 'n' samples will be calculated. In other words, the RUL of each component is the difference between the intersections of the exponential model with a value of health indicators at the time t_i and time of reaching failure threshold at $t_{EoL(i)}$ [$T_{RUL(i)} = t_{EoL(i)} - t_{(i)}$].

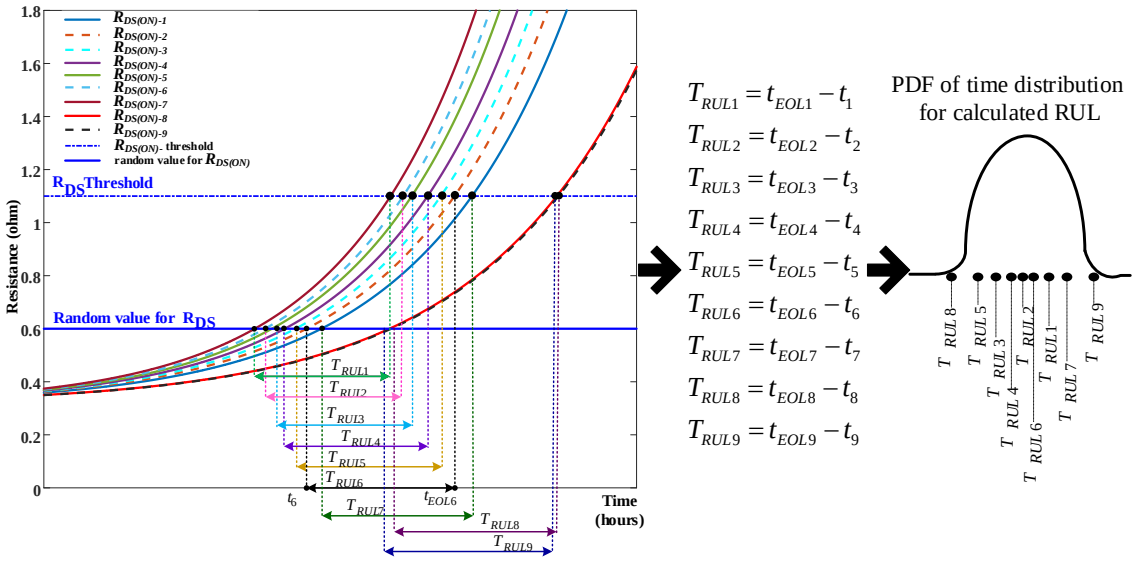


Figure 4-1. Dataset for SiC-MOSFET health indicator ($R_{DS(ON)}$), RUL definition, and pdf distribution

For example, the SiC-MOSFET degradation model and calculated RUL times are shown in Figure 4-1. With a random value of $R_{DS(ON)}$ = 0.6 Ω and the threshold value of 1.1 Ω for the component (solid and dashed blue color lines in Figure 4-1) and considering all calculated $T_{RUL(i)}$ for nine samples, the lifetime distribution for RUL (or time-to-failure distribution) can be obtained and fitted with an appropriate distribution function like Beta, Gamma or Skew normal distribution. For simplicity, a normal distribution is used to fit data in this research. Therefore, RUL is represented by a probability distribution, describing the probability of the predicted RUL of the component with time. It should be noted that due to the uncertainties in the lifetime prediction, the reliability metric is usually expressed in terms of statistical values rather than a fixed value. A similar procedure is implemented for electrolytic capacitors based on *ESR* decrement to calculate RUL's PDF [85]. These PDF characteristics will be used in the proposed survival measurement described in the next section.

Once the converter module is implemented and is under operation, the different system parameters need to be continuously monitored. Considering a power electronic converter with '*x*' components, the whole system cannot function if any '*x*' components fail. It means that the failure of each component results in a loss of operation for the converter.

4.2. System-level health monitoring procedure

An isolated DC/DC converter with four devices-under-measurements (DUMs) shown in Figure 4-2 is considered a system in this work. For simplicity of analysis, it is assumed that the diodes and high-frequency transformers have a longer life than SiC FETs and capacitors. The operational converter parameters have a very high likelihood to have characteristics very similar to the ones that underwent qualification.

The system-level survival index is described as follows. As described in the previous section, a set of values for *'n'* samples of two major components, SiC-MOSFET, and capacitor, is provided to find the probability of RUL at any given operation time (t_i). With these values, PDFs of RUL for each component can be derived in terms of "*time in the future*" operation, which means how much time in the future with respect to the present time of operation is remained for the component to be failed.

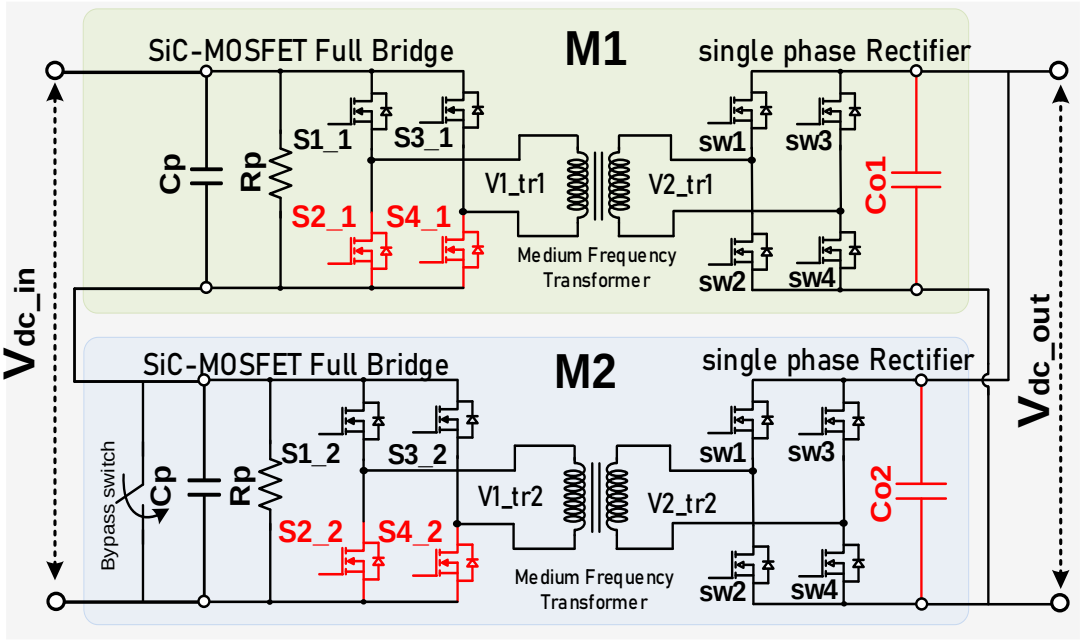


Figure 4-2.The fault-tolerant modular DC/DC converter for system-level RUL prediction (DUMs are in red color)

Considering the converter system in Figure 4-2, four SiC switches and two capacitors are used (number of 6 DUMs). Therefore, in this case, the corresponding PDF of RUL for these six components will be considered to evaluate the system-level survival index.

4.2.1. System-level probability of survival for fault-tolerant modular DC-DC converter

Considering the fault-tolerant modular DC-DC converter shown in Figure 2-2 and introduced in CHAPTER 2, the probability of survival for the entire power converter under normal and faulty operating mode is calculated. There are *J* number of DUMs in each module (here *J*=3), *M* number of modules in each cluster (here *M*=4), and *K* number of paralleled clusters (here *K*=6). Therefore, the total number of health indicator parameters would be $J \times M \times K$ is equal to 72.

Considering the hardware setup shown in Figure 4-2, there are three DUMs inside of each module (two $R_{DS(ON)}$ and one ESR_C). The component-level remaining useful life for the J^{th} DUM (PDF_{DUM_J}) is calculated based on the proposed methodology described in Section 4.2. The module-level probability of survival ($P_{Module-m}$) is calculated as equation

$$P_{Module-m} = PDF_{DUM1} \times PDF_{DUM2} \times PDF_{DUM3} \times \ . \ . \ . \times PDF_{DUM_J} \qquad (4.1)$$

where PDF_{DUM_J} is calculated using equation

$$PDF_{DUM_J} = \left(\int_0^{\infty} pdf_x.dt - \int_o^{t} pdf_x.dt \right) \Big|_{x \;=\; R_{DS(ON)} \;\; or \;\; ESR_C} . \qquad (4.2)$$

To calculate the cluster-level probability of survival, the correlation of the probability among all modules inside the same cluster is considered. Under the faulty operation mode of the converter, it is assumed that only one module inside each cluster can be bypassed to keep the whole converter operating. The operational condition of a cluster is defined so that at least three modules are still operating, and only one of the modules inside the same cluster is faulty and will be bypassed. If two or more than two modules of each cluster get faulty and bypassed, that cluster is considered "out of operation," and the whole DC/DC converter (system) will stop working.

Different combinations of scenarios are considered. First, all four modules inside each cluster are operating (surviving), called "normal operating mode," where all clusters are operating normally. Second, if one module fails and the other three modules are working, the cluster is called "faulty operating mode," With bypassing the faulty module, the same cluster will continue its operation. Third, if two or more than two modules fail, the whole cluster will be considered "out-of-operation" and will stop the whole converter's operation. The first two possible operating modes are reflected in calculating the probability of survival, where the last scenario is not reflected since it will shut down the whole system.

To reflect the probability of survival for one module failure under the faulty operating mode, the equation (4.3) is used to calculate the probability of survival for one cluster.

$$
\begin{aligned}
P_{Cluster-k} = & \left\{\left(P_{Module-1}\right)\times\left(P_{Module-2}\right)\times\left(P_{Module-3}\right)\times\left(P_{Module-4}\right)\right\} + \\
& \left\{\left(P_{Module-1}\right)\times\left(P_{Module-2}\right)\times\left(P_{Module-3}\right)\times\left(1-P_{Module-4}\right)\right\} + \\
& \left\{\left(P_{Module-1}\right)\times\left(P_{Module-2}\right)\times\left(1-P_{Module-3}\right)\times\left(P_{Module-4}\right)\right\} + \\
& \left\{\left(P_{Module-1}\right)\times\left(1-P_{Module-2}\right)\times\left(P_{Module-3}\right)\times\left(P_{Module-4}\right)\right\} + \\
& \left\{\left(1-P_{Module-1}\right)\times\left(P_{Module-2}\right)\times\left(P_{Module-3}\right)\times\left(P_{Module-4}\right)\right\}.
\end{aligned}
\tag{4.3}
$$

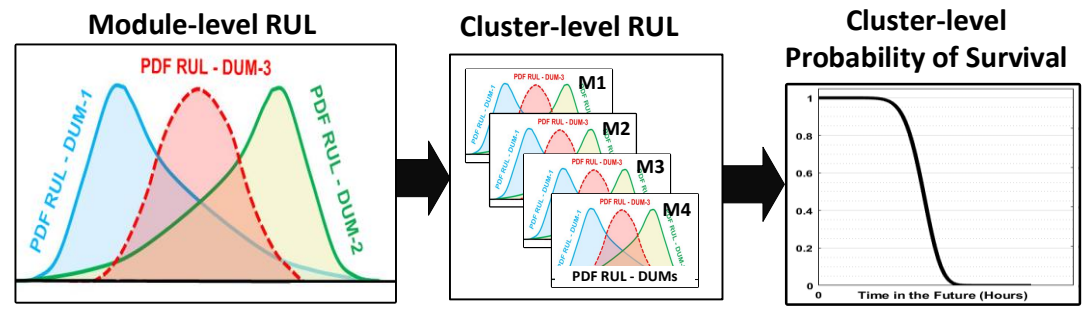
The whole calculation procedure for the cluster-level probability of survival starting from component-level RUL evaluation is shown in Figure 4-3(a). Figure 4-3 (b) shows the modular DC/DC converter (see Figure 2-2 in CHAPTER 2) from a probability perspective. To predict the system-level RUL index, the correlation of the probability of survival for all clusters is considered so that the failure of one cluster fails in the whole system.

The equation for the system-level RUL prediction is defined as equation (4.4), where it is the multiplication of the survival index for each cluster

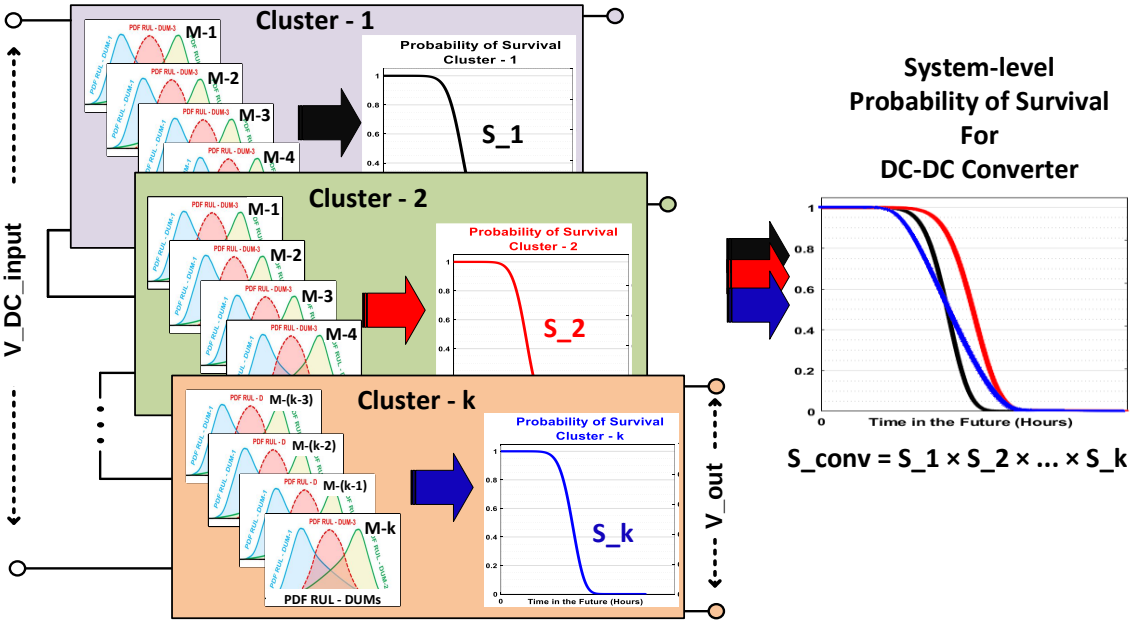
$$
P_{DC/DC\_converter} = \left(P_{Cluster-1}\right)\times\left(P_{Cluster-2}\right)\times \ . \ . \ . \ \times\left(P_{Cluster-k}\right). \tag{4.4}
$$

The system-level survival calculation method can be modified with a different configuration of any power electronic converters, including DC/DC, DC/AC, etc. The only requirement for the proposed methodology measures the health indicator parameters within the converter. The equations (4.1) to (4.4) can be used in fault-tolerant operation mode, while in case of any fault, the faulty module will be bypassed. All DUMs inside the faulty module will be taken off from the equation. Therefore, health indicator parameters ($R_{DS(ON)}$ and ESR_C) and related RUL PDFs will no longer present

n the calculation. But, the probability of survival of that cluster will still be calculated without a faulty module. It means that the procedure appropriately modifies itself to compensate for the loss of faulty modules during the operation.



(a)



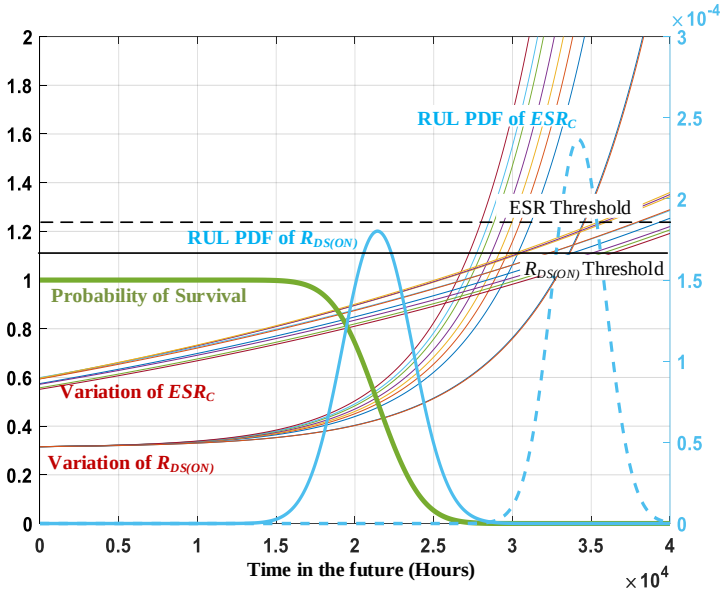
(b)

Figure 4-3. (a) The procedure of cluster-level probability of survival calculation (b) The system-level probability of survival calculation for the whole modular fault-tolerant DC/DC converter described in CHAPTER 2

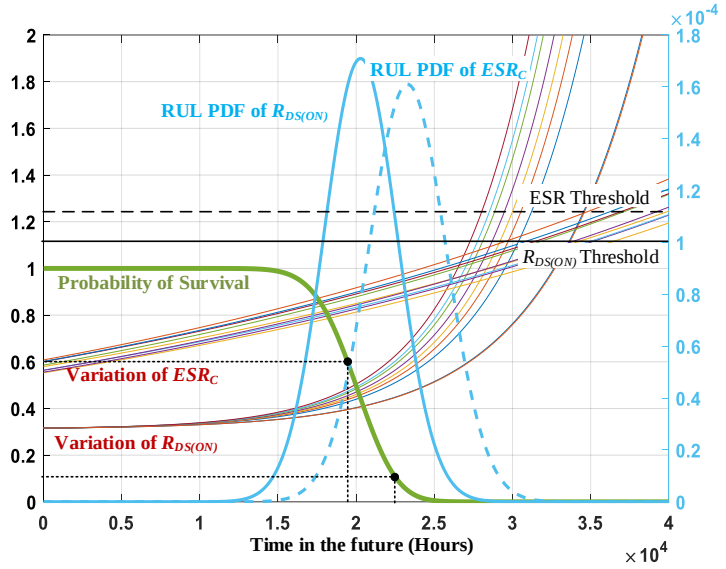
Assuming the converter shown in Figure 4-2, there are two clusters, *K=2*, one module in each cluster, *M=1*, and three DUMs in each module, *J=3*. The total number of parameters would be six health indicators, four $R_{DS(ON),}$ and two ESR_C. The effective survival probability of the converter at a specific time *'t'* in the future is given by equations (4.1) - (4.4), based on the combined evaluation of the areas under the RUL PDF curves, is

$$P_{DC/DC\_converter} = \left[\underbrace{\left(PDF_{R_{DS(ON)-S2\_1}}\right) \times \left(PDF_{R_{DS(ON)-S4\_1}}\right) \times \left(PDF_{ESR_{C-OUT-1}}\right)}_{Cluster-1} \right] \times \left[\underbrace{\left(PDF_{R_{DS(ON)-S2\_2}}\right) \times \left(PDF_{R_{DS(ON)-S4\_2}}\right) \times \left(PDF_{ESR_{C-OUT-2}}\right)}_{Cluster-2} \right]. \quad (4.5)$$

This equation can be extended to '*k*' parameters for different configurations of a power converter with '*k*' num ber of critical components. From the above equation, it can be seen that the survival probability ($P_{DC/DC\_converter}$) of the converter at any given time in the future will be affected by the PDF of the most critical component(s) (ones that are most likely to fail first). However, the actual failure of any one part will constitute the failure of the system. For example, the RUL PDFs of *k* = 2 parameters, one $R_{DS(ON)}$ and one ESR_C, were considered and derived with available degradation data (n=9 samples for SiC-MOSFET and n=9 samples for capacitor) for a random set of 'present' values for these two parameters. Figure 4-5 shows the dataset, threshold values, and the RUL PDFs for components. The system-level survival probability of the converter is calculated based on equation (4.1).



(a)



(b)

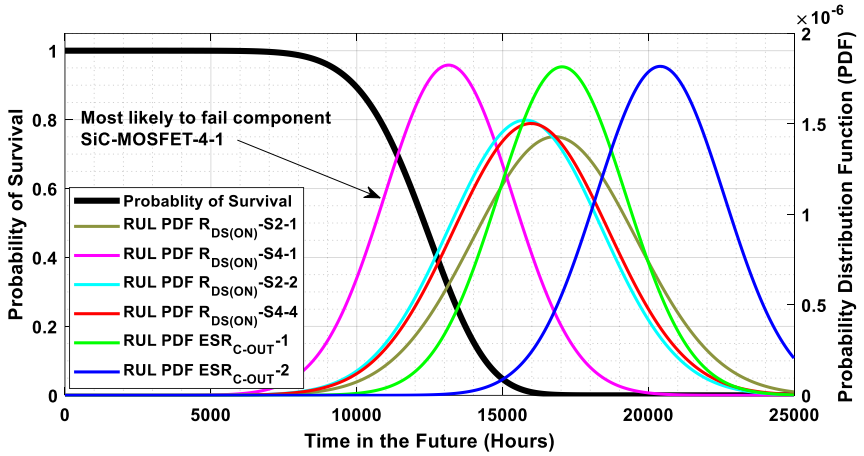
Figure 4-4. The RUL PDFs and probability of system survival with two components (a) Almost no overlap (b) Considerable overlap

Figure 4-5 shows the dataset, threshold values, and the RUL PDFs for components. The system-level survival probability of the converter is calculated based on equation (4.1). Figure 4-5(a) shows the scenario where there is no overlap between the respective RUL PDFs of the two parameters, which means that the probability of

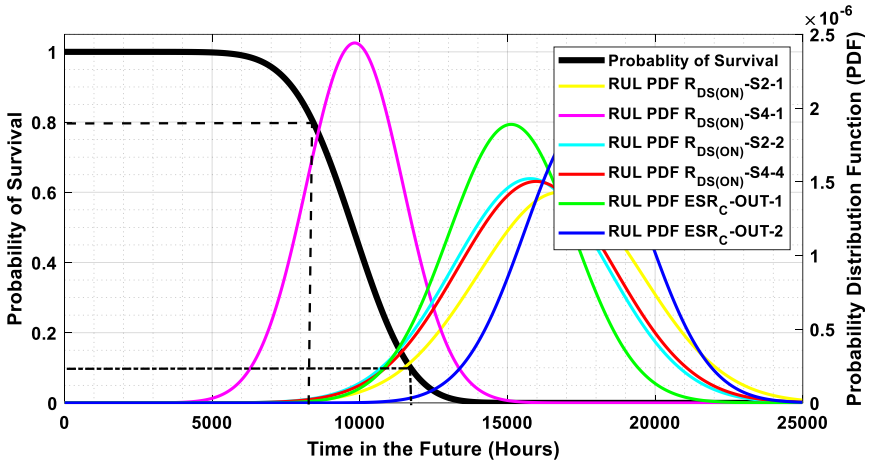
survival of the overall system is determined mainly by that of the FET, which is most likely to fail much earlier than the capacitor. Figure 4-5(b) shows the scenario with significant overlap (as will be in most practical applications involving multiple devices).

Figure 4-5 shows the PDFs for six components calculated by component-level RUL prediction described earlier. The system-level survival probability of the converter is calculated based on equation (4.1). It shows that the overall system reliability index is determined mainly by the component, which is most likely to fail much earlier than other components. For example, in Figure 4-5(a)), for a scenario of $R_{DS(ON)\_1}$=0.538 **Ω**, $R_{DS(ON)\_2}$=0.561 **Ω**, $R_{DS(ON)\_3}$=0.6105 **Ω**, $R_{DS(ON)\_4}$=0.5018 **Ω**, ESR_{C_1}=1.4025 **Ω**, ESR_{C_2} =1.32684 **Ω** for health indicators, the PDF of RUL for $R_{DS(on)}$ of $S_{4\text{-}1}$ plays crucial role to fail the whole system, since its value is close to the threshold value of SiC-MOSFET failure. In Figure 4-5(b), another scenario consists of values for $R_{DS(ON)\_1}$=0.556 **Ω**, $R_{DS(ON)\_2}$=0.661 **Ω**, $R_{DS(ON)\_3}$=0.571 **Ω**, $R_{DS(ON)\_4}$=0.568 **Ω**, ESR_{C_1}=1.523 **Ω**, ESR_{C_2}=1.4415 **Ω** which concludes to estimate system-level survival probability based on $R_{DS(on)}$ of $S_{4\text{-}1}$ which is most likely to fail earlier than other components. From these estimates, it will be possible to extract a wide range of information. Under case (b) in Figure 4-5, there is an 80 % chance (probability of 0.8) that the converter will survive for another 8,100 hours and a 10 % chance that it will function for 11,900 hours, given the same conditions. The more expected time for operation, the less probability of happening. Also, it can be estimated that the converter will fail after 13,500 hours. Such information will help both operators and supply chain personnel estimate when replacement parts are needed or take any urgent action to

protect the system from potential damages. When the operating conditions change, the RUL estimate also adapts.



(a)



(b)

Figure 4-5. The RUL PDFs and probability of survival with six health indicator values
(a) $R_{DS(ON)\_1}$= 0.538, $R_{DS(ON)\_2}$=0.561, $R_{DS(ON)\_3}$=0.6105, $R_{DS(ON)\_4}$=0.501, ESR_{C_1}= 1.402, ESR_{C_2}=1.326
(b) $R_{DS(ON)\_1}$= 0.556, $R_{DS(ON)\_2}$=0.661, $R_{DS(ON)\_3}$=0.571, $R_{DS(ON)\_4}$=0.568, ESR_{C_1}= 1.523, ESR_{C_2}=1.4415

Considering a modular fault-tolerant DC/DC described in CHAPTER 2 consists of 6 clusters in parallel, four modules in each cluster, a total of 24 modules, the equation (4.1) can be extended as below. There are three DUMs in each module (two $R_{DS(ON)}$ and one ESR_C). Therefore, a total of 72 health indicators would be used in the effective

survival probability of the converter equation. To monitor any converter's health operation in real-time mode, a machine learning algorithm is used and trained considering a large number of combinations among health indicators to cover any possibility of variation. For the converter used in this research, all possibilities of variation for six health indicators, including four $R_{DS(ON)}$ of SiC-MOSFETs and two ESR_C of capacitors, are changing between its initial value up to its failure threshold $R_{initial} < R_{DS(ON)} < R_{threshold}$ and $ESR_{initial} < ESR_C < ESR_{threshold}$. Then, the *RUL PDFs* of all components and probability of survival index for the whole system (*P_converter*) are calculated by considering all possible combinations among health indicators. Using this data, an Artificial-Neural-Network (ANN) is trained to perform online health-monitoring with new incoming input data from health indicators ($R_{DS(ON)}$ and *ESR*). A two-layer backpropagation network shown in Figure 4-6 with sigmoid hidden neurons and linear output neurons is implemented to fit multi-dimensional mapping.

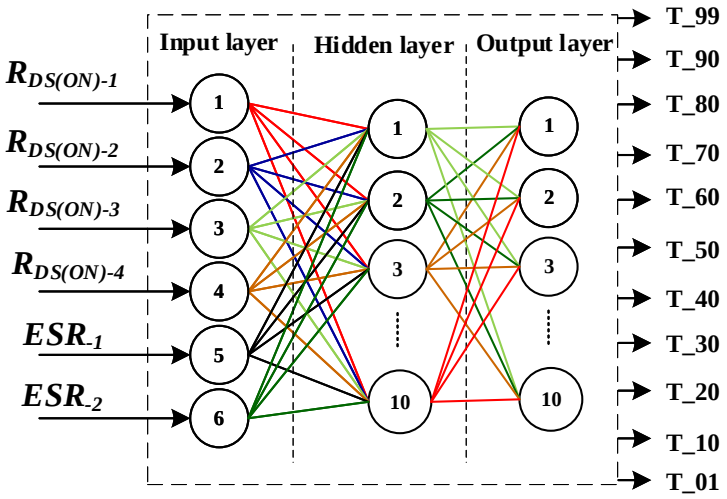


Figure 4-6. The trained ANN for online RUL prediction

The input layer has six neurons to receive six input variables: the $R_{DS(ON)}$ and *ESR*. The output layer has one neuron, which outputs the system-level probability of survival in eleven indices between 01 % to 99 % of failure chance. The hidden layer has ten neurons. Each neuron in one layer is connected with each neuron in the next layer. Each connection has a weight. Each neuron computes the sum of the weighted inputs and the bias. Afterward, it uses an activation function, Levenberg–Marquardt, Bayesian, and Gradient, to compute the neuron's output and send the output to the next layer. The specification of trained ANN is presented in Table 4.1.

Table 4.1 The trained ANN specification and information

Number of hidden layers	2
Number of hidden neurons	10
Number of inputs	6
Number of outputs	11
Training Performance	0.0383
Validating Performance	0.0423
Test Performance	0.0055

The Levenberg–Marquardt algorithm (LMA) [96], which is a hybrid technique that uses both Gauss-Newton and steepest descent approaches to converge to an optimal solution, is used. This algorithm typically requires more memory but less time. Training automatically stops when generalization stops improving, as indicated by an increase in the mean square error of the validation samples. The Bayesian Regularization method

typically requires more time but can result in good generalization for difficult, small, or noisy datasets.

Training stops according to adaptive weight minimization (regularization). The third method, Scaled Conjugate Gradient, requires less memory. Training automatically stops when generalization stops improving, as indicated by an increase in the mean square error of the validation samples. The data is split into three categories, training, validation, and test. The training dataset is presented to the ANN network during training, and the network is adjusted according to its error. The validation dataset is used to measure network generalization and to halt training when generalization stops improving. The testing dataset does not affect training and provides an independent measure of network performance during and after training.

To get more understandable information, instead of getting time-series output from ANN, lifetime indicator of survival ($T\__x$) is defined in each 10 percent decrement of survival probability and used to monitor the health condition of the converter, as shown in Figure 4-7 (it may be noted that it is the zoomed-in region of the probability of survival plot in Figure 4-5). Thus, the system-level reliability assessment is performed using time $T\__{99}$ (hours in the future) with 99 % probability of survival, $T\__{90}$ (hours in the future) with 90 % probability of survival, etc., still, $T\__{01}$ (hours in the future) with 1 % probability of survival. Thus, the system-level reliability assessment is performed using time $T\__{99}$ with a 99 % probability of survival, $T\__{90}$ with a 90 % probability of survival, etc.

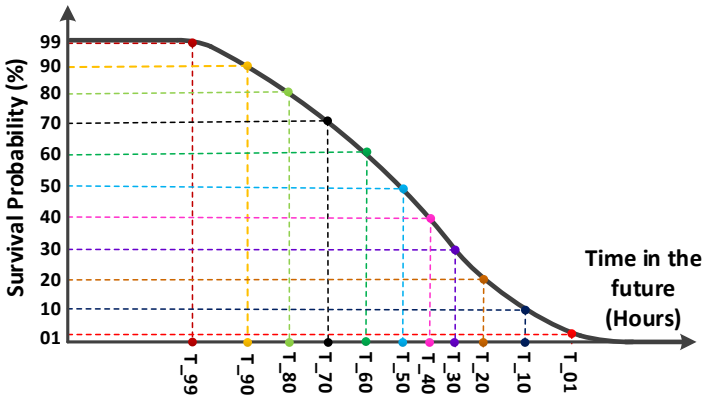
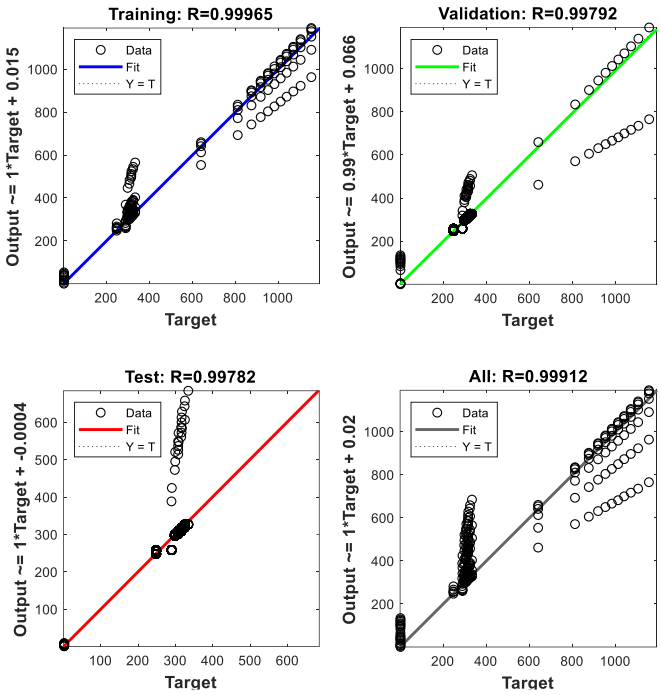


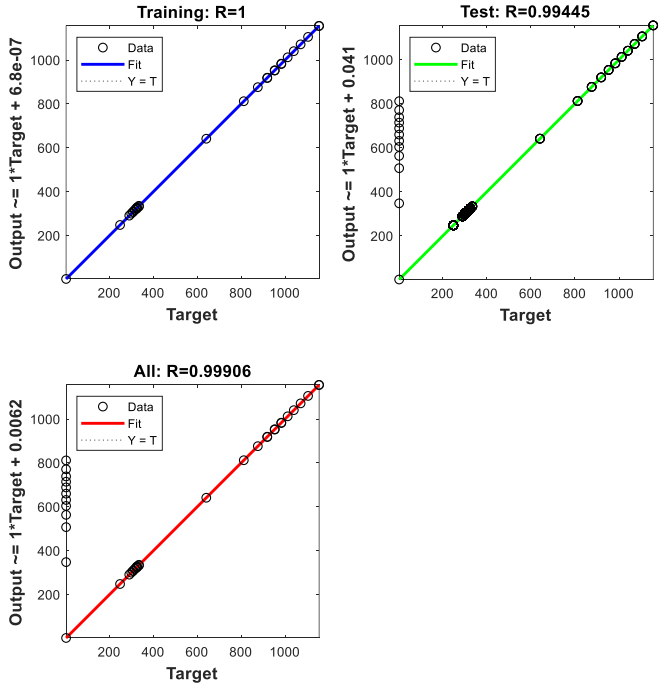
Figure 4-7. The lifetime indicator of survival probability (T_x)

The ANN inputs are the current values of health indicators ($R_{DS(ON)}$ and ESR_C) in practical operation, and the outputs are the $T\__x$ lifetime indicator of survival index. The evaluation process from training/test data for the trained ANN is shown in Figure 4-8. The training process is to tune the weights and biases in the ANN to fit the training data, which are a set of measured health indicators of SiC MOSFETs and capacitors. The backpropagation algorithm is widely used in the training process. Many software programs have toolboxes to automatically train the ANN, which Neural Net Fitting Toolbox in MATLAB is used. The investigation of ANN models is beyond the scope of this paper. By definition, Mean-Squared-Error (MSE) is the average squared difference between outputs and targets where lower values are better, and zero means no error. Regression R-values measure the correlation between outputs and targets. An R-value of 1 means a close relationship, 0 a random relationship. Figure 4-8 (a) shows the regression plot with an R-value of 0.99912 for the overall training process of the Levenberg-Marquardt method. For Bayesian Regularization and Scaled Conjugate Gradient methods, the R-value is 0.99906 and 0.99296, shown in Figure 4-8 (b) and Figure 4-8 (c), respectively.



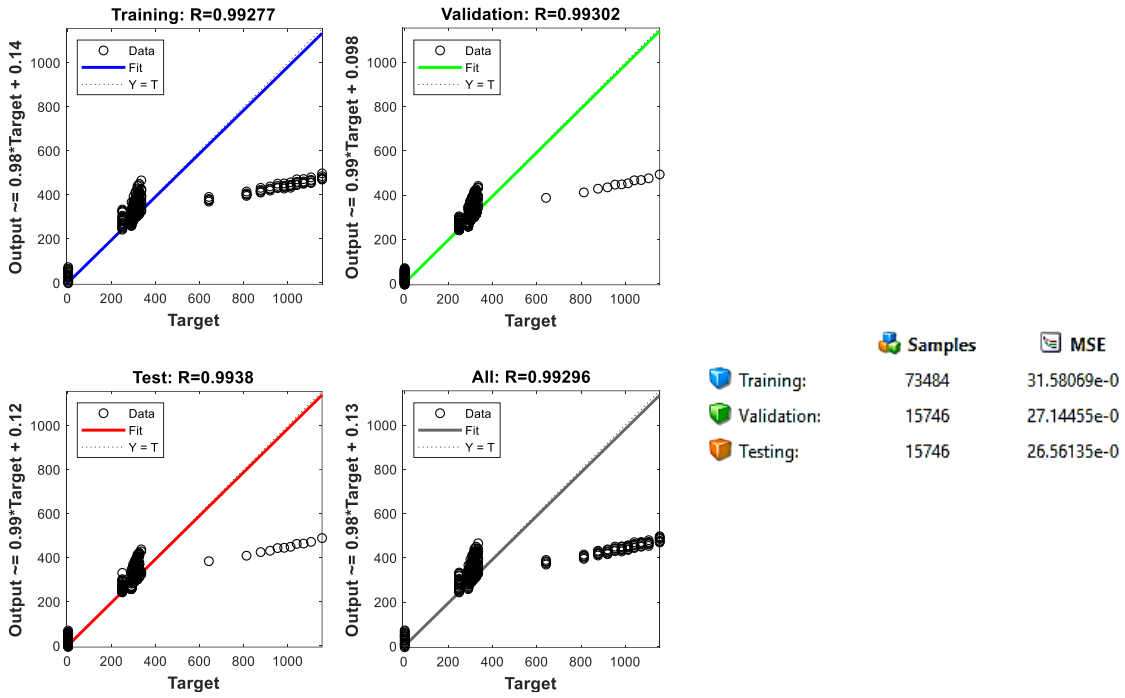
	Samples	MSE
Training:	73484	2.16560e-0
Validation:	15746	6.81634e-1
Testing:	15746	8.81190e-1

(a)



	Samples	MSE
Training:	73484	1.52255e-4
Validation:	15746	0.00000e-0
Testing:	15746	26.83174e-0

(b)



(c)

Figure 4-8. The evaluation indexes of trained ANN (i) Regression plot (ii) Histogram of mean-square error (iii) training performance
(a) Levenberg-Marquardt (b) Bayesian Regularization (c) Scaled Conjugate Gradient

It can be seen that the best MSE is for the Bayesian Regularization method, which means less error between the actual value and predicted value by the trained ANN under this methodology. It is clear that by taking more data points in the training set, the curve estimation can be further improved, while it may take a longer time to arrive at the model.

CHAPTER 5.

PRACTICAL IMPLEMENTATION OF THE PROPOSED ONLINE HEALTH MONITORING FOR MODULAR DC-DC CONVERTER

5.1. Fault-tolerant isolated modular DC-DC Converter

To further prove the proposed online health monitoring capability and feasibility, a scaled-down hardware prototype of a fault-tolerant ISOSP (input series output series-parallel) isolated DC/DC converter is designed and implemented, as shown in Figure 5-1. The specification of the hardware setup is provided in Table 5.1.

Table 5.1 The specification of the proposed converter act as a system for system-level RUL prediction

Parameter	Hardware
Input Voltage	200 VDC
Output voltage	100 VDC
Maximum output power	1000 W
Number of modules	2
Switching frequency	20 kHz
Transformer magnetizing inductance	3.84 mH
Transformer leakage inductance	2.84 μH
Voltage balancing resistor	22.5 kΩ

The SST for the given specifications requires two isolated DC/DC converter modules (M1 and M2) using M.F. transformers. The high voltage primary side of each module is cascaded in series, and the lower voltage secondary side arranged in a parallel

configuration, as shown in Figure 5-1. Each module consists of two $V_{DS(ON)}$ circuit, which is introduced in section 3.1 to measure $R_{DS(ON)}$ of SiC-MOSFETs, voltage and current sensors to measure the ESR_C of output capacitors. The input voltage is 200 V (D.C.) and divided between the individual 2-cascaded modules, and the output voltage is regulated at 100 V with a closed-loop voltage controller (see Figure 5-2). An electric load with a maximum power of 1 kW is connected to the converter to carry the load current up to 10 A, which is the current rate of the SiC-MOSFETs. Since the outputs of two modules are parallel, in normal operation mode, each module carries half of the maximum load current (5 A). To consider faulty operation mode, module-2 (M2) in Figure 5-1 is bypassed with a mechanical switch. In this operation mode, the load current will be delivered through only one module (M1). Therefore, a maximum of 10 A will pass through all SiC-MOSFETS and degrade all DUTs faster than normal operation mode.

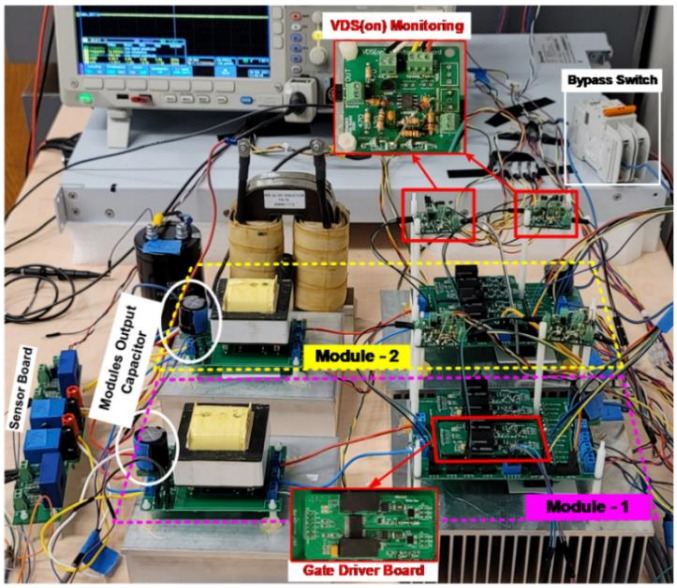


Figure 5-1. The scaled-down experimental hardware setup for the fault-tolerant DC/DC converter for system-level RUL prediction

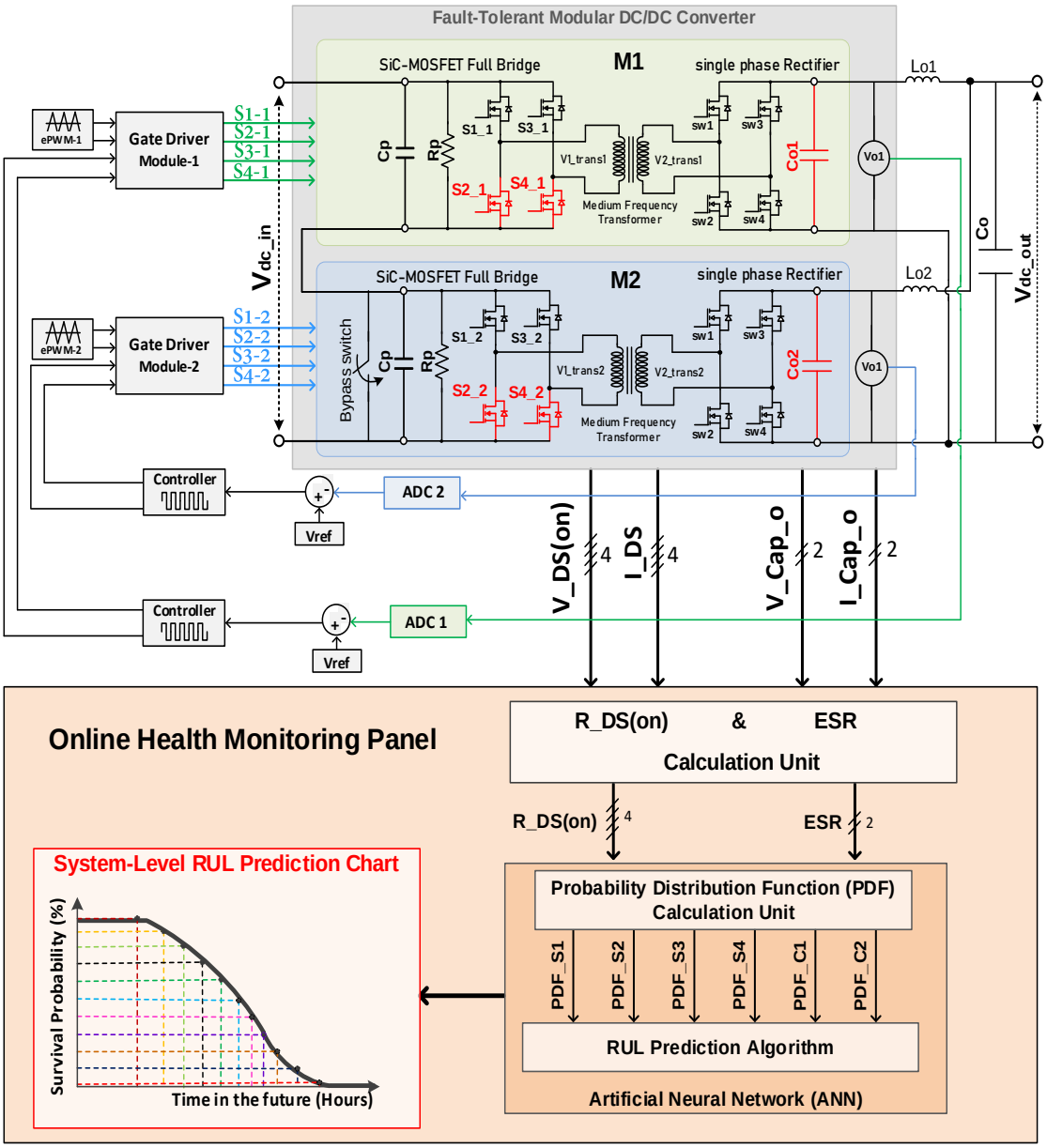


Figure 5-2. The schematic of hardware setup with online health monitoring panel implemented in ANN

In Figure 5-2, the values for the voltage and current measurements of components are sent to the health indicator calculation unit to calculate the $R_{DS(ON)}$ and ESR_C. these parameters are then used in ANN panel to evaluate the system-level RUL indices while converter is operating.

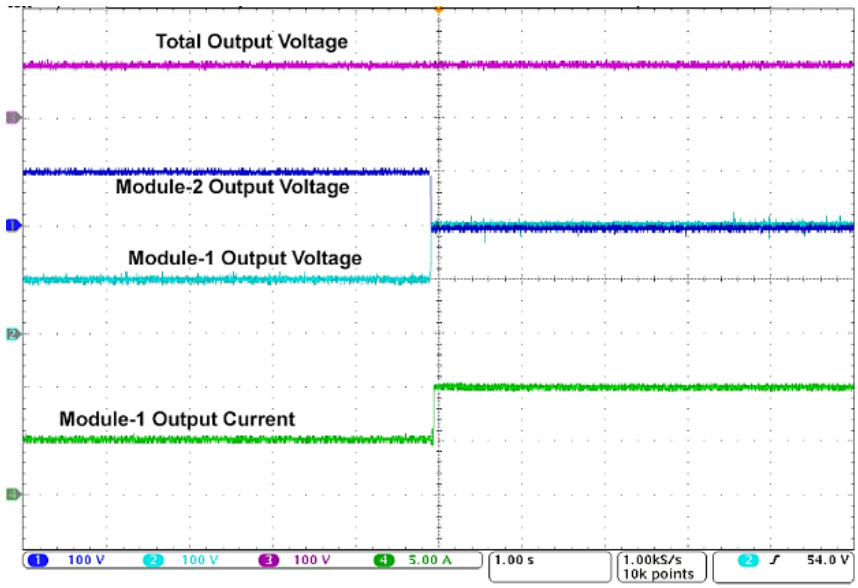


Figure 5-3. (i) The output voltage of converter – 100 V/div
(ii) M-2 output voltage – 100 V/div
(iii) M-1 output voltage – 100 V/div
(iv) M-1 output current – 5 A/div

The output voltage of the converter (V_{out_total}) along with M1 voltage, M2 (the faulty module) voltage, and M1 output current are shown in Figure 5-3. As expected, the controller regulates the total output voltage at the reference value (here is 100 V DC). The rise in the amplitude of M1 voltage is visible, which is done to compensate for the zero voltage of M2 when it is bypassed. The output current of M1 is increased to 10 A in case of bypassing M2.

5.2. Online Health Monitoring of Isolated DC-DC Converter

In this section, the experimental validation results of the proposed online health monitoring of power converter are provided and discussed. The overall online health monitoring procedure is depicted in Figure 5-4.

In order to evaluate the probability of survival index in a modular DC/DC converter, data collection for the most vulnerable power components, SiC-MOSFET, and the capacitor is done while the converter is running. The primary health indicators such as $V_{DS(ON)}$, ESR_C, and T_j are calculated. Using the proposed component-level RUL prediction algorithm, the present operation mode of the system converter is assessed. If there is a fault or any failure in components, an alarm flag is set to ON; otherwise, the system-level RUL index is evaluated for the whole converter via the proposed survival probability algorithm. Based on the survival index, if there is an urgent action of maintenance or replacement for the converter, an alarm flag is set to ON; otherwise, the algorithm will continue to predict the RUL of the power converter.

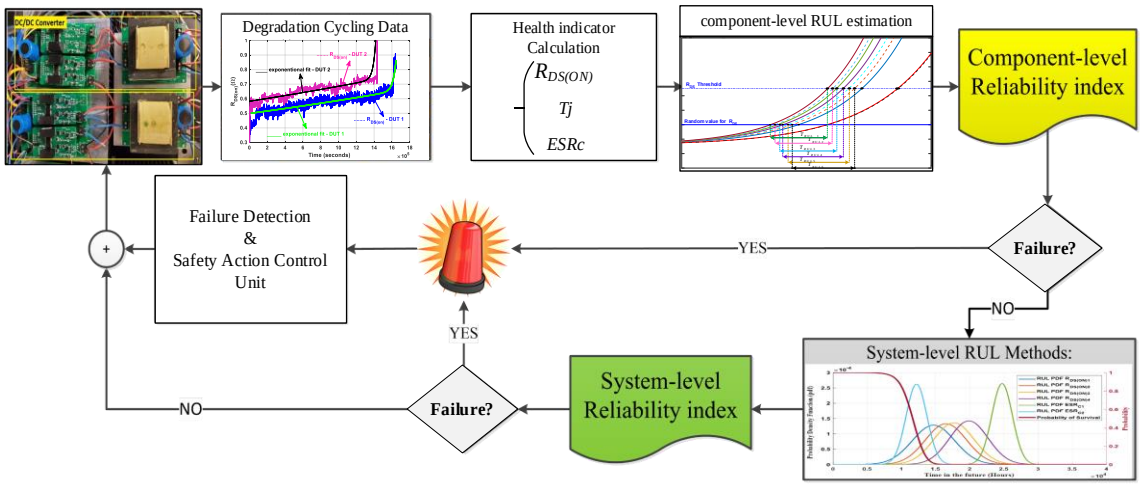
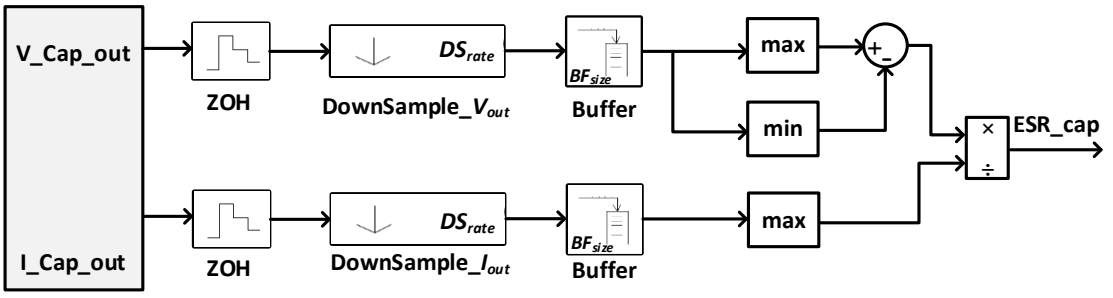
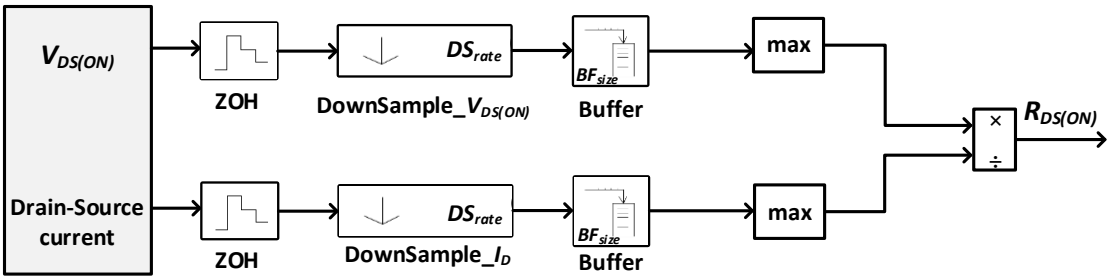


Figure 5-4. The proposed online health monitoring procedure for power electronic converter

As it is shown in Figure 5-2, the online health monitoring panel consists of different units, parameter calculation unit, PDF calculation unit, and RUL prediction unit. All units are programmed in the dSPACE-RTI1202 platform to perform the online survival index of the whole power converter as a system. The main input parameters of the trained ANN are the measured voltage and currents of power components (SiC-MOSFETs and output capacitors), and the output is a system-level probability of survival index. Since both closed-loop voltage controller and online health monitoring panel are programmed on the same platform, due to the memory limitation of the dSPACE, a down-sampling and buffering technique is used for the parameter calculation unit, as shown in Figure 5-5.



(a)



(b)

Figure 5-5. The down-sampling and buffering unit for health indicators calculation units
(a) $ESR_C = \Delta V_{C-ripple}/I_{C\_max}$ (b) $R_{DS(ON)} = V_{DS(ON)}/I_D$

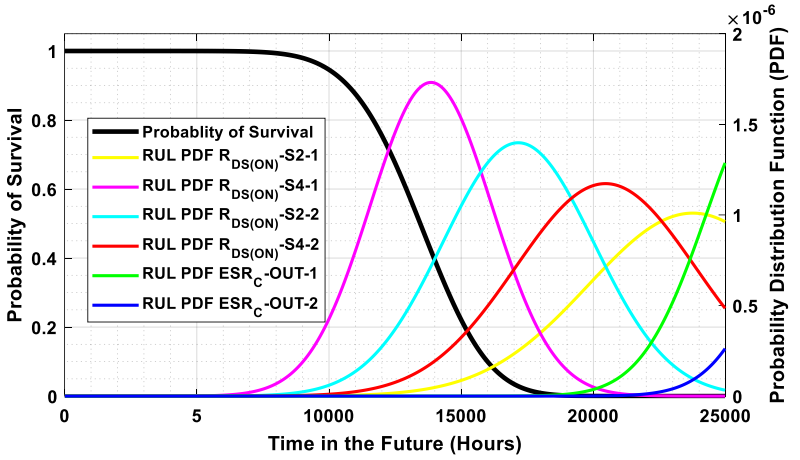
The switching time for SiC-MOSFETs is 50 µs; therefore, the down-sample rate (DS_{rate}) and buffer size (BF_{size}) for $R_{DS(ON)}$ calculation unit are set to 10^6 and 24, respectively. For the ESR_C calculation unit, the sampling time is 25 µs; therefore, a down-sample rate of 10^6 and buffer size of 48 are chosen. Using this technique, every 20 minutes, health indicator parameters are calculated and sent to the ANN unit to predict the survival index. The different data rates can be calculated and implemented as

$$Data\_Rate = \frac{\left(T_{sample/switching} \times DS_{rate} \times BF_{size}\right)}{60} \text{ (per minutes).} \qquad (5.1)$$

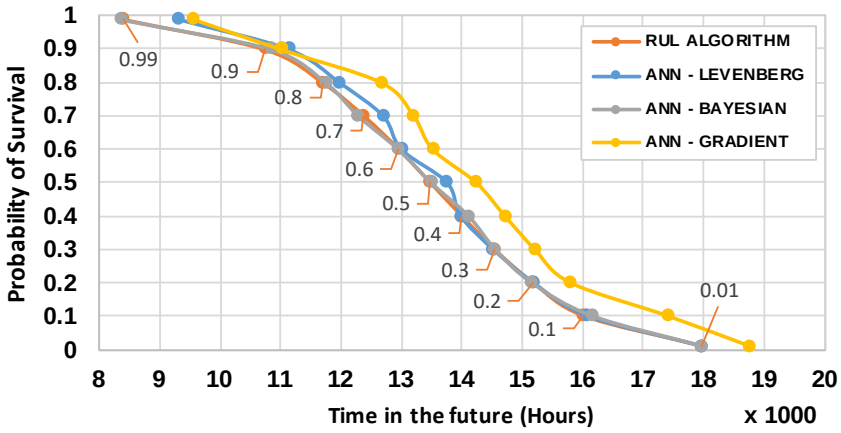
Under DC/DC system operating states, it will take a long time for DUMs' health indicators to increase and reach the failure threshold. Therefore, to accelerate the degradation rate of DUMs, all SiC-MOSFETs and AECs are take out from modular DC/DC converter regularly and put in their relevant degradation setup shown in Figure 3-6 to degrade fast enough. For the fast degradation process of SiC-MOSFETs, maximum voltage, maximum current, and high ambient temperature are applied. Therefore all SiC-MOSFETs are the most vulnerable components to fail and reach $R_{DS(ON)}$ threshold value sooner than that of all ESR_C. Then, all DUMs are placed back on the DC/DC converter to operate. During the operation, all health indicators of DUMs are measured and saved for online health monitoring purposes. Three different evaluating states are chosen, Beginning, Middle, and almost End. To evaluate the performance of the proposed online health monitoring panel, a vector of new values of

health indicators (four $R_{DS(ON)}$ and two ESR_C) are measured and sent to the ANN. The output of ANN is captured as predicted system-level survival probability.

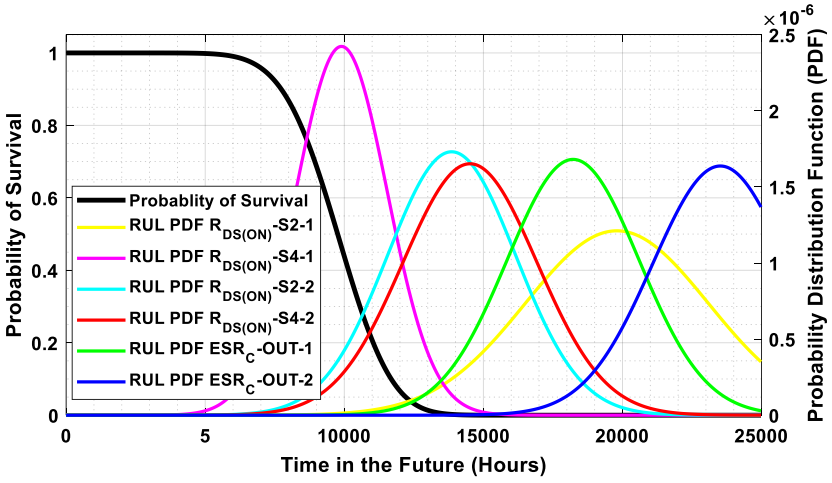
The experimental results of the predicted probability of survival index for three operating states of modular DC/DC (Beginning, Middle, and almost End) are shown in Figure 5-6. The three different trained ANN (Levenberg–Marquardt, Bayesian Regularization, and Scaled Conjugate Gradient) are used to compare the results with each other and also with the calculated survival index via the proposed RUL algorithm. For each operating state, the RUL PDF graphs and the probability of survival are plotted along with calculated and predicted time interval indexes. For example, in Figure 5-6(a), at the beginning of the operation, for input values of 0.4647, 0.603, 0.554, and 0.5018 ohms for four $R_{DS(ON)}$ ($S_{2\text{-}1}$, $S_{4\text{-}1}$, $S_{2\text{-}2}$, and $S_{4\text{-}2}$) and values of 1.25 and 1.144 ohms for two ESR_C (C_{out}-1 and C_{out}-2), the T_{99} is equal to 8349.75. It can be interpreted that with 99 % of probability, the modular DC/DC converter will work for another 8349.75 hours until its end-of-life (EOL). From an operator's point of view, knowing different time interval indexes ($T\_{99, \ldots, } T\_{01}$) can help make a further decision regarding doing required maintenance or replacement in power converters, resulting in reducing periodic maintenance costs without having enough information of time in the future operation.


Probablity of Survival
RUL PDF R_DS(ON)-S2-1
RUL PDF R_DS(ON)-S4-1
RUL PDF R_DS(ON)-S2-2
RUL PDF R_DS(ON)-S4-2
RUL PDF ESR_C-OUT-1
RUL PDF ESR_C-OUT-2
Probability of Survival
Probability Distribution Function (PDF)
Time in the Future (Hours)
×10^-6

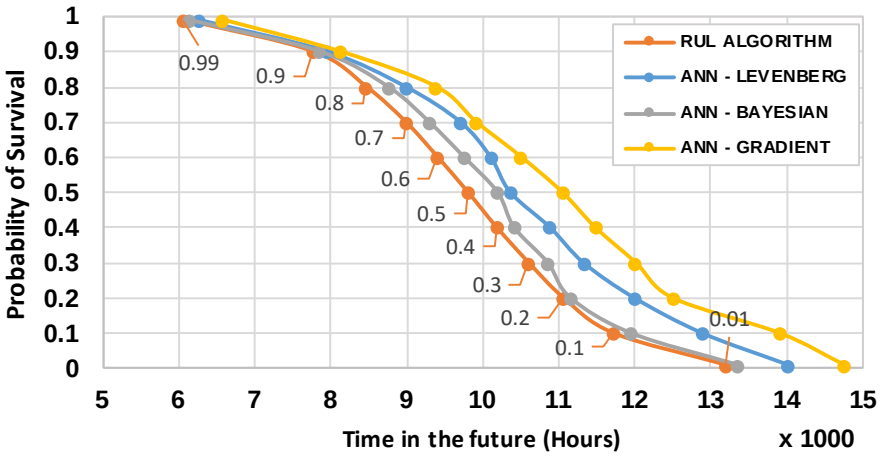
(a)


RUL ALGORITHM
ANN - LEVENBERG
ANN - BAYESIAN
ANN - GRADIENT
0.99
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.01
Probability of Survival
Time in the future (Hours)
x 1000

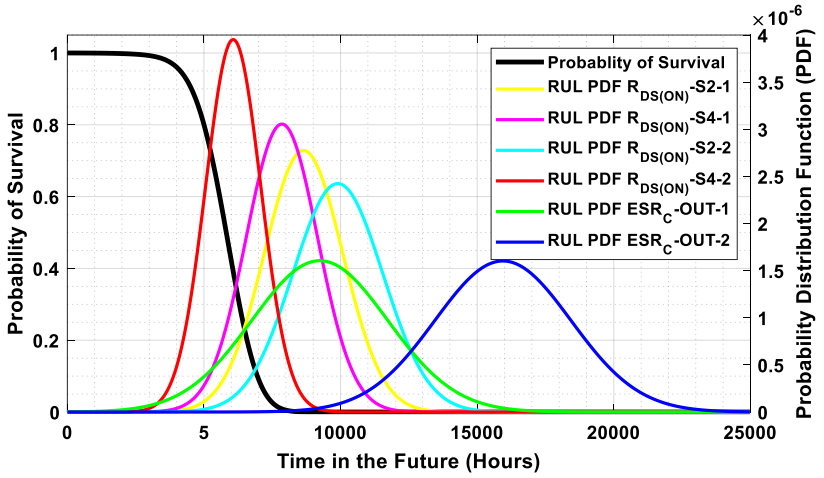
(b)


Probablity of Survival
RUL PDF R_DS(ON)-S2-1
RUL PDF R_DS(ON)-S4-1
RUL PDF R_DS(ON)-S2-2
RUL PDF R_DS(ON)-S4-2
RUL PDF ESR_C-OUT-1
RUL PDF ESR_C-OUT-2
Probability of Survival
Probability Distribution Function (PDF)
Time in the Future (Hours)
×10^-6

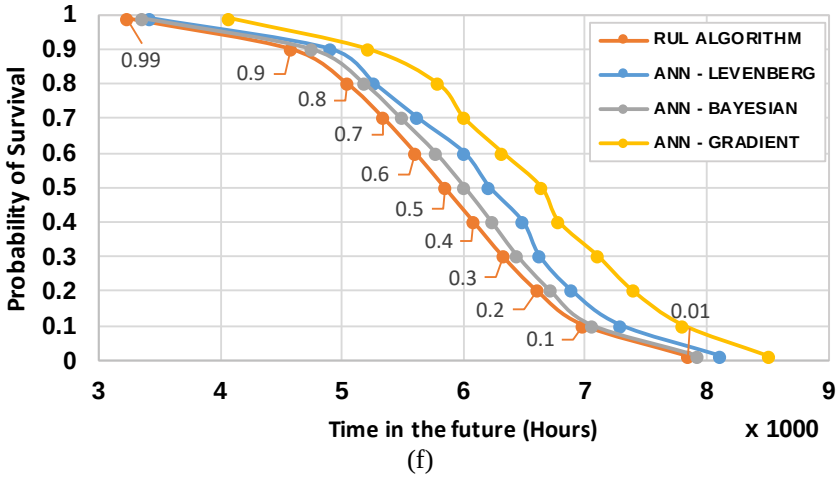
(c)



(d)



(e)



(f)

Figure 5-6. The Experimental comparison between calculated survival probability by the algorithm and predicted survival probability from ANN for three different values of health indicators captured from hardware:

Beginning of operation:

$R_{DS(ON)\_1}$= 0.4647, $R_{DS(ON)\_2}$=0.603, $R_{DS(ON)\_3}$=0.554, $R_{DS(ON)\_4}$=0.5018, ESR_{C_1}= 1.25, ESR_{C_2}=1.144

(a) RUL PDFs for component's failure and system-level survival index

(b) Estimated system-level RUL via algorithm and trained ANN

Middle of operation:

$R_{DS(ON)\_1}$= 0.51, $R_{DS(ON)\_2}$=0.692, $R_{DS(ON)\_3}$=0.612, $R_{DS(ON)\_4}$=0.597, ESR_{C_1}= 1.483, ESR_{C_2}=1.2801

(c) RUL PDFs for component's failure and system-level survival index

(d) Estimated system-level RUL via algorithm and trained ANN

End of operation:

$R_{DS(ON)\_1}$= 0.678, $R_{DS(ON)\_2}$=0.705, $R_{DS(ON)\_3}$=0.668, $R_{DS(ON)\_4}$=0.7288, ESR_{C_1}= 1.764, ESR_{C_2}=1.526

(e) RUL PDFs for component's failure and system-level survival index

(f) Estimated system-level RUL via algorithm and trained ANN

In Figure 5-6(a), at the beginning state of operation for the converter, the highest value of health indicators belongs to the $R_{DS(ON)}$ of S4-1. Therefore, the system-level survival index is mostly affected by the RUL PDF of the corresponding health indicator of $R_{DS(ON)\_2}$=0.603 Ω. For middle and end operating states, as all DUMs are degrading by the time, the most likely component to fail is $R_{DS(ON)\_2}$=0.692 Ω (see Figure 5-6(c)) and $R_{DS(ON)\_4}$=0.7288 Ω (see Figure 5-6(e)), respectively.

For the predicted online-health monitoring survival index, the remaining lifetime of the converter is shown in Figure 5-6(b)-(d)-(f), for the beginning, middle and end operating states, respectively. Since the trained ANN with the Bayesian Regularization method has less MSE compare to the other methods (see Figure 4-8), the relative graph follows the RUL index calculated by the algorithm so closely.

The calculated Mean-Square-Root-Error (MSRE) in Table 5.2 for three different training methods show the high precision prediction for the Bayesian Regularization method, which is less than 3 % in all operating states. This high-precision index is crucial for sensitive applications like downhole oil and gas, defense applications,

aerospace, etc. The precision of ANN depends on the training rate, means how many steps changes for health indicator are considered. As mentioned earlier, due to the limitation for P.C. and MATLAB computational memory, only seven-step changes for $R_{DS(ON)}$ and six-step changes for ESR_C are considered during the ANN training. Therefore, an error can be expected to be between the results of the RUL algorithm and the ANN models.

Table 5. 2 Root-Mean-Square Error (RMSE %) for three types of trained ANN in different operating states

Operating State	Levenberg–Marquardt	Bayesian Regularization	Scaled Conjugate Gradient
Beginning	3.696 %	0.5591 %	6.879 %
Middle	6.8589 %	2.853 %	12.336 %
End	5.567 %	2.649 %	14.307 %

A summary of the predicted time of operation in the future (hours) for Bayesian Regularization-ANN is given in Table 5.3. From the *T_99* index, it can be said that with 99 % of probability, the DC/DC converter will operate for another 8349.75, 6120.45, and 3349.73 hours the beginning, middle, and end operating states, respectively. A safe decision can be made for replacing or repairing the converter until the failure happens. With 50 % probability (*T_99)*, 13490.4, 10190.4, and 6007.48 hours should be considered as the remaining time of operation for the system. A high-risk decision can be made about the converter operation lifetime with the *T_01* index, which indicates 17949.6, 13549.9, and 7928.98 hours with a 1 % of probability. This column can be considered as a high-risk prediction index clarified by red color in Table 5.3.

Table 5.3 The evaluation of trained BAYESIAN-ANN for values of SiC-MOSFETS switches and capacitors

Operation State	ANN Inputs - health indicators (Ω)						BAYESIAN-ANN Outputs – Time of operation in the future (hours)									
	$R_{DS(ON)1}$	$R_{DS(ON)2}$	$R_{DS(ON)3}$	$R_{DS(ON)4}$	ESR_{C1}	ESR_{C2}	T_{99}	T_{90}	T_{80}	T_{70}	T_{60}	T_{50}	T_{40}	T_{30}	T_{20}	T_{10}	T_{01}
Beginning	0.4647	0.603	0.554	0.5018	1.2582	1.1944	8349.75	10849.83	11749.4	12289.8	12949.4	13490.4	14109.5	14549.8	15149.5	16149.3	17949.6
Middle	0.514	0.692	0.612	0.597	1.4031	1.2081	6120.45	7849.82	8749.46	9289.8	9749.4	10190.4	10409.5	10849.8	11449.3	11949.5	13549.9
End	0.678	0.705	0.668	0.7288	1.2764	1.4526	3349.73	4749.87	5184.44	5482.85	5768.41	6007.48	6227.51	6441.85	6709.53	7047.54	7928.98

CHAPTER 6.

SUMMARY AND CONTRIBUTION

With the growth in offshore oil and gas extraction, there is increased exploitation of the deep and ultra-deep reserves, which demands reliable, cost-effective technologies for improved recovery rates, especially in long-distance dispersed fields. An ISOSP (input series output series-parallel) fault-tolerant solid-state transformer (SST) to improve the power density of subsea and offshore DC distribution systems using SiC-MOSFET-based modules is proposed. Higher switching frequency helped minimize the size of passive components, especially isolation transformers. Analysis, simulation, and real-time HiL results were discussed for two scenarios – normal and faulty, and it was shown that the operation of the proposed structure is not interrupted. Fault-tolerance with redundancy in the ISOSP DC/DC converter of the MVDC distribution system was further verified through experimental results from a scaled-down laboratory prototype. A small-signal circuit was derived for the proposed configuration, and the equivalent transfer function was evaluated along with a bode plot.

In the context of MVDC power distribution architectures, the proposed conversion system can provide higher efficiency and power density in the form of a single isolated DC/DC SST as compared to a traditional 3-stage process – involving an inverter for MVDC to MVAC conversion followed by an LF transformer to step-down the voltage and then a rectifier to generate the DC link voltage needed for the drive system [10]. Further, the proposed SST configuration can be useful for MVAC systems

as well if power density is of much more concern than efficiency. For this purpose, even if MVAC transmission is used to transfer power to the subsea hubs, a 3-stage process – a converter for LF AC to MF AC, followed by an MF transformer and a rectification stage to generate DC link voltage for the drives – can still provide at least 50 % net weight reduction, though at a lower efficiency. This will particularly be very attractive for future subsea factories, especially when they will be powered by offshore wind energy, as efficiency may not be as much of a concern. Overall, it is expected that the reduction in the total size and weight of the system due to smaller converter components will allow easier installation, maintenance, and repair in future subsea/offshore operations without any significant compromises in efficiency compared to traditional approaches. A similar SST concept in a step-up operation will also be beneficial in offshore wind energy applications, primarily when MVDC or HVDC collection grids are involved.

This research introduced a power cycling, and thermal cycling accelerated lifetime experiment and a new power FET degradation test procedure using thermal equilibrium characteristics, with SiC-MOSFET power devices as DUT. The implemented hardware setup was able to degrade two DUTs simultaneously in different ambient temperatures with a precise device switching loss model using a double-pulse-test. Data acquisition with the control unit system was achieved for the post-processing of the degradation dataset. Besides, to consider the practical use of DUTs, a mission profile consisting of different current steps was applied to an H-bridge-based test setup, enabling tests on multiple DUTs simultaneously with lower input power. Due to both

conduction and switching losses, equilibrium junction temperature could be reached for different ambient temperatures, with a lower heating current than the conventional testing methods. Moreover, an improved $V_{DS(ON)}$ measurement circuit for $R_{DS(ON)}$ estimation in fast switching power FETs was also presented. Overall, the proposed approach offers a new, efficient, reliable evaluation procedure for power FETs, considering ambient temperature variations and mission profile. The experimental results proved the capability and feasibility of junction equilibrium temperature in the presence of step changes in the load current.

A statistical method to predict the probability of survival for power converters based on the measured data of component level degradation (qualification) and using machine learning is presented. An experimental hardware setup for the device degradation test and system-level RUL measurement is provided. This approach aims to estimate the probability of survival for a converter by predicting the RUL of all the system's critical power components. The main advantage of the proposed technique is that it uses real degradation data to estimate both component-level and system-level RUL indices, which results in increased precision and feasibility of the proposed approach. An Artificial Neural Network (ANN) with three different training methods is trained to predict the RUL index of the whole power electronic system. Moreover, since the machine learning-based algorithm is light in computational memory usage, it can be implemented on graphics processing units (GPUs) or FPGAs. The proposed method can gain further traction to be implemented in modern concepts, including digital twins.

A degradation circuit setup to achieve a precise measurement, considering the noise during fast switching operation of the SiC-MOSFET, is also suggested in this paper for $R_{DS(ON)}$ measurement. The lab-scale experimental hardware setup for modular DC/DC converter with 200/100 V DC conversion is implemented to perform as a system for the online health monitoring procedure. The experimental estimated and predicted probability of survival indices are provided to prove the validity, preciseness, and feasibility of the proposed measure theory-based approach for remaining useful lifetime prediction of power converters. The generality of the proposed procedure is the main advantage that can be extended and implemented on any configuration of power electronic circuits.

FUTURE WORK

The interleaving capability of the proposed fault-tolerant DC/DC converter can be simulated and validated under normal and faulty operating of the converter. The expected results are to minimize the output voltage ripple and reducing the output capacitor size since the output voltage ripple frequency would be multiple times the interleaved converters' operating frequency, depends on how many are interleaved.

The hardware setup of the proposed mission profile-based power cycle test bench of SiC-MOSFETs can be implemented. The reliability indices under different ambient temperatures can be assessed experimentally. First, the hardware setup should be appropriately designed. All measurement circuits, including $V_{DS(on)}$ and $ESR_{C,}$ should be considered, and test PCB should be built and implemented. Data monitoring and logging for health indicators (junction temperature T_j, $R_{DS(on),}$ etc.) should be carried out. The proposed algorithm and ANN will be programmed in dSPACE for online health monitoring. The proposed health-monitoring system for power converters under the new accelerated lifetime test can be presented and evaluated with experimental results. The correlation between the proposed new method with conventional degradation methods can be interpreted.

RELATED PUBLICATIONS

[1] A. R. Sadat and H. S. Krishnamoorthy, "Fault-Tolerant ISOSP Solid-State Transformer for MVDC Distribution," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2020.3032832.

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