ELECTRON TRANSPORT PROPERTIES OF LAYERED SEMICONDUCTORS AND SUPERCONDUCTORS

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In Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy

> By Guoxiong Su May 2015

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Abstract

The discovery of graphene has stimulated enormous studies of two-dimensional (2D) materials due to its unique electronic properties and its importance in potential technological applications. However, the lack of a band gap in the electronic structure of graphene also limits its possible applications. Recently, a growing interest has been focused on other layered 2D semiconductors beyond graphene, such as metal chalcogenides, providing unique opportunities beyond silicon era for the next-generation electronics, photonics, and energy applications. Besides the widely studied MoS_2 , other important metal chalcogenides include SnS_2 (with a band gap of 2.1 eV), and SnS (with a band gap of 1.1 eV), which are earth-abundant and environment-friendly materials particularly desirable for future sustainable electronic/photovoltaic applications. However, despite its technological importance, the synthesis of thin crystal arrays of such 2D semiconductors at designed locations on suitable substrates has not been realized. Here in this dissertation we focused on a novel approach to the controlled synthesis of thin crystal arrays of SnS_2 and SnS at predefined locations on the chip, by integrating a top-down process—standard nanofabrication, and a bottom-up process—chemical vapor deposition. We also have demonstrated their application as fast photodetectors with photocurrent response time $\sim 5 \ \mu s$. This opens a pathway for the large-scale production of layered 2D semiconductor devices, important for applications in integrated nano-electronic/photonic systems. Due to the remarkable changes in the electronic properties of layered semiconductors as their thickness is reduced, we have also studied the electron transport properties of a layered superconductor, β -PdBi₂. The latest experimental data from previous work show a T_C of 5.4 K for the bulk β -PdBi₂ single crystal. The temperature dependence of the specific heat suggests that β -PdBi₂ is a multiple-band/multiple-gap superconductor. However, there is no direct proof from scanning tunneling microscopy or other experiments. Here, we describe a novel experimental approach to point-contact spectroscopy for nanoplate superconductor and have employed this method to unveil the existence of two superconducting gaps in β -PdBi₂, which is important for understanding its pairing mechanism.

Contents

1	Intr	oducti	on	1
	1.1	Crysta ductor	and Electronic Band Structure of Various Layered Semicon-	4
		1.1.1	SnS_2	4
		1.1.2	SnS	4
	1.2	Crysta β -PdB	al and Electronic Band Structure of a Layered Superconductor $i_2 \ldots \ldots$	7
		1.2.1	β -PdBi ₂	7
	1.3	Outlin	e	9
2	Exp	erimer	ntal Techniques	10
	2.1	Synthe	esis	10
		2.1.1	Mechanical Exfoliation	11
		2.1.2	Chemical Vapor Deposition	11
	2.2	Device	e Fabrication	12
		2.2.1	Spin Coating	13
		2.2.2	Photolithography	14
		2.2.3	Electron-beam Lithography	15
		2.2.4	Material Deposition	15
		2.2.5	Lift-off	16
		2.2.6	Buffered Oxide Etch	16

	2.3	Materi	ials Characterization	16
		2.3.1	Optical Microscopy	17
		2.3.2	Scanning Electron Microscopy	17
		2.3.3	Energy-dispersive X-ray Spectroscopy	17
		2.3.4	Atomic Force Microscopy	18
		2.3.5	Raman Spectroscopy	18
		2.3.6	Transmission Electron Microscopy	19
		2.3.7	X-ray Photoelectron Spectroscopy	19
	2.4	Measu	rement Setup	20
		2.4.1	Cryogenic Probe Station	20
		2.4.2	Oxford Instruments ³ He Fridge	21
3	Syn	thesis	of \mathbf{SnS}_2 and \mathbf{SnS} via Chemical Vapor Deposition	22
	3.1	Introd	uction	23
	3.2	Chemi	cal Vapor Deposition	24
		3.2.1	Substrate Preparation	25
		3.2.2	CVD Setup	25
		3.2.3	Growth Results	26
		3.2.4	Growth Recipes	28
		3.2.5	Growth Mechanism	30
		3.2.6	Different Substrate Effect	31
		3.2.7	Pressure Effect	31
		3.2.8	Nucleation Sites	34
		3.2.9	Selective Growth of Hexagonal SnS_2 or Orthorhombic SnS Crystal Arrays by Varying the Sulfur Source Temperature	34
		3.2.10	The Effect of Cooling Stage on the Growth of Hexagonal SnS_2 Crystal Grains $\ldots \ldots \ldots$	38
		3.2.11	The Effect of Cooling Rate on the Growth of Hexagonal SnS_2 Crystal Grains	39

	3.3	Chara	cterization	42
		3.3.1	AFM	42
		3.3.2	Raman Spectroscopy	45
		3.3.3	SEM and EDX	46
		3.3.4	TEM	46
		3.3.5	XPS Analysis of the Nucleation Sites	50
	3.4	Concl	usion	50
4	SnS	5_2 Field	l Effect Transistors and Photodetectors	53
	4.1	Introd	luction	53
	4.2	Exper	imental Details	53
	4.3	Photo	detector Measurements	56
		4.3.1	Mechanical Chopper	56
		4.3.2	Acousto-Optic Modulator	58
		4.3.3	Photoresponsivity	63
		4.3.4	Specific Detectivity	65
		4.3.5	Quantum Efficiency	66
	4.4	Mecha	anism	66
	4.5	Concl	usion	67
5	Obs	servati	on of Multiple Superconducting Gaps in β -PdBi $_2$	69
	5.1	Introd	luction	69
		5.1.1	Andreev Reflection	69
		5.1.2	Point-contact Andreev Reflection Spectroscopy	72
		5.1.3	Layered Superconductor	75
	5.2	Exper	imental Details	76
		5.2.1	Crystal Growth and Bulk Characterization	77
		5.2.2	Device Fabrication and Characterization	78

		5.2.3	Electrical Measurement	80
	5.3	Electro	on Transport Properties	80
		5.3.1	Characterization of Critical Temperature (T_C)	80
		5.3.2	Normalized Differential Conductance	81
		5.3.3	Origin of the dI/dV Dip \ldots	83
		5.3.4	The Existence of Two SC Gaps	83
		5.3.5	Energy Gap as a Function of Temperature	86
		5.3.6	Standard Four-terminal Differential Resistance R as a Function of DC Bias Current I	88
	5.4	Conclu	nsion	88
6	Con	clusio	n and Outlook	90
\mathbf{A}	Pub	olicatio	ns, Patent and Conference Participation	92
	A.1	Public	ation	92
	A.2	Patent		93
	A.3	Confei	rence Participation	93

List of Figures

1.1	Crystal structure of SnS_2	4
1.2	Band structure of SnS_2	5
1.3	The crystallography structure of orthorhombic SnS	6
1.4	Calculated band structure of SnS	6
1.5	Crystal structure of β -PdBi ₂	7
1.6	Electronic bands for β -PdBi ₂	8
2.1	Schematic diagram of our CVD experiment setup	12
2.2	Schematic flow chart of nanofabrication process	13
3.1	Schematic diagram of experimental procedures to pattern seed arrays and use these predefined sites to seed the growth of SnS_2 crystals by CVD.	25
3.2	Schematic diagram of experimental procedure to pattern seed arrays using nanofabrication techniques described in chapter 2	26
3.3	Illustration of the CVD experimental setup with schematic sketch of synthesis mechanism involving three major steps: source material e-vaporation, reaction, and condensation on the substrate.	27
3.4	(a, b) Optical microscope images of thin SnS_2 crystal arrays with semi- hexagon shape produced by different CVD recipes (Figure 3.5)	28
3.5	(a, b) CVD recipes used to produce samples shown in Figures 3.4a and b, respectively.	29
3.6	Optical microscope image of thick SnS_2 crystal arrays on the sapphire substrate.	32

3.7	(a) Optical microscope image of SnS_2 crystal array with full-hexagonal shape; and (b) the CVD recipe used for this sample	33
3.8	Effect of different nucleation materials. Optical images of CVD growth results using cross marks (nucleation sites) of: (a) Cr (10 nm); (b) SiO ₂ (5nm)/Cr (2nm); (c) Ni (2 nm); (d) Pd (2 nm); (e) SiO ₂ (70 nm); and (f) Al ₂ O ₃ (70 nm). The substrates are: SiO ₂ (300nm)/Si for (b) and (d), and SiO ₂ (200nm)/Si for the rest. Scale bars: 100 μ m	35
3.9	Optical images of devices with (a) hexagonal SnS_2 crystal arrays and (b) orthorhombic SnS crystal arrays, after seeded CVD growth with the same recipe shown in (c) using cross marks of Pd (70 nm)/Cr (5 nm) on SiO ₂ (200nm)/Si substrates as the catalyst sites. As a control, the only difference for these two CVD experiments is a sulfur source position at 17 cm away from the furnace center for (a) and 19 cm for (b), respectively. (d) A higher magnification image for the four crystals in the upper left corner of (a). Note that one crystal appears darker in (a) when imaged with lower magnification (likely due to different illumination condition). Scale bar: 10 μ m	37
3.10	Optical images (left) of devices after seeded CVD growth with corresponding recipes (right) using cross marks of Pd $(2nm)/Cr (1nm)$ on SiO ₂ (300nm)/Si substrates as the catalyst sites. As a control, the only change in these recipes is the temperature for argon purging during the cooling stage from 680 °C to 580 °C.	40
3.11	Optical images (left) of devices after seeded CVD growth with corresponding recipes (right) using cross marks of Pd (2nm)/Cr (1nm) on SiO ₂ (300nm)/Si substrates as the catalyst sites. As a control, the only change in these recipes is the cooling rate from 660 °C to 580 °C.	41
3.12	AFM image of a semihexagonal SnS_2 crystal (scale bar: 5 μ m). Inset: a line scan showing a thickness of 20 nm	43
3.13	(a) Optical image and (b) a zoom-in AFM image of a few-layer tri- angular crystal (Inset: a line scan showing an average thickness of 3 nm)	44
3.14	Statistical distribution of SnS_2 crystal thickness for a given growth condition.	44
3.15	Raman spectra of a typical SnS_2 crystal	45

3.16	Raman scattering characterization of typical hexagonal SnS_2 crystals. (a) An optical image (Left) and Raman mapping (Right) with a 514 nm laser for a typical SnS_2 hexagonal crystal. Scale bar: 2 μ m. (b) An optical image (Left) and Raman mapping (Right) with a 633 nm laser for another SnS_2 crystal. Scale bar: 2 μ m. (c) Raman spectra of the SnS_2 crystal of (a) and the Si substrate.	47
3.17	Orthorhombic SnS crystal arrays and Raman scattering characteriza- tion. (a) An optical microscope image of SnS crystal arrays on SiO ₂ (200 nm)/Si substrate, produced by the CVD recipe described in main text. Scale bar: 100 μ m. (b) A higher magnification image for the four crystals in the upper left corner of (a). Note that one crystal ap- pears darker in (a) when imaged with lower magnification (likely due to different illumination condition). Scale bar: 10 μ m. (c) An optical image (Left) and Raman mapping (Right) with a 633 nm laser for a SnS crystal (scale bar: 1 μ m); and (d) the Raman spectra for this SnS crystal and the Si substrate	48
3.18	SEM image of a typical thick SnS_2 crystal	49
3.19	EDX analysis of the thick hexagonal SnS_2 crystal in Figure 3.18	49
3.20	TEM characterization of CVD produced thin SnS_2 crystals. (a) Bright- field TEM image of the semihexagonal SnS_2 crystals. (b) TEM selected- area-electron-diffraction (SAED) pattern of the crystal, showing single- crystal quality with hexagonal structure. Standard HRTEM image (c) and an IFFT image (d), showing defect-free hexagonal structure. Scale bar: 2 nm	51
3.21	XPS analysis on Pd/Cr and Pd seeds before the CVD growth, and Pd/Cr and Pd seeds after the CVD growth. (a)-(b) XPS data of Cr $2p_{3/2}$ peak for the Pd (2 nm)/Cr (1 nm) seeds before and after CVD growth, respectively; (c)-(d) XPS data of Pd $3d_{3/2}$ and $3d_{5/2}$ peaks for the Pd (2 nm)/Cr (1 nm) seeds before and after CVD growth, respectively; (e)-(f) XPS data of Pd $3d_{3/2}$ and $3d_{5/2}$ peaks for the Pd	
	(2 nm) seeds before and after CVD growth, respectively.	52

55	Photodetection with thin SnS_2 FET device. (a) Optical image of the FET device under study. Scale bar: 1 μ m. (b) Schematic diagram of the device configuration. (c) Drain-source current I_{DS} as a function of back-gate voltage V_G at fixed drain-source bias $V_{DS} = 2$ V for the SnS_2 photodetector in the dark state and under illumination at 4.1 μ W with a blue laser ($\lambda = 457$ nm). (d) I_{DS} vs. V_{DS} curves for the device with various illumination power (Inset: a zoom-in view of data for the dark state). Drain-source current I_{DS} recorded as a function of time with a sampling rate of 660 kHz when the laser beam was modulated periodically at a frequency ~ 800 Hz via: (e) a mechanical chopper; and (f) an acousto-optic modulator (with the laser beam only partially deflected).	4.1
57	Photoresponse of the device of Figure 4.1 with laser modulated by a mechanical chopper. (a) Drain-source current I_{DS} as a function of time when the laser beam was modulated periodically at a frequency ~ 400 Hz via a mechanical chopper; and (b) its rising edge. (c) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 800 Hz via a mechanical chopper; and (d) its rising edge	4.2
58	³ Photocurrent response for a different device with a 30 nm thick SnS_2 channel. (a) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 800 Hz via a mechanical chopper; and (b) its rising edge (Inset: optical image of the device. Scale bar: 1 μ m)	4.3
59	⁴ Photoresponse of the device of Figure 4.1 with laser modulated by an acousto-optic modulator. (a) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 400 Hz via an acousto- optic modulator; and (b) its rising edge. (c) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 800 Hz via an acousto-optic modulator; and (d) its rising edge	4.4
60	5 Time-resolved photocurrent measured with an amplifier sensitivity of 10 μ A/V (bandwidth: 3 dB attenuation at 800 kHz). (a) Drain-source current I _{DS} recorded as a function of time when the laser beam was modulated periodically at a frequency ~ 800Hz via an acousto-optic modulator; and (b) its rising edge	4.5
64	⁵ Logarithmic scale plot of photoresponsivity R as a function of incident laser power (with a blue laser: $\lambda = 457$ nm) at $V_{DS} = 2$ V and $V_G = 0$ V for the device of Figure 3; and (b) R vs. V_G at constant laser power $P = 4.1 \ \mu W$ at $V_{DS} = 2$ V	4.6

4.7	Photodetection using a SnS ₂ FET device with a 15 μ m wide source- drain gap (much larger than the focused laser spot ~ 3.6 μ m). (a) I_{DS} vs. V_{DS} curves at $V_G = 0$ V for the device with various illumination power. Inset: Optical image of the device (scale bar: 1 μ m). (b) I_{DS} vs. V_G at fixed drain-source bias $V_{DS} = 10$ V in the dark state and under illumination at 153 nW with a blue laser ($\lambda = 457$ nm)	67
4.8	Photophotocurrent response of the same SnS_2 device illuminated with a red laser ($\lambda = 633$ nm)	68
5.1	Electrical transport at an ideal (barrierless) N/S interface at $T = 0K$. Incoming electrons with $eV < \Delta$ are reflected as holes and, for each electron, a Cooper pair is transmitted (Andreev reflection). Electrons approaching the interface with $eV > \Delta$ are normally transmitted as electron-like quasiparticles	70
5.2	Normalized conductance curves of an N–S junction with $\Delta = 2.66 \text{ meV}$ at $T = 0.24$ K calculated by numerical simulation of the BTK model at different values of the barrier strength Z, from pure Andreev $(Z = 0)$ to pure tunneling $(Z = 10)$ regimes.	71
5.3	(a) Experimental arrangement for point-contact measurements with the typical needle-anvil technique. A metallic tip (Au, Pt-Ir, Pt, Ag) is gently pressed against the surface of the sample. (b) The "soft" point-contact technique where a tiny spot of Ag paste (or a tiny flake of In) replaces the tip	73
5.4	(a) Schematic diagram of a superconductor microcrystal lying on top of three normal metal electrodes and a circuit designed for obtaining Andreev reflection spectra for the target N–S junction between the $I_+(V_+)$ electrode and the superconductor. (b) Optical microscope image of a device with a suspended microcrystal of Fe _{1+y} Te _{1-x} Se _x bridging six parallel metal electrodes (35 nm Pd/5 nm Cr) spaced ~ 500 nm apart. The four center electrodes (labeled as 2-5) are designed to be 1 μ m wide while the two outside electrodes (labeled as 1 and 6) are 4 μ m wide.	74
5.5	Schematic diagram of a superconductor nanoplate patterned with three normal metal electrodes and a circuit designed for obtaining AR spec- tra for the target N–S junction between the $I_+(V_+)$ electrode and the	75
	superconductor	61

(a) (001) XRD pattern of β -PdBi ₂ bulk crystal with preferred orienta- tion along c axis; the inset shows a SEM image of one representative crystal. (b) Resistivity of β -PdBi ₂ bulk crystal from 2 to 300 K; the inset presents resistivity data between 4 and 6 K. (Unpublished results from Dr. Paul Chu's group at TcSUH.)	78
Optical and AFM image of β -PdBi ₂ device. (a) Optical microscope image of a device with a mechanically exfoliated β -PdBi ₂ nanoplate patterned with eight 4- μ m wide metal electrodes (50 nm Pd/5 nm Cr) spaced 4 μ m apart. (Scale: 10 μ m.) (b) AFM image of the device	79
R as a function of temperature T at zero bias current for the micro- crystal of Figure 5.7.	81
Normalized differential conductance dI/dV (black square) versus bias voltage V at temperature $T = 0.24$ K and magnetic field $B = 0$ T for the N–S junction between electrode 18 and the superconductor, and a fitting (red solid line) to the data by the BTK theory (see section 5.3.4.)	82
(a) Raw data of differential conductance dI/dV versus V measured at different temperature under $B = 0$ T. For clarity, the curves are vertically shifted down by an amount of 1.5 mS degressively from top to bottom, starting from the data for $T = 0.96$ K. (b) Raw data of dI/dV versus V measured under different magnetic field at temperature T = 0.24 K. For clarity, the curves are vertically shifted down by an amount of 1 mS degressively from top to bottom, starting from the data for $B = 0.025$ T	84
Standard four-terminal resistance R (left axis) and measured differen- tial conductance dI/dV (right axis) as a function of DC bias current I (a) at $T = 4$ K and under $B = 0$ T and (b) at $T = 0.24$ K and under $B = 0.4$ T. Same I_+ and I terminals were used to keep the electric field distribution identical for both measurements.)	85
Energy gaps as a function of temperature $(\Delta_L(T), \text{ black diamonds}; \Delta_S(T), \text{ red diamonds})$ determined from the fitting of BTK theory. The solid lines represent BCS predictions.	87
Standard four-terminal differential resistance of the superconductor nanoplate measured by a standard four-terminal configuration (a) at various temperature with $B = 0$ T and (b) under various magnetic field at temperature $T = 0.24$ K	89
	(a) (001) XRD pattern of β -PdBi ₂ bulk crystal with preferred orientation along c axis; the inset shows a SEM image of one representative crystal. (b) Resistivity of β -PdBi ₂ bulk crystal from 2 to 300 K; the inset presents resistivity data between 4 and 6 K. (Unpublished results from Dr. Paul Chu's group at TcSUH.) Optical and AFM image of β -PdBi ₂ device. (a) Optical microscope image of a device with a mechanically exfoliated β -PdBi ₂ nanoplate patterned with eight 4- μ m wide metal electrodes (50 nm Pd/5 nm Cr) spaced 4 μ m apart. (Scale: 10 μ m.) (b) AFM image of the device R as a function of temperature T at zero bias current for the microcrystal of Figure 5.7

List of Tables

2.1	Spin Coating Parameters	14
4.1	Comparison of Key Device Performance Figures-of-Merit for Photode-	
	tectors Based on 2D Layered Materials	62

Chapter 1

Introduction

The discovery of graphene [1] has stimulated vigorous investigation of two-dimensional (2D) materials [2] due to its unique electronic properties and its importance in potential technological applications [3–5]. However, the lack of a band gap in the electronic structure of graphene also limits its possible applications. [6, 7] Recently, a growing interest has been focused on other layered 2D semiconductors beyond graphene. [8–10] In particular, metal dichalcogenides, with finite band gaps have been emerging as potential building blocks for next-generation electronic/photonic applications. Metal dichalcogenides materials are represented by a generalized formula of MX_2 , where M is a metal and X is a chalcogen. Representative metal chalcogenides, including the widely studied MoS_2 , possess similar layered crystal structures with weak interaction between adjacent layers, thus allowing the formation of stable thin-layer crystals with thickness down to a few or even a single atomic layer. Other important chalcogenides, involving earth-abundant and environment-friendly materials desirable for sustainable applications, include SnS_2 (band gap: 2.1 eV) [11–13] and SnS (band gap: 1.1 eV)

[14].

So far, commonly adopted for research purpose are mechanical [11] and liquid exfoliation [15] methods for creating thin layers of such 2D semiconductors. Recently, chemical vapor deposition (CVD) has been emerging as an attractive method for producing thin films [16–20] or randomly nucleated crystal grains of MoS_2 [21–24]. However, critically needed is a generally effective method for pinning down the positions of thin crystal grains of layered 2D semiconductors at predefined locations on substrates, which is important for integrated nanoelectronic/photonic system applications. For SnS_2 and SnS, there has been even no report of CVD synthesis of thin crystal grains. Here we propose a general strategy for the controlled CVD synthesis of thin crystal arrays of layered semiconductors at predefined locations on chip and have demonstrated for the first time the successful seeded growth of arrays of thin SnS_2 and SnS crystal grains on SiO_2/Si substrates, promising large-scale optoelectronic and photovoltaic applications. This achievement is enabled by two key ideas: the engineering of nucleation sites by standard nanofabrication, and the seeded growth of SnS_2 and SnS crystals by CVD on predefined nucleation sites.

Here we demonstrate such CVD-grown high quality SnS_2 crystalline layers as high speed photodetectors as high speed photodetectors with fast response time ~ 5 μ s, best among photodetectors based on other 2D materials with reported response time ranging from 70 μ s to a few seconds. [25–35] Our work demonstrates the significant potential of CVD synthesized SnS_2 thin crystals for integrated optoelectronics applications. Such earth-abundant and environmentally friendly tin-based chalcogenides are particularly desirable for sustainable green optoelectronics applications.

Recently, layered superconductors have attracted a lot to attention due to the low-dimensionality of their electronic states. Most of superconductors with the highest transition temperature are layered materials. Most recently, attention was paid to Bi-based and Bi-containing superconductors, such as $Bi_2Sr_2Ca_2Cu_3O_x$, whose T_C is higher than 110 K. The latest experimental data from Imai et al. show a T_C of 5.4 K for the bulk β -PdBi₂ single crystal. [36] The temperature dependence of the specific heat suggests that β -PdBi₂ is a multiple-band/multiple-gap superconductor. The electronic band structure and Fermi surface of the β -PdBi₂ by first-principles calculations suggest a complicated superconducting gap structure for this materi-[37] The presence of multiple Fermi surfaces suggests that β -PdBi₂ should be al. a multiple-band/multiple-gap superconductor, as was indicated in Imai et al.'s experiment. However, there is no direct proof from scanning tunneling microscopy or other experiments. Here, we describe a novel experimental approach to point-contact spectroscopy for nanoplate superconductor and have employed this method to unveil the existence of two superconducting gaps in β -PdBi₂ which is important for understanding its pairing mechanism.

This chapter is organized as follows. Section 1.1 discusses the crystal and electronic band structure of various layered semiconductors. Section 1.2 presents the crystal and electronic band structure of layered superconductor β -PdBi₂. Section 1.3 describes the outline of this dissertation.

1.1 Crystal and Electronic Band Structure of Various Layered Semiconductors

1.1.1 SnS_2

Tin disulfide is a layered semiconductor with a hexagonal CdI_2 type crystal structure as shown in Figure 1.1. The three dimensional crystal consists of S-Sn-S trilayers which are covalently bonded within the trilayer but each trilayer is weakly coupled to the nearest trilayers by van der Waals force. Figure 1.2 presents the energy band structure of SnS_2 calculated by Fong et al. [38]



Figure 1.1: Crystal structure of SnS_2 . (Adapted from [11])

1.1.2 SnS

Tin monosulfide crystallizes in an orthorhombic structure as shown in Figure 1.3. It is composed of double SnS layers with tin and sulfur atoms covalently bonded within the layers and weak van der Waals interaction between the double layers. [39] Figure



Figure 1.2: Band structure of SnS_2 . (Adapted from [38])

1.4 shows the calculated band structure of SnS [14].



Figure 1.3: The crystallography structure of orthorhombic SnS.



Figure 1.4: Calculated band structure of SnS. (Adapted from [14])

1.2 Crystal and Electronic Band Structure of a Layered Superconductor β -PdBi₂

1.2.1 β -PdBi₂

 β -PdBi₂ tetragonal structure is shown in Figure 1.5. It is composed with triple Bi-Pd-Bi layers with Pd and Bi atoms covalently boned within layers and weak van der Waals force between each layer. Figure 1.6 presents the electronic bands for β -PdBi₂.



Figure 1.5: Crystal structure of β -PdBi₂.



Figure 1.6: Electronic bands for β -PdBi₂. (Adapted from [37])

1.3 Outline

This dissertation consists of six chapters. Following the current introductory chapter, the details of the experimental techniques employed in material synthesis, device fabrication and electrical measurement are given in chapter 2. In chapter 3, the synthesis of SnS₂ and SnS via CVD is discussed. Devices fabricated based on such SnS₂ nanocrystal and their characterization are reported in chapter 4. Electrical characterization of β -PdBi₂ nanoplate is described in chapter 5. To conclude, chapter 6 gives a summary of the progress made by this dissertation work and highlights its potential impact in the relevant field of research.

Chapter 2

Experimental Techniques

This chapter shows the experimental techniques used to obtain the materials, fabricate the devices and characterize the samples. A significant part of the fabrication process was carried out in a cleanroom, using advanced nanofabrication techniques. This chapter consists of four sections including: synthesis, device fabrication, material characterization, and electronic measurement. Each section presents the corresponding techniques in details with the description of the instrument used.

2.1 Synthesis

Tin monosulfide, tin disulfide nanoplates were synthesized using chemical vapor deposition (CVD) method. β -PdBi₂ was synthesized in bulk form and then mechanically exfoliated into thin nanocrystals using a scotch tape method.

2.1.1 Mechanical Exfoliation

Mechanical exfoliation allows us to produce the cleanest, high-quality and micrometersized atomically thin nanosheets of layered materials. In a typical mechanical exfoliation process, thin crystals are first peeled off from their bulk crystals by using a scotch tape method. These freshly exfoliated thin crystals on the scotch tape are adhered to a target substrate and then rubbed by a chopstick-like tool. After removing the scotch tape, single layer and multilayer nano plates are obtained on the substrate due to the weak interlayer van der Waals forces in these layered materials.

Some of the materials under study were first synthesized in bulk form via vapor transport method. These mechanically exfoliated nanosheets were identified under the optical microscope and further measured by atomic force microscopy.

2.1.2 Chemical Vapor Deposition

It is well known that mechanical exfoliation is the most efficient way to obtain highly crystalline atomically thin 2D layered nanosheets. However, it is not suitable for large-scale production because of the lack of thickness controllability. Recently, CVD was attracting significant attention as a practical method for producing thin films or crystal grains of metal dichalcogenides. In a typical CVD process, one or more volatile precursors, such as S and MoO_3 , react and/or decompose on the substrate to produce the desired deposit.

The CVD system setup generally includes a single/multiple-zone furnace, a quartz tube, and a gas flow control system. Depends on operating pressure, CVD is classified as the following: atmospheric pressure CVD (APCVD), low-pressure CVD (LPCVD), and ultrahigh vacuum CVD (UHVCVD). In this work, thin crystals of layered semiconductors SnS_2 and SnS are obtained with APCVD and LPCVD. Figure 2.1 shows a schematic diagram of our CVD experiment setup.



Figure 2.1: Schematic diagram of our CVD experiment setup.

2.2 Device Fabrication

As shown in Figure 2.2, the whole device fabrication process includes spin coating, exposure, development, material deposition, and lift-off. The thin nanocrystals obtained from the CVD or the mechanical exfoliations were identified under an optical microscope. The optical images were used to design electrodes on top of the nanocrystals with computer-aided design (CAD) software, such as DesignCAD and AutoCAD. Then the sample was taken to the cleanroom for pattern making. First the photoresist or electron-beam (e-beam) lithography resist, typically MICROPOSIT[®] S1818 or Poly(methyl methacrylate) (PMMA), is spin-coated onto the target substrate and

then soft baked on a hot plate or in an oven for the resist solidifying. Photolithography and e-beam lithography are used to fabricate a three-dimensional binary structure on top of the target substrate.



Figure 2.2: Schematic flow chart of nanofabrication process.

2.2.1 Spin Coating

Spin coating is a procedure to deposit uniform thin films of photoresist or e-beam lithography resist onto the target substrate. The substrate is covered 3/4 with the resist and then spun at high speed for 30 to 60 seconds to produce a thin film. The thickness of the film depends on the angular speed of spin coater as well as the viscosity and concentration of the resist. A Brewer Science[®] Cee[®] 200X spin coater is used in the University of Houston (UH) Nanofabrication Facility. The spin coating parameters for both S1818 and PMMA are listed in Table 2.1.

Resist	Spinning speed (rpm)	Thickness (nm)
S1818	3000	2000
PMMA A4	3000	200

Table 2.1: Spin Coating Parameters

2.2.2 Photolithography

Photolithography is a widely used process that uses optical radiation to transfer a geometric pattern from a photomask to the resist on the substrate. The advantages of photolithography are low cost and fast operation. Also, photolithography is capable to produce the patterns on the entire wafer at once.

First, the substrate is spin coated with a light-sensitive chemical, i.e. photoresist. There are two types of photoresist: positive and negative. A positive photoresist becomes soluble in the developer when exposed; with a negative photoresist, unexposed regions are soluble in the developer. In this work, we used a positive photoresist, Shipley MICROPOSIT[®] S1818, and the developer for it is Shipley MICROPOSIT[®] MF-319. A quartz photomask with opaque chromium patterns was applied to selectively expose the photoresist. Then the substrate is submerged in the developer, MF-319, for 40 seconds. This produces a three-dimensional binary structure of the photoresist on the substrate. The ABM mask aligner is used for photolithography in the Nanofabrication Facility at UH.

2.2.3 Electron-beam Lithography

The highest resolution of the ABM mask aligner is 1 μ m. In order to produce patterns with nanometer-sized features, electron-beam lithography (e-beam lithography) is used. E-beam lithography is the practice of scanning a focused beam of electron with high energy to draw custom patterns on a surface coated with an electron-sensitive resist, such as PMMA. PMMA was spin coated and then baked on a hot plate at 180 $^{\circ}C$ for 20 minutes. Unlike photolithography, no mask is used in e-beam lithography. The patterns are designed using CAD software, such as DesignCAD and AutoCAD. The electron beam changes the solubility of PMMA, enabling selective removal of the exposed region of PMMA by developing in Methyl isobutyle ketone (MIBK). FEI XL-30FEG scanning electron microscope (SEM) equipped with JCNabity Nanometer Pattern Generation System (NPGS) is used for e-beam lithography in UH Nanofabrication Facility.

2.2.4 Material Deposition

Electron beam physical vapor deposition (EBPVD) is a method of depositing a thin film with high precision thickness. The material to be deposited is heated to a high vapor pressure by electron bombardment in a high vacuum. The gas phase material is transported by diffusion and then deposited on the cooler workpiece with the substrate. The deposition rate is measured by a piezoelectric crystal monitor. In this work, materials deposited using this system are listed as following: chromium (Cr), palladium (Pd), nickel (Ni), aluminum oxide (Al₂O₃), and silicon dioxide (SiO₂).

2.2.5 Lift-off

Lift-off process is a step to remove the resist mask and excess material on top of it, leaving the desired pattern on the substrate. In this work, acetone is used as the solvent to remove the resist, S1818 and PMMA.

2.2.6 Buffered Oxide Etch

Buffered oxide etch (BOE), is a wet etchant used in nanofabrication to etch thin films of silicon dioxide (SiO₂) or silicon nitride (Si₃N₄). It is a mixture of hydrofluoric acid (HF), ammonium fluoride (NH₄F) and deionized (DI) water. A common buffered oxide etch solution comprises a 6:1 volume ratio of 40% NH₄F in water to 49% HF in water. The silicon wafer covered with 300 nm SiO₂ thin films was exposed to 6:1 BOE for 4 minutes to etch the oxide away. The chemical reaction is:

$$SiO_2 + 4 HF = SiF_4 + 2 H_2O$$

This procedure was used to gain electrical access to the silicon substrate which was used as a back-gate to study the electric field effect.

2.3 Materials Characterization

The materials characterization techniques used in this work include optical microscopy, scanning electron microscopy (SEM), atomic force microscopy (AFM) and Raman scattering experiment.

2.3.1 Optical Microscopy

For SnS_2 and SnS crystals synthesized via CVD, optical images of the substrates are taken and named in terms of the distance away from the center of the furnace for each growth. For β -PdBi₂ nanocrystals obtained by mechanically exfoliation, optical images of materials are taken using an optical microscope (Omano OMM200T Trinocular Metallurgical Microscope) for pattern design. The optical images of fabricated devices are taken for further measurement. The thickness of the materials is determined by the color of the images.

2.3.2 Scanning Electron Microscopy

A scanning electron microscope (SEM) is a microscope that uses electrons instead of light to form an image. It is a useful tool for imaging beyond the optical diffraction limit. SEM can achieve resolution better than 1 nm. It shows the topography of the sample.

2.3.3 Energy-dispersive X-ray Spectroscopy

Energy-dispersive X-ray spectroscopy (EDX) is an analytical technique used for the elemental analysis or chemical characterization of a sample due to the interaction between X-ray and the sample. In this work, EDX is employed to reveal the elemental composition of CVD synthesised nanocrystals.

2.3.4 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is an indirect imaging technique which is competent to provide the three-dimensional topographical information of a sample by measuring the force between the sample and a probe. AFM imaging is carried out in tapping mode, and the height information is used to determine the thickness of studied devices.

2.3.5 Raman Spectroscopy

Raman spectroscopy is a spectroscopic technique used to observe vibrational, rotational, and other low-frequency modes in a system. It is commonly used to identify the synthesized material, provide its crystal structure and the number of layers in fewlayer metal dichalcogenides. In this work, SnS₂ and SnS nanocrystals are identified using Raman spectroscopy.

As previously mentioned in the acknowledgement section, all the Raman spectroscopy experiments and analysis were performed in collaboration with Dr. Viktor Hadjiev from Department of Mechanical Engineering and the Texas Center for Superconductivity at the University of Houston (TcSUH). Raman scattering were performed using a T64000 Horiba JY Raman microscope equipped with Ar⁺ and HeNe lasers set to operate at 514 nm and 633 nm, respectively. A short-working distance objective with magnification $100 \times$ was used to focus the laser beam to a spot with diameter 1.2 μm (633 nm laser) or 0.7 μm (514 nm laser). The corresponding depth of focus of the objective was 1.1 μm (633 nm) or 0.4 μm (514 nm). Raman mapping involved a raster scan of the focused beam over a two-dimensional area on the sample at step size 0.5 μm . The Raman images were produced by deconvolution of Raman spectra recorded at each step into the spectra of constituent compounds coded with different colors. Brighter colors correspond to higher Raman intensities.

2.3.6 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is a microscopy technique where an electron beam is transmitted through an ultra-thin specimen, interacting with the specimen as it passes through. After passing through the specimen, transmitted electrons are collected and focused by the objective lens and a magnified real image of the specimen is obtained by an electronic imaging devices such as a charge-coupled device (CCD) camera.

TEM is capable to provide significantly higher resolution images than optical microscopy due to the small de Broglie wavelength of electrons. In this work, TEM is performed to show the quality of thin SnS_2 crystals grown by CVD.

2.3.7 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis (ESCA), is the most widely used surface analysis technique due to its relative simplicity in use and data interpretation. It can be applied to a wide range of materials and provides the elemental composition, empirical formula, chemical state and electronic state of the elements information from the surface of the measured material. XPS spectra are obtained by exciting a material with a beam of X-rays while
simultaneously measuring the kinetic energy and number of emitted photoelectrons. In this work, XPS experiments were performed on Pd and Pd/Cr nucleation sites before and after CVD growth.

2.4 Measurement Setup

After the devices are prepared as described in section 2.2, they are ready for electrical measurements. Electrical measurements were performed in a Lake Shore TTP6 cryogenic probe station with the temperature range from 77 K to room temperature (295 K). The low temperature (< 77 K) measurements are carried out in an Oxford Instruments Heliox VL top loading variable temperature fridge.

2.4.1 Cryogenic Probe Station

Lake Shore TTP6 is a cryogenic micro-manipulated probe station configured with six probe arms and an optical system. The base pressure is $\sim 10^{-5}$ Torr at 295 K and $\sim 10^{-6}$ Torr at 77 K. The sample is mounted on a metallic base called cold head and the temperature is controlled with a heater and a continuous flow refrigeration system using liquid nitrogen. The probe tips making the electrical connections are also thermally linked to the cold head to minimize the heat transfer to the sample.

2.4.2 Oxford Instruments ³He Fridge

Oxford Instruments helium-3 (³He) fridge is capable of reaching a base temperature of ~ 0.24 K and magnetic fields up to 17 T. The introduction and operation details are described in Dr. Debtanu De's dissertation. [40]

Chapter 3

Synthesis of SnS₂ and SnS via Chemical Vapor Deposition

This chapter is based on our previously published papers [41, 42]:

1. Novel layered two-dimensional semiconductors as the building blocks for nanoelectronic/photonic systems. G. Su, D. De, V. Hadjiev, and H. Peng, Proc. SPIE 9083, 908304 (2014).

 Chemical Vapor Deposition of Thin Crystals of Layered Semiconductor SnS₂ for Fast Photodetection Application. G. Su, V. Hadjiev, P. Loya, J. Zhang, S. Lei, S. Maharjan, P. Dong, P. Ajayan, J. Lou, and H. Peng, Nano Letters 15, 506 (2015).

3.1 Introduction

Layered two-dimensional (2D) semiconductors such as metal chalcogenides provide unique opportunities beyond silicon era for the next-generation electronics, photonics, and energy applications. Besides the widely studied MoS_2 , other important chalcogenides include SnS_2 (with a band gap of 2.1 eV), and SnS (with a band gap of 1.1 eV), which are earth-abundant and environment-friendly materials particularly desirable for future sustainable electronic/photovoltaic applications. However, despite its technological importance, the synthesis of thin crystal arrays of such 2D semiconductors at designed locations on suitable substrates has not been realized. Here we report a novel approach to the controlled synthesis of thin crystal arrays of SnS_2 and SnS at predefined locations on the chip, by integrating a top-down process—standard nanofabrication, and a bottom-up process—chemical vapor deposition. This general approach can also be applied to achieve the large-scale production of other layered 2D semiconductors, opening a pathway for their future applications in integrated nanoelectronic/photonic systems. Many metal chalcogenides have common crystal structures consisting of stacked layers which interact via weak van der Waals force between adjacent layers, allowing the formation of stable thin crystals with thickness down to single atomic layer. Mechanical and liquid exfoliation are typically adopted to prepare thin slabs of such 2D semiconductors. Recently, chemical vapor deposition (CVD) has been emerging as an attractive method for producing thin films or randomly-nucleated crystal grains of MoS₂. However, critically needed is a generally effective method for pinning down the positions of thin crystal grains of layered 2D semiconductors at predefined locations on substrates, which is important for integrated nano-electronic/photonic system applications. For SnS_2 and SnS, there has been even no report of CVD synthesis of thin crystal grains. Here we propose a general strategy for the controlled CVD synthesis of thin crystal arrays of layered semiconductors at predefined locations on chip and have demonstrated for the first time the successful seeded growth of arrays of thin SnS_2 and SnS crystal grains on SiO_2/Si substrates, promising large-scale optoelectronic and photovoltaic applications. This achievement is enabled by two key ideas: the engineering of nucleation sites by standard nanofabrication, and the seeded growth of SnS_2 and SnS crystals by CVD on predefined nucleation sites.

3.2 Chemical Vapor Deposition

In order to achieve the controlled CVD synthesis of thin SnS_2 crystal arrays at predefined locations on the chip, we employed two key experimental strategies: (1) engineering nucleation sites by top-down nanofabrication process; and (2) seeded growth of SnS_2 crystals by bottom-up CVD process on predefined nucleation sites. As shown in Figure 3.1, this illustrates a general effective method for pinning down the positions of thin crystal grains of layered 2D semiconductors at predefined locations on substrates, which is promising for integrated nano-electronic/photonic system applications.



Figure 3.1: Schematic diagram of experimental procedures to pattern seed arrays and use these predefined sites to seed the growth of SnS_2 crystals by CVD.

3.2.1 Substrate Preparation

In experiments, we first pattern nucleation sites on SiO_2/Si substrates (300 nm SiO_2 , from silicon quest international) by nanofabrication techniques described in chapter 2, e.g., cross marks shown in Figure 3.2 with lateral dimension of micrometers. Typical nucleation sites are thin-film pads made of Pd/Cr, Cr, SiO_2/Cr , or Ni (~ nm thick), which are found to serve as effective seeds for CVD growth of thin SnS_2 crystals. Different nucleation sites are discussed in section 3.2.7. A different substrate, c-plane sapphire (University Wafer), has also been tested.

3.2.2 CVD Setup

We use a thermal-CVD method (Figure 3.3) for the growth of SnS_2 and SnS crystals at the predefined nucleation sites on SiO_2/Si substrates. In the CVD setup (Figure 3.3), sulfur source (S powder), tin source (either Sn or SnO_2 powder), and substrate



Figure 3.2: Schematic diagram of experimental procedure to pattern seed arrays using nanofabrication techniques described in chapter 2.

are placed at different positions (thus different temperatures) in a furnace heated under argon gas follow (typically 60 sccm) in low vacuum (typically 30 kPa) or under atmospheric pressure. In a typical recipe, in low vacuum, the center zone of the furnace is first heated to 710 °C, and then maintained for some time (5 to 40 minutes) in the growth stage before cooled down to room temperature. It is worthwhile to note that the substrate is placed at a position away from the center zone, since the nucleation of thin SnS₂ crystals occurs mostly in a substrate temperature range of 580 °C to 670 °C while there is nearly no crystal growth at the zone center. By varying the CVD processing recipes, the amount of source materials, their temperatures and pressure of the system, we have achieved the selective synthesis of either SnS₂ or SnS crystal arrays directly on insulating substrate SiO₂/Si.

3.2.3 Growth Results

Figure 3.4a presents an optical microscope image of arrays of SnS_2 crystals on SiO_2/Si , produced by CVD using lithographically patterned seed pads of Pd (1 nm thick)/Cr



Figure 3.3: Illustration of the CVD experimental setup with schematic sketch of synthesis mechanism involving three major steps: source material evaporation, reaction, and condensation on the substrate.

(0.5 nm thick) as nucleation sites. For this growth, the center zone of the furnace was first heated to 710 °C under an argon flow of 60 sccm in a vacuum of 30 kPa (with 0.05 g SnO₂ positioned at 710 °C, 2.3 g S at 115 °C, and the substrate at 640 °C), and then maintained for 40 minutes in the growth stage before cooled down to room temperature. It is obvious that thin semi-hexagon SnS₂ crystals nucleated at the seed sites (cross marks). When we modified the CVD recipe by increasing the SnO₂ material to 0.2 g and placing the S source at a higher temperature of 225 °C, the result (Figure 3.4b) shows apparent seeded-growth of thin crystals on the predefined sites with a yield of almost 100 %, demonstrating the effectiveness of patterned Pd/Cr as the nucleation sites.



Figure 3.4: (a, b) Optical microscope images of thin SnS_2 crystal arrays with semihexagon shape produced by different CVD recipes (Figure 3.5).

3.2.4 Growth Recipes

Figure 3.5a and b presents the CVD recipes for the samples shown in Figures 3.4a and b, respectively. In Figure 3.5a, we show the recipe for the growth of semi-hexagon SnS_2 array of Figure 3.4a: the center zone of the furnace was first heated to 710 °C under an argon flow of 60 sccm in a vacuum of 30 kPa (with 0.05 g SnO_2 powder positioned at 710 °C, 2.3 g sulfur powder at 115 °C, and a target SiO_2/Si substrate at 640 °C), and then maintained for 40 minutes in the growth stage before cooled down to room temperature. The growth recipe of semi-hexagon SnS_2 array of Figure 3.4b is shown in Figure 3.5b, which is similar to that of Figure 3.5a, except that: SnO_2 material was increased to 0.2 g, the S source (2.3 g) was placed at a high temperature of 225 °C, and the growth stage at 710 °C was reduced to 10 minutes.



Figure 3.5: (a, b) CVD recipes used to produce samples shown in Figures 3.4a and b, respectively.

3.2.5 Growth Mechanism

This supports the scenario of growth mechanism shown in Figure 3.3: vapors of the source materials (Sn and S) are first generated via sublimation, then react at elevated temperatures (~ 710 °C) to form gaseous Sn–S species (e.g., SnS₂ clusters), and finally these gaseous species are transported downstream and condensed as thin SnS₂ crystals at the predefined nucleation sites on the substrate. It is impressive that there is nearly no crystal on the bare SiO₂ substrate away from the predefined nucleation sites, which implies that diffusion of SnS₂ clusters on substrate likely cause them to end at those energetically favorable seed sites. The lateral dimension of typical semi-hexagon SnS₂ crystals is 20–50 μ m. By varying the growth time and the amount of source materials, we have achieved SnS₂ crystals with thickness from 3 to 80 nm (i.e., ~ 5 to 136 layers considering a monolayer thickness of 0.59 nm), as revealed by AFM images. We note that the exact control of the layer numbers of SnS₂ crystals is not realized in our CVD methods, although there is a statistical distribution of the crystal thickness for growth under a given condition (see Section 3.3.1).

The novelty of our CVD approach (Figure 3.1) lies in the use of patterned nucleation sites to seed the growth of thin SnS_2 crystal arrays on insulating substrates, which is different from existing approaches such as mask patterning method [43, 44] or lithography method [45–48]. The growth mechanism in our CVD approach is consistent with the scenario shown in Figure 3.3. In general, the nucleation of SnS_2 crystals on predefined sites can be facilitated from two different mechanisms: (1) the aggregation of gaseous-phase SnS_2 clusters on a general defect site to form thin crystals; or (2) the chemical binding of gaseous-phase SnS_2 clusters to specific nucleation

sites (e.g., Pd/Cr pads).

3.2.6 Different Substrate Effect

We note that for CVD growth on bare SiO₂/Si substrates without nucleation sites, the yield of SnS₂ or SnS crystals is low and their positions are random and uncontrollable. We also tested the CVD growth on a different substrate, c-plane (0001) sapphire wafer. Figure 3.6 shows the optical microscope image of thick SnS₂ crystal arrays on the sapphire substrate with the same growth recipe as that of Figure 3.4b. The yield of SnS₂ crystals are much higher than that in Figure 3.4b. There are multiple SnS₂ crystals on the same nucleation sites. In addition, a lot of SnS₂ crystals are observed on the bare sapphire substrate, which are barely seen for bare SiO₂/Si substrate as shown in Figures 3.4a and b. This might be explained by the surface orientation of c-plane sapphire single crystal.

3.2.7 Pressure Effect

It is worth noting that by performing CVD growth under vacuum (~ 30 kPa), we usually obtain thin crystals (Figures 3.4a and b) showing a shape of semi-hexagon with clear crystal edges. However, if the CVD growth is performed under atmospheric pressure with larger amount of Sn source material, we can also produce thick SnS_2 crystals with a full-hexagonal shape (Figure 3.7a, reflecting the natural crystal shape of bulk SnS_2 [11]), which may be related to a higher growth rate under more precursor vapor supply. The thickness ranges from a few hundreds nanometer to micrometer



Figure 3.6: Optical microscope image of thick SnS_2 crystal arrays on the sapphire substrate.

thick. A CVD recipe for producing full-hexagonal crystal arrays is shown in Figure 3.7b as follows: (1) the center zone of the furnace was first heated from 20 °C to 705 °C in 10 min under an argon flow of 60 sccm at atmospheric pressure (with 0.5 g Sn powder positioned at 705 °C, 1.15 g sulfur powder at 213 °C, and a target SiO₂/Si substrate at 705 °C) (at the center); (2) the argon flow was then stopped and the temperature was retained at 705 °C for 5 minutes before decreased to 580 °C in 30 minutes; and (3) the system was purged with an argon flow of 500 sccm and cooled down naturally from 580 °C to room temperature in ~ 2 hours.



Figure 3.7: (a) Optical microscope image of SnS_2 crystal array with full-hexagonal shape; and (b) the CVD recipe used for this sample.

3.2.8 Nucleation Sites

Our further experimental test by using different nucleation materials suggests that the chemical binding to specific nucleation materials is the key mechanism for the nucleation of SnS_2 crystals. As shown in Figure 3.8a, b, and c, we have discovered that Cr, Ni, or Cr with a cap layer on top (e.g., Pd/Cr and SiO₂/Cr) serves as an effective seed. But Pd, SiO₂, and Al₂O₃ do not function as a seed to nucleate SnS_2 crystals (Figures 3.8e and f). Interestingly, SiO₂ and Al₂O₃ tend to repel the nucleation of SnS_2 crystals since crystals are usually away from the cross marks (Figures 3.8e and f). However, it is important to note that SiO₂/Cr works well as a seed for CVD (Figure 3.8b), promising future integrated electronic applications since SiO₂ is insulating.

3.2.9 Selective Growth of Hexagonal SnS₂ or Orthorhombic SnS Crystal Arrays by Varying the Sulfur Source Temperature

Importantly, for the CVD growth performed under atmospheric pressure, when the tin source material is increased significantly to ~ 5.7 g, either orthorhombic SnS or hexagonal SnS₂ crystal arrays can be selectively synthesized by modifying the sulfur source position (thus its temperature). Figure 3.9 illustrates the effect of the sulfur source temperature on the selective growth of either hexagonal SnS₂ crystal arrays or orthorhombic SnS crystal arrays, when the tin source material is sufficient. Note that we used a tin source of 5.69 g in the growth of Figure 3.9. In these two control experiments, all other conditions are the same, except that the sulfur source was



Figure 3.8: Effect of different nucleation materials. Optical images of CVD growth results using cross marks (nucleation sites) of: (a) Cr (10 nm); (b) SiO₂ (5nm)/Cr (2nm); (c) Ni (2 nm); (d) Pd (2 nm); (e) SiO₂ (70 nm); and (f) Al₂O₃ (70 nm). The substrates are: SiO₂ (300nm)/Si for (b) and (d), and SiO₂ (200nm)/Si for the rest. Scale bars: 100 μ m.

positioned at 17 cm away from the furnace center for the growth of hexagonal SnS_2 crystal arrays (Figure 3.9a) and at 19 cm away for orthorhombic SnS crystal arrays (Figure 3.9b), respectively. When the temperature of the furnace center is 690 °C, the sulfur source temperature is calibrated to be 209 °C and 100 °C for the processing of Figures 3.9a and b, respectively. This indicates that for sufficient tin source material in the CVD growth, holding the sulfur source slightly below its melting point leads to the growth of SnS crystal arrays. This is reasonable since the melting point of sulfur is 115.2 °C and lowering its source temperature to 100 °C reduces the amount of sulfur vapors available for the crystal synthesis, thus leading to a SnS phase instead of SnS₂.

Figures 3.9b and d show arrays of orthorhombic SnS crystals produced by using Pd/Cr as seed. For growth of typical orthorhombic SnS crystal arrays such as that of Figure 3.9b, the recipe is as follows (Figure 3.9c): (1) the tin source (5.69 g) and the substrate were first heated from 25 °C to 690 °C in 7 min under an argon flow of 150 sccm; (2) the temperature was retained at 690 °C for 20 min with continued argon flow of 150 sccm; and (3) the system was cooled down naturally from 690 °C to room temperature in ~ 2 hours. The temperature of the sulfur source (1.15 g, placed 19 cm upstream from the center) was calibrated to be 100 °C when the tin source was at 690 °C. The orthorhombic crystal shape reflects the natural crystal structure of SnS, and Raman scattering experiments (Figures 3.17a and b) further confirm that such orthorhombic crystals are indeed SnS with characteristic A₁g symmetry Raman modes at 192 cm⁻¹ and 218 cm⁻¹ (see section 3.3.2). [49]



Figure 3.9: Optical images of devices with (a) hexagonal SnS₂ crystal arrays and (b) orthorhombic SnS crystal arrays, after seeded CVD growth with the same recipe shown in (c) using cross marks of Pd (70 nm)/Cr (5 nm) on SiO₂ (200nm)/Si substrates as the catalyst sites. As a control, the only difference for these two CVD experiments is a sulfur source position at 17 cm away from the furnace center for (a) and 19 cm for (b), respectively. (d) A higher magnification image for the four crystals in the upper left corner of (a). Note that one crystal appears darker in (a) when imaged with lower magnification (likely due to different illumination condition). Scale bar: 10 μ m.

3.2.10 The Effect of Cooling Stage on the Growth of Hexagonal SnS₂ Crystal Grains

To elucidate the growth mechanism for SnS_2 crystals, we discuss the CVD process in details. For the sample of Figure 3.7a, we used the recipe shown in Figure 3.7b, with the tin source material (weight: 0.50 g) placed at the furnace center and the sulfur source material (weight: 1.15 g) placed 17 cm upstream (Figure 3.3) from the center. The sulfur source temperature was calibrated at 213 $^{\circ}C$ when the furnace center was at 705 °C. By performing control experiments (Figure 3.10) with argon purging at different temperatures during the 30-minute cooling step from 705 $^{\circ}C$ to 580 °C, we found that the nucleation of SnS_2 crystals occurs mainly during cooling from 680 °C to 580 °C. In those control experiments, all other conditions are the same, except that the system was purged with argon gas flow of 1000 sccm at different temperatures (marked by the red arrow). We used a tin source of 0.50 g placed at the furnace center and a sulfur source of 1.15 g placed at 17 cm upstream away from the center. When an argon purging (1000 sccm) was used at a temperature of 660 $^{\circ}C$ during the cooling step, the resultant hexagonal crystals are much thinner. We have produced thin SnS_2 crystals with a thickness down to 4 nm (~ 7 atomic layers). With an argon purging at 680 $^{\circ}C$ during cooling, there is no growth of SnS₂ crystals on substrates. This favors a growth mechanism that Sn–S gas phase is first formed at high temperatures, and then during the cooling from 680 °C to 580 °C such floating Sn-S gases are condensed on the nucleation sites and grown into hexagonal SnS_2 crystals. This mechanism explains the absence of SnS_2 crystal growth with the argon purging above 680 $^{\circ}C$, since the floating Sn–S gases are diluted by the argon flow and thus the crystal nucleation on substrates is diminished. Furthermore, additional control experiments (Figure 3.11) have revealed that the yield of SnS_2 crystal growth also depends on the cooling rate from 660 °C to 580 °C. Therefore, the cooling stage from 680 °C to 580 °C without argon flow is critical for the seeded nucleation of SnS_2 crystals on predefined sites in the CVD process when we use a relatively small amount of tin source material ~ 0.50 g.

3.2.11 The Effect of Cooling Rate on the Growth of Hexagonal SnS_2 Crystal Grains

In Figure 3.11, we show the results of control experiments of CVD growth with different cooling rate during the crystal nucleation stages from 660 °C to 580 °C. In those control experiments, all other conditions are the same, except that the cooling time from 660 °C to 580 °C was varied from 6 to 26 minutes. We used a tin source of 0.50 g placed at the furnace center and a sulfur source of 1.15 g placed at 17 cm upstream away from the center. The results reveal that the yield of SnS_2 crystal growth depends on the cooling rate, and the crystal nucleation on catalyst sites is optimized with suitable cooling time between 6 to 26 minutes.



Figure 3.10: Optical images (left) of devices after seeded CVD growth with corresponding recipes (right) using cross marks of Pd (2nm)/Cr (1nm) on SiO₂ (300nm)/Si substrates as the catalyst sites. As a control, the only change in these recipes is the temperature for argon purging during the cooling stage from 680 °C to 580 °C.



Figure 3.11: Optical images (left) of devices after seeded CVD growth with corresponding recipes (right) using cross marks of Pd (2nm)/Cr (1nm) on SiO₂ (300nm)/Si substrates as the catalyst sites. As a control, the only change in these recipes is the cooling rate from 660 °C to 580 °C.

3.3 Characterization

3.3.1 AFM

Figure 3.12 shows an AFM image of a typical semihexagonal thin crystal with a thickness of 20 nm (~ 34 layers) and lateral dimension ~ 20 μ m. AFM line scan indicates a smooth crystal surface with average roughness about 0.6 nm (i.e., one monolayer for SnS₂). As shown in Figure 3.13, we can also produce thinner few-layer crystals with a thickness ~ 3 nm (5 layers), which display a triangular crystal shape. However, for such thin few-layer triangular crystals, the CVD yield is low, and the surface roughness follows the substrate, leading to lower crystal quality.

We note that the exact control of the layer numbers of SnS_2 crystals is not realized in our CVD methods, although there is a statistical distribution of the crystal thickness for growth under a given condition as shown in Figure 3.14. Such a statistical distribution of SnS_2 crystal thickness is measured by an atomic force microscope on a total of 39 SnS_2 thin crystals. The CVD growth condition is similar to that of Figure 3.5 except that the target SiO_2/Si substrate was placed at a position ~ 560 °C and 0.34 g S was heated to 115 °C in a position when the zone-center temperature reached 710 °C. Those measured 39 SnS_2 thin crystals are distributed within a 1 cm wide substrate.



Figure 3.12: AFM image of a semihexagonal SnS₂ crystal (scale bar: 5 μ m). Inset: a line scan showing a thickness of 20 nm.



Figure 3.13: (a) Optical image and (b) a zoom-in AFM image of a few-layer triangular crystal (Inset: a line scan showing an average thickness of 3 nm).



Figure 3.14: Statistical distribution of SnS_2 crystal thickness for a given growth condition.

3.3.2 Raman Spectroscopy

Raman spectra (Figure 3.15) confirms that such thin crystals as shown in Figure 3.12 are indeed SnS_2 with characteristic A_{1g} mode at 314 cm⁻¹.



Figure 3.15: Raman spectra of a typical SnS_2 crystal.

Figure 3.16 shows the optical image of a hexagonal crystal and its Raman mapping of the A_{1g} mode at 314 cm⁻¹ for SnS₂, [50] excited with the 514 nm laser line. Since the laser energy (2.41 eV) is larger than the SnS₂ band gap (2.1 eV), light is mostly absorbed and scattered at the surface and the Raman image in Figure 3.16a reveals the uniformity of the hexagonal crystal surface. When we use a laser excitation with energy (1.96 eV, 633 nm line) less than the SnS₂ band gap (2.1 eV), light can penetrate through SnS₂ crystals and reach the substrate. The nucleation site (cross mark) underneath a hexagonal crystal can be seen clearly in the Raman image (Figure 3.16b), indicating that it indeed serves as the nucleation site for crystal growth. Corresponding Raman spectra (Figure 3.16c) confirm that such hexagonal crystals are indeed SnS_2 .

The orthorhombic crystal shape reflects the natural crystal structure of SnS, and Raman scattering experiments (Figures 3.17a and b) further confirm that such orthorhombic crystals are indeed SnS with characteristic Ag symmetry Raman modes at 192 cm^{-1} and 218 cm^{-1} [49].

3.3.3 SEM and EDX

Figure 3.18 presents the SEM image of a thick hexagonal SnS_2 crystal with lateral size ~ 50 μ m. The EDX analysis of such crystal is shown in Figure 3.19. The atomic percents of Sn and S are 23.35 % and 47.35 %, respectively, which gives the atomic ratio of Sn : S \approx 1 : 2.

3.3.4 TEM

The high quality of such thin SnS_2 crystals is further examined by TEM imaging. Figures 3.20a and b show the bright-field TEM image and the selected-area-electrondiffraction (SAED) pattern of a SnS_2 crystal, respectively, which clearly demonstrates single-crystal quality with expected hexagonal crystal structure. Figure 3.20c shows a standard high-resolution TEM (HRTEM) image of atoms arranged in the hexagonal pattern, giving an interplanar lattice spacing of 0.32 nm, which corresponds to the (100) plane of SnS_2 and agrees well with the known value of 0.317 nm for SnS_2 crystal.



Figure 3.16: Raman scattering characterization of typical hexagonal SnS_2 crystals. (a) An optical image (Left) and Raman mapping (Right) with a 514 nm laser for a typical SnS_2 hexagonal crystal. Scale bar: 2 μ m. (b) An optical image (Left) and Raman mapping (Right) with a 633 nm laser for another SnS_2 crystal. Scale bar: 2 μ m. (c) Raman spectra of the SnS_2 crystal of (a) and the Si substrate.



Figure 3.17: Orthorhombic SnS crystal arrays and Raman scattering characterization. (a) An optical microscope image of SnS crystal arrays on SiO₂ (200 nm)/Si substrate, produced by the CVD recipe described in main text. Scale bar: 100 μ m. (b) A higher magnification image for the four crystals in the upper left corner of (a). Note that one crystal appears darker in (a) when imaged with lower magnification (likely due to different illumination condition). Scale bar: 10 μ m. (c) An optical image (Left) and Raman mapping (Right) with a 633 nm laser for a SnS crystal (scale bar: 1 μ m); and (d) the Raman spectra for this SnS crystal and the Si substrate.



Figure 3.18: SEM image of a typical thick SnS_2 crystal.



Figure 3.19: EDX analysis of the thick hexagonal SnS_2 crystal in Figure 3.18.

[51-56] Figure 3.20d shows the IFFT image of the SnS₂ crystal.

3.3.5 XPS Analysis of the Nucleation Sites

We performed XPS experiments on Pd and Pd/Cr samples before and after CVD growth (Figure 3.21). As shown in Figures 3.21a and b, the XPS data show that the binding energy of the Cr $2p_{3/2}$ peak is the same before and after the CVD growth. But for both the Pd/Cr seed (Figures 3.21c and d) and the Pd only seed (Figures 3.21e and f), the Pd $3d_{3/2}$ and $3d_{5/2}$ peaks disappear after the CVD growth, which suggests that the Pd-capping layer is changed at high temperatures during CVD (e.g., Pd may be diluted or buried via diffusion, or its binding states may be changed due to chemical reactions).

3.4 Conclusion

In summary, we have achieved for the first time successful CVD of thin crystals of layered semiconductors SnS_2 and SnS. Different conditions of CVD are studied. With a novel strategy for controlled CVD synthesis of thin crystal arrays of layered semiconductors, we have accomplished for the first time successful seeded growth of arrays of thin SnS_2 single crystals at predefined locations on the chip. This novel approach for seeded growth of high quality 2D semiconductor crystal arrays may open a pathway toward integrated optoelectronics applications.



Figure 3.20: TEM characterization of CVD produced thin SnS_2 crystals. (a) Brightfield TEM image of the semihexagonal SnS_2 crystals. (b) TEM selected-area-electrondiffraction (SAED) pattern of the crystal, showing single-crystal quality with hexagonal structure. Standard HRTEM image (c) and an IFFT image (d), showing defectfree hexagonal structure. Scale bar: 2 nm.



Figure 3.21: XPS analysis on Pd/Cr and Pd seeds before the CVD growth, and Pd/Cr and Pd seeds after the CVD growth. (a)-(b) XPS data of Cr $2p_{3/2}$ peak for the Pd (2 nm)/Cr (1 nm) seeds before and after CVD growth, respectively; (c)-(d) XPS data of Pd $3d_{3/2}$ and $3d_{5/2}$ peaks for the Pd (2 nm)/Cr (1 nm) seeds before and after CVD growth, respectively; (e)-(f) XPS data of Pd $3d_{3/2}$ and $3d_{5/2}$ peaks for the Pd (2 nm) seeds before and after CVD growth, respectively; (e)-(f) XPS data of Pd $3d_{3/2}$ and $3d_{5/2}$ peaks for the Pd (2 nm) seeds before and after CVD growth, respectively; (e)-(f) XPS data of Pd $3d_{3/2}$ and $3d_{5/2}$ peaks for the Pd (2 nm) seeds before and after CVD growth, respectively.

Chapter 4

SnS₂ Field Effect Transistors and Photodetectors

4.1 Introduction

A photodetector is a sensor of light or other electromagnetic energy, which can convert incident radiation into an electrical signal. Photodetectors are applied in wide fields of digital photography, chemical/biological detection, photovoltaic cells, and space communication. [57–67]

4.2 Experimental Details

We employ field effect transistors (FETs) based on CVD-grown SnS_2 thin crystals as high speed photodetectors. The photodetector devices (Figures 4.1a and b) are constructed via electron-beam lithography and lift-off process as described in chapter 2. Drain and source metal electrodes of 45 nm Pd (on top of 5 nm Cr adhesion layer) are patterned to electrically contact a thin SnS₂ crystal (as the conduction channel). A schematic diagram of the device configuration is shown in Figure 4.1b, where degenerately doped Si substrate is used as a back gate and the gate dielectrics is a 300 nm-thick SiO₂ layer. Figure 4.1a shows an optical microscope image of a photodetector with a source-drain gap ~ 2 μ m. The thickness of the SnS₂ crystal was determined to be ~ 80 nm by AFM. In photocurrent measurements for Figure 4.1, we focus a collateral laser beam (~ mm size) into a laser spot with a diameter of 3.6 μ m and placed the focused laser spot on the SnS₂ channel between the source and drain.

Figure 4.1c shows the drain-source current I_{DS} as a function of gate voltage V_G for the dark state and under illumination with a blue laser (wavelength 457 nm) at power 4.1 μ W. The FET shows a typical n-type behavior with higher conductance at positive V_G , similar to what was previous reported for mechanically exfoliated SnS₂ thin layers. [11, 68] Figure 4.1d presents I_{DS} vs. V_{DS} curves at $V_G = 0$ V under illumination with various laser powers. The dark-state IV curve is strongly nonlinear and asymmetric with respect to the bias polarity, indicating considerable Schottky barriers at the contacts. As the illumination intensity increases, the IV curves become more and more linear and symmetric, attributable to photoinduced hot-carrier transport over the contact barriers.



Figure 4.1: Photodetection with thin SnS₂ FET device. (a) Optical image of the FET device under study. Scale bar: 1 μ m. (b) Schematic diagram of the device configuration. (c) Drain-source current I_{DS} as a function of back-gate voltage V_G at fixed drain-source bias V_{DS} = 2 V for the SnS₂ photodetector in the dark state and under illumination at 4.1 μ W with a blue laser ($\lambda = 457$ nm). (d) I_{DS} vs. V_{DS} curves for the device with various illumination power (Inset: a zoom-in view of data for the dark state). Drain-source current I_{DS} recorded as a function of time with a sampling rate of 660 kHz when the laser beam was modulated periodically at a frequency ~ 800 Hz via: (e) a mechanical chopper; and (f) an acousto-optic modulator (with the laser beam only partially deflected).
4.3 Photodetector Measurements

To measure the photoresponse speed of the SnS_2 FET device, we adopted two experimental methods to modulate the power of the laser beam by either a flying-wheel mechanical chopper or an acousto-optic modulator, and measure the corresponding rise (fall) time of the photocurrent.

4.3.1 Mechanical Chopper

In Figure 4.1e, we present the drain-source current I_{DS} measured as a function of time at a sampling rate of 660 kHz when the collateral laser beam was modulated periodically at a fixed frequency ~ 800 Hz via a mechanical chopper. As shown clearly, the drain-source current I_{DS} demonstrates two states as the laser is on and off. Via examining the rising (falling) edges associated with turning on (off) the laser, we obtain a photoresponse rise (fall) time 12 μ s (17 μ s) for the SnS₂ photodetector, which is defined as the time duration of the net photocurrent ($I_{ON}-I_{OFF}$) to change from 10 % to 90 % in amplitude.

However, we find that in this experimental configuration with mechanical light chopper, the measured photocurrent response time is merely limited by the time to turn on (off) the laser beam which depends on the rotating speed of the flying wheel of the mechanical chopper. This is evident from our control experiments (Figure 4.2): when we increased the speed of the mechanical chopping, the measured rise (fall) time is reduced accordingly since the laser beam is turned on (off) faster. For the device of Figure 4.1, with a chopping speed ~ 400 Hz, the rise time is 24 μ s (Figures 4.2a and b). The rise time reduces to 12 μ s as the chopping speed increases to ~ 800 Hz (Figures 4.2c and d). In a different device with thinner SnS₂ crystal ~ 30 nm, we also observed similar photoresponse time limited by the switching speed of the mechanical chopper. As shown in Figure 4.3, with a chopping speed ~ 800 Hz for the flying-wheel mechanical chopper, we found a rise time ~ 11 μ s (similar to that of the device in Figure 4.2) limited by the laser modulation speed.



Figure 4.2: Photoresponse of the device of Figure 4.1 with laser modulated by a mechanical chopper. (a) Drain-source current I_{DS} as a function of time when the laser beam was modulated periodically at a frequency ~ 400 Hz via a mechanical chopper; and (b) its rising edge. (c) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 800 Hz via a mechanical chopper; and (d) its rising edge.



Figure 4.3: Photocurrent response for a different device with a 30 nm thick SnS_2 channel. (a) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 800 Hz via a mechanical chopper; and (b) its rising edge (Inset: optical image of the device. Scale bar: 1 μ m).

4.3.2 Acousto-Optic Modulator

To pursue a better determination of the actual photoresponse time, we used an alternative acousto-optic modulator to modulate the laser beam with a faster turning on (off) time (rated ~ 150 ns in switching time). As shown in Figure 4.1f, for the same device, the measured photoresponse rise (fall) time is now 5 μ s (7 μ s), which is merely limited by the bandwidth of the current preamplifier (3 dB attenuation at 200 kHz for a current sensitivity of 1 μ A/V, corresponding to an electronic rise time ~ 5 μ s).

Unlike mechanical chopper, in the experimental configuration with an acoustooptic modulator (with a switching time rated at 150 ns), for the same device as measured in Figure 4.2, the measured rise time is ~ 6 μ s for both modulation at 400 Hz and 800 Hz as shown in Figures 4.4a to d. Additionally, a comparison between

Figure 4.1f and Figure 4.4d reveals that the photoresponse rise time is similar (~ 5 μ s) even if the measurements are under different applied drain-source bias V_{DS} and laser power with the acousto-optic modulator.



Figure 4.4: Photoresponse of the device of Figure 4.1 with laser modulated by an acousto-optic modulator. (a) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 400 Hz via an acousto-optic modulator; and (b) its rising edge. (c) I_{DS} vs. time when the laser beam was modulated periodically at a frequency ~ 800 Hz via an acousto-optic modulator; and (d) its rising edge.

Unfortunately, we are not able to accurately further determine the photocurrent speed since the signal-noise ratio is worse for amplification of electrical current with higher bandwidth in experiments (Figure 4.5), considering a small on-state photocurrent ~ 120 nA. In experiments, we use a commercial current amplifier (Stanford Research System, SR 570) to measure photocurrent. The bandwidth of the amplifier is related to the sensitivity selected. For a sensitivity of 10 μ A/V, the instrumentlimited bandwidth is 800 kHz (3 dB attenuation). Figure 4.5a shows the drain-source current I_{DS} as a function of time when the laser beam was modulated periodically at a frequency ~ 800 Hz via an acousto-optic modulator, for the same device of Figure 4.1. The signal-noise ratio is worse for the data with a sensitivity of 10 μ A/V compared with that for a sensitivity of 1 μ A/V (Figure 4.1e). Figure 4.5b shows a rising edge of the photocurrent response. Nevertheless, the actual photoresponse time should be much faster in the thin crystalline SnS₂ photodetector, and our measurements (albeit limited by instrumentation capability) provide an upper limit of photoresponse rise (fall) time as 5 μ s (7 μ s).



Figure 4.5: Time-resolved photocurrent measured with an amplifier sensitivity of 10 μ A/V (bandwidth: 3 dB attenuation at 800 kHz). (a) Drain-source current I_{DS} recorded as a function of time when the laser beam was modulated periodically at a frequency ~ 800Hz via an acousto-optic modulator; and (b) its rising edge.

To our knowledge, a rise time of 5 μ s demonstrated here is the fastest response time ever reported for photodetectors based on layer 2D semiconductors, [25–35] compared with recently reported rise time \sim 1 ms for black phosphorous, [34] \sim 70 μs for fewlayer MoS₂ [33] (~ 1 sec for monolayer MoS₂ [32]), and ~ 18 ms for In₂Se₃. [26] Table 4.1 lists the relevant figures-of-merit reported in literatures for other devices based on semicondcuting layered materials. The observed high speed photocurrent response can be attributed to the high quality single crystal (as shown by TEM in Figure 3.20) and thus high charge-carrier mobility of the CVD-synthesized thin SnS_2 crystals. Experimentally, we found that the crystal quality strongly affects the photoresponse speed. For those SnS_2 crystals in the order of 10 nm thick with good crystallinity and smooth surface, we observe similar photoresponse time in the order of μ s. Two typical samples with thickness of 80 nm and 30 nm are shown in Figures 4.1 and 4.3, respectively. In contrast, for those thin few-layer SnS_2 crystals with low crystal quality and a rough surface (e.g., the sample of Figures 3.13 with a surface roughness comparable to its thickness $\sim 3 \text{ nm}$), the photoresponse is much slower with a rise time in the order of seconds. Our experimental observations indicate that the crystal defects may strongly influence the dynamics of photogenerated carriers (e.g., by affecting the balance between the generation rate and the recombination rate of photocarriers), thus leading to a photoresponse speed dependent on the quality and thickness of SnS_2 crystals.

Material	Rising time	Falling time	Responsivity (mA/W)	Detectivity (Jones)	Ref.
Hexagonal Tellurium Nanoplates	4.4 s	2.8 s	389.5k		[16]
Black phospho- rus	$1 \mathrm{ms}$		4.8		[34]
$1L MoS_2$	$600 \mathrm{\ ms}$		880k	$\sim 2 \times 10^{12}$	[32]
$1L MoS_2$	$50 \mathrm{ms}$		8		[30]
$> 1L MoS_2$	$> 1000 \mathrm{\ ms}$		~ 150	2×10^{10}	[31]
$> 1L WS_2$	$5.3 \mathrm{ms}$		21.4M		[25]
$> 1L In_2Se_3$	$18 \mathrm{\ ms}$		395k	2.26×10^{12}	[26]
> 1L GaTe	$6 \mathrm{ms}$		10M		[27]
> 1L GaSe	$300 \mathrm{\ ms}$		2.8k		[28]
> 1L GaS	$30 \mathrm{ms}$		4.2k	10^{13}	[69]
$1T MoS_2$	$43.7~\mu\mathrm{s}$				[70]
$MoS_2/Graphene$	0.28s		10k		[71]
Graphene	$25 \mathrm{\ ps}$		0.5		[64]
$> 1L MoS_2$	$70 \ \mu { m s}$	110 $\mu {\rm s}$	570	9×10^9	[33]
$CNT-MoS_2$	$15 \ \mu s$		> 10		[72]
Mo-doped ReSe_2	$96 \mathrm{ms}$	$340 \mathrm{ms}$	55.5k		[73]
MoSe ₂	$60 \mathrm{ms}$	$60 \mathrm{ms}$	13		[74]
> 1L GaSe			17		[75]
$1L MoSe_2$	$\sim 25 \text{ ms}$	$\sim 25 \text{ ms}$			[76]
SnS_2	$5 \ \mu s$	$7 \ \mu \mathrm{s}$	8.8	2×10^9	[42]

Table 4.1: Comparison of Key Device Performance Figures-of-Merit for Photodetectors Based on 2D Layered Materials

4.3.3 Photoresponsivity

To further characterize the device performance, we now discuss other figures of merit. Figure 4.6a shows the photoresponsivity as a function of incident laser power (in logarithmic scale) with a blue laser at wavelength 457 nm (photon energy E_{ph} = 2.72 eV). The photoresponsivity R was obtained from the experimental data of Figure 4.6d by using the formula $R = I_{ph}/P$, where I_{ph} is the net photocurrent and P is the incident laser power. It is clear that the responsivity decreases as the laser power is increased, which could be related to enhanced scattering or recombination rate of hot carriers as their density increases at higher laser power. A quantitative fitting of the data yields a power law behavior $R \propto P^{\alpha-1}$ with the fitting parameter $\alpha = 0.77$, which is similar to the reported behavior for few-layer black phosphorous $(\alpha = 0.7)$ [34] and few-layer MoS₂ $(\alpha = 0.71)$ [33]. With an incident laser power of 0.24 μW (power density 2.4 \times 10 4 W/m²), the device demonstrates a photoresponsivity R = 8.8 mA/W at bias $V_{DS} = 2 \text{ V}$ and $V_G = 0 \text{ V}$. On the other hand, the photoresponsivity is also strongly dependent on the gate voltage. In Figure 4.6b, we plot the photoresponsivity R as a function of gate voltage V_G at fixed incident laser power of 4.1 μ W. Under illumination with a constant laser power, the photoresponsivity is greatly enhanced as V_G sweeps to the positive side, e.g., the responsivity at $V_G = 10$ V is increased to more than 1.5 times of that at $V_G = 0$ V (Figure 4.6b). This enhancement of photoresponse can be explained by the increase of carrier mobility or the reduction of trapping of photoinduced carriers as the charge-carrier density is increased by sweeping V_G towards the FET ON state. Given the strong dependence of photoresponsivity on measurement conditions such as incident laser power (density), applied gate voltage V_G , and drain-source bias V_{DS} , it is not practical to directly compare and evaluate the responsivity performance of photodetector devices made from different layered 2D materials [25–35] unless photocurrent measurements are done under similar conditions.



Figure 4.6: Logarithmic scale plot of photoresponsivity R as a function of incident laser power (with a blue laser: $\lambda = 457$ nm) at $V_{DS} = 2$ V and $V_G = 0$ V for the device of Figure 3; and (b) R vs. V_G at constant laser power P = 4.1 μ W at $V_{DS} = 2$ V.

Nevertheless, we list a few other materials for simple comparison with our SnS₂ devices which can also be found in Table 4.1. For the device of Figure 4.1, we have a photoresponsivity R = 8.8 mA/W measured with an incident laser power $P = 0.24 \mu$ W (power density $2.4 \times 10^4 \text{ W/m}^2$) and $V_G = 0$ V at bias $V_{DS} = 2$ V. For few-layer black phosphorous [34], R = 4.8 mA/W was reported with a lower laser power $P = 0.01 \mu$ W (power density $\sim 0.24 \text{ W/m}^2$ with a laser spot 230 μ m in diameter) and $V_G = 0$ V at bias $V_{DS} = 0.2$ V. For single-layer MoS₂, R = 8 mA/W was obtained [30] with $P = 80 \mu$ W ($8 \times 10^5 \text{ W/m}^2$ with a beam spot $\sim 10 \times 10 \mu$ m²) and $V_G = 50$ V at $V_{DS} = 1$ V, although a high R = 880 A/W was reported [32] with much lower

power $P = 150 \text{ pW} (0.24 \text{ W/m}^2)$ and $V_G = -70 \text{ V}$ at $V_{DS} = 8 \text{ V}$.

4.3.4 Specific Detectivity

Furthermore, we note that photoresponsivity not only depends on the measurement conditions such as laser power, V_G and V_{DS} , but also is strongly related to the device geometry and the Schottky barrier at the contacts. Therefore, we next estimate the specific detectivity D^* , which is more useful for direct comparison between devices with different geometry (e.g. detector area) if other measurement conditions are similar. The specific detectivity is inversely proportional to the noise equivalent power (NEP), i.e., the minimum detectable optical signal power generating a photocurrent signal equal to the noise current in the dark state within a bandwidth of 1 Hz. Considering a dominating shot noise in the dark state current I_{dark} , we have NEP = $(2eI_{dark})^{1/2}/R$, and $D^* = A^{1/2}/NEP = RA^{1/2}/(2eI_{dark})^{1/2}$ with A the photodetector area. Thus with $I_{dark} = 5.8$ pA at $V_{DS} = 2$ V (Figure 4.1d), the specific detectivity D^* is calculated to be 2×10^9 Jones for our SnS₂ device, measured with a 457-nm laser under power density $2.4 \times 10^4 \text{ W/m}^2$ and $V_G = 0 \text{ V}$ at bias $V_{DS} = 2 \text{ V}$. This is comparable to what are reported for few-layer MoS₂: $D^* \sim 9 \times 10^9$ Jones measured [33] with a 532-nm laser under power density 2×10^4 W/m² (V_G unspecified) at bias $V_{DS} = 10$ V; and $D^* \sim 2 \times 10^{10}$ Jones measured [31] with a 455-nm laser under power density 500 W/m² (V_G unspecified) at bias $V_{DS} = 1$ V.

4.3.5 Quantum Efficiency

Next, we estimate the quantum efficiency of the SnS₂ photodetector. The external quantum efficiency (*EQE*), i.e., the ratio of the number of photogenerated carriers to the number of incident photons, can be calculated to be ~ 2.4 % by using *EQE* = $hcR/(e\lambda)$, where *h* is Planck's constant, *c* is the speed of light, λ is the laser wavelength, and *e* is the electron charge. The absorption coefficient of SnS₂ at $\lambda = 457$ nm (2.72 eV) is $\eta = 3 \times 10^4$ cm⁻¹. [77] Considering a relevant device thickness d = 80 nm, we obtain a photo absorption probability $p = 1 - exp(-\eta d) = 21.3$ % and thus can estimate the internal quantum efficiency IQE = EQE/p = 11.3 %.

4.4 Mechanism

Finally, we discuss the mechanism of the photocurrent generation. Our devices are in a configuration of metal-semiconductor-metal junctions, and the main mechanism for photocurrent generation seems to be the carrier excitation in the semiconducting SnS₂ channel (band gap: $E_g = 2.1 \text{ eV}$) instead of in the contact region with Schottky barriers. This is confirmed by our control experiments for another larger device with 15 μ m wide SnS₂ channel: we observed photocurrent response with the focused laser spot (~ 3.6 μ m) well restricted inside the SnS₂ channel away from the contacts as shown in Figure 4.7. In addition, as shown in Figures 4.8a and b, when we used another laser ($\lambda = 633 \text{ nm}$) with photon energy $E_{ph} = 1.96 \text{ eV} < E_g$, we saw much weaker photocurrent response: two order of magnitude smaller than that of Figure 4.1d for the 457-nm laser ($E_{ph} = 2.72 \text{ eV}$). This reveals that light absorption is much weaker to generate charge carriers within the band gap, confirming that photoninduced carrier excitation inside SnS_2 channel dominates the photocurrent response in our devices.



Figure 4.7: Photodetection using a SnS₂ FET device with a 15 μ m wide source-drain gap (much larger than the focused laser spot ~ 3.6 μ m). (a) I_{DS} vs. V_{DS} curves at $V_G = 0$ V for the device with various illumination power. Inset: Optical image of the device (scale bar: 1 μ m). (b) I_{DS} vs. V_G at fixed drain-source bias $V_{DS} = 10$ V in the dark state and under illumination at 153 nW with a blue laser ($\lambda = 457$ nm).

4.5 Conclusion

In summary, with a novel strategy for controlled CVD synthesis of thin crystal arrays of layered semiconductors, we have achieved for the first time successful seeded growth of arrays of thin SnS₂ single crystals at predefined locations on the chip. Moreover, we have demonstrated the application of such CVD-grown high-quality thin SnS₂ crystals as high-speed photodetectors with fast photocurrent response time $\sim 5 \ \mu s$ (which is an upper limit and merely limited by instrumentation capability). This



Figure 4.8: Photophotocurrent response of the same SnS_2 device illuminated with a red laser ($\lambda = 633$ nm).

novel approach for seeded growth of high quality 2D semiconductor crystal arrays may open a pathway towards integrated optoelectronics applications.

Chapter 5

Observation of Multiple Superconducting Gaps in β -PdBi₂

5.1 Introduction

5.1.1 Andreev Reflection

Andreev reflection (AR), a quantum transport phenomenon, occurs at the interface between a normal metal (N) and a superconductor (S) with low potential barriers. For example, let us consider an N–S junction with no potential barrier as shown in Figure 5.1. For incoming electrons with $eV < \Delta$, Δ being the energy gap in the S side, will not be able to propagate through the interface since only Copper pairs exist in this energy range in S. For each electron, a hole of opposite wave vector is reflected and a Cooper pair is transmitted in the S side, the total charge and momentum are conserved. For electrons approaching the interface with $eV > \Delta$ are normally transmitted as electron-like quasiparticles. Because of AR, the conductance of the junctions is doubled for $V < \Delta/e$. Blonder, Tinkham, and Klapwijk (BTK) have developed a theory [78] describing the electrical transport in an N–S junction with different potential barriers. The evolution of the dI/dV conductance as a function of biased voltage V for different potential barriers characterized by the barrier strength Z is schematically shown in Figure 5.2.



Figure 5.1: Electrical transport at an ideal (barrierless) N/S interface at T = 0K. Incoming electrons with $eV < \Delta$ are reflected as holes and, for each electron, a Cooper pair is transmitted (Andreev reflection). Electrons approaching the interface with $eV > \Delta$ are normally transmitted as electron-like quasiparticles. (Adapted from [79])



Figure 5.2: Normalized conductance curves of an N–S junction with $\Delta = 2.66$ meV at T = 0.24 K calculated by numerical simulation of the BTK model at different values of the barrier strength Z, from pure Andreev (Z = 0) to pure tunneling (Z = 10) regimes.

5.1.2 Point-contact Andreev Reflection Spectroscopy

Point-contact AR spectroscopy (PCAR) [78–83] is the technique can provide fundamental information on the energy gap Δ of a superconductor due to the enhanced electrical conductance occurs at bias voltage $V < \Delta/e$. The common method for fabrication of point contacts is so-called "needle-anvil" technique, where a sharp metallic tip is mechanically pressed against the sample surface (Figure 5.3a). Typically, the tip has an ending diameter of tens of micrometers and it is easily deformed during the contact [84]. Due to the poor thermal and mechanical stability of the thus-prepared N–S point contacts, significant challenges remain to make the device if the sample is very small (tens of micrometers). Since 2001, so-called "soft" point-contact technique is developed. In this technique, the contact is made between the clean sample surface and a small drop (~ 50 μ m in diameter) of Ag or In paste. The Ag or In electrode is connected to circuit through a thin Au wire (10-25 μ m in diameter) stretched over the sample as shown in Figure 5.3b. The contacts are mechanically and thermally stable enough to perform the measurements in a cryocooler. However, it is difficult to make several contacts on the same sample at the same time.

In 2012, Peng et al. [85, 86] developed a novel experimental approach by designing devices with suspended superconducting (SC) micro-scale crystals bridging multi-terminal normal metal electrodes (Figure 5.4), and have employed this to unveil the existence of two energy gaps in $Fe_{1+y}Te_{1-x}Se_x$. A $FeTe_{0.5}Se_{0.5}$ microcrystal obtained by mechanically cleaving was manipulated onto preprinted multi-terminal metal electrodes with a sharp probe tip attached to a micromanipulator. Figure 5.4b shows the optical image of a typical device. The advantage of this method is



Figure 5.3: (a) Experimental arrangement for point-contact measurements with the typical needle-anvil technique. A metallic tip (Au, Pt-Ir, Pt, Ag) is gently pressed against the surface of the sample. (b) The "soft" point-contact technique where a tiny spot of Ag paste (or a tiny flake of In) replaces the tip. (Adapted from [79])

that they are able to make several contacts on one device which is important to reproduce statistical results from different combination of terminals. However, the disadvantage of this method is that the superconductor crystal is not stable on the preprinted electrodes. It is worth to mention that Peng et al. have also designed a circuit for obtaining AR spectra for the target N–S junction between the electrode and superconductor, which also provide diagnostic information on the surface (Figure 5.4a).

In this work, we develop a novel experimental approach to point-contact spectroscopy by combining the "soft" point-contact technique with modern nanofabrication process (Figure 5.5). Several electrodes (~ 4 μ m in diameter) are patterned on the surface of the superconductor using nanofabrication process as mentioned in chapter 2, indicating a good thermomechanical stability. The size of electrodes is much smaller than "needle-anvil" and "soft" point-contact techniques.



Figure 5.4: (a) Schematic diagram of a superconductor microcrystal lying on top of three normal metal electrodes and a circuit designed for obtaining Andreev reflection spectra for the target N–S junction between the $I_+(V_+)$ electrode and the superconductor. (b) Optical microscope image of a device with a suspended microcrystal of $Fe_{1+y}Te_{1-x}Se_x$ bridging six parallel metal electrodes (35 nm Pd/5 nm Cr) spaced ~ 500 nm apart. The four center electrodes (labeled as 2–5) are designed to be 1 μ m wide while the two outside electrodes (labeled as 1 and 6) are 4 μ m wide. (Adapted from [85])



Figure 5.5: Schematic diagram of a superconductor nanoplate patterned with three normal metal electrodes and a circuit designed for obtaining AR spectra for the target N–S junction between the $I_+(V_+)$ electrode and the superconductor.

5.1.3 Layered Superconductor

Recently, layered superconductors have been attracting enormous interest because of the low-dimensionality of their electronic states. Most of superconductors with the highest transition temperature are layered materials. Most recently, attention was paid to Bi-based and Bi-containing superconductors, such as $Bi_2Sr_2Ca_2Cu_3O_x$, whose T_C is larger than 110 K.

In 1963, Matthias et al. [87] have found several superconducting phases in the Pd-Bi alloys: monoclinic α -PdBi with a T_C of 3.8 K, monoclinic α -PdBi₂ with a T_C of 1.7 K, tetragonal β -PdBi₂ with a T_C of 4.25 K, and hexagonal γ -Pd₃Bi₅ with a T_C of 4 K. The latest experimental data from Imai et al. shows a T_C of 5.4 K for β -PdBi₂. [36] The temperature dependences of the upper critical magnetic field and the specific heat suggest that β -PdBi₂ is a multiple-band/multiple-gap superconductor.

The electronic band structure and Fermi surface of the β -PdBi₂ by First-principles calculations suggest a complicated superconducting gap structure for this material. [37] The presence of multiple Fermi surfaces suggests that β -PdBi₂ should be a multiple-band/multiple-gap superconductor, as was indicated in Imai et al.'s experiment. However, there is no direct proof from STM or other measurements. Figure 1.5 shows the crystal structure of β -PdBi₂. Because of the weak van de Waals force between two Bi-layers, β -PdBi₂ can be easily peeled off by mechanical method.

Point-contact spectroscopy is a very useful tool for studying superconducting gap structures via Andreev reflection (AR) spectrum at normal metal/superconductor (N–S) junctions. PCAR spectroscopy has been employed to reveal the existence of two SC gaps in MgB₂ [88], Ba_{0.55}K_{0.45}Fe₂As₂ [89], and Fe_{1+y}Te_{1-x}Se_x [85, 86]. Here we describe a novel experimental approach to point-contact spectroscopy for nanoplate superconductor and have employed this method to unveil the existence of multiple gaps/multiple band in β -PdBi₂ which is important for understanding its pairing mechanism.

5.2 Experimental Details

In this section, we report the synthesis of single crystal bulk material of β -PdBi₂, and its bulk characterizations, which are done by Kui Zhao from Dr. Paul Chu's group at TcSUH (unpublished results). The devices fabricated with mechanically-exfoliated β -PdBi₂ nanoplate by using nanofabrication techniques as mentioned in chapter 2. Their electronic properties are further characterized by electrical measurement with novel diagnostic method.

5.2.1 Crystal Growth and Bulk Characterization

The synthesis of single-crystal bulk material of β -PdBi₂, and its bulk characterizations are done by Kui Zhao from Dr. Paul Chu's group at TcSUH (unpublished results). Single-crystal bulk materials of β -PdBi₂ were synthesized through a melt-growth method. Stoichiometric amount of Pd and Bi grains were sealed in an evacuated quartz tube, which was heated up to 700 °C, kept for 10 hours and then slowly cooled to 450 °C in 30 hours. For retaining the β -phase, the quartz tube was hence quenched in iced water directly from 450 °C.

X-ray powder diffraction (XRD) was performed on the single crystals at room temperature from 10 to 90 degrees using a Panalytical Xpert Diffractometer. Electrical resistivity as a function of temperature $\rho(T)$ and field $\rho(H)$ was measured by employing a standard 4-probe method using a Linear Research LR400 ac bridge operated at 15.9 Hz in a Quantum Design Physical Property Measurement System (PPMS) up to 7 T and down to 1.9 K.

 β -PdBi₂ single crystals with shining metallic luster, typical size of 5 mm², and preferred orientation along the c-axis after cleavage, were obtained through the meltgrowth method, as shown in Figure 5.6a. The calculated lattice parameter c [12.963(3) Å] is consistent with previous report. [36, 90, 91] A representative SEM image of the β -PdBi₂ single crystal is also shown as the inset of Figure 5.6a. Electrical resistivity measurement has shown that the superconducting transition temperature (T_C) of the grown β -PdBi₂ crystal is 5.4 K, which is consistent with work from Imai et al.



Figure 5.6: (a) (001) XRD pattern of β -PdBi₂ bulk crystal with preferred orientation along c axis; the inset shows a SEM image of one representative crystal. (b) Resistivity of β -PdBi₂ bulk crystal from 2 to 300 K; the inset presents resistivity data between 4 and 6 K. (Unpublished results from Dr. Paul Chu's group at TcSUH.)

5.2.2 Device Fabrication and Characterization

Thin layer of β -PdBi₂ is obtained by mechanically exfoliation, followed by transferring onto a degenerately n-doped silicon wafer covered with a 300 nm layer of thermally grown silicon dioxide. Figure 5.7 shows an optical image and an AFM image of the device, where a β -PdBi₂ nanoplate is patterned with eight 4- μ m wide metal electrodes of 5 nm Cr/50 nm Pd spaced 4 μ m apart as designed via electron-beam lithography and lift-off process. Each electrode is labeled for further measurement. The thickness of the β -PdBi₂ nanomembrane was determined to be ~ 120 nm by AFM, as shown in Figure 5.7b.



Figure 5.7: Optical and AFM image of β -PdBi₂ device. (a) Optical microscope image of a device with a mechanically exfoliated β -PdBi₂ nanoplate patterned with eight 4- μ m wide metal electrodes (50 nm Pd/5 nm Cr) spaced 4 μ m apart. (Scale: 10 μ m.) (b) AFM image of the device.

5.2.3 Electrical Measurement

A schematic diagram of the Andreev reflection device configuration is shown in Figure 5.5. In this circuit [85], a small AC current superimposed to a DC bias current is driven between the I_+ and I_- terminals while both the DC voltage drop and the AC voltage drop across the N–S junction are monitored between the V_+ and V_- terminals. In this way, the AR spectrum, i.e. the differential conductance dI/dV versus the DC voltage bias V, is obtained for the target junction between the $I_+(V_+)$ electrode and the superconductor. We note that the I_+ and V_+ terminals are connected to the opposite ends of the same electrode so that the measured voltage drop is exactly across the target N–S junction by excluding the electrode resistance in series. The critical temperature and the critical current of the SC nanomembrane are characterized in a standard four-terminal configuration. Low temperature measurements were performed in Oxford Instruments ³He fridge as described in chapter 2.

5.3 Electron Transport Properties

5.3.1 Characterization of Critical Temperature (T_C)

Figure 5.8 presents the differential resistance R measured in a standard four-terminal configuration as a function of temperature at zero bias current, showing $T_C \sim 5$ K. Measurement configurations are labeled by the electrode numbers in a sequence of $I_+ - V_+ - V_- - I_-$. T_C obtained for the thin film β -PdBi₂ is slightly lower than T_C reported for bulk material (5.4 K), which is possible due to the crystal quality of exfoliated sample.



Figure 5.8: R as a function of temperature T at zero bias current for the microcrystal of Figure 5.7.

5.3.2 Normalized Differential Conductance

Figure 5.9 shows the normalized differential conductance dI/dV versus bias voltage V at temperature T = 0.24 K and under magnetic field B = 0 T for the N–S junction between the electrode 18 and the superconductor of the device shown in Figure 5.7. From the normarlized dI/dV spectrum, we found three characteristic features: (1) two clear plateaus for |V| < 3 mV, (2) a dip between first and second plateau at $|V| \sim 1 \text{ mV}$, and (3) a dip before the dI/dV returns to the normal state value at $|V| \sim 4 \text{ mV}$.



Figure 5.9: Normalized differential conductance dI/dV (black square) versus bias voltage V at temperature T = 0.24 K and magnetic field B = 0 T for the N–S junction between electrode 18 and the superconductor, and a fitting (red solid line) to the data by the BTK theory (see section 5.3.4.)

As shown in Figure 5.10a, when the temperature T is increased, the two plateaus at low bias shrink with the smaller plateau vanishing at T \sim 1.55 K and the larger one vanishing at T \sim 5 K. On the other hand, the position of the first characteristic dI/dV dip shifts to lower bias as T increases, while the dip depth is reducing until it is

not distinguishable above T = 1.55 K. Similarly, the position of the second dip shifts to lower bias as T increases and vanishes above T = 4.5 K. Similarly, as magnetic field increases, the plateaus shrink, while the first dip vanishes at B = 0.15 T and the second dip vanishes above B = 0.8 T (Figure 5.10b).

5.3.3 Origin of the dI/dV Dip

Similar dips have been observed in traditional PCAR spectra for bulk superconductors. [79, 92, 93] Similar to Peng et al.'s results, we have also observed that the existence of such dI/dV dips when the critical current I_c is reached. As shown in Figure 5.11, such a concurrent occurrence of the dI/dV dip and I_c has been observed for different temperature and magnetic field measurements. The origin of the dI/dV dips is explained in reference [85] as following: a smooth change in conductance curve for a N–S junction from a higher linear conductance state at low bias voltage (AR regime) to a lower linear conductance state at high bias voltage (Ohm's law regime) results a dip at inflection point for the corresponding differential conductance curve.

5.3.4 The Existence of Two SC Gaps

Further detailed analysis shows that the two plateaus are attributable to the existence of two SC gaps. The red solid line in Figure 5.9 represents a numerical fitting of the experimental dI/dV data at T = 0.24 K (normalized by the data at T = 5.5 K in Figure 5.10a) using the generalized BTK model with the broadending parameter Γ [94, 95]. The plateaus are well fit by the sum of two BTK conductance as $\sigma =$



Figure 5.10: (a) Raw data of differential conductance dI/dV versus V measured at different temperature under B = 0 T. For clarity, the curves are vertically shifted down by an amount of 1.5 mS degressively from top to bottom, starting from the data for T = 0.96 K. (b) Raw data of dI/dV versus V measured under different magnetic field at temperature T = 0.24 K. For clarity, the curves are vertically shifted down by an amount of 1 mS degressively from top to bottom, starting from the data for B = 0.025 T.



Figure 5.11: Standard four-terminal resistance R (left axis) and measured differential conductance dI/dV (right axis) as a function of DC bias current I (a) at T = 4 K and under B = 0 T and (b) at T = 0.24 K and under B = 0.4 T. Same I_+ and I_- terminals were used to keep the electric field distribution identical for both measurements.)

 $w_S \sigma_S + (1 - w_S) \sigma_L$, where σ_S and σ_L are the normalized conductance for the small and large SC gaps, respectively, and w_S is the weight factor of the small SC gap. The fitting gives $\Delta_S = 0.36 \text{ meV}$ ($\Gamma_S = 0.42 \text{ meV}$) and $\Delta_L = 2.66 \text{ meV}$ ($\Gamma_L = 0.67 \text{ meV}$) for the small and large SC gaps, respectively, the weight factor for the small SC gap is $w_S = 0.865$ and the barrier strength is Z = 0.37.

5.3.5 Energy Gap as a Function of Temperature

All experimetal data of the normalized conductance at different temperatures are fitted by the BTK formula with constant barrier strength Z = 0.37, weight factor $w_S = 0.865$, $\Gamma_S = 0.42$ meV, and $\Gamma_L = 0.62 \sim 0.67$ meV upto 1.55 K. Starting from 2 K, since the small gap disappeared ($\Delta_S = 0$ meV), barrier strength changed to Z = 0.255, $\Gamma_L = 0.6 \sim 0.66$ meV, and weight factor w_S still kept constant. The resulting energy gaps Δ_S and Δ_L as a function of temperature is shown in Figure 5.12. By comparing to the BCS prediction, we found that the small gap closed ~ 1.8 K, and the large gap closed between 4.5 K to 5 K. The small gap is not obvious above $T \sim 2$ K, however, its existence (with a very small or even negligible gap value) before reaching T_C cannot be ruled out. The temperature dependencies of two SC gaps are in good agreement with the prediction of the BCS theory. Our data give experimental support for the two-gap model.

The corresponding coupling strength for both gaps are $2\Delta_S/k_BT_C = 1.7$ and $2\Delta_L/k_BT_C = 12.3$ for $T_C = 5$ K, respectively, which are different than the reported values $(2\Delta_S/k_BT_C = 2.5 \text{ and } 2\Delta_L/k_BT_C = 6 \text{ for } T_C = 5.4 \text{ K})$ by Imai et al. Their

values are calculated by using the two-band model to fit the specific heat data measured above 2 K. For the small SC gap, for $T_1 = 1.8$ K, the corresponding coupling strength is $2\Delta_S/k_BT_1 = 4.6$. The discrepancy might be due to the ballistic condition of AR spectroscopy. We note that in our fitting, we use a simple two-gap BTK model without the interband coupling between different Fermi pockets, which is responsible for the superconductivity. [96] We may also need to consider the contribution from normal metal, which might be due to defects or inhomogeneity.



Figure 5.12: Energy gaps as a function of temperature ($\Delta_L(T)$, black diamonds; $\Delta_S(T)$, red diamonds) determined from the fitting of BTK theory. The solid lines represent BCS predictions.

5.3.6 Standard Four-terminal Differential Resistance R as a Function of DC Bias Current I

In addition, we have performed extra experiments to verify the SC behavior of the nanoplate under study. Figure 5.13 presents the differential resistance R measured in a standard four-terminal configuration as a function of DC bias current at different temperature and under different magnetic field. The data demonstrate that a decreasing critical current I_C as temperature increases, and the normal state is reached at T = 5 K. Similarly, critical current I_C decreases as the magnetic field increases, and the normal state is reached at B = 0.9 T, which is consistent with the bulk data [36].

5.4 Conclusion

In summary, with novel experimental approach to PCAR spectroscopy, experimental support has been found for the two SC gaps in β -PdBi₂. Their dependence on temperature and magnetic filed is also been studied. This work opens up new opportunity to understand the pairing mechanism and study gap structures in layered superconductors.



Figure 5.13: Standard four-terminal differential resistance of the superconductor nanoplate measured by a standard four-terminal configuration (a) at various temperature with B = 0 T and (b) under various magnetic field at temperature T = 0.24 K.

Chapter 6

Conclusion and Outlook

This dissertation focused on the study of electron transport properties of a layered semiconductor SnS_2 and a layered superconductor β -PdBi₂.

Thin crystals of layered semiconductors SnS_2 and SnS were synthesized via chemical vapor deposition—a process suitable for high-quality and large-scale production. Different experimental parameters, such as source materials, growth temperatures, pressure, and nucleation sites were tested. We have also proposed a growth mechanism to understand the growth results and guide us to obtain few-layer SnS_2 crystals. Seeded growth of arrays of thin SnS_2 and SnS single crystals at predefined locations on the chip is successfully achieved with a novel strategy for controlled chemical vapor deposition method. Moreover, we have demonstrated the application of such CVD-grown high-quality thin SnS_2 crystals as high-speed photodetectors with fast photocurrent response time ~ 5 μ s, which is the fastest response time ever reported for photodetectors based on layer 2D semiconductors to our knowledge. The observed high speed photocurrent response can be attributed to the high single-crystal quality (as shown by TEM) and thus high charge-carrier mobility of the CVD-synthesized thin SnS_2 crystals. This novel approach for seeded growth of high quality 2D semiconductor crystal arrays may open a pathway towards integrated optoelectronics applications.

Single-crystal bulk materials of β -PdBi₂ is synthesized by a melt-growth technique. β -PdBi₂ nanoplate is obtained by mechanically exfoliation. Point-contact spectroscopy is a very useful tool for studying superconducting gap structures via Andreev reflection spectrum at normal metal/superconductor junctions. In this dissertation we presents a novel experimental approach to point-contact spectroscopy for nanoplate superconductor and have employed this method to unveil the existence of the two superconducting gaps in β -PdBi₂, which is consistent with the temperature dependencies of the specific heat studied by Imai et al. Energy gaps' dependencies on temperature and magnetic filed are also been studied. This work opens up new opportunity to understand the pairing mechanism and study gap structures in layered superconductors.

To summarize, novel approaches that combined two-dimensional layered semiconductors and superconductors with modern nanofabrication techniques may open up new opportunity to understand the physics of low-dimensional materials and develop next-generation nano-electronics, photonics and energy applications.
Appendix A

Publications, Patent and Conference Participation

A.1 Publication

- "Chemical vapor deposition of thin crystals of layered semiconductor SnS₂ for fast photodetection application", Su, G.; Hadjiev, V. G.; Loya, P. E.; Zhang, J.; Lei, S.; Maharjan, S.; Dong, P.; Ajayan, P. M.; Lou, J.; Peng, H. Nano Letters, 2015, 15 (1), 506-513.
- "Cellular dynamical mean-field theory study of an interacting topological honeycomb lattice model at finite temperature", Chen, Y-H.; Hung, H-H.; Su, G.; Fiete, G. A.; Ting, C. S. *Physical Review B*, 2015, 91, 045122.

- "Novel layered two-dimensional semiconductors as the building blocks for nanoelectronic/photonic systems", Su, G.; De, D.; Hadjiev, V. G.; Peng, H. Proceedings SPIE, 2014,9083, 908304.
- "Electric field effects in ultrathin β-ZrNBr nano-crystals", De, D.; Su, G.; See, S.; Guloy, A.; Ting, C. S.; Peng, H. Applied Physics Letters, 2013, 103, 043107.
- "Multiscale simulation on a light-harvesting molecular triad", Su, G.; Czader, A.; Homouz, D.; Bernardes, G.; Mateen, S.; Cheung, M. S.; The Journal of Physical Chemistry B, 2012, 116 (29), 8460-8473.

A.2 Patent

 "Methods for the synthesis of arrays of thin crystal grains of layered semiconductors SnS₂ and SnS at designed locations ", Haibing Peng, Guoxiong Su, Debtanu De, US2014/0332814 A1, 2014.

A.3 Conference Participation

- Su, G.; Hadjiev, V. G.; Loya, P. E.; Zhang, J.; Lei, S.; Maharjan, S.; Dong, P.; Ajayan, P. M.; Lou, J.; Peng, H. 48th TcSUH Semiannual Fall Student Symposium, Houston, USA, 2014, "Chemical vapor deposition of thin crystals of layered semiconductor SnS₂ for fast photodetection application".
- Su, G.; Peng, H.; Ting, C. S. American Physical Society March Meeting, Denver, USA, 2014, "Multiple Superconducting Gaps in β-PdBi₂ Observed by

Nano-Scale Andreev Reflection Spectroscopy".

Su, G.; Peng, H.; Ting, C. S. 46th TcSUH Semiannual Fall Student Symposium, Houston, USA, 2013, "Multiple Superconducting Gaps in β-PdBi₂ Observed by Nano-Scale Andreev Reflection Spectroscopy". (3rd prize)

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