Design, Fabrication and Characterization of Rubbery Stretchable Transistors

by
Shubham Patel

A thesis submitted to the program of Mechanical Engineering,
Cullen College of Engineering
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE
in Mechanical Engineering

Chair of Committee: Dr. Cunjiang Yu

Committee Member: Dr. Dong Liu

Committee Member: Dr. Xiaonan Shan

University of Houston
May 2020

ACKNOWLEDGMENTS

First and foremost, I would like to thank my research advisor, Dr. Cunjiang Yu for his insight, leadership, and inspiration to be a better researcher and student. Thank you for your continued support throughout my master thesis research as it could not have been completed without it.

Thank you Yongcao Zhang and Hyunseok Shim for your time, effort and guidance during my research. Their expertise in this field were the biggest support to complete my research. I am grateful and thankful.

I would like to thank my lab mates for their great help and guidance during my research. I also would like to express my gratefulness to my friends for their endless support and encouragement and finally I am thankful to my parents for their continuous guidance and support during my research time.

May 7, 2020

ABSTRACT

Stretchable Electronics surpass existing rigid electronics and benefit humans, machines, robots etc. where most of the activities are associated with mechanical deformation and strain. Most of the stretchable electronics are realized by using strategical architectures to realize mechanical stretching of the devices rather than imposing strain directly into the materials. However there have been recent development of stretchable electronics by fabricating them from intrinsically stretchable elastomeric electronic materials i.e., rubbery electronics from scratch. Here, this novel approach of using intrinsically stretchable, rubbery electronic materials to fabricate electronic devices which are stretchable like rubber has been used. Stretchable complimentary organic transistor based inverters were fabricated using rubbery organic semiconducting materials and were tested with and without mechanical stretching and their electrical performances were obtained. It was found that the inverters can function normally even under mechanical stretching. In addition, stretchable rubbery synaptic transistors were investigated which were also fully based on rubbery electronic materials and exhibit synaptic characteristics. These characteristics were retained even when the synaptic transistor had been stretched by 30%

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

In the past few decades, there have been significant technical advances and device development in electronics. With the advancements in nanotechnology, materials science of electronic materials, the electronic components have been miniaturized with nanoscale resolution, thus small form factor [1-5]. The future applications demand extension of electronics in healthcare and wearable format [1]. However, electronic technology developed so far are rigid because they have been fabricated on hard and fragile substrates like silicon and glass. With the fast development of the modern world electronics, the rigid parts can no longer meet the demand of advanced electronics scenario specially when deployed with irregular surfaces, dynamic deformable surfaces and in wearable fashion, where the flexibility and stretchability are needed. "Stretchability" is the key to merge the sensors on to a complex, intrinsic and deformable surface. As a result, electronics that are flexible as films and stretchable as rubber, will soon replace traditional rigid electronics. Future electronics will be highly deformable and will adapt to different shapes by stretching, shrinking or wrinkling as desired. Emerging applications will be realized when new electronics adapt stretchability.

1.1 Background: Stretchable Electronics

Stretchable electronics involves technology in which electronic circuits are made by depositing stretchable electronic devices onto stretchable substrates or embed

them completely in a stretchable material like Polydimethylsiloxane (PDMS). Some of the potential applications of stretchable electronics [3] (figure 1.1) are bio-inspired devices for healthcare monitoring, soft robotics, stretchable displays (figure 1.2) etc.

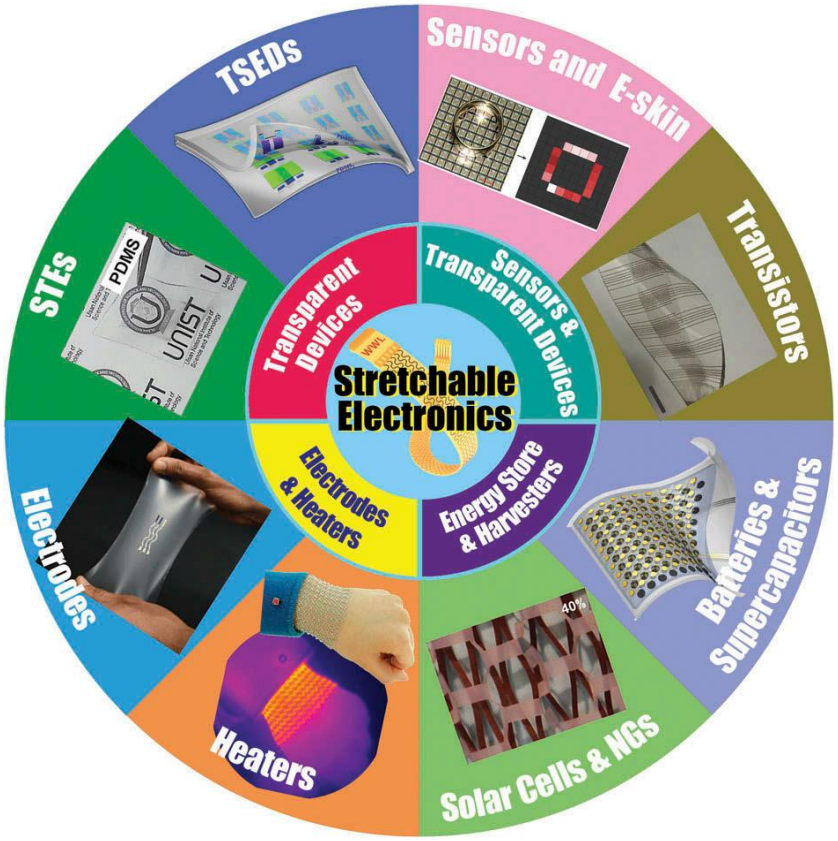

Figure 1.1: Applications of Stretchable Electronics

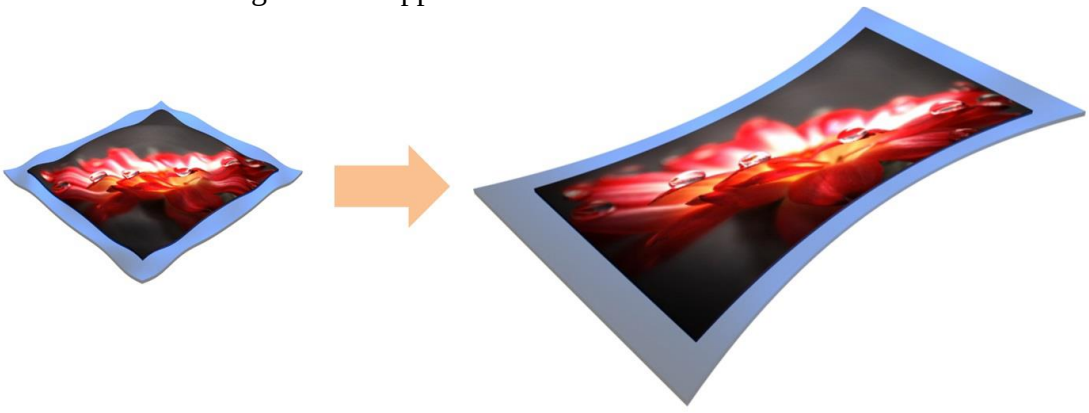

Figure 1.2: Stretchable Display

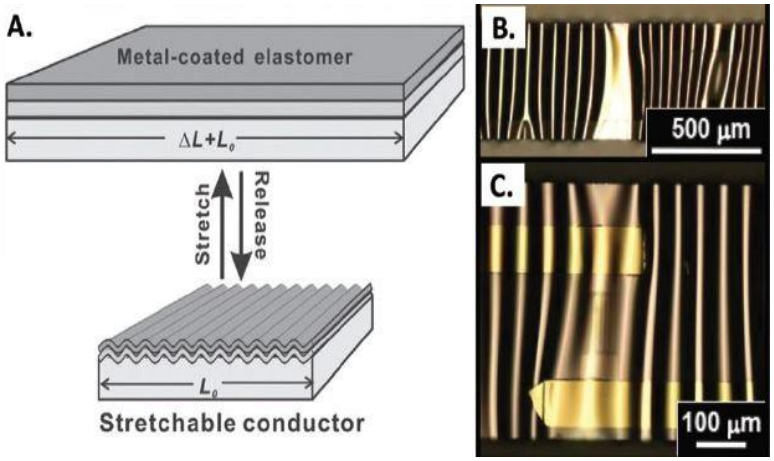

Figure 1.3: Schematic Illustration of development of Buckled Structures through Substrate Stretching [7]

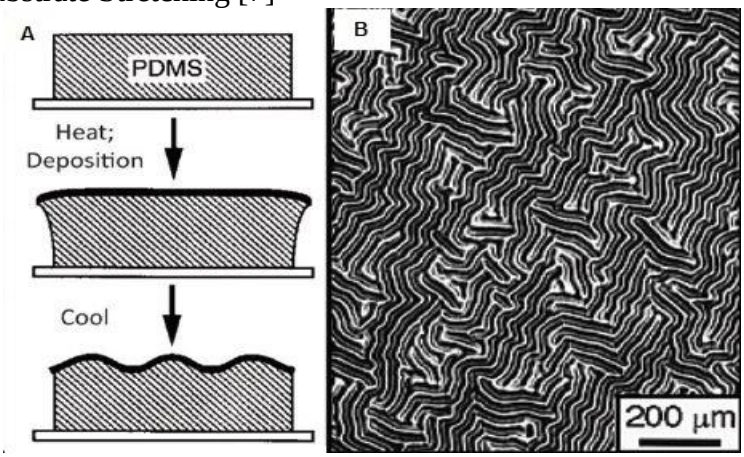

Figure 1.4: Schematic illustration of development of Buckled structures through thermal treatment [7]

Two main ways of achieving elastic properties in stretchable electronics are by using Out-of-Plane stretchable structures and In-Plane stretchable structures. Such structures use specific geometries in order to stretch in a prescribed direction. Such designs allow greater strain by enabling deformation by bending or twisting, thereby keeping local strains small.

Out-of-Plane structures involve structures with 3D configuration. Common examples of such structures are metallic thin films on a pre-stretched substrates that are wrinkled or buckled. To achieve such wrinkled or buckled structures, several techniques

have been devised. One such way is to deposit metal films over pre-stretched flat elastomeric substrate and subsequently release the strain (figure 1.3) [7-10]. Another technique involves the heating and subsequent cooling of metal thin films deposited over a polymeric substrate which cause ordered wrinkled on the film due to difference of thermal coefficient of metal and the substrate (figure 1.4) [7]. When stretched, the buckled substrate will have an initial tendency to flatten which will increase its capacity to withstand higher strains when compared to thin films on a naturally flat substrate.

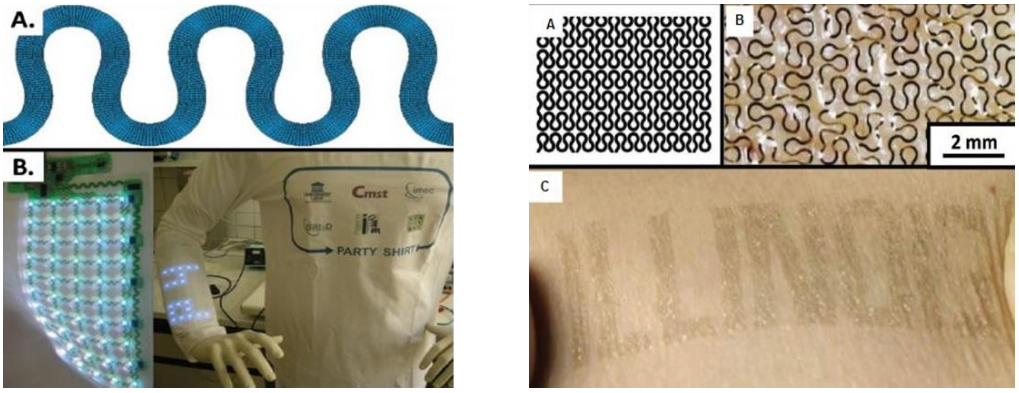

Figure 1.5: Illustration of Serpentine Architecture specifically horseshoe design [7]

In-Plane structures are the structures which are tangent to the planar substrate. The most common example of In-Plane structures are serpentine architectures which are conductive paths deposited over a stretchable substrate that have an in-plane meandering shapes that enables stretching [7]. The horseshoe design is the most common example of such serpentine architecture. Such design have been used in island-bridge structures in which non-stretchable structures were connected via stretchable interconnects of such serpentine architectural designs as shown in figure 1.5 which enables the stretching of devices with non-stretchable parts which are present as like islands.

However, both of the techniques involve structural engineering of electronics and require laborious tools, techniques, they require complex device design, complicated fabrication procedures etc. Recently, an approach of developing intrinsically stretchable electronic materials have been considered to fabricate intrinsically elastic electronic devices i.e., rubbery electronics [11, 12]. These rubbery electronics are those electronics which have high elastic properties like rubber In this approach, intrinsically stretchable electronic materials including stretchable conducting materials for electrodes, semiconductor for active components and dielectric materials have been synthesized and deposited/embedded over a stretchable substrate using conventional thin film deposition techniques. This approach has simple fabrication process and does not require complicated structural engineering for accommodation of strain as compared to the methods discussed previously and is much cheaper.

1.2 Motivation

New emerging applications like soft robotics, wearable healthcare systems etc. where stretchability is a core requirement for proper functioning has given rise to interest in potential new stretchable electronic devices based on intrinsically stretchable semiconductors. Using such semiconducting materials systems, the motivation is to:

1. Develop and investigate transistors technologies based on organic materials which can be the building block of the stretchable organic electronic systems.
2. Investigate the performance of the above stated transistors under mechanical deformations of various strains.

3. Develop stretchable organic inverters and validate that the concept of combining P-channel transistors and N-type transistors into a complementary circuit i.e., inverter.

4. Investigate the performance of the above stated inverter under mechanical deformation

5. To explore a new type of transistor technology inspired from biological computational systems i.e., biological synapse. The biological synapse has high computation speed, very low energy consumption etc. Also investigate this new transistor under mechanical strain.

1.3 Thesis Outline

This thesis include the concept of stretchable electronics with focus on particularly two technology advancements- 1) intrinsically stretchable P-channel and N-channel transistors and organic inverters using combination of P-channel and N-channel transistors, 2) stretchable synaptic transistors.. In chapter two, first an overview of Organic Thin Film Transistors (OTFT) and organic inverters is covered and then the detailed fabrication process has been described. Afterwards the device characterization with and without mechanical stretching is described. In chapter three, first an overview of the biological synapse has been discussed and then how it analogues to synaptic transistor has been described. Then the detailed fabrication process has been described and then device characterization with and without mechanical stretching is described. In chapter four, the thesis has been concluded and potential future works has been described.

CHAPTER 2

STRETCHABLE COMPLIMENTARY ORGANIC INVERTER

2.1 Introduction

Organic electronics has been an interesting field of interest academically and commercially. Most of this interest is due to its low thermal requirements while fabricating these devices and their high degree of mechanical flexibility. These characteristics are due to two basic properties of organic semiconductors:

1. Organic semiconductors enjoy semiconducting properties at a molecular level
2. Bonding between organic molecules can be weak, usually formed by Vander Waals bonds

As no covalent bonds need to be broken or re-formed, organic semiconductor materials can be manipulated using a small energetic input. Printed and evaporated materials can form semiconducting channels on nearly any substrate. No epitaxial growth is required to achieve at least some semiconducting properties, and materials can be engineered to self-assemble into favourable configurations for device performance in low thermal input processes since that assembly is not energetically expensive.

2.1.1 Organic thin Film Transistor (OTFT)

The first OTFT was reported in 1986 that consisted of organic macromolecule, polythiophene as organic semiconducting material for facilitating the flow of electric current [13]. Interest in organic semiconductors began to intensify in the late 80's and

early 90's, in large part because of reports describing OTFTs, an organic heterojunction organic solar cell by Tang in 1986 [14], and organic light emitting diode by Tang and Van Slyke in 1987 [15]. A number of programs were established at academic and industrial research centres to investigate one or more of these device architectures.

An OTFT is composed of a semiconducting film deposited over a channel through which the current flows. At one end of the channel there is an electrode called source and at the opposite side there is a second electrode called drain. The physical dimension of the channel are fixed but the portion of the active material actually available for the conduction of current can be varied by applying a voltage (V_g) to a third electrode called gate. The channel is in contact with a dielectric layer working as a capacitor, and allows current modulation through the gate voltage. The main constituting elements of an OTFT are: three contacts (source, drain and gate), an active semiconducting material and a dielectric layer [16][17]. This whole schematic is shown in figure 2.1. A minimum gate voltage required to collect charge carriers at the organic layer/dielectric layer interface flowing from source to drain is known as Threshold voltage (V_{th}).

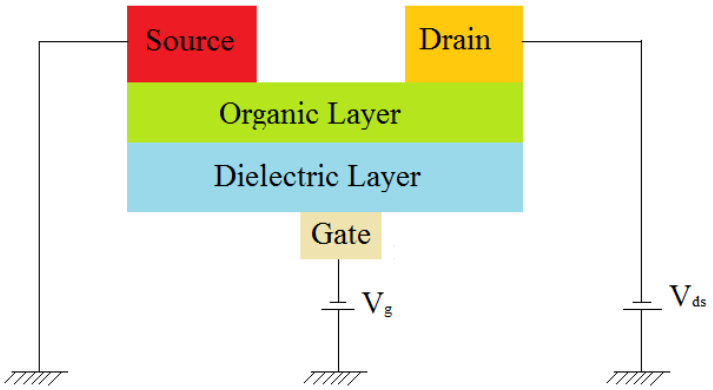

Figure 2.1: Basic schematic of OTFT

At this time, if a small source-drain voltage (V_{ds}<<V_g) is applied between source and drain electrode, the carriers will flow from one side to the other side, resulting a small current in the channel. Nevertheless, before injected carriers become mobile, deep traps should be filled first [18]. For this reason, the effective gate voltage is a deduction of threshold voltage (V_{th}) from V_g. The amount of the current in the channel is proportional to V_{ds}, thus this is called the linear regime of the transistor (figure 2.2 (a) (b)).In such case,the transistor is modeled as a resistor whose resistivity is determined by the mobility and geometrical factors ($\mu\frac{W}{L}$), and the charge carrier density is determined by the capacitance and the applied voltage beyond the threshold ($C_i(V_g-V_{th})$). This gives the current in linear region as:

$$I_D = \frac{W}{L}\mu C_i(V_g - V_{th} - \frac{V_{ds}}{2})V_{ds} \quad (1)$$

where L, W and Ci are the channel length, the width and the generated capacitance per unit area respectively. μ is the field effect mobility. The x-intercept of the extrapolation of the fitted curve was used to find the threshold voltage (V_{th}).

As the drain current is directly proportional to V_g, and the field effect mobility in the linear regime (μ_{lin}) can thus be extracted from the gradient of I_{ds} versus V_g at a constant V_{ds}. This can be defined as:

$$\mu_{lin} = \frac{\delta I_{ds}}{\delta V_g} \cdot \frac{L}{WC_iV_{ds}} \quad (2)$$

If V_{ds} is further enhanced to a point where $V_{ds}=V_g-V_{th}$, the channel will be pinched off. In the meantime, the current in the channel reaches highest. After this point, further increasing of source-drain voltage will not lead to substantial improvement of the drain

current but result in a broaden of depletion region. This is the saturation regime (figure 2.2 (a) (c)).

At this point, current can given as:

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_i(V_g - V_{th})^2 \quad (3)$$

where L, W and Ci are the channel length, the width and the generated capacitance per unit area respectively. μ is the field effect mobility. The x-intercept of the extrapolation of the fitted curve was used to find the threshold voltage (V_{th}).

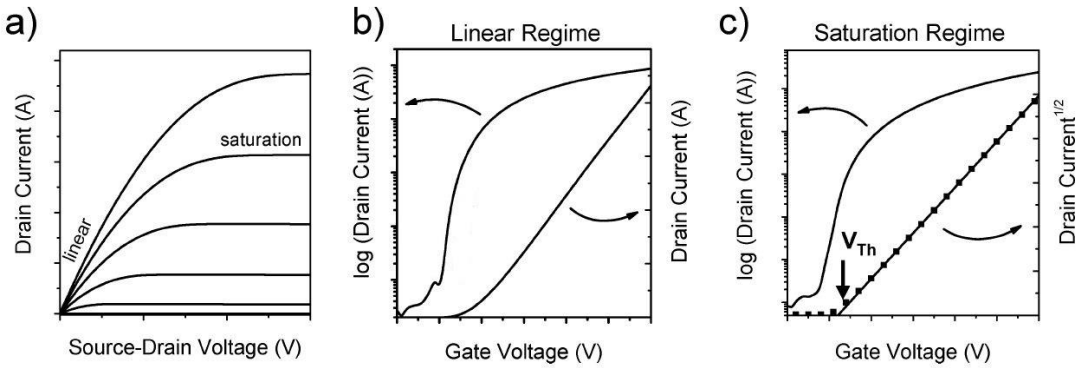

Figure 2.2: Representative current-voltage characteristics of an N-channel OTFT (a) Output characteristics indicating linear and saturation regimes (b) transfer characteristics in the linear regime ($V_{ds} << V_g$) (c) transfer characteristics in the saturation regime ($V_{ds} > V_g - V_{th}$), indicating the threshold voltage V_{th}, where the linear fit to the square root of the drain current intersects with the x-axis

Figure 2.2 (a) shows typical output characteristics (that is the drain current versus source-drain voltage for different constant gate voltages) of a n-channel transistor. From the output characteristics, the linear regime at low V_{ds} and the saturation regime at high V_{ds} are evident.

Figure 2.2 (b) shows the transfer characteristics (that is the drain current versus gate voltage at constant V_{ds}) of the same transistor in the linear regime (V_{ds}, V_g) both as a semilog plot and as a linear plot. The gradient of the current increase in the linear

regime is directly proportional to the mobility according to equation 2 and is constant if the mobility is gate voltage independent. Most semiconductors, however, show gate voltage dependent mobilities, and thus, the curve shape may deviate from being linear.

Figure 2.2 (c) shows a transfer curve in the saturation regime. Here the square root of the drain current should be linearly dependent on the gate voltage, and its gradient is proportional to the mobility according to equation 3. Extrapolating the linear fit to zero yields the threshold voltage V_{th}.

The physical nature of the semiconductor as the well the used gate dielectric may enable different device structures that can show different transistor behaviour. Some of the common used structures are the bottom contact/top gate (BC/TG figure 2.3 (a)), bottom contact/ bottom gate (BC/BG figure 2.3 (b)), top contact/bottom gate (TC/BG figure 2.3 (c)) structures. One of the important differences between these structures is that the position of the injecting electrodes in relation to the gate. In the BC/BG structure, charges are directly accumulated at the interface of the semiconductor and dielectric. Whereas in the other two strucutres,the source/drain electrodes and the channel are separated by the semiconducting layer and hence charges travel through the undoped semiconductor first before reaching the channel.

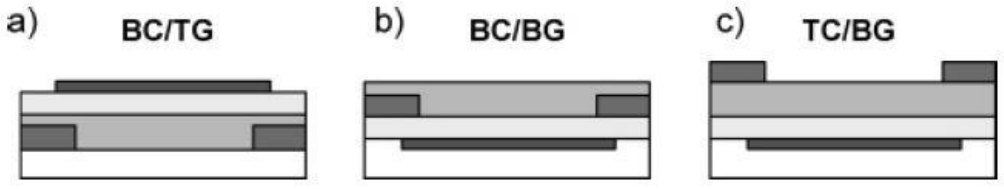

Figure 2.3: Common transistor device structures (a) bottom contact/top gate (BC/TG), (b) bottom contact/ bottom gate (BC/BG) (c) top contact/bottom gate (TC/BG)

Now based on the material used, there are P-channel Thin Film Transistor (TFT) and N-channel TFT. P-channel TFT consists of a P-type film deposited over the channel over which the dielectric is applied. Majority carriers are holes. N-channel TFT consists of an N-type film deposited over the channel over which the dielectric is applied. Majority carriers are electrons.

2.1.2 Complementary Organic Inverter

For the past few years, the research in OTFTs have grown dramatically due to their potential applications in integrated circuits and stretchable displays. One of the major applications of OTFTs is to act as the basic electronic element in complementary digital circuits. The main advantages of such circuits are low-power dissipation, high noise margin, easy circuit design etc. In order to develop such circuits, inverter is necessary to be fabricated first. Till now, one of the major approach to make an organic inverter had been by integrating a P-channel and N-channel transistors which act complementary to each other.

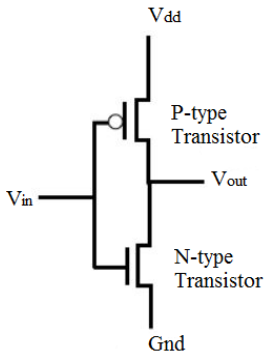

Figure 2.4: Logic Diagram of Organic Inverter

A complementary inverter consist of a P-channel and a N-channel transistor connected at the drain and gate terminals, a supply voltage V_{dd} at the P-channel

transistor source terminal, and a ground connected at the N-channel transistor source terminal, where V_{in} is connected to gate terminals and V_{out} is connected to the drain terminals (figure 2.4).

When a high voltage ($\approx V_{dd}$) is given at input terminal V_{in} of the inverter, the P-channel TFT becomes open circuit and N-channel TFT switched ON so the output will be from ground. When a low voltage (less than V_{dd}, $\approx 0V$) is applied to the V_{in}, the N-channel TFT switches off and P-channel TFT switches ON. So the output becomes V_{dd}. This whole logic is given in table 2.1.

Table 2.1: Organic Inverter Logic Table

Input (V)	**Logic Input**	**Output (V)**	**Logic Output**
0	0	V_{dd}	1
V_{dd}	1	0	0

2.2 Device Design, Methods and Fabrication

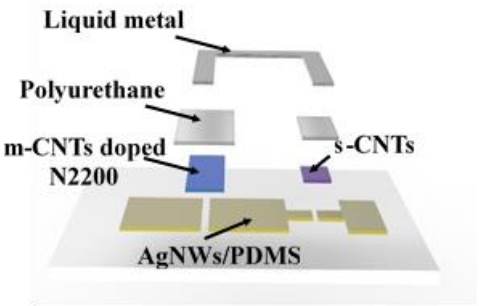

Figure 2.5: Schematic of Stretchable Organic Inverter

The design of the fabricated inverter is shown in figure 2.5. It consisted of AgNWs/PDMS conductor containing two channels. The first channel i.e., top channel of inverter was for P-channel transistor (s-CNTs film) and the second channel i.e., bottom channel of inverter was for N-channel transistor (m-CNTs doped N2200 film).

Over both P-channel and N-channel films, a dielectric film (PU) was present over which the liquid metal was aligned.

2.2.1 Preparation of AgNWs/PDMS Conductor

The AgNWs were patterned on a glass substrate by drop-casting of the solution (AgNWs-120, Zhejiang Kechuang Advanced Materials Co., LTD) through a shadow mask that was prepared by a programmable cutting machine (Silhouette Cameo). The sample was baked on a hot plate at 90°C till the solution got dry. Now the required channels were created by the needle as shown in figure 2.5. PDMS precursor (weight ratio of prepolymer: curing agent is 10:1) was spin-coated on the patterned AgNWs at 300 rpm for 60 s, and then, the sample was cured in the oven at 90°C for 2 hours. The AgNWs was embedded in the PDMS after curing since the relatively high viscosity of the PDMS precursor could penetrate through the network of AgNWs.

2.2.2 Preparation of Polyurethane (PU) Solution

The polyurethane dielectric solution was prepared by dissolving the PU into Tetrahydrofuran (THF) with the concentration of 75 mg/mL at 65℃ for 2 hours.

2.2.3 Preparation of N2200/m-CNTs Composite Solution

The preparation of N2200/m-CNTs composite involved preparing the N2200 solution, m-CNTs suspension and mixing the above solutions with desired ratio. The N2200 was dissolved in the mesitylene (10 mg/mL) at room temperature for 24 hours.

The m-CNTs was dispersed in mesitylene with the concentration of 0.01 mg/mL, 0.1 mg/mL, 0.2 mg/mL and 0.3 mg/mL by applying ultrasonication with consecutive tip sonication for 2 hours and bath sonication for 1 hours. Thereafter, N2200/m-CNTs composite with different m-CNTs contents (0.1, 1, 2 and 3 wt.%) was obtained by mixing the N2200 solution with the pre-prepared m-CNT suspension (0.01 mg/mL, 0.1 mg/mL, 0.2 mg/mL, 0.3 mg/mL) with the volume ratio of 1:1, respectively, followed by 2 hours bath sonication.

2.2.4 Preparation of s-CNTs Solution

The s-CNTs solution was prepared by diluting the bulk solution from 10 μg/mL to 0.1 μg/mL with deionized water.

2.2.5 Fabrication of Stretchable Organic Inverter

The fabrication of the stretchable organic Inverter consisted of 3 parts: preparation of AgNWs/PDMS conductor with source and drain electrodes, creation of semiconductor and dielectric layer and patterning the liquid metal. The s-CNTs channels were UVO treated for 18 minutes followed by treatment with 1% wt. (3-Aminopropyl)triethoxysilane (APTES) solution for 10 minutes. After removing APTES solution, 10 microliters of s-CNTs solution was applied to the channel and then baked at 90^{o}C for 10 minutes followed by cleaning with Deionised water for one minute. The inverter was dried in the vacuum oven at 70 ^{o}C for 1 hour. N-channel semiconductor was prepared in the glovebox in Nitrogen environment. N2200/m-CNTs solution was

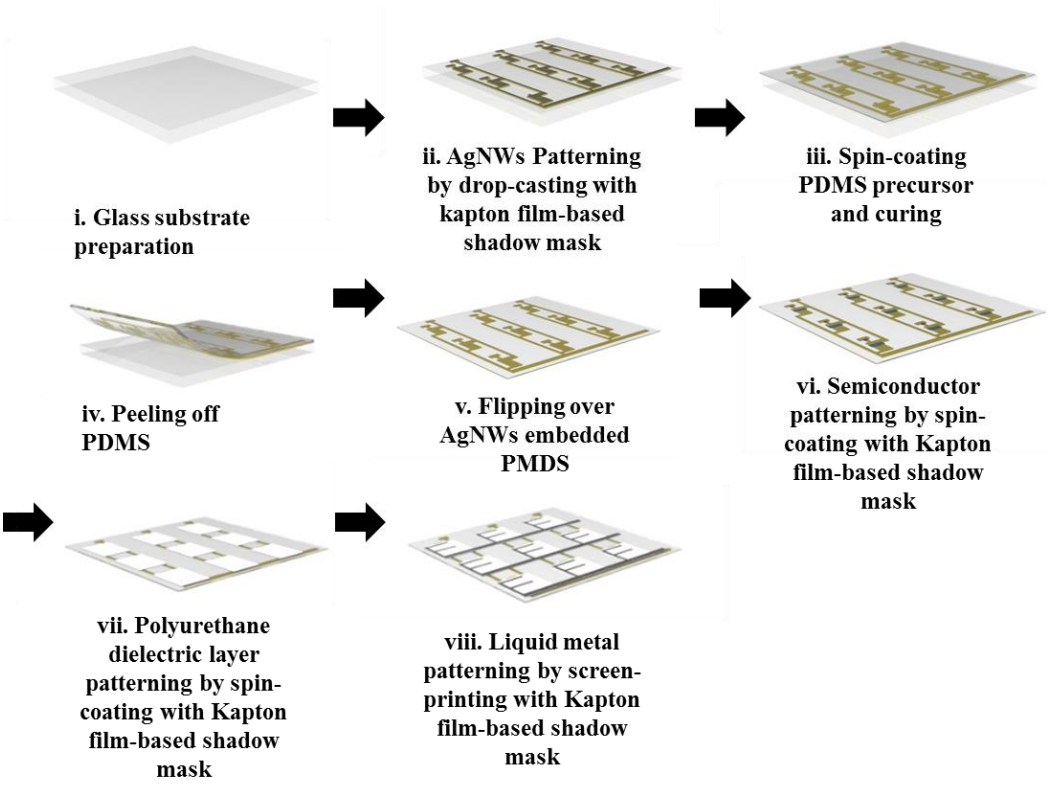

Figure 2.6: Fabrication Process Flow for Organic Inverter

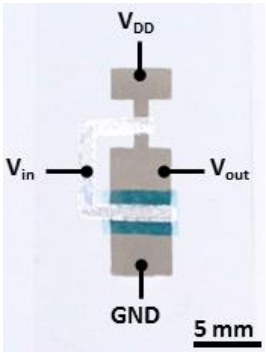

Figure 2.7: Prepared Stretchable Organic Inverter

applied to the n-channel and spincoated at 1000rpm for 60s. After annealing at 150 ^{o}C for 30 minutes, the PU solution was spincoated over both n-channel and p-channel at 1000 rpm for 60s followed by baking at 100 ^{o}C for 60 minutes in Nitrogen environment. Finally to pattern the gate electrode, the liquid metal was aligned and applied through a designed Kapton Film-based shadow mask onto the channel. This whole process flow

has been shown in figure 2.6. The prepared stretchable organic complimentary inverter is shown in figure 2.7.

2.2.6 Device Measurement

The electrical properties of the stretchable complimentary organic inverter were characterized by using semiconductor analyser (4200SCS, Keithley Instruments Inc.). The testing was done at 0%, 10% and 30% strain.

2.3 Results and Discussions

2.3.1 Performance of P-channel and N-channel TFTs

The field effect mobilities were obtained from the output current versus voltage in the saturation region. In this regime, the plot of $\sqrt{I_{ds}}$ versus V_g was fitted and extracted the mobilities from equation (3).

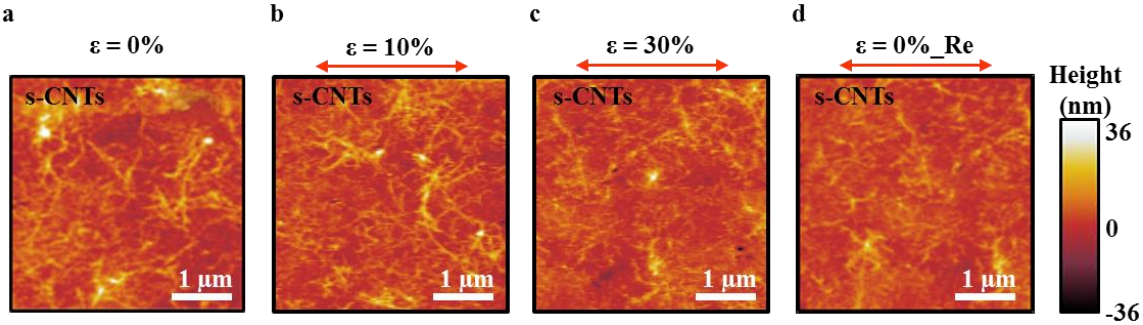

Figure 2.8: AFM image of s-CNTs under mechanical strains of 0, 10, 30 and 0% (released)

Because of the extreme aspect ratio, CNTs are naturally highly curved and entangled in their macroscale assemblies, making them ideal materials for stretchable electronics [19,20]. Here the s-CNTs had been used as a P-channel material for the TFT. As shown in the AFM image (figure 2.8), upon stretching, the entanglements of the s-

CNTs decreases as the strain % increases and even upon the releasing the mechanical stretching, there is little to no recovery of the entanglements of the s-CNTs. This indicates that there is a degradation of the P-channel TFT.

The transfer characteristic of the P-channel (s-CNTs) transistor was measured under various percentage of strains. A V_{ds} of -10 V was given and the input voltage was swept from 0V to -40V and the I_{ds} was measured. Figure 2.9(a) and (b) shows the transfer characteristic of the P-channel TFT under 0, 10, 30 and 0% (released) mechanical strains perpendicular and parallel to channel lengths direction respectively. The μ_{FE} and V_{th} of s-CNTs transistor of stretchable inverter under different levels of mechanical strains had been calculated and plotted and shown in figure 2.9(c).

When the TFT had been stretched from 0% to 30% strain perpendicular to the channel length direction, there was a large decrease in μ_{FE} from 2.29 cm^2/V.s to 0.36 cm^2/V.s and a slight change in V_{th} from -13.49 V to -11.27 V for the P-channel TFT. Upon fully releasing from the mechanical stretching, μ_{FE} recovers slightly to 0.22 cm^2/V.s and V_{th} recovers slightly to -12.18 V. When it has been stretched for the direction parallel to channel length, there is a moderate decrease in μ_{FE} from 2.30 cm^2/V.s to 0.59 cm^2/V.s and slight change in V_{th} from -15.25 V to 14.26 V. Upon release from mechanical stretching, μ_{FE} recover slightly to 0.62 cm^2/V.s and V_{th} slightly recover to -15.06 V. All these show that the degradation of P-channel transistor as shown previously may have caused very low or negligible recovery of μ_{FE} and V_{th} when the mechanical stretching had been released fully.

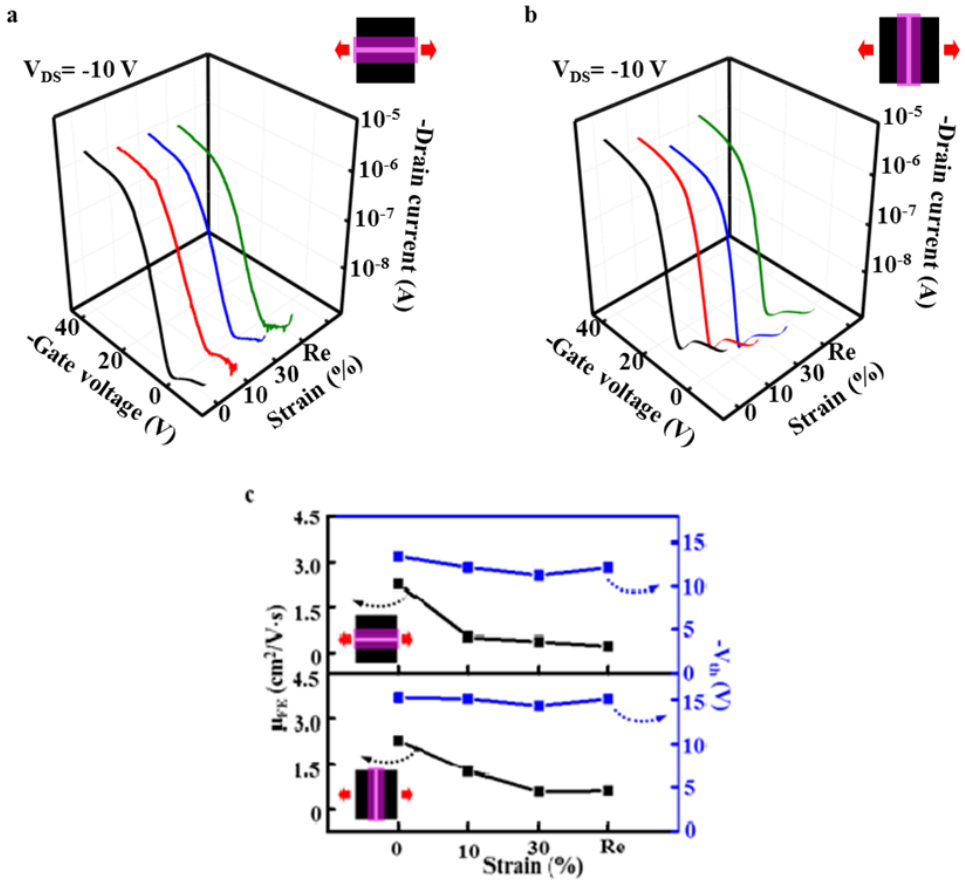

Figure 2.9: Electrical Performance of P-channel TFT part of organic inverters.
(a) Electrical performance when stretched perpendicular to channel length
(b) Electrical Performance when stretched parallel to channel length (c) Field effect mobility vs strain% vs threshold voltage

Here m-CNTs/N2200 had been used as N-channel material. Microcrack mechanism [21] was induced for m-CNTs/N2200 by sandwiching the m-CNTs/N2200 (semiconductor) layer between PDMS and PU as shown in fabrication process. Comparing the m-CNTs/N2200 film with and without PU after stretching, it was observed that the m-CNTs/N2200 film without PU started forming observable cracks when stretched to30% (figure 2.10 (b)) but the m-CNTs/N2200 film with PU didn't form any observable crack as shown figure 2.10 (d). This may have been due to the fact that the adhesion between PU and the m-CNTs/N2200 film improved the ductility by

limiting the localization of strain that was responsible for crack formation [22]. The spincoating also improved adhesion by conformally coating the m-CNTs/N2200 with PU, thus limiting delamination [21]. This may have led to minimum or zero degradation of N-channel film.

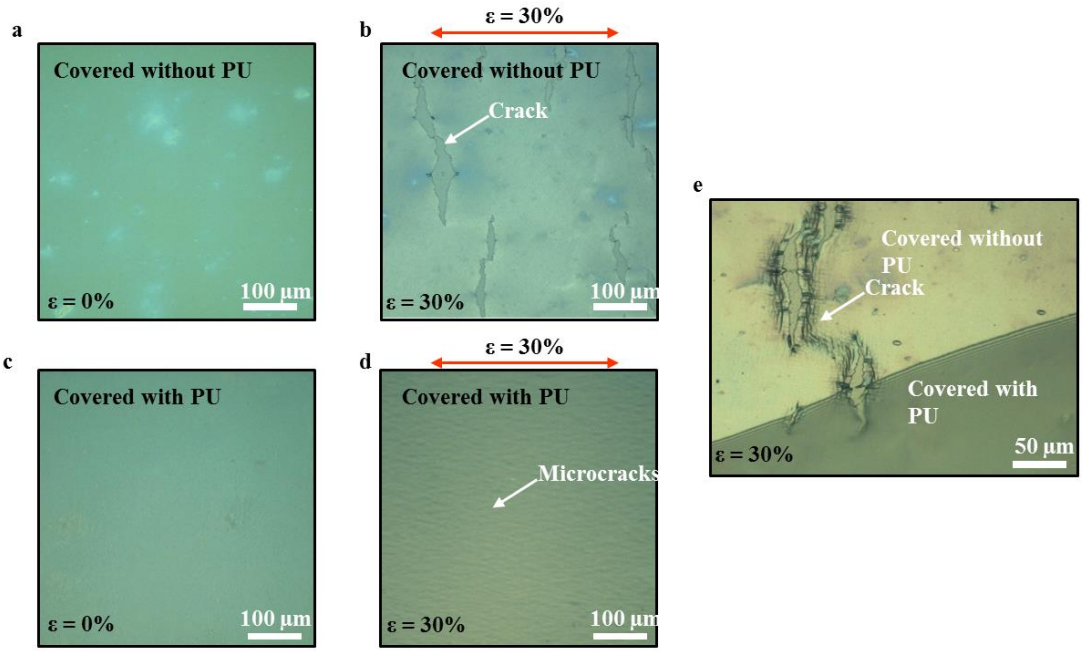

Figure 2.10: Microcrack mechanism for N2200 doped with m-CNTs under strains. (a),(b) Optical microscopic images of N2200 doped with m-CNTs without covering PU dielectric before (a) and after stretching to 30% of strain. (c),(d) Optical microscopic images of N2200 doped with m-CNTs with covering PU dielectric before (c) and after stretching to 50% of strain (e) Optical microscopic images of cracks across the area between area which covers with PU and without PU

The transfer characteristic of the N-channel (m-CNTs/N2200) transistor was measured under various percentage of strains. A V_{ds} of 30 V was given and the input (Gate) voltage was swept from 0V to 40V and the output current was measured. Figure 2.11 (a) and (b) shows the transfer curve of the N-channel transistor of stretchable inverter under 0, 10, 30 and 0% (released) mechanical strains perpendicular and parallel to channel lengths direction respectively. The μ_{FE} and V_{th} of N-channel TFT under

different levels of mechanical strains had been calculated and plotted and shown in figure 2.11 (c).

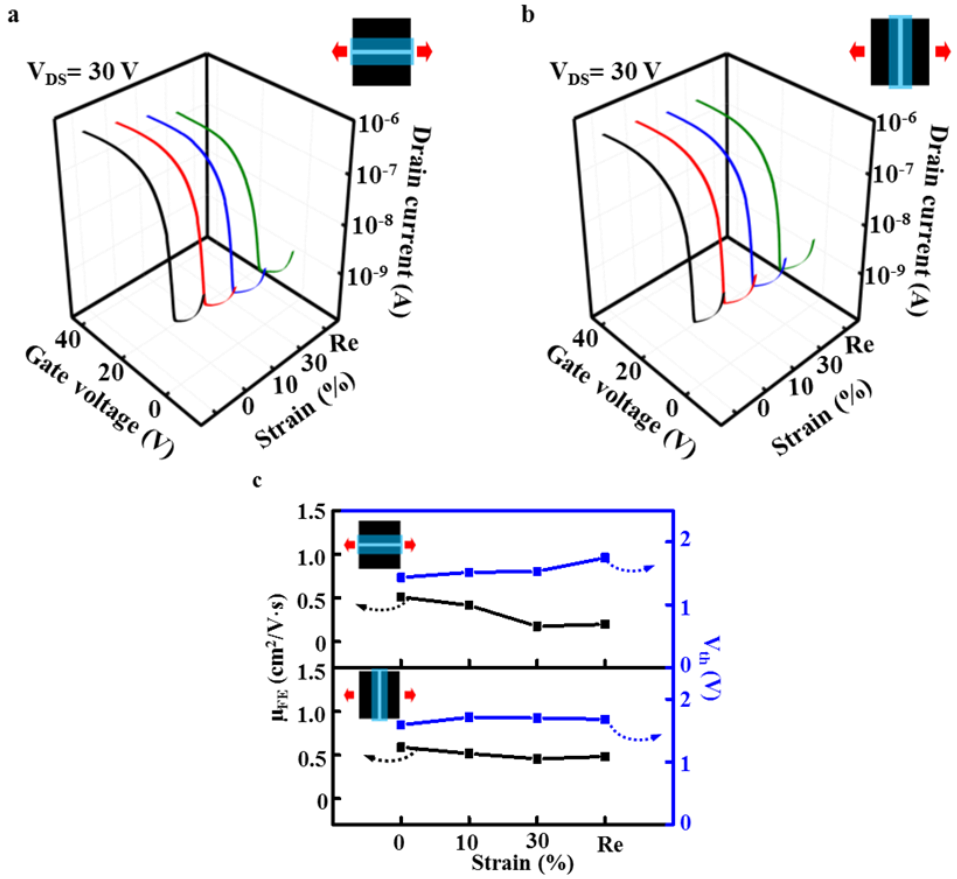

Figure 2.11: Electrical Performance of N-channel TFT part of organic inverters.
(a) Electrical Performance when stretched perpendicular to channel length
(b) Electrical Performance when stretched parallel to channel length
(c) Field effect mobility vs strain% vs threshold voltage

When the N-channel transistor had been stretched from 0 to 30% strain perpendicular to the channel length direction, there was a slight decrease in μ_{FE} from 0.58 cm^2/V.s to 0.45 cm^2/V.s and a slight change in V_{th} from 1.59 V to 1.69 V. Upon fully releasing from the mechanical stretching, μ_{FE} recovers to 0.48 cm^2/V.s and V_{th} changed to 1.67 V. When it had been stretched for the direction along the channel length, there was a moderate decrease in μ_{FE} from 0.50 cm^2/V.s to 0.17 cm^2/V.s and a slight

change in V_{th} from 1.43 V to 1.53 V. Upon release from mechanical stretching μ_{FE} recovered to 0.48 $cm^2/V.s$ and V_{th} changed to 1.67 V. This indicated that N-channel TFT may had less degradation as compared to the P-channel TFT.

2.3.2 Performance of Stretchable Organic Inverter

Now the Voltage Transfer Curve (VTC) (figure 2.12) was measured to find output voltage (V_{out}) under various V_{dd} while the input voltage (V_{in}) was swept from 0 to 30 V. At V_{in} near 0, the P-channel transistor was in closed circuit and the N-channel transistor was in open circuit so conduction took place through the P-channel transistor. So V_{out} was high as seen in figure 2.9. But as the V_{in} increased the P-channel transistor started conducting less and less and ultimately became open circuit. Simultaneously as V_{in} increased, N-channel transistor became more and more closed and ultimately became closed circuit. At that point, conduction was only through N-channel transistor which was a closed circuit and was connected to ground. So conduction was from ground to output with low value as shown in figure 2.11.

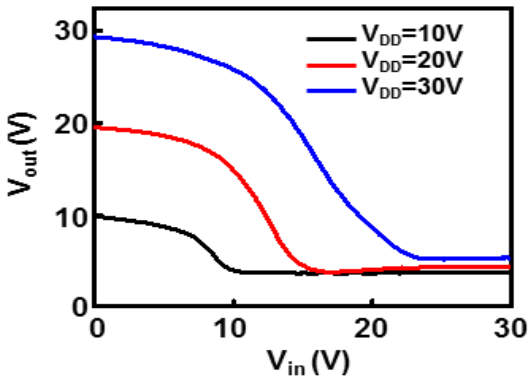

Figure 2.12: Voltage Transfer Curve of the stretchable organic inverter with different V_{DD}

The VTC of the stretchable inverter was measured when it was stretched to various percentage of strains and the voltage transfer curves was obtained for V_{dd} = 10 V under 0%, 10%, 30% and 0%(Released) strain and the strain were applied in both parallel and perpendicular to channel length direction (figure 2.13). Owing to the stretchable nature of the inverter, assumption that stretching induced stain to be evenly distributed across the entire inverter was made.

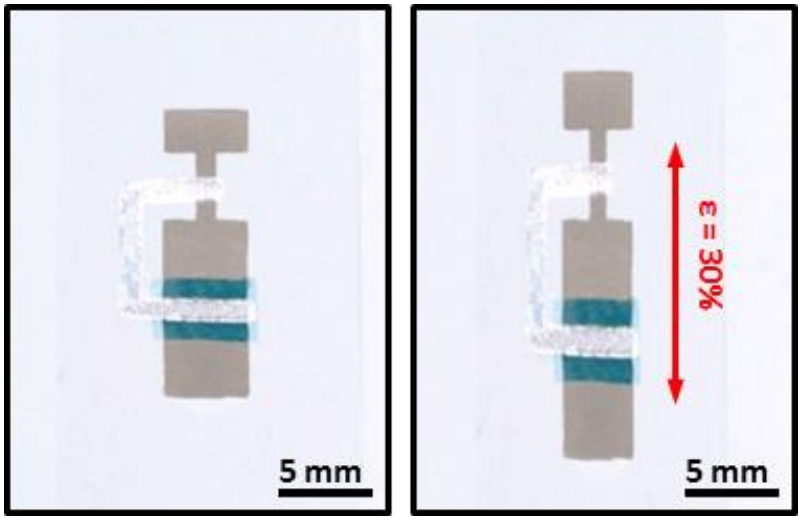

Figure 2.13: Stretching of inverter by 30% Strain in channel length direction

From the voltage transfer curve (figure 2.14) it was found that as the strain percentage increased output voltage decreased for the same sweep of input voltage from 0 to 15 V and as the strain becomes 0 again the output voltage increased back. That was the case for both when strain was applied in a direction perpendicular and parallel to channel length. This was due to the fact that upon application of strain, the p-channel transistor degraded faster than the n-channel transistor.

Now the gain and V_m was calculated and plotted for stretching in both perpendicular and parallel to channel length. The results are shown in figure 2.15.

Switching Threshold voltage (V_m) is defined as the point when V_{in} is equal to V_{out}. This value can be obtained from the Voltage Transfer curve by the intersection of the curve with the line $V_{in} = V_{out}$. In this region, both P-channel and N-channel TFT are saturated.

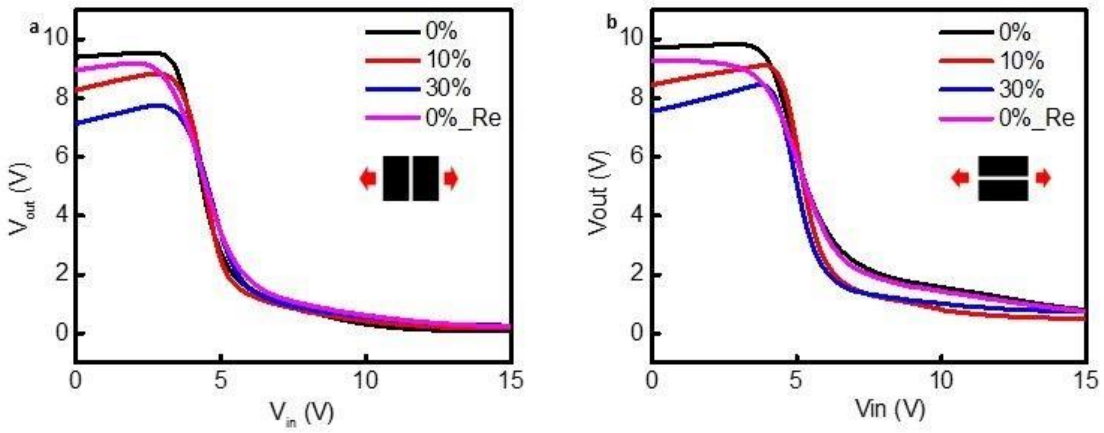

Figure 2.14: Voltage transfer curves under various percentage of strains
(a) Strain applied along channel length (b) Strain applied perpendicular to channel length

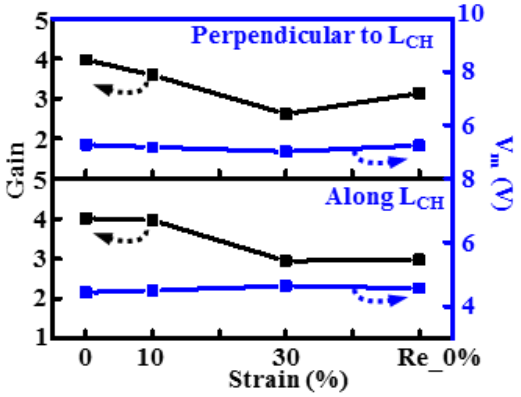

Figure 2.15: Gain vs Strain % vs V_m(V) for organic inverter

As the channel was stretched in a direction perpendicular to channel length, its gain decreased moderately from 4.007 to 2.945 and the V_m changed very slightly from 4.45 to 4.65 V. When the channel was released from mechanical stretching, gain recovered slightly to 2.975 and the V_m recovered slightly to 4.58 V.

As the channel was stretched in a direction parallel to channel length, its gain decreased moderately from 3.968 to 2.614 and the V_m changed very slightly from 5.27 to 5.01 V. When the channel was released from mechanical stretching, gain recovered slightly to 3.312 and the V_m recovered slightly to 5.24 V.

All these results suggest that the organic stretchable inverter can maintain normal operations and relatively stable device performance while under a high level of mechanical stretching.

CHAPTER 3

STRETCHABLE SYNAPTIC TRANSISTOR

3.1 Introduction

There has been lot of progress in developing soft machines, robots etc. which imitates soft animals. But the neurological functions have been little realized in such systems. Synapse are critical biological structure of the neuron which allows the transmission of electrical or chemical signals. Synapses together with neurons are responsible for information flow and processing behind human brain. They consume an extremely small amount of energy, so a human brain consumes only as much energy as a domestic lightbulb requires. The computation done by the human brain is numerous and complex. If such capabilities can be mimicked by computers then it would led to huge advancement in the field of computers when factors such as size, power consumption etc. are considered. Today's computers are bulky in size, consume lot of power and are very expensive. If the potential of the mimicking efforts of the human brain i.e., synapse are fully realized then this can lead to computers which are small in size, have higher speed and will consume low power. Till now most of the result which have been realized by artificial synapse are in the field of pattern recognition [23], parallel processing [24] , neuron-like electronics etc. Also if we are able to realize stretchable artificial synapse, then this can lead to huge advancements in wearable systems. Today's wearable devices are rigid, non-stretchable, uncomfortable etc. If stretchable artificial synapse are realized then this can lead to wearable devices being soft, skin compatible, more flexible etc. This the potential of artificial synapse.

Neurons generate action potentials (spikes) in their soma [25]. The spikes propagate through the axon and are transmitted to the next neuron through the synapses. The synapses transmit the signal by releasing neurotransmitters on receiving signal from the presynaptic neuron. Neurotransmitters diffuse through the synaptic gap and bind to the receptor sites at the post-synaptic neuron. The membrane potential of the post-synaptic neuron increases as it receives more neurotransmitters and if it reaches a threshold, the neuron fires an action potential. This spiking activity generated by neurons and transmitted through synapses is responsible for information flow and processing behind the complex computations performed by the brain [25][26].This whole process has been shown in figure 3.1.

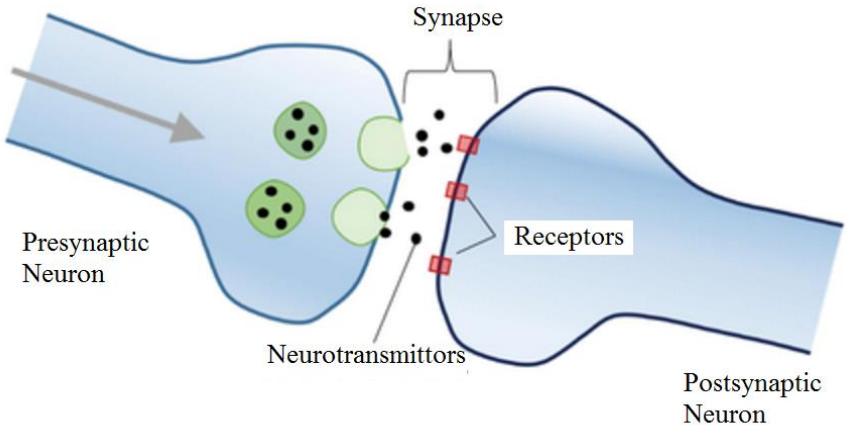

Figure 3.1: Schematic diagram of the deformable synapse and its synaptic transmission

The brain store the information in the form of memories. Those memories can be classified into Sensory Memory (SM), Short Term Memory (STM) and Long Term Memory (LTM) [27]. SM is the shortest term element of the memory. Next comes STM, which is the second stage of the memory. And finally comes the LTM which theoretically can be unlimited. One important characteristic of such synapse is

excitatory postsynaptic current. When a pre synaptic potential fire an action potential it causes the flow of ions (neurotransmitters) to the postsynaptic receptors. This flow of ions is responsible for Excitatory Postsynaptic Current (EPSC).

This understanding of biological synapse and research in advanced materials have led to development of artificial synaptic devices which mimic the biological synapse like Synaptic Transistors. This Synapse and Synaptic Transistor analogy has been well described in figure 3.2 (a), (b) [28] where the gate electrode mimics the presynaptic neuron and source/drain electrodes mimics the post-synaptic neuron. The channel current between source and drain electrodes is regarded as synaptic weight.

Take the case of Synaptic transistor developed by Wan group who had developed a self-learning synaptic transistor [28]. Their concept and schematic diagram has been shown in figure 3.2.

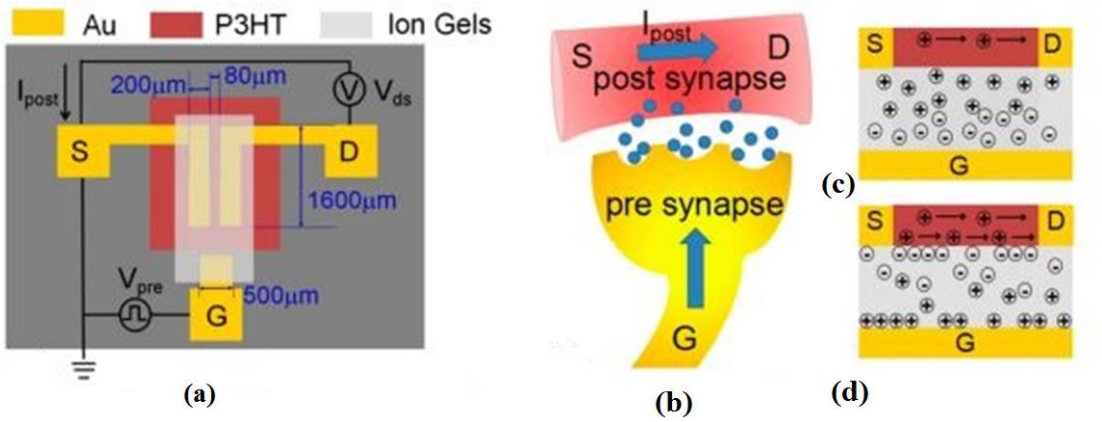

Figure 3.2: (a) Schematic image of P3HT based Organic Field Effect Transistor (OFET) with in-plane gate structure (b) Schematic of artificial synapse based on P3HT-based OFET (c) Schematic of ion-gel gated P3HT transistor at rest state (d) Schematic of ion-gel gated P3HT transistor when Pre-synaptic spike is applied

Wan group presented an artificial synapse based on P3HT-based OFET which mimicked neuromorphic functions. In this synapse, transmission of the information occurred via the motion of ions from presynaptic neuron to postsynaptic neuron. To represent the synaptic strength, a potential spike signal was applied on the presynaptic neuron which triggered the EPSC. In this synapse, mobile ions played an essential role in triggering the EPSC. The conductance of the channel was considered synaptic weight. During the test of the synapse, a constant V_{ds} was applied and there was some initial current. At this stage, most of the negative ions were close to gate electrode (figure 3.3 (c)) and the current of the P3HT channel was small. When a presynaptic spike was applied at gate, ions moved from the ion gel to semiconductor and a double layer was formed at the interface of P3HT film and ion gel and lots of holes were accumulated near the P3HT (figure 3.3 (d)) and a high current (EPSC) passed from source to drain in the channel just produced. When the spike got over, the EPSC decayed to the initial current. This whole behavior is similar to the biological synapse.

Till now, most of the works in synaptic transistors had been focused on P-channel organic synaptic transistors with ion gel as the gate dielectric. But this had some drawbacks. The electrochemical reaction during the device operation caused electrochemical doping of the bulk semiconductor layer often and led to the degradation of the electronic device. To overcome this problem, rubbery polymer dielectric like Polyurethane (PU) which induces hysteresis, can be a good option. A rubbery N-channel organic transistor shows good stretching performance with moderate hysteresis for synaptic behaviors.

3.2 Device Design, Methods and Fabrication

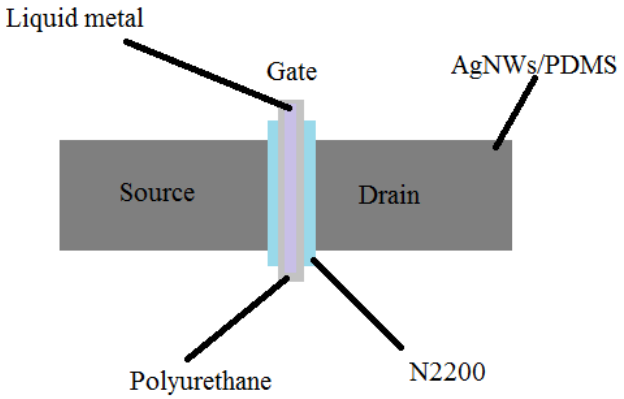

Figure 3.3: Schematic of N-channel Synaptic Transistor

The schematic of the fabricated N-channel synaptic Transistor was shown in figure 3.3. It consisted of AgNWs/PDMS conductor containing one channel. The first layer over the channel was the semiconducting N2200 film. Over which the dielectric layer of Polyurethane was present. Over the dielectric film (Polyurethane), the liquid metal was aligned.

3.2.1 Preparation of N2200 Solution

The preparation of the N2200 solution is done by dissolving the N2200 polymer in Mesitylene (10mg/mL) at room temperature for 24 hours. Then the solution was sonicated for around 30 minutes till the solute N2200 gets fully dissolved in the Mesitylene.

3.2.2 Fabrication of Stretchable Synaptic Transistor

The fabrication of the stretchable synaptic transistor consisted of: preparation of AgNWs/PDMS conductor (as done in chapter 2) with source and drain electrodes,

creation of semiconductor layer and dielectric layer (as done in chapter 2) and patterning the liquid metal. The N-channel semiconducting layer was prepared in the glovebox

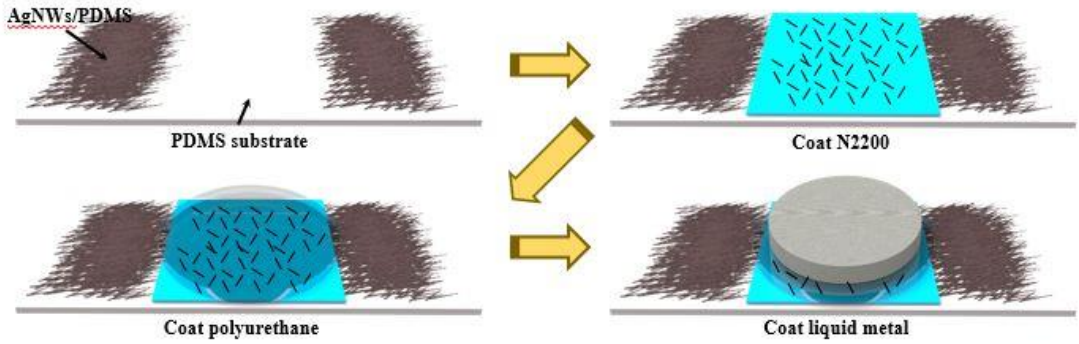

Figure 3.4: Fabrication Process Flow for Synaptic Transistor

under Nitrogen environment. N2200 solution was applied to the channel and spincoated at 1000rpm for 60s. After annealing at 150^{o}C for 30 minutes, the PU solution was spincoated over the channel at 1000rpm for 60s followed by baking at 100 ^{o}C in Nitrogen environment for 60 minutes. Finally to pattern gate electrode, the liquid metal was aligned and applied through a designed Kapton Film-based shadow mask onto the channel. This whole fabrication process flow has been shown in figure 3.4.

3.2.3 Material Characterization and Device Measurements

The frequency dependent capacitance of the PU dielectric was measured by using an impedence analyser (M204, Autolab). The electrical properties of the transistor and synaptic function was characterized by using a semiconductor analyser (4200SCS, Keithley Instruments Inc.). The presynaptic pulse was applied to the gate electrode using a function generator (DG4062, RIGOL Technologies Inc.) and the post synaptic current

was measured by applying a constant V_{ds} between the source and drain using the power supply (1627A, BK Precision).

3.3 Results and Discussions

Firstly the specific capacitance per unit area of the PU dielectric was measured and found to be 0.662nF/cm^2 at a low frequency region and 0.474 nF/cm^2 at 300 kHz. PU is the elastic polymer dielectric that contains hydroxyl group, which results in high concentration of trap sites [29]. To characterize the single pulse-induced EPSC, a pre-synaptic pulse (10V) was applied on the gate with V_{ds} of 10 V. The electrons were collected at the interface between the N2200/m-CNTs and the PU dielectric upon applying the presynaptic pulse. At the end of the pulse, the channel conductance reached

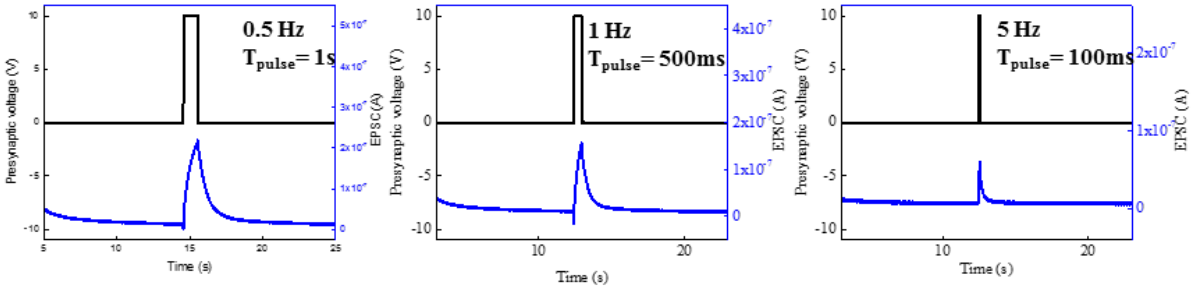

Figure 3.5: Single presynaptic pulse induced EPSC at different frequencies under 0% strain

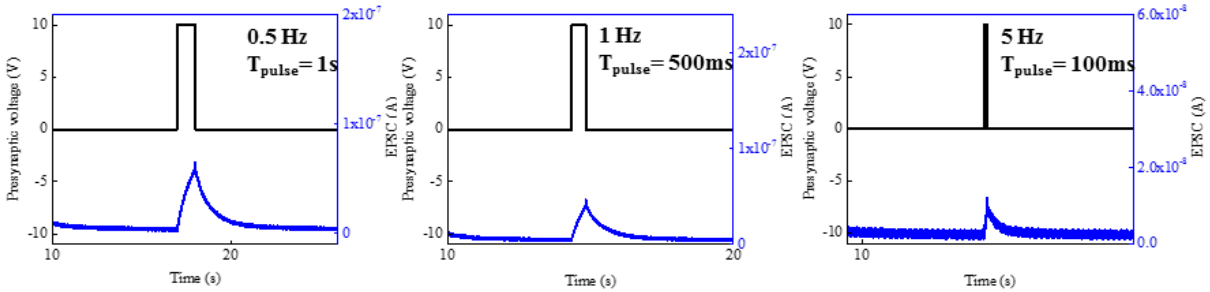

Figure 3.6: Single presynaptic pulse induced EPSC at different frequencies under 30% strain

an equilibrium due to relaxation [30]. The results were shown in figure 3.5. The intensity of EPSC was decreased from 200 to 70 nA depending on decrease in pulse from 1000 to 100ms. Upon stretching by 30% the EPSC decreased as shown in figure 3.6. This was attributed to geometric change in channel.

The EPSC was further tested under two successive presynaptic pulses with Δt_{pre} of two seconds. It was found that the second EPSC peak from second pulse was larger than the peak from first pulse. Even when it has been stretched by 30% it showed similar trend. The required results are shown in figure 3.7 and 3.8.

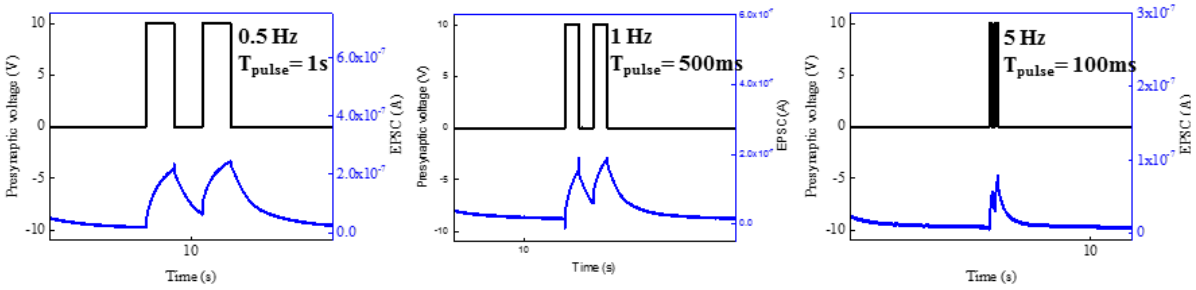

Figure 3.7: EPSC triggered by two successive presynaptic pulses under 0% strain

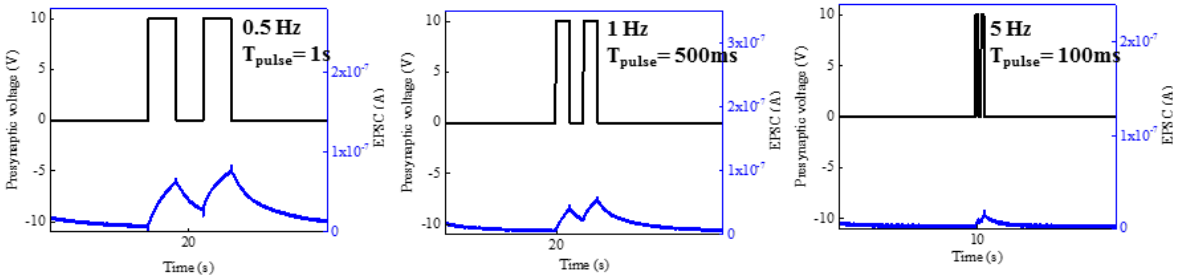

Figure 3.8: EPSC triggered by two successive presynaptic pulses under 30% strain

To characterize the synaptic memory behavior, pulses with frequency of 10 Hz was chosen and a drain voltage of (10 V) was kept for all pulses during the measurement. The transistor was tested with and without strain (30%). Figure 3.9(a) shows the EPSC results for 10 consecutive presynaptic pulses with a width of 50 ms for 0% strain. Figure

3.9(b) shows the EPSC results for 10 successive presynaptic pulses with a width of 50 ms for 30% strain. Also some other synaptic behavior characteristics like SM, STM and LTM existing were observed (figure 3.9) in both cases i.e. at 0% and 30% .This implied that even after application of strain, the transistor retains a significant amount of the original memory (including SM, STM, LTM) hence can function normally even after application of 30% strain.

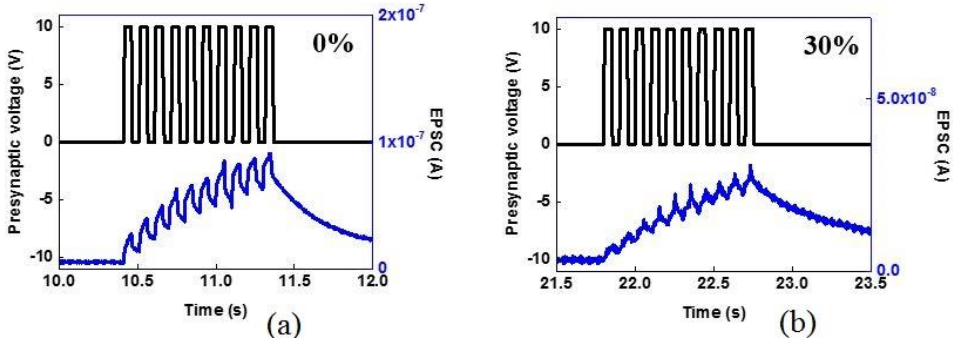

Figure 3.9: EPSC results for 10 successive pulses under (a) 0% strain (b) 30% strain

This type of synaptic transistor has a lot of potential applications like in soft machines, neuroprosthetics [31], soft robots [26] etc.

CHAPTER 4

Conclusion

In this chapter, all the completed work would be concluded and several ideas for potential future work would be proposed.

Through this report, some of the new stretchable inverters and synaptic transistors have been demonstrated which had been fabricated.

The stretchable organic inverters were successfully fabricated by drop casting method and tested for the electrical performance with and without mechanical stretching conditions. The inverters were found to be functioning normally even under 30% stretching conditions. So it can be concluded that organic inverter fabricated by the process described can work normally even in stretched conditions. The fabrication method adopted herein to demonstrate the concept of intrinsically stretchable P-channel and N-channel transistors and thereof the inverter is manual masking, drop-casting and spin-coating and suitable for prototyping and validation. However, for large scale fabrication and commercialization of stretchable electronics using intrinsically stretchable materials, new fabrication steps are required to investigate. The materials demonstrated here have limited mobility, and hence future research will also direct the field to develop high-mobility intrinsically stretchable materials. Logic circuits, operational frequency and power consumption would also be investigated in future while advancement of the technology from contemporary proof-of-concept stage towards high-end product development.

The stretchable synaptic transistors were successfully fabricated by drop casting method and tested for the electrical performance with and without mechanical stretching conditions. The transistors were found to be functioning normally even under 30% stretching conditions. Their memory behavior was also observed and it was found that the devices retained a significant amount of their memory even when they were stretched by 30%. So it can be concluded that stretchable synaptic transistor can work well under mechanical strain conditions. For future work, the performance of the synaptic transistor can be improved more by directing more research in the materials aspect. It has also some potential applications like in Soft robotics, Neuromorphic computing etc.

REFERENCES

[1] Duarte Dias, João Paulo Silva Cunha, "Wearable Health Devices- Vital Sign Monitoring, Systems and Technologies," *sensors,* vol. 18, 1-28, 2014

[2] Wei Zheng, Weicheng Huang, Feng Gao, Huihui Yang, Mingjin Dai, Guangbo Liu, Bin Yang, Jia Zhang, Yong Qing Fu, Xiaoshuang Chen, Yunfeng Qiu, Dechang Jia, Yu Zhou, PingAn Hu, "Kirigami-Inspired Highly Stretchable Nanoscale Devices Using Multidimensional Deformation of Monolayer MoS_2," *Chemistry of Materials,* vol.30, 6063-6070, 2018

[3] Wei Wu, "Stretchable electronics: functional materials, fabrication strategies and applications," *Science and Technology of Advanced Materials,* vol.20, 187-224, 2019

[4] Soyul Kwak, Jihyeon Kang, Inho Nam, Jongheop Yi, "Free-Form and Deformable Energy Storage as Forerunner to Next-Generation Smart Electronics," *micromachines,* vol. 11, 1-25, 2020

[5] Kai Dong, Xiao Peng, Zhong Lin Wang, "Fiber/Fabric-Based Piezoelectric and Triboelectric Nanogenerators for Flexible/Stretchable and Wearable Electronics and Artificial Intelligence," *Advanced Materials,* vol.32, 1-43, 2019

[6] T. Someya, Stretchable electronics, John Wiley & Sons, 2013

[7] Daniel Felix Fernandes, Carmel Majidib, Mahmoud Tavakoli, "Digitally printed stretchable electronics: a review," *Journals of Materials Chemistry C,* vol. 7, 14035-14068, 2019

[8] Yugang Sun, Won Mook Choi, Hanqing Jiang, Yonggang Y. Huang, John A. Rogers, " Controlled buckling of semiconductor nanoribbons for stretchable electronics," *Nature nanotechnology,* vol. 1,201-207, 2006

[9] Jaemin Kim, Mincheol Lee, Hyung Joon Shim, Roozbeh Ghaffari, Hye Rim Cho, Donghee Son, Yei Hwan Jung, Min Soh, Changsoon Choi, Sungmook Jung, Kon Chu, Daejong Jeon, Soon-Tae Lee, Ji Hoon Kim, Seung Hong Choi, Taeghwan Hyeon, Dae-Hyeong Kim, "Stretchable silicon nanoribbon electronics for skin prosthetics," *nature communications,* vol. 5, 1-11, 2014

[10] Sheng Xu, Yihui Zhang, Jiung Cho, Juhwan Lee, Xian Huang, Lin Jia, Jonathan A. Fan, Yewang Su, Jessica Su, Huigang Zhang, Huanyu Cheng, Bingwei Lu, Cunjiang Yu, Chi Chuang, Tae-il Kim, Taeseup Song, Kazuyo Shigeta, Sen Kang, Canan Dagdeviren, Ivan Petrov, Paul V. Braun, Yonggang Huang, Ungyu Paik John A. Rogers, "Stretchable batteries with self-similar serpentine interconnects and integrated wireless recharging systems," *nature communications,* vol. 4, 1-8, 2013

[11] Kyoseung Sim, Zhoulyu Rao, Hae-Jin Kim, Anish Thukral, Hyunseok Shim, Cunjiang Yu, "Fully rubbery integrated electronics from high effective mobility intrinsically stretchable semiconductors," *Science Advances,* vol. 5, 1-10, 2019

[12] Hae-Jin Kim, Kyoseung Sim, Anish Thukral, Cunjiang Yu, "Rubbery electronics and sensors from intrinsically stretchable elastomeric composites of semiconductors and conductors," *Science Advances,* vol. 3, 1-8, 2017

[13] A. Tsumura, H. Koezuka, T. Ando, "Macromolecular electronic device: Field effect transistor with a polythiophene thin film," *Applied Physics Letters*, vol.49, 1210-1212, 1986

[14] C. W. Tang, "Two-layer organic photovoltaic cell," *Applied Physics Letters*, Vol. 48, 183-185, 1986

[15] C. W. Tang, S. A. VanSlyke, "Organic electroluminescent diodes," *Applied Physics Letters*, vol. 51, 913-915, 1987

[16] Gilles Horowitz, "Organic Field-Effect Transistors," *Advanced Materials*, vol. 10, 365-377, 1998

[17] Brijesh Kumar, Brajesh Kumar Kaushik, yuvraj Singh Negi, "Organic Thin Film Transistors: Structures, Models, Materials, Fabrication and Applications: A review," *Polymer Reviews*, vol.54, 33-111, 2014

[18] Jana Zaumseil, Henning Sirringhaus, "Electron and Ambipolar Transport in Organic Field-Effect Transistors," *Chemical Reviews*, vol. 107, 1296-1323, 2007

[19] Le Cai, Chuan Wang, "Carbon Nanotube Flexible and Stretchable Electronics," *Nanoscale Research Letters*, vol. 10, 1-21, 2015

[20] Tsuyoshi Sekitani, Takao Someya, "Stretchable, Large-area Organic Electronics," *Advanced Materials*, vol. 22, 2228-2246, 2010

[21] Alex Chortos , Josh Lim , John W. F. To , Michael Vosgueritchian , Thomas J. Dusseault , Tae-Ho Kim , Sungwoo Hwang , Zhenan Bao, "Highly Stretchable Transistors Using a Microcracked Organic Semiconductor," *Advanced Materials*, vol. 26, 4253-4259, 2014

[22] Nanshu Lu, Xi Wang, Zhigang Suo, Joost Vlassak, "Metal films on polymer substrates stretched beyond 50%," *Applied Physics Letters*, vol. 91, 2007

[23] Sanghyeon Choi, Seonghoon Jang, Jung-Hwan Moon, Jong Chan Kim, Hu Young Jeong, Peonghwa Jang, Kyung-Jin Lee, Gunuk Wang, "A self-rectifying TaO_y/nanoporous TaO_x memristor synaptic array for learning and energy-efficient neuromorphic systems," *NPG Asia Materials*, vol. 10, 1097-1106, 2018

[24] Chaoxing Wu , Tae Whan Kim, Hwan Young Choi, Dmitri B. Strukov, J. Joshua Yang, "Flexible three-dimensional artificial synapse networks with correlated learning and trainable memory capability," *nature communications*, vol. 8, 1-9, 2017

[25] Duygu Kuzum, Shimeng Yu, H-S Philip Wong, "Synaptic electronics:materials, devices and application," *Nanotechnology*, vol. 24, 1-22, 2013

[26] Hyunseok Shim, Kyoseung Sim, Faheem Ershad, Pinyi Yang, Anish Thukral, Zhoulyu Rao, Hae-Jin Kim, Yanghui Liu, Xu Wang, Guoying Gu, Li Gao, Xinran Wang, Yang Chai, Cunjiang Yu, " Stretchable elastic synaptic transistors for neurologically integrated soft engineering systems," *Science Advances*, vol. 5, 1-11, 2019

[27] Takeo Ohno, Tsuyoshi Hasegawa, Tohru Tsuruoka, Kazuya Terabe, James K. Gimzewski, Masakazu Aono, "Short-term plasticity and long-term potentiation mimicked in single organic synapses," *nature materials*, vol.10, 591-595, 2011

[28] Chuan Qian, Jia Sun, Ling-an Kong, Guangyang Gou, Junliang Yang, Jun He, Yongli Gao, Qing Wan, "Artificial Synapses Based on in-Plane Gate Organic

Electrochemical Transistors," *Applied Materials & Interfaces,* vol. 8, 26169-26175, 2016

[29] Yuxin Wang, Xingyi Huang, Tao Li, Liqiang Li, Xiaojun Guo, Pingkai Jiang, " Polymer-Based Gate Dielectrics for Organic Field-Effect Transistors," *Chemistry of Materials,* vol.31, 2212-2240, 2019

[30] Fei Yu, Li Qiang Zhu, Wan Tian Gao, Yang Ming Fu, Hui Xiao, Jian Tao, and Ju Mei Zhou, "Chitosan-based Polysaccharide Gated Flexible Indium-Tin-Oxide Synaptic transistor with Learning Abilities," *Applied Materials and Interfaces,* vol. 10, 1-21, 2018

[31] Yeongin Kim, Alex Chortos,Wentao Xu, Yuxin Liu, Jin Young Oh, Donghee Son, Jiheong Kang, Amir M. Foudeh, Chenxin Zhu, Yeongjun Lee, Simiao Niu, Jia Liu, Raphael Pfattner, Zhenan Bao, Tae-Woo Lee," A bioinspired flexible organic artificial afferent nerve," *Science,* vol. 360, 998-1003, 2018