# AN EMPIRICAL CHARACTERIZATION OF CONCRETE CHANNEL AND MODULATION SCHEMES WITH PIEZO ELECTRIC TRANSDUCERS BASED TRANSCEIVERS

A Thesis

Presented to

the Faculty of the Department of Electrical and Computer Engineering

University of Houston

In Partial Fulfillment

of the Requirements for the Degree of

Master of Science

in Electrical Engineering

by

Sai Shiva Kailaswar

August 2012

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# ABSTRACT

Structural Health Monitoring plays a vital role in improving the safety and maintainability of critical engineering structures. A network comprised of Piezo-electric sensors and actuators has been devised to monitor the condition of concrete structures. A feasible data communication mechanism for sensor networks is needed to ensure effective transmission of information regarding the structural health conditions from sensor nodes to the central processing unit. This thesis work lays the foundation toward designing a communication system using stress waves modulated with information inside concrete structure. The following tasks are essential in designing an effective communication system, namely, i) measurements of concrete channel response, ii) measurements of different modulation schemes, and iii) the design of receiver amplifier based on Automatic gain control technique. The proposed solution utilizes GNU Radio, a software development toolkit to implement different modulation schemes and Universal Software Radio Peripheral to connect the hardware (concrete channel) with software-defined radios.

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# CHAPTER 1. INTRODUCTION

## 1.1 Background

Continuous monitoring of concrete structures is very much essential to prevent any disastrous events. Estimating the condition of structures is quite important after natural hazards such as earthquakes or terrorist attacks. Structural Health Monitoring (SHM) systems are modeled to test the health and performance by continuously monitoring the structures like bridges, dams, buildings, stadiums, platforms, airframes, wind turbines and it goes on. It is the process of invoking the damage detection scheme in concrete structures [1]. Structural health monitoring is playing a vital role in improving the safety and maintainability of critical engineering structures. SHM systems help in detecting the damage with minimal human interaction [2].

As the health of structures gradually degrade over time, continuous monitoring of concrete structures helps in capturing early symptoms of the health decay by comparing key health indicators against previously recorded levels. Real-time structural monitoring gives knowledge of how a structure performs during and immediately after adverse effects helping in making an emergency management to such sudden disasters [3].

Piezoelectric sensors embedded in structures inter-connect to form an integrated network to monitor the concrete structures [4]. A viable data communication scheme for sensor networks is necessary to ensure effective transmission of data from sensor nodes to center processing unit. This is because the status and conditions of the structure must be sent through the sensor network to a center-processing unit to take further necessary actions.

## 1.2 Objectives

The primary objective of this research is to design a feasible data communication system to monitor the concrete structure. Concrete structure embedded with piezoelectric sensors is considered. The designed communication system uses stress waves modulated with information inside concrete structure. The piezoelectric sensors can thus communicate each other and deliver critical information regarding the status of the integrity of the structures.

More specific objectives for this study are detailed below:

- Measurement of concrete channel response is the primary task in designing an effective communication system. This measurement aims to find the suitable frequency band to transmit data through the concrete structure. Function generator and oscilloscope are used to generate the input signal and display the output signal. A data acquisition system was used to collect the input and output signal samples.
- Implementing different modulation schemes for concrete communication to find the capability of concrete channel in transmitting the information through the sensor network in concrete structure. The proposed solution utilizes GNU Radio, a software development toolkit to implement different modulation schemes and universal software radio peripheral to connect the hardware with software defined radios to transmit/receive information.
- To design an automatic gain control (AGC) circuit in the receiver side to stabilize and improve the performance of the system [5]. Software simulation of AGC was done using LTSpice software, and hardware implementation was performed on

breadboard using analog multiplier, op-amps, resistors, and capacitors. ExpressSCH software was used to develop schematic of AGC circuit. This schematic can then be linked to PCB file and ExpressPCB software can be used to develop a printed circuit board of designed AGC.

### 1.3 Structural Health Monitoring using piezoelectric sensors

Embedding sensors in civil structures for structural health monitoring applications require data communication capabilities between sensor nodes in the network [6]. The fundamental feature of embedding piezoelectric sensors in networks for structural health monitoring is their capability for data communication between sensor nodes [7]. Piezoelectric sensors embedded in large structures and inter-connected as a sensor network can be used to monitor structural health of concrete structures. These inter-connected sensors give rise to an integrated network for defect monitoring and ensuring the normal operation of the structure [8]. Data communication between sensors is essential as the present condition and status of the structure must be sent to center processing unit through the network. This helps in taking necessary actions if needed by the human operators. A feasible data communication arrangement for sensor networks is needed to ensure effective transmission of information regarding the structural health conditions from sensor nodes to the central processing unit.

In this research, one such communication system is designed using stress waves modulated with information. The stress waves are modulated using different modulation schemes. This stress waves modulated with information are excited from a transmitter, where these excited signals propagate through concrete channel and are received by the

receiver. The received signals are then demodulated and the information transmitted is recovered. The constellations are recovered for all the modulation schemes implemented showing the capability of data transmission in concrete structure between the sensor nodes.

### 1.4 Overview of thesis

The first chapter gives an introduction to the project and defines the problem statement. The second chapter presents different data communication schemes for structural health monitoring applications. It also gives description about smart aggregate node networks. The third chapter illustrates the communication system design which describes the complete system about how digital data generated from source is converted to analog form in the transmitter side and the analog signal received is converted back into the digital form in the receiver side for further data analysis. The fourth chapter demonstrates the experimental setup used to measure the frequency response of the concrete channel and frequency response considering concrete channel and transmitter amplifier as a channel. The fifth chapter defines the various blocks used in GNU Radio, a software defined radio system to modulate and demodulate the data using different modulation schemes. It also includes the constellations recovered by various modulation schemes illustrating the capability of transmitting data through the concrete channel. It also discusses about various blocks used to calculate Bit Error Rate for various Signals to Noise Ratios for different modulation schemes. The sixth chapter explains about the design of automatic gain circuit for the considered system specifications and limitations. The seventh chapter illuminates the results obtained from the experiments performed.

The thesis is concluded in the eighth chapter by the summary of outcomes and the future work, which is followed by the list of references.

### 1.5 Summary

This chapter illustrates the motivation behind structural health monitoring of concrete structures. This chapter also discusses the importance of piezoelectric sensors and necessity of communication system for monitoring applications. The main objectives for designing an effective communication system using concrete structure embedded with piezoelectric sensors are explained.

# CHAPTER 2. LITERATURE REVIEW

This chapter presents different data communication schemes in sensor networks that use acoustic waves and guided elastic waves for structural health monitoring applications.

## 2.1 Underwater communication scheme

Underwater sensor networks are usually implemented to monitor the health of marine and river environments [10]. Data communication between these nodes is important in sending the status of the structure to the center-processing unit for further analysis. All environments, especially underwater domain cannot support typical wireless sensor model, which utilizes RF as a communication medium [11]. Due to high electromagnetic wave attenuation in water channels and high power consumption to achieve acceptable transmission ranges between nodes, an RF-based communication is not appropriate for underwater communications. As a result, underwater environment has demanded the use of acoustics to enable communication in underwater wireless sensor networks [12]. Table 2.1 shows the comparison of acoustic, EM and optical waves in sea environment [13].

Considering price, power consumption, and network reliability in underwater environment, an acoustic modem is regarded as the best option. Figure 2.1 shows the design of low cost and high efficient acoustic modem [10].

**Table 2.1.** Comparison of acoustic, EM and optical waves in sea environment

| Parameter | Acoustic | EM | Optical |
|---|---|---|---|
| Nominal Speed | ~1500 | ~33,333,333 | ~33,333,333 |
| Power loss | >0.1db/m/HZ | ~28db/1km/100MHz | Propto turbidity |
| Bandwidth | ~KHz | ~MHz | ~10 – 150 MHz |
| Frequency and | ~KHz | ~MHz | ~$10^{14}$ – $10^{13}$ Hz |
| Antenna size | ~0.1m | ~0.5m | ~0.1m |
| Effective range | ~Km | ~10m | ~10 – 100m |

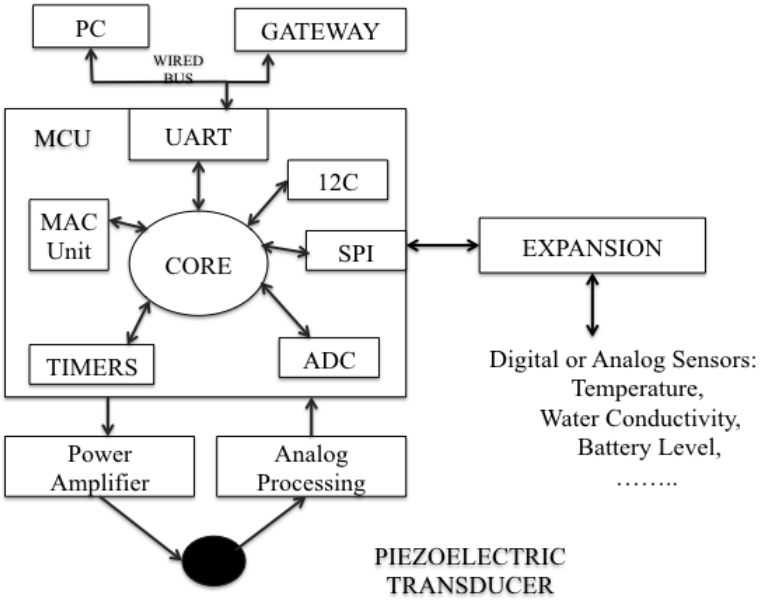


**Figure 2.1.** Acoustic modem architecture diagram

Micro-controlling processing core (MCU) is used in order to obtain optimal power consumption [14,15]. The advantages of the design include

- Low power consumption ranges

- Small packing board design
- Portability
- Low final cost

Micro-core performs the modulation and demodulation algorithms, sensor data reading, data measures processing, and actuators digital interface tasks. Some of the examples of ultra-low power microcontrollers include Texas Instruments MSP430 [16] and ARM Cortex-M0 [17]. Modulation schemes implemented should deal with low consumption and bandwidth. Implementing multi-level modulations like QPSK, M-PSK can increase the bandwidth efficiency [18, 19 and 20]. The demodulation can be accomplished by a phase-locked loop (PLL) as shown in Figure 2.2

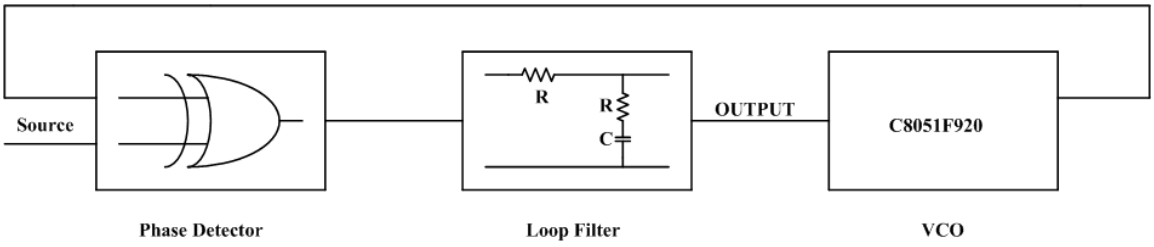


**Figure 2.2.** PLL for demodulation

A power amplifier is used to amplify the modulated signal to transmit the acoustic wave through the water channel and to achieve reliable communication ranges. A piezoelectric transducer is used to transmit/receive various signals in the sensor network. Due to attenuation in water, the acoustic wave under goes analog processing before being demodulated. It amplifies the converted electric signals. An expansion block acts as an interface to both digital and analog sensors. Finally, this micro-controller communicates with the host system through a wired bi-directional bus.

This communication system is designed to underwater sensor network deployment, which focuses on two factors namely low cost and low power consumption using piezoelectric transducers to transmit/receive acoustic signals in water channel.

### 2.2 Data communication scheme using guided elastic waves

Unlike conventional data communication technologies that use Electromagnetic radio waves or acoustic waves, the proposed method [8] makes use of guided elastic waves for structural health monitoring applications.

Guided waves are the waves that travel along a rod, tube, pipe, or plate-like structure that are formed as a result of interaction between ultrasonic excitation signals propagating in a medium and the medium's boundaries. Pipe waves are guided waves when propagating in pipes or thin cylindrical cells [22, 23]. The proposed method utilizes elastic waves as message carriers and steel pipes as transmission channels.

They are three fundamental difficulties when guided waves are utilized for data communication or pipe inspection or monitoring. They are dispersion, multi-mode, and ambient noise.

A. Dispersion

Dispersion referred as multipath propagation in communication theory cause signal time spreading, phase, and frequency shift. These frequency shifting and time spreading result in destructive interference, which causes signal attenuation, and results in poor performance in many stages of communication flow at the receiver including synchronization, signal detection, demodulation, etc. These elastic signals are highly dispersive in nature.

B. Multi-mode

Pipe waves are characterized by an infinite number of dispersive longitudinal and torsional modes and a doubly infinite number of flexural modes [24]. The longitudinal and torsional modes are both axisymmetric while each flexural mode exhibit an infinite number of non-axisymmetric circumferential mode orders [25, 26]. Proper selection of wave modes is needed and is critical for signal transmission.

C. Ambient noise

The addition of random signal of specific mean and variance to the propagating signal is known as noise. The presence of noise reduces the signal-to-noise power ratio resulting in poor performance for signal detection at the receiver. This ambient noise can be reduced using adaptive filtering methods.

These are the problems associated with elastic waves when used for propagation in pipes. These characteristics of guided elastic waves make it difficult to understand the channel response or exchange of structural information data along pipes.

The system being proposed developed a time reversal based guided elastic wave communication scheme. To compensate the signal and channel dispersion in the communication system design, time reversal based pulse position modulation (TR-PPM) method was utilized. Time reversal is an adaptive waveform transmission scheme that implements iterative probing and learning from the returned sensing signals based on the interaction of the sensor and the environment [8]. This leads to enhanced signal detection.

Three-step laboratory tests are performed using piezoelectric transducers in a pitch-catch mode. The first one is to measure channel response between the transmitter and receiver on a pipe. The second one is to perform time reversal transmission by reversing the sounding signal and feeding it back to the same channel. The third one is to perform the time reversal communication experiment by sending the modulated time reversals signals as a stream of binary bits at a given data rate.

The experimental results demonstrated that time reversal Pulse Position Modulation (PPM) can effectively overcome dispersion of guided elastic waves; achieve signal synchronization, and thus achieving data communication through steel pipes successfully using guided elastic waves.

### 2.3 Smart aggregate node networks

Piezoelectric health monitoring systems use piezoelectric transducers to monitor the structural health of concrete function as one actuator with many sensors [21]. These actuators and sensors form a sensor network to give a fully automated system.

The two major problems should be taken into consideration are high attenuation of electromagnetic wave propagation in concrete [27] and high power consumption depending on the radiated power of the antenna. They are many techniques to overcome these problems.

The goal of this research is to design a communication system using a different method of communication with the smart aggregate system, namely modulated stress wave communication. This method makes use of stress waves generated by exciting the piezoelectric transducers with high voltage sinusoidal or modulated waves with

information for communication between transmitter and receiver. Overview of the communication system designed to monitor the concrete structure is discussed in the following chapter.

## 2.4 Summary

Various data communication schemes are possible in sensor networks. Some of them are discussed in this chapter using acoustic waves and guided elastic waves for communication. The problems associated using these waves for propagation and the solutions to overcome these problems to form a successful data communication scheme are demonstrated.

# CHAPTER 3. OVERVIEW OF COMMUNICATION SYSTEM DESIGN

A feasible data communication arrangement for sensor networks is needed to ensure effective transmission of information regarding the structural health conditions from sensor nodes to the central processing unit. This thesis work lays the foundation toward designing a communication system that uses stress waves modulated with information inside concrete structure. The following tasks are essential in designing an effective communication system, namely, i) measurements of concrete channel response, ii) measurements of different modulation schemes and iii) the design of receiver amplifier based on Automatic gain control (AGC) technique.

This chapter discusses the overview of the communication system designed to monitor the concrete structures.

## 3.1 Concrete Structure

The dimensions of the concrete structure used and the placement of the piezoelectric transducers are shown in Figure 3.1. The structure shown in Figure 3.1 is analyzed by checking the outer cables to which piezoelectric transducers (PZT) were attached. The name of the concrete structure is assigned as CS, and the PZT's are assigned with the numbers as shown in the Figure 3.1. For example, the right most PZT is named as CS-4. Every PZT can act as actuator and sensor.

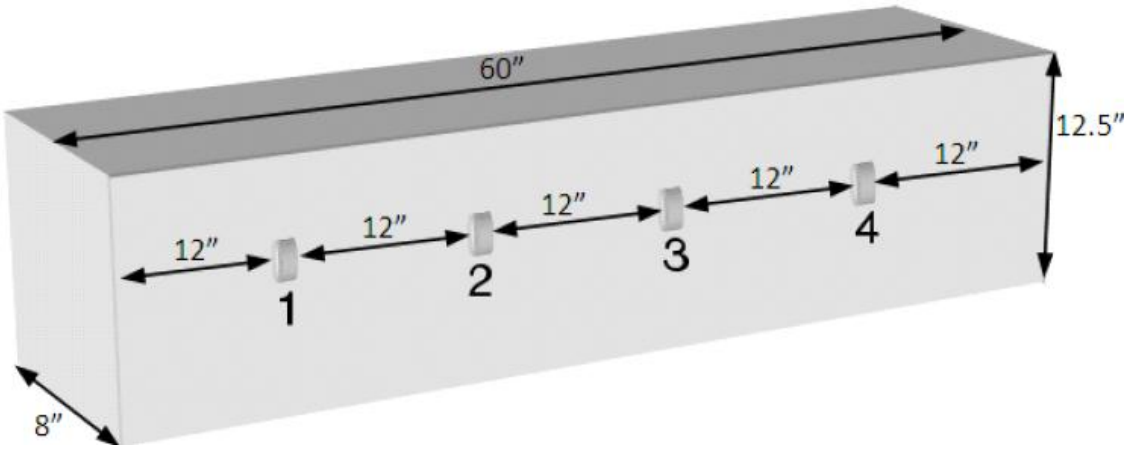


**Figure 3.1.** Concrete Structure configurations

### 3.2 Piezoelectric sensors

A sensor is the device that identifies changes in the ambient conditions. It measures any physical quantity and converts it into a signal, which can be used for further processing. Sensors aid in detecting the present health of the system. A sensor's sensitivity is the minimum input of physical parameter that will create a detectable output change. If the sensor sensitivity is high, then it can respond to a very small change in the system.

A transducer is a device that transfigures the energy from one form to another. A piezoelectric sensor embedded in the structure measures the change in strain, acceleration, and force experienced by the structure. A piezoelectric transducer (PZT) is a device that includes a piezoelectric sensor to sense the mechanical change encountered by the structure and converts the mechanical energy to electric energy such as voltage signal and also converts the electric energy to mechanical energy while transmitting. A piezoelectric transducer can also be used for communication as it utilizes a form of active sensing.

Piezoelectric materials are very light weight, inexpensive, has fast response and solid-state actuation [9]. Piezoelectric transducer is very delicate and is easily deteriorated by the vibrator during the casting of concrete structure. In order to prevent this, a piezoelectric patch is first applied with an insulating coating to prevent water and moisture damage and then inserted into a cubic concrete block to form a smart aggregate. This smart aggregate can be inserted at the desired position in a concrete structure before casting.

**Figure 3.2.** Smart Aggregate

Figure 3.2 shows the smart aggregate that is embedded into the concrete block shown in Figure 3.1

The piezoelectric material generates electric charge when subjected to a stress or strain. The piezoelectric material also generates the stress or strain when an electric field is applied to a piezoelectric substance in its poled direction [9]. This property made piezoelectric material to act as both an actuator and a sensor.

Distance between the piezoelectric actuator and piezoelectric sensor has a relation where the longer the distance between actuator and sensor, the weaker the received signal is. In this research, the piezoelectric transducers are embedded in the concrete structure at a fixed distance.

### 3.3 Universal Software Radio Peripheral

Universal Software Radio Peripheral (USRP) is designed to allow general-purpose computers to function as high BW software radios. It serves as a digital baseband and IF section of a radio communication system. USRP does all the waveform specific processing, like modulation and demodulation on the host CPU [29]. USRPs connect to a host computer through a high-speed USB or gigabit Ethernet link that is used by the host-based software to control the USRP hardware and transmit/receive data. USRPs with GNU Radio software suite create complex software-defined radio systems.

A motherboard of the USRP includes the following subsections: clock generation, synchronization, FPGA, Analog-to-digital converters, Digital-to-analog converters, host processor interface, and power regulation. All the High-speed general-purpose operations like digital up and down conversion, decimation and interpolation are done on FPGA. These basic components are used for baseband signal processing.

USRP has many products, which include USRP N200, USRP N210, USRP1, USRP B100, USRP E100, USRP E110, and USPR2. USRP1 is recommended for applications that do not require higher bandwidth and dynamic range. Considering bandwidth and dynamic range, USRP2 is preferred to USRP1. This project uses USRP2, which has a Gigabit Ethernet interface and can transfer 50 MS/s of complex, baseband

samples to/from the host. USRP2 uses a dual 14-bit, 100 MS/s ADC and dual 16-bit, 400 MS/s, DAC. It contains a Xilinx Spartan 3-2000 FPGA and a SD card reader.

USRP2 was not intended to replace USRP1, where USRP1 uses USB interface to transfer samples to the host and receive samples from the host. Table 3.1 shows the difference between USRP1 and USRP2.

**Table 3.1.** Differences between USRP1 and USRP2

| | USRP1 | USRP2 |
|---|---|---|
| Interface | USB 2.0 | Gigabit Ethernet |
| FPGA | Itera EP1C12 | Xilinx Spartan 3 2000 |
| RF Bandwidth to/from host | 8MHz @ 16bits | 25 MHz @ 16bits |
| Cost | $700 | $1400 |
| ADC Samples | 12-bit, 64 MS/s | 14-bit, 100 MS/s |
| DAC Samples | 14-bit, 128 MS/s | 16-bit, 400 MS/s |
| Daughterboard capacity | 2 TX, 2 RX | 1 TX, 1RX |
| SRAM | None | 1 Megabyte |
| Power | 6V, 3A | 6V, 3A |

USRP2 added the following new features

- 1 MByte of high-speed SRAM.
- Locking to an external 10 MHz reference.
- 1 Pulse Per Second (PPS) input
- Configuration stored on standard SD cards
- Standalone operation
- Capability to lock multiple systems to perform MIMO operations.

- Compatibility with the same daughter boards as the original USRP.

Figure 3.3 shows the USRP2 motherboard.

**Figure 3.3.** USRP2 motherboard

In the first step in the receiver path, the analog to digital converter connected to USRP FPGA converts the received signal into digitized samples. USRP FPGA configuration includes digital-down conversion in the receive path to translate the signal into the baseband and decimate the data as required. This Digital-Down Conversion (DDC) is implemented with 4 stages cascaded integrator-comb (CIC) filters. They are high performance filters using only adders and delays. In the DDC stage, it first down converts the signal from the IF band to the baseband and then it decimates the data. This data is sent to the host computer via Ethernet.

In the transmit path, the exact inverse is performed. The baseband I/Q samples are sent to the USRP board. Digital Up Conversion (DUC) interpolates the signal and converts it to the IF band and finally sends it through the digital-to-analog converter.

### 3.4 Daughterboard

A modular front-end called a daughterboard is used for analog operations such as up/down conversion, filtering and other signal conditioning. Daughter boards allow USRP to perform applications that operate between DC to 6 GHz. They are three classes of daughter boards: transmitters, receivers, and transceivers

- Transmitter daughter board modules can modulate an output signal to a higher frequency.
- Receiver daughter board modules can acquire an RF signal and convert it to a baseband.
- Transceiver daughter board modules combine the functionality of a transmitter and receiver daughter board.

In this project, one Low Frequency Transmitter (LFTX) daughter board and one Low Frequency Receiver (LFRX) daughter board with a frequency range of DC – 30 MHz and maximum input/output of ± 1V are used in the transmitter and receiver side respectively.

### 3.5 Organization of the Communication system

Figure 3.4 shows the overview of the implemented communication system. Universal Software Radio Peripheral (USRP) hardware connects to the computer using Gigabit Ethernet link or USB.

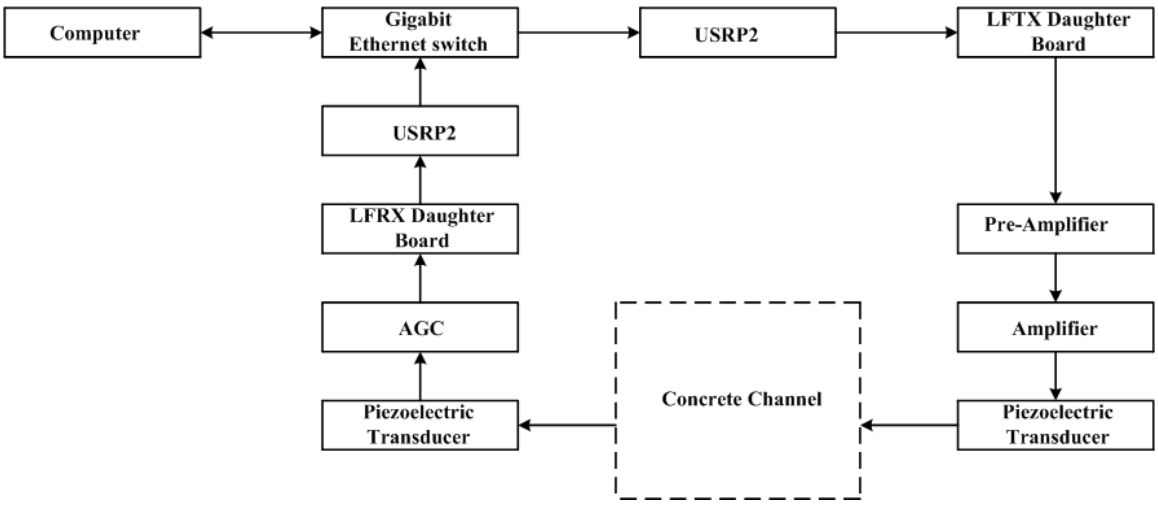


**Figure 3.4.** Communication system design

In our experiments, USRP2 with Gigabit Ethernet switch is used to connect to the host computer. This connection connects the host computer to USRP, where USRP is used to transmit and to receive the signals from hardware. The host computer uses GNU radio, an open source software development kit that provides signal-processing blocks to implement software-defined radios.

The digital signals received by USRP from computer are up converted using FPGA and converted into analog signals using Digital to analog converter. USRP uses daughterboard to transmit and receive the analog signals from hardware. This daughter boards are designed based on the frequency range to be used and many other like power input/output options etc. In the experiment, Low frequency transmitter (LFTX) and Low frequency receiver (LFRX) daughter boards with a frequency range of DC – 30MHz and maximum input/output of ±1V are used.

On the receiver side, USRP receives the analog signal from hardware, converts into digital signal using Digital-to-analog converter, down converts it, and transmits it to

the computer using the Gigabit Ethernet switch. The received digital signal in computer is processed using the GNU radio signal processing blocks.

The purpose of the transmitter amplifier is to drive the piezoelectric transducers, which are commonly high capacitive loads that can be difficult to drive with good stability and settling time. The transmitter amplifier used in this project is Trek 2205 Piezo driver/power amplifier. It has a DC voltage gain of 50 V/V, large signal bandwidth of DC to greater than 75 KHz and small signal bandwidth of DC to greater than 100 KHz. It has an input voltage range from 0 to ±10V DC or peak AC.

The ± 1V (2Vpp) signal from the LFTX daughter board can be fed into the transmitting amplifier with a gain of 50 V/V, which results in ±50 V (100 Vpp) signal into the piezoelectric transducer. In order to increase the signal to noise ratio (SNR) and enable the system to utilize the full range of the driving amplifier, the pre-amplifier is used to output up to ±5V (10 Vpp) signal from the LFTX daughter board. The generated high voltage signal from the transmitter amplifier is used to excite the piezoelectric material to generate stress or strain inside the structure.

The receiving amplifier should have a high input impedance and low output impedance in order to be compliant to the 50Ω and ±1V LFRX input. One such amplifier is designed based on the Automatic gain control (AGC) logic, which is discussed in chapter 6.

This chapter demonstrates the overview of the communication system to monitor the structural health conditions of concrete structure. To implement such communication system, information about frequency response of the structure being monitored is

important. The experimental setup to realize the response of concrete structure is discussed in the next chapter.

### 3.6 Summary

A viable data communication scheme for sensor networks is needed to assure effective transmission of information regarding structural health conditions from sensor nodes to the central processing unit. This chapter illustrates the communication system designed using stress waves modulated with information. Universal software radio peripheral was used to connect the hardware and software-defined radios. Organization and working of communication system using daughter boards, pre-amplifier, transmitter side amplifier and automatic gain control circuit on the receiver side is demonstrated.

# CHAPTER 4. MEASUREMENT OF CONCRETE CHANNEL RESPONSE

The elementary task in designing the effective communication system is finding the concrete channel response. Concrete channel response assists in finding the suitable spectrum to transmit the information through concrete. This chapter discusses about the experimental setup for the measurement of concrete channel response.

## 4.1 Setup for measuring the transfer function of concrete channel plus amplifier

This basic experimental setup is used to measure the frequency response of the channel, considering the concrete and transmitting amplifier as a channel for various frequencies keeping the amplitude of the signal from the function generator as constant. Experimental setup is shown in Figure 4.1

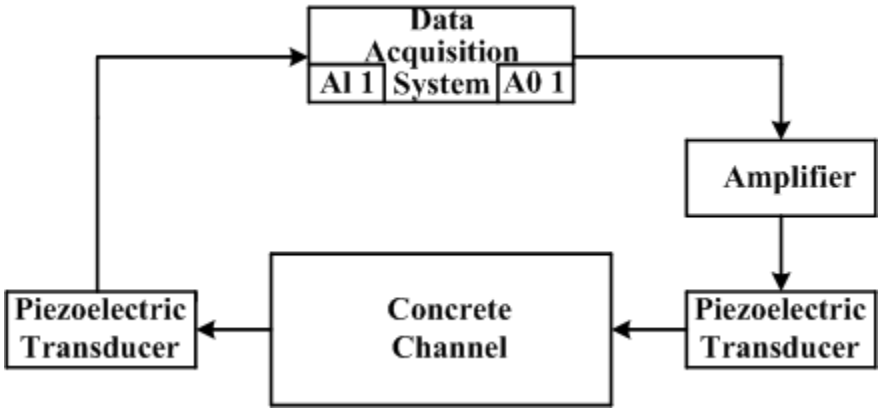


**Figure 4.1.** Experimental setup to measure concrete channel plus amplifier response

### 4.1.1 NI USB X Series 6361 Data Acquisition System

Data acquisition system samples the signals that measure real world physical conditions and convert the resulting samples into digital form that can be manipulated by

the computer. Piezoelectric actuator takes the information from data acquisition system and generates the mechanical stress or strain in the concrete structure. Piezoelectric sensor can also convert the stress or strain into an electrical signal that can be sampled by the data acquisition system.

Data acquisition system used in this project to measure channel response of the concrete channel is NI USB data acquisition system. This X Series Data Acquisition has 16 analog inputs with 2 MS/s sampling rate for one-channel, 1 MS/s sampling rate for multi-channel, 16 bit-resolution and the maximum working voltage for analog inputs is ±10V. It has two analog outputs with 2.86 MS/s sampling rate, 16 bit-resolution and the maximum working voltage for analog outputs is ±10V.

This data acquisition system can generate the signal as the function generator and can receive the signal as digital oscilloscope. The use of this data acquisition system helps in changing the amplitude, frequency, sampling rate etc. of the signal.

### 4.1.2 Transmitter side amplifier

The amplifier used in this project is Trek 2205 Piezo driver/power amplifier. It has a DC voltage gain of 50 V/V, large signal bandwidth of DC to greater than 75 KHz and small signal bandwidth of DC to greater than 100 KHz. It has an input voltage range from 0 to ±10V DC or peak AC.

This amplifier takes the output signal of function generator as input and generates a high voltage output signal to be transmitted into the concrete structure. The piezoelectric actuator is connected to the output of this amplifier. The generated high

voltage signal is used to excite the piezoelectric material to generate stress or strain inside the structure.

The purpose of this amplifier is to drive the piezoelectric transducers, which are commonly high capacitive loads that can be difficult to drive with good stability and settling time.

### 4.1.3 Experimental evaluation

Lab view is used to connect the data acquisition system to the PC interface. A graphical user interface is designed which allows the user to change various parameters like sampling rate, frequency and amplitude of the input signal, samples to be read and samples to write into a file. The respective ports, which are used for analog input and analog output, are selected. Function generator block is used in the Lab View software to generate a sinusoidal wave with 6VPP. Once the data acquisition system (DAS) is connected to PC via USB cable, if the PC has the entire driver's required installed, then the two LED's on DAS glow showing the device is ready and active to perform the experiment. In our experiment, tests are performed for two sampling rates 200k Sam/sec and 500k Sam/sec, the amplitude for the input signal is selected as ±3V and kept constant for the frequency range used.

For every frequency used, Lab view program is designed to collect 100,000 samples for both input signal i.e. from function generator block used and output signal from concrete channel for further data processing.

As PZT's are inefficient, they need a high power signal to generate the acoustic signal to transmit in the concrete channel. So, the amplifier is used to convert the low

power signal to high power signal. The ±3V(6 VPP) signal generated by function generator in the Lab view is sent to the amplifier using analog output (AO1) port on the data acquisition system. The amplifier connected to the actuator outputs the ±150V (300 VPP) signal, which is good enough to drive the PZT's to generate acoustic signal.

The ideal concrete channel propagates the mechanical strain wave through the concrete excluding other piezoelectric transducers during transmission, like wireless channels excluding the antennas. The output of the PZT sensor in the concrete channel is connected to the data acquisition system using the analog input (AI1) port. The collected data is used for estimating the response and channel distortion of the channel. The channel here includes amplifier plus the concrete channel, as the samples from function generator and PZT sensor are only collected and used for further data analysis.

Figure 4.2 shows the graphical user interface in Lab view used for the experiment for this measurement. The user can manually select the desired frequency and amplitude for the input signal. The input signal is generated from the function generator in Lab view, which is fed to the amplifier using AO 0 module on the data acquisition system. The lower block displays the signal received from the sensor using the AI 0 module on the data acquisition system. The sampling rate in this example is selected as 200K Sam/sec. Samples to write was selected as 100,000 for every frequency. So, even for a least frequency signal like 100Hz signal for 0.5 seconds, we can estimate almost 50 peaks to investigate the exact peak of the signal.

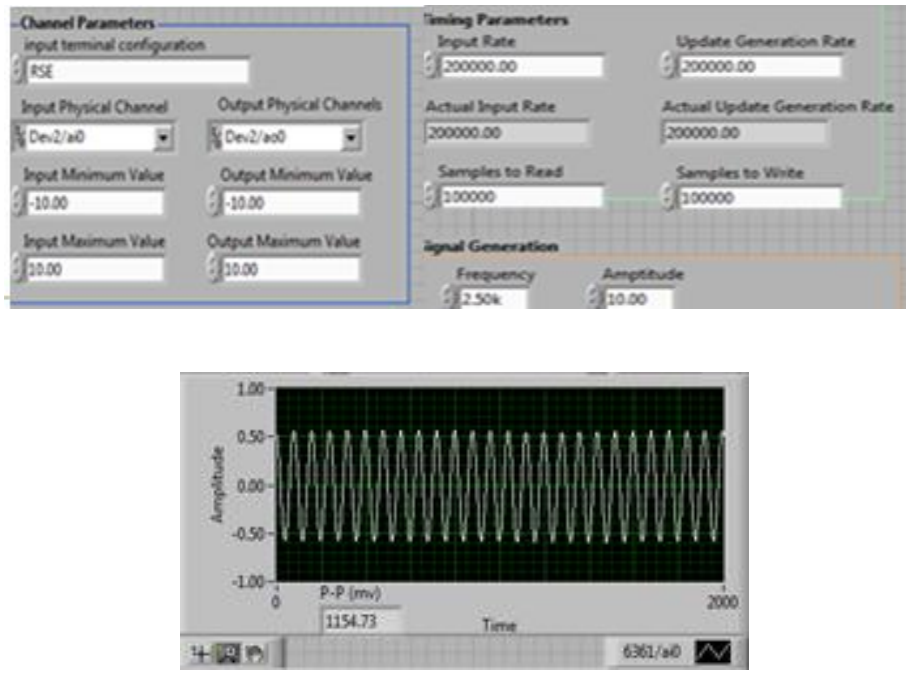


**Figure 4.2.** Graphical user interfaces in Lab View

## 4.2 Setup for measuring the response of concrete channel

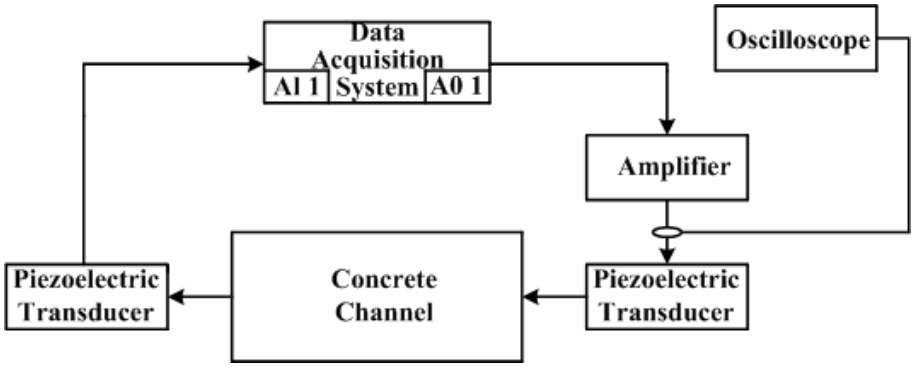


**Figure 4.3.** Experimental setup to measure response of the channel

The second experiment finds the response of the concrete channel for various frequencies keeping the amplitude of the signal from the function generator as constant. Figure 4.3 shows the experimental set up to estimate the frequency response of the concrete channel.

### 4.2.1 Experimental Evaluation

The aim of this experiment is to collect the samples of the input signal going into the concrete channel after amplification of original signal and the samples of the output signal from the PZT sensor. The oscilloscope is connected to the output of the amplifier to collect the signal samples while amplifier is connected to the PZT actuator with the help of PD 3120 divider/combiner. This is done so because the amplifier can operate differently in the presence and absence of load.

The reason behind using the oscilloscope to collect the signal samples at the output of amplifier is because the input range for the data acquisition system used is only ±10V. The maximum working voltage for analog inputs considering signal plus common mode is ±11V. The output of the amplifier is in the range of 300 Vpp. So, the oscilloscope, which can measure up to 400Vpp, is used to display and collect the output samples of the signal in the presence of load.

The data acquisition system and amplifier used for the previous experiment are used. Data acquisition system generates the signal using the function generator designed in Lab view software and generates ±3V signal, which is sent to the amplifier. The output from the PZT sensor can be seen in the same graphical user interface used for the previous experiment. This experiment is also performed for 200k Sam/sec and 500k Sam/sec. The amplitude for the input signal ±3V was kept constant for the frequency range used. The collected samples were used for further data analysis and processing.

The response of the concrete channel has been obtained using the experimental setup described in this chapter. Various modulation schemes implemented based on the

information derived from the response of the concrete channel is discussed in the next chapter.

### 4.3 Summary

The elementary task in designing the feasible communication system using concrete structure was to find the concrete channel response. These measurements aim to find the suitable frequency band for communication in the concrete structure. Experimental setup to find the response considering concrete plus transmitter amplifier as channel and only concrete as a channel are discussed. Data acquisition system and oscilloscope are used to collect the input and output signal samples for further data analysis.

# CHAPTER 5. MODULATION SCHEMES FOR CONCRETE COMMUNICATION

The response of the concrete channel is necessary in obtaining the spectrum suitable for communication between the sensor networks in a concrete structure. This knowledge about frequency response is utilized in selecting the frequency band to transmit the stress waves modulated with information using the communication system designed. These stress waves are modulated using different modulation schemes. GNU Radio, a software defined radio system, is used in order to implement a fully functional communication system and eliminated the need for hardware design. Signal processing blocks in GNU Radio that are written in C++ and implemented using python scripts utilized to implement different modulation schemes. This chapter illustrates the implementation of various modulation schemes for concrete structure and finding the capability of concrete structure as a communication channel.

## 5.1 Software defined radio

A software-defined radio is a radio system, which uses software to implement signal-processing blocks instead of using hardware. The radio hardware problems are turned into software problems. The fundamental characteristic of software radio is that software defines the transmitted waveforms, and it demodulates the received waveforms [28]. This is contrary to most radios in which the processing is done with analog circuitry or analog circuitry incorporated with digital chips. The flexibility of software radios made them a revolution in radio design due to its ability to design radios that change on

the fly, creating new choices to users. They also have a potential to build decentralized communication systems.

Figure 5.1 shows the transmit path of typical software radio block diagram.

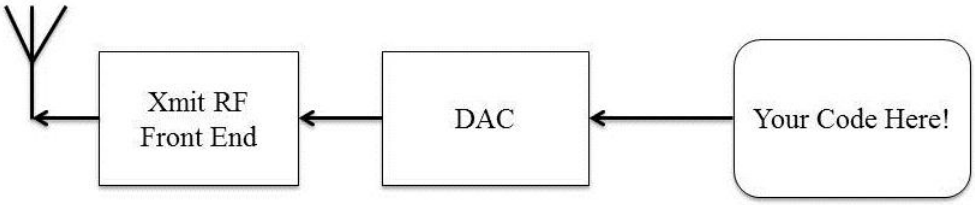


**Figure 5.1.** Transmit path of typical software radio block diagram

Figure 5.2 shows the received path of typical software radio block diagram.

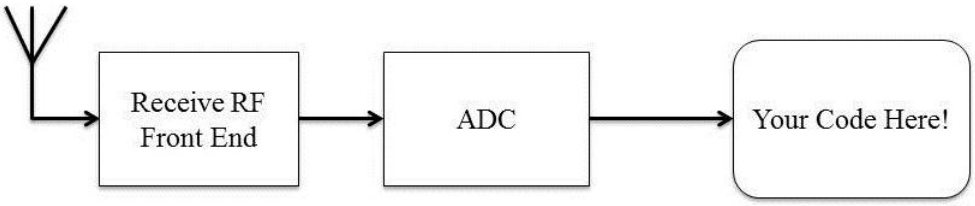


**Figure 5.2.** Receive path of typical software radio block diagram

The associated hardware plays an important role to understand the software part of the radio. The transmit path consists of an antenna, a RF front end, and digital-to-analog converter (DAC) and a bunch of code. This digital-to-analog and analog-to-digital converters act as a bridge between physical world of continuous analog signals and the world of discrete digital samples manipulated by software. In this project, Universal Software Radio Peripheral 2 (USRP2) is used to convert the digital samples to analog signals and analog signals to digital samples.

## 5.2 GNU Radio

GNU Radio, an open source software development kit that provides signal-processing blocks to implement software-defined radios, is used to design the communication model. As GNU Radio is a software development kit, it can only generate digital data. GNU Radio uses Universal software radio peripheral (USRP) to transmit the generated digital data streams and receives digital data streams from the receiver. GNU Radio utilizes filters, modulators, demodulators, decoders and many other elements to generate and process the digital data stream. It uses C++ to design the signal processing blocks, which are implemented using python scripts. It supports both wireless communication research and real-world radio systems.

GNU Radio typically comes pre-packaged with the program GNU Radio-Companion (GRC), which allows a user to graphically construct a working communication system rather than spending time typing the python code. A generic transmitter and receiver design was implemented in GRC, and different modulation types were easily switched as the experiments demanded.

## 5.3 Transmitter and Receiver Design

The basic transmitter design using differential binary phase shift keying is shown in Figure 5.3

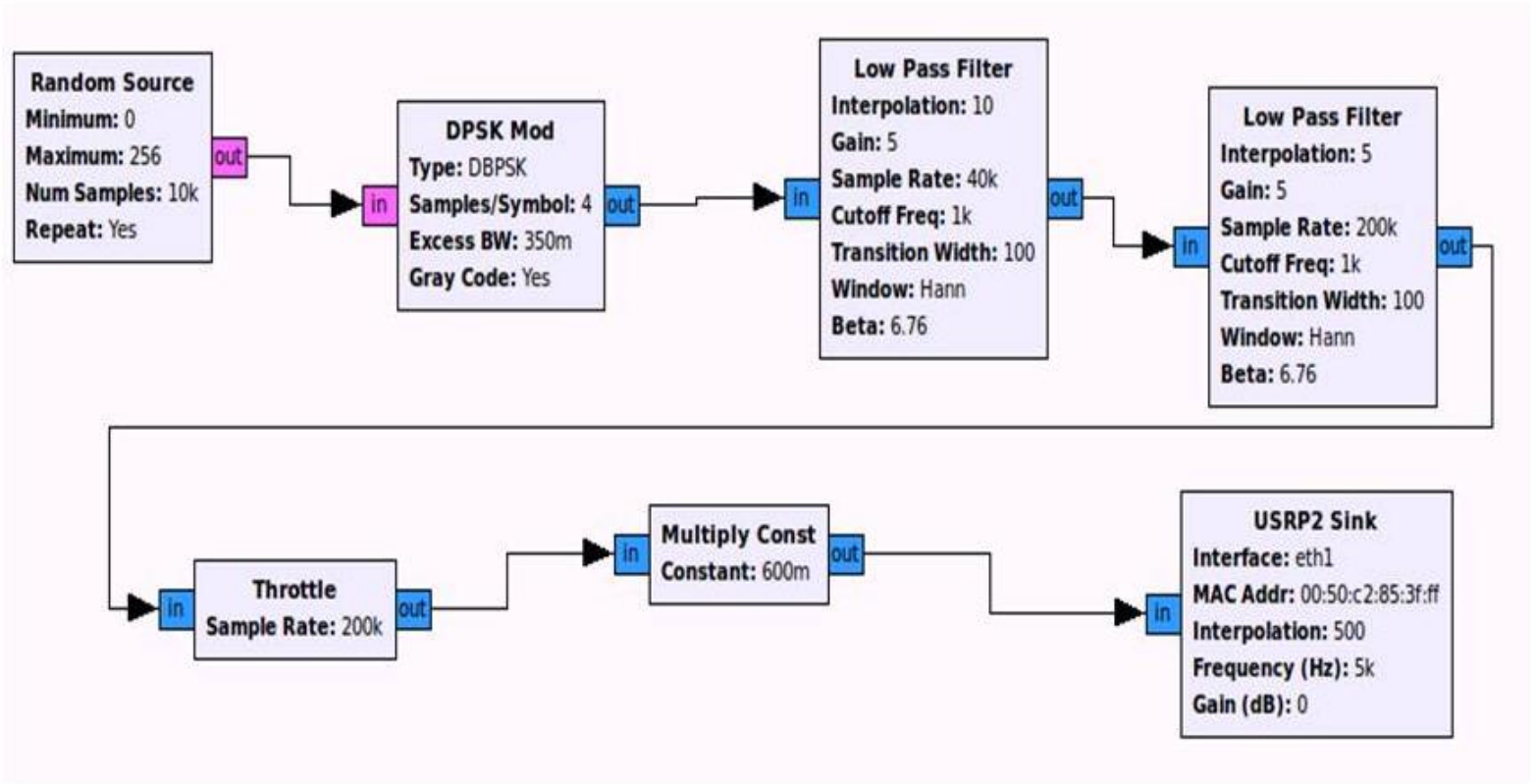


**Figure 5.3.** Transmitter flow graph in GRC for DBPSK system

The random source block first generates the message. The values are chosen such that 10000 samples are generated and repeated with values ranging from [0, 256). The output of the random source block is in the byte format.

DBPSK modulator receives the data and outputs the time-domain signal. The data is executed in the following steps.

- The received data is first divided into k-bit vectors, known as chunks. For DBPSK, it is one bit per symbol. So, received data is converted into 1-bit vectors.
- These chunks are then converted into gray coded bytes
- The gray coded bytes are differentially encoded using differential encoder
- These differential encoder bytes are then converted into symbols, which are in the complex form.
- These generated symbols are then received by a Root Raised Cosine (RRC) filter with an excess bandwidth of 0.35 for pulse shaping.

The data generated from DBPSK modulator is the data generated after RRC filter stage. Next, the data is interpolated in two stages by up sampling by 10 and 5 using two low pass filters and simultaneously filtered. The throttle is used to control the sampling rate. It has no functional value; rather it serves as a safeguard against computer freezes. Multiply constant block varies the TX gain. Lastly, the USRP sink interpolates the data up to 100 MSa/sec, and it up converts the signal to 5 kHz center frequency. Figure 5.4 shows the receiver flow graph in GRC for DQPSK system.

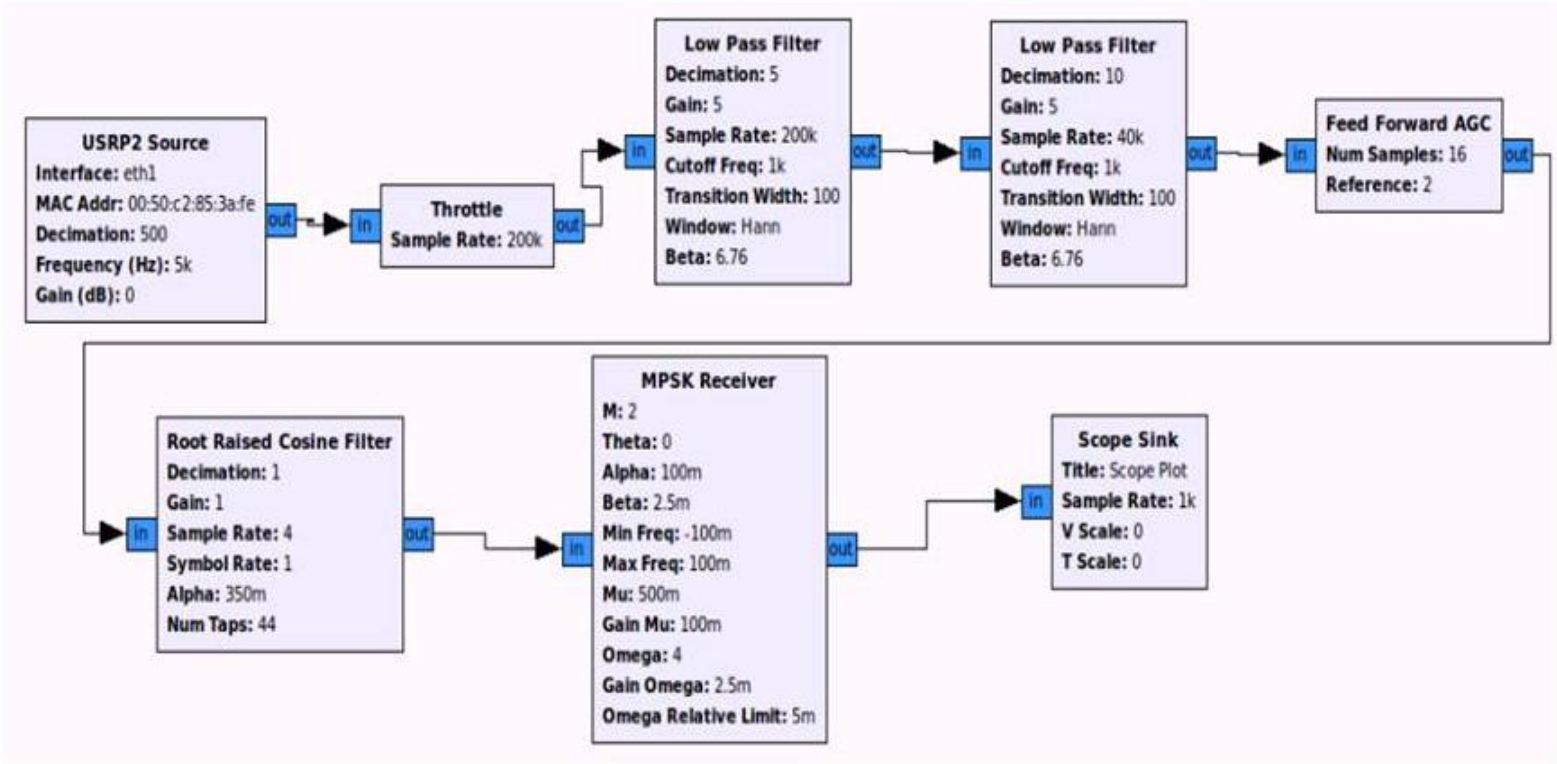


**Figure 5.4.** Receiver Flow Graph in GRC for DBPSK system

On the receiver side, USRP source provides the sampled and the down converted data from the ADC. It also decimates the data to allow a lower sampling rate. Throttle has no functional value, it controls the sampling rate and safe guards the system against freezing. The low pass filters decimate the data further to match the data rate in the transmitter. A feed forward AGC block is used to adjust the gain to an appropriate level for a range of input signal levels to the block. It is used to maintain the strong signal. Root raised cosine filter (RRC) is used in order to remove the inter symbol interference. The MPSK receiver block contains both demodulation of the data and the Costas loop. The function of Costas loop is to synchronize the phase of the received waveform with the input waveform. Scope sink block is used to display the recovered constellation at the output of MPSK receiver block.

Depending upon type of modulation scheme, the costas alpha and beta values, theta, M and other values change in the MPSK receiver block. The other value that should be taken into consideration is bits per symbol. It is 1 for DBPSK, 2 for DQPSK, and 3 for D8PSK.

These transmitter and receiver flow graphs are easily switched to implement DBPSK, DQPSK, and D8PSK, and the constellation of every modulation is successfully recovered. Figure 5.5 shows the recovered constellation for DBPSK modulation for center frequency of 5 KHz, symbol rate of 1K and corresponding signal to noise ratio of 13dB.

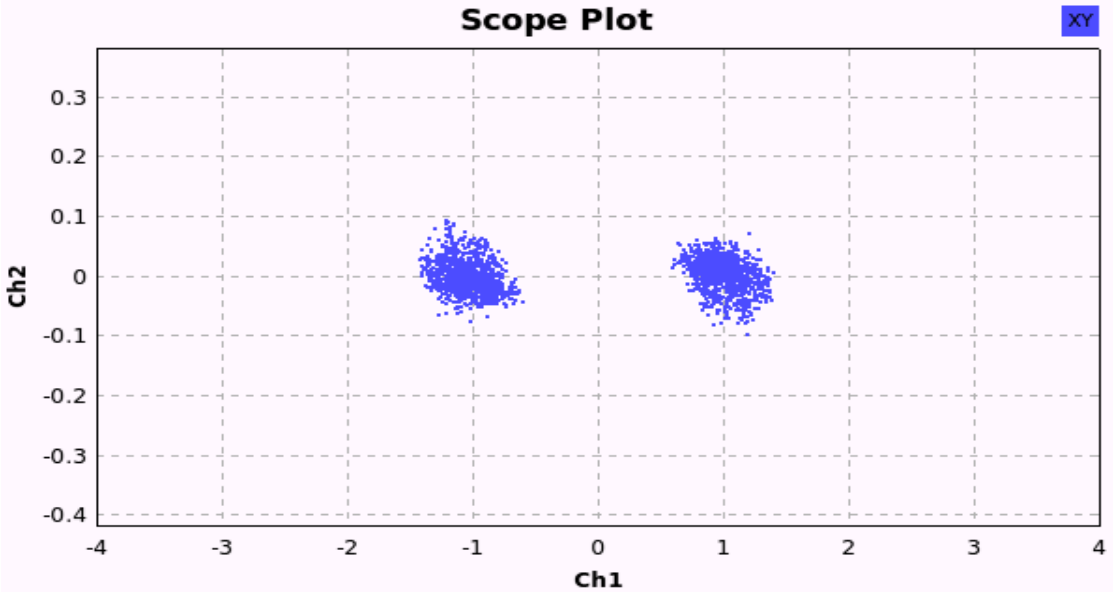


**Figure 5.5.** Recovered constellation for DBPSK

Figure 5.6 shows the constellation recovered for DQPSK for center frequency of 5 KHz, symbol rate of 1K, and corresponding signal to noise ratio of 13dB.

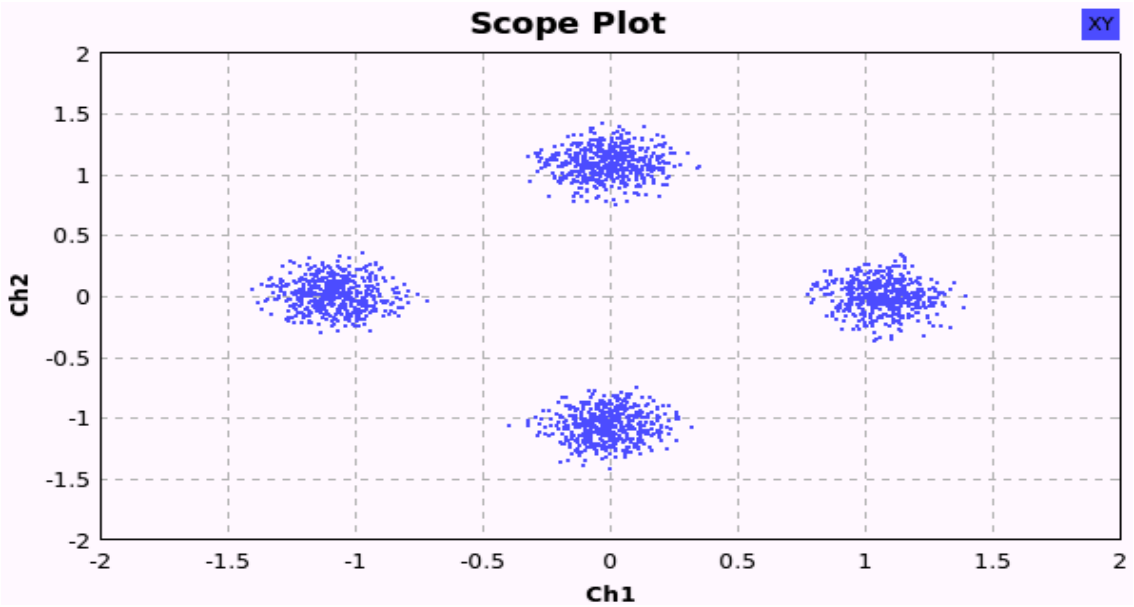


**Figure 5.6.** Recovered constellation for DQPSK

Figure 5.7 shows constellation recovered for D8PSK for center frequency of 5 KHz, symbol rate of 1K, and corresponding signal to noise ratio of 13dB.

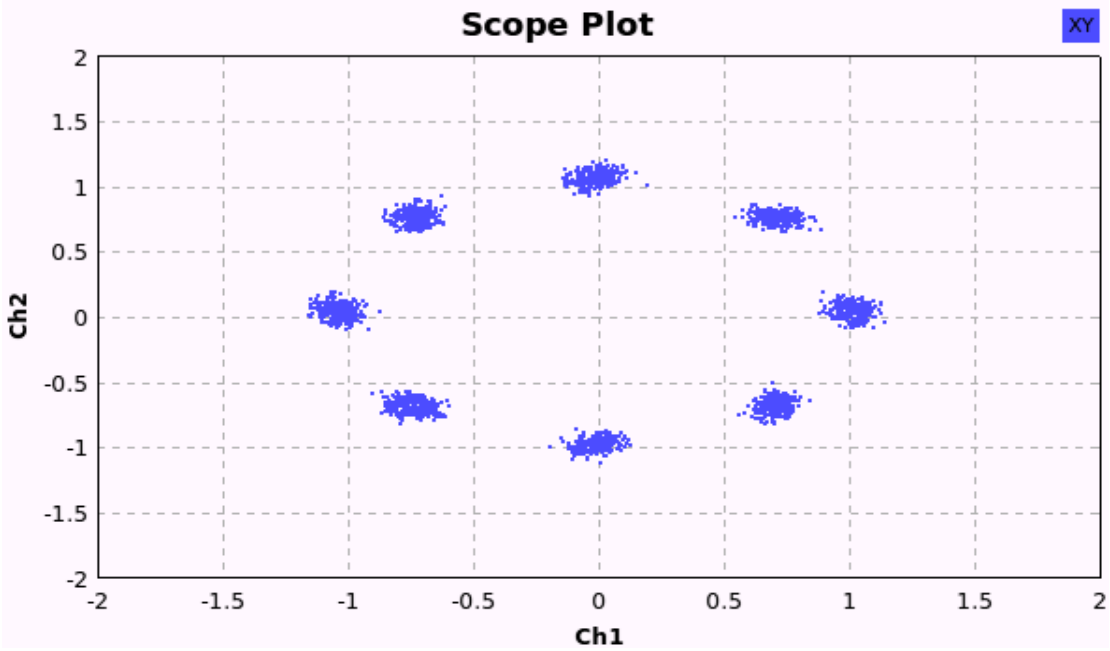


**Figure 5.7.** Recovered constellation for D8PSK

### 5.4 BER versus SNR for different modulation schemes

The constellations recovered for modulation schemes determine the concrete channel capability in transmitting the information. The next task is to find the Bit Error Rate (BER) for different signals-to-noise ratio (SNR) for different modulation schemes.

GNU Radio includes digital-bert python scripts that are used to calculate BER for various SNR. But these scripts are only applicable for BPSK. These scripts are modified to be applicable for DBPSK, DQPSK and D8PSK. Benchmark scripts in digital-bert are customized to include options to change center frequency, symbol rate, and TX gain, etc.

An infinite number of 1's from the vector source is generated. The output data stream is received by scrambler block. It scrambles the input stream using an LFSR. It works by XORing the incoming data stream by the output of the LFSR. It has the following parameters

- Mask – polynomial mask for LFSR
- Seed – Initial shift register contents
- Len – shift register length.

In this experiment, default values of the block are considered.

self._scrambler = gr.scrambler_bb (0x8A, 0x7F, 7) .

The output of the scrambler is then converted into gray coded bytes. This gray-coded information is then differentially encoded using differential encoder block. Depending upon the value selected for bits per symbol, the gray coded data is converted into symbols. These symbols are passed through root raised cosine filter (RRC) for pulse shaping. Then low pass filters are used to interpolate the data by up sampling. Throttle was used to control the sampling rate and multiply const block was used to change the TX gain. Finally, USRP sink interpolates the data to 100MSa/sec and up convert the signal to the selected center frequency.

On the receiver side, the inverse of the transmitter flow is performed. USRP source provides the sampled and down converted data from ADC. It also decimates the data to allow a lower sampling rate. The throttle is used to control the sampling rate. The low pass filters decimate the data further to match the data rate in the transmitter. AGC block was used to maintain the strong signal. Then RRC to remove the inter symbol

interference. MPSK receiver block is used to demodulate and it includes Costas loop. MPSK receiver block values are chosen based on the modulation scheme implemented.

Signal to noise ratio (SNR) is found by finding the ratio between the signal power and the noise power. SNR is estimated by collecting the samples of the received signal for every transmitted signal in the receiver side. These received signals include transmitted signal plus noise. The signal power can be determined using the mean of the absolute values of in-phase and quadrature components of the received signal. The noise of the system is estimated by running only the benchmark script on the receiver side. These collected samples helped in finding the SNR of the system for every transmitted signal.

The output of the MPSK receiver is differentially decoded using differential decoder block. The constellation decoder that outputs the data in bytes receives the output of the differential decoder. This gray coded data is then converted to un gray data. This data is descrambled using an LFSR in descramble block. This block has the parameters similar to scrambler block. The values used in the scrambler block in TX side are used for the descrambler block in RX side.

self._descrambler = gr.descrambler_bb (0x8A, 0x7F, 7) .

Finally, the bit error rate for particular signal to noise ratio is found by counting the number of zero’s in the received data. Bit error rate for various signals to noise ratio was found by varying the TX gain and compared with different center frequencies, symbol rate for various modulation schemes.

The final task in designing an effective communication system to monitor the concrete structure is to design the receiver amplifier. This amplifier is designed using Automatic Gain Control (AGC) logic, which is described in detail in the following chapter.

### 5.5 Summary

The knowledge about frequency response of concrete channel was utilized in selecting the frequency band to transmit and receive the stress waves modulated with information. GNU Radio, a software defined radio system is used to implement different modulation schemes and eliminated the need of hardware design. The constellations are recovered showing the capability of concrete channel in transmitting the information. BER-SNR performance is evaluated for different center frequencies, different symbol rates by varying the TX gain for various modulation schemes implemented.

# CHAPTER 6. AUTOMATIC GAIN CONTROL

Automatic gain control, as the name indicates, is a circuit that automatically controls the gain of the signal. The primary ideal function is to maintain the constant signal level at the output, regardless of signal variations at the input of the system [5]. The need for selectivity and good control of the output signal's level became a fundamental issue in any communication system. This project involves designing automatic gain control circuit to stabilize the output amplitude and improve the performance of the system.

## 6.1 components of AGC system

The AGC system designed has three components. They are analog multiplier, precision half wave rectifier and comparator. The detailed description of each component is discussed in further sections.

The main factors that must be taken into consideration while designing automatic gain control circuits are

- Frequency response
- Available control voltage
- Desired control range of the analog multiplier
- Settling time
- System configuration

Taking these factors into consideration, an AGC circuit is designed. Figure 6.1 shows the block diagram of AGC circuit.

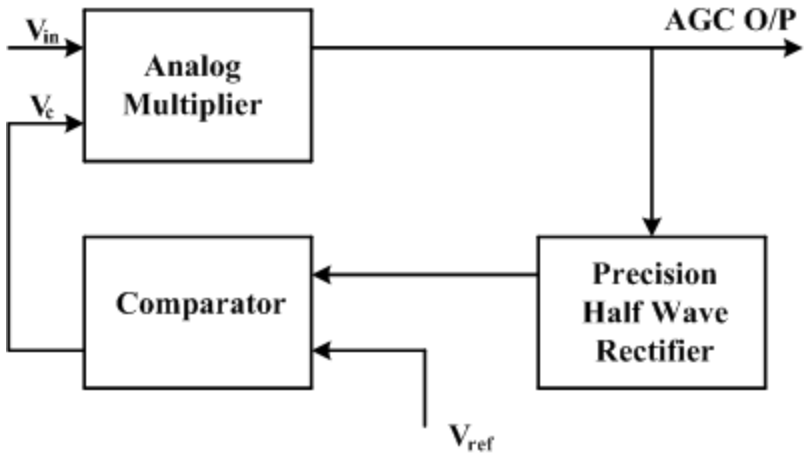


**Figure 6.1.** Block Diagram of AGC circuit

### 6.2 Working of AGC circuit

Voltage controlled amplifier is a special case of analog multiplier where one input is held at a steady state voltage, the signal at the second input will be scaled in proportion to the level on the fixed input. The analog multiplier in Figure 6.1 acts as voltage-controlled amplifier.

The input signal is fed into one of the input of the analog multiplier/voltage controlled amplifier whose gain is controlled by an external signal Vc (control voltage). The output of the analog multiplier is fed into precision half wave rectifier, which outputs the average DC value of the output signal of analog multiplier. The reference voltage Vref is a DC signal that is selected based on the required constant output amplitude of the AGC system, which is the output of the analog multiplier. The reference voltage and output of the DC value at the output of precision half wave rectifier is compared and the result of comparison is used to generate control voltage (Vc) to the analog multiplier. The two signals are compared until the constant output amplitude is reached at the output of analog multiplier.

AGC works on the idea where if the DC value of the input signal is less than the reference voltage, then it compares with the reference voltage and generates the control voltage. The two signals are compared until the DC value of the input signal of precision half wave rectifier is equal to reference voltage. When they both are equal, it outputs the constant signal. It basically works as an attenuator rather than an amplifier. If the signal needs to be amplified, then the output of AGC can be fed into inverting or non-inverting amplifier to get amplified to the required level.

Software simulation of AGC circuit is done using LTSpice. The design of AGC circuit is discussed in the further sections.

### 6.3 Analog Multiplier

An analog multiplier is device that takes two analog signals as inputs and the signal at the output is the product of the two input signals. If both the input and output signals are voltages, the transfer characteristics is the product of the two voltages divided by the scaling factor K, which has the dimension of voltage. Figure 6.2 shows the basic analog multiplier

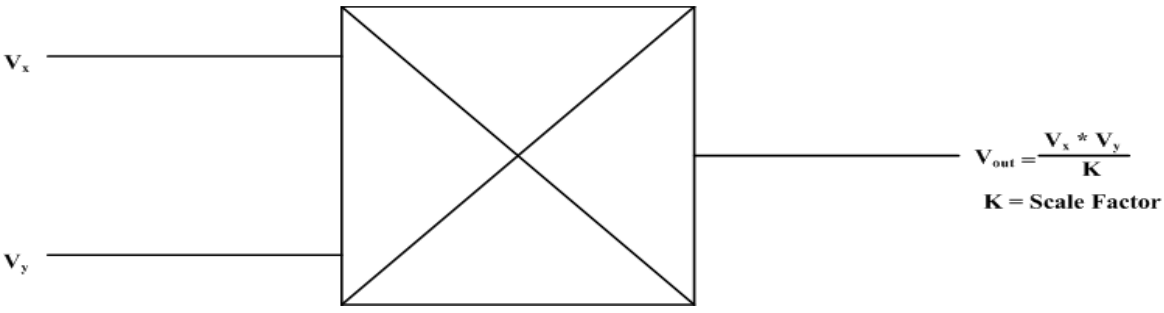


**Figure 6.2.** Basic analog multiplier

**Table 6.1.** Definitions of Multiplier Quadrants

| Type | $V_X$ | $V_Y$ | $V_{out}$ |
|---|---|---|---|
| Single Quadrant | Unipolar | Unipolar | Unipolar |
| Two Quadrant | Bipolar | Unipolar | Bipolar |
| Four Quadrant | Bipolar | Bipolar | Bipolar |

The most accurate, cheapest and simplest way of designing the analog multipliers is by using log-antilog amplifiers. The computation relies on the fact that antilog of the sum of the logs of two numbers is the product of those numbers. Log – antilog amplifiers are used in this AGC circuit to design analog multiplier. Figure 6.3 shows the multiplication using log and antilog amplifiers

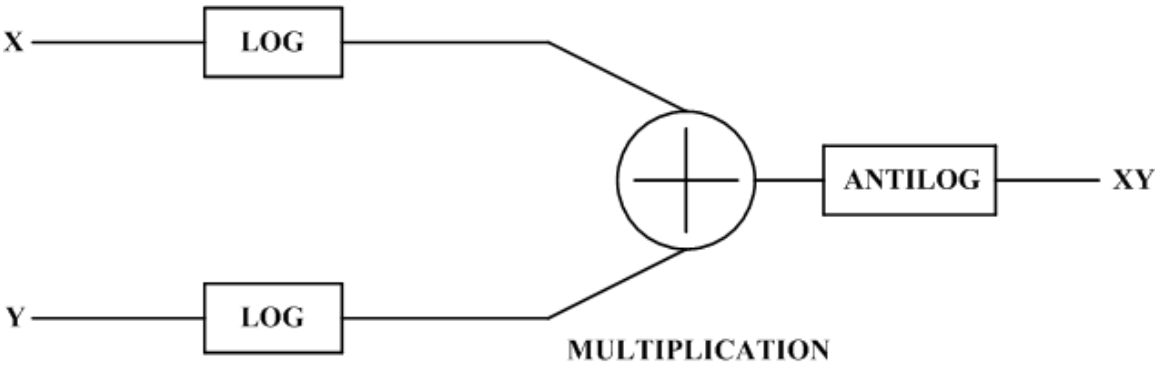


**Figure 6.3.** Multiplication using log and anti-log

### 6.3.1 Log and Anti-Log amplifier

Figure 6.4 shows the basic logarithm amplifier

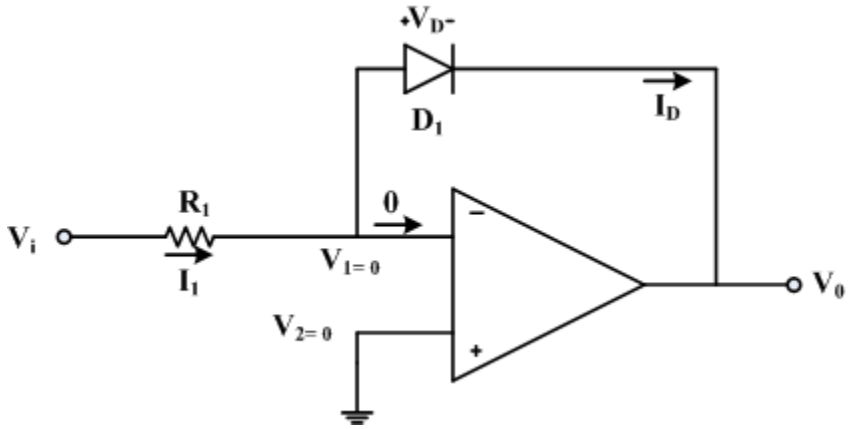


**Figure 6.4.** Basic logarithm amplifier

The ideal diode shows the following transfer equation [5],

$$I_D = I_S(e^{\frac{V_D}{nV_T}} - 1), \tag{6-1}$$

where

$I_S$ = Reverse saturation current,

n = constant between 1 and 2 for silicon diodes,

$V_T = \frac{kT}{q}$ = Thermal voltage, (6-2)

and k = Boltzmann constant.

Restricting the operation voltage in such a way that the exponential term is greater than 1 and $n \approx 1$ can approximate the above equation as

$$I_D \approx I_S e^{\frac{V_D}{V_T}z} . \tag{6-3}$$

From Figure 6.5, diode is part of the feedback loop of an operational amplifier. Current $I_D$ can be expressed as

$$i_D = \frac{V_{in}}{R} . \tag{6-4}$$

Thus, we can express $i_D$ as

$$i_D = \frac{V_{in}}{R} = I_s e^{\frac{V_o}{V_T}} . \tag{6-5}$$

Solving for $V_o$ gives

$$V_o = -V_T \ln\left(\frac{V_{in}}{I_S R}\right) . \tag{6-6}$$

The output voltage is proportional to the logarithm of the input voltage. The restriction in using logarithm amplifier is that it works only for positive voltages. The input voltage should be greater than zero.

The logarithm amplifier can also be implemented using n-p-n transistor instead of diode. The emitter-base junction of an n-p-n transistor is similar to that of a diode. The transistor to act as a diode, the base-collector junction of a transistor should be shorted. Based on this, a logarithm amplifier is designed using transistor instead of diode and the relation between output voltage and input voltage still remains unchanged. Most logarithmic amplifiers are based on the inherent logarithmic relation between the collector current and base-emitter voltage in silicon bipolar transistors. Figure 6.5 shows the logarithmic amplifier using a transistor

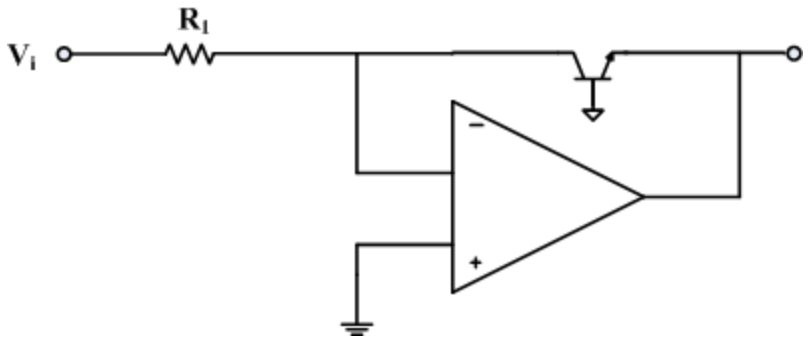


**Figure 6.5.** Logarithmic amplifier using a transistor

The base terminal of the transistor can be grounded, because the collector terminal connected to inverting port of op-amp is in virtual ground. So, the connection functions the same as in the case where base-collector junction is shorted.

The logarithmic amplifier holds the relation of output voltage proportional to the logarithmic of input voltage. The anti-log amplifier performs the function inverse to that of log-amps where the output voltage is proportional to the exponential of input voltage. Figure 6.6 shows the anti-log amplifier using a transistor

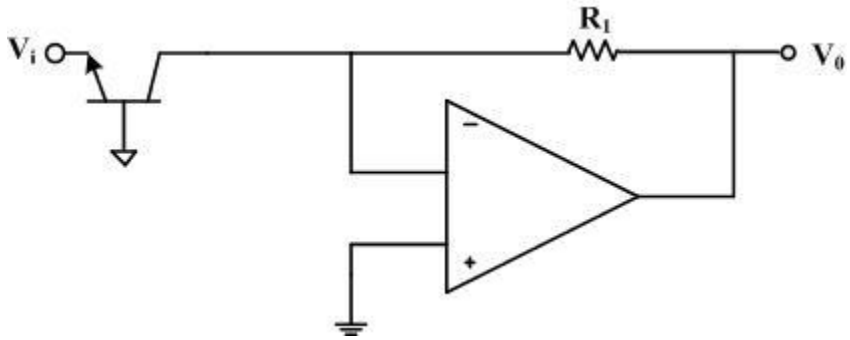


**Figure 6.6.** Anti-log amplifier using a transistor

The input and output voltage in an anti-log amplifier are related as

$$V_o = I_S R_1 \exp\left(\frac{-V_i}{V_T}\right). \quad (6\text{-}7)$$

The main drawback of this circuit is the high temperature dependence it shows due to the presence of $I_S$ in the transfer function. Placing a matched diode or diode-connected transistor can compensate the high temperature dependency.

### 6.4 Software simulation of AGC

The relation between input voltage and output voltage in log and anti-log amplifier can be utilized to design an analog multiplier. Software simulation of AGC is done using LTSpice.

The first step towards simulation of AGC is designing a one quadrant analog multiplier using log and anti-log amplifiers, as log and anti-log amplifiers work only for positive inputs. Figure 6.7 shows the one-quadrant analog amplifier

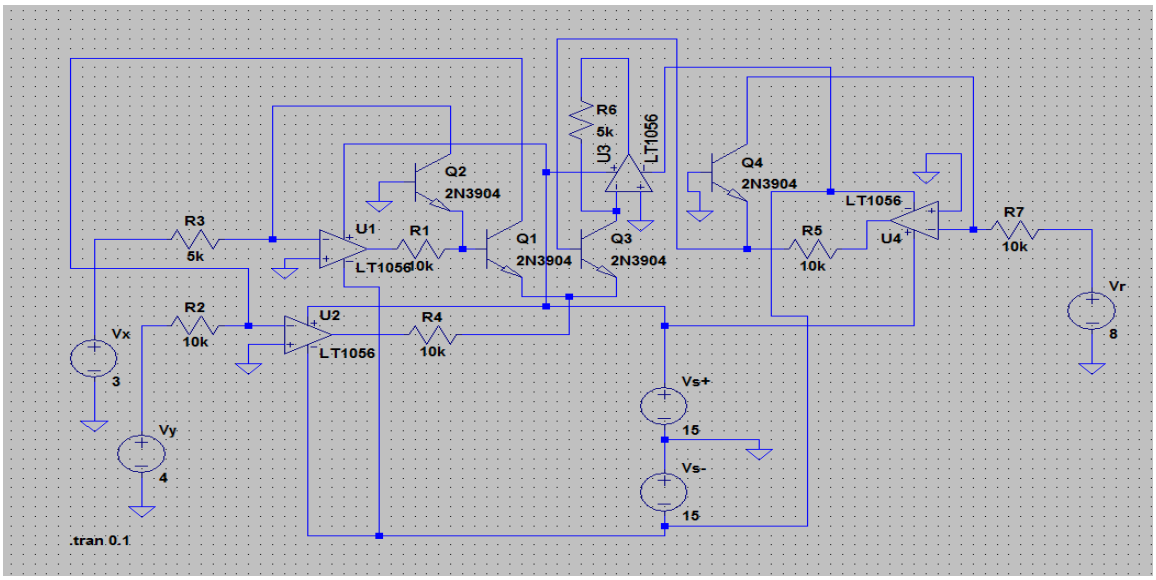


**Figure 6.7.** One quadrant analog multiplier

The inputs to the analog multiplier are $V_x$ *and* $V_y$ and the scaling factor is $V_r$. The use of log and anti-log amplifier in designing the analog multiplier does not require any

extra arrangement of placing the matched diode for temperature compensation. The reason behind this is that the temperature dependence terms in log operation of two inputs are compensated by the reference voltage term, which acts as the divisor for two input voltages (From Figure 6.2) and the anti-log operation at the end performed by op - amp U3. The output resulting at the output of op- amp U3 is

$$V_{out} = \frac{V_x V_y}{V_r} * \frac{R_6 R_7}{R_3 R_2}. \tag{6-8}$$

The values of $R_6, R_7, R_3, R_2$ are chosen such that the ratio of $R_6 R_7 \; and \; R_3 R_2$ is equal to 1. The final output of the analog multiplier is

$$V_{out} = \frac{V_x V_y}{V_r}. \tag{6-9}$$

This analog multiplier works only for positive values, as it is a one-quadrant multiplier. The input to the AGC circuit implemented in this project is the output signal from the piezoelectric sensor of the concrete channel, which is an AC signal. AC signal consists of both positive and negative cycles of the signal. One-quadrant multiplier is converted into two-quadrant multiplier where one input to the multiplier can take positive and negative values, but the other input still only works for positive values.

Figure 6.8 shows the two-quadrant multiplier where only one input to the multiplier can take positive. One-quadrant multiplier is converted into two-quadrant multiplier by adding the DC offset to the output of the concrete channel. This addition of DC offset makes the AC signal shift to the positive range.

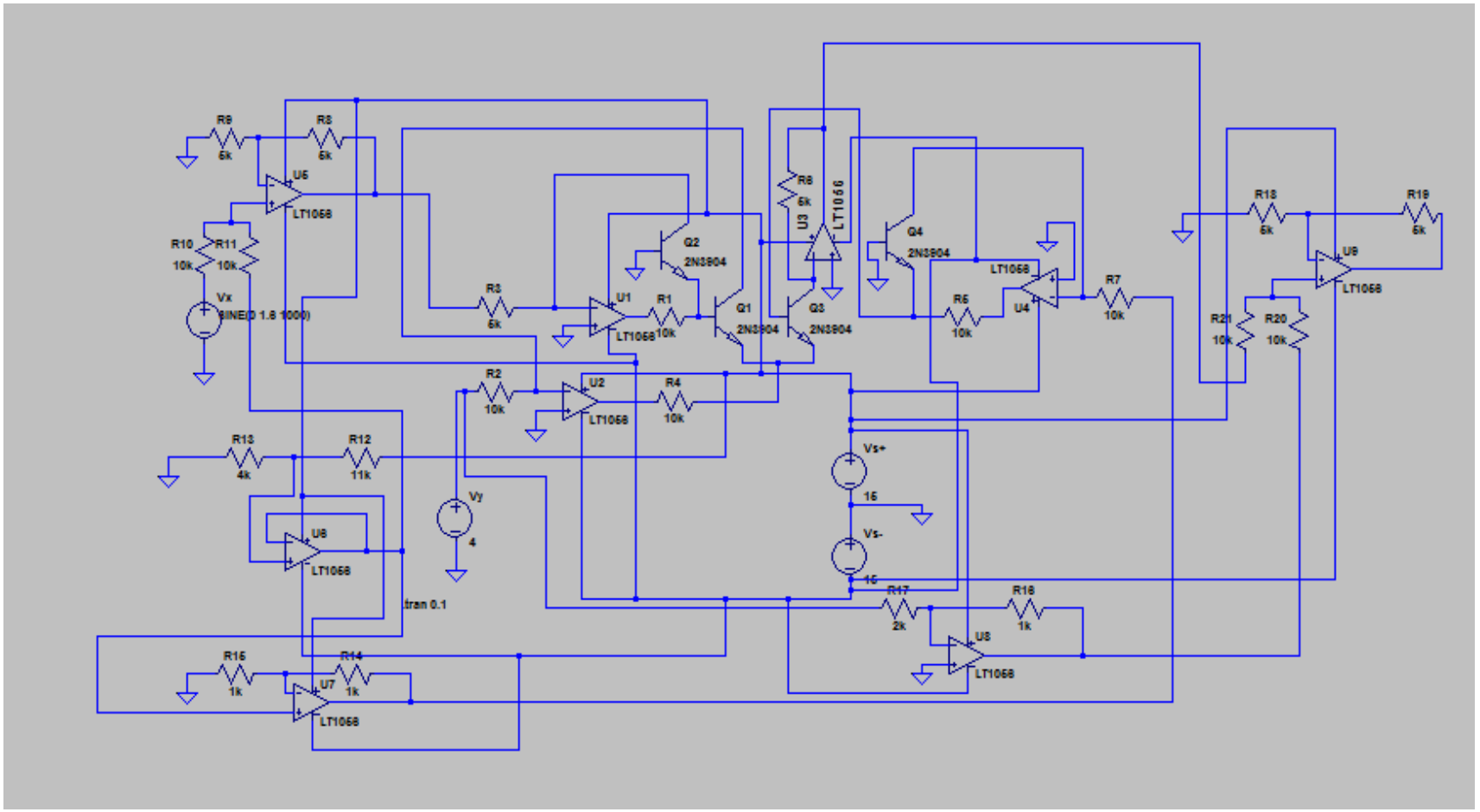


**Figure 6.8.** Two quadrant multiplier

The maximum signal magnitude coming out of the concrete channel is found to be in the range of 4 Vpp. So the addition of 4v to the concrete channel output shifts the signal to a positive range.

The inputs to the analog multiplier are $V_x + 4$ and $V_y$. The output of the analog multiplier (op amp U3) is

$$V_{out} = \frac{(V_x+4)V_y}{8} = \frac{V_xV_y}{8} + \frac{V_y}{2}. \quad (6\text{-}10)$$

To remove the extra component $\frac{V_y}{2}$ from the output of analog multiplier, $V_y$ is given to inverting amplifier U8 that outputs $-\frac{V_y}{2}$. The output of analog multiplier (U3) and U8 are added to give the desired output at the output of U9.

Final output of the two-quadrant multiplier is

$$V_{final} = \frac{V_xV_y}{8}. \quad (6\text{-}11)$$

The 4v and 8v sources are generated using a 15v power supply and op- amps U7 and U8. This makes the design simpler, as a single power supply is used to generate 4v and 8v using voltage divider technique.

The above analog multiplier can now take the AC signal as input. The designed analog multiplier can be modeled as Figure 6.9 with

$$V_{out} = \frac{V_1V_2}{8}. \quad (6\text{-}12)$$

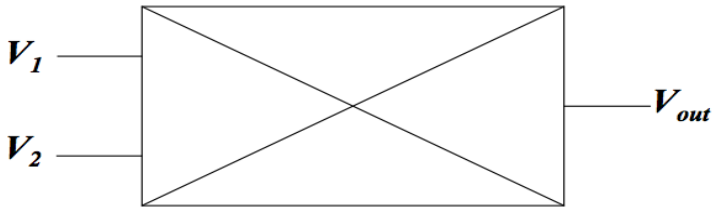


**Figure 6.9.** Analog multiplier model

A piezoelectric transducer has a very high DC output impedance and can be modeled as a proportional voltage source and filter network. Figure 6.10 shows the frequency response of a piezoelectric sensor. For use as a sensor, the flat region of the frequency response is typically used between the high-pass cut off and the resonant peak. A simplified equivalent circuit model shown in Figure 6.11 can be used in this region, as a charge source in parallel with the source capacitance, with the charge directly proportional to the applied force [28].

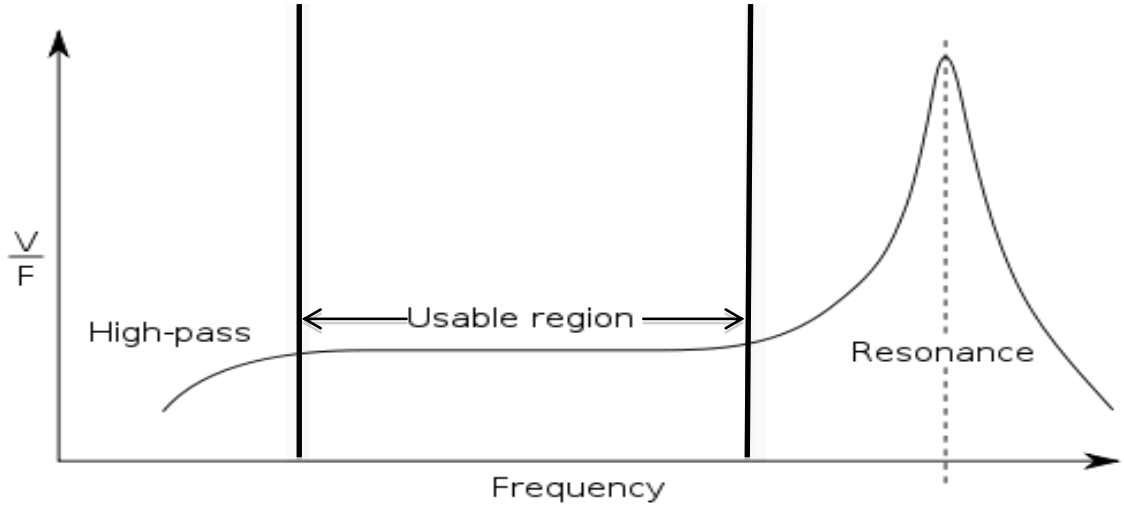


**Figure 6.10.** Frequency response of a piezoelectric sensor

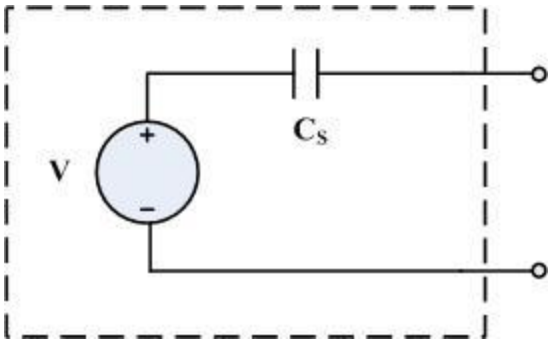


**Figure 6.11.** Piezoelectric sensor model

The high output impedance of the piezoelectric transducer demands the amplifier to have high input impedance. As a result, a high value resistor (R1 = 10 MΩ) is connected in parallel to the piezoelectric transducer as shown in Figure 6.12.

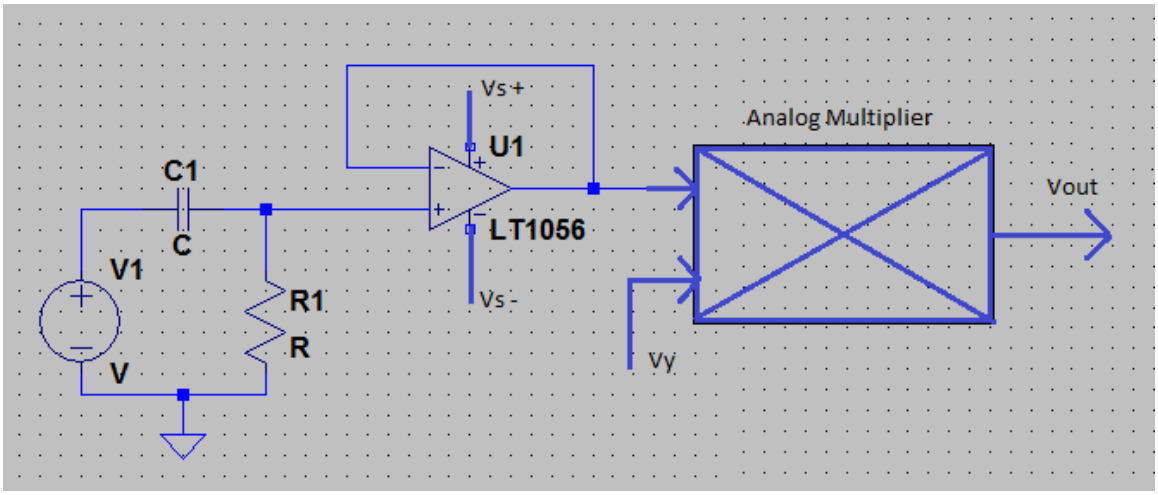


**Figure 6.12.** Analog multiplier for piezoelectric sensor input

Figure 6.12 shows the complete design of analog multiplier using piezoelectric sensor, output of the concrete channel. The next step in designing AGC is use to half wave rectifier to find the DC value of the AC signal generated at the output of the analog multiplier.

The combination of diode and resistor can be used as half wave rectifier. Figure 6.13 shows the simple half wave rectifier. If the diode direction is reversed, output is the positive half wave of the input ac signal.

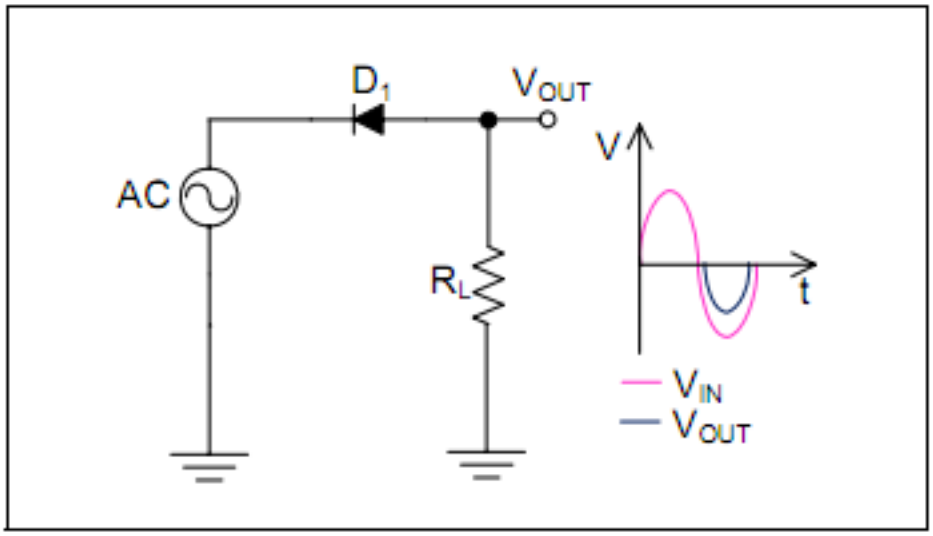


**Figure 6.13.** Basic half wave rectifier

Most of the signals at the output of the concrete channel are in the range of mVpp. The above half wave rectifier works only for the signals, which are higher than breakdown voltage of diode ($V_\gamma$= 0.7 V). This can hinder the rectification of the signal. So a diode combination with op-amp can be used as precision half wave rectifier that can rectify the signals that are smaller than the diode breakdown voltage. Figure 6.14 shows the analog multiplier with precision half wave rectifier.

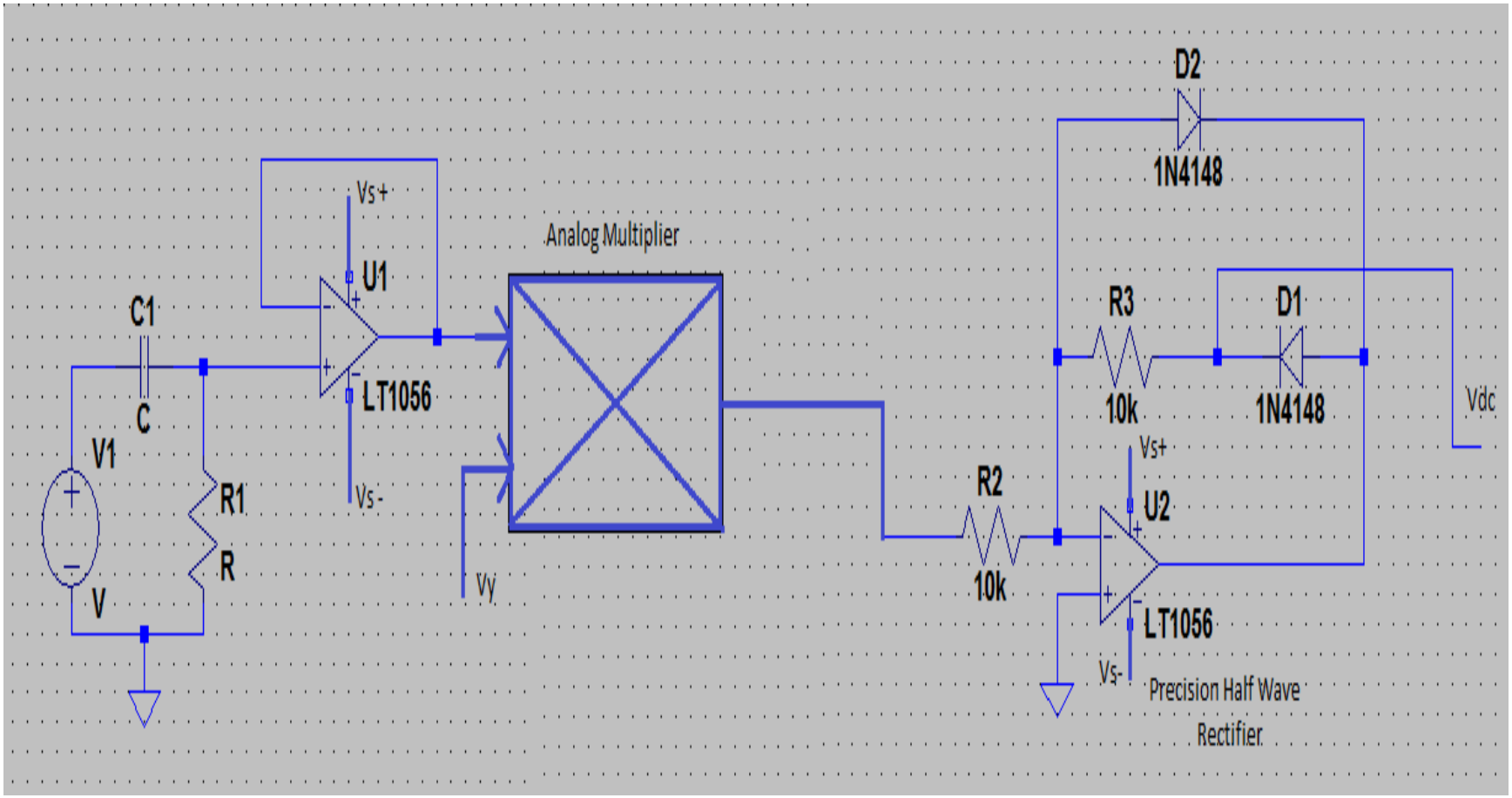


**Figure 6.14.** Analog multiplier with precision rectifier

The output of the precision half wave rectifier is

$$V_{dc} = \frac{V_p}{\pi}, \tag{6-13}$$

where $V_p$ represents the peak of the signal to the precision half wave rectifier and $\frac{V_p}{\pi}$ is the average DC value of the signal.

The output of U2 op amp does not give the half wave rectified signal because the output consists of half wave rectified signal along with diode D1 breakdown voltage. So the output is taken between diode D1 and R1 as shown in Figure 6.14, which gives the desired half wave rectified signal with average DC value $V_{dc}$ without including the diode breakdown voltage.

The next step to complete the AGC circuit is to design a comparator that compares $V_{dc}$ with the reference voltage and generates the control voltage Vc, which is fed as the other input to analog multiplier. Using this control voltage as input, analog multiplication is performed and then the signal is given to precision half wave rectifier that outputs the new $V_{dc}$. This new $V_{dc}$ is again compared with reference voltage and control voltage is generated. This cycle continues until $V_{dc}$ is equal to reference voltage.

For any input signal, where the DC value of it is higher than reference voltage is compared until both $V_{dc}$ and reference voltage is equal. When $V_{dc}$ and reference voltage become equal, as long as $V_{dc}$ remains constant, then the signal generated at the output of analog multiplier remains constant. This completes the design of AGC circuit. Figure 6. 15 show the complete AGC circuit.

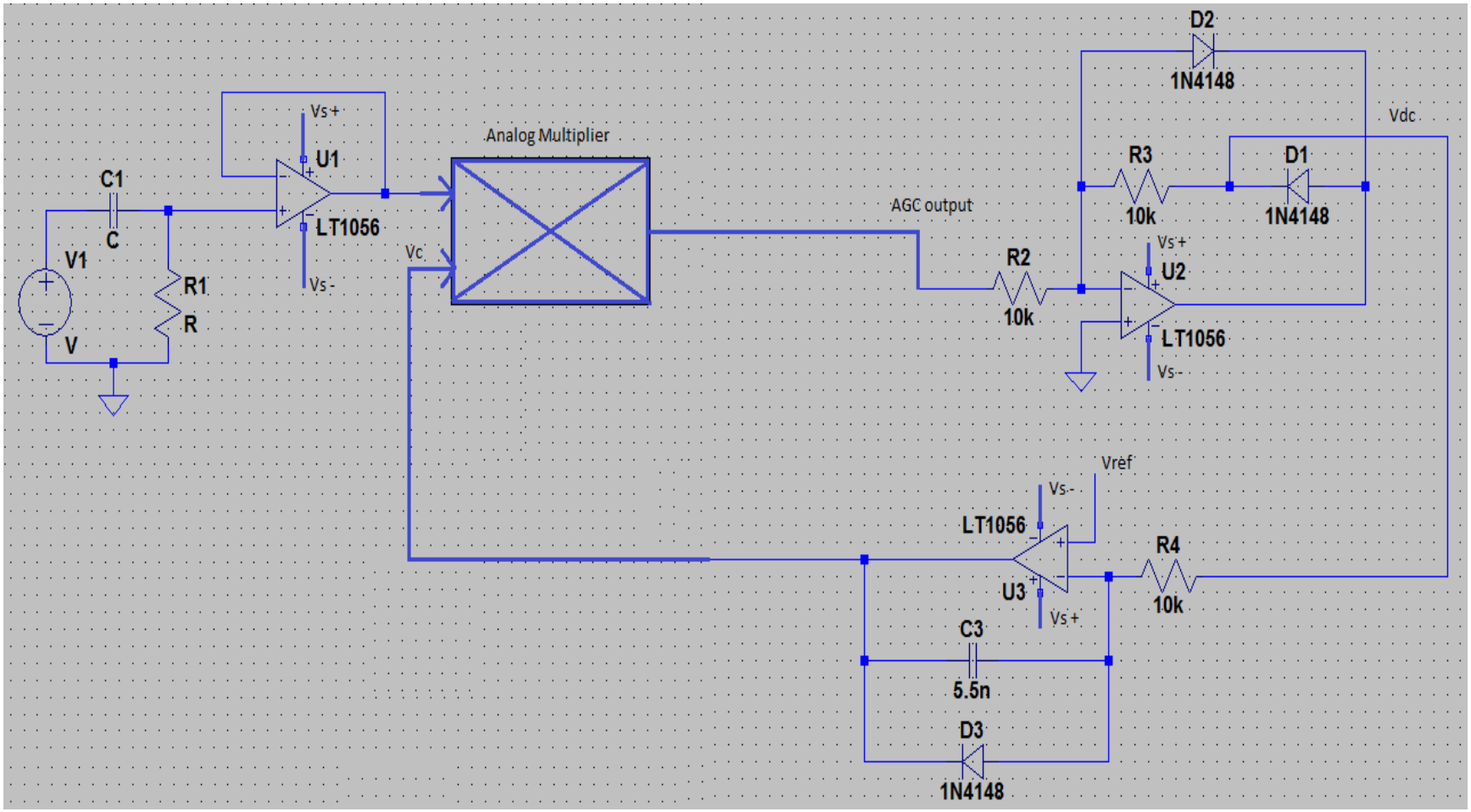


**Figure 6.15.** Complete AGC circuit

The last stage compares the reference voltage $V_{ref}$ and $V_{dc}$. The combination of precision half wave rectifier and comparator can be referred to as a rectifier with a filter, because of the use of capacitor in the last stage. The value of capacitor is chosen such that it should prevent the whole system going into oscillation. If the system goes into oscillation, then we get an amplitude-modulated output instead of AGC. If this is noticed, then the capacitor value should be increased to stabilize the system to give AGC.

As the designed analog multiplier works only for positive values of control voltage $V_c$, the second input to the multiplier. Diode D3 is used to prevent the control voltage $V_c$ from ever going negative. The moment $V_c$ tries to go to negative; diode D3 will conduct making $V_c$ to clamp down to zero. When control voltage is zero, then there is no gain in the analog multiplier and output is zero. But, the circuit output will not struck at zero, as reference voltage is applied. This reference voltage helps the control voltage take highest possible value that results in the output with highest gain in the next cycle. The regular functioning of the circuit is not obstructed due to the presence of $V_{ref}$. So there is no chance of $V_c$ going into negative, as long as reference voltage is applied. Even if control voltage is going to negative, diode D3 prevents it from ever going into negative.

The gain of the analog multiplier is controlled by $V_c$. If the input is increasing the gain is decreased and if the input is decreasing, the gain is increased so as to keep the output constant. This AGC circuit works in the following range.

If the input signal to the multiplier from concrete channel is

$$V_{in} = V_{pi} \sin(\omega t)\,, \tag{6-14}$$

then the designed analog multiplier gives the output

$$V_{out} = \frac{V_{in} * V_c}{8} = \frac{V_{pi} * V_c}{8} * \sin(\omega t), \tag{6-15}$$

using $$V_{rp} = \frac{V_{pi} * V_c}{8}. \tag{6-16}$$

As AGC is basically an attenuator, $V_c$ at most can be equal to 8V. When $V_c$ is 8v, then $V_{pi} = V_{rp}$. If $V_{pi} < V_{rp}$, then $V_c$ has to be greater than 8V which is not possible. For this circuit to work as AGC, $V_{pi\,(\min)} = V_{rp}$. $V_{pi\,(\max)}$ can be very large value, which is greater than $V_{rp}$. For all those values greater than $V_{rp}$, $V_c$ can take its minimum value, which is very nearly zero. The minimum value of $V_c$ is mostly 10 times the offset voltage of the op-amps that are used in the analog multiplier. So, this AGC circuit will work for the variation of voltage starting from $V_{rp}$, up to very large values of the signal. If the analog multiplier is designed such that $V_{out} = \frac{V_{in} * V_c}{10} = \frac{V_{pi} * V_c}{10} * \sin(\omega t)$, then the maximum value of $V_c$ can be 10V. Remaining values remain the same.

Depending upon the hardware, which is taking the output of AGC, we can use inverting/non-inverting amplifier to amplify the AGC signal in order to utilize the full range of the hardware. In this project, the AGC output is given to the LFRX that can only take $\pm$1V input. So the $V_{ref}$ and the amplifier gain at the AGC output is selected such that every signal at the output of concrete channel should be greater than $V_{ref}$ and it should be less than $\pm$1V. The output impedance of the amplifier should be low in order to complaint to the 50Ω and $\pm$1V LFRX input. Figure 6.16 shows AGC circuit with amplifier at its output.

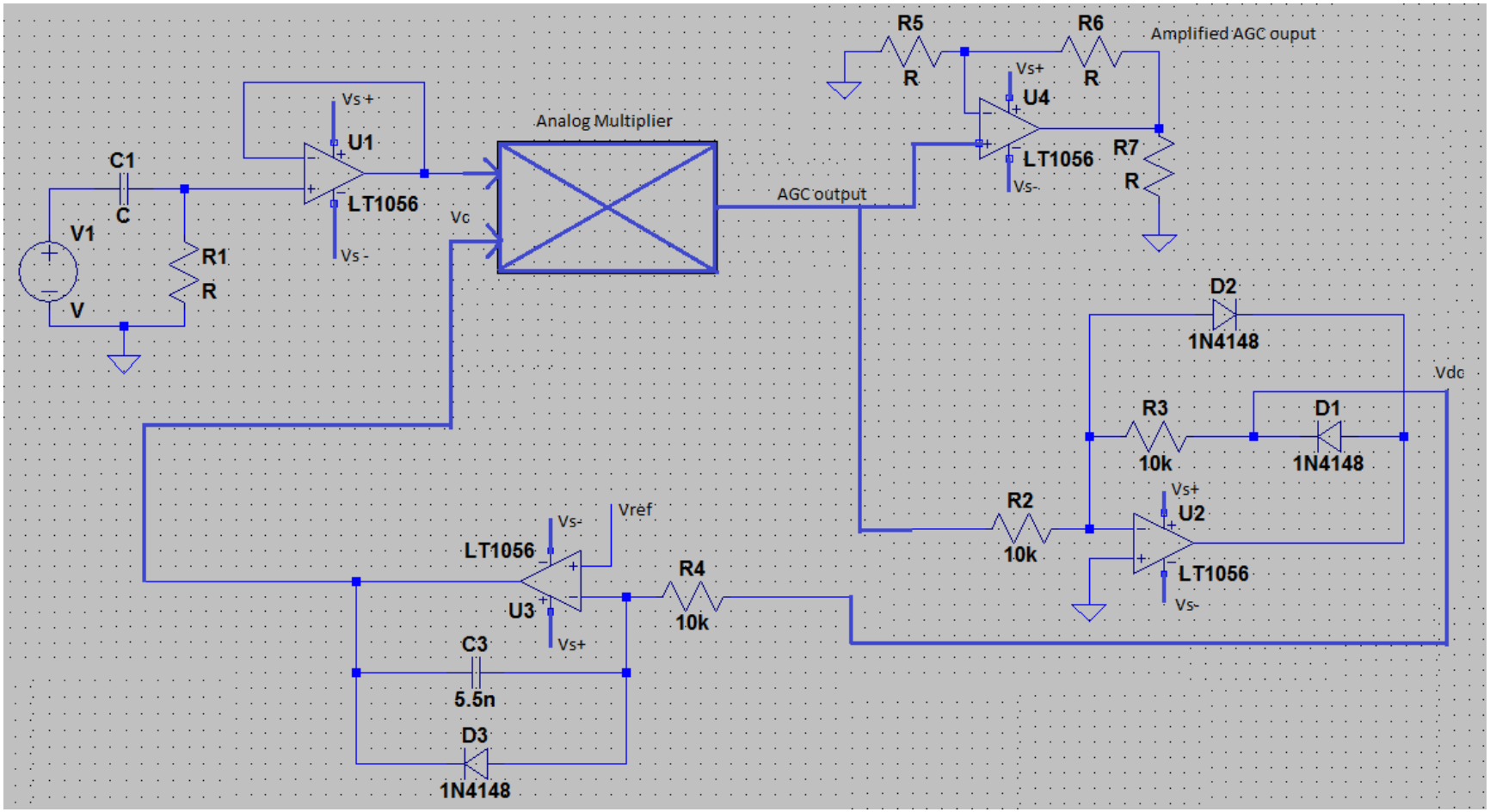


**Figure 6.16.** AGC circuit with amplifier at its output

Considering the working range of AGC and limitations, the software simulation of AGC is successfully performed. The next section discusses about the hardware implementation of AGC.

### 6.5 Hardware implementation of AGC

The hardware implementation of AGC is done on breadboard. The DC power supply was used for the supply voltage of op-amps. The supply voltage of op-amps is $\pm$15 V. Hardware implementation of analog multiplier circuit is found more susceptible to noise and offset voltage-related problems as these errors get multiplied. For this reason, it is difficult to manufacture general-purpose analog multipliers [29]. They are generally manufactured using specialist technologies and laser trimming.

AD633, four-quadrant analog multiplier IC, which is featured with laser-trimmed accuracy and stability, is found to a better solution in hardware implementation of AGC circuit. Figure 6.17 shows the functional block diagram of AD633.

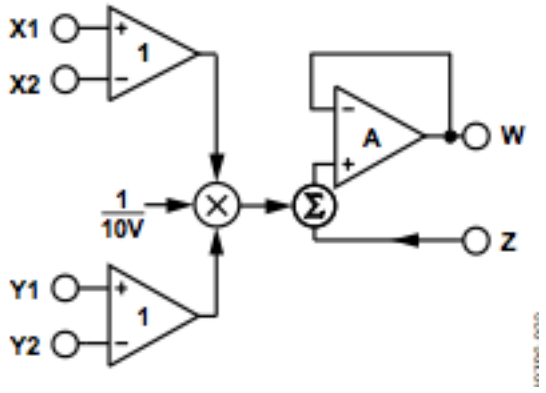


**Figure 6.17.** Functional block diagram of AD633

The transfer function of AD 633 is

$$W = \frac{(X1-X2)(Y1-Y2)}{10} + Z\ . \tag{6-17}$$

Features of AD 633 [30] are as follows:

- 4- quadrant multiplication
- Low cost
- Laser-Trimmed accuracy and stability
- Total error within 2% of full scale
- Differential high impedance X and Y inputs
- High-Impedance unity-gain summing point
- Laser-trimmed 10V scaling reference

AD633 has $\pm$10 V signal voltage range for input amplifiers. Figure 6.18 shows the pin configurations of AD633. Figure 6.19 shows the hardware implementation of AGC using AD633 4-quadrant analog multiplier.

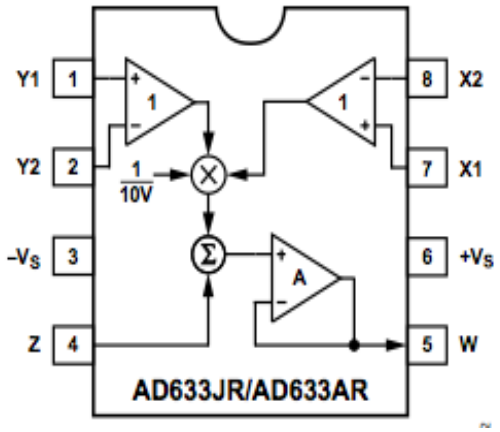


**Figure 6.18.** Pin configuration of AD633

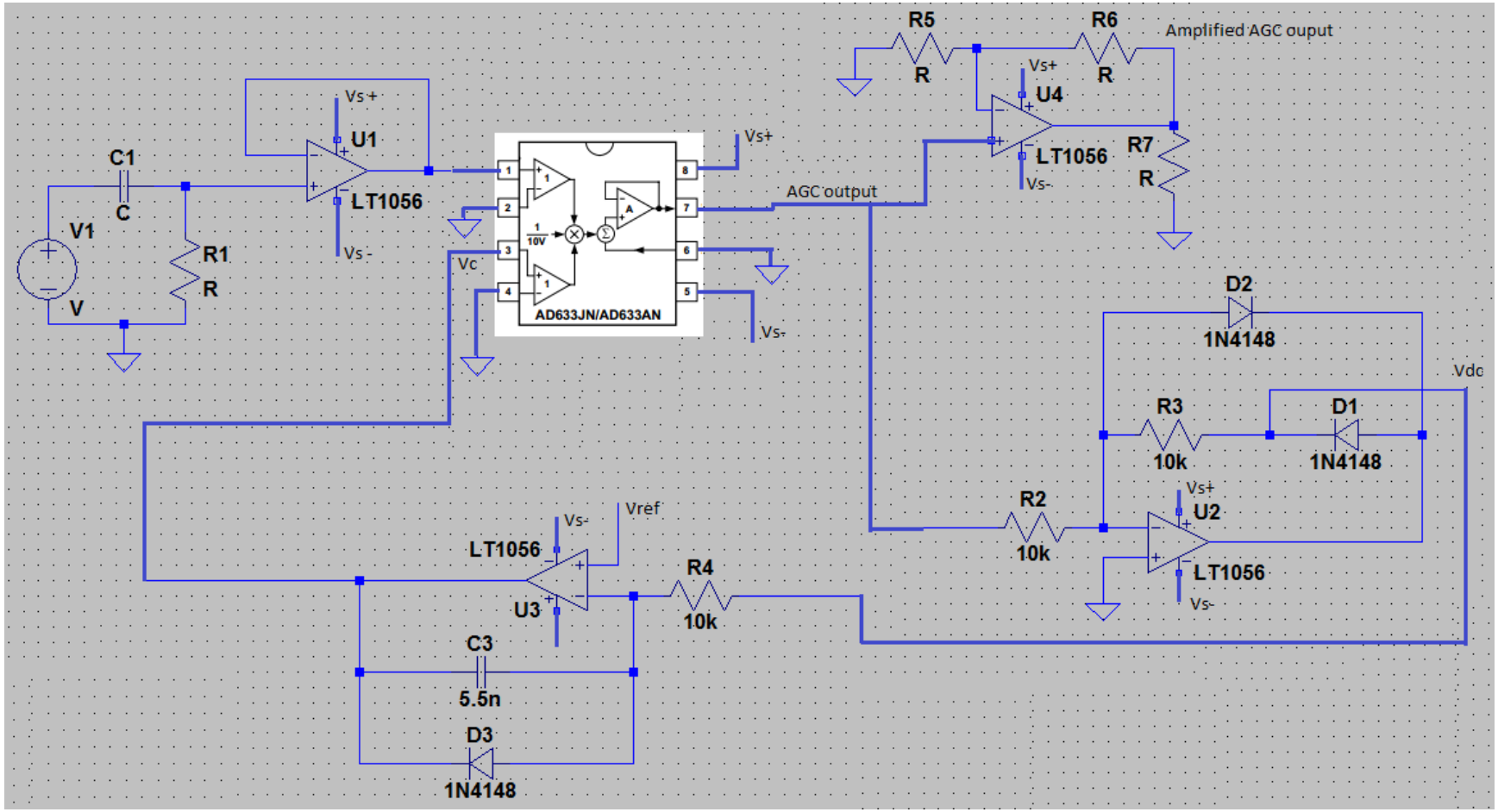


**Figure 6.19.** Hardware implementation of AGC

Software simulation of AGC using LTSpice and hardware implementation of AGC using AD 633 analog multiplier is successfully performed.

### 6.6 PCB schematic of AGC circuit

After successful hardware implementation of AGC, schematic of AGC circuit is developed using EXPRESS SCH software. Figure 6.20 shows the schematic of AGC circuit. Two variable resistors R6 and R10 are used. The reference voltage is generated using the power supply voltage of 15V, instead of using another voltage source. R10 is used to change the value of the reference voltage. R6 is used to change the gain of the non-inverting amplifier at the output of AGC. This schematic can then be linked to PCB file and EXPRESS PCB software can be used to develop a printed circuit board of designed AGC.

### 6.7 Summary

The limitation of input signal range of LFRX daughterboard led to design automatic gain control circuit on the receiver side. This chapter demonstrates the design of automatic gain control circuit using analog multiplier, precision half wave rectifier and comparator. LTSpice was used for software simulation. Hardware implementation was performed on breadboard using analog multiplier IC, LT 1056 op-amps, resistors, capacitors, diodes, and DC power supply. PCB schematic was developed using ExpressSCH, which can be linked to PCB file using ExpressPCB to develop printed circuit board layout of AGC.

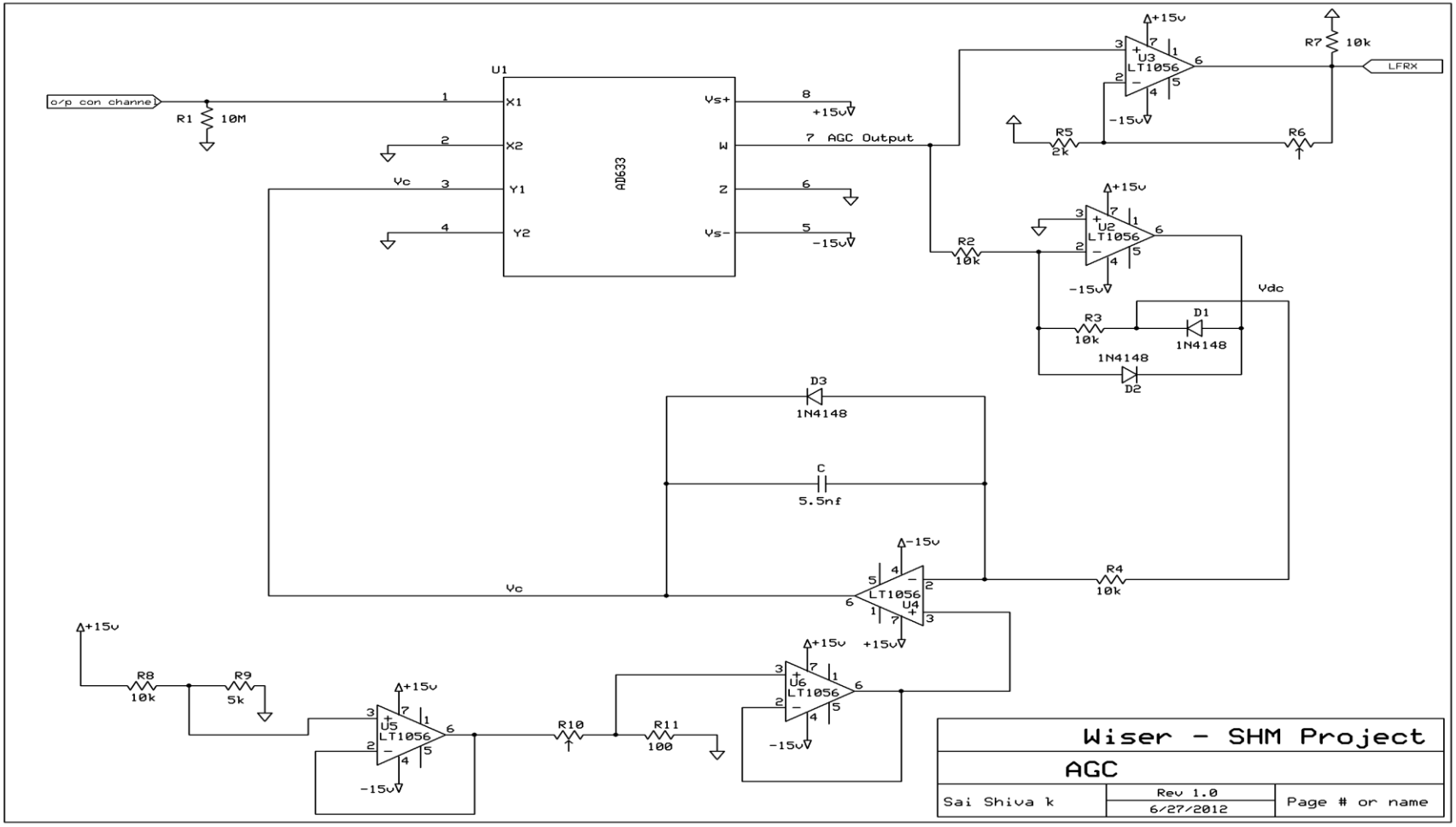


**Figure 6.20.** Schematic of AGC circuit

# CHAPTER 7. RESULTS

In this chapter, experimental results necessary in designing an effective communication system are analyzed and discussed. Measurement of concrete channel response is calculated using coherent detection method. Bit error rate for various Signals to noise ratio are measured by various TX gain and compared for different center frequencies, symbol rates for different modulation schemes. Automatic gain control circuit is designed and simulated using LTSpice. Hardware implementation of AGC is performed on breadboard using Analog multiplier, Op-amps, other components and equipment necessary to build the whole circuit.

## 7.1 Measurement of Concrete Channel Response

Evaluating the ability of a channel to transmit information usually involves estimation of channel response for single frequency input. The first experiment involves collecting the samples from the signal generated by function generator for every frequency and the samples from the output of the concrete channel. The required samples are collected from the lab view. Coherent detection method was followed to calculate the gain of the channel for various frequencies. This method involves computing the cross correlation of both signals. Correlation of two signals computes the degree to which both signals are similar.

The gain of the concrete channel is found using the following mechanism.

The input signal is generated as $x(t) = Vcos\ (2 * pi * f_c * t)$, (7-1)

with the output signal considered as $y\ (t)$ .

$$Rxy(\tau) = \frac{1}{N}\sum_{t=0}^{N-1} y(t) * x(t-\tau)\,. \tag{7-2}$$

Channel gain at frequency $f_c$ is $2Rxy\ (\tau_{max})/V^2$, (7-3)

where V is the amplitude of input signal. N is the total number samples. $Rxy(\tau)$ represents the cross correlation of input and output signal. By varying $\tau$, maximum correlation point $\tau_{max}$ is found.

Figure 7.1 depicts the channel gain while frequency of the input signal is varied.

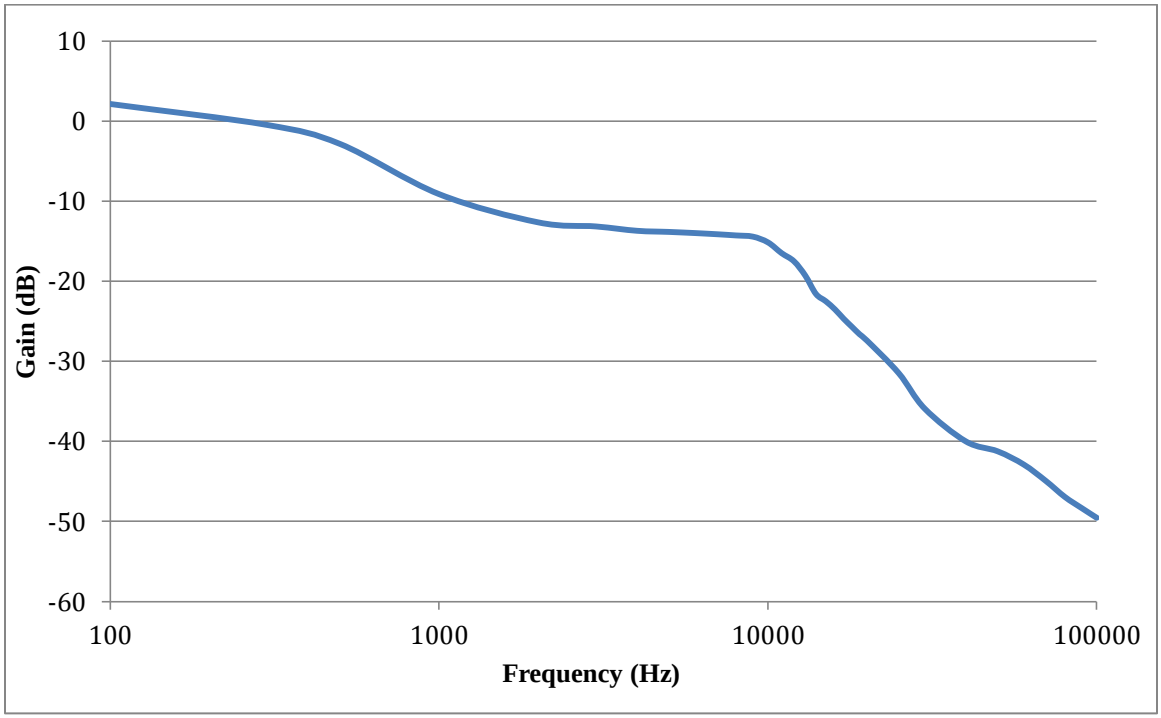


**Figure 7.1.** Concrete channel plus transmitter amplifier response

The first experiment has calculated the channel response considering the Amplifier and concrete channel as a channel. This shows the gain is constant from 2 KHz to 10 KHz.

The second experiment calculates the response of concrete channel solely without the amplifier. The response of the amplifier is plotted in Figure 7.2 shows the effect of amplifier on the concrete channel response for various frequencies.

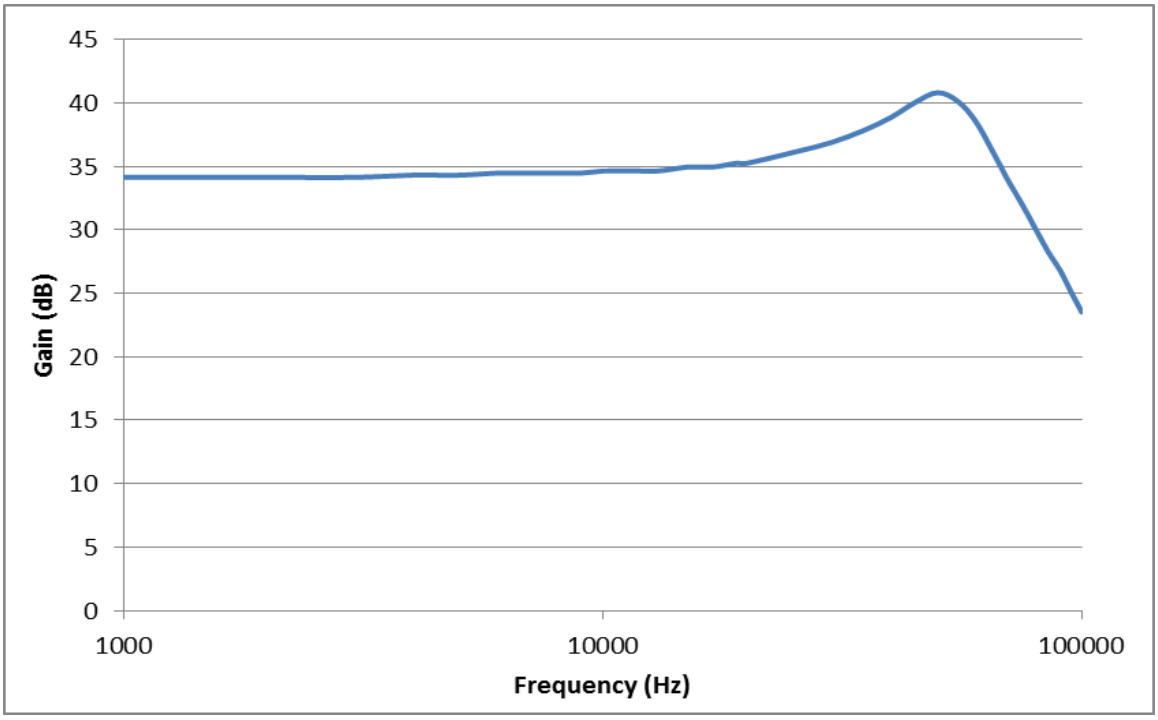


**Figure 7.2.** Transmitter Amplifier Response

The transfer function of a channel is a mathematical representation of the channel capacity to transfer the information. The second experiment involves measuring the peak-to-peak voltage of the output signal from PZT sensor and the output signal from the amplifier while connected to the load. The oscilloscope was used to measure the peak-to-peak voltage of the signal from the amplifier. The samples of both signals are collected in the LAB View and further processed to find the transfer function of concrete channel.

The transfer function of the concrete channel is found by taking the ratio of the peak-to-peak voltage from the amplifier and from the PZT sensor as

$$H(f) = \frac{V_{sen}(f)}{V_{amp}(f)}, \tag{7-4}$$

where $f$ is the frequency in Hz,

$H(f)$ is the transfer function,

$V_{sen}(f)$ is the voltage measured at the output of the PZT sensor,

$V_{amp}(f)$ is the voltage measured at the output of the amplifier. In the experiment, CS4 was used as the transmitter transducer and CS1 is used as the receiving transducer. Figure 7.3 depicts the channel gain while the frequency of the input signal is varied.

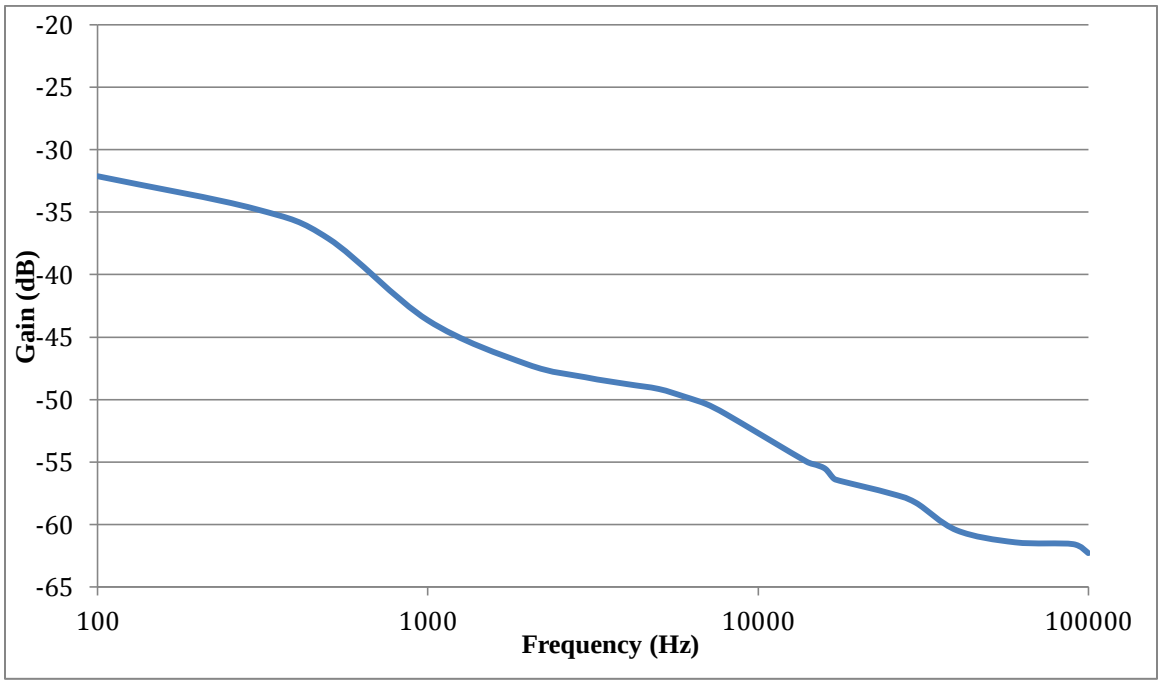


**Figure 7.3.** Concrete channel response

As the frequency response of the transmitter amplifier and concrete channel is constant around 2 KHz – 10 KHz, it will easiest to communicate through the concrete channel within this frequency band.

### 7.2 Bit Error Rate versus Signal to Noise Ratio

Bit error rate is found for various signals to noise ratio. Different signals to noise ratio are produced by varying the TX gain. BER vs. SNR is plotted for different modulation schemes and compared for different center frequencies, symbol rates. Bit error rate for different signals to noise ratio is found to evaluate the accuracy of concrete channel in transmitting the information.

#### 7.2.1 Bit Error Rate versus Signal to Noise Ratio for DBPSK

Figure 7.4 shows BER versus SNR for different center frequencies

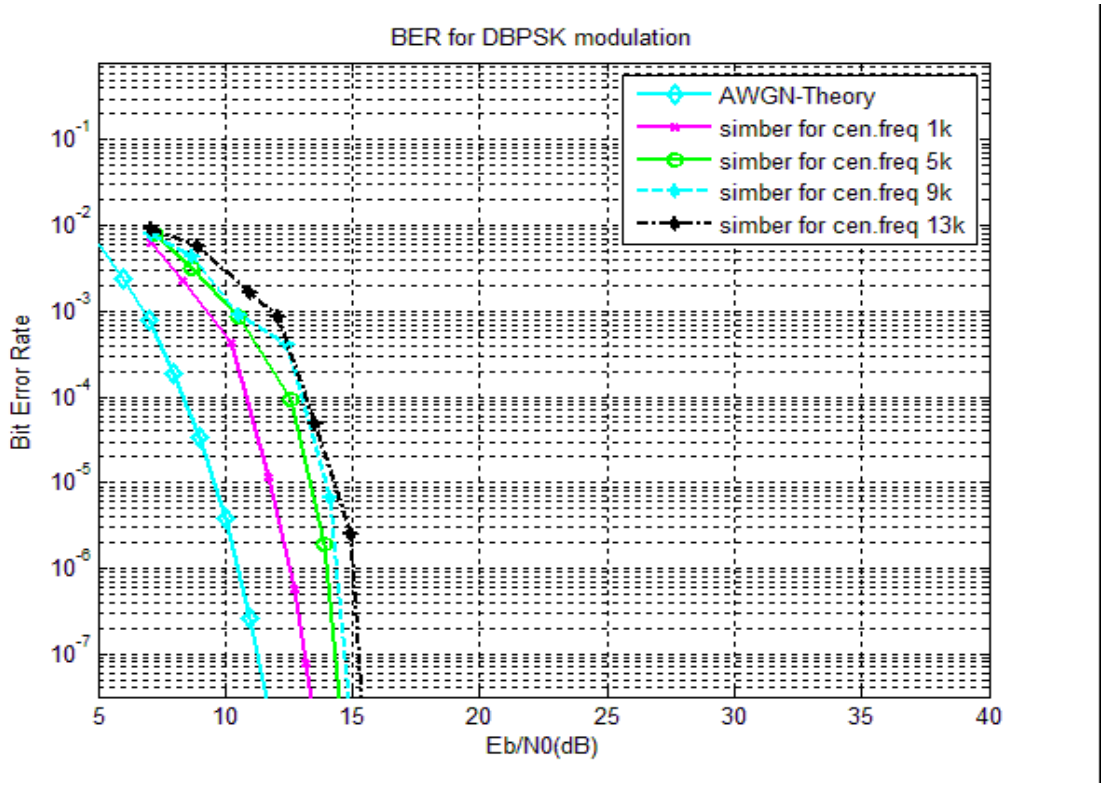


**Figure 7.4.** BER versus SNR for DBPSK for different center frequencies

This experiment is conducted for different center frequencies. Symbol rate was kept constant as 1K symbols/sec. As DBPSK represents 1 bit per symbol, data rate is

considered to be 1K bits/sec. The simulated Bit Error Rate (BER) for different center frequencies is compared with the theoretical BER in Additive White Gaussian Noise (AWGN) channel. Figure 7.5 shows BER versus SNR for different symbol rates

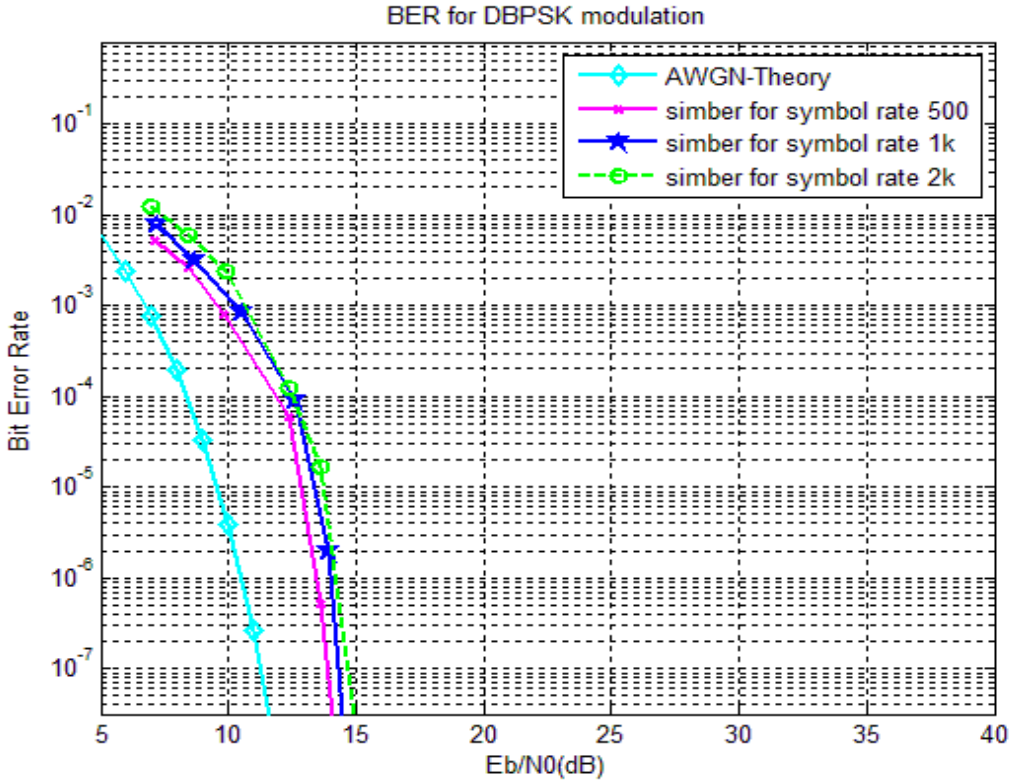


**Figure 7.5.** BER versus SNR for DBPSK for different symbol rates

This experiment is conducted for different symbol rates. The center frequency is considered to be 5 KHz. The simulated BER-SNR is compared with the theoretical BER-SNR in AWGN channel.

### 7.2.2 Bit Error Rate versus Signal to Noise Ratio for DQPSK

The first experiment is conducted for different center frequencies, considering the constant symbol rate of 1K symbols/sec. As in DQPSK, 2 bits represent a symbol. 1K

symbols/sec represent 2K bits/sec. Bandwidth efficiency is increased by two times when compared to DBPSK. Figure 7.6 shows the performance of BER-SNR for different center frequencies, while the performance under AWGN channel is added for comparison.

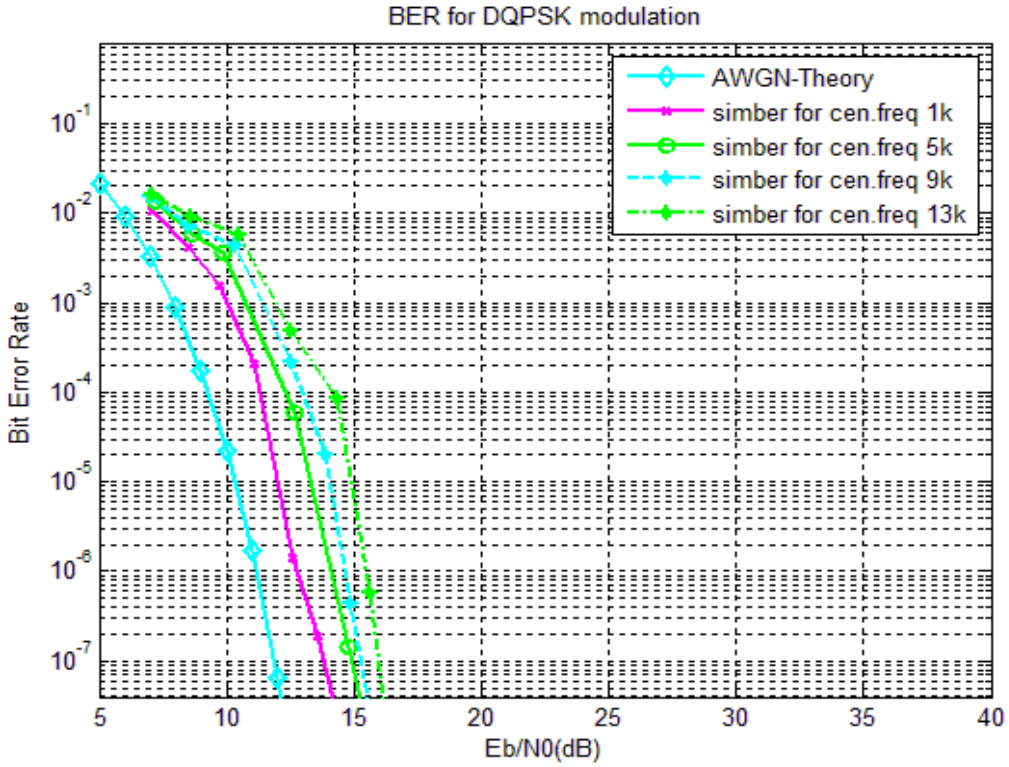


**Figure 7.6.** BER versus SNR for DQPSK for different center frequencies

Figure 7.7 shows BER versus SNR for different symbol rates, considering the center frequency as 5 KHz for all symbol rates.

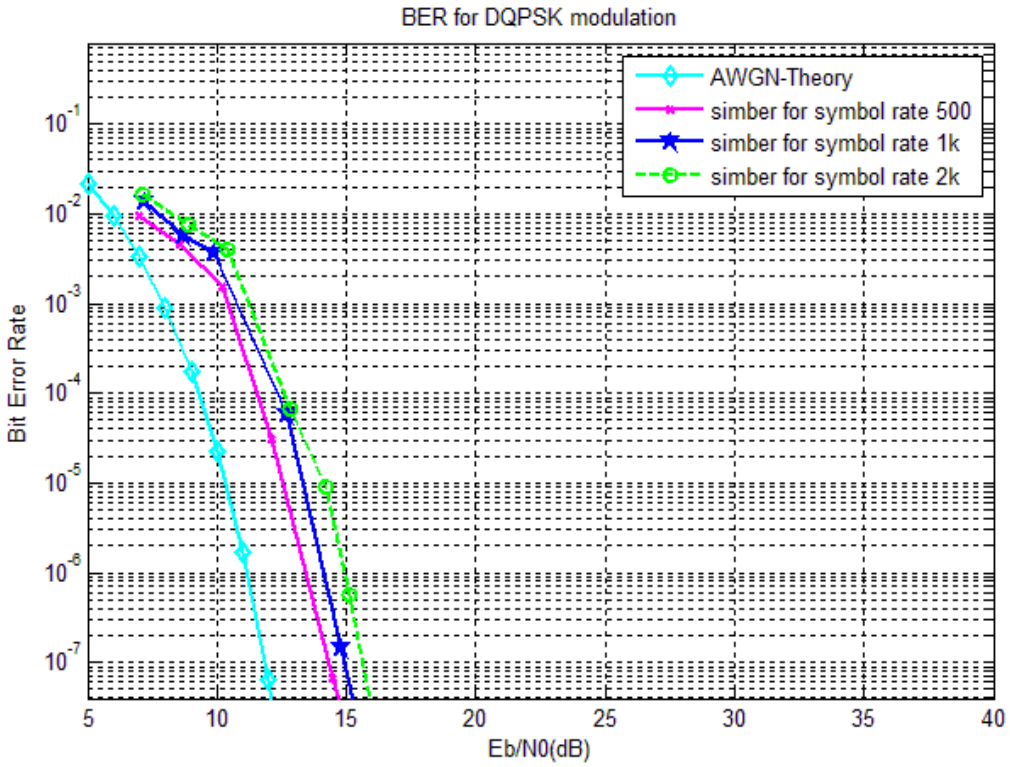


**Figure 7.7.** BER versus SNR for DQPSK for different symbol rates

### 7.2.3 Bit Error Rate versus Signal to Noise Ratio for D8PSK

The first experiment is conducted for different center frequencies, considering the constant symbol rate of 1K symbols/sec. As in D8PSK, 3 bits represent a symbol. 1K symbols/sec represent 3K bits/sec. Bandwidth efficiency is increased by three times when compared to DBPSK. Figure 7.8 shows the performance of BER-SNR for different center frequencies, while the performance under AWGN channel is added for comparison.

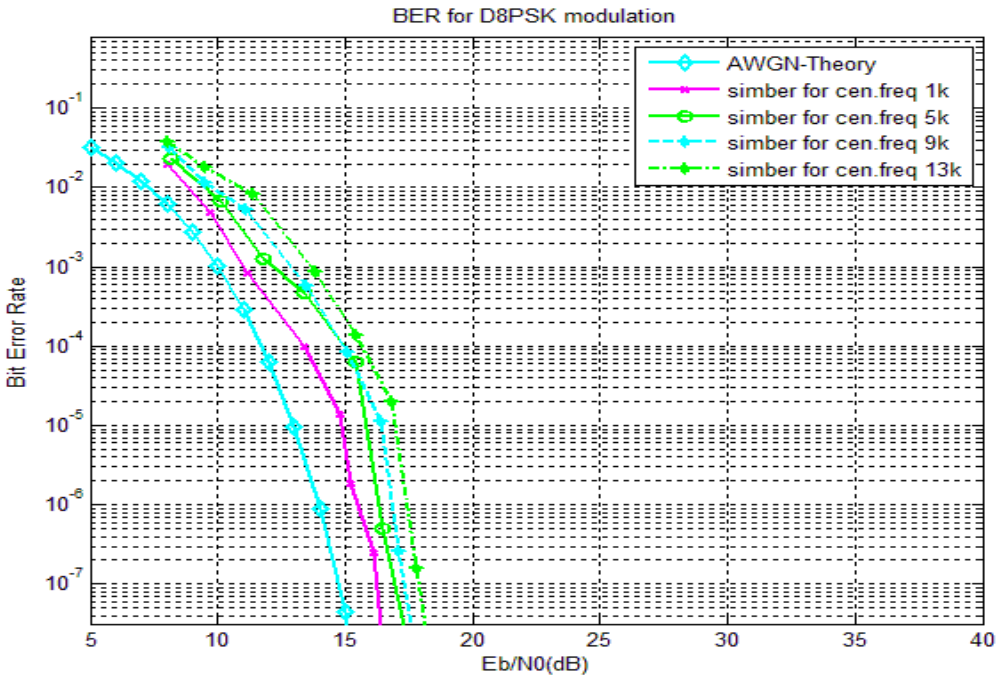


**Figure 7.8.** BER versus SNR for D8PSK for different center frequencies

Figure 7.9 shows BER versus SNR for different symbol rates. This experiment is conducted for different symbol rates, considering the center frequency as 5 KHz for all symbol rates.

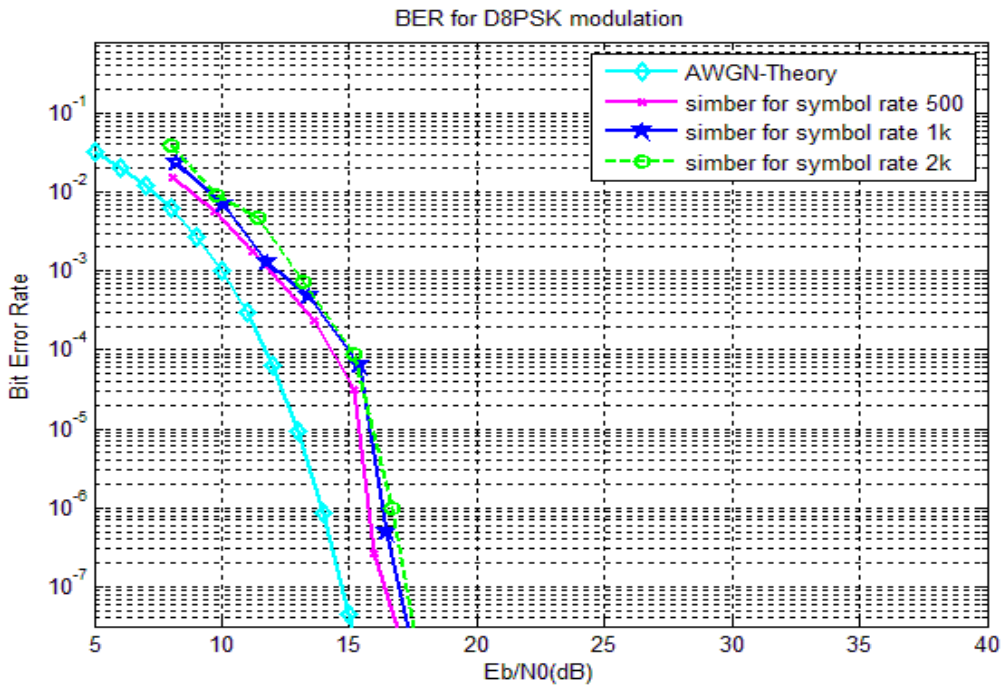


**Figure 7.9.** BER versus SNR for D8PSK for different symbol rates

### 7.3 Automatic Gain Control Circuit Results

Automatic Gain Control (AGC) Circuit on the receiver side is used to stabilize and improve the performance of the system as an attenuator rather than an amplifier. It works based on the value of the reference voltage in the last stage. AGC compares the output of the precision half wave rectifier to the reference voltage and generates the control voltage that is given as feedback to the analog multiplier. The DC value of the generated output of AGC is compared with the reference voltage until they both are equal to give the constant output

$$V_{ref} = \frac{V_p}{\pi}. \qquad (7\text{-}5)$$

So $V_p$ is the desired peak of the signal at the AGC output. $\frac{V_p}{\pi}$ is the output of the precision half wave rectifier. In another way, the value of reference voltage is chosen such that

$$V_{ref} = \frac{(Desired\ peak\ of\ the\ signal\ at\ the\ output\ of\ AGC)}{\pi} . \quad (7\text{-}6)$$

AGC works for any input signal whose peak is greater than the desired peak of the signal at the output of AGC. It attenuates the signal such that it reaches the desired peak of the signal at the output of AGC. If the input signal peak is less than the desired peak at the output of AGC, then it acts as the linear amplifier where output is followed by the input value.

### 7.3.1 Software simulation

Software simulation of AGC is done using LTSpice. The desired output of the AGC was chosen to be 320 Vpp, where $V_p$ = 160 mv. So the reference voltage is selected such that

$$V_{ref} = \frac{(Desired\ peak\ of\ the\ signal\ at\ the\ output\ of\ AGC)}{\pi} , \quad (7\text{-}7)$$

$$V_{ref} = \frac{160mv}{\pi} = 50.929mv . \quad (7\text{-}8)$$

If the DC value of the output of AGC is greater than $V_{ref}$, then it is attenuated until it reaches 320 Vpp. So, if the input is signal is greater than 320 Vpp, it is attenuated by AGC to give the constant output at 320Vpp. If the input signal is less than 320Vpp, then the output of ACG is equal to input.

The output of the AGC should be connected to LFRX daughterboard, which can take input up to 2 Vpp. So, the non-inverting amplifier to amplify the signal to 1.8Vpp follows AGC output. This is done to utilize the full range of LFRX daughterboard.

Figure 7.10 shows the input, output, and amplified output of AGC for an input signal of 3.2Vpp. The red signal represents the input signal. Blue signal represents the AGC output and green signal represents the amplified AGC output. The reference voltage is chosen as 50.92mv to give the constant output of 320mVpp.

Figure 7.11 shows the frequency response of AGC circuit designed. The frequency response of AGC is estimated for a single input signal 3.2 Vpp and the reference voltage is chosen as 50.92mv to give the constant output of 320Vpp. The blue line represents the actual output of AGC. The green line represents the output of the amplified AGC. As AGC acts as an attenuator, the gain of AGC is in the range of -9 dB. It is amplified using non-inverting amplifier to increase the gain to the range of 7 dB. The constant gain represents the working of AGC to give the constant output.

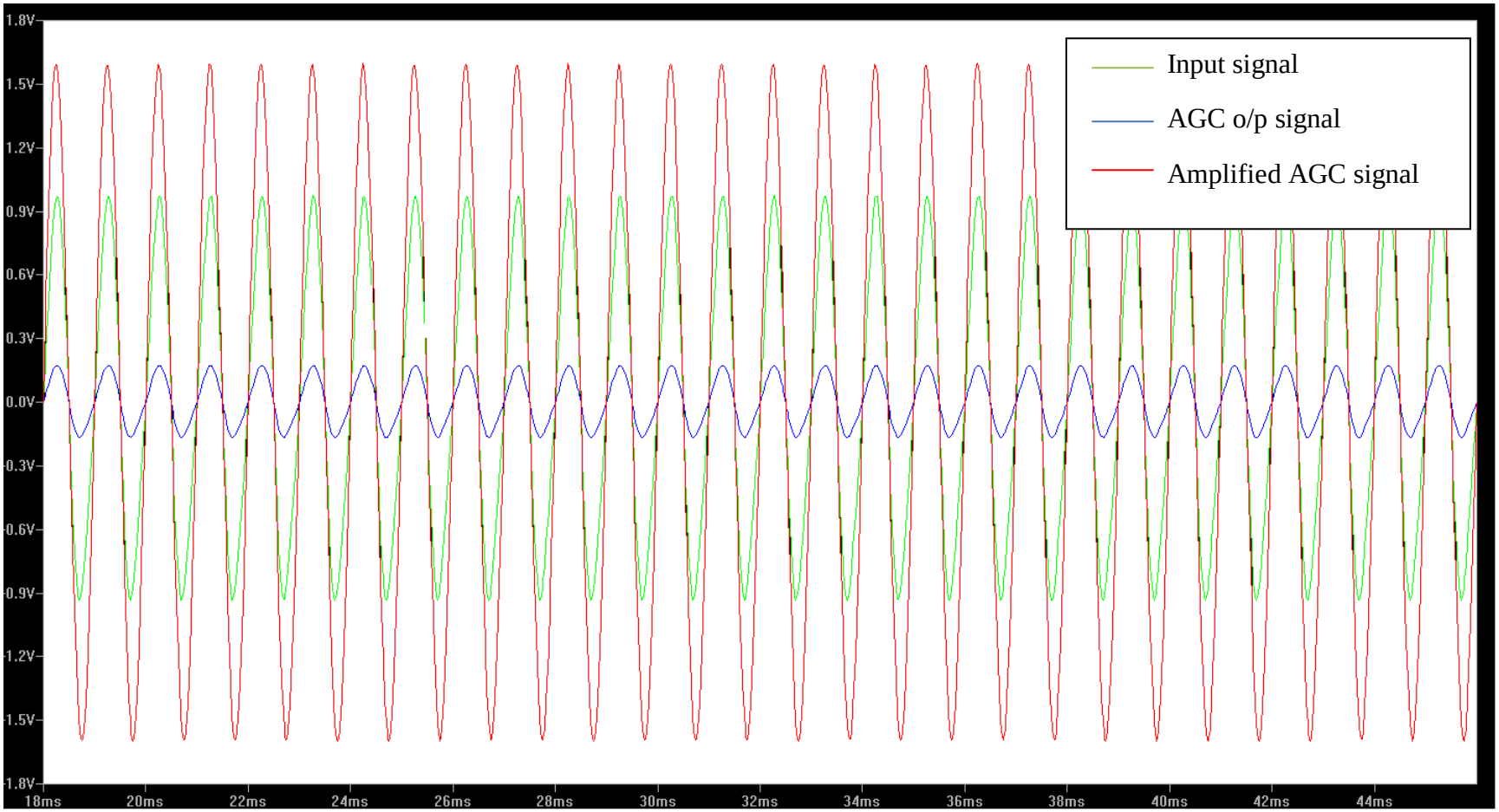


**Figure 7.10.** Input, Output and Amplified output of AGC in LTSpice

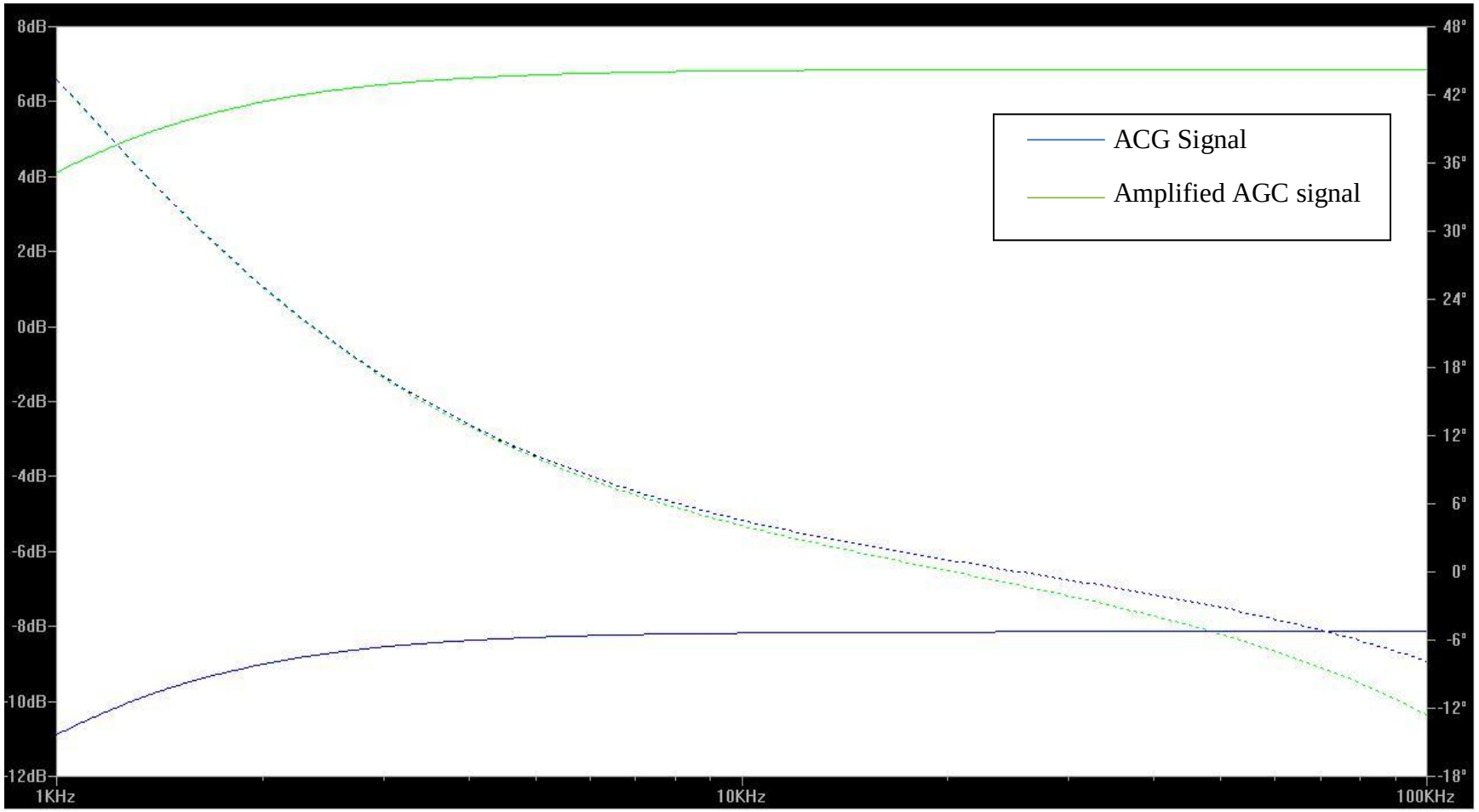


**Figure 7.11.** Frequency response of AGC in LTSpice

### 7.3.2 Hardware Implementation

Hardware implementation of AGC is performed on breadboard using AD 633 multiplier, LT 1056 Op-amps, IN4148 small signal diode, resistors, and capacitors. DC power supply is used for supply voltage of $\pm$ 15V. The reference voltage is chosen to give the constant output of 300mVpp. Using a voltage divider, reference voltage is generated from the power supply +15V. Variable resistor can be used in voltage divider to change the value of reference voltage. The circuit is tested for various input signal voltages for various frequencies.

Figure 7.12 shows the output of AGC for input signal of 1.6 Vpp at frequency 1 KHz. The input signal is attenuated to 300mVpp. Oscilloscope with two channels used in the channel response measurement was used to capture the input and the output of AGC. The green signal represents the input signal and the yellow signal represents the output of AGC. This signal is amplified to $\pm 0.9\,\mathrm{V}$ using non-inverting amplifier to give the amplified AGC output.

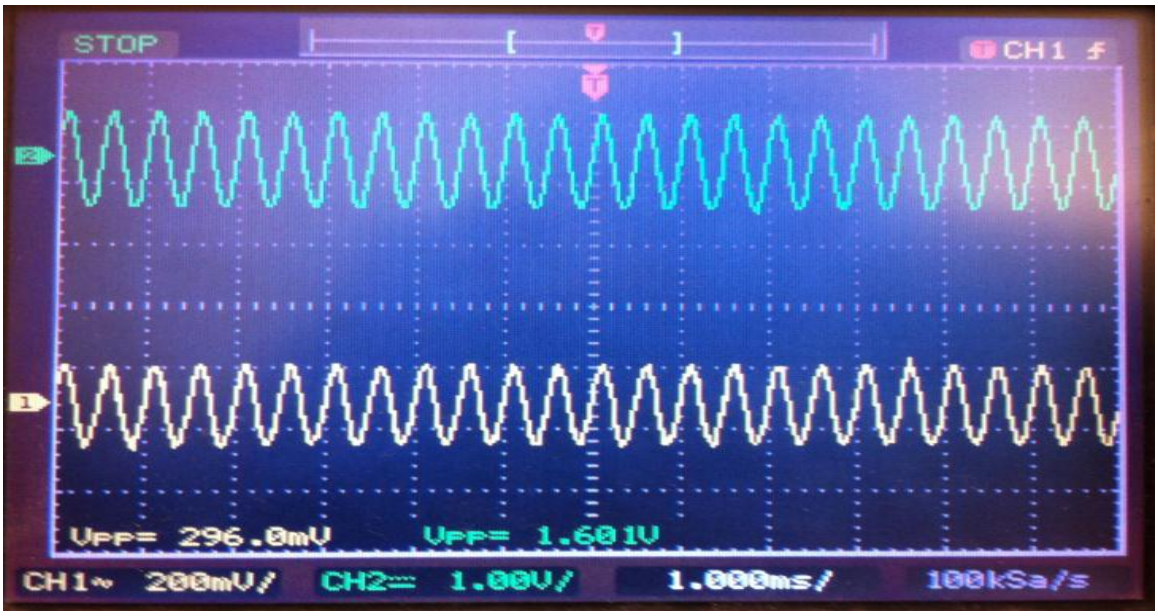


**Figure 7.12.** AGC output for 1 KHz signal for 1.6Vpp signal

Figure 7.13 represents the AGC input and output for 20 KHz signal for 850mVpp.

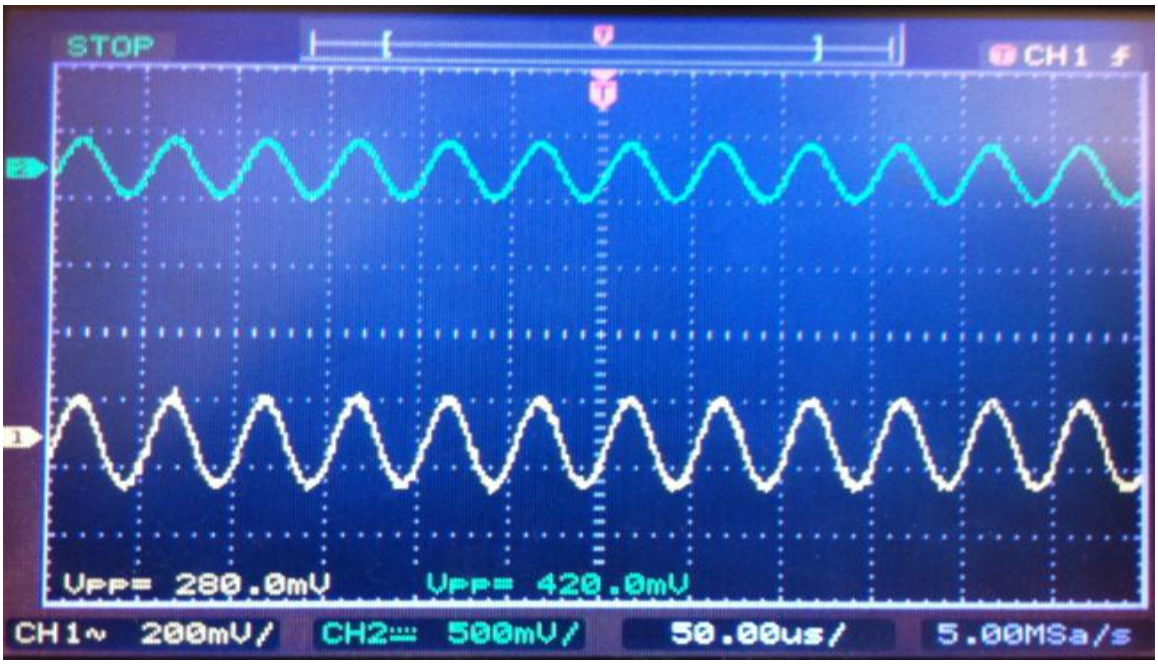


**Figure 7.13.** AGC output for 20 KHz for 420mVpp

If the input signal peak is less than the desired peak at the output of AGC, then the output follows the input. Figure 7.14 shows the AGC for input signal that is less than the desired peak at the output of AGC.

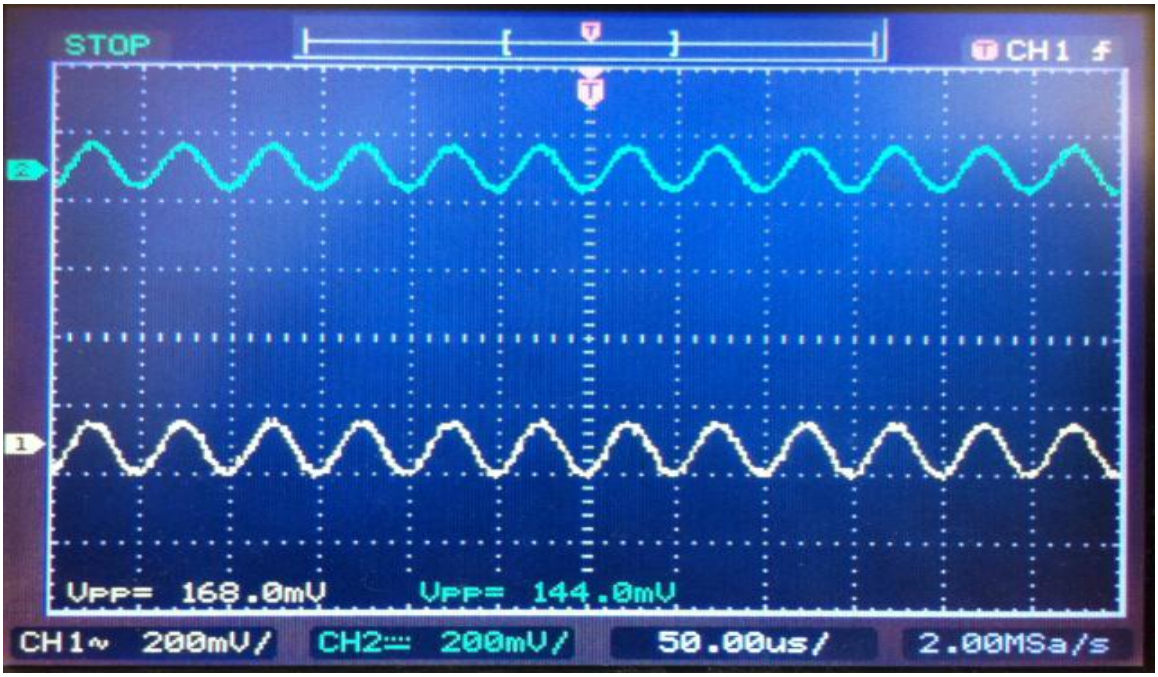


**Figure 7.14.** AGC Output for 20 KHz for 144mVpp

Hardware Implementation of AGC is successfully performed showing the AGC output to be linear with input for input signals less than the desired peak at the output and for input signal higher than the desired peak; it gets attenuated to reach the constant level. Figure 7.15 shows the output voltage for the range of input signal values. The reference value is chosen to be 320mVpp.

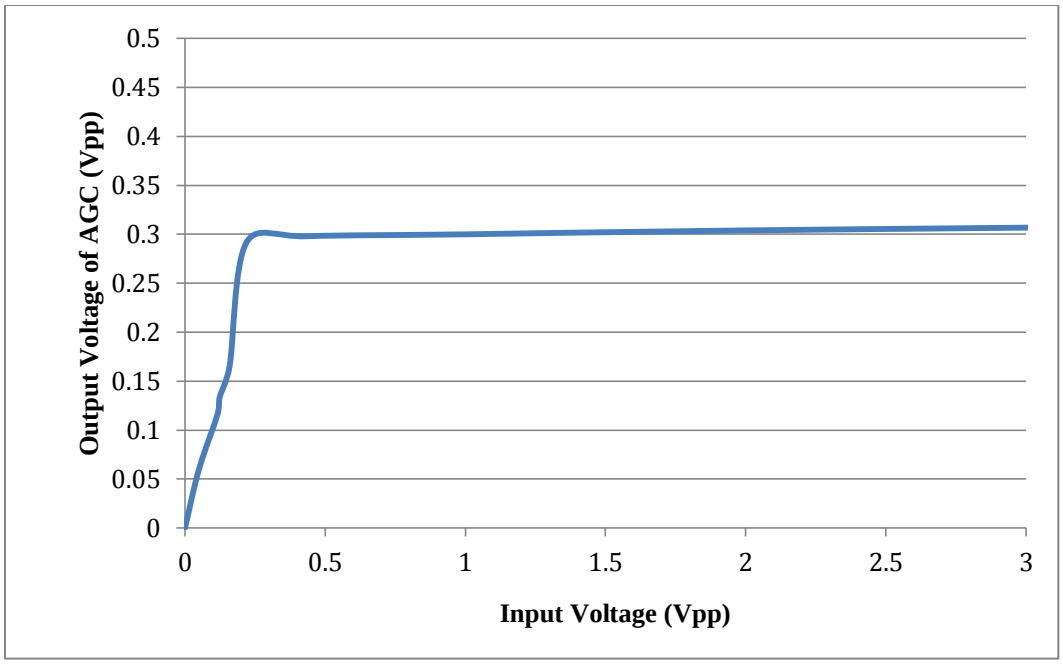


**Figure 7.15.** Input Voltage vs Output Voltage of AGC

### 7.4 Bit Error Rate versus Signal to Noise Ratio using AGC

After successful implementation of AGC, BER vs. SNR is plotted for different modulation schemes using the implemented AGC on the receiver side at the output of the concrete channel. BER – SNR performance is compared with and without AGC on the receiver for different modulation schemes. Figure 7.16 shows the BER – SNR performance for different modulation schemes with/without AGC.

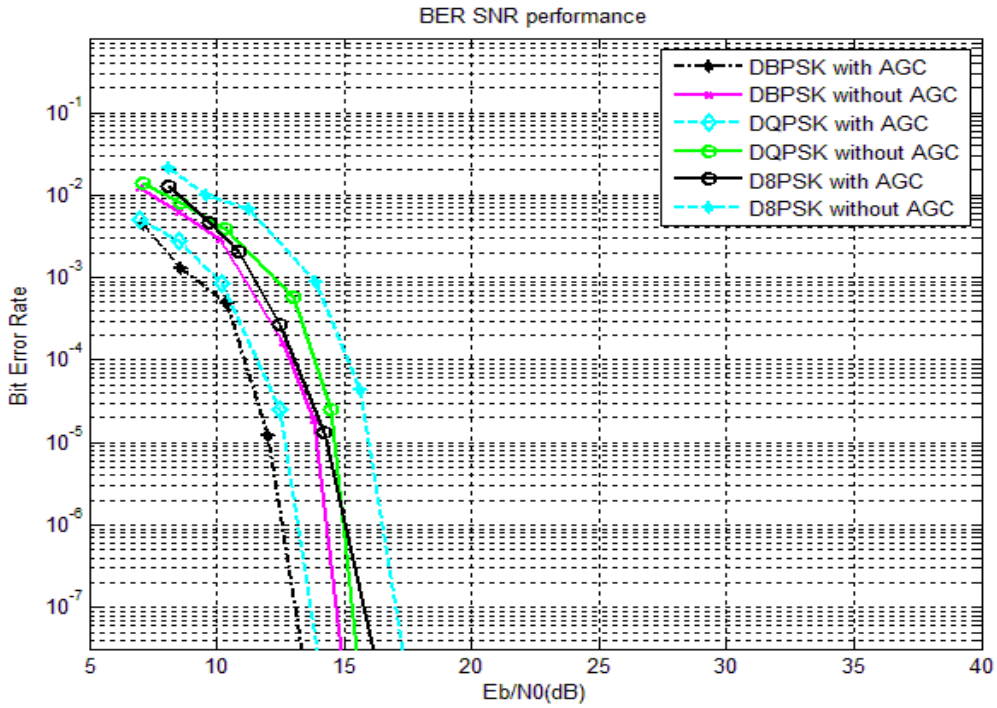


**Figure 7.16.** BER vs SNR with and without AGC

Center frequency is considered to be 9 KHz and Symbol rate is considered to be 3.3 Symbols/sec. The simulated results prove that AGC on the receive side improves the BER – SNR performance.

### 7.5 Summary

This chapter discussed the experimental results necessary in designing the effective communication system. Measurement of concrete channel response was performed using coherent detection method. BER – SNR performance was evaluated to find the accuracy of concrete channel in transmitting the information for various signals to noise ratios. Automatic gain control circuit was successfully simulated and implemented using hardware. The schematic was developed for PCB layout of AGC. BER – SNR performance is compared with and without AGC on receiver side.

# CHAPTER 8. CONCLUSION

## 8.1 Summary of Contributions

Communication through concrete has always been an arduous task with high electromagnetic attenuation in concrete structures. A network comprised of piezoelectric sensors and actuators has been devised to monitor the condition of concrete structures. A novel data communication scheme is designed that utilizes stress waves modulated with information for structural health monitoring applications.

Measurement of concrete channel response helped in finding the suitable frequency spectrum to send data through concrete. Different modulation schemes have been implemented using the designed communication system. Recovery of constellations has proved the capability of concrete channel in effectively transmitting the data. Bit error rate for various signals to noise ratio is found for different modulation schemes and compared based on center frequency, symbol rate to find the accuracy of concrete channel in transmitting the information. Automatic gain control (AGC) circuit has been successfully designed and implemented to improve the performance and stabilize the system.

Overall, an effective communication system to monitor the concrete structures is designed and it has been found that concrete can be effectively utilized as a communications channel.

## 8.2 Future Work

While these tests have shown to be conclusive and informative, there are many future tests that need to be performed on the concrete channel. To enhance the data

throughput and to reduce the multipath fading, multiple input multiple output (MIMO) system is preferable to single input single output (SISO) system. One of the first objectives would be the feasibility for MIMO communications, and therefore testing systems using FDMA or CDMA would be helpful in discussing the full application of the concrete communication channel. More comprehensive tests are required using at least two USRP transmitters and one USRP receiver. These tests can aim to measure the BER of a system that had two or more transmitters and one receiver decoding both messages at the same time. Testing the ability of the system with the presence of noise would also be a useful test that would demonstrate the system's capabilities in a typical noisy scenario.

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