NOVEL CONTROL ALGORITHMS FOR POWER QUALITY IMPROVEMENT USING FOUR-LEG CONVERTER

by

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ABSTRACT

In a three-phase four-wire microgrid system, a significant number of end-user devices are unevenly distributed with largely unpredictable switching on or off characteristics both in time and space. Under such circumstances, substantial negative and zero sequence currents are drawn from the utility grid resulting in disrupting the sensitive devices, overheating the neutral conductors, and damaging the power generating sources. Such problems further aggravate by degrading the active power flow capacity of the distributing system with leading or lagging power-factor currents in the presence of reactive loads.

A shunt converter, such as a four-leg converter, can be used to mitigate the above-mentioned power quality (PQ) problems in a three-phase four-wire microgrid system. However, the effectiveness of the four-leg converter mainly depends upon the control techniques. Thus, this dissertation focuses on the control algorithms for the four-leg converter to eliminate the PQ problems caused by different loading conditions in a three-phase four-wire system. Also, as an extension of this work, the use of a stand-alone four-leg converter in an aircraft power generation system is investigated to improve the power quality as well as transient and dynamic performance during load-on and load-off operations for aircraft loads.

First, a detection technique using reduced order generalized integrator (ROGI) is investigated to achieve accurate and rapid detection of unbalanced currents. Next, a novel decoupling method named double reduced-order generalized integrators (DROGI) is proposed for the four-leg converter. Such a strategy decouples the compensation mode (DC-AC) and rectification mode (AC-DC) of the converter. As a result, more flexibility

and selectivity in terms of control methods are achieved. Further, based on DROGI, grid voltage modulated direct power control (GVM-DPC) without PLL is proposed to eliminate the impact of PLL. Moreover, considering unbalanced nonlinear grid/load conditions, a novel method, namely triple-ROGI, is proposed to compensate and absorb the required current, and provide selective harmonic currents to the system. These control algorithms are verified by simulation and experimental results. Also, a control strategy, named dual current control, is proposed for stand-alone four-leg converter in aircraft power generation system. The effectiveness of the control method is validated by simulation results.

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Introduction

1.1 Motivation

With the advancement of power electronics, renewable energy resources (RES) such as photovoltaics and wind energy are being increasingly used for generating electrical power [1]–[3]. Such systems, along with the improvement of system efficiency and flexibility, has promoted the installation of RES and led to a new paradigm- microgrid (MG) [4]. Fig. 1.1 shows a typical scheme of a microgrid, which can be considered as a three-phase four-wire system [5]. Apart from the electrical main grid, several other generation units, known as distributed power generation (DPG), are integrated into the microgrid system as well. As a result, the electrical system is modified from the typical structure (Generation-Transmission-Distribution) to a decentralized system [6].

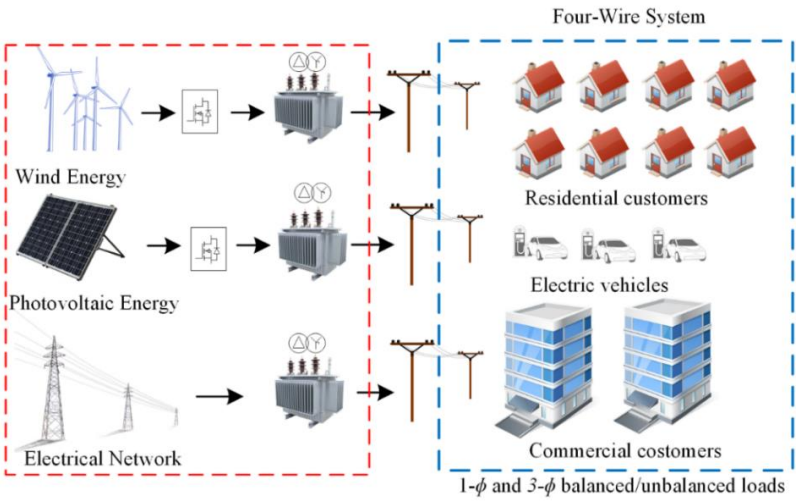


Figure 1.1: The typical scheme of a three-phase four-wire microgrid.

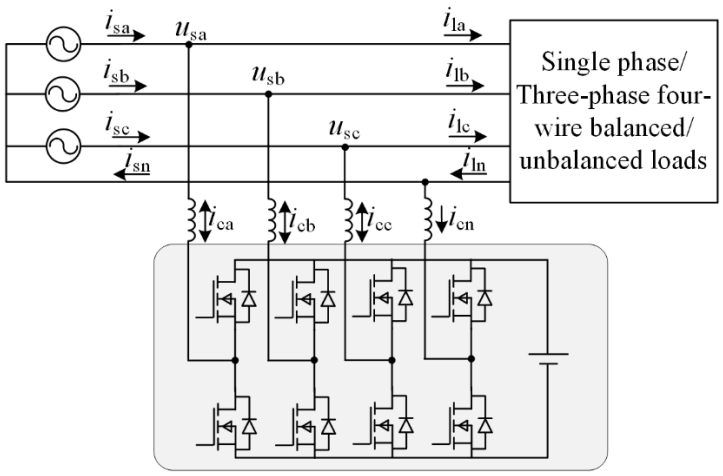


Figure 1.2: The structure of the four-leg converter.

The MG has two types of operation, grid-connected or islanded mode. However, unlike the main grid, the power capability of a typical MG is typically low(<1MW), and cannot supply load changes instantly, so a weak grid in the isolated MG is prominent [7]. Also, from Fig. 1.1, it can be seen that several distributed loads (single-phase loads) are connected to the MG, like domestic lighting, fan, and computer power supplies. Such uneven distribution causes unbalanced/nonlinear loads and adds negative effects to the isolated MG. Even though utilities take measures to equally distribute loads among all the three phases, some unbalanced loading conditions still take place. This situation may lead to adverse power quality (PQ) problems, such as poor power factor, unbalanced currents, increased neutral current, and increased harmonics. Such PQ problems could cause [8, 9]:

1. Malfunctioning of protection relays and measuring instruments.
2. Increased losses in the distribution transformer (zero sequence currents circulating in the delta side).
3. Unexpected noise and vibration of electric machines due to negative-sequence currents.

4. Low system efficiency (poor power factor operation).

Also, in isolated MG, the grid is not able to avoid the voltage sag, swell, unbalance, and harmonics across the consumers' load end [10]. Thus, power quality issues become significant and create challenges for load balancing and harmonics compensation in isolated MG.

Among the many techniques for mitigating the power quality problems in an isolated MG, a four-leg converter operating as a shunt compensator is extensively used for minimizing the above mentioned PQ problems [11, 12]. In general, the first three legs of the converter are connected in shunt across the point of common coupling (PCC), while the fourth leg is connected to the neutral point of the system, as shown in Fig. 1.2. Such configuration enables the converter to balance the three-phase currents drawn from the AC source, reduce neutral current, and compensate harmonic currents (if required) and reactive power. Another interesting application for the four-leg converter is found in the aerospace industry. The electrical system of an aircraft can be considered as a three-phase four-wire isolated MG [13]. However, in this case, rather than operating as a shunt compensator, the four-leg converter operates as an inverter (stand-alone converter) supplying 400 Hz, 115V *RMS* phase voltage to the load.

Regardless of the application, either 60 *Hz* in isolated MG or 400 *Hz* in aircraft electrical generation system, the control technique for four-leg converter in terms of reliability, fast dynamic response, and accuracy is a matter of high interest and challenging task.

1.2 Research objectives

This dissertation focuses on the control algorithms for a four-leg converter to improve power quality in a microgrid system with balanced and unbalanced loads. The work is further extended to develop novel control strategies for the operation of standalone four-leg converter in More Electric Aircraft systems to achieve better power quality and response time.

1.2.1 Novel Unbalanced Currents Detection Method

Under unbalanced loading conditions, to ensure the efficiency and stability of isolated MG, only positive sequence current is supposed to be generated by DPG, and the detection of unbalanced currents should be accurate and rapid. To ensure efficient and stable operation of Distributed Power Generation, only positive sequence current should be generated from DPG even during unbalanced loading conditions. To achieve proper unbalanced current compensation, an accurate and rapid detection scheme of unbalanced currents is necessary. Although numerous detection methods are proposed in the literature, like instantaneous reactive power theory (IRPT) and synchronous reference frame theory (SRFT), the dynamic response performance of these techniques is poor [14]–[16]. Thus, a novel strategy, named reduced-order generalized integrator (ROGI) for unbalanced current and voltage detection scheme is proposed in this thesis [17]. Because of polarity selectivity and filtering capability of ROGI, the proposed method can decompose the positive-/ negative-/ zero-sequence components of unbalanced currents accurately and rapidly. Furthermore, a ROGI based control algorithm is developed for a four-leg converter whose DC bus is supported by a DC power supply. The feasibility of the proposed method is demonstrated by computer simulation results.

1.2.2 Decoupling Control Algorithms under Unbalanced Linear Loads

To reduce the size of the shunt compensator (four-leg converter), the DC bus voltage can be supported with DC capacitors, rather than a separate DC power supply. However, such configuration results in a challenging task for designing the controller. This is because the converter is not only required to compensate unbalanced loads with required sequential currents, but also to absorb positive currents from the grid to maintain the DC link voltage. To achieve this, a novel control algorithm using double reduced-order generalized integrators (DROGI) for a four-leg shunt converter is proposed [18]. The first integrator is adopted to extract required reference compensation currents for power quality improvement and the second one is to decouple compensation currents and rectification currents of the converter side. The reference rectification currents are generated using an outer-loop DC-link voltage controller (PI) and are synchronized to the three-phase voltages. Since the compensation mode (DC-AC) and rectification mode (AC-DC) of the converter are decoupled and regulated separately, the four-leg converter operation with a good dynamic response, robust performance, and flexible controllability are achieved. Moreover, another novel control algorithm named grid voltage modulated direct power control (GVM-DPC) without PLL for the four-leg converter is proposed as well [19]. The effectiveness of the proposed algorithm is validated by simulation and experimental results.

1.2.3 Triple-ROGI Based Control Method under Unbalanced Distorted Loads/ Grid Condition.

Under unbalanced distorted loads/ grid conditions, the converter should compensate and absorb the required currents with respect to the positive sequence components of grid voltages. However, the limitation of conventional Synchronous Reference Frame (SRF)

PLL is that it cannot achieve sufficient harmonic filtering and fast dynamic response. The problem may get worse when the grid voltage is particularly unbalanced.

To accurately extract the fundamental frequency positive sequence component in grid voltage, ROGI based PLL is proposed. Thanks to the characteristics of ROGI, which helps to extract the positive sequence components of unbalanced grid voltage for obtaining the PLL. This novel structure of PLL with a pre-filtering ROGI features high filtering capability, fast dynamic response, and simple structure. Also, to compensate selective harmonic currents in the system (like 1^{st}, 3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th}, and 17^{th} order), multiple proportional resonant (PR) controllers are employed. As a result, the PQ problems caused by unbalanced nonlinear loading condition is mitigated. The detailed operation and verification are conducted by simulation and experimental results.

1.2.4 Dual Current Control Strategy for Stand-alone Four-leg Converter

As an extension, ROGI based controller is applied to an aircraft electrical system by considering it as a three-phase four-wire microgrid system. Rather than operating as a shunt compensator, the four-leg converter operates as an inverter (stand-alone converter) supplying 400 Hz, 115V RMS phase voltage to electrical loads. Further, the operational challenges during the unbalanced load condition to maintain the balanced output voltage of the generation system also need to be addressed.

To ensure the generation system to supply only positive sequence voltage to the loads, a dual current control strategy is proposed for the four-leg converter. The output voltages and currents of the converter are decomposed using ROGI. Further, the detected positive and negative sequence voltage are controlled in their respective d-q domain (positive sequence d-q co-ordinate is counterclockwise and negative sequence d-q co-ordinate is

clockwise). The feasibility of the operation of the proposed control strategy is demonstrated by simulation in MATLAB/Simulink.

1.3 Summary of Dissertation Organization

This dissertation is organized as follows:

Chapter 2 provides a novel unbalanced current detection method which is a reduced-order generalized integrator (ROGI). This method features high filtering capability, fast dynamic response, and simple structure. Also, based on ROGI, a control algorithm is developed for the four-leg converter whose DC bus is supported by the power supply. The feasibility of the proposed method is demonstrated by simulation results.

Chapter 3 presents two novel decoupling control strategies for the four-leg converter under unbalanced linear loads. One control method is double reduced-order generalized integrator (DROGI) for shunt compensation of unbalanced loads. One integrator is operated on load currents to obtain the reference compensation currents and the second one is used to decompose the converter currents. The reference rectification currents are generated using a PI controller to regulate the DC link voltage at its reference value. As a result, the compensation currents for improving power quality and rectification currents for maintaining DC link voltage are decoupled and regulated separately. The other algorithm, namely grid voltage modulated direct power control (GVM-DPC) is to form the non-PLL control system. The feasibility of the proposed control strategies is demonstrated by both simulation and experimental results.

Chapter 4 presents the control algorithms for four-leg converter under unbalanced nonlinear loads/grid conditions. First, a novel control algorithm is proposed to compensate

for unbalanced non-linear loads in three-phase four-wire isolated MG. The detection and compensation for unbalanced non-linear load currents are implemented using DROGI with a proportional resonant (PR) controller, such that the four-leg converter can compensate for selective harmonic currents to the system. Further, considering the distortion of grid voltage and nonlinear unbalanced loading conditions, another novel method namely triple-ROGI is proposed for the four-leg converter. The positive sequence components of distorted supply voltages are extracted by employing ROGI based PLL in this case. As a result, the four-leg converter compensates and absorbs the required currents with respect to the positive sequence components of grid voltages. Even under distorted voltage supply and unbalanced nonlinear loading conditions, the DPG still supplies constant magnitude with sinusoidal balanced currents to the system. The effectiveness of the proposed algorithms is validated by simulation and experimental results.

Chapter 5 presents a dual current control strategy for the four-leg converter during stand-alone operation. First, the output voltage of the converter is sensed and transformed into $\alpha\beta$ domain. ROGI is used to decompose the positive and negative sequence components of the output voltage. Further, the detected positive and negative sequence voltage are controlled in their respective d-q domain (positive sequence d-q co-ordinate is counterclockwise and negative sequence d-q co-ordinate is clockwise). PI controller is used to regulate the voltage to its reference value. Finally, the output of the controller is converted into modulation signal in *abc* domain and 3D-SVM is used to drive the four-leg converter.

Chapter 6 summarizes the contributions of the work and proposes recommendations for the follow-on research in the areas of PCC voltage regulation strategy, fault-tolerant operation of the four-leg converter, and modulation simplification.

Chapter 2

A Novel Method Based on Reduced Order Generalized Integrator for Detection of Unbalanced Currents

2.1 Introduction

In a three-phase four-wire microgrid system, numerous single-phase loads such as domestic lightings, fans, and microwave ovens are connected to the grid. Such unevenly distributed loads may cause substantial negative and zero sequence currents drawn from the AC source, thereby de-energizing the sensitive loads, and overheating neutral conductor [20]–[22]. However, a four-leg converter operating as a shunt compensator, shown as Fig. 2.1, is an effective way to address this issue by compensating desired currents (negative and zero sequence currents) to the system so that the AC source only needs to supply positive sequence active power to the system with balanced currents [23]. But, as discussed in [24], the detection method extracting the desired compensation currents affects the compensation performance of the four-leg converter intensely. Thus, a proper unbalanced currents detection scheme with a fast dynamic response, easy structure, and precise detecting are necessary to investigate and develop.

Various methods separating the positive, negative, and zero sequence components of unbalanced currents have been reported in the literature [25]–[27]. Instantaneous symmetrical component (ISC) theory proposed by Charles Legeyt Fortescue calculates the positive and negative sequence component in a stationary ($\alpha\beta$) reference frame [25]. It

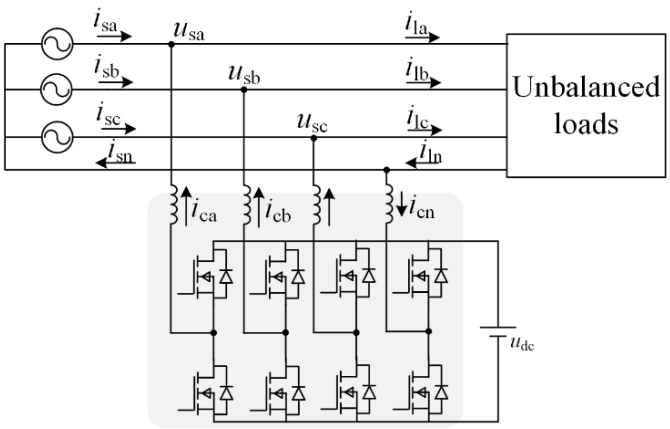


Figure 2.1: The structure of the four-leg converter with DC power supply.

multiplies the transformation matrix by the phasor representation of the unbalanced currents and decomposes the positive and negative sequence components rapidly. However, this method is only suitable for fundamental frequency unbalanced currents and sensitive to the harmonics [28]. Another approach named the double decouple synchronous reference frame (DDSRF) can effectively extract the fundamental frequency sequence components of the unbalanced currents and attenuate the harmonic currents [29]–[31]. This method exploits two synchronous reference frames rotating at the fundamental frequency (one counterclockwise for positive sequence component and the other one clockwise for negative sequence component). As a result, the positive sequence components and negative sequence components can be isolated and extracted. However, due to the inherent drawback of SRF, such strategy suffers from poor dynamics [32]. To increase the dynamic response, an alternative technique combining dual second-order generalized integrator (DSOGI) as a pre-filter is proposed in [33]. The unbalanced currents are transformed to the stationary ($\alpha\beta$) reference frame, and the fundamental frequency α and β components are extracted and delayed with 90 degrees by using DSOGI. Furthermore, these signals are used as ISC to calculate the positive and negative sequence components. The dynamic

response of this method is fast, but the estimation of positive and negative sequence components suffers from oscillatory ripples, and the operating principle is complex [34].

To address the aforementioned issues, this chapter presents a novel reduced-order generalized integrator (ROGI) based method for the detection of 3-phase unbalanced parameters. It features unity gain and zero phase shift response at integrator frequency, such that the positive and negative sequence components of unbalanced quantities can be extracted accurately and rapidly. Furthermore, a ROGI based control algorithm is proposed for the control of the four-leg converter whose DC link is fed with an active DC power supply. The detailed operation of the control algorithm is explained below. The feasibility of the proposed method is demonstrated by computer simulation results as well.

2.2 Unbalanced Currents Detection Scheme

To extract the positive and negative sequence components of the unbalanced current, a novel reduced-order generalized integrator (ROGI) based detection method is applied in this chapter. The transfer function of ROGI in *s* domain can be expressed as

$$F(s)=\frac{1}{s-j\omega}, \tag{2.1}$$

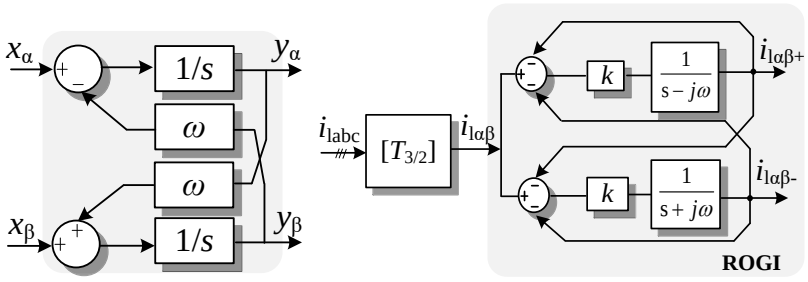
where ω is the fundamental angular frequency of the grid.

To implement ROGI in the digital signal processor (DSP), j in the denominator of equation (2.1) is replaced by the relationship of $x_\alpha=jx_\beta$ in the $\alpha\beta$ reference frame [35]. Fig. 2.2(a) shows the block diagram of ROGI. The positive and negative sequence detection schemes based on ROGI are also represented in Fig. 2.2(b). The transfer functions of $i_{l\alpha\beta+}$, $i_{l\alpha\beta-}$ and $i_{l\alpha\beta}$ can be obtained as

$$\begin{cases} i_{l\alpha\beta+} = \dfrac{k(s+j\omega)}{s^2+2ks+\omega^2} i_{l\alpha\beta} \\ i_{l\alpha\beta-} = \dfrac{k(s-j\omega)}{s^2+2ks+\omega^2} i_{l\alpha\beta} \end{cases}, \tag{2.2}$$

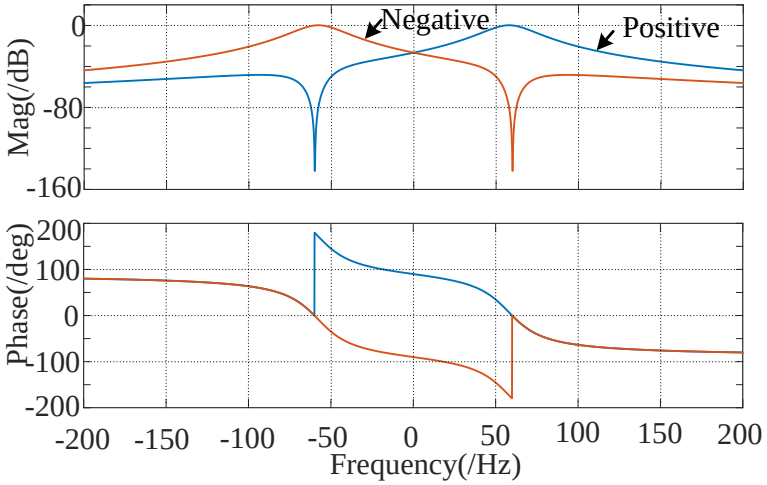
where $i_{l\alpha\beta+}$ and $i_{l\alpha\beta-}$ are positive and negative components of unbalanced load currents, k is the coefficient to tune the dynamics of ROGI.

The parameter k in equation (2.2) is required to be chosen judiciously based on the requirement of fast dynamics and good harmonic rejection capability. Fig. 2.3(a) shows the bode plot of sequence extraction transfer functions in equation (2.2). It can be observed that for the positive sequence component, ROGI operates as a band-pass filter at 60Hz, but

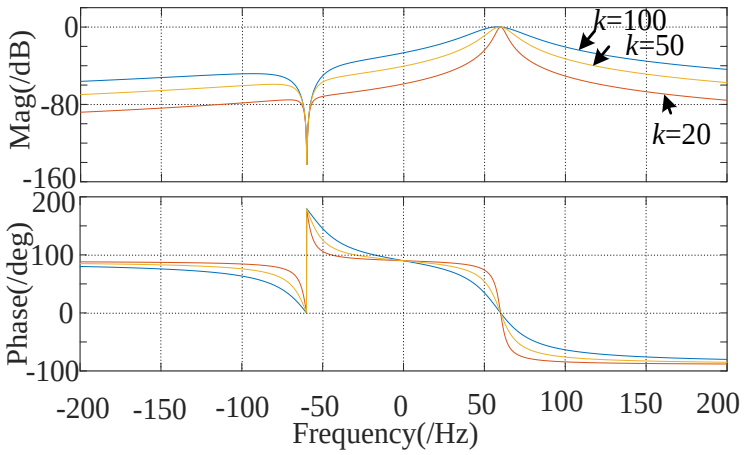


(a) (b)

Figure 2.2: Blocks of ROGI control method. (a) Implementation of F(s). (b) ROGI based detection scheme.



(a)

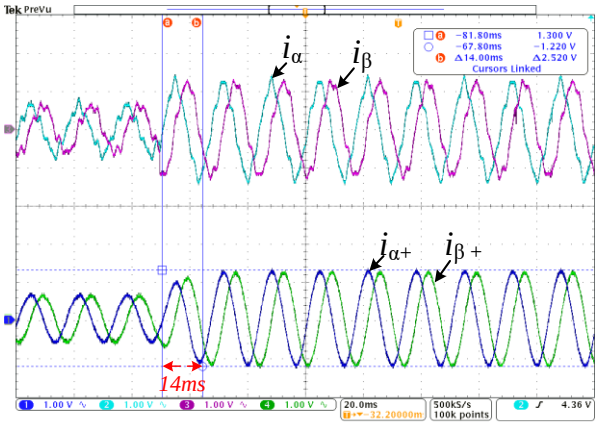


(b)

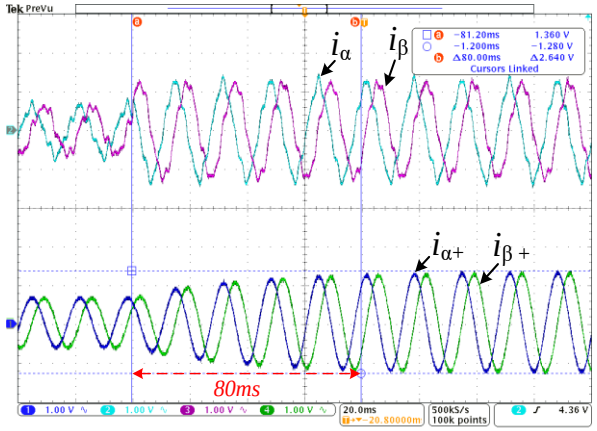
Figure 2.3: Bode plot of sequence extraction transfer functions. (a) Bode plot of ROGI (k=100). (b) Bode plot of ROGI with various *k*.

as a notch filter at -60Hz. Similarly, for the negative sequence component, the ROGI operates as a band-pass filter at -60Hz, but as a notch filter at 60Hz. Therefore, ROGI has the characteristics of frequency and polarity selectivity. Moreover, unity gain and zero phase shift response at integrator frequency ensure that ROGI does not introduce any delay in the system as well. Fig. 2.3(b) is the bode plot of positive sequence extraction transfer function with different values of *k*. It can be observed that the bandpass of ROGI becomes narrower with a decrease in *k* value, which makes the system respond with slower dynamic but with better filtering capacity and high selectivity. To enable the system with better dynamics, the value of *k* is chosen as 100 in this case. Moreover, for digital implementation of ROGI in DSP, equation (2.2) is discretized using the trapezoidal method [36] from *s* domain to *z* domain as

$$\begin{cases} i_{l\alpha+} = \dfrac{T_s}{2}\left[i_{l\alpha}(n)+i_{l\alpha}(n-1)+i_{l\alpha+}(n-1)\right]-\dfrac{\omega T_s}{2}\left[i_{l\beta+}(n)+i_{l\beta+}(n-1)\right] \\ i_{l\beta+} = \dfrac{T_s}{2}\left[i_{l\beta}(n)+i_{l\beta}(n-1)+i_{l\beta+}(n-1)\right]+\dfrac{\omega T_s}{2}\left[i_{l\alpha+}(n)+i_{l\alpha+}(n-1)\right] \end{cases}, \quad (2.3)$$



(a)



(b)

Figure 2.4: Experimental waveforms of unbalanced currents and its positive components in αβ reference frame. (a) k=100. (b) k=30.

where T_s is sampling time and is chosen to be the same as the switching period in this chapter.

To verify the filtering capacity and polarity selectivity of ROGI, an experimental test is performed with distorted inputs to ROGI. Fig. 2.4 shows the variation of unbalanced currents and the respective extracted positive sequence currents in the αβ reference frame with different values of k. A step-change in unbalanced currents is performed to further verify the dynamic response of ROGI. It can be seen that ROGI can detect the positive sequence currents and filter out other frequency harmonics. Meanwhile, by increasing the

value of *k*, the time required for detecting unbalanced currents is reduced and the dynamic performance of ROGI is improved. These results match with the above-discussed analysis.

2.3 ROGI Based Control Algorithm for the Four-leg Converter

Fig. 2.5 shows the block diagram of the control scheme using ROGI for the four-leg converter. First, the unbalance load currents are sensed and transformed into positive and negative sequence components with the help of ROGI. Then, the detected positive sequence active power demand from the load side can be expressed as

$$\bar{P}_{+} = u_{s\alpha} \cdot i_{l\alpha+} + u_{s\beta} \cdot i_{l\beta+}, \tag{2.4}$$

where $u_{s\alpha}$ and $u_{s\beta}$ are the grid voltages in $\alpha\beta$ domain. Furthermore, the desired compensation currents can be derived as

$$\begin{bmatrix} i_{ac}^{*} \\ i_{bc}^{*} \\ i_{cc}^{*} \end{bmatrix} = \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} - \underbrace{\sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \frac{1}{u_{s\alpha}^{2} + u_{s\beta}^{2}} \begin{bmatrix} u_{s\alpha} & -u_{s\beta} \\ u_{s\beta} & u_{s\alpha} \end{bmatrix} \begin{bmatrix} \bar{P}_{+} \\ 0 \end{bmatrix}}_{T_{pq/abc}}. \tag{2.5}$$

Finally, these reference currents are used by the current controller to generate PWM signals for the four-leg converter. A proportional controller is used as the current controller, and its design method is explained below.

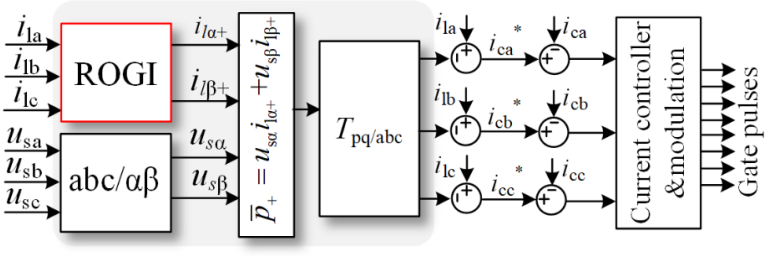


Figure 2.5: ROGI based control algorithm for the four-leg converter.

2.3.1 Current Controller Design

To achieve desired current compensation, the reference currents given in equation (2.5) should be tracked accordingly. In general, the current control system in the converter should operate as a first-order lag system, which is expressed as

$$T\frac{di_c}{dt}+i_c(t)=i_c^*(t), \tag{2.6}$$

where T is the time constant of the first-order lag system.

Further, applying Kirchhoff voltage law (KVL) to analyze the voltage across inductor L in Fig. 2.1 yields

$$\frac{di_c}{dt}=\frac{u_r(t)-u_s(t)}{L}=\frac{G_{pwm}m(t)-u_s(t)}{L}, \tag{2.7}$$

where G_{pwm} is the gain of the converter, m(t) is modulation signal, u_{r}(t) is the pole voltage of converter, and u_{s}(t) is the grid voltage. Substituting equation (2.7) into (2.6), the modulation signal can be derived as

$$m(t)=\frac{L}{G_{pwm}T}\left[i_s^*(t)-i_s(t)\right]+\frac{1}{G_{pwm}}u_s(t). \tag{2.8}$$

It consists of dynamic components and feed-forward components. According to the control theory, the feed-forward components does not affect stabilization in the closed-loop control system, thus the current control system can be simplified as

$$m(t)=\frac{L}{G_{pwm}T}\left[i_s^*(t)-i_s(t)\right]. \tag{2.9}$$

Therefore, the block diagram of the current control system can be represented as in Fig. 2.6. T_{r} is the time constant due to computation and modulation of the converter, L is the interfacing inductor.

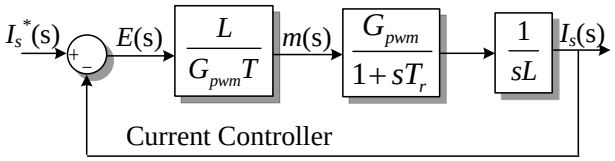


Figure 2.6: Block diagram of the current control system.

From Fig. 2.6, the closed-loop transfer function of the control system can be derived as

$$\frac{I_s(s)}{I_s^*(s)} = \frac{\frac{1}{TT_r}}{s^2 + s\frac{1}{T_r} + \frac{1}{TT_r}}. \tag{2.10}$$

According to the standard second-order system, the damping factor is usually chosen as 0.707, which yields

$$T=2T_{\mathrm{r}}. \tag{2.11}$$

Thus, it can be concluded that a proportional controller, $k=L/(G_{\mathrm{pwm}}T)$, ensures that the current control system operates as a first-order lag system with a time constant $T=2T_{\mathrm{r}}$. Since the switching frequency is high, T is relatively low, and the output of the controller can track the reference signal accurately.

2.3.2 Switching Pulses Generation

To generate the switching pulses, the converter currents (i_{ca}, i_{cb}, and i_{cc}) are compared with their reference rectification currents given in equation (2.5). These current errors are amplified using a proportional current controller and added up to generate modulation signals for three-phase legs of the converter. Modulation signal for the fourth leg is generated by

$$m_{\mathrm{n}}=-(m_{\mathrm{a}}+m_{\mathrm{b}}+m_{\mathrm{c}}), \tag{2.12}$$

where m_{a}, m_{b}, and m_{c} are the modulation signal of three-phase legs respectively. Finally,

all the modulation signals are compared with carrier signals to generate gate pulses for the four-leg converter.

2.4 Simulation Study

This section provides the simulation verification of the proposed ROGI based control algorithm for the four-leg converter. The system parameters are provided in Table 2.1. The initial simulation is performed in MATLAB/Simulink.

Fig. 2.7 shows the waveforms of gird voltage and currents. It can be seen that during the unbalanced reactive loads condition, the grid current is in the same phase of grid voltage, which means the grid source operates at unity power factor. Further, to show the dynamic response of the proposed algorithm, phase 'b' load is turned off during the operation of the system. From Fig. 2.8, it can be observed that load side currents become more unbalanced and unequal, but the converter can provide fast corrective action and the grid currents remain balanced. These simulation results verify the effectiveness of the proposed control algorithm under both transient and steady-state conditions.

Table 2.1: Parameters of the Four-leg Converter with DC Power Supply

Parameters	**Value**
DC-link voltage u_{dc}	320 V
Grid voltage u_s (RMS)	110 V
Grid frequency f	60 Hz
Switching frequency f_s	20 kHz
Interfacing inductor	6 mH
Phase A loads	30 Ω and 6 mH
Phase B loads	40Ω
Phase C loads	27.5 Ω and 6 mH

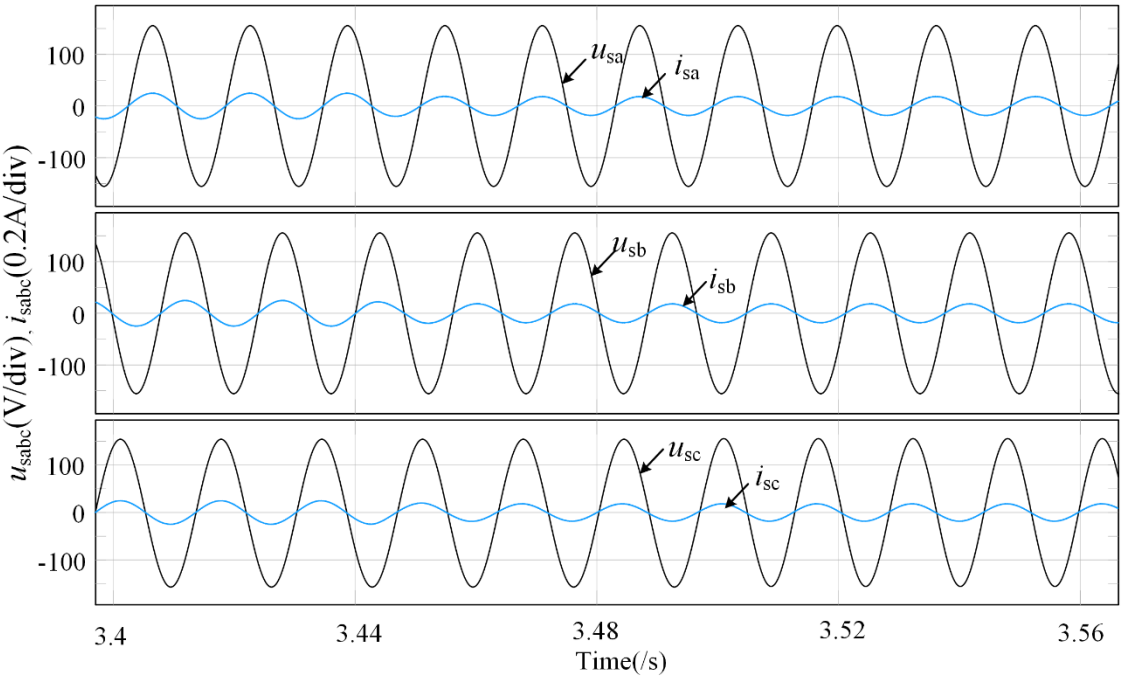


Figure 2.7: Simulation results of grid voltage and currents.

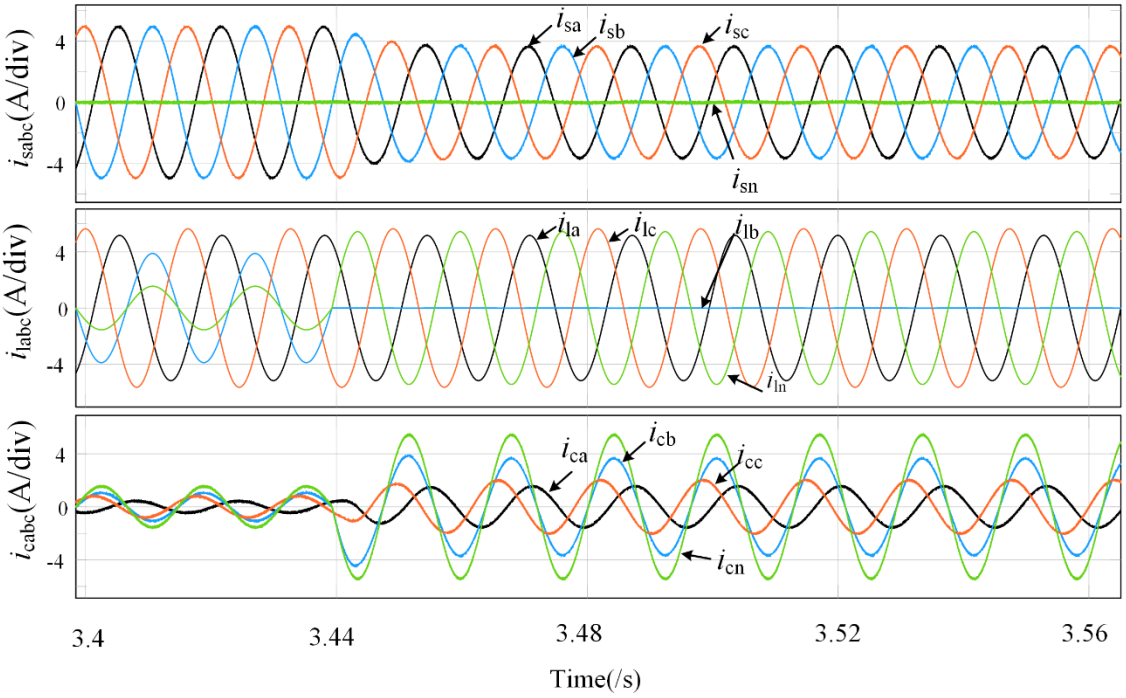


Figure 2.8: Simulation results using the proposed control strategy with heavy-load to light-load variation.

2.5 Conclusion

In this chapter, an unbalanced currents detection technique using reduced order generalized integrator (ROGI) is presented for a four-leg converter whose DC bus is supported by an active power supply. The controller can effectively and accurately detect the positive and negative sequence components of load side currents based on the proposed ROGI technique. The simulation results show the satisfactory operation of the converter during transient and steady-state periods.

2.6 Publications

1. S. Jiao, S. Kumar Pramanick, K. Rajashekara, and N. Satheesh. "Four-leg Inverter with Reduced Order Generalized Controller for Unbalanced Load Detection and Compensation," 2018 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 3170–3174.

Chapter 3

Decoupling Control Algorithms for Four-Leg Converter under Unbalanced Reactive Loading Condition with DC Input Capacitor

3.1 Introduction

Four-leg converter has been used to mitigate the power quality (PQ) problems, such as unbalanced loading, increased neutral current, and poor power factor operation, in a three-phase four-wire microgrid system, as discussed in chapter 2. However, a dedicated DC power supply is required to support the DC bus voltage of the converter, which in turn increases the size and cost of the converter. In this chapter, a compensation scheme based on four-leg converter with the DC power supply replaced by DC capacitors is presented, which helps to achieve reduced size and flexible operation of the converter.

Such configuration, as shown in Fig. 3.1, results in a challenging task for designing the controller. This is due to the fact that the converter not only requires to compensate unbalanced loads with required currents, but also need to absorb positive sequence active power from the grid to maintain the DC link voltage. To achieve this, various control algorithms have been reported in the literature. The most common used methods are instantaneous reactive power theory (IRPT) and synchronous reference frame theory (SRFT). IRPT, proposed by Prof. H. Akagi, which utilize three-phase (*abc*) to two-phase ($\alpha\beta$) transformation for obtaining the active and reactive power components of loads [37]–

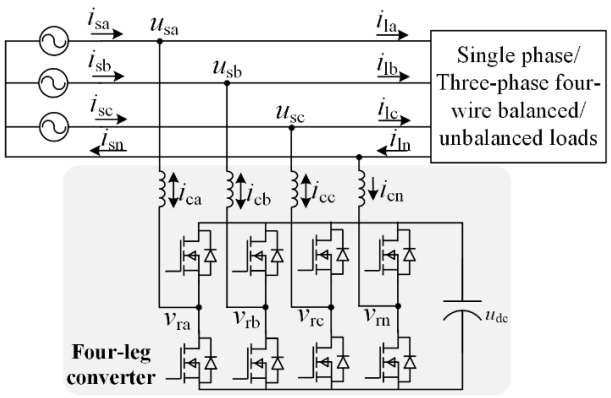


Figure 3.1: Structure of four-leg converter as a shunt compensator.

[39]. Furthermore, the synchronous reference compensation currents are obtained using power equations using the known grid voltages. However, since the output power calculation involves a low-pass filter and DC link voltage regulation is inherently realized, the dynamic response of IRPT during transient periods is relatively poor [40]. SRFT employs the transformation of three-phase quantities (*abc*) to a rotating frame (*dq*) with the help of phase-locked-loop (PLL) [41]–[43]. The reference compensation signals are synchronized with utility grid phase voltages. But, SRPT based converter is not capable of providing fast corrective action for dynamically changing loads [44].

To overcome the drawbacks of the above-mentioned control algorithms, a novel control algorithm using double reduced-order generalized integrators (DROGI) for a four-leg shunt converter is proposed in this chapter [45]. The first integrator is adopted to extract required reference compensation currents for power quality improvement and the second one is used to decouple compensation currents and rectification currents of the converter side. The reference rectification currents are generated using an outer-loop DC-link voltage controller (PI) and are synchronized to the three-phase voltages. Since the compensation mode (DC-AC) and rectification mode (AC-DC) of the converter are decoupled and regulated separately, the four-leg converter operation with a good dynamic response, robust

performance, and flexible controllability is achieved. Moreover, another novel control algorithm named grid voltage modulated direct power control (GVM-DPC) without PLL for the four-leg converter is proposed as well [19]. The effectiveness of the proposed algorithms is validated by simulation and experimental results.

3.2 Generalized Model of the Compensation System

Under a balanced 3-phase grid system, the three-phase voltages can be represented by

$$\begin{cases} u_a(t) = \sqrt{2}V\sin\left(\omega t + \Phi_{vn}\right) \\ u_{\mathrm{b}}(t) = \sqrt{2}V\sin\left(\omega t - \frac{2}{3}\pi + \Phi_{vn}\right) \\ u_{\mathrm{c}}(t) = \sqrt{2}V\sin\left(\omega t + \frac{2}{3}\pi + \Phi_{vn}\right) \end{cases}, \tag{3.1}$$

where V is RMS value of phase PCC voltages, ω is the fundamental angular frequency of the grid, and Φ_{vn} is the phase angle of phase PCC voltage.

Due to unevenly distributed reactive loads, the load currents can be decomposed as the summation of positive, negative and zero sequence components, which can be expressed as [46]

$$\begin{cases} i_a(t) = \sqrt{2}I_+\sin\left(\omega t + \Phi_{I+}\right) + \sqrt{2}I_-\sin\left(\omega t + \Phi_{I-}\right) \\ \qquad +\sqrt{2}I_0\sin\left(\omega t + \Phi_{I0}\right) \\ i_{\mathrm{b}}(t) = \sqrt{2}I_+\sin\left(\omega t - \frac{2}{3}\pi + \Phi_{I+}\right) + \sqrt{2}I_-\sin\left(\omega t + \frac{2}{3}\pi + \Phi_{I-}\right) \\ \qquad +\sqrt{2}I_0\sin\left(\omega t + \Phi_{I0}\right) \\ i_{\mathrm{c}}(t) = \sqrt{2}I_+\sin\left(\omega t + \frac{2}{3}\pi + \Phi_{I+}\right) + \sqrt{2}I_-\sin\left(\omega t - \frac{2}{3}\pi + \Phi_{I-}\right) \\ \qquad +\sqrt{2}I_0\sin\left(\omega t + \Phi_{I0}\right) \end{cases}, \tag{3.2}$$

where I+, I-, and I0 are RMS values of positive, negative, and zero sequence currents. $\Phi_{\mathrm{I+}}$, $\Phi_{\mathrm{I-}}$, and Φ_{I0} are phase angles of corresponding sequence currents.

The instantaneous power in a three-phase four-wire system can be expressed as

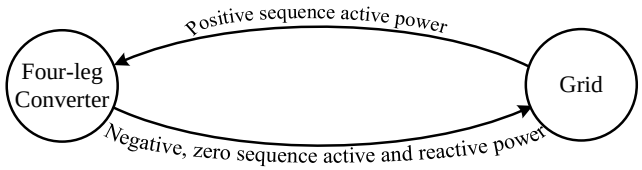


Figure 3.2: Power flow between grid and converter.

$$\begin{aligned} p(t) &= u_{\mathrm{a}}(t) i_{\mathrm{a}}(t) + u_{\mathrm{b}}(t) i_{\mathrm{b}}(t) + u_{\mathrm{c}}(t) i_{\mathrm{c}}(t) \\ &= u(t) i_{+}(t) + u(t) i_{-}(t) + u(t) i_{0}(t) \end{aligned} . \tag{3.3}$$

Substituting equation (3.1) and (3.2) in (3.3), the instantaneous power with respect to load side can be expressed as the sum of such powers:

$$\begin{cases} \bar{p}_{+} = 3VI_{+}\cos\left(\Phi_{vn} - \Phi_{I+}\right) \\ \tilde{p}_{-} = -3VI_{-}\cos\left(2\omega t + \Phi_{vn} + \Phi_{I-}\right) \\ \bar{q}_{+} = -3VI_{+}\sin\left(\Phi_{vn} - \Phi_{I+}\right) \\ \tilde{q}_{-} = 3VI_{-}\sin\left(2\omega t + \Phi_{vn} + \Phi_{I-}\right) \end{cases} , \tag{3.4}$$

where $\bar{p}_{+}$ is positive sequence active power, $\tilde{p}_{-}$ is active power due to negative sequence currents, $\bar{q}_{+}$ and $\tilde{q}_{-}$ are reactive powers that being exchanged between the loads and power supply from the grid.

Obviously, from equation (3.4), it can be noticed that the three-phase utility grid will only supply positive sequence active power if $\tilde{p}_{-}$, $\bar{q}_{+}$, and $\tilde{q}_{-}$ are compensated by the four-leg converter. At the same time, to achieve power quality improvement in the three-phase four-wire system, zero sequence current needs to be compensated as well.

As mentioned earlier, in addition to power quality improvement, DC link voltage (u_{dc}) should also be maintained. For this purpose, the four-leg converter absorbs positive sequence active power from the grid accordingly. Thus, the power flow between converter and grid is shown as in Fig. 3.2.

3.3 DROGI Based Control Algorithm

Fig. 3.3 shows the block diagram of the control scheme using DROGI for the four-leg converter. This control strategy employs double ROGIs to extract the reference compensation currents along with corresponding decoupled currents (compensation currents and rectification currents) of the converter. Further, these reference currents and the decoupled currents are used by the current controller to generate PWM signals for the four-leg converter.

Power quality improvement is achieved through the compensation mode (DC-AC) of the four-leg converter. The unbalanced load currents are sensed and separated into positive and negative sequence components with the help of ROGI. Then, the detection of positive sequence active power demand from the load side is facilitated by IRPT. Eventually, the reference compensation currents are obtained by subtracting positive sequence currents from actual load currents, which are expressed as

$$\begin{cases} i_{ac}^{*} = i_{la} - i_{la+} \\ i_{bc}^{*} = i_{lb} - i_{lb+} \\ i_{cc}^{*} = i_{lc} - i_{lc+} \end{cases}. \tag{3.5}$$

Using rectification mode (AC-DC), DC link voltage regulation of the converter is performed. As discussed above, the converter should also absorb positive sequence active power from the grid to regulate the DC link voltage. Similar to the load side positive sequence active power detection, the second ROGI is employed to decompose the converter currents. As a result, positive sequence active power components of converter side currents can be extracted. The magnitude of reference rectification current is generated using a PI controller to maintain the DC link voltage at its reference value.

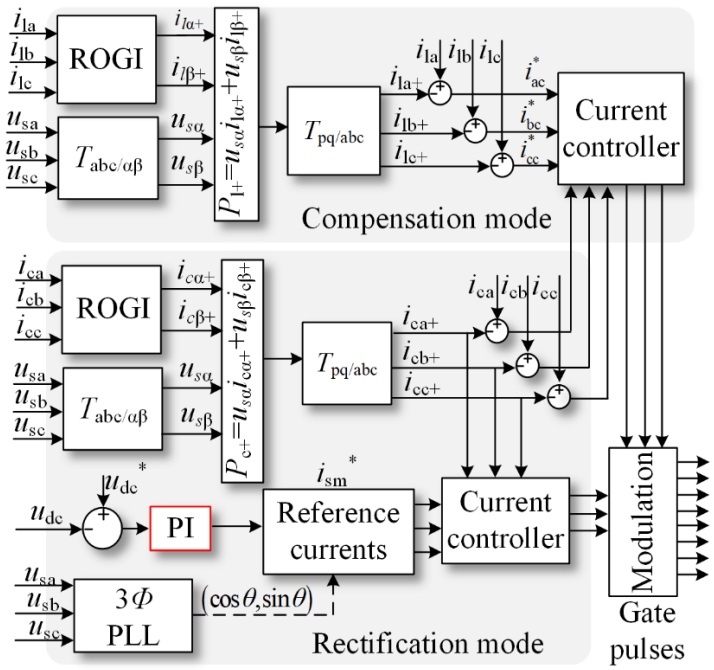


Figure 3.3: DROGI control algorithm.

Then, the extracted positive sequence active power components of converter currents (i_{ca+}, i_{cb+}, and i_{cc+}) and the reference currents from PI controller are used in the current controller to maintain the DC link voltage. The remaining converter currents (i_{ca}-i_{ca+}, i_{cb}-i_{cb+}, and i_{cc}-i_{cc+}) track reference compensation currents using another current controller for improving power quality. Consequently, the compensation mode (DC-AC) and rectification mode (AC-DC) of the converter are decoupled and regulated separately. The detailed operation is explained below.

3.3.1 Reference Compensation Currents Generation

To improve the power quality under unbalanced reactive loads, the required compensation currents should be obtained accurately. As discussed above, ROGI has the characteristics of frequency selectivity and polarity selectivity. Thus, the unbalanced load currents are sensed to extract positive sequence currents with the help of ROGI initially.

Further, the corresponding positive sequence active and reactive powers are obtained by employing IRPT without an output low-pass filter, which is given by

$$\begin{bmatrix} \bar{p}_+ \\ \bar{q}_+ \end{bmatrix} = \begin{bmatrix} u_{s\alpha} & u_{s\beta} \\ -u_{s\beta} & u_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{l\alpha+} \\ i_{l\beta+} \end{bmatrix}, \tag{3.6}$$

where $u_{s\alpha}$ and $u_{s\beta}$ are PCC voltages in the $\alpha\beta$ reference frame.

The positive sequence active power demand from loads can be expressed as

$$\bar{p}_+ = u_{s\alpha} i_{l\alpha+} + u_{s\beta} i_{l\beta+}. \tag{3.7}$$

Since the grid should only supply positive sequence active power to the loads, the required reference compensation currents can be obtained by subtracting positive sequence active currents from actual load currents, which can be expressed as

$$\begin{bmatrix} i_{ac}^* \\ i_{bc}^* \\ i_{cc}^* \end{bmatrix} = \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} - \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \frac{1}{u_{s\alpha}^2 + u_{s\beta}^2} \begin{bmatrix} u_{s\alpha} & -u_{s\beta} \\ u_{s\beta} & u_{s\alpha} \end{bmatrix} \begin{bmatrix} \bar{p}_+ \\ 0 \end{bmatrix}, \tag{3.8}$$

where i_{ac}^*, i_{bc}^* and i_{cc}^* are required compensation currents.

3.3.2 Reference Rectification Currents Generation

For the operation of four-leg converter, the DC link voltage of converter should also be maintained at a minimum value, as given in [47]

$$V_{min} = 2\sqrt{2} V_{LL} / \sqrt{3} m, \tag{3.9}$$

where V_{LL} is the amplitude of line-line PCC voltage, m is the modulation index and is chosen as 1.

To decouple the compensation and rectification modes of the converter, the second ROGI is employed to decompose converter currents. Similarly, the positive sequence

active currents absorbed by the converter can also be obtained with the help of IRPT without any output low-pass filter. The magnitude of reference currents is generated using a proportional-integral (PI) controller, which is expressed as

$$i^{*}_{\mathrm{sm+}}(n) = K_p\left(u^{*}_{\mathrm{dc}} - u_{\mathrm{dc}}\right) + K_i\int\left(u^{*}_{\mathrm{dc}} - u_{\mathrm{dc}}\right)dt, \tag{3.10}$$

where $i^{*}_{\mathrm{sm+}}$ is the amplitude of reference positive sequence active power current, u_{dc} is the sensed DC side voltage and u_{dc}^{*} is the reference DC side voltage, K_{p} and K_{i} are the proportional and integral gains of the voltage loop PI controller respectively.

The sensed DC side voltage (u_{dc}) is compared with its reference value (u_{dc}^{*}). The voltage error is fed to a PI controller, as shown in Fig. 3.3. Then, the reference rectification currents can be generated by synchronizing with three-phase voltage as

$$\begin{cases} i^{*}_{\mathrm{ca+}} = i^{*}_{\mathrm{sm+}}\sin\left(\omega t + \Phi_{\mathrm{vn}}\right) \\ i^{*}_{\mathrm{cb+}} = i^{*}_{\mathrm{sm+}}\sin\left(\omega t - \dfrac{2}{3}\pi + \Phi_{\mathrm{vn}}\right) \\ i^{*}_{\mathrm{cc+}} = i^{*}_{\mathrm{sm+}}\sin\left(\omega t + \dfrac{2}{3}\pi + \Phi_{\mathrm{vn}}\right) \end{cases}. \tag{3.11}$$

3.3.3 Simulation and Experimental Results

This section provides the simulation and experimental verification of the proposed DROGI based control method. Comparative performance of the proposed control method with IRPT and SRFT control algorithms are also presented. The simulation is carried out based on MATLAB/SIMULINK. The verification is based on the system parameters provided in Table 3.1

Table 3.1: Parameters of the System

Parameters	Value
DC-link voltage u_{dc}	320V
The capacitance of the DC side capacitor	3600μF
Grid voltage u_s	110V
Grid frequency f	60Hz
Switching frequency f_s	20kHz
Interfacing inductor	6mH
Phase A loads	30Ω and 6mH
Phase B loads	40Ω
Phase C loads	27.5Ω and 6mH

3.3.3.1 Simulation results

The verification of the proposed scheme is performed in MATLAB/Simulink. The simulation results of the proposed control method are presented in Fig. 3.4. These results depict waveforms of PCC voltages (u_s), grid currents (i_s), converter currents (i_c), load currents (i_l) and DC link voltage (u_{dc}). It can be noticed from Fig. 3.4(a) that the grid supplies balanced currents to the system and DC link voltage is regulated at the reference voltage of 320 V by rectification mode (AC-DC).

To verify the reactive power compensation capability of the proposed scheme, the load of phase ‘c’ is made more inductive (20 ohm/13 mH). The voltages and currents of phase ‘c’ at the source and load terminals are shown in Fig. 3.4(b). It can be seen that the grid current is in the same phase with the grid voltage, which means the grid source operates at unity power factor. However, the current lags voltage due to reactive load, at the load side. Further, to illustrate the dynamic response of the proposed algorithm, phase ‘b’ load is turned off during the operation of the system. From Fig. 3.4(c), it can be observed that the

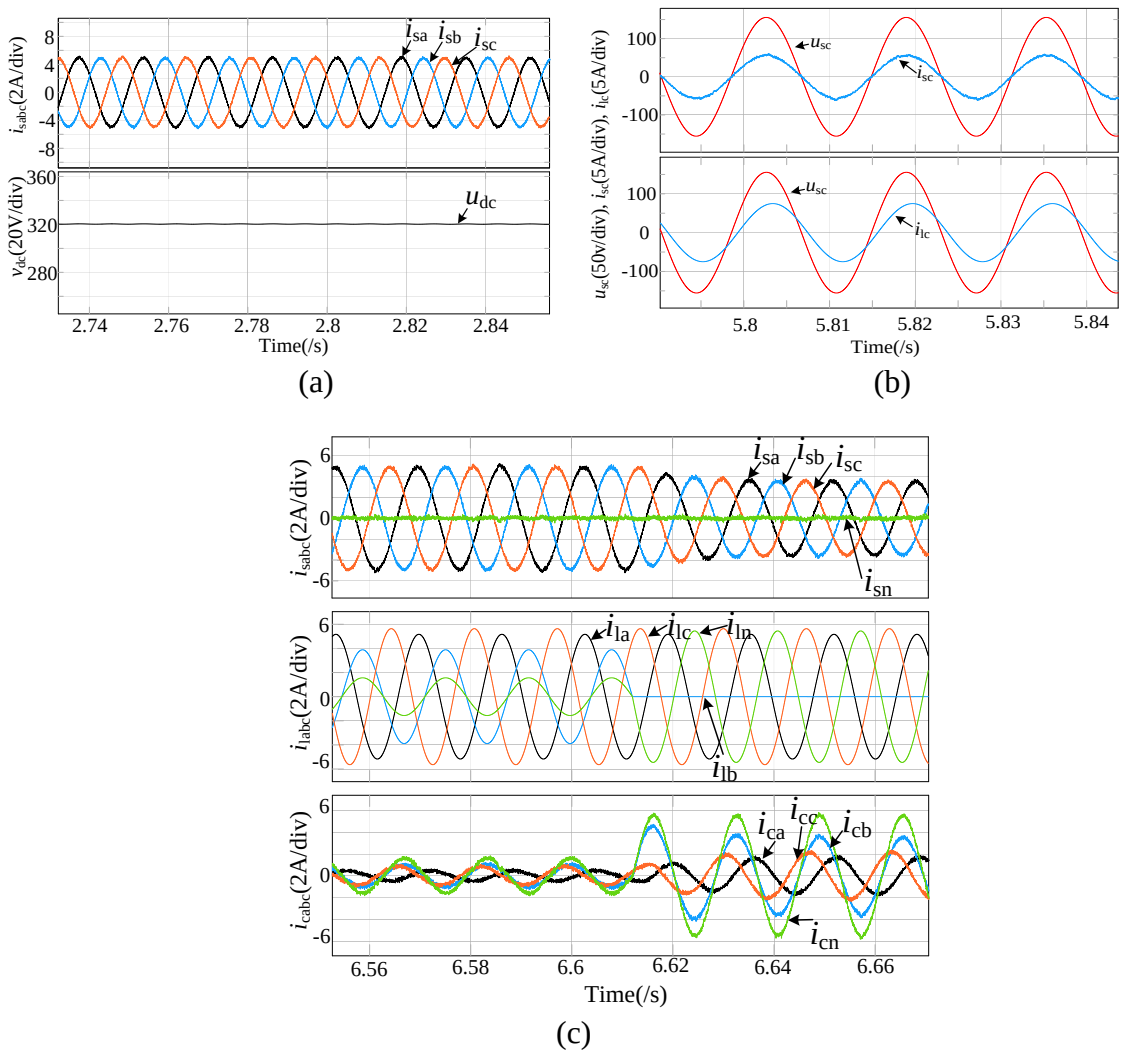
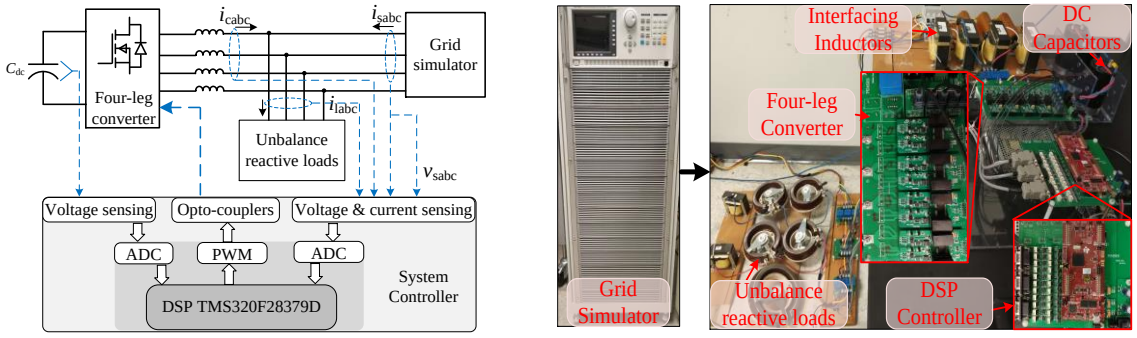


Figure 3.4: Simulation results under compensation. (a) Simulation results of grid currents and DC link voltage at steady state after compensation. (b) Simulation results of grid voltage and currents before and after power factor correction. (c) Simulation results using the proposed control strategy with heavy-load to light-load variation.

load side currents become more unbalanced and unequal, but the converter can provide fast corrective action to maintain the grid currents at balanced conditions. It demonstrates the fast dynamic response of the proposed control strategy. These simulation results verify the effectiveness of the proposed control algorithm under both transient and steady-state periods.

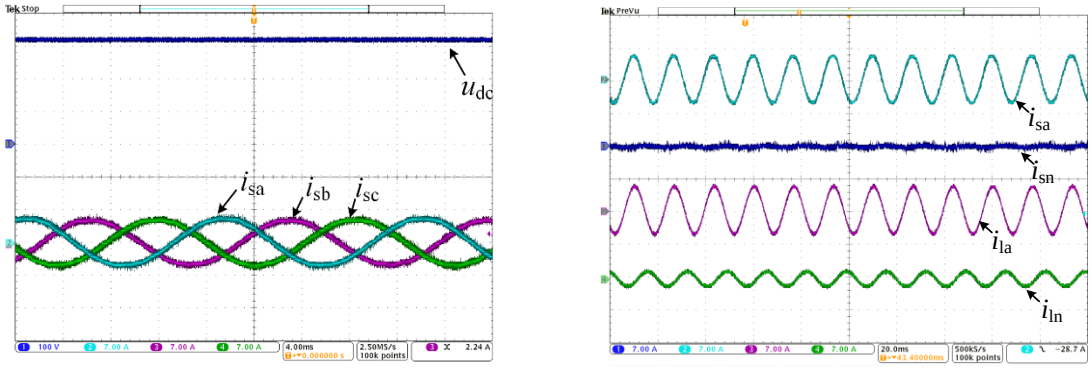
3.3.3.2 Experimental results

A prototype of the four-leg converter, as shown in Fig. 3.5(a)-(b), is developed to validate the proposed control algorithm. A digital signal processor TMS320F28379D platform is used to operate control strategies for the experimental setup. Voltage and current sensing are performed using Hall Effect sensors LEM LV-25 and LEM LA-25 respectively. The three-phase voltages are simulated by a programmable Chroma 61611 ac-power source. The experimental results are observed using a digital scope oscilloscope (TEKTRONIX MDO4024C).



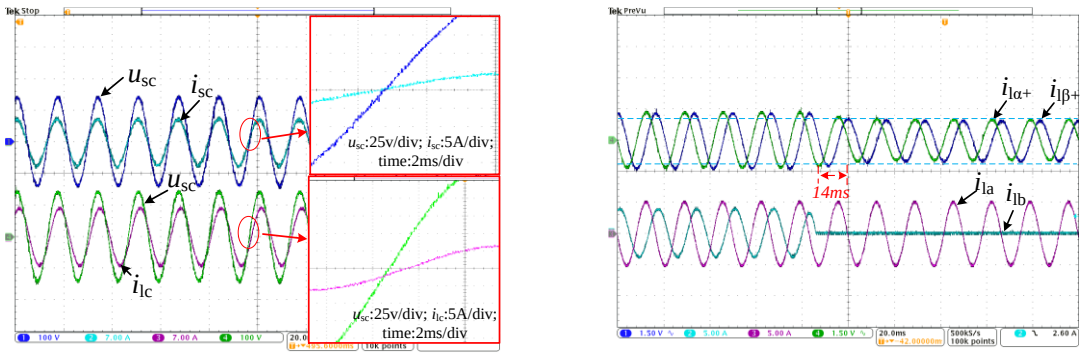
(a) (b)

Figure 3.5: (a) Block diagram of the experimental prototype. (b) Experimental setup for the verification of the proposed control algorithm.



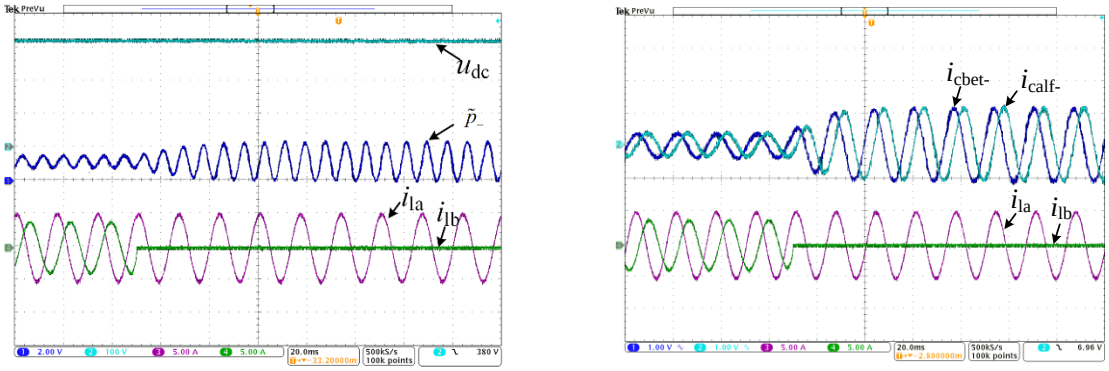
(a) (b)

Figure 3.6: (a) Experimental results of grid currents and DC voltage (i_{sa}=7A/div, i_{sb}=7A/div, i_{sc}=7A/div, u_{dc}=100V/div, time scale=4ms/div). (b) Experimental results of grid currents and load currents (i_{sa}=7A/div, i_{sn}=7A/div, i_{la}=7A/div, i_{ln}=7A/div, time scale=20ms/div).



(a) (b)

Figure 3.7: (a) Experimental results of grid voltage, grid current and load current (u_{sc}=100V/div, i_{sc}=7A/div, i_{lc}=7A/div, time scale=20ms/div). (b) Experimental waveforms of unbalanced load currents and its positive components with k=100 ($i_{l\alpha+}$=6.5A/div, $i_{l\beta+}$=6.5A/div, i_{la}=5A/div, i_{lb}=5A/div, time scale=20ms/div).

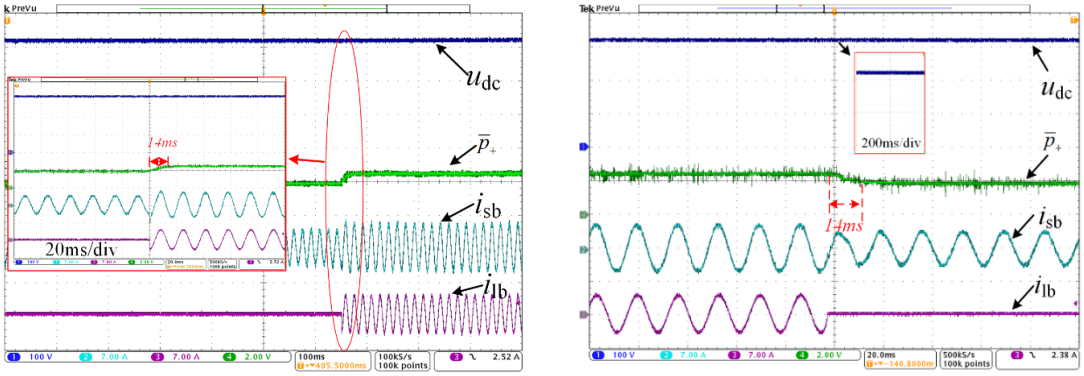


(a) (b)

Figure 3.8: (a) Experimental results of load currents, DC voltage and compensating negative sequence active power (u_{dc}=100V/div, $\tilde{p}_{-}$=400W/div, i_{la}=5A/div, i_{lb}=5A/div, time scale=20ms/div). (b) Experimental results of load currents and compensating negative sequence currents (i_{cbet-}=2A/div, i_{calf-}=2A/div, i_{la}=5A/div, i_{lb}=5A/div, time scale=20ms/div).

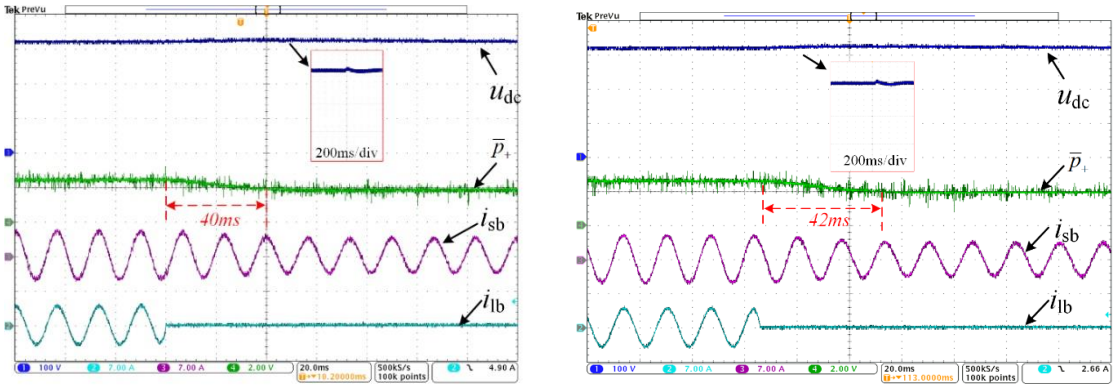
Fig. 3.6 (a)-(b) show the waveforms of DC link voltage, grid currents, grid side neutral current, phase ‘a’ load current and load side neutral current. During the operation of the converter, the grid currents are balanced and the DC link voltage is maintained at 320V constantly, as shown in Fig. 3.6, it can be seen that during unbalanced loading conditions, grid supplies only balanced and sinusoidal currents to the system with the help of the four-leg converter. To verify the reactive power compensation of the proposed strategy, the load of phase ‘c’ is made more inductive (20 ohm/13 mH). The voltages and currents of phase

'c' at the source and load terminals are shown in Fig. 3.7(a). It can be observed that the current of the load side is lagging with 17.5 degrees due to reactive loading conditions. But, with the help of a four-leg converter, the current and voltage of AC source terminals are in the same phase which means the AC source is operating with a unity power factor. Thus, the four-leg converter could compensate the required reactive power to the system as well. These results show the effectiveness of the controller during a steady-state condition.



(a) (b)

Figure 3.9: (a) Experimental results of DROGI with light-load to heavy-load variation (u_{dc}=100V/div, $\bar{p}_+$ =1kW/div, i_{sb}=7A/div, i_{lb}=7A/div, time scale=100ms/div). (b) Experimental results of DROGI with heavy-load to light-load variation (u_{dc}=100V/div, $\bar{p}_+$=1kW/div, i_{sb}=7A/div, i_{lb}=7A/div, time scale=20ms/div).



(a) (b)

Figure 3.10: (a) Experimental results of IRPT with heavy-load to light-load variation (u_{dc}=100V/div, $\bar{p}_+$=1kW/div, i_{sb}=7A/div, i_{lb}=7A/div, time scale=20ms/div). (b) Experimental results of SRFT with heavy-load to light-load variation (u_{dc}=100V/div, $\bar{p}_+$=1kW/div, i_{sb}=7A/div, i_{lb}=7A/div, time scale=20ms/div).

Fig. 3.7(b) shows the variation of load-side positive sequence currents, which are generated by DAC of DSP controller in αβ reference frame. Phase 'b' load is turned off during the operation of the system. It can be noticed that only 14ms is required for the controller to detect the positive sequence components of unbalanced currents. Fig. 3.8 depicts the compensated negative sequence active power, DC link voltage, compensated negative sequence currents i_{cbet-}, i_{calf-} in $\alpha\beta$ reference frame and the load currents under transient conditions, in which the compensated negative sequence active power and negative sequence currents i_{cbet-}, i_{calf-} are generated and measured from DAC of DSP. It can be observed that after turning off phase 'b' load, the frequency of negative sequence active power from the compensation currents remains twice the fundamental frequency which matches the above theoretical analysis. The magnitudes of compensating negative currents and their active power are automatically adjusted during load change to obtain balanced sinusoidal grid currents. The DC link voltage is maintained at its reference voltage constantly. Thus, the four-leg converter provides necessary compensation for all phases even under dynamic operating conditions, as evident from its satisfactory operation.

The performance of DROGI based control method is also compared with the other two conventional methods -SRF and IRP theories. The rated converter operation is considered as a heavy load condition, which is 1.1kW. The complete disconnection of one phase load (phase 'b') is considered as light load condition (around 800W of converter operation). Figs. 3.9-3.10 show the DC link voltage, positive sequence active power demand of load, phase 'b' grid current and phase 'b' load current with proposed DROGI, IRPT and SRPT based detection techniques. Figs. 3.9 shows the experimental results using DROGI. It can be observed that only 14ms is required to detect the change in positive sequence active

power demand during the variation of loading condition, while the DC link voltage is well controlled at its reference value, both during the transient and steady-state operation. From Fig. 3.10, it can be seen that IRPT and SRFT need 40ms and 42ms respectively to detect the change in positive sequence active power, which demonstrates the poor dynamic response of IRPT and SRFT as compared with that of proposed DROGI detection scheme. An overshoot of about 20V in the DC link voltage is also observed during transient operation using conventional control strategies. These results confirm that through decoupled control, the DROGI scheme is stable, robust and can regulate the DC link voltage steadily. Hence, the proposed DROGI scheme is identified with a better dynamic response as compared to conventional methods like IRPT and SRFT.

3.4 Grid Voltage Modulated Direct Power Control

Furthermore, to eliminate the impact of PLL, another novel control algorithm named grid voltage modulated direct power control (GVM-DPC) without PLL for the four-leg converter is proposed as well. Its control diagram is shown in Fig. 3.11. Similar to the DROGI based control method, double ROGIs are applied to get the desired compensation currents and decouple the converter side currents. But for maintaining the DC bus voltage, a direct power control (DPC) is used, such as the PLL can be eliminated.

As shown in Fig. 3.11, the reference rectification power is generated using a PI controller over DC link voltage error from the reference value

$$P_c^*(n) = K_p\left(u_{\mathrm{dc}}^* - u_{\mathrm{dc}}\right) + K_i\int\left(u_{\mathrm{dc}}^* - u_{\mathrm{dc}}\right)dt \quad (3.12)$$

Further, another inner PI controller in DC link voltage regulator loop based on rectification power error is used to generate the required amplitude of modulating signals

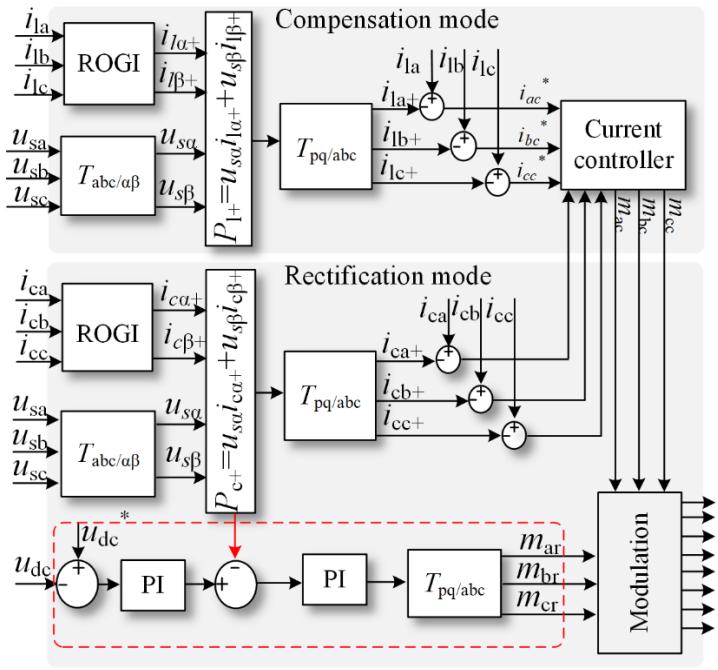


Figure 3.11: Diagram of GVM-DPC.

$$m_{pc}^{*}(n)=K_{p1}\left(p_{c}^{*}-p_{c}\right)+K_{i1}\int\left(p_{c}^{*}-p_{c}\right)dt, \tag{3.13}$$

where K_{p1} and K_{i1} are the proportional and integral gains of the inner current loop PI controller. Moreover, the output of PI controller is converted into modulation signals from the rectification mode controller, which is expressed as,

$$\begin{bmatrix} m_{ar} \\ m_{br} \\ m_{cr} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \frac{1}{u_{s\alpha}^{2}+u_{s\beta}^{2}} \begin{bmatrix} u_{s\alpha} & -u_{s\beta} \\ u_{s\beta} & u_{s\alpha} \end{bmatrix} \begin{bmatrix} m_{pc}^{*} \\ 0 \end{bmatrix}, \tag{3.14}$$

where m_{ar}, m_{br} and m_{cr} are modulation signals from the rectification control block for the first three legs of the four-leg converter.

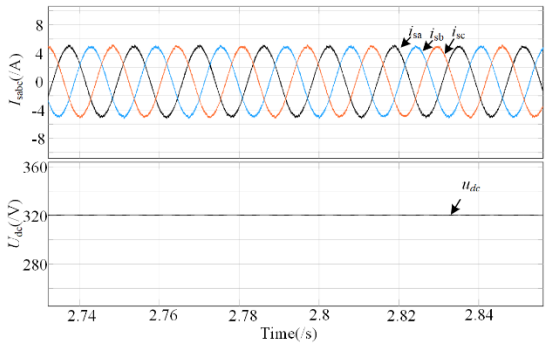
Finally, the reference compensation currents and its corresponding decoupled currents are implemented in a current controller for power quality improvement. As a result, the

synchronization unit (PLL) is not required in this control strategy and the compensation mode and rectification mode of the converter are decoupled as well.

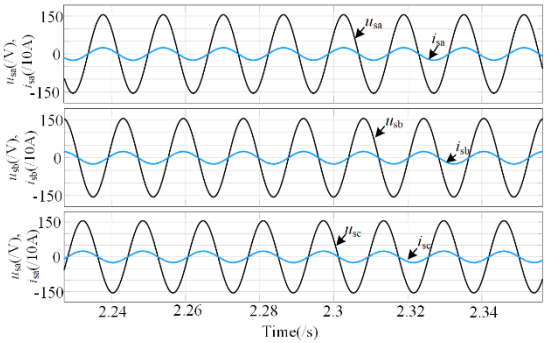
3.4.1 Simulation Study

The verification of the proposed scheme is performed in MATLAB/Simulink. The system parameters are listed in Table 3.1. The simulation results of the proposed control method are presented in Fig. 3.12 during step load changing condition. These results depict waveforms of PCC voltages (u_s), grid currents (i_s), converter currents (i_c), load currents (i_l) and DC link voltage (u_{dc}).

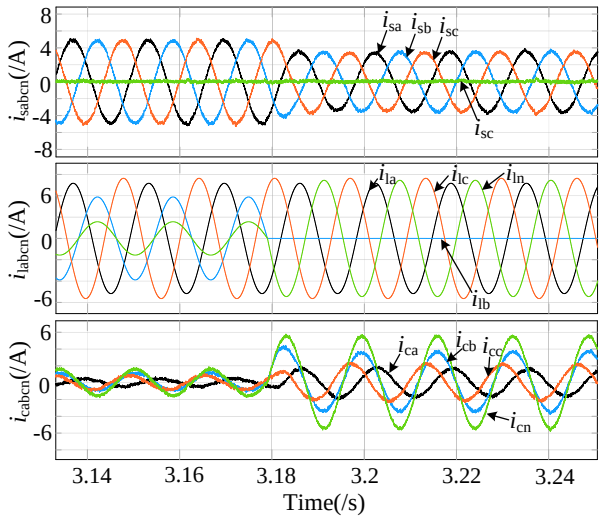
During the operation, the phase 'b' load is turned off. It can be noticed from Fig. 3.12(a) that the power source supplies balanced currents to the system and DC link voltage is maintained at the reference voltage of 320V by rectification mode. In Fig. 3.12(b), the grid current is in the same phase with grid voltage, which means the grid source operates in the unity power factor. Further, from Fig. 3.12(c), it is observed that the load currents become more unequal and unbalanced, but the converter can provide fast corrective action and the grid currents remain balanced.



(a)



(b)



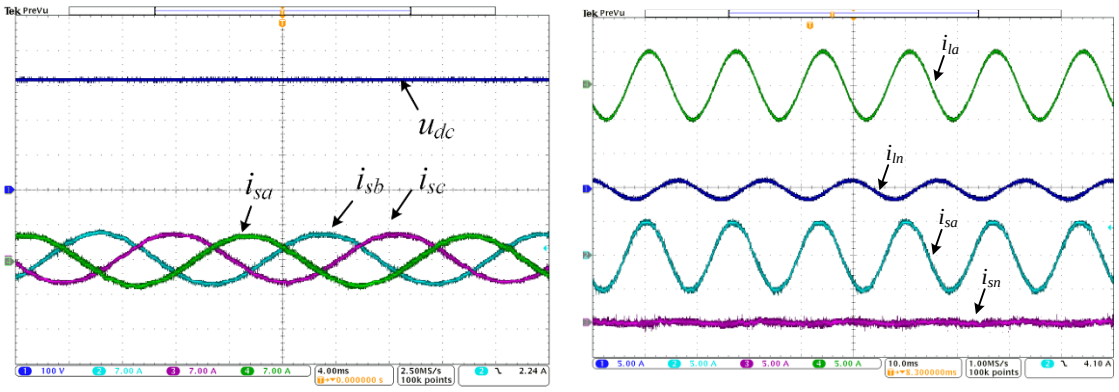
(c)

Figure 3.12: Simulation results of compensation (a) Simulation results of grid currents and DC link voltage at steady state after compensation. (b) Simulation results of grid voltage and currents with unity power factor. (c) Simulation results of the proposed control strategy with heavy-load to light-load variation.

3.4.2 Experimental Study

Fig. 3.13 depicts the waveforms of DC link voltage (u_{dc}), grid currents, and load currents. It can be seen that the DC link voltage is maintained at 320V constantly. Meanwhile, balanced and sinusoidal grid currents are achieved during the unbalanced loading condition with the help of the four-leg converter. These results show the satisfactory operation of the proposed control algorithm during a steady state condition.

To verify the dynamic performance of the proposed control method, the phase ‘b’ load is turned off during the operation of system. Fig. 3.14 shows the waveforms of DC link voltage (u_{dc}), phase ‘b’ load current (i_{lb}), the compensated negative sequence active power (P_{n_ca}) and positive sequence active power (P_{l+}) demand of the load. It can be observed that, after turning off phase ‘b’ load, only 12ms is required to detect the change in positive sequence active power demand from the load side and the DC link voltage is well controlled with respect to its reference value. Since the loads are highly unbalanced, the



(a) (b)

Figure 3.13: (a) Experimental results of grid currents and DC voltage (i_{sa}=5A/div, i_{sb}=5A/div, i_{sc}=5A/div, u_{dc}=100V/div, time scale=4ms/div). (b) Experimental results of grid currents and load currents (i_{sa}=5A/div, i_{sn}=5A/div, i_{la}=5A/div, i_{ln}=5A/div, time scale=10ms/div).

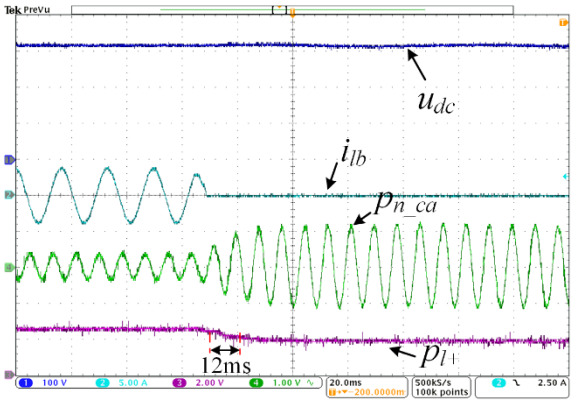


Figure 3.14: Experimental results of proposed control method with heavy-load to light-load variation (u_{dc}=100v/div, i_{lb}=5A/div, P_{n_ca}=200W/div, P_{l+}=1KW/div, time scale=20ms/div).

higher amount of negative sequence active power is compensated from the four-leg converter. These results confirm that the proposed control algorithm is effective, stable, and robust.

3.5 Conclusion

In this chapter, a control method named double reduced-order generalized integrator (DROGI) for shunt compensation of unbalanced loads using a four-leg converter in a distributed system is proposed. One integrator is operated on load currents to obtain the reference compensation currents and the second one is used to decompose the converter

currents. The reference rectification currents are generated using a PI controller to regulate the DC link voltage at its reference value. As a result, the compensation currents for improving power quality and rectification currents for maintaining DC link voltage are decoupled and regulated separately. Also, in order to eliminate the impact of PLL, another novel control algorithm named grid voltage modulated direct power control (GVM-DPC) without PLL for the four-leg converter is proposed as well. The proposed control algorithms for the four-leg converter improve the power quality problems in terms of load balancing, reduced neutral current and achieving unity power factor operation in a three-phase four-wire microgrid system. The effectiveness of the proposed algorithms has been analyzed through steady-state and dynamic response.

3.6 Publications

1. S. Jiao, K. R. Ramachandran Potti, K. Rajashekara and S. K. Pramanick, "A Novel DROGI-Based Detection Scheme for Power Quality Improvement Using Four-Leg Converter Under Unbalanced Loads," in *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 815-825, Jan. –Feb. 2020.
2. S. Jiao, R. K. Raj and K. Rajashekara, "A Novel DROGI Based Control Algorithm Without PLL for Shunt Compensation Using Four-leg Converter," 2019 *IEEE Industry Applications Society Annual Meeting*, Baltimore, MD, USA, 2019, pp. 1–6.
3. S. Jiao, K. Rajashekara, R. K. Potti, L. Ben-Brahim and A. Gastli, "A Double Reduced Order Generalized Integrator based Algorithm for Control of Four-leg Converter to Enhance Power Quality," 2019 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 4293–4298.

Chapter 4

A Novel Four-leg Converter Control Algorithm for Unbalanced Nonlinear Load Compensation for Grid-Connected Systems

4.1 Introduction

In a three-phase four-wire microgrid system, it is possible that several unbalanced linear and non-linear loads are connected, which could lead to adverse Power Quality (PQ) problems, such as unbalanced AC source currents, increased neutral current, and poor power factor operation. The proposed control strategies in Chapter 2-3 are suitable for mitigating the above linear loads related PQ problems. However, the nonlinear loads like arc furnaces, air-conditioners, and switched-mode power supplies draw harmonic currents from the AC source [48]–[52]. As a result, the Total Harmonic Distortion (THD) of AC source currents is increased and higher than 5% (above the recommended limits as in the IEEE 1547 standards) [53]. Moreover, when the grid voltage becomes unbalanced and distorted, the PQ problems further aggravate and negative sequence components of grid voltage harm the operation of the converter by deteriorating Phase Locked Loop (PLL) performance [54]. Thus, a proper synchronization technique and control strategy for the four-leg converter is crucial to mitigate the effects of poor grid operating conditions.

Under unbalanced nonlinear loads and unbalanced distorted grid conditions, the purpose of the four-leg converter is to compensate the desired currents such that AC source currents can be balanced and in phase with the Fundamental Frequency Positive Sequence

Components (FFPSC) of the grid voltage [55]. Thus, the synchronization method plays a very important role for the converter to get the desired reference currents. The three-phase synchronous reference frame phase-locked loop (SRF-PLL) is one of the most used techniques for grid synchronization. However, SRF-PLL suffers from phase estimation inaccuracy in the presence of unbalanced distorted grid voltages [56]. To solve this issue, including additional filters either ahead or within the PLL block are proposed [57]–[59]. In [57], a pre-filtering technique, namely moving average filter (MAF) is presented. It uses two MAFs to extract the fundamental positive sequence component of grid voltage for SRF-PLL. However, due to the window width of MAF, the dynamic performance of PLL is poor. Its improved version, namely differential MAF-PLL proposed in [58], incorporates a special proportional component in the MAF-based PLL. This approach increases the open-loop bandwidth and enhances the transient performance of PLL. Reference [59] proposes another approach with decoupled double synchronous reference frame PLL (DDSRF-PLL) which exploits two synchronous reference frames rotating at the fundamental frequency, one counterclockwise and the other one clockwise. In this case, the positive sequence component of grid voltage can be extracted accurately. But, due to the presence of low pass filters in DDSRF, such method suffers from poor dynamics.

To overcome the limitations of the aforementioned studies, this chapter proposes a novel synchronization technique namely ROGI-PLL for the four-leg converter under unbalanced distorted grid condition. Such approach has the unique feature that the FFPSC of grid voltage can be detected accurately and rapidly, without any computational intensive filtering technique and low pass filters. Hence, the open-loop bandwidth of SRF-PLL can be increased and the transient performance of PLL can be improved. A comparison of the

proposed scheme and traditional methods (DDSRF-PLL and DSOGI-PLL) is carried out through simulation and experimental tests. Furthermore, to compensate unbalanced nonlinear loads, based on ROGI-PLL, a novel control algorithm, namely Triple-ROGI (TROGI), is proposed. As a result, the AC source currents are balanced and in phase with the FFPSC of the grid voltage. Also, since the compensation mode (DC-AC) and rectification mode (AC-DC) of the four-leg converter with dc-link supported by capacitors are decoupled, better flexibility and selectivity in terms of control methods for the converter are achieved. The effectiveness of the proposed control strategy is verified through simulation and experimental results.

4.2 Generalized Model of the Compensation System

In a three-phase four-wire microgrid system, under unbalanced distorted gird condition, the three-phase voltages can be mathematically expressed as [60]

$$\begin{cases} u_{sa}(t)=\sum_{n=1}^{\infty}\sqrt{2}V_{n+}\sin\left(n\omega t+\theta_{vn+}\right)+\sum_{n=1}^{\infty}\sqrt{2}V_{n-}\sin\left(n\omega t+\theta_{vn-}\right) \\ \qquad\qquad +\sum_{n=1}^{\infty}\sqrt{2}V_{n0}\sin\left(n\omega t+\theta_{vn0}\right) \\ u_{sb}(t)=\sum_{n=1}^{\infty}\sqrt{2}V_{n+}\sin\left(n\left(\omega t-\frac{2}{3}\pi\right)+\theta_{vn+}\right)+\sum_{n=1}^{\infty}\sqrt{2}V_{n-}\sin\left(n\left(\omega t+\frac{2}{3}\pi\right)+\theta_{vn-}\right) \\ \qquad +\sum_{n=1}^{\infty}\sqrt{2}V_{n0}\sin\left(n\omega t+\theta_{vn0}\right) \\ u_{sc}(t)=\sum_{n=1}^{\infty}\sqrt{2}V_{n+}\sin\left(n\left(\omega t+\frac{2}{3}\pi\right)+\theta_{vn+}\right)+\sum_{n=1}^{\infty}\sqrt{2}V_{n-}\sin\left(n\left(\omega t-\frac{2}{3}\pi\right)+\theta_{vn-}\right) \\ \qquad +\sum_{n=1}^{\infty}\sqrt{2}V_{n0}\sin\left(n\omega t+\theta_{vn0}\right) \end{cases}, \tag{4.1}$$

where u_{sa}, u_{sb}, and u_{sc} are three-phase voltage. V_{n+}, V_{n-}, and V_{n0} are RMS values positive, negative, and zero sequence components of grid voltage. θ_{vn+}, θ_{vn-}, and θ_{vn0} are phase angles of corresponding sequence grid voltage, n=1, 2, 3….

Similarly, due to the unevenly distributed nonlinear loads, the load currents can be decomposed into

$$\begin{cases} i_{la}(t)=\sum_{n=1}^{\infty}\sqrt{2}I_{n+}\sin\left(n\omega t+\theta_{in+}\right)+\sum_{n=1}^{\infty}\sqrt{2}I_{n-}\sin\left(n\omega t+\theta_{in-}\right) \\ \qquad +\sum_{n=1}^{\infty}\sqrt{2}I_{n0}\sin\left(n\omega t+\theta_{in0}\right) \\ i_{lb}(t)=\sum_{n=1}^{\infty}\sqrt{2}I_{n+}\sin\left(n\left(\omega t-\frac{2}{3}\pi\right)+\theta_{in+}\right)+\sum_{n=1}^{\infty}\sqrt{2}I_{n-}\sin\left(n\left(\omega t+\frac{2}{3}\pi\right)+\theta_{in-}\right) \\ \qquad +\sum_{n=1}^{\infty}\sqrt{2}I_{n0}\sin\left(n\omega t+\theta_{in0}\right) \\ i_{lc}(t)=\sum_{n=1}^{\infty}\sqrt{2}I_{n+}\sin\left(n\left(\omega t+\frac{2}{3}\pi\right)+\theta_{in+}\right)+\sum_{n=1}^{\infty}\sqrt{2}I_{n-}\sin\left(n\left(\omega t-\frac{2}{3}\pi\right)+\theta_{in-}\right) \\ \qquad +\sum_{n=1}^{\infty}\sqrt{2}I_{n0}\sin\left(n\omega t+\theta_{in0}\right) \end{cases}, \tag{4.2}$$

where i_{la}, i_{lb}, and i_{lc} are three-phase currents. I_{n+}, I_{n-}, and I_{n0} are RMS values of each frequency positive, negative, and zero sequence components of load currents. θ_{vn+}, θ_{vn-}, andθ_{vn0} are phase angles of corresponding sequence load currents.

Based on equation (4.1) and (4.2), the instantaneous power with respect to load side can be expressed as follows:

$$\begin{aligned} P &= (u_s^+ + u_s^- + v_s^0)\cdot(i_l^+ + i_l^- + i_l^0) \\ &= \underbrace{(u_s^+ \cdot i_l^+}_{\bar{P}_+} + \underbrace{u_s^- \cdot i_l^-}_{\bar{P}_-} + \underbrace{u_s^0 \cdot i_l^0}_{\bar{P}_0}) + (\underbrace{u_s^+ \cdot i_l^- + u_s^- \cdot i_l^+}_{\tilde{P}_{+-}} + \underbrace{u_s^0 \cdot i_l^{+-} + u_s^{+-} \cdot i_l^0}_{\tilde{P}_0}) \end{aligned}, \tag{4.3}$$

$$\tilde{P}_{+-} = \sum_{n=1}^{\infty} -3V_{n+}I_{n-}\cos\left(2n\omega t + \theta_{vn+} - \theta_{in-}\right) + \sum_{n=1}^{\infty} -3V_{n-}I_{n+}\cos\left(2n\omega t + \theta_{vn-} + \theta_{in+}\right) + \sum_{\substack{m=1 \\ m\neq n}}^{\infty}\left[\sum_{n=1}^{\infty} 3V_{m+}I_{n+}\cos\left((m\omega - n\omega)t + \theta_{vm+} - \theta_{in+}\right)\right] + \sum_{\substack{m=1 \\ m\neq n}}^{\infty}\left[\sum_{n=1}^{\infty} 3V_{m-}I_{n-}\cos\left((m\omega - n\omega)t + \theta_{vm-} - \theta_{in-}\right)\right] + \sum_{\substack{m=1 \\ m\neq n}}^{\infty}\left[\sum_{n=1}^{\infty} -3V_{m+}I_{n-}\cos\left((m\omega + n\omega)t + \theta_{vm+} + \theta_{in-}\right)\right] + \sum_{\substack{m=1 \\ m\neq n}}^{\infty}\left[\sum_{n=1}^{\infty} -3V_{m-}I_{n+}\cos\left((m\omega + n\omega)t + \theta_{vm-} + \theta_{in+}\right)\right], \quad (4.4)$$

$$\tilde{P}_{0} = \sum_{n=1}^{\infty} -3V_{n0}I_{n0}\cos\left(2n\omega t + \theta_{vn0} + \theta_{in0}\right) + \sum_{\substack{m=1 \\ m\neq n}}^{\infty}\left[\sum_{n=1}^{\infty} 3V_{m0}I_{n0}\cos\left((m\omega - n\omega)t + \theta_{vm0} - \theta_{in0}\right)\right] + \sum_{\substack{m=1 \\ m\neq n}}^{\infty}\left[\sum_{n=1}^{\infty} -3V_{m0}I_{n0}\cos\left((m\omega + n\omega)t + \theta_{vm0} + \theta_{in0}\right)\right], \quad (4.5)$$

$$\bar{P}_{+} = \underbrace{3V_{+}I_{+}\cos\left(\theta_{v+} - \theta_{i+}\right)}_{\bar{P}_{1+}} + \underbrace{\sum_{n=2}^{\infty} 3V_{n+}I_{n+}\cos\left(\theta_{vn+} - \theta_{in+}\right)}_{\bar{P}_{n+}}, \quad (4.6)$$

$$\bar{P}_{-} = \sum_{n=1}^{\infty} 3V_{n-}I_{n-}\cos\left(\theta_{vn-} - \theta_{in-}\right), \quad (4.7)$$

and

$$\bar{P}_{0} = \sum_{n=1}^{\infty} 3V_{n0}I_{n0}\cos\left(\theta_{vn0} - \theta_{in0}\right), \quad (4.8)$$

where "-" indicates the average powers, "~" is the oscillation powers, and "+, - ,0" means positive, negative, and zero sequence components, respectively.

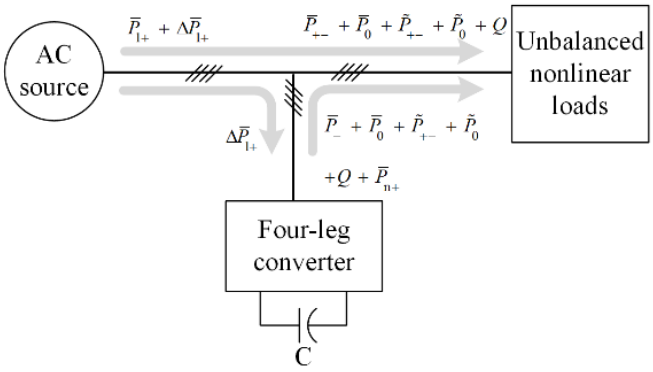


Figure 4.1: Power flow of the system.

From equation (4.3), it can be concluded that the AC source currents will be balanced and in phase with the FFPSC of the grid voltage if $\bar{P}_{n+}$, $\bar{P}_{-}$, $\bar{P}_0$,$\tilde{P}_{+-}$, $\tilde{P}_0$ and reactive power (Q) consumption of loads are compensated by the four-leg converter. Furthermore, to maintain the DC bus voltage, the converter should absorb positive sequence active power $\Delta\bar{P}_{1+}$ as well. Thus, the complete power flow of the system is shown in Fig. 4.1.

4.3 Proposed Synchronization Technique and Control Strategy

4.3.1 Proposed Synchronization Method-ROGI Based PLL.

As discussed above, under unbalanced distorted grid condition, the FFPSC of the grid voltage should be extracted and synchronized by the converter. A proper synchronization with the grid is a very important aspect for proper control of converter operation. Using

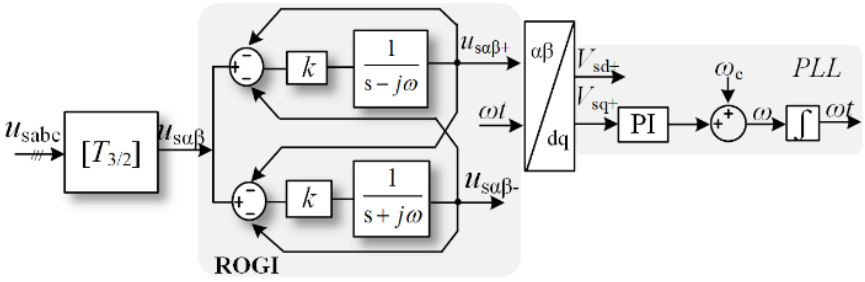


Figure 4.2: Diagram of the proposed ROGI-PLL.

the ROGI presented in [61], the FFPSC of unbalanced distorted grid voltage can be estimated accurately and rapidly. Thus, a ROGI operating as a pre-filter is introduced in this chapter for PLL to detect the phase angle and frequency.

The diagram of ROGI-PLL is illustrated in Fig. 4.2. By regulating V_{sq+} to be zero, the frequency (ω) of the FFPSC of unbalanced distorted grid voltage can be detected and fed back to the ROGI for FFPSC extraction. Also, due to the fast dynamic response of ROGI, the open-loop bandwidth of PLL can be increased, which improves the dynamic performance of synchronization. A comparison of ROGI-PLL with traditional synchronization methods (DDSRF-PLL, DSOGI-PLL) is also be provided in the following section.

4.3.2 Proposed Control Strategy-TROGI.

Considering unbalanced nonlinear loads compensation, a ROGI-PLL based control algorithm, namely Triple-ROGI (TROGI), is proposed in this chapter. Two additional ROGIs are utilized to generate the desired compensation and rectification currents such that the AC source currents are balanced and in phase with the FFPSC of the grid voltage. The block diagram of the proposed control method is shown in Fig. 4.3.

First, the phase angle (θ_{V1+}) and frequency (ω) of FFPSC ($u_{s\alpha+}$ and $u_{s\beta+}$) of unbalanced distorted grid voltage are estimated by using ROGI-PLL. Furthermore, to calculate the desired compensation currents, the load currents (i_{la}, i_{lb}, and i_{lc}) are sensed to extract the FFPSC with the help of the second ROGI. Since AC source currents should be balanced and in phase with the FFPSC of the grid voltage, the compensation currents can be estimated by the following expression

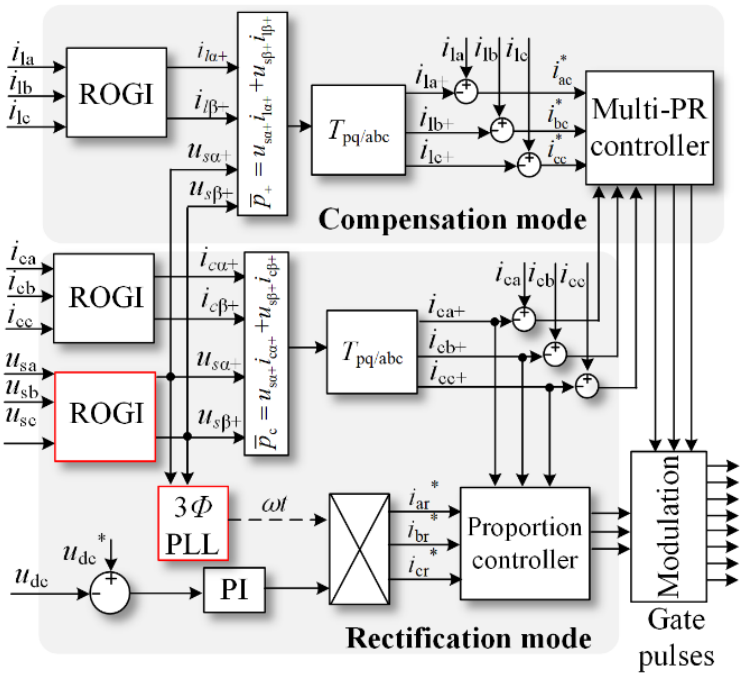


Figure 4.3: Proposed control algorithm.

$$\begin{bmatrix} i_{ac}^{*} \\ i_{bc}^{*} \\ i_{cc}^{*} \end{bmatrix} = \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} - \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \frac{1}{u_{s\alpha+}^{2} + u_{s\beta+}^{2}} \begin{bmatrix} u_{s\alpha+} & -u_{s\beta+} \\ u_{s\beta+} & u_{s\alpha+} \end{bmatrix} \begin{bmatrix} \bar{p}_{+} \\ 0 \end{bmatrix}, \tag{4.9}$$

where $\bar{p}_{+}$ is the positive sequence active power demand from loads.

Moreover, during the operation of the four-leg converter, the DC bus voltage should be maintained at the reference value. Thus, the third ROGI is employed to extract the desired absorbing currents (i_{ca+}, i_{cb+}, and i_{cc+}). Their reference values are generated by synchronizing with FFPSC of unbalanced distorted grid voltage

$$\begin{cases} i_{ca+}^{*} = i_{sm+}^{*} \sin\left(\omega t + \theta_{v1+}\right) \\ i_{cb+}^{*} = i_{sm+}^{*} \sin\left(\omega t - \frac{2}{3}\pi + \theta_{v1+}\right) \\ i_{cc+}^{*} = i_{sm+}^{*} \sin\left(\omega t + \frac{2}{3}\pi + \theta_{v1+}\right) \end{cases}, \tag{4.10}$$

where i^*_{sm+} is the amplitude of reference fundamental frequency positive sequence current, and it is estimated from a PI controller.

4.3.3 Proportional Resonant Controller.

To compensate unbalanced non-linear loads in a three-phase four-wire system, the reference currents for the compensation mode (i_{ac}^*, i_{bc}^*, i_{cc}^*) should be tracked properly. Hence, an improved multi-PR controller is used to regulate the compensation currents, which is expressed as,

$$G_{\mathrm{PR}}(s) = K_p + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_n^{\ 2}}, \tag{4.11}$$

where K_p and K_r are the proportional and integral gains of the PR controller respectively. ω_c decides the bandwidth, ω_n is the resonant frequency, which is set to 1st, 3rd, 5th, 7th, 11th, 13th, and 17th order frequencies for the unbalanced harmonic current compensation in this chapter.

Based on equation (4.11), the close loop transfer function of the current control system can be derived as

$$i_a = \frac{G_{PR}(s)G_{pwm}(s)G_0(s)}{1+G_{PR}(s)G_{pwm}(s)G_0(s)} i_{ref}^*, \tag{4.12}$$

where G_pwm(s) is the transfer function of modulation and G_o(s) is the transfer function of the output filter.

From equation (4.12), it can be noticed that if the gain of G_PR(s)G_pwm(s)G_o(s) is large enough, the actual current i_a can track the reference current i_ref^*. As a result, the compensation currents can be provided by the converter into the system. Fig. 4.4 shows the bode plot of PR controller for different values of K_r and ω_c. It can be seen that, with an

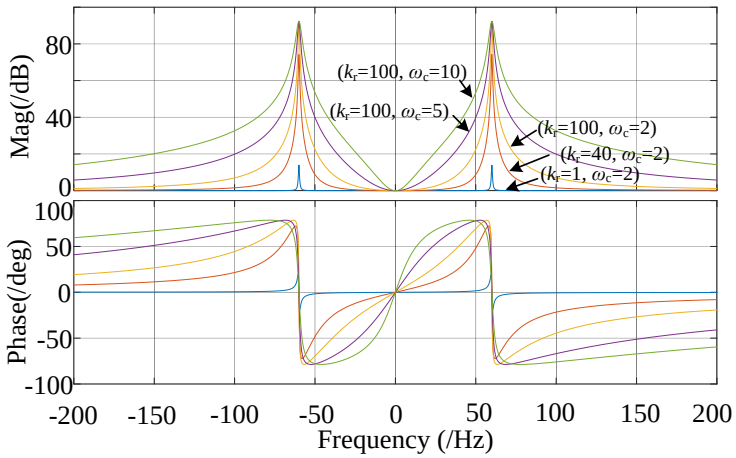


Figure 4.4: Bode plot of PR controller with various values of K_r and ω_c.

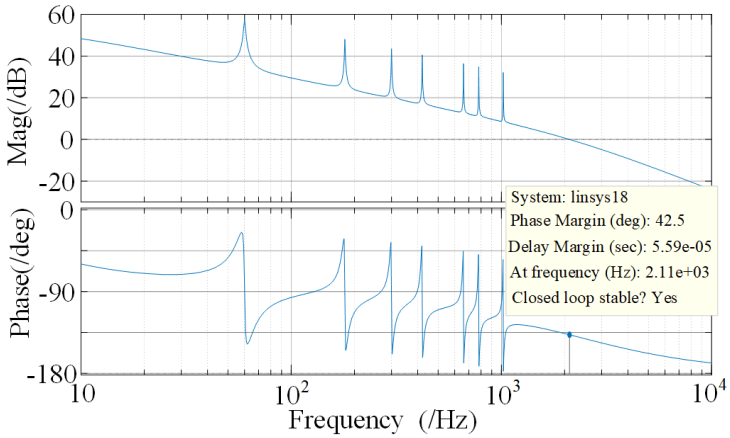


Figure 4.5: Bode plot of open loop transfer function.

increase in values of K_r and ω_c, the overall gain and bandwidth of PR controller are increased. To keep the gain of $G_{PR}(s)G_{pwm}(s)G_o(s)$ large enough and to account for the grid frequency variation, K_r and ω_c are set to be 70 and 2 respectively. The open-loop transfer function of the control system is shown in Fig. 4.5. It can be seen that the phase margin is 42.5 degrees, which guarantees the stability of the proposed control system. Further, to implement PR controller in DSP, equation (7) is discretized from *s* domain to *z* domain, which can be expressed as [62]

$$G_{\mathrm{PR}}(z)=\frac{b_0+b_1z^{-1}+b_2z^{-2}}{1+a_1z^{-1}+a_2z^{-2}}, \tag{4.13}$$

where a_1, a_2, b_0, b_1, and b_2 are the coefficients and expressed as

$$\begin{cases} b_0=\dfrac{2K_I\omega_cC}{C^2+2\omega_cC+\omega^2}+K_P \\ b_1=\dfrac{\left(2\omega^2-2C^2\right)K_P}{C^2+2\omega_cC+\omega^2} \\ b_2=\dfrac{K_P\left(C^2-2\omega_cC+\omega^2\right)-2K_I\omega_cC}{C^2+2\omega_cC+\omega^2} \\ a_1=\dfrac{2\omega^2-2C^2}{C^2+2\omega_cC+\omega^2} \\ a_2=\dfrac{C^2-2\omega_cC+\omega^2}{C^2+2\omega_cC+\omega^2} \\ C=\dfrac{\omega}{\tan\dfrac{\omega T_s}{2}} \end{cases}. \tag{4.14}$$

4.4 Simulation and Experimental Study

In this section, detailed simulation and experimental verification of the proposed PLL and control strategy is provided. Comparative performance of the proposed ROGI-PLL traditional synchronization methods (DDSRF-PLL, DSOGI-PLL) are also presented. The parameters of the system is given in Table 4.1.

Table 4.1: Parameters of the system under Unbalanced Distorted Load/Grid Condition

Parameters	**Value**
DC-link voltage u_{dc}	320V
Grid frequency f	60Hz
Interfacing inductor	6mH
Phase A loads	30Ω and 16mH
Phase B loads	Diode bridge with 40Ω
Phase C loads	27.5Ω and 6mH

4.4.1 Simulation Results

To evaluate the performance of the proposed ROGI-PLL, simulations of ROGI-PLL, DDSRF-PLL, and DSOGI-PLL are carried out in MATLAB/SIMULINK. The comparison performance is studied in two cases.

1) Case 1: Grid Frequency Deviation:

Grid frequency jumps from 60 Hz to 55 Hz. Fig. 4.6 shows the simulated frequency tracking and phase angle estimation performance of the three PLL methods. It can be seen that ROGI-PLL can track the frequency within 2.5 fundamental cycles with the fastest dynamic response, compared with the other two PLLs. This is due to the presence of a low pass filter in those conventional PLLs.

2) Case 2: Unbalanced Grid Voltage Condition.

In this case, the RMS value of phase b voltage drops to 90V. Fig 4.7 shows that the proposed PLL has a smaller settling time to detect the amplitude of FFPSC of unbalanced

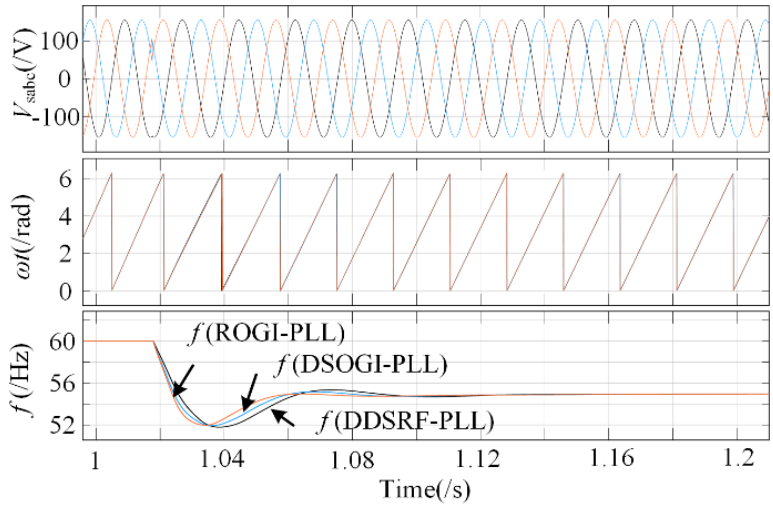


Figure 4.6: Simulation results of proposed ROGI-PLL, DDSRF-PLL, and DSOGI-PLL under grid frequency jump.

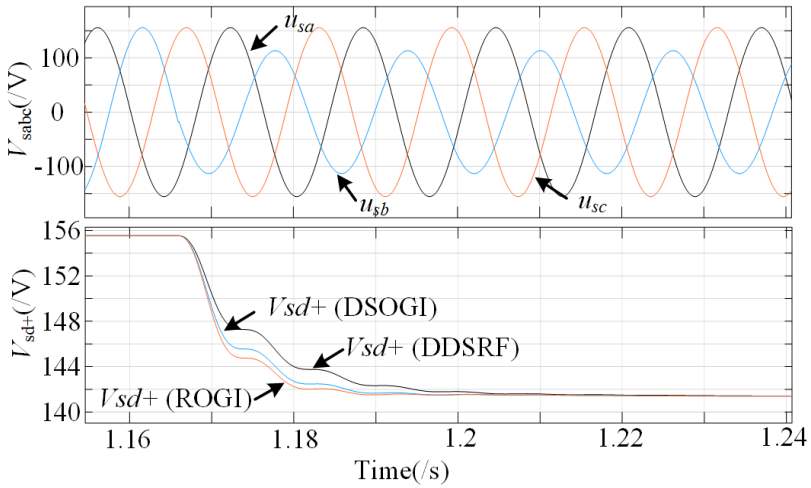


Figure 4.7: Simulation results of proposed ROGI-PLL, DDSRF-PLL, and DSOGI-PLL under unbalanced grid voltage condition.

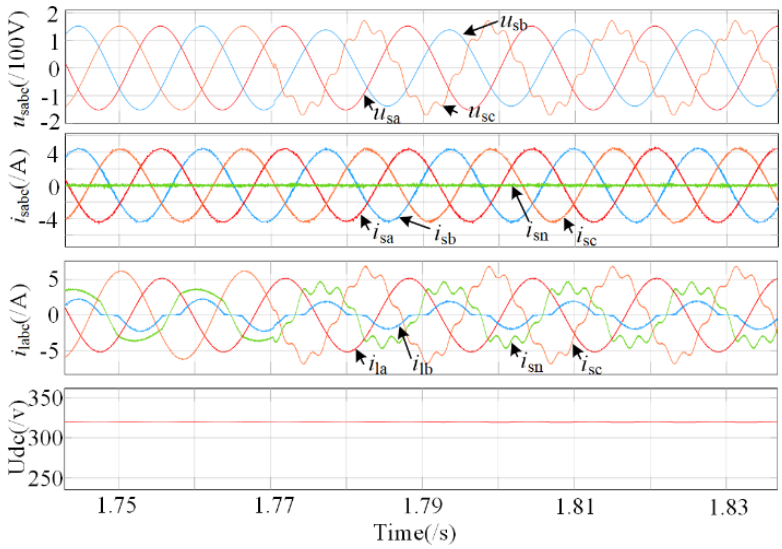
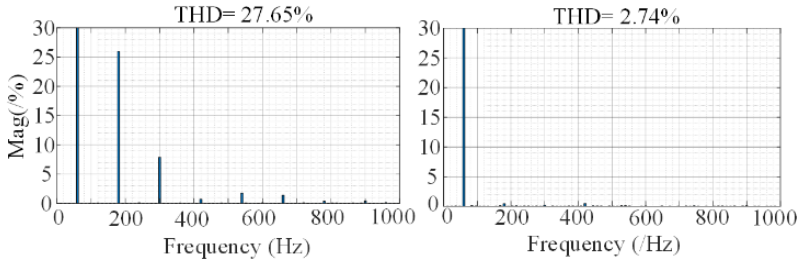


Figure 4.8: Simulation results of proposed control strategy (TROGI) under unbalanced nonlinear loads and unbalanced distorted grid condition.



(a) (b)

Figure 4.9: Simulation results of THD analysis of phase b current. (a) THD value of load side current. (b) THD value of AC source side current.

grid voltage. The simulation results of the proposed control strategy are presented in Fig. 4.8. These results illustrate waveforms of grid voltages (u_s), grid currents (i_s), load currents (i_l) and DC bus voltage (u_{dc}).

From Fig. 4.8, it can be observed that, under the unbalanced nonlinear loads condition and distorted grid voltage conditions, grid currents are still balanced and sinusoidal. Also, the DC bus voltage is maintained constant irrespective of load or source-side disturbances, since the compensation mode (DC-AC) and rectification mode (AC-DC) of the converter are decoupled.

Fig. 4.9 shows the THD analysis of phase 'b' current. It can be seen that the THD value of the grid-side current is reduced to be 2.74%, while the THD value of the load side current is still high. This simulation result verifies the tracking performance of the PR controller.

4.4.2 Experimental Results

To further validate the performance of the proposed ROGI-PLL and control strategy, a prototype of the four-leg converter is developed, as shown in Fig. 4.10. Algorithms are

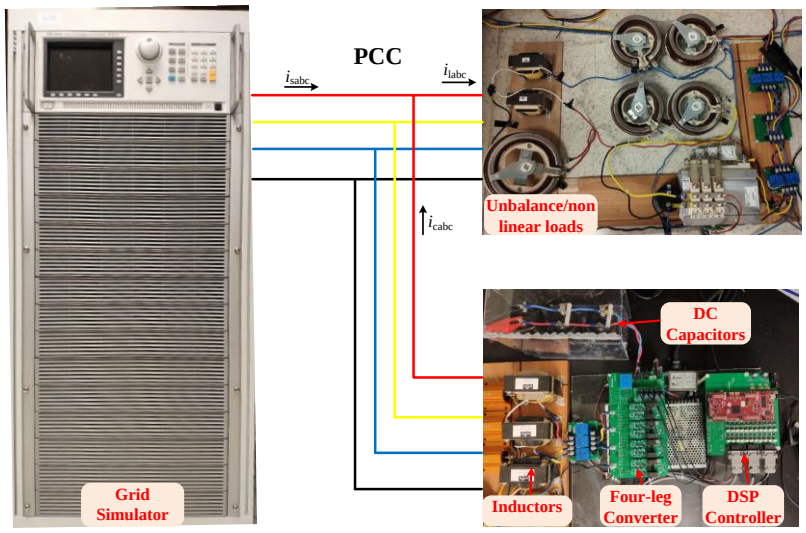
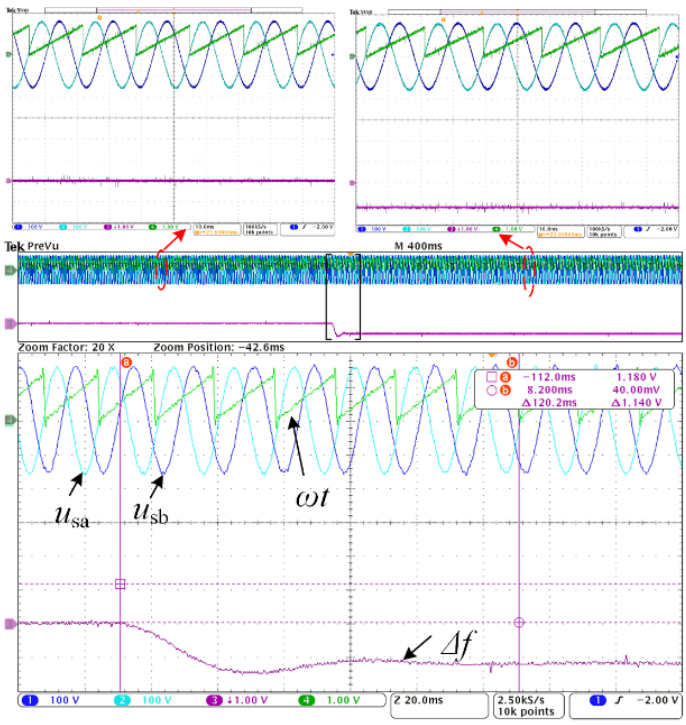


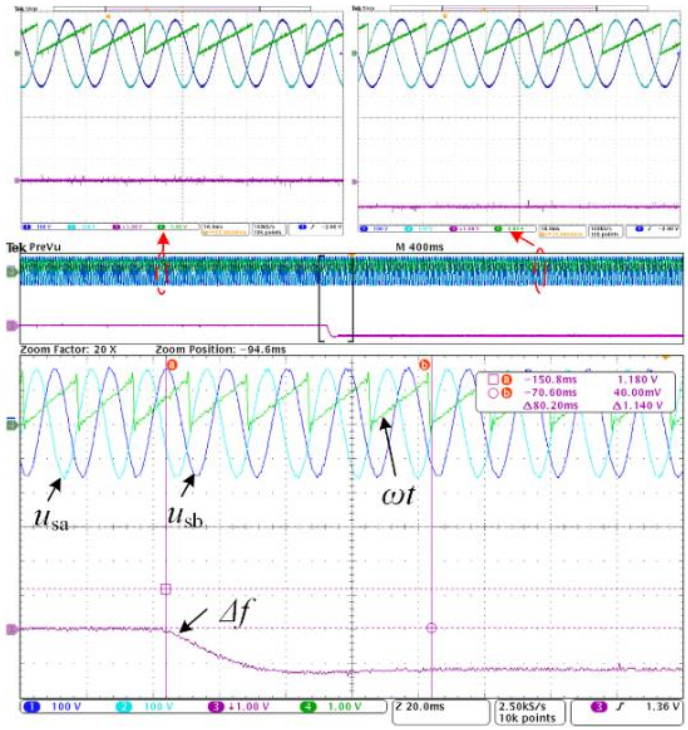
Figure 4.10: Experimental setup.

implemented on a digital signal processor TMS320F28379D platform. A programmable AC source-Chroma 61611 is employed to provide the desired grid voltage. Voltage and current sensing are performed using Hall Effect sensors LEM LV-25 and LEM LA-25 respectively. The experimental results are observed using a digital scope oscilloscope (TEKTRONIX MDO4024C). The control algorithm is verified and demonstrated under steady-state and dynamic conditions.

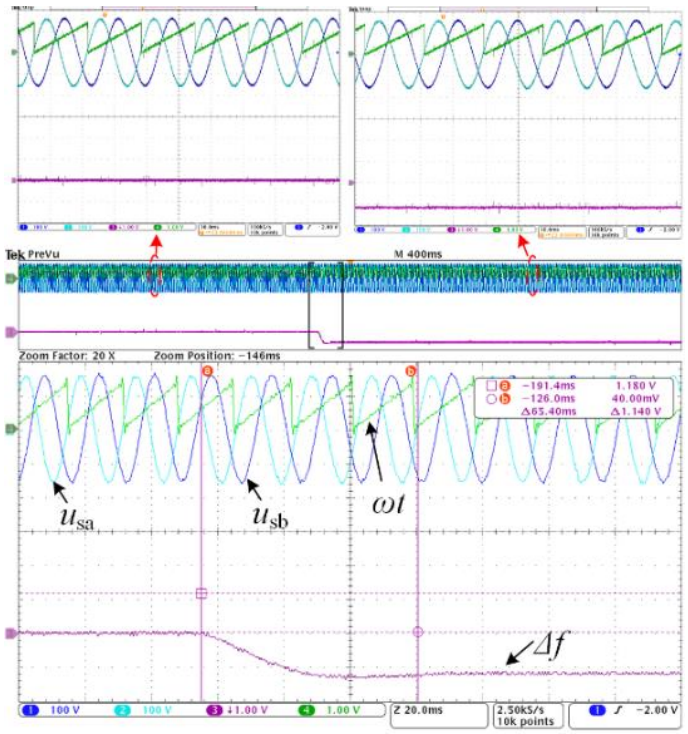
Fig. 4.11 depicts the tracking performances of phase angle for three PLL methods when the grid voltage undergoes a frequency step change from 60 Hz to 55 Hz. It can be seen that the proposed ROGI-PLL takes 65.4ms to detect the change in phase angle. However, DDSRF-PLL and DSOGI-PLL need 120.2ms and 80.2ms, respectively.



(a)



(b)



(c)

Figure 4.11: Comparison experimental results of the three PLL methods when frequency changes from 60Hz to 55Hz. (a) DDSRF-PLL. (b) DSOGI-PLL. (c) ROGI-PLL.

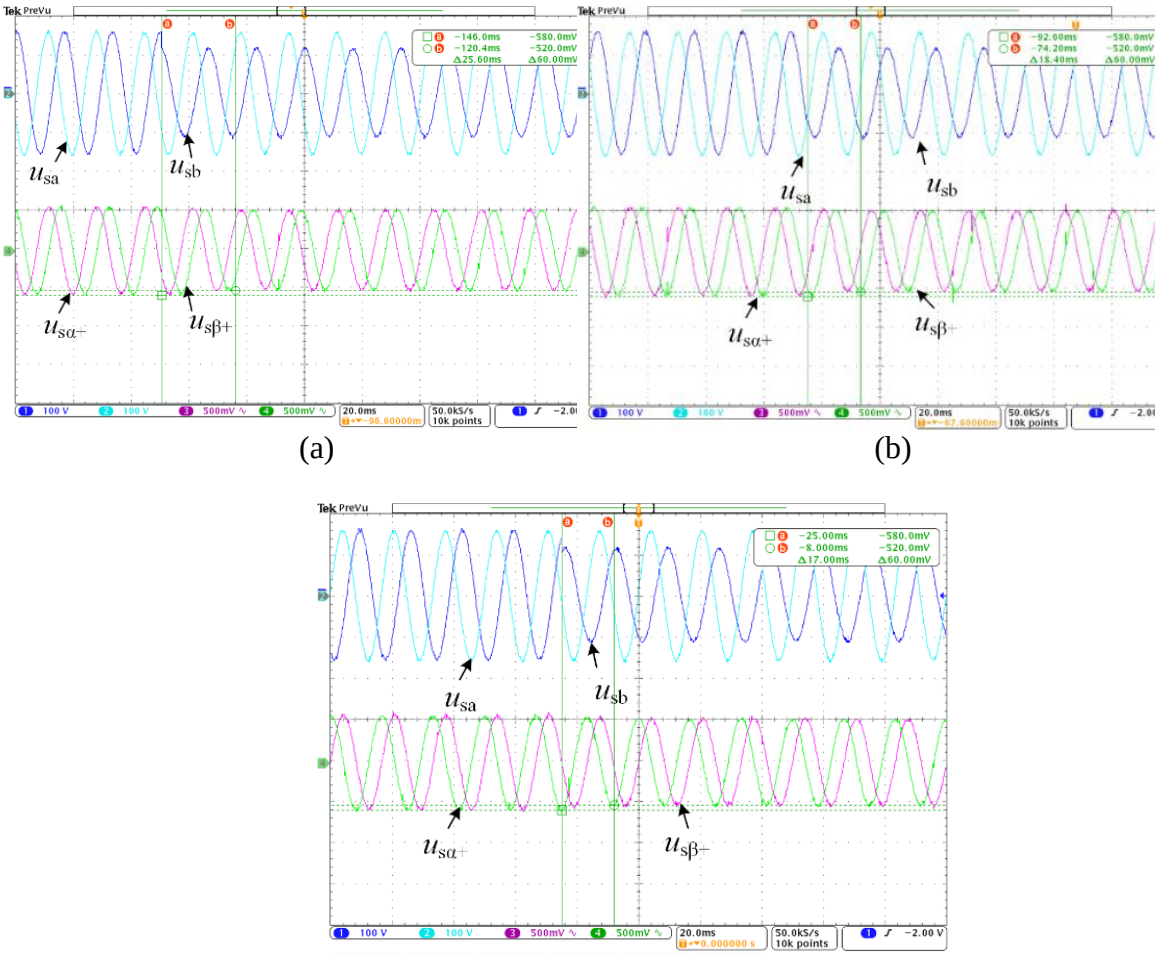


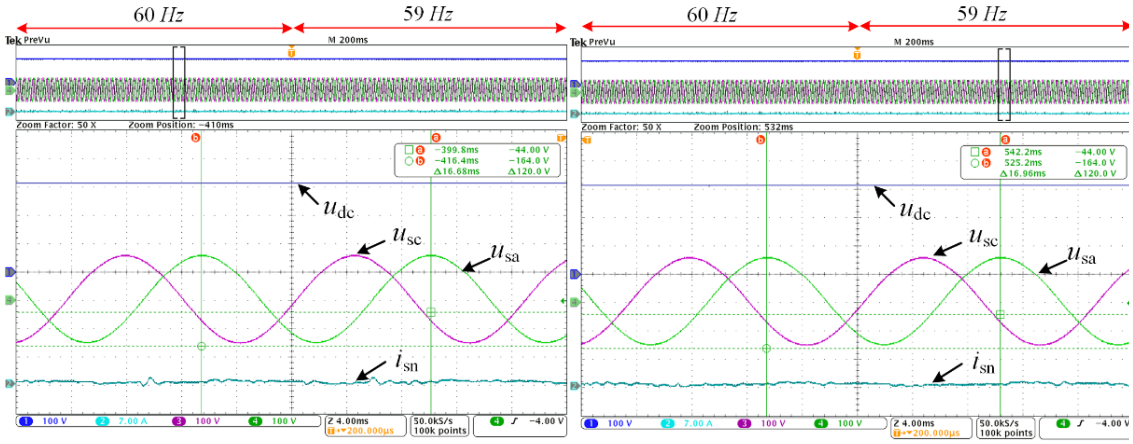
Figure 4.12: Comparison experimental results of the three PLL methods under unbalanced grid condition. (a)DDSRF-PLL. (b) DSOGI-PLL. (c) ROGI-PLL.

The experimental waveforms are also shown under unbalanced grid voltage condition in Fig. 4.12. It can be observed that only 17ms is required for ROGI-PLL to detect the FFPCS of unbalanced grid voltage. But it takes 18.4ms and 25.6ms for DSOGI-PLL and DDSRF-PLL, respectively. These experimental results demonstrate the fast dynamic response of the proposed ROGI-PLL.

To evaluate the effectiveness of the proposed control strategy. The experimental tests are carried out under two conditions.

1) Case 1: Balanced grid and unbalanced nonlinear loads condition.

Fig. 4.13 shows the compensation results when the gird frequency changes from 60 Hz to 59 Hz. It can be seen that even though the frequency of grid is varied, the DC bus voltage is still regulated constantly. Also, with the compensation of the four-leg converter, the neutral current of grid side is zero. Furthermore, to verify the reactive power compensation



(a) (b)

Figure 4.13: Experimental result of control strategy when the grid undergoes a frequency step from 60 Hz to 59 Hz. (a) 60 Hz. (b) 59Hz. (u_{sa}=100V/div, u_{sc}=100V/div, i_{sn}=7A/div, u_{dc}=100V/div, time scale=4ms/div).

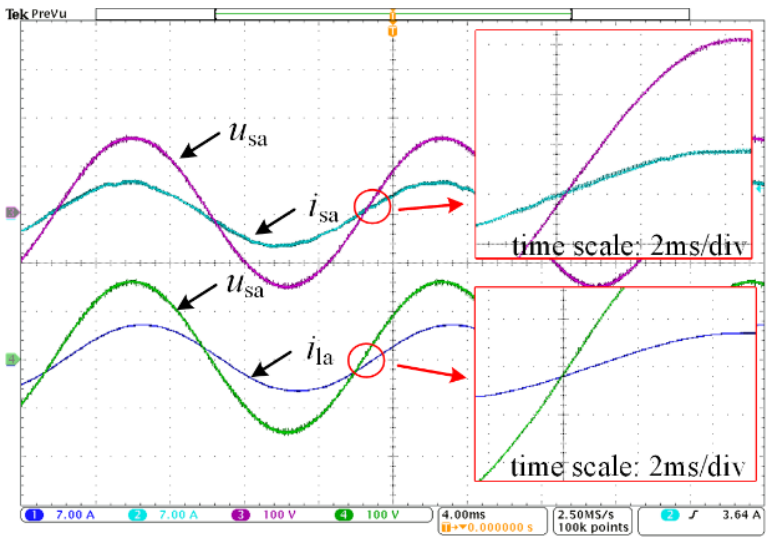


Figure 4.14: Experimental results of phase ‘a’ grid voltage, grid current and load current (u_{sa}=100V/div, i_{sa}=7A/div, i_{la}=7A/div, time scale=4ms/div).

of the proposed control method, the waveforms of phase ‘a’ grid voltage, grid current and load current are shown in Fig. 4.14. It can be observed that current of load side is lagging at 14 degrees due to reactive loading conditions. But, with the help of four-leg converter, the current and voltage of AC source terminal are in the same phase which means the AC source is operating with unity power factor. Fig. 4.15 illustrates the experimental results of

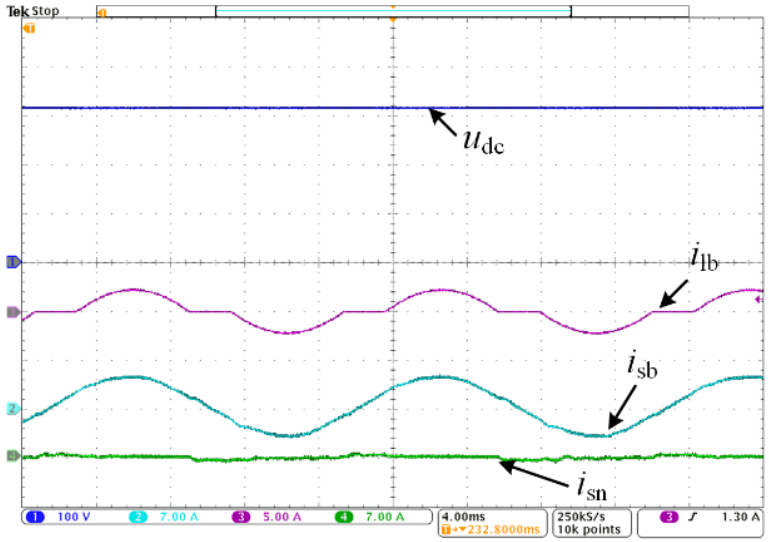


Figure 4.15: Experimental results of phase ‘b’ grid current, load current, DC bus voltage, and grid neutral current(i_{sb}=7A/div, i_{lb}=7A/div, i_{sn}=7A/div, u_{dc}=100V/div).

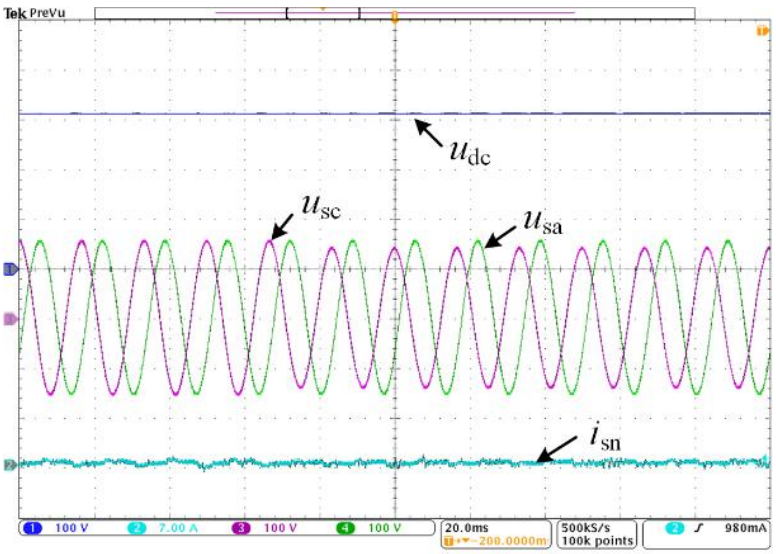


Figure 4.16: Experimental results of grid voltage, grid neutral current, and DC bus voltage (u_{sa}=100V/div, u_{sc}=100V/div, i_{sn}=7A/div, u_{dc}=100V/div, time scale=20ms/div).

phase ‘b’ grid current, load current, DC bus voltage, and grid neutral current. It can be seen that because of the nonlinear load in phase ‘b’, the load currents are distorted. However, with the help of the PR controller, the selective harmonic currents are compensated by the converter, so that the grid current is sinusoidal.

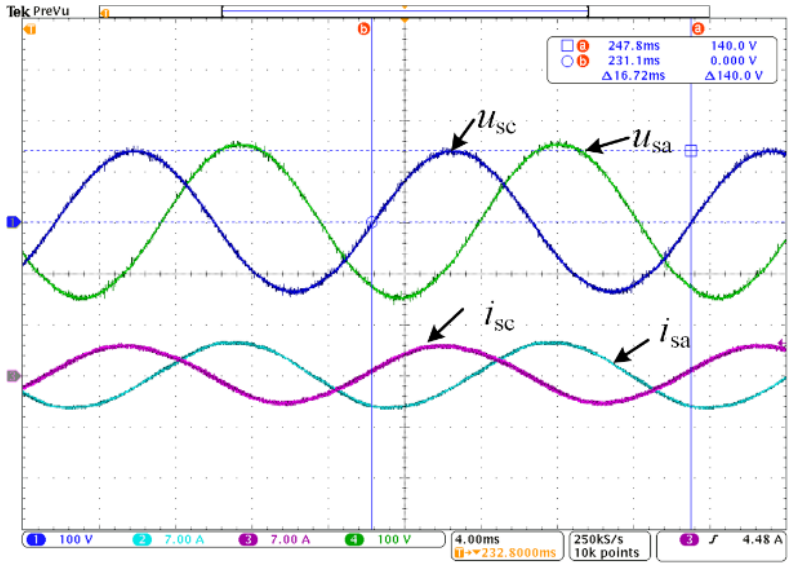


Figure 4.17: Experimental results of grid voltage, grid current (u_{sa}=100V/div, u_{sc}=100V/div, i_{sa}=7A/div, i_{sc}=7A/div, time scale=4ms/div).

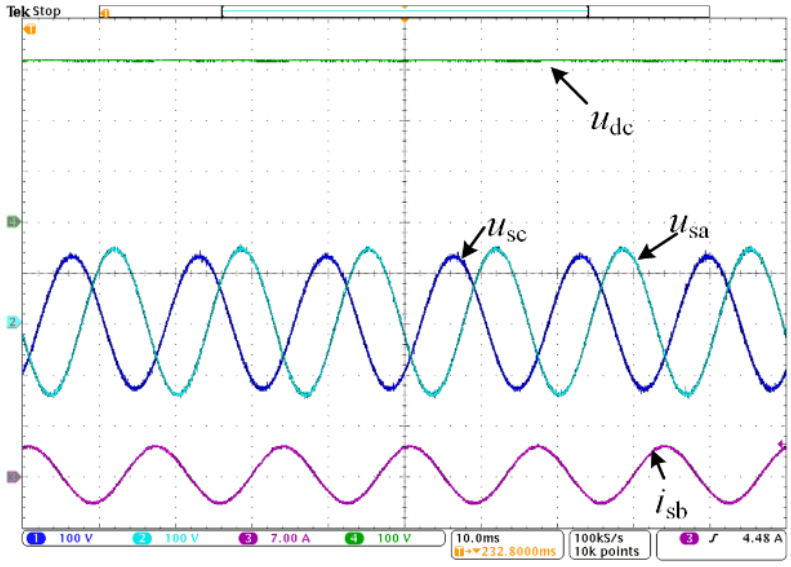


Figure 4.18: Experimental results of grid voltage, grid current, and DC bus voltage (u_{sa}=100V/div, u_{sc}=100V/div, i_{sb}=7A/div, u_{dc}=100V/div, time scale=10ms/div).

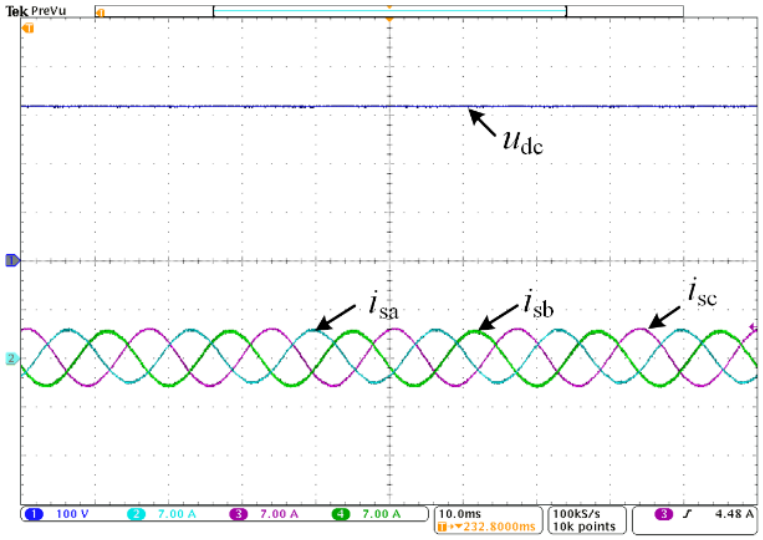


Figure 4.19: Experimental results of grid current, and DC bus voltage (i_{sa}=7A/div, i_{sb}=7A/div, i_{sc}=7A/div, u_{dc}=100V/div, time scale=10ms/div).

2) Case 2: Unbalanced grid and unbalanced nonlinear loads condition.

Under this condition, the RMS value of phase 'c' grid voltage is changed from 110V to 100V. Fig. 4.16-4.19 show the experimental waveforms of DC bus voltage, phase 'a' and 'c' grid voltages, and grid currents with proposed control technique. From Fig. 4.16, it can be seen that after the step change of grid voltage, the DC bus voltage of the converter is still regulated at its reference value (320V) constantly, and the neutral current of the grid side is zero. Fig. 4.17-4.19 show the grid currents and unbalanced grid voltage. It can be noticed that even though three-phase grid voltages are unbalanced, the grid side currents are still balanced and sinusoidal, which demonstrate the satisfactory operation of the proposed control algorithm.

4.5 Conclusion

This chapter proposes a novel ROGI-PLL based four-leg converter control algorithm for unbalanced nonlinear loads compensation, under both balanced grid and adverse grid conditions. In this approach, the phase angle and frequency of FFPSC from unbalanced

distorted grid voltage are estimated accurately and rapidly by using ROGI as a pre-filter for PLL. This scheme enables to increase the open-loop bandwidth of PLL and improve the dynamic performance of synchronization. Furthermore, considering unbalanced nonlinear loads compensation, two additional ROGIs are utilized to generate the desired compensation and rectification currents. As a result, the AC source currents are balanced and in phase with the FFPSC of the grid voltage. Also, since the compensation mode (DC-AC) and rectification mode (AC-DC) of the four-leg converter are decoupled, more flexibility and selectivity in terms of control methods for the converter are achieved. The effectiveness of the proposed control strategy is verified through simulation and experimental results for a 1.1 kW rated system.

4.6 Publications

1. S. Jiao, K. R. Ramachandran Potti, and K. Rajashekara, "A Novel DROGI Algorithm for Non-linear Unbalanced Load Compensation using Four-leg Converter," 2020 *IEEE Applied Power Electronics Conference (APEC)*, New Orleans, LA, 2020.
2. S. Jiao, K. R. Ramachandran Potti, and K. Rajashekara, "A Novel Phase-Locked Loop based Four-leg Converter Control for Unbalanced Load Compensation under Distorted and Unbalanced Grid Condition," 2020 *Energy Conversion Congress and Exposition (ECCE)*. (accepted)
3. S. Jiao, K. R. Ramachandran Potti, and K. Rajashekara, "A Novel Four-leg Converter Control Algorithm for Unbalanced Nonlinear Load Compensation for Grid Connected Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*. (submitted)

Chapter 5

Dual Current Loop Control Strategy for A Stand-alone Four-leg Converter in Aircraft Power Generation Applications

5.1 Introduction

The control algorithms for the four-leg converter to mitigate the PQ problems in a three-phase four-wire microgrid system have been presented in chapter 2-4. The proposed control algorithms help to achieve effective compensation of desired currents from the converter so that the AC source can supply balanced and sinusoidal currents irrespective of load or source-side disturbances. As an extension of this work, power quality improvements of a stand-alone system consisting of an ac load being fed by a four leg inverter is being investigated in this chapter. As an example, application of the four-leg converter for an aircraft electrical system consisting of a three-phase four-wire stand-alone power system with an induction generator is considered [63]. With the increasing trend and advancement of on-board electrical power generation for more electric aircraft (MEA) architecture, requirements to meet improved power quality, transient and dynamic performances during load-on and load-off operations for aircraft loads are very important [64]–[67].

The overall diagram of the aircraft generation system is shown in Fig.5.1. In this system, a squirrel cage induction generator (IG) is coupled to the aircraft engine. During generation mode, the active rectifier converts and control the variable frequency stator generated voltage to the desired DC voltage (320V), while the four-leg converter supplies ac loads at

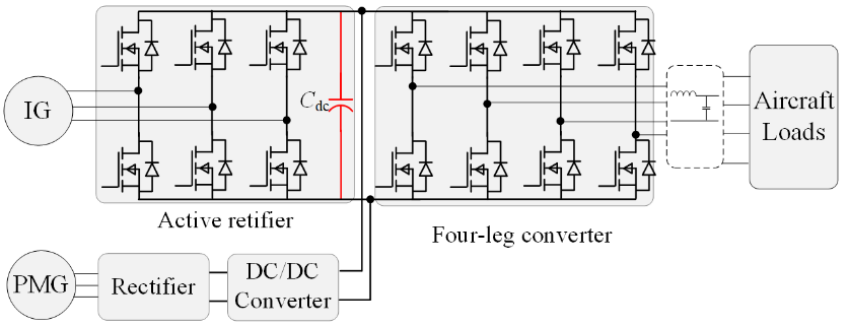


Figure 5.1: Overall diagram of the aircraft generation system.

400Hz/ 115V AC voltage.

In this chapter, instead of operating the converter as a shunt compensator for microgrid applications, the four-leg converter is operated as an inverter (stand-alone converter) supplying 400 Hz, 115V RMS phase voltage to electrical loads for aircraft applications, like single-phase loads, heating loads, and compressor loads [68]. For the aircraft electrical system, only positive sequence voltage should be supplied by the converter to the loads. To achieve this, a dual current loop control strategy is proposed in this chapter for the four-leg converter. The output voltages and currents of the converter are sensed and decomposed into positive and negative sequence components using ROGI. Further, the detected positive and negative sequence voltages are controlled in their respective d-q domain (positive sequence d-q co-ordinate rotates in counterclockwise and negative sequence d-q co-ordinate in clockwise directions). Finally, a Three Dimensional Space Vector Pulse Width Modulation (3D-SVPWM) is implemented to drive the four-leg converter. The feasibility of the operation of the proposed control strategy is demonstrated through simulation in MATLAB/Simulink.

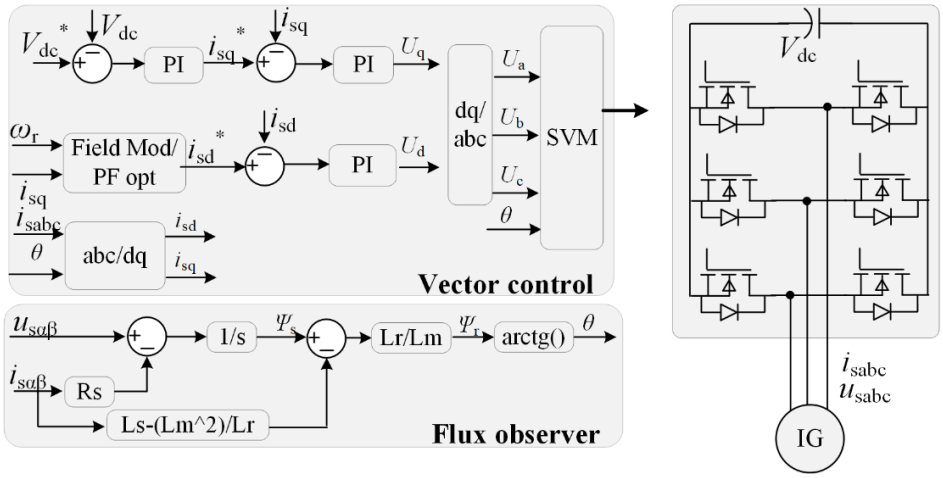


Figure 5.2: The overall block diagram of the control strategy for the generator side converter.

5.2 Control Strategy for Active Rectifier

The overall block diagram of the control strategy for the generator side converter is shown in Fig. 5.2. The sensorless field-oriented control strategy is used for the PWM rectifier, in which the rotor flux and speed are estimated based on the voltage model [69]. The DC-link voltage controller regulates the torque producing current component (q-axis) of the generator, while the flux producing current component is obtained from the voltage constraint equation.

There are two constraints to be satisfied to meet the required reference power-current constraint and voltage constraint. The current constraint is driven based on the relation:

$$I_{sd}^2 + I_{sq}^2 = I_{sm}^2 . \tag{5.1}$$

Whereas the voltage constraint is based on

$$\begin{cases} V_{sd}^2 + V_{sq}^2 = V_{sm}^2 \\ \left[\frac{R_s * I_{sq}}{\omega_e} + L_s * I_{sd}\right]^2 + \left[\frac{R_s * I_{sd}}{\omega_e} - \sigma L_s * I_{sq}\right]^2 \le \frac{V_{sm}^2}{\omega_e^2} \end{cases}, \tag{5.2}$$

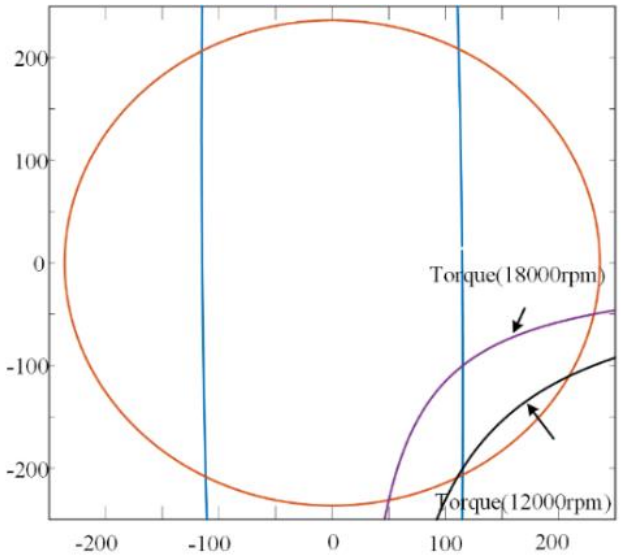


Figure 5.3: Operating constraint of the generator subsystem.

and

$$P_{sys} = -\omega_e \frac{T_e^*}{P} - R_s I_{sm}^2, \tag{5.3}$$

where V_{sd}, V_{sq}, I_{sd}, I_{sq}, are the d-q axis stator voltages and currents. R_s is the stator winding resistance. L_s is the stator inductance. ω_e , P_{sys}, P are the electrical frequency, rated power, and pole pairs of the induction machine.

Fig. 5.3 shows the different operating equilibrium points based on torque equation (5.3) for rated power under different speeds. Furthermore, it can be noted that the maximum constraint of the induction generator is limited by the voltage constraint of the system. The underrated current operation, the q-axis current variation along the rated circle operation is not really significant. Hence, it is not preferred to limit the q-axis current based on the rated current constraint, especially during the overloaded operation of the induction generator under field-oriented control. Thus, the DC voltage control loop will set the q-axis current reference, which is kept unreserved and not limited by the rated current constraint operation of the machine. Rather, the q-axis current loop will drive the operating point to move along the voltage circle and also to meet the power requirement.

5.3 ROGI Based Dual Current Loop Control Strategy

The topology of the stand-alone four-leg converter is shown in Fig. 5.4. The DC bus voltage (V_{dc}) is generated using PWM rectifier fed with induction generator. The four-leg converter is used to generate three-phase balanced AC voltages (400 Hz, 115V) from the generated DC-link voltage (320V) for the aircraft loads. An LC filter is used at the output of the four-leg converter to filter out the fundamental frequency AC voltage. From Fig. 5.4, it can be noticed that the neutral line of the four-wire system is provided by connecting the fourth leg of the four-leg inverter to the neutral point of loads. This configuration provides path for the zero-sequence current to flow and enables the four-leg inverter to regulate the zero-sequence voltage at the loads. In the aircraft electrical system, only the positive sequence voltage is supposed to be supplied by the converter to the loads. Therefore, a ROGI based dual current loop control strategy for the four-leg converter is proposed in this chapter. The overall control strategy is shown in Fig. 5.5.

First, the output voltage u_{iabc} and currents i_{iabc} are sensed and transformed into $\alpha\beta$ domain. Then, ROGI is used to decompose the positive and negative sequence components of voltages and currents. Furthermore, the detected positive and negative sequence voltages are controlled in their respective d-q domain (positive sequence d-q co-ordinate rotates in

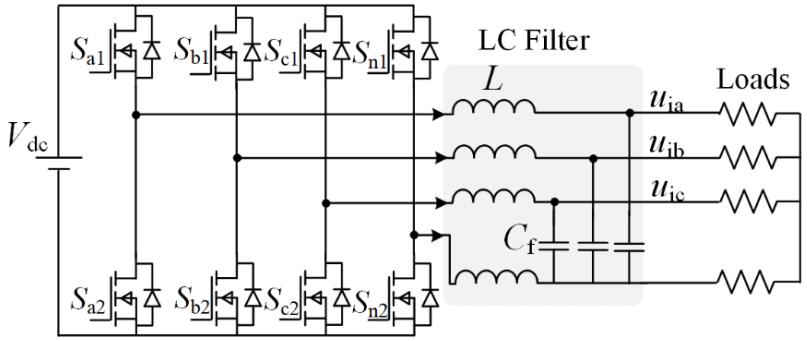


Figure 5.4: The topology of the stand-alone four-leg converter.

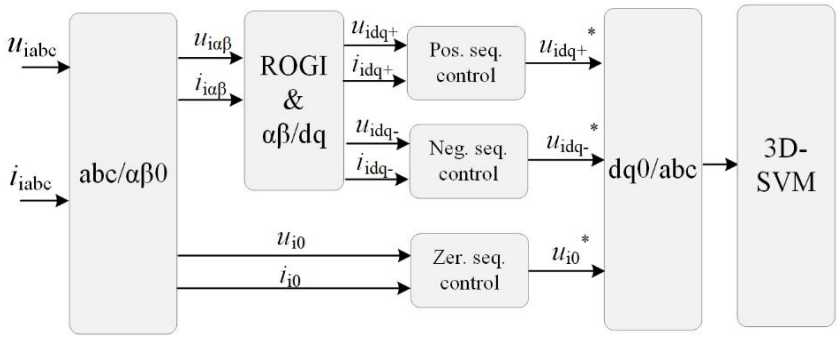


Figure 5.5: Diagram of control strategy for the stand-alone four-leg converter.

counterclockwise and negative sequence d-q co-ordinate in clockwise directions). PI controllers are used to regulate the voltage to respective reference values. In this case, the reference values for positive sequence d-q voltage are set to be 162 and 0 respectively, and the reference values for negative sequence d-q voltage are set to be 0. Finally, the outputof the controller is converted into modulation signals in *abc* domain and 3D-SVPWM is used to drive the four-leg converter [70].

As discussed in [71], the positive and negative sequence components of the four-leg converter control model can be decoupled and regulated separately. Thus, for positive sequence voltage regulation, an outer voltage regulator and inner current controller are used. They can be mathematically expressed as

$$\begin{cases} i_{id\_ref+} = k_{pv}\left(u_{id\_ref+} - u_{id+}\right) + k_{iv}\int\left(u_{id\_ref+} - u_{id+}\right) - \omega C_f u_{iq+} \\ i_{iq\_ref+} = k_{pv}\left(u_{iq\_ref+} - u_{iq+}\right) + k_{iv}\int\left(u_{iq\_ref+} - u_{iq+}\right) + \omega C_f u_{id+} \\ u_{d+}^* = k_{pi}\left(i_{id\_ref+} - i_{id+}\right) + k_{ii}\int\left(i_{id\_ref+} - i_{id+}\right) - \omega L i_{iq+} \\ u_{q+}^* = k_{pi}\left(i_{iq\_ref+} - i_{iq+}\right) + k_{ii}\int\left(i_{iq\_ref+} - i_{iq+}\right) + \omega L i_{id+} \end{cases}, \quad (5.4)$$

where i_{d_ref+}, i_{q_ref+} are the reference values of the positive sequence voltages in *dq* domain. k_{pv} and k_{iv} are the PI parameters of the outer voltage controller, k_{pi} and k_{ii} are the values of inner PI regulator. u_{id+}, u_{iq+}, i_{id+}, and i_{iq+} are the output positive sequence voltages and currents in *dq* domain respectively. In equation (5.4), $\omega C_f u_{iq+}$ and $\omega C_f u_{iq+}$ are the

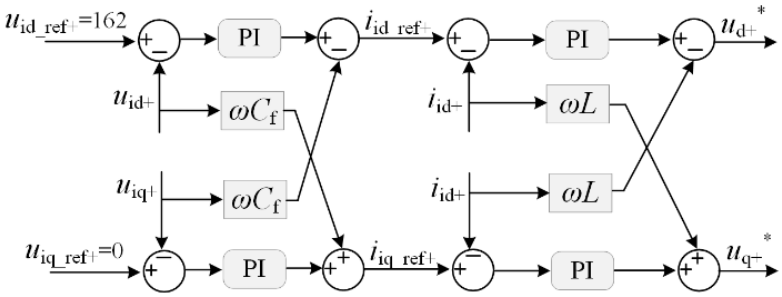


Figure 5.6: Control scheme of positive sequence voltage.

decoupling terms in outer voltage controller, and ωLi_{iq+} and ωLi_{id+} are the decoupling terms in the inner current regulator. Thus, the control diagram of positive sequence voltage controller can be shown as Fig. 5.6.

Similarly, to regulate the output negative sequence voltage, two controllers (outer voltage controller and inner current regulator) are implemented to ensure that the generated negative sequence voltage is zero. The difference of this control loop with positive sequence voltage regulation is that clockwise d-q co-ordinate is employed to transform the negative sequence voltage into DC values using the same PLL angle used for reference 3-phase voltage generation. Its controller is expressed as

$$\begin{cases} i_{id\_ref-} = k_{pv}\left(u_{id\_ref-} - u_{id-}\right) + k_{iv}\int\left(u_{id\_ref-} - u_{id-}\right) + \omega C_f u_{iq-} \\ i_{iq\_ref-} = k_{pv}\left(u_{iq\_ref-} - u_{iq-}\right) + k_{iv}\int\left(u_{iq\_ref-} - u_{iq-}\right) - \omega C_f u_{id-} \\ u_{d-}^* = k_{pi}\left(i_{id\_ref-} - i_{id-}\right) + k_{ii}\int\left(i_{id\_ref-} - i_{id-}\right) + \omega Li_{iq-} \\ u_{q-}^* = k_{pi}\left(i_{iq\_ref-} - i_{iq-}\right) + k_{ii}\int\left(i_{iq\_ref-} - i_{iq-}\right) - \omega Li_{id-} \end{cases}, \quad (5.5)$$

where i_{d_ref-}, i_{q_ref-} are the reference values of the positive sequence voltage in *dq* domain. u_{id-}, u_{iq-}, i_{id-}, and i_{iq-} are the output positive sequence voltages and currents in *dq* domain respectively.

The control diagram of negative sequence voltage regulation is shown as Fig.5.7. $\omega C_f u_{iq-}$ and $\omega C_f u_{iq-}$ are the decoupling terms in outer voltage controller, and ωLi_{iq-} and

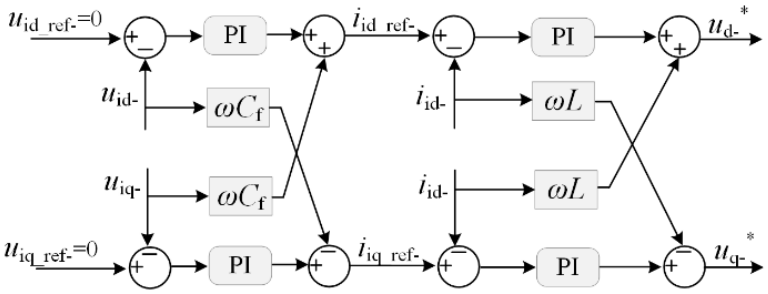


Figure 5.7: Control scheme for negative sequence voltage regulation.

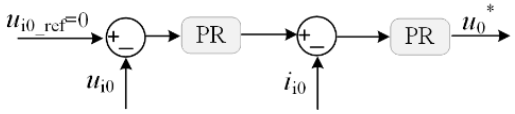


Figure 5.8: Control scheme for zero-sequence voltage regulation.

$\omega L i_{id-}$ are the decoupling terms in the inner current regulator respectively.

The zero-sequence voltage regulator is implemented using PR controller since the zero-sequence voltage is an ac quantity. The inner current control loop of zero-sequence voltage loop is also regulated using a PR controller. The reference value for zero-sequence voltage is set to be 0. The control scheme of the zero sequence voltage can be shown in Fig. 5.8.

5.4 Three-dimensional Space Vector Modulation in *abc* Domain

In the four-leg converter, the fourth leg extends the space vectors from two-dimensional plane to a three-dimensional plane which makes the selection of the vectors more complex. Most of the 3D-SVPWM are based on $\alpha\beta\gamma$ reference plane [72]–[75]. But such approach does not provide a clear picture of the vector positions in the space and makes the controller complicated [76]. Alternatively, in this chapter, the 3D-SVPWM in *abc* domain is implemented, such that the selection of the tetrahedron that contains a given voltage vector is simplified and easy to extend to multi-level (three-level) four-leg converter [77, 78].

5.4.1 Switching vectors of 3D-SVPWM

In general, the space vector modulation is used to generate an average voltage vector equal to the reference voltage vector. To achieve this, a switching function S_i is defined as

$$S_i = \begin{cases} 1 & \text{if } S_{i1} \text{ ON} \\ 0 & \text{if } S_{i2} \text{ ON} \end{cases} \qquad (i = a,\ b,\ c,\ n), \tag{5.6}$$

where S_{i1} is the switching status of the upper device, and S_{i2} is the switching status of the lower device, as shown in Fig.5.4.

Then, the phase voltage (u_{an}, u_{bn}, and u_{cn}) can be expressed as

$$u_{in}=V_{dc}*(S_i-S_n) \quad (i=a, b, c), \tag{5.7}$$

where S_n is the fourth leg switching function.

Table 5.1: Switching States and Vector in abc Domain

Status	S_a	S_b	S_c	S_n	U_{an}	U_{bn}	U_{cn}	**Vector**
1	0	0	0	0	0	0	0	V_1
2	0	0	1	0	0	0	1	V_2
3	0	1	0	0	0	1	0	V_3
4	0	1	1	0	0	1	1	V_4
5	1	0	0	0	1	0	0	V_5
6	1	0	1	0	1	0	1	V_6
7	1	1	0	0	1	1	0	V_7
8	1	1	1	0	1	1	1	V_8
9	0	0	0	1	-1	-1	-1	V_9
10	0	0	1	1	-1	-1	0	V_{10}
11	0	1	0	1	-1	0	-1	V_{11}
12	0	1	1	1	-1	0	0	V_{12}
13	1	0	0	1	0	-1	-1	V_{13}
14	1	0	1	1	0	-1	0	V_{14}
15	1	1	0	1	0	0	-1	V_{15}
16	1	1	1	1	0	0	0	V_{16}

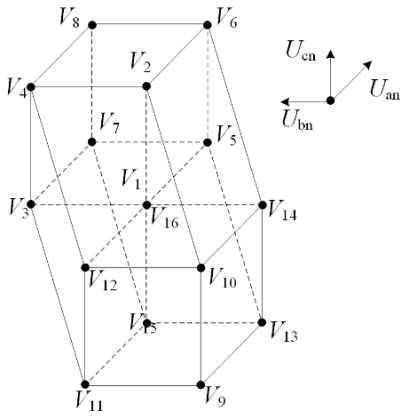


Figure 5.9: Switching vectors of the four-leg converter in *abc* domain

To simplify the notation, the phase voltages are normalized with DC link voltage V_{dc}. Therefore, all the 16 switching vectors in *abc* domain and respective switching functions are presented in Table 5.1. Also, based on the magnitude and polarity of the output phase voltage (u_{an}, u_{bn}, and u_{cn}), these 16 vectors can be divided into three types: positive, negative and zero vectors. Specifically, V_2-V_8 are positive vectors, V_9-V_{15} are negative vectors, and V_1, V_{16} are zero vectors.

Fig. 5.9 shows the voltage space vector diagram for the four-leg converter modulation. All vectors are in the vertices of two cubes: one is placed in the positive region (V_2-V_8) and the other one is in the negative region (V_9-V_{15}). V_1 and V_{16} are in the common vertex of both cubes. The region included in this dodecahedron is equivalent to the one that appears in $\alpha\beta\gamma$ reference plane [79].

5.4.2 Selection of Tetrahedron.

Similar to the sector selection of 2D-SVPWM in $\alpha\beta$ domain, the two cubes of 3D-SVPWM, as shown in Fig. 5.9, can be divided into 24 tetrahedrons, and each tetrahedron contains four vectors. To simplify the discussion, six indices are defined as

$$k_1=\begin{cases}1 & \left(v_{a\_ref}\geq 0\right)\\ 0 & \left(v_{a\_ref}<0\right)\end{cases}\quad k_4=\begin{cases}1 & \left(v_{a\_ref}-v_{b\_ref}\geq 0\right)\\ 0 & \left(v_{a\_ref}-v_{b\_ref}<0\right)\end{cases}$$
$$k_2=\begin{cases}1 & \left(v_{b\_ref}\geq 0\right)\\ 0 & \left(v_{b\_ref}<0\right)\end{cases}\quad k_5=\begin{cases}1 & \left(v_{b\_ref}-v_{c\_ref}\geq 0\right)\\ 0 & \left(v_{b\_ref}-v_{c\_ref}<0\right)\end{cases}$$
$$k_3=\begin{cases}1 & \left(v_{c\_ref}\geq 0\right)\\ 0 & \left(v_{c\_ref}<0\right)\end{cases}\quad k_6=\begin{cases}1 & \left(v_{a\_ref}-v_{c\_ref}\geq 0\right)\\ 0 & \left(v_{a\_ref}-v_{c\_ref}<0\right)\end{cases}, \tag{5.8}$$

where v_{a_ref}, v_{b_ref}, and v_{c_ref} are the reference vectors, normalized with V_{dc}. Then, a pointer (N) to the effective region in which the reference vector is calculated as

$$N=1+\sum_{i=1}^{6}k_i\cdot 2^{i-1}. \tag{5.9}$$

From equation (5.9), it can be known that the pointer (N) ranges from 1 to 64, but has only 24 different possible values which correspond to the 24 tetrahedrons. The selection of tetrahedron to the pointer (N) can be shown in Fig. 5.10.

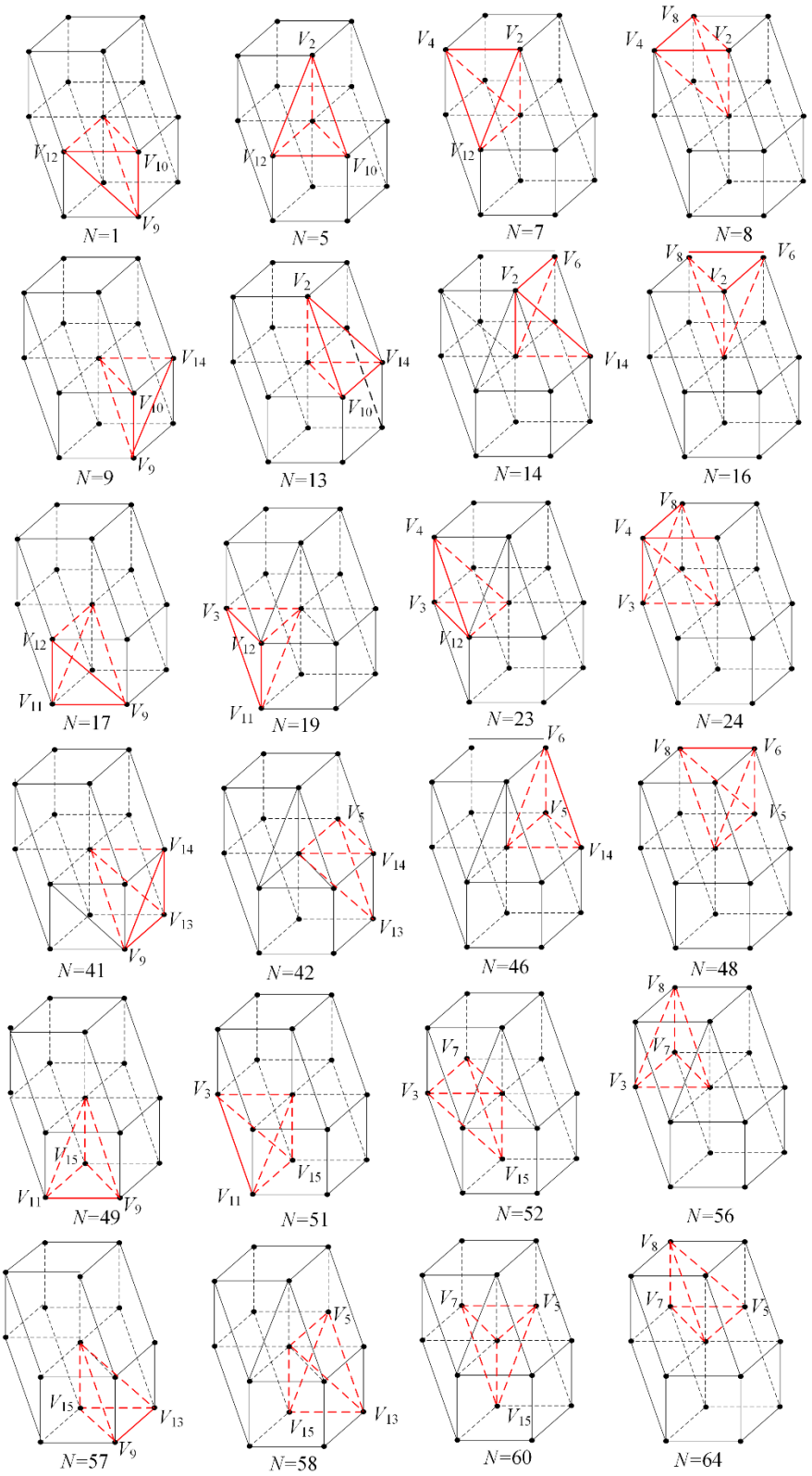


Figure 5.10: Tetrahedrons with respective to different pointer (*N*).

5.4.3 Calculation of Duty Cycles

Once the tetrahedron is chosen, the duty cycles for each vector in the tetrahedron that generate the equivalent reference voltage vector should be calculated. The relation between reference voltage vector and duty cycles can be easily derived as

$$u_{ref} = \begin{bmatrix} u_{aref} \\ u_{bref} \\ u_{cref} \end{bmatrix} = \begin{bmatrix} V_{d1a} & V_{d2a} & V_{d3a} \\ V_{d1b} & V_{d2b} & V_{d3b} \\ V_{d1c} & V_{d2c} & V_{d3c} \end{bmatrix} \cdot \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix}, \tag{5.10}$$

where u_{ref} is the reference voltage vector, d_1, d_2, and d_3 are the duty cycles, V_{d1}, V_{d2}, and V_{d3} are non-zero switching vectors, and their subscription *a*, *b*, and *c* indicate the projection values in *abc* domain.

From equation (5.7), the duty cycles can be expressed as

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} V_{d1a} & V_{d2a} & V_{d3a} \\ V_{d1b} & V_{d2b} & V_{d3b} \\ V_{d1c} & V_{d2c} & V_{d3c} \end{bmatrix}^{-1} \cdot u_{ref}, \tag{5.11}$$

and

$$d_0 = 1 - d_1 - d_2 - d_3, \tag{5.12}$$

where d_0 is the duty cycle of zero-vector (V_1 or V_{16}).

For example, when the value of N is 1, V_9(-1,-1,-1), V_{10}(-1,-1,0), and V_{12} (-1,0,0) are chosen, based on Table 5.2. According to equation (5.11), the duty cycles are expressed as

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} -1 & -1 & -1 \\ -1 & -1 & 0 \\ -1 & 0 & 0 \end{bmatrix}^{-1} \cdot u_{ref} = \begin{bmatrix} -u_{\text{cref}} \\ -u_{\text{bref}} + u_{\text{cref}} \\ -u_{\text{aref}} + u_{\text{bref}} \end{bmatrix}, \tag{5.13}$$

Similarly, the corresponding duty cycles d_1, d_2, and d_3 to different pointer N can be obtained as shown in Table 5.2.

Table 5.2: Summary of the Duty Cycle Calculation

N	V_{d1}	V_{d2}	V_{d3}	d_1	d_2	d_3
1	V_9	V_{10}	V_{12}	$-u_{cref}$	$-u_{bref}+u_{cref}$	$-u_{aref}+u_{bref}$
5	V_2	V_{10}	V_{12}	u_{cref}	$-u_{bref}$	$-u_{aref}+u_{bref}$
7	V_2	V_4	V_{12}	$-u_{bref}+u_{cref}$	u_{bref}	$-u_{aref}$
8	V_2	V_4	V_8	$-u_{bref}+u_{cref}$	$-u_{aref}+u_{bref}$	u_{aref}
9	V_9	V_{10}	V_{14}	$-u_{cref}$	$-u_{aref}+ u_{cref}$	$u_{aref}-u_{bref}$
13	V_2	V_{10}	V_{14}	u_{cref}	$-u_{aref}$	$u_{aref}-u_{bref}$
14	V_2	V_6	V_{14}	$-u_{aref}+u_{cref}$	u_{aref}	$-u_{bref}$
16	V_2	V_6	V_8	$-u_{aref}+u_{cref}$	$u_{aref}-u_{bref}$	u_{bref}
17	V_9	V_{11}	V_{12}	$- u_{bref}$	$u_{bref}-u_{cref}$	$-u_{aref}+u_{cref}$
19	V_3	V_{11}	V_{12}	u_{bref}	$- u_{cref}$	$-u_{aref}+u_{cref}$
23	V_3	V_4	V_{12}	$u_{bref}-u_{cref}$	u_{cref}	$-u_{aref}$
24	V_3	V_4	V_8	$u_{bref}-u_{cref}$	$-u_{aref}+u_{cref}$	u_{aref}
41	V_9	V_{13}	V_{14}	$-u_{aref}$	$u_{aref}-u_{cref}$	$-u_{bref}+u_{cref}$
42	V_5	V_{13}	V_{14}	u_{aref}	$-u_{cref}$	$-u_{bref}+u_{cref}$
46	V_5	V_6	V_{14}	$u_{aref}-u_{cref}$	u_{cref}	$-u_{bref}$
48	V_5	V_6	V_8	$u_{aref}-u_{cref}$	$-u_{bref}+u_{cref}$	u_{bref}
49	V_9	V_{11}	V_{15}	$-u_{bref}$	$-u_{aref}+u_{bref}$	$u_{aref}-u_{cref}$
51	V_3	V_{11}	V_{15}	u_{bref}	$-u_{aref}$	$u_{aref}-u_{cref}$
52	V_3	V_7	V_{15}	$-u_{aref}+u_{bref}$	u_{aref}	$-u_{cref}$
56	V_3	V_7	V_8	$-u_{aref}+u_{bref}$	$u_{aref}-u_{cref}$	u_{cref}
57	V_9	V_{13}	V_{15}	$-u_{aref}$	$u_{aref}-u_{bref}$	$u_{bref}-u_{cref}$
58	V_5	V_{13}	V_{15}	u_{aref}	$-u_{bref}$	$u_{bref}-u_{cref}$
60	V_5	V_7	V_{15}	$u_{aref}-u_{bref}$	u_{bref}	$-u_{cref}$
64	V_5	V_7	V_8	$u_{aref}-u_{bref}$	$u_{bref}-u_{cref}$	u_{cref}

5.4.4 Switching Sequence of the Selected Vectors

Once the duty cycles are calculated, the selected switching vectors should be placed in a sequence and optimized to reduce switching loss. In this chapter, two zero vectors are selected and the switching sequence is symmetric in each sampling period [80]. As an example, the sequence of vector for the case N = 1, is as shown in Fig. 5.11.

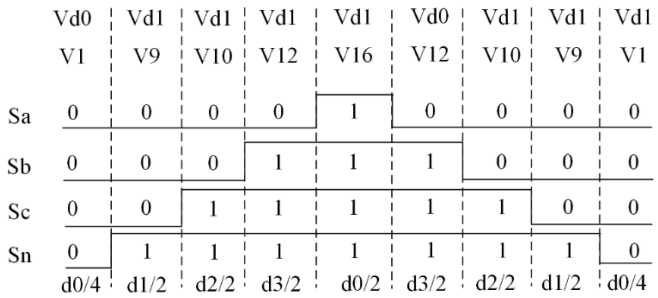


Figure 5.11: The switching sequence of the center symmetrical manner.

5.5 Simulation Study

This section provides the simulation verification of the ROGI based dual current loop control strategy for the stand-alone four-leg converter. The system parameters are provided in Table 5.3. The simulation is performed in MATLAB/Simulink. Load-on and load-off conditions are conducted to verify the dynamic performance of the control strategy.

Fig. 5.12 shows the simulation waveforms of the modulation signals. It can be noticed that the third harmonic signals are injected which helps to achieve the increased DC bus voltage utilization. Fig. 5.13 shows the waveforms of positive and negative sequence voltages in *dq* domain. It can be seen that positive sequence voltage are generated constantly, but the negative sequence voltage is regulated to be zero. The waveforms of DC bus voltage is shown in Fig. 5.14. From Fig. 5.14, it can be seen that at time t = 0.25s and t = 0.4s, only a variation of 2.2V is observed in the DC bus voltage. Fig. 5.15 shows output voltage and currents during load-on and load-off conditions. It can be seen that the output voltage u_{iabc} is regulated at 115V (RMS) constantly. At 0.4s, after loads are cut off, it takes 50ms for the output voltages to settle down. These results validate the good dynamic response and effectiveness of control strategies.

Table 5.3: Parameters of the Stand-alone Four-leg Converter

Parameters	Value
DC-link voltage V_{dc}	320 V
Output voltage u_{iabc}	115V (rms)
Output frequency	400 Hz
Switching frequency	50 kHz
Rated power	120 kVA

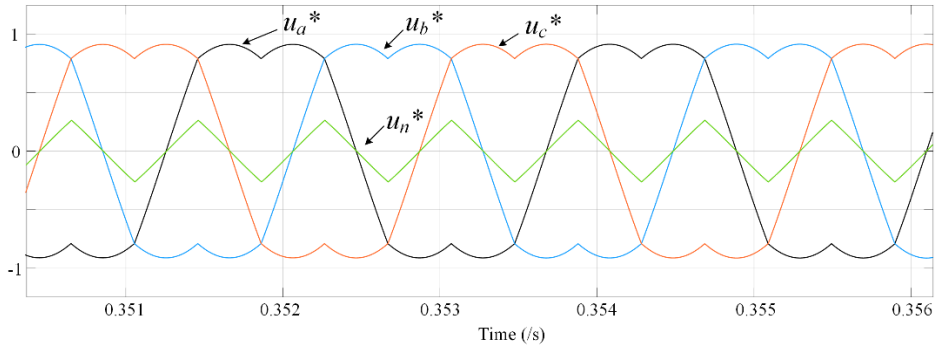


Figure 5.12: Simulation waveforms of the modulation signals.

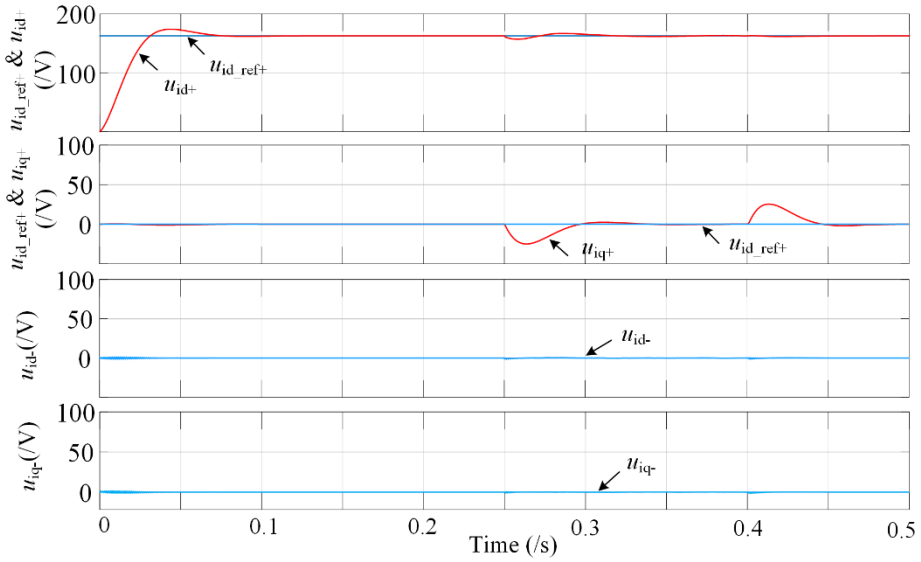


Figure 5.13: Simulation waveforms of positive and negative voltage in *dq* domain.

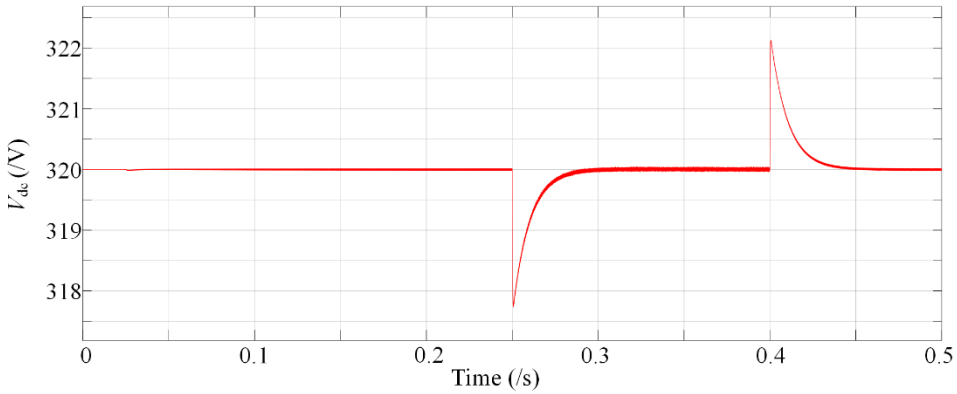


Figure 5.14: Simulation waveform of DC bus voltage (V_{dc}).

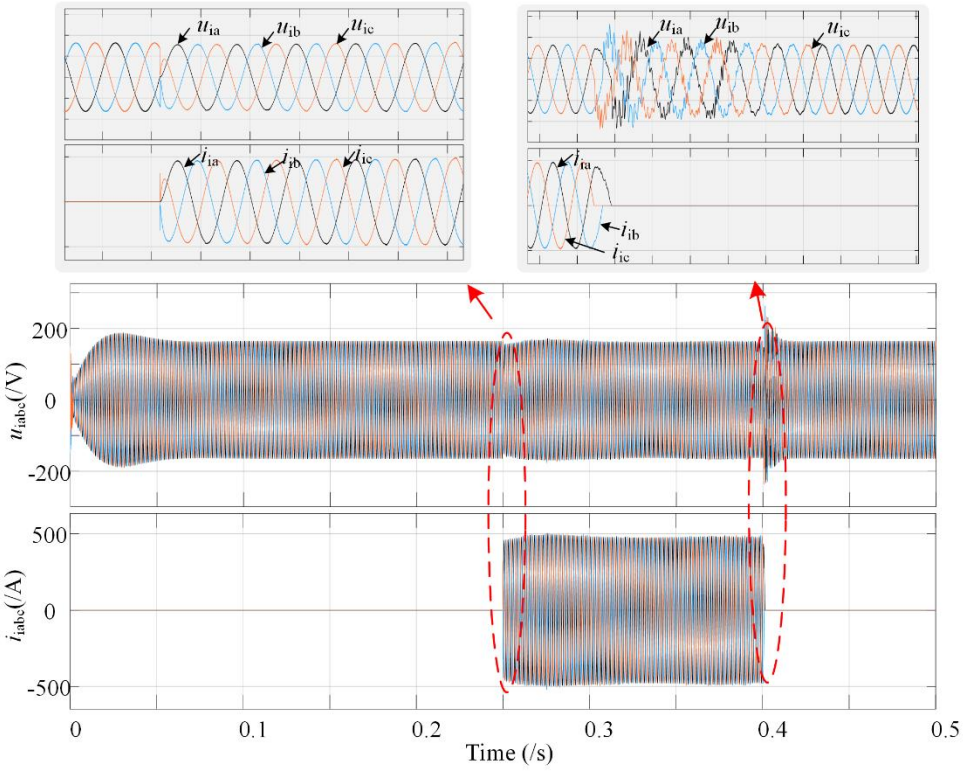


Figure 5.15: Simulation waveforms of output voltage and currents.

5.6 Conclusion

In this chapter, a ROGI based dual current loop control strategy is proposed for stand-alone four-leg converter operation used for aircraft electrical power generation system. The output voltages and currents of the converter are sensed and decomposed into positive and negative sequence components using ROGI. Furthermore, the detected positive and

negative sequence voltages are controlled in their respective d-q domain (positive sequence d-q co-ordinate rotates in counterclockwise and negative sequence d-q co-ordinate rotates in the clockwise direction). Finally, Three Dimensional Space Vector Pulse Width Modulation (3D-SVPWM) is implemented to drive the four-leg converter. As a result, only positive sequence voltage (400Hz, 115V rms) is generated by the converter and applied to the aircraft loads. For the dynamic response, only 50ms is required for the output voltages to settle down. The feasibility of the operation of the proposed control strategy is demonstrated by simulation using MATLAB/Simulink.

5.7 Publications

1. S. Jiao, R. K. Potti, K. Rajashekara, Y. Jia, "Induction Generator Based Electrical Power Generation System for More Electric Aircraft Applications," 2020 *AIAA Propulsion & Energy Forum*. (accepted)

Chapter 6

Conclusions and Future Work

This dissertation focuses on the control algorithms for a four-leg converter to improve power quality in a microgrid system with balanced and unbalanced loads. The work is further extended to develop novel control strategies for the operation of a standalone four-leg converter in More Electric Aircraft systems to achieve better power quality and response time.

6.1 Summary

An unbalanced currents detection technique using reduced order generalized integrator (ROGI) is presented for a four-leg converter whose DC bus is supported by an active power supply. The controller can effectively and accurately detect the positive and negative sequence components of load side currents based on the proposed ROGI technique. The simulation results show the satisfactory operation of the converter during transient and steady-state periods.

A control method named double reduced-order generalized integrator (DROGI) for shunt compensation of unbalanced loads using four-leg converter in a distributed system is proposed. One integrator is operated on load currents to obtain the reference compensation currents and the second one is used to decompose the converter currents. The reference rectification currents are generated using a PI controller to regulate the DC link voltage at its reference value. As a result, the compensation currents for improving

power quality and rectification currents for maintaining DC link voltage are decoupled and regulated separately. Also, to eliminate the impact of PLL, another novel control algorithm named grid voltage modulated direct power control (GVM-DPC) without PLL for the four-leg converter is proposed as well. The effectiveness of the proposed algorithms has been analyzed through a steady-state and dynamic response. This research highlights in detail the design of the proposed control algorithm for a four-leg converter for improving power quality problems in terms of load balancing, reduced neutral current and achieving unity power factor operation in a three-phase four-wire power system.

A novel ROGI-PLL based four-leg converter control algorithm for unbalanced nonlinear loads compensation, under both balanced grid and adverse grid conditions is proposed. In this approach, the phase angle and frequency of FFPSC from unbalanced distorted grid voltage are estimated accurately and rapidly by using ROGI as a pre-filter for PLL. This scheme enables to increase the open-loop bandwidth of PLL and improve the dynamic performance of synchronization. Furthermore, considering unbalanced nonlinear loads compensation, two additional ROGIs are utilized to generate the desired compensation and rectification currents. As a result, the AC source currents are balanced and in phase with the FFPSC of the grid voltage. Also, since the compensation mode (DC-AC) and rectification mode (AC-DC) of the four-leg converter are decoupled, more flexibility and selectivity in terms of control methods for the converter are achieved. The effectiveness of the proposed control strategy is verified through simulation and experimental results for a 1.1 kW rated system.

A ROGI based dual current loop control strategy is proposed for stand-alone four-leg converter operation used for aircraft electrical power generation system is proposed. The

output voltages and currents of the converter are sensed and decomposed into positive and negative sequence components using ROGI. Furthermore, the detected positive and negative sequence voltages are controlled in their respective d-q domain (positive sequence d-q co-ordinate rotates in counterclockwise and negative sequence d-q co-ordinate rotates in the clockwise direction). Finally, Three Dimensional Space Vector Pulse Width Modulation (3D-SVPWM) is implemented to drive the four-leg converter. As a result, only positive sequence voltage (400Hz, 115V RMS) is generated by the converter and applied to the aircraft loads. For the dynamic response, only 50ms are required for the output voltages to settle down. The feasibility of the operation of the proposed control strategy is demonstrated by simulation in MATLAB/Simulink.

6.2 Future Work

The work presented in this dissertation proposes separate methodologies to address each problem in microgrid control and operation. The solutions can be improved in the following aspects.

6.2.1 PCC Voltage Regulation Strategy under Adverse Grid Condition

The control strategy for the four-leg converter under an unbalanced distorted grid condition is proposed. However, the regulation of unbalanced grid voltage is not considered. Therefore, the PCC voltage regulation strategy by using the four-leg converter under adverse grid condition is to be investigated.

6.2.2 Novel Topology of the Four-leg Converter to Reduce the DC Capacitors

Reduced capacitors applied for the four-leg converter are to be investigated. The DC bus voltage of the converter is supported by the DC capacitors. However, the capacitance

is large which means the size of the capacitor is high. Thus, the topology of the four-leg converter to reduce the capacitance of the DC side capacitors needs to be developed.

6.2.3 Fault-tolerant Operation of the Four-leg Converter

The function of the four-leg converter in this research is to compensate unbalanced loads, reduce neutral current, and compensate reactive power and harmonics. But this thesis did not consider the fault operation of the converter. When the converter falls into fault operation, the PQ problems of the microgrid will be aggravated. So fault-tolerant operation of the four-leg converter should be investigated as well.

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