A VIDEO SCANNER

A Thesis

Presented to

the Faculty of the Department of Electrical Engineering

University of Houston

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

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Gary L. Hornbuckle

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ABSTRACT

A major problem encountered in adapting a digital computer to deal with the real world is that of providing the computer with sensory information. This paper describes a video scanner system for providing a computer with a rudimentary sense of sight.

The video scanner described hereby uses a closed circuit television system to generate an electronic analog of a real world scene and then directly transforms this analog into a matrix of binary numbers which represent the light intensities at discrete points in the scene.

A particular advantage of this direct transformation is that no special preparation of the visual information is necessary. The system is capable of transforming literally any image which can be received by the television camera.

Possible applications for the system include input for scene analysis, object identification and optical measurement.

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CHAPTER I

INTRODUCTION

The problem of converting real world visual information into a form suitable for computer analysis has been approached from many angles. The work which has been done in low bandwidth acquisition has been limited to techniques which require special preparation of the image (i.e., "flying spot" scanners). This paper describes an experimental system for converting static images using a closed circuit television camera, a simple analog to digital conversion system, and a small scale digital computer. The technique used provides reasonably fast (2 - 3 seconds) acquisition time and does not require any special preparation of the image. Although the system described was built for a specific set of equipment, the general technique is adaptable to a variety of such equipment.

The basic suppositions of the technique are that the real world image is static and that the image transformation system (the closed circuit television and the digitizer) are sufficiently stable to allow multiple scans of the image in order to gather the required information without serious distortion. When these two qualifications are met, the inherent information storage properties of a static image can be exploited. The conversion system then becomes a low bandwidth transformer between the real world memory (the image) and the computer memory. The bulk of this paper is devoted to an example of the application of this multiple pass technique for image transformation and acquisition.

CHAPTER OUTLINES

Chapter II describes the characteristics of the specific computer used in the experimental system.

Chapter III is a detailed discussion of the general purpose interface which was constructed between the scanner and the computer.

Chapter IV is a functional description of the television system in relation to the scanner.

Chapter V is a description of the input and output control section of the scanner.

Chapter VI is a description of the scanner circuitry and its operation.

Chapter VII is a description of a device for retransforming the stored digital image to a real world image.

Chapter VIII is a description of the computer software package which was written for initial testing of the image transformation system.

CHAPTER II

DESCRIPTION OF THE SDS MODEL 92 COMPUTER INPUT/OUTPUT OPERATIONS

In its present implementation, the video scanner is interfaced to a Scientific Data Systems Model 92 digital computer. For brevity, this machine will be referred to as the SDS92. Detailed discussion of the SDS92 will be limited to the data input and output sections.

GENERAL DESCRIPTION

The SDS92 is a general purpose digital computer of the classical von Neumann type. It consists of a central control unit (CCU), an arithmetic and logic unit (ALU), a memory unit (MU), and an input/output controller (IOC). Data and instructions are stored in and share the MU and are operated on by the ALU and IOC under the direction of the CCU. The combination of the CCU,ALU,MU, and IOC is reffered to as the central processing unit (CPU).

INFORMATION STORAGE

The basic unit of information storage in the SDS92 is a 12 bit binary group called a word. A data word consists of an unscaled 12 bit binary number in two's complement form. The most significant bit (MSB) is reserved as a sign bit where a zero in the MSB indicates a positive number and a one indicates a negative number.Figure 1 illustrates the organization of the data word.

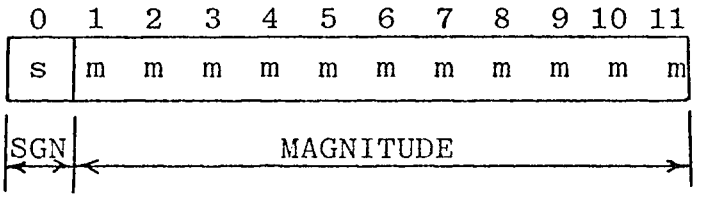


FIGURE 1

An instruction consists of one or two words of storage. The first word always contains a six bit operation field or op code, a three bit address mode field, and a three bit address value field. Certain address modes may logically extend the address value field to a second, adjacent word. Figure 2 illustrates the organization of an instruction.

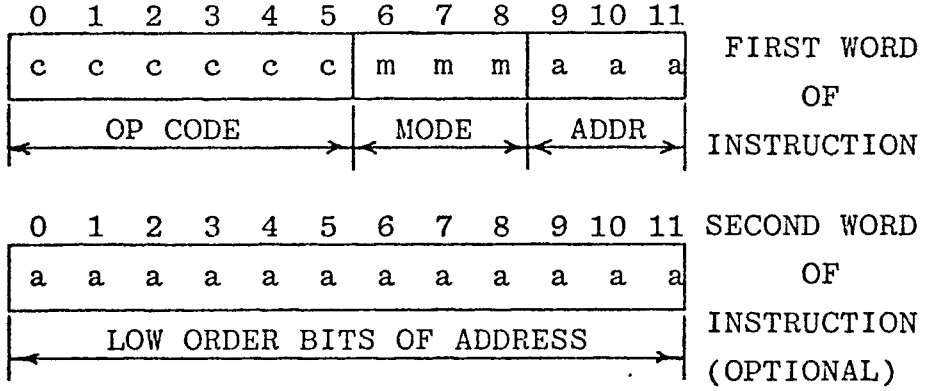


FIGURE 2

When an address value is extended to a second word, the three address value bits in the first word of the instruction are the most significant and the 12 bits of the second word are the least significant. See the SDS92 Computer Reference Manual[1] for further details on addressing facilities, arithmetic and logical instructions.

ENERGIZE OUTPUT M INSTRUCTION

An external device is connected to the IOC data bus in the SDS92 by the Energize Output M (EOM) instruction. The EOM is a two word instruction the general form of which is shown in Figure 3.

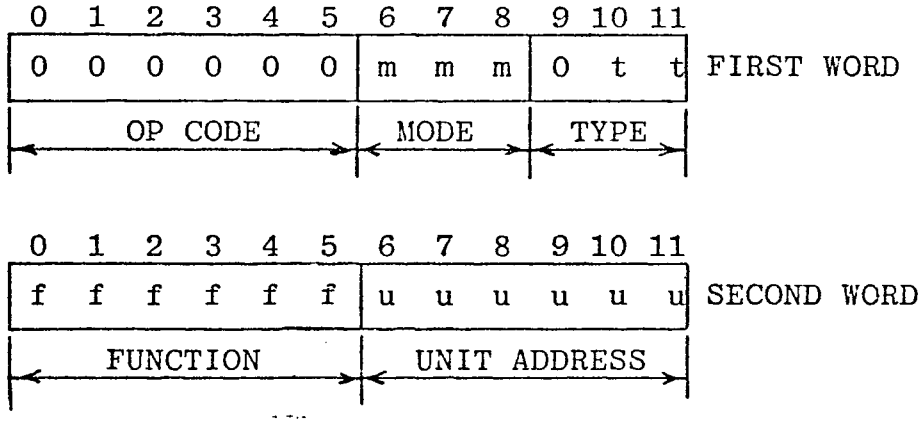
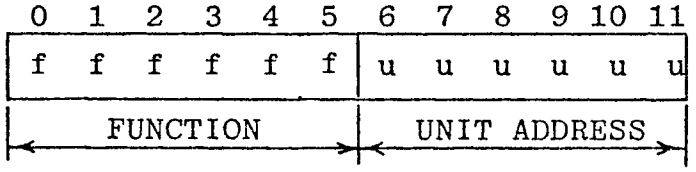


FIGURE 3

The EOM operates in one of four different modes according to the type of operation to be performed. The type of operation is determined by the setting of bits 10 and 11 in the first word of the instruction. The type of operation is determined according to the following scheme:

BIT 10	BIT 11	TYPE OF OPERATION
0	0	Buffer Control
0	1	Input/Output
1	0	Internal
1	1	System

Two of these types, the Internal and Input/Output, are of particular use with the video scanner system. The Internal type is used in a special situation which will be explained in Chapter IIIof this paper. The Input/Output type is used to actually connect the external device to the IOC and pass an input/output function code . The Input/Output type EOM utilizes the second instruction word in the following format:



BIT	USE
0- 5	Control function code peculiar to device
6-11	Unit (device) address code

The only information that an EOM can pass to a device is the five bit control function code in bits 0-5 of the second word of the EOM. An EOM must be issued to a device prior to any attempt to transfer data to or from the device.

INPUT/OUTPUT INSTRUCTIONS

There are four input/output instructions which are used by the video scanner system. Parallel Output (POT) and Parallel Input (PIN) cause any word in th MU to be presented in parallel at a connector; or , inversely, cause signals sent to a connector to be stored in any MU location. The execution of a POT or PIN causes a signal to be sent to the

device involved in the input or output operation.

PARALLEL INPUT INSTRUCTION

During a PIN, the signal from the IOC tells the device to send its data word as soon as it is ready. When the device is prepared to transfer the data word, the device transmits a Ready signal to the IOC while at the same time presenting its data word. The IOC places the received data word into the specified MU location. The CPU is placed in a wait state during a PIN operation and no other instruction may be executed during a PIN operation.

PARALLEL OUTPUT INSTRUCTION

During the execution of a POT instruction, the IOC transmits a signal to the external device to allert it to receive a data word. When the device is prepared to receive the data word, it transmits a Ready signal to the IOC which then releases the data word to the device. The CPU is placed in a wait state during a POT operation and no other instruction may be executed during a POT operation.

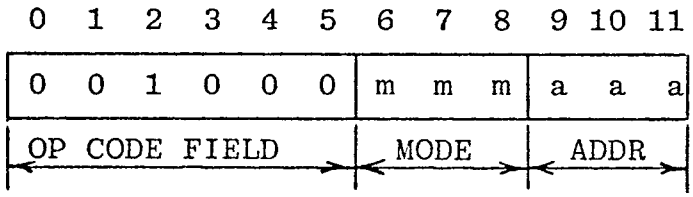
BLOCK PARALLEL INPUT AND BLOCK PARALLEL OUTPUT

PIN and POT can transfer only one word of data per execution. The inefficiency of this type of operation for transfering large blocks of sequential MU locations is alleviated by the Block Parallel Input (BPI) and Block Parallel Output (BPO) instructions. BPI and BPO operate in the same manner as the PIN and POT instructions but can transfer from 1 to 4096 words per execution.

Table 1 gives specific formats and details about the POT, BPO, PIN, and BPI instructions.

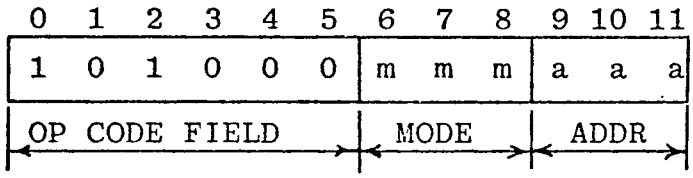
TABLE 1

POT (PARALLEL OUTPUT)



POT transfers the contents of the specified MU location in parallel to a device. Instruction time is 5 microseconds plus the wait for Ready.

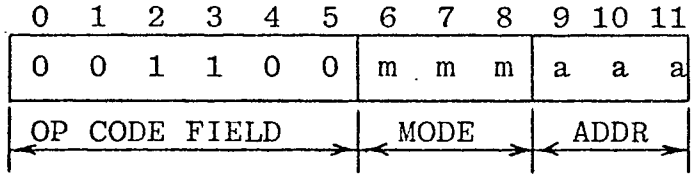
BPO (BLOCK PARALLEL OUTPUT)



Starting with the specified MU location, BPO transfers the contents of N sequential MU locations in parallel to the device. The word count ,N, minus one is placed in CPU register A previous to execution of the BPO. BPO can transfer up to 4096 words per execution. Instruction time is 5.25 microseconds plus N times 1.75 microseconds plus N-1 times the wait for Ready between each word transfer.

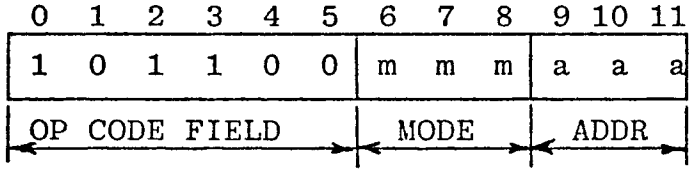
TABLE 1, continued

PIN (PARALLEL INPUT)



PIN stores the contents of the 12 input lines in parallel at the specified MU location. Instruction time is 8.75 microseconds plus the wait for Ready.

BPI (BLOCK PARALLEL INPUT)



Starting with the specified MU location, BPI transfers N words from the 12 input data lines in parallel into sequential MU locations. The word count ,N, minus one is placed in CPU register A previous to execution of the BPI. BPI can input up to 4096 words per execution. Instruction time is 5 microseconds plus N times 1.75 microseconds plus N-1 times the wait for Ready between each transfer.

Details of the input/output signals and timing are presented in Chapter III along with a description of the general purpose input/output interface which was constructed for the video scanner system.

CHAPTER III
THE GENERAL PURPOSE INPUT/OUTPUT INTERFACE

The general purpose input/output interface was designed to provide a quick and easy way of connecting the video scanner system and up to six other devices to the SDS92 data and control lines. The interface consists of the following:

1. A set of cables which connect the SDS92 to the interface chassis.

2. A set of SDS type NX50 line receivers which provide proper termination of the lines driven by the SDS92 and conversion to logic levels suitable for use with standard transistor-transistor logic (TTL) integrated circuits.

3. An input data bus with pullup resistors suitable for driving the data input and control lines going to the SDS92 with TTL open collector devices.

4. A unit address decoder designed to decode up to eight device addresses with the required buss timing.

5. A set of prewired device connector slots in the interface chassis.

In addition to the normal complement of data and control lines, the general purpose interface includes provisions for use of the POT/PIN Extender. The POT/PIN Extender is a

special device installed in the SDS92 which allows up to 24 bits of data to be transferred to or from an external device in parallel.

INTERFACE CABLES

Three cables are required to connect the SDS92 to the interface chassis. One cable contains the POT data buss and its associated timing signals, another cable contains the PIN data buss and its associated timing signals, and the third cable contains the priority interrupt lines.

The POT cable is an SDS type EZ51. The cable is terminated on each end by a printed circuit connector board. The connector board designated as P01 plugs into the interface chassis at slot 23 and the connector board designated as P02 plugs into the SDS92 mainframe at slot 28L. Table 2 gives the pin connections for the POT cable and a brief description of each signal line.

TABLE 2 POT CABLE CONNECTIONS

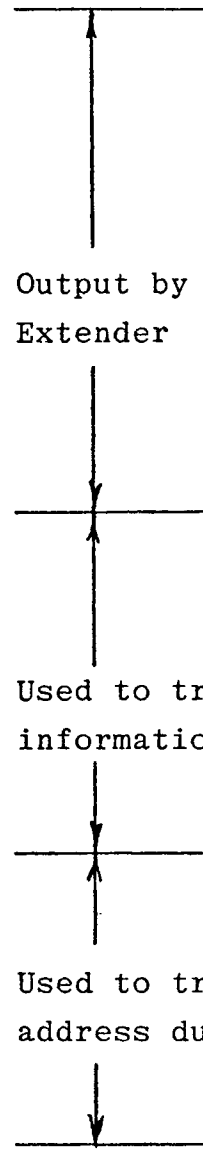
Pin	Signal	Description
1	POT1	A signal from the computer indicating that the POT instruction is in a wait phase.
2	POT2	A strobe signal generated during the wait phase of the POT instruction.
3	IOC	A signal generated for each EOM instruction in the Input/Output mode.
4	BUC	A signal generated for each EOM instruction in the Buffer Control mode.
5	SYS	A signal generated for each EOM instruction in the System Control mode.
6	EOM	A signal generated for each EOM instruction.

TABLE 2, continued

Pin	Signal	Description
7	Q1	A timing signal supplied for external use.
8	Q2	A timing signal supplied for external use.
9	RTF-	A ready signal supplied by external units on POT/BPO instructions to initiate data transfer.A zero volt level initiates the transfer.
10	RTI-	A signal from the computer to external units indicating that a PIN instruction has terminated.
11	BT-	A signal supplied by external units to terminate BPO and BPI instructions. A zero volt level on this line will cause the computer to halt block transfers and proceed with the program.
12	Q2	Same as pin 8.
13	SKSS	A signal generated for each SES instruction.
14	SIO-	A response signal generated by external devices interrogated by an I/O unit test SES instruction.A zero volt condition on this line will cause the flag flip flop to be set.
15	SSC-	A response signal from external devices interrogated by an SES instruction, System mode. A zero volt condition on this line will cause the flag flip flop to be set.
16	RT-	A ready signal supplied by external units on POT/BPO instructions to initiate data transfer. The transfer is initiated when this line is at a zero volt level.
17	ST	A signal derived from the manual start button on the computer control panel and can be used as a manual reset .

TABLE 2, continued

Pin	Signal	Description
18	C17	
19	unused	
20	C0	Output data MSB
21	C1	" " 2SB
22	C2	" " 3SB
23	C3	" " 4SB
24	C4	" " 5SB
25	C5	" " 6SB
26	C6	" " 7SB
27	C7	" " 8SB
28	C8	" " 9SB
29	C9	" " 10SB
30	C10	" " 11SB
31	C11	" " 12SB
32	C12	" " 13SB
33	C13	" " 14SB
34	C14	" " 15SB
35	C15	" " 16SB
36	C16	" " 17SB
37	C17	" " 18SB
38	C18	" " 19SB
39	C19	" " 20SB
40	C20	" " 21SB
41	C21	" " 22SB
42	C22	" " 23SB
43	C23	" " LSB



The PIN cable is an SDS type EZ52. The cable is terminated on each end by a printed circuit connector card. The connector card designated as P01 plugs into the interface chassis at slot 19 and the connector card designated as P02 plugs into the SDS92 mainframe at slot 31L. Table 3 gives the pin connections for the PIN cable and a brief description of each signal.

TABLE 3 PIN CABLE CONNECTIONS

Pin	Signal	Description
1	PIN	A strobe signal generated each cycle during the PIN instruction.
2	unused	
3	SIO-	A response signal from external devices interrogated by an I/O test SES instruction. A zero volt signal on this line will cause the flag flip flop to be set.
4-7	unused	
8	RTI-	A signal from the computer to external units indicating that a PIN/BPI instruction has terminated.
9	RTF-	A ready signal supplied by the external unit on PIN/BPI instructions to initiate data transfer. A zero volt level on this line initiates the transfer.
10-12	unused	
13	SKSS-	A strobe signal generated for each SES instruction.
14	unused	
15	SSC-	A response signal from external units interrogated by an SES instruction, System mode. A zero volt condition on this line will cause the flag flip flop to be set.

TABLE 3, continued

Pin	Signal	Description
16	RT-	A ready signal supplied by the external unit on PIN/BPI instructions to initiate data transfer. A zero volt level initiates the transfer.
17	unused	
18	BT-	A signal supplied by external units to terminate BPO and BPI instructions. A zero volt level on this line will cause the computer to halt block transfers and proceed with the program.
19	unused	
20	CD0-	Input data MSB
21	CD1-	" " 2SB
22	CD2-	" " 3SB
23	CD3-	" " 4SB
24	CD4-	" " 5SB
25	CD5-	" " 6SB
26	CD6-	" " 7SB
27	CD7-	" " 8SB
28	CD8-	" " 9SB
29	CD9-	" " 10SB
30	CD10-	" " 11SB
31	CD11-	" " 12SB
32	CD12-	" " 13SB
33	CD13-	" " 14SB
34	CD14-	" " 15SB
35	CD15-	" " 16SB
36	CD16-	" " 17SB
37	CD17-	" " 18SB

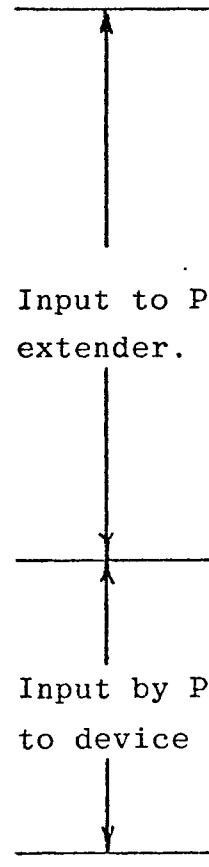


TABLE 3, continued

Pin	Signal	Description	
38	CD18-	Input data 19SB	
39	CD19-	" " 20SB	
40	CD20-	" " 21SB	Input by PIN instruction
41	CD21-	" " 22SB	to device
42	CD22-	" " 23SB	
43	CD23-	" " LSB	

The priority interrupt cable is an SDS type E69. The cable is terminated on each end by a printed circuit connector card. The connector card designated as P01 plugs into the interface chassis at slot 25 and the connector card designated as P02 plugs into the SDS92 mainframe at slot 44N. Table 4 gives the pin connections for the interrupt cable and a brief description of the interrupt signal characteristics.

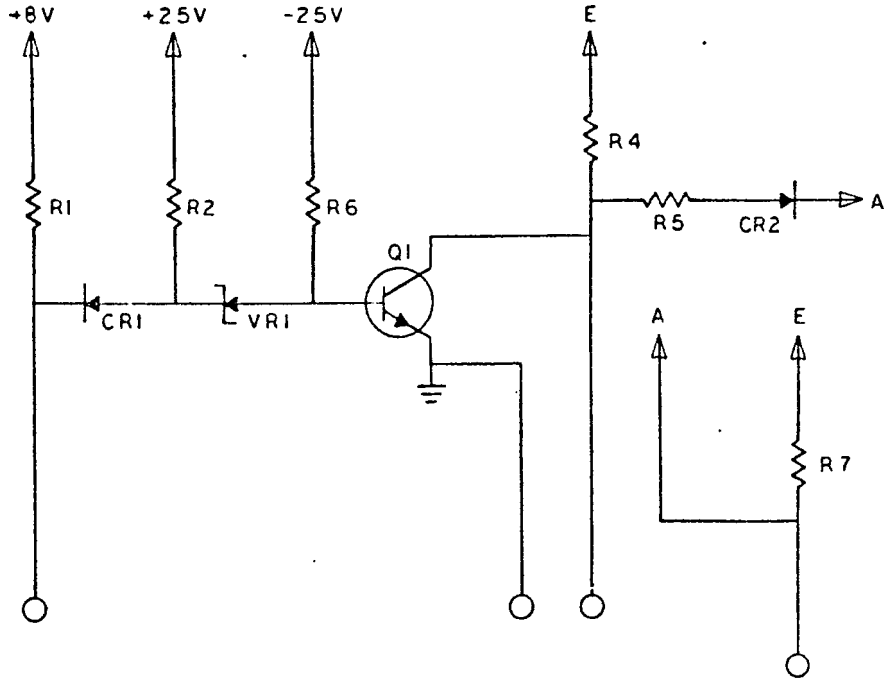
TABLE 4 INTERRUPT CABLE CONNECTIONS

Pin	Signal	Description
1-4	unused	
5	I5	I5 interrupt request
6	I6	I6 interrupt request Minimum duration: 5.25 microseconds Maximum duration: must be false before the computer resets the interrupt request flip flop.

LINE RECEIVERS

The line receivers used in the general purpose interface are SDS type NX50. The NX50 is a printed circuit assembly consisting of 17 inverting circuits which serve as long cable terminators and as converters from the +8 volt SDS buss levels to +4 volt levels suitable for use with TTL devices. Each input has a resistor connected to +8 volts so that if the cable driver or the cable is disconnected, the inverter input will be maintained at +8 volts. Sixteen of the circuits are arranged in pairs with a common "return" point which can be connected to circuit ground for noise abatement. Figure 4 is a schematic diagram of one inverter element. The NX50 inverters have a typical propagation delay of 60 nanoseconds and can drive up to 36 milliamps or 22 standard TTL unit loads.

FIGURE 4 ' NX50 INVERTER ELEMENT



The pin connections for the NX50 are given by Table 5. The three NX50 cards in the interface chassis occupy slots 20,21, and 22. A wire list of the received signals is presented in Appendix C of this paper.

TABLE 5 NX50 PIN CONNECTIONS

Pin	Signal	Description
1	CON	Ground this pin for 0 to +4 volt TTL compatible output.Leave open for 0 to +8 volt SDS compatible output.
2	IN2	Input circuit 2.
3	IN1	Input circuit 1.
4	OT1	Output circuit 1.
5	CM1-2	Common return circuits 1 and 2.
6	OT2	Output circuit 2.
7	OT3	Output circuit 3.
8	CM2-3	Common return circuits 2 and 3.
9	OT4	Output circuit 4.
10	IN4	Input circuit 4.
11	IN3	Input circuit 3.
12	IN6	Input circuit 6.
13	IN5	Input circuit 5.
14	OT5	Output circuit 5.
15	CM5-6	Common return circuits 5 and 6.
16	OT6	Output circuit 6.
17	OT7	Output circuit 7.
18	CM7-8	Common return circuits 7 and 8.
19	OT8	Output circuit 8.
20	IN8	Input circuit 8.
21	IN7	Input circuit 7.
22	IN10	Input circuit 10.

TABLE 5, continued

Pin	Signal	Description
23	IN9	Input circuit 9.
24	OT9	Output circuit 9.
25	CM9-10	Common return circuits 9 and 10.
26	OT10	Output circuit 10.
27	OT11	Output circuit 11.
28	CM11-12	Commom return circuits 11 and 12.
29	OT12	Output circuit 12.
30	IN12	Input circuit 12.
31	IN11	Input circuit 11.
32	IN14	Input circuit 14.
33	IN13	Input circuit 13.
34	OT13	Output circuit 13.
35	CM13-14	Common return circuits 13 and 14.
36	OT14	Output circuit 14.
37	OT15	Output circuit 15.
38	CM15-16	Common return circuits 15 and 16.
39	OT16	Output circuit 16.
40	IN16	Input circuit 16.
41	IN15	Input circuit 15.
42	IN17	Input circuit 17.
43	OT17	Output circuit 17.
44	CM17	Return circuit 17.
45	P8	+8 volt power.
46	M25	-25 volt power.
47	P25	+25 volt power.

INPUT DATA BUSS

A data and command buss with pullup resistors is provided for input to the SDS92. The buss operates at SDS

logic levels of 0 to +8 volts and each input lines requires 6 milliamps of current sink drive at 0 to +2 volts for a logic zero and 100 microamps at +6 to +8 volts for a logic one.

The pullup resistors on this buss were chosen according to manufacturers recommended data for open collector TTL.[2] The worst case design formulas for open collector TTL pullup resistors as provided by the manufacturer are:

$$Rp(max) = \frac{Vcc - Voh(min)}{N \times Ioh + Iih}$$

$$Rp(min) = \frac{Vcc - Vol(max)}{Iol - Iil}$$

where ,

Rp(max) = maximum allowable value of pullup resistor
Rp(min) = minimum allowable value of pullup resistor
Vcc = power supply voltage
Voh(min)= minimum voltage required by the load for a high state
Vol(max)= maximum voltage required by the load for a low state
Iih = current required by the load when load input is at a high state
Iil = current required by the load when load input is at a low state
Ioh = current drained by an open collector gate with its output high
Iol = current sink capability of open collector gate with its output low
N = number of open collector gates tied to buss

The worst case formulas were applied for an open collector driver of the SN7438[2] type being received by an SDS type NX50 in the SDS92 mainframe. For such a situation, the design parameters are:

Vcc = +8.0 volts
Voh(min) = +6.0 volts
Vol(max) = +2.0 volts
Iih = 100 microamps or 0.1 milliamps
Iil = 6 milliamps
Ioh = 250 microamps or 0.25 milliamps
Iol = 30 milliamps

In order to allow for expansion of the interface, two cases of drive requirements were considered. The first case is where only one SN7438 is tied to the buss. For this case N = 1 and the design formulas yield:

$$Rp(max) = \frac{8.0 - 6.0}{1 \times 2.5 \times 10^{-4} + 1 \times 10^{-4}} \simeq 5700\ \Omega$$

$$Rp(min) = \frac{8.0 - 2.0}{3.0 \times 10^{-2} - 6.0 \times 10^{-3}} \simeq 250\ \Omega$$

so choose $250 < Rp < 5700\ \Omega$.

The second case is where up to four SN7438 drivers may be connected to the buss. For this case N = 4 and the design formulas yield:

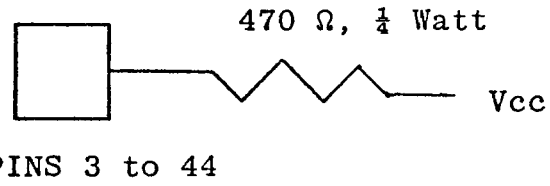
$$Rp(max) = \frac{8.0 - 6.0}{4 \times 2.5 \times 10^{-4} + 1.0 \times 10^{-4}} \simeq 1800\ \Omega$$

and Rp(min) = 250Ω as in case 1, so choose

$$250\Omega < Rp < 1800\ \Omega\ .$$

For both cases, the most restrictive requirements are those of the second case. Accordingly, pullup resistors of 470 Ω were chosen as meeting the design requirements for both cases. The pullup resistors are mounted on a printed circuit card which plugs into slot 18 of the interface chassis. Figure 5 is a diagram of the buss pullup card.

FIGURE 5 DIAGRAM OF THE BUSS PULLUP CARD



UNIT ADDRESS DECODER

The unit address decoder was constructed to provide the devices connected to the interface with properly timed input/output initiation signals. The first task in designing the decoder was to select the unit addresses to be used. It was decided to provide at least three input ports and three

output ports in addition to the one input port and one output port to be used by the scanner system. It was also decided that the addresses chosen for the interface would not conflict with those already chosen by the computer manufacturer for the input/output offered for the SDS92. These requirements led to the selection of the unit address codes given in Table 6.

TABLE 6

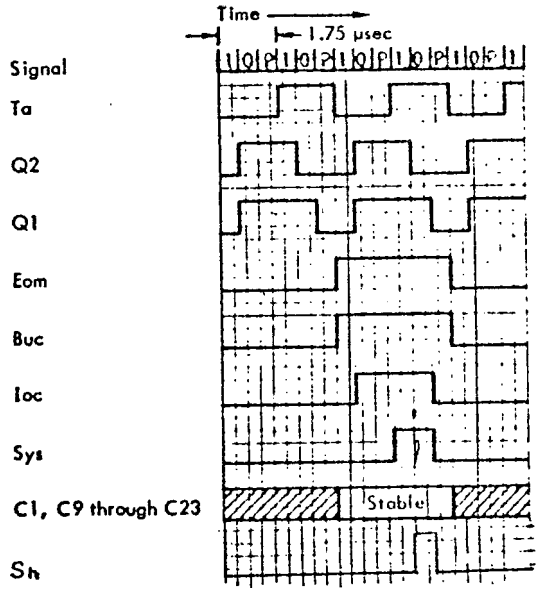
UNIT ADDRESS AND SLOT ASSIGNMENT

Address (octal)	Slot	Device
20	9	Video scanner system input
21	10	Video scanner system output
22	11	General purpose input 1
23	12	General purpose output 1
24	13	General purpose input 2
25	14	General purpose output 2
62	15	General purpose input 3
63	16	General purpose output 3

EOM INTERFACE SIGNALS AND TIMING

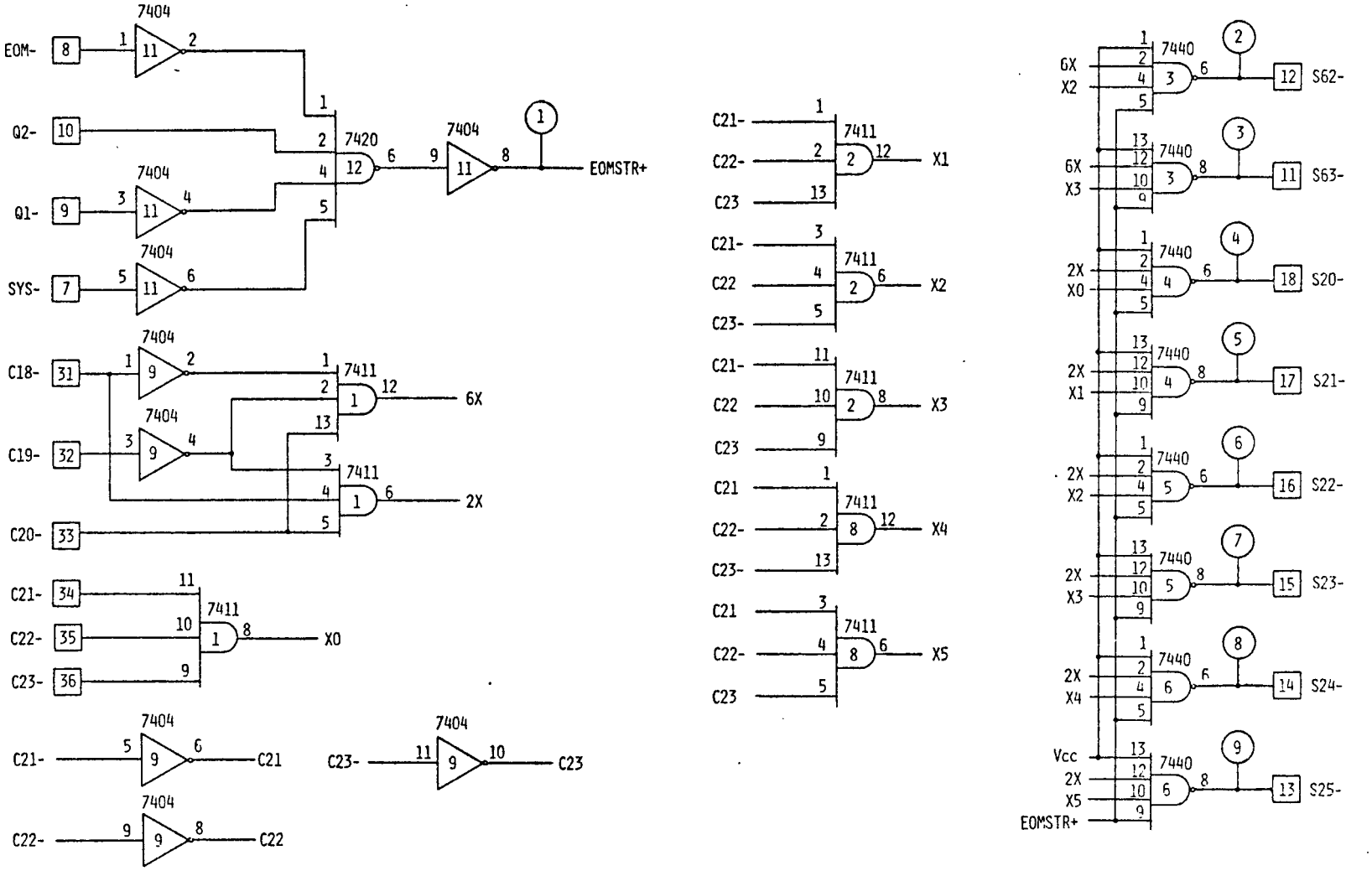
The unit address decoder uses the interface signals EOM, Q2, Q1, and SYS to pick the unit address off output data lines C18 to C23 and send a strobe stobe signal, Sn , to the selected device. Figure 6 is a diagram of the EOM instruction signal timing.

FIGURE 6 EOM INSTRUCTION SIGNAL TIMING



DECODER CIRCUITRY

Figure 7 is a diagram of a circuit designed to perform the required decode function. Referring to Figure 7, it can be seen that the EOM-, Q1-, and SYS- signals are inverted and applied to the four input NAND gate at location 12. The Q2- signal is also applied to the NAND at 12, resulting in a pulse whenever the condition EOM(Q2-)Q1(SYS) is met. This pulse is inverted and becomes EOMSTR, which is then applied as a gate signal to the final decoder section composed of NAND gates located at 3, 4, 5, and 6. The circuit composed of the inverters at location 9 and the three input AND gates



DEVICE DECODER
Figure 7

at location 1 decodes the first digit of the octal address from data lines C18-, C19-, and C20- and produces outputs 2X and 6X. The least significant digit of the octal address is on data lines C21-, C22-, and C23- and is decoded by the AND gates at locations 1, 2, and 8 and inverters at location 9. These circuits produce the terms X0, X1, X2, X3, X4, and X5.

The outputs of the first and second digit decoders are applied to the final decoder section at locations 3, 4, 5, and 6 to produce the individual device address pulses S62-, S63-, S20-, S21-, S22-, S23-, S24-, and S25- whenenever the gate signal , EOMSTR, is high. The representative pulse for the individual address pulses, Sn , is shown in Figure 6.

The unit address decoder is constructed on a printed circuit card which plugs into slot 17 of the interface chassis. Table 7 is a pin listing for the device decoder card.

TABLE 7 PIN LISTING FOR DEVICE DECODER CARD

Pin	Signal	Description
1,2	Vcc	+5 volt power
3-6	not used	
7	SYS-	SYS from SDS92 after inversion by NX50
8	EOM-	EOM from SDS92 after inversion by NX50
9	Q1-	Q1 from SDS92 after inversion by NX50
10	Q2-	Q2 from SDS92 after inversion by NX50
11	S63-	Device select pulse address 63_8
12	S62-	" " " " 62_8
13	S25-	" " " " 25_8
14	S24-	" " " " 24_8
15	S23-	" " " " 23_8
16	S22-	" " " " 22_8
17	S21-	" " " " 21_8

TABLE 7, continued

Pin	Signal	Description
18	S20-	Device select pulse address 20_8
19-30	unused	
31	C18-	Output data line C18 after inversion
32	C19-	" " " C19 " "
33	C20-	" " " C20 " "
34	C21-	" " " C21 " "
35	C22-	" " " C22 " "
36	C23-	" " " C23 " "
37-44	unused	
45,46	GND	Ground return

PREWIRED DEVICE CONNECTORS

A set of prewired device connectors is provided in the interface chassis. These connectors were included to provide an easy means of connecting additional devices to the general purpose interface. Six of the slots are for general purpose inputs and outputs 1, 2, and 3 and one set of slots is reserved for the video scanner system. The slot assignments and addresses for the connectors are given in Table 6. Table 8 is a pin listing for the output units 63_8, 25_8, and 23_8.

TABLE 8

PIN LISTING FOR OUTPUT UNITS 63_8, 25_8, AND 23_8

Pin	Signal	Description
1,2	Vcc	+5 volt power
3	POT1-	POT1 from SDS92 after inversion by NX50
4	POT2-	POT2 " " " " " "
5	IOC-	IOC " " " " " "
6	BUC-	BUC " " " " " "
7	SYS-	SYS " " " " " "
8	EOM-	EOM " " " " " "
9	Q1-	Q1 " " " " " "
10	Q2-	Q2 " " " " " "
11	RTI	RTI- " " " " " "
12	ST-	ST " " " " " "
13	C0-	C0 " " " " " "
14	C1-	C1 " " " " " "
15	C2-	C2 " " " " " "
16	C3-	C3 " " " " " "
17	C4-	C4 " " " " " "
18	C5-	C5 " " " " " "
19	C6-	C6 " " " " " "
20	C7-	C7 " " " " " "
21	C8-	C8 " " " " " "
22	C9-	C9 " " " " " "
23	C10-	C10 " " " " " "
24	C11-	C11 " " " " " "
25	C12-	C12 " " " " " "
26	C13-	C13 " " " " " "
27	C14-	C14 " " " " " "
28	C15-	C15 " " " " " "
29	C16-	C16 " " " " " "
30	C17-	C17 " " " " " "

TABLE 8, continued

Pin	Signal	Description
31	C18-	C18 from SDS92 after inversion by NX50
32	C19-	C19 " " " " " "
33	C20-	C20 " " " " " "
34	C21-	C21 " " " " " "
35	C22-	C22 " " " " " "
36	C23-	C23 " " " " " "
37	SKSS-	SKSS " " " " " "
38	SIO-	Response signal to I/O unit test SES
39	RTF-	High speed ready
40	BT-	Block output terminate
41	RT-	Low speed ready
42	I5	I5 interrupt
43	I6	I6 interrupt
44	Sn-	Select pulse unit n (63_8, 25_8, 23_8)
45,46	GND	Ground return

Table 9 is a pin listing for the general purpose input units 62_8, 24_8, and 22_8.

TABLE 9

PIN LISTING FOR INPUT UNITS 62_8, 24_8, AND 22_8

Pin	Signal	Description
1,2	Vcc	+5 volt power
3	PIN-	PIN from SDS92 after inversion by NX50
4	unused	
5	C12-	C12 from SDS92 after inversion by NX50. Brought to input device to pass function codes with EOM instructions.
6	C13-	C13 from SDS92 after inversion by NX50
7	C14-	C14 " " " " " "

TABLE 9, continued

Pin	Signal	Description
8	C15-	C15 from SDS92 after inversion by NX50
9	C16-	C16 " " " " " "
10	C17-	C17 " " " " " "
11	RTI	RTI- " " " " " "
12	ST-	ST " " " " " "
13	CD0-	Input data buss to SDS92 MSB
14	CD1-	" " " " " 2SB
15	CD2-	" " " " " 3SB
16	CD3-	" " " " " 4SB
17	CD4-	" " " " " 5SB
18	CD5-	" " " " " 6SB
19	CD6-	" " " " " 7SB
20	CD7-	" " " " " 8SB
21	CD8-	" " " " " 9SB
22	CD9-	" " " " " 10SB
23	CD10-	" " " " " 11SB
24	CD11-	" " " " " 12SB
25	CD12-	" " " " " 13SB
26	CD13-	" " " " " 14SB
27	CD14-	" " " " " 15SB
28	CD15-	" " " " " 16SB
29	CD16-	" " " " " 17SB
30	CD17-	" " " " " 18SB
31	CD18-	" " " " " 19SB
32	CD19-	" " " " " 20SB
33	CD20-	" " " " " 21SB
34	CD21-	" " " " " 22SB
35	CD22-	" " " " " 23SB
36	CD23-	" " " " " LSB
37	SKSS-	SKSS from SDS92 after inversion by NX50
38	SIO-	Response signal to I/O unit test SES

TABLE 9, continued

Pin	Signal	Description
39	RTF-	High speed ready
40	BT-	Block input terminate
41	RT-	Low speed ready
42	I5	I5 interrupt
43	I6	I6 interrupt
44	Sn-	Select pulse unit n (62_8, 24_8, 22_8)
45,46	GND	Ground return

INTERFACE SIGNAL TIMING CONSIDERATIONS

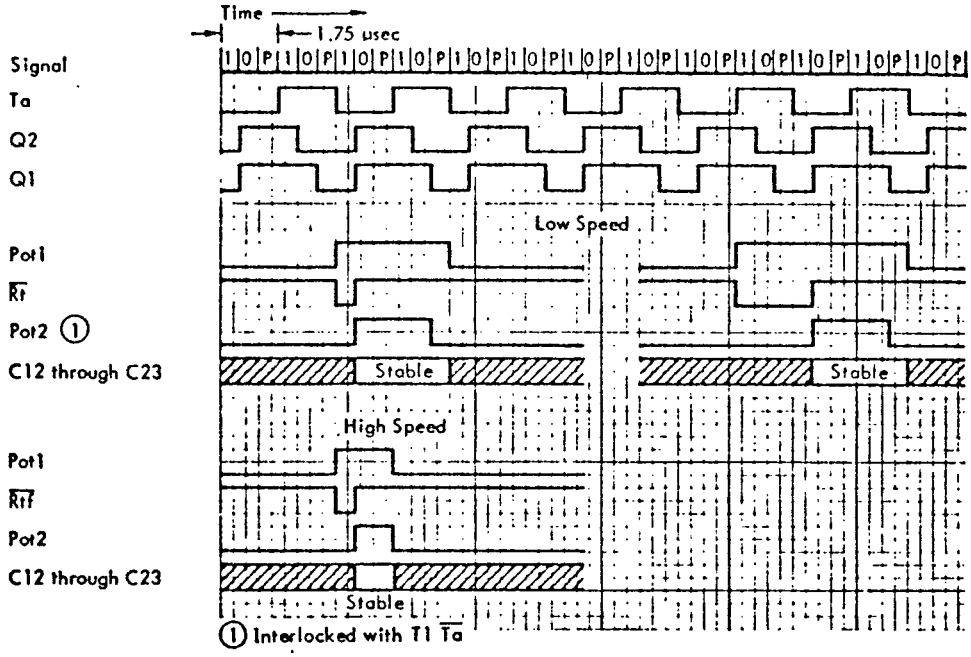
At this point in the discussion of the general purpose interface , it is germane to present information concerning the signals necessary to perform actual data transfer to and from the SDS92.

PARALLEL OUTPUT (POT) TIMING

The POT instruction is preceded by an EOM to select the proper device. The POT instruction causes the SDS92 to access the memory word to be transfered and enter a wait phase. Figure 8 is a signal timing diagram for the POT instruction.

FIGURE 8

SIGNAL TIMING DIAGRAM FOR THE POT INSTRUCTION

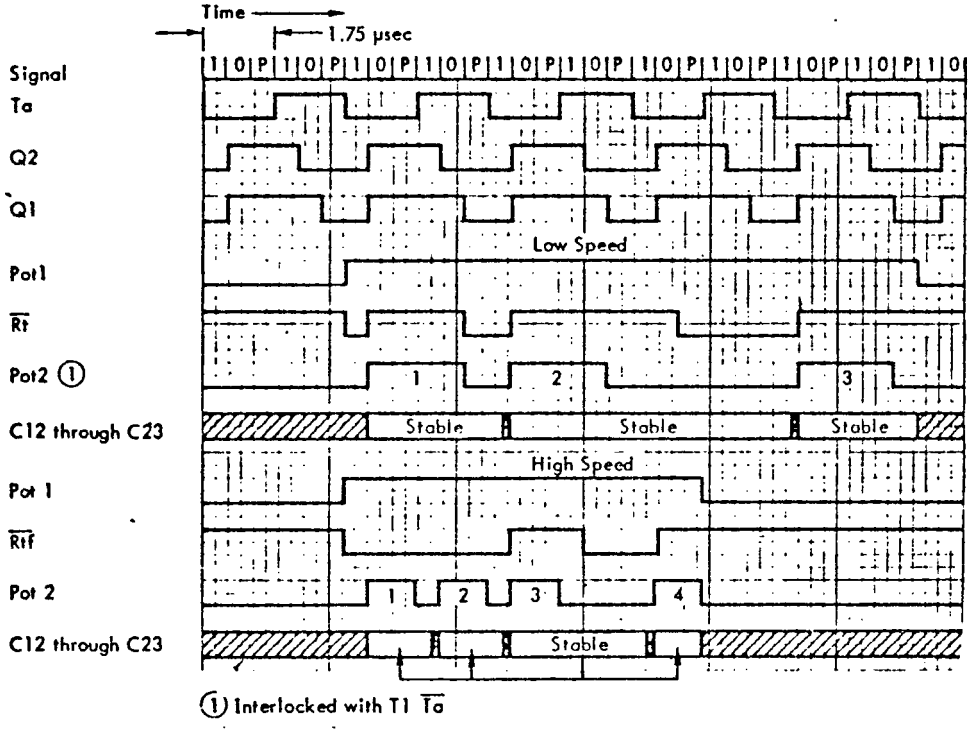


The SDS92 supplies POT1 during the wait phase and will stay in the wait phase until the device responds with either RT- for low speed POT operation or RTF- for high speed POT operation. When either RT- or RTF- are received by the SDS92, it generates the POT2 signal, indicating to the external unit that the output data lines are valid. The manufacturer recommends that the ready signal (RT- or RTF-) be kept down until the POT2 signal is given. When POT2 falls, the output operation is concluded.

BLOCK PARALLEL OUT (BPO) TIMING

Figure 9 is a timing diagram for the BPO instruction.

FIGURE 9
TIMING DIAGRAM FOR THE BPO INSTRUCTION



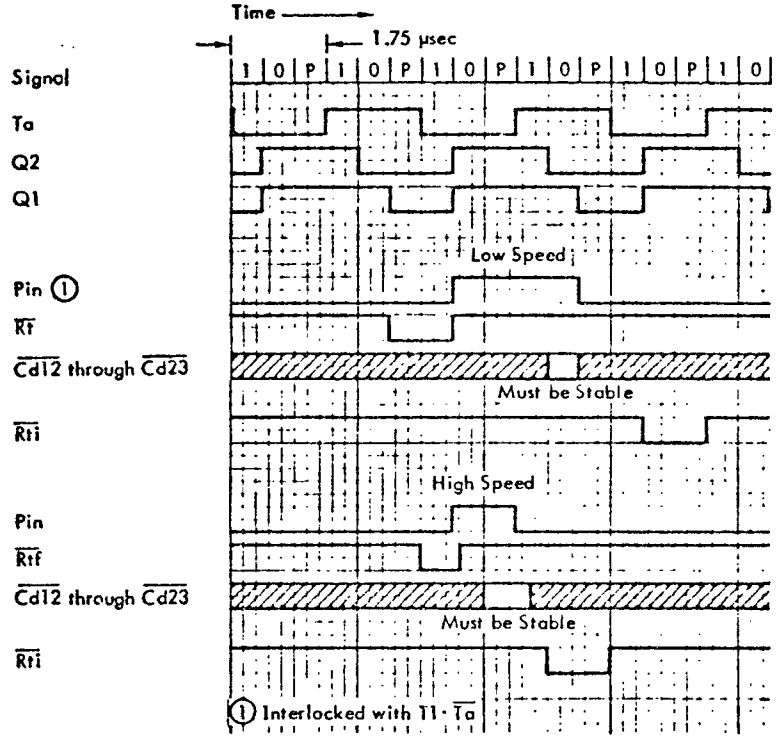
Execution of the BPO instruction proceeds as with the POT instruction until entering the wait phase. At this point the BPO will continue to generate POT2 signals and transfer data under control of the RT- and RTF- signals until the word count in CPU register A is exhausted or the device

gives a BT- (Block Terminate) signal. The manufacturer cautions that in the case of the BPO, the output data lines may not be valid during the leading edge of POT2 and so should be strobed at the trailing edge of POT2.

PARALLEL INPUT (PIN) TIMING

As with the POT instruction, the PIN instruction must be preceeded by an EOM to select the external unit. Figure 10is a timing diagram for the PIN instruction.

FIGURE 10
TIMING DIAGRAM FOR THE PIN INSTRUCTION



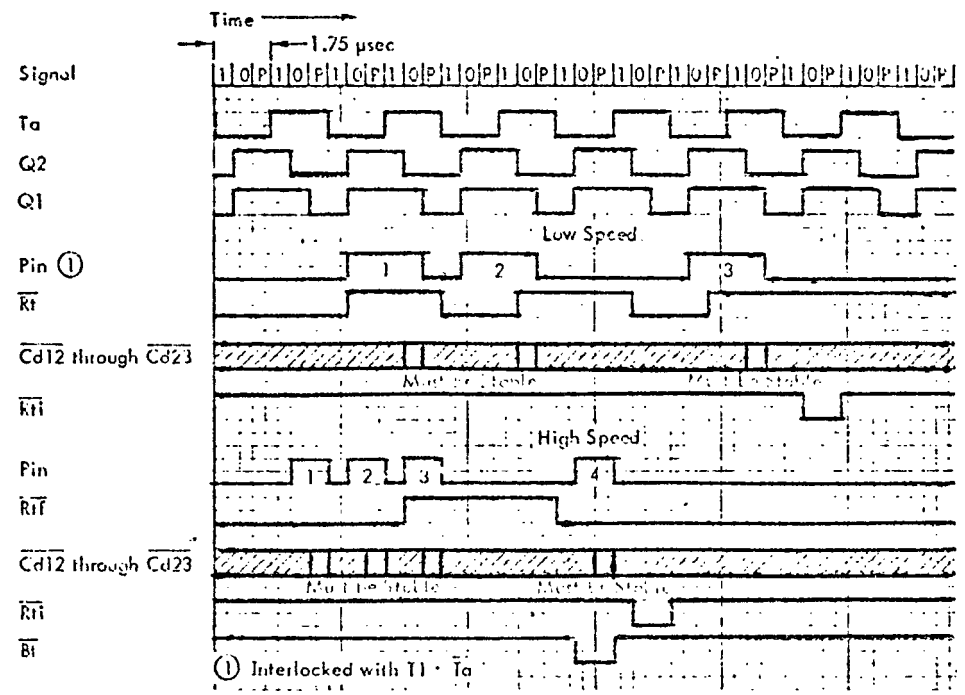
During the execution of the PIN instruction, the SDS92 is placed in a wait state until the external device supplies an RT- for low speed PIN operation or an RTF- for high speed PIN operation. When the SDS92 receives either of these ready signals, it generates the PIN signal, indicating that the input data lines are being strobed. The manufacturer recommends that the input data lines be held valid for the duration of the PIN signal. After the PIN signal falls, the SDS92 generates a terminate signal, RTI, indicating to the device that the input operation is has been concluded.

BLOCK PARALLEL INPUT (BPI) TIMING

Figure 11 is a timing diagram for the BPI instruction.

FIGURE 11

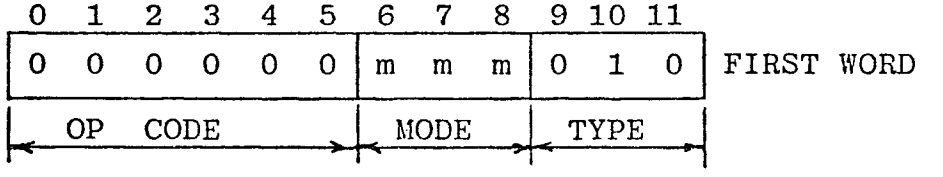
TIMING DIAGRAM FOR THE BPI INSTRUCTION

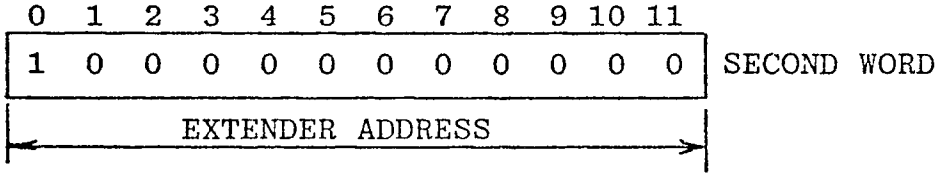


Execution of the BPI instruction proceeds as with the PIN instruction until entering the wait phase. Upon entering the wait phase, the BPI instruction will continue to generate PIN signals and transfer data to the SDS92 under control of the RT- or RTF- signals until either the word count in CPU register A is exhausted or the external device gives a BT- (Block Terminate) . At this point, the SDS92 supplies the device with an RTI signal to indicate that the transfer has been concluded. As with the PIN operation, the manufacturer recommends that the input data lines be held valid for the duration of the PIN signal.

POT/PIN EXTENDER

The POT/PIN Extender consists of a 12 bit register which can be loaded or read by a special EOM/POT or EOM/PIN sequence to output or input words of 24 bits. An Internal Mode EOM, the Extender Alert EOM, is used to signal the POT/PIN Extender that it is to take part in the input or output operation. The format of the Extender Allert EOM is:





For output, the 12 bit extender register is loaded by giving an Extender Alert EOM followed by a POT. This sequence loads the POT/PIN Extender register with data which will be output on data lines C0 to C11. A second EOM/POT sequence is given to select the external device and trigger the transfer of the entire 24 bit word with the data from the second EOM/POT on data line C12 to C23. The manufacturer recommends that the two EOM/POT sequences be executed in direct sequence. Note that use of the POT/PIN Extender in an ontput operation precludes use of the BPO instruction.

Two EOM/PIN sequences are required for use of the POT/PIN Extender on input. The first EOM/PIN sequence causes a data word to be input to the SDS92 in the normal manner over input data lines CD12 to CD23. The EOM issued in this first sequence is an ordinary device select EOM and the data input on CD12 to CD23 is considered to be the least significant in the 24 bit transfer. The second EOM/POT sequence uses an Extender Alert EOM and causes the data word on input data lines CD0 to CD11 to be stored as the most significant bits of the 24 bit transfer. Note that the use of the POT/PIN Extender in an input operation precludes use of the BPI instruction.

CHAPTER IV

DESCRIPTION OF THE CLOSED CIRCUIT TELEVISION SYSTEM

Detailed descriptions of the various parts of the closed circuit television system are given in the manufacturer's manuals [3,4,5,6], so this chapter will present a brief description of the television system as it relates to the video scanner and a description of the modifications which were made to the system.

GENERAL DESCRIPTION

The closed circuit television system (CCTVS) consists of the following three major parts:

1) a Series 6100 COHU high resolution television camera[3],
2) a Series 6900 COHU camera controller[4] with variable scan rate sync generator[5], and
3) a Model CQF Conrac high resolution television monitor[6].

The CCTVS is set up for 30 frame per second, 1225 line scan with EIA RS-343 compatible video output.This television system is used as the image transformer for the video scanner. The camera converts the light image into an electronic analog and the camera controller provides timing signals to the camera and video scanner system. The monitor is used as an operator feedback when adjusting the camera.

MODIFICATIONS

Neither the camera nor the monitor were modified. The only modification made to the camera controller was to tap off some of the timing signals from the sync generator, buffer them, and bring them out to external connectors. Figure 12 is a schematic of the sync generator with modifications. The signals brought out of the sync generator were Master Oscillator, $\overline{\text{Frame Sync}}$, and $\overline{\text{Video On}}$.These three signals were buffered by the 74L00 NAND gates on the monitor driver card. The monitor driver card is a small printed circuit card which is attached to the camera controller chassis and which mounts one 74L00 integrated circuit.

After buffering, $\overline{\text{Master Oscillator}}$, Frame Sync, and Video On are brought to BNC type connectors mounted on the camera controller chassis. Figure 13 is a timing diagram for the sync generator signals.The Master Oscillator (MO) is clock for all timing signals in the sync generator. Frame Sync is a pulse which occurs at the end of every complete frame of composite video.Video On is a signal which is true whenever the Composite Video contains image information.These three timing signals are used by the video scanner to sync with the television system.

The sync generator signals and the EIA RS-343 compatible composite video are connected to the video scanner by means of individual coaxial cables.

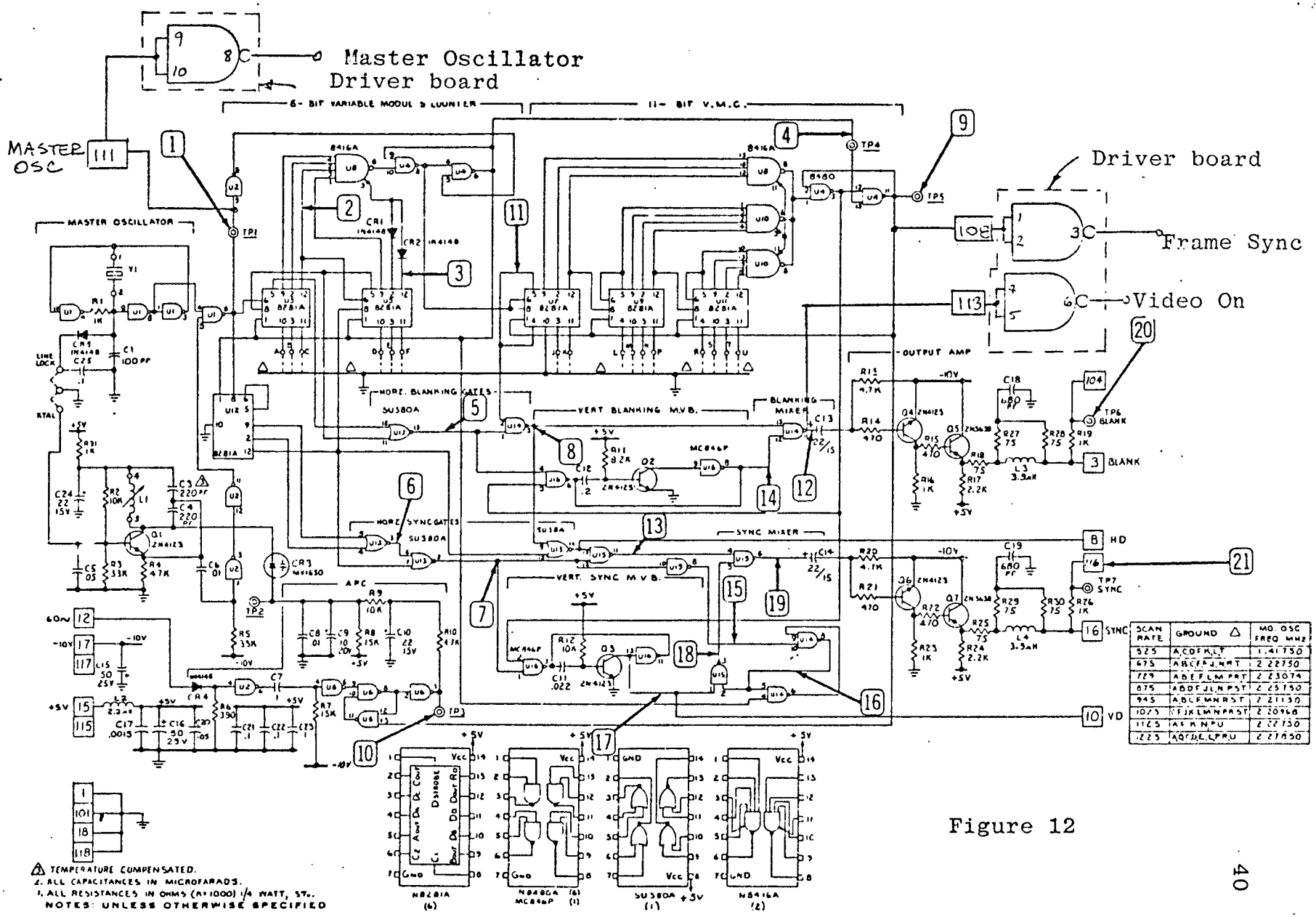


Figure 12

⚠ TEMPERATURE COMPENSATED.
2. ALL CAPACITANCES IN MICROFARADS.
1. ALL RESISTANCES IN OHMS (K=1000) 1/4 WATT, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED

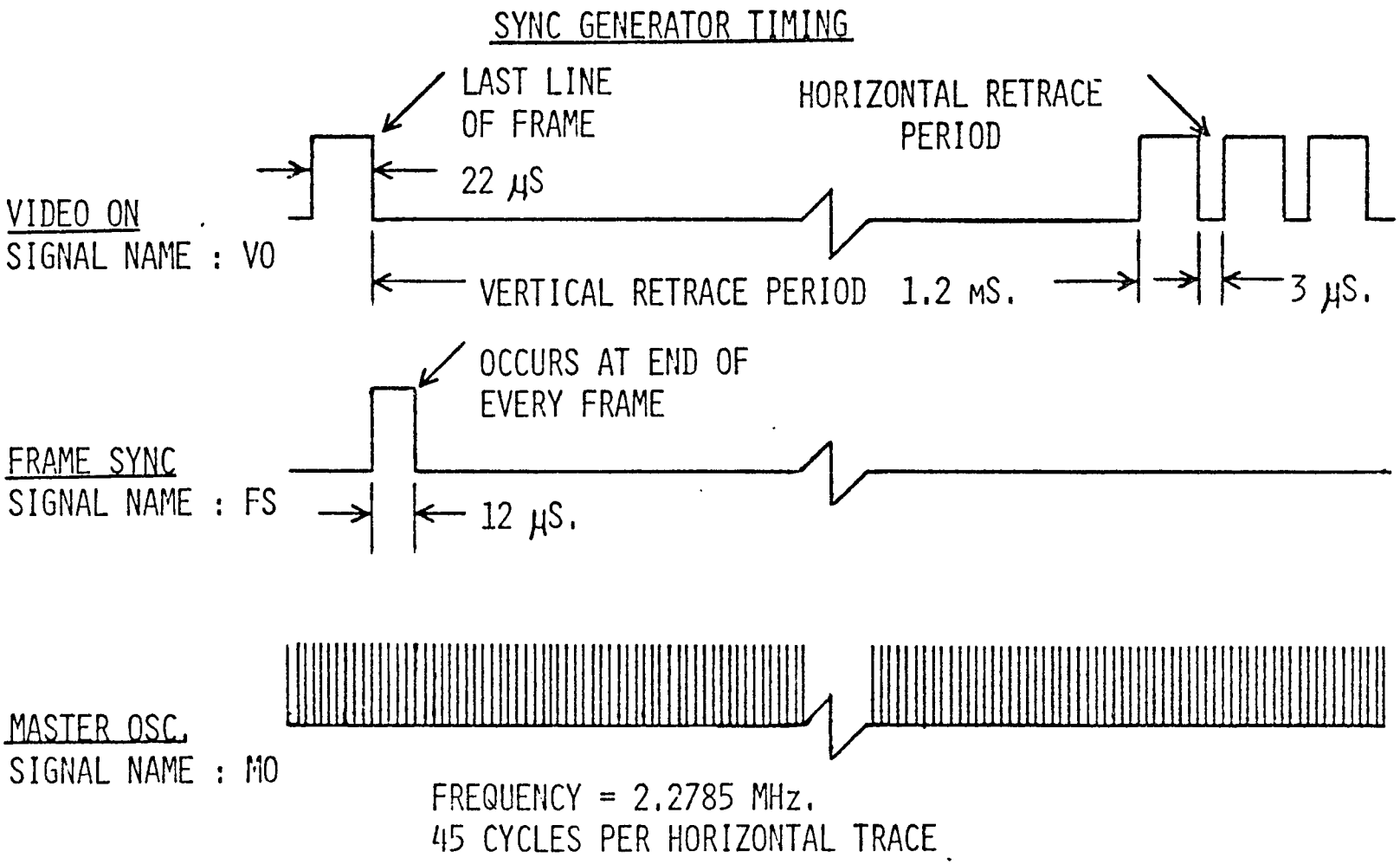

SYNC GENERATOR TIMING
LAST LINE
OF FRAME
HORIZONTAL RETRACE
PERIOD
22 μS
VIDEO ON
SIGNAL NAME : VO
VERTICAL RETRACE PERIOD 1.2 mS.
3 μS.
OCCURS AT END OF
EVERY FRAME
FRAME SYNC
SIGNAL NAME : FS
12 μS.
MASTER OSC.
SIGNAL NAME : MO
FREQUENCY = 2.2785 MHz.
45 CYCLES PER HORIZONTAL TRACE

Figure 13

CHAPTER V
INPUT/OUTPUT CONTROL SECTION OF THE VIDEO SCANNER

The control section of the video scanner was designed to provide input/output timing between the scanner and the computer. The control section was also designed to utilize the general purpose input/output interface as described in Chapter III. The control section is capable of performing the following functions:

FUNCTION	FUNCTION BIT	DESCRIPTION
LOAD CONTROL REGISTER	12	load the control register in the scanner interface from the computer
LOAD DATA REGISTER	14	load a data register in one of the device controllers from the computer
RUN	16	set a bit in the scanner interface which indicates a run or I/O test condition
RESET	17	reset the scanner hardware

Each function is initiated by executing an EOM instruction in system mode for device 021 with the appropriate function bit (see Chapter II) set. A detailed description of each function is given below.

LOAD CONTROL REGISTER

The LOAD CONTROL REGISTER command causes the control section to load a 12 bit control register from the next 12 bit word passed to it. The 12 bit word contains control information for the scanner system and must be output using the following instruction sequence:

EOM	034221	EOM in system mode, load control register bit on, run bit on, device 021
POT	CONWD	Parallel out the 12 bit control word

The control word is formatted as follows:

BIT	NAME	FUNCTION
0	VS ENABLE	A one in this bit enables the video scanner
1	D/A ENABLE	A one in this bit enables the digital to analog converters in the video display system
2	Z AXIS MOD	A one in this bit enables the pulse width modulator in the video display system
3	ERASE	A one in this bit erases the display screen
4	VIEW	A one in this bit sets the display device to view mode (8)
5	NONSTORE	A one in this bit sets the display device to nonstore mode
6	WRITE THRU	A one in this bit sets the display device to write thru mode
7	CLOCK PHASE	A zero sets the video scanner clock at a base time phase and a one sets the video scanner clock at base time plus one-half period
8-11	NOT USED	reserved for expansion

LOAD DATA REGISTER

The LOAD DATA REGISTER command causes the interface to load the next 24 bit data word passed to the interface into one of two data registers. If the VS ENABLE bit (bit 0) is on in the control register, the video scanner data input register is loaded. The format of this register is as follows:

BIT	ASSIGNMENT
0	Horizontal Base Count MSB
1-6	" " "
7	Horizontal Base Count LSB
8	Horizontal Increment MSB
9-14	" " "
15	Horizontal Increment LSB
16	Vertical Skip Count MSB
17-22	" " "
23	Vertical Skip Count LSB

The format of this register is included here for completeness. The purpose of this register will be explained in detail in Chapter VI.

If the D/A ENABLE bit (bit 1) is on in the control register, the D/A data register is loaded. The format of the D/A data register is as follows:

BIT	ASSIGNMENT
0	DAC0 (X Axis) MSB
1-6	" "
7	DAC0 (X Axis) LSB
8	DAC1 (Y Axis) MSB
9-14	" "
15	DAC1 (Y Axis) LSB
16	DAC2 (Z Axis, modulation level) MSB
17-22	" "
23	DAC2 (Z Axiz, modulation level) LSB

The format of this register is included here for completeness. The purpose of this register will be explained in detail in Chapter VII.

RUN

The RUN command was implemented as a hardware debug aid. If the RUN bit is a zero, the control section will accept commands and data from the computer, but will not act on them.

This is advantageous when the data path from the computer to the controller registers must be tested, If the RUN bit is a one, the control section will accept commands and data in the normal manner.

RESET

The RESET command causes the controller to set its logic at an initial state and cancel any commands currently beingexecuted.

SPECIAL NOTE

When the LOAD DATA REGISTER command is used, the data registers involved are 24 bits long; therefore, the following instruction sequence must be used to load them:

EOM	034221	EOM to load contol register
POT	CONWD	POT a control word
EOM	024000	EOM to allert extender
POT	HITWLVE	POT bits 0-11 of 24 bit data word to extender
EOM	031221	EOM to allert device 021, LOAD DATA REGISTER and RUN bits on
POT	LOTWLVE	POT bits 0-11 from extender and bits 12-23 from LOTWLVE

See Chapter III for operating details of the Extender Allert EOM.

IMPLEMENTATION

Figure 14 is a circuit diagram of the hardware which was constructed to implement the operations described in the first part of this chapter. The circuit is compatible with the general purpose input/output interface as described in Chapter III and is constructed on a printed circuit board which plugs into slot 10 of the interface chassis.

CIRCUIT OPERATION

In reference to figure 14, it can be seen that when the program issues an EOM to device 021, the general purpose interface device decoder will generate the S21- signal at pin 44 of the controller card. The S21- sets the type 7474 flip-flop at location 12 and causes the DSEL (device select) condition to be set. At the same time, the function bits of the EOM are latched into the type 7474 flip-flops at locations 8,9, and 10.

If the command is a RESET, bit C16- at pin 29 is low, which causes the RESET condition to be raised. The leading edge of RESET generates a pulse through the differentiator network connected to pin 8 of the type 7474 flip-flop located at position 8. This pulse is buffered by the type 7440 gates at location 17. The reset pulse , RSTP, and its inverse, RSTP-, are made available at pins 4 and D of the 44 pin external connector. The RSTP- pulse resets the type 7474 flip-flop at position 12 thus dropping the DSEL condition and concluding the I/O operation.

If the command is not a RESET, the appropriate function bit latch and the DSEL latch remain set after the EOM is finished so that a subsequent POT instruction will cause the data to be routed to the proper register. When the POT1-

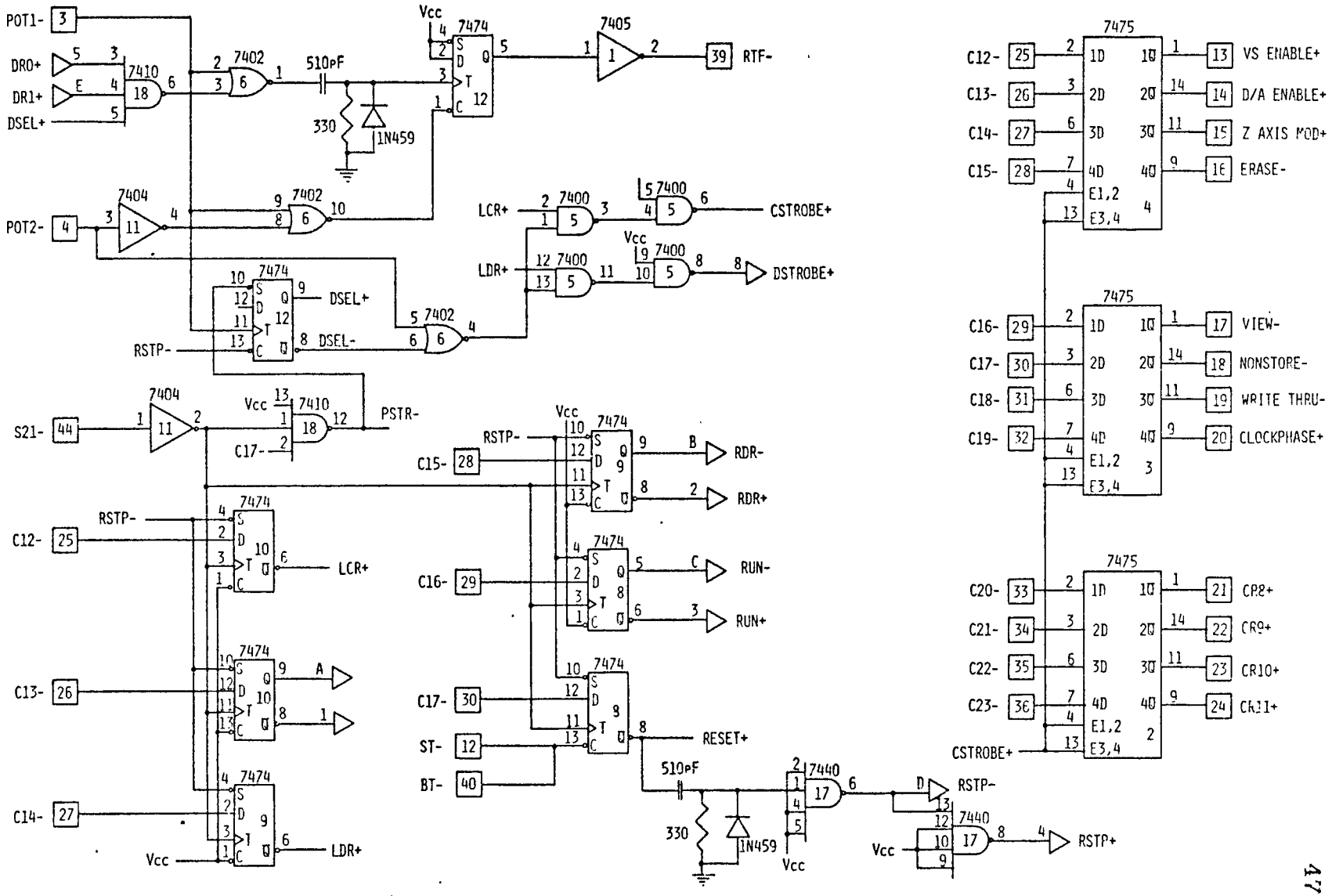

POT1-
DR0+
DR1+
DSEL+
POT2-
S21-
C12-
C13-
C14-
C15-
C16-
C17-
ST-
BT-
C20-
C21-
C22-
C23-
CSTROBE+
LCR+
LDR+
RSTP-
RSTP+
PSTR-
RTF-
CSTROBE+
DSTROBE+
DSEL+
DSEL-
RDR-
RDR+
RUN-
RUN+
RESET+
A
1
LCR+
LDR+
VS ENABLE+
D/A ENABLE+
Z AXIS MOD+
ERASE-
VIEW-
NONSTORE-
WRITE THRU-
CLOCKPHASE+
CR8+
CR9+
CR10+
CR11+
7410
7402
7404
7474
7405
7400
7475
7440
510pF
330
1N459
Vcc

Figure 14

signal occurs, the RTF flip-flop at location 12 is set if both device ready indicators (DR0 and DR1) are true. DR0 indicates the ready status of the scanner and DR1 indicates the ready status of the display system. As soon as the computer receives the RTF- signal, it issues the POT2- to strobe the data on the data lines to the interface. When POT2- occurs, the appropriate register is loaded by the strobe signals generated by the type 7400 NAND gates at location 5. POT2- also clears the RTF flip-flop. When POT1- goes high, the DSEL flip-flop is cleared and the I/O operation is concluded.

The command register is implemented by the type 7475 latches at locations 2, 3, and 4. The scanner input register and the D/A register are located on other cards.

CHAPTER VI

IMPLEMENTATION OF THE VIDEO SCANNER

The video scanner uses the television sync signals described in Chapter V to address and convert selected points in the video output from the television system. The television system produces a 1225 line 2:1 interlace scan output. This means that 612.5 horizontal lines are scanned on each pass or half-frame. Each horizontal line in a half-frame contains 22 microseconds of video image information and 3 microseconds of timing information (see Figure 13). The television sync generator produces three timing signals which provide a convenient means for constructing an image addressing scheme. One signal, Frame Sync (FS), occurs at the end of each half-frame and can be used as an initial starting point for addressing . Another signal, Video On (VO), is high during the 22 microseconds of image information in each horizontal line. VO can be used to drive a counter to provide vertical addressing. A third signal, Master Oscillator (MO), is the main clock for the television system. MO goes through 45 cycles during the time that Video On is up and can be used to drive a counter to provide horizontal addressing.

ASSUMPTIONS

Two simplifying assumptions were made about the video information. First, it was assumed that the television system is stable enough that the difference between successive half-frames of video is negligable. This assumption allows that any half-frame may be digitized without regard to sequence.

Second, it was also assumed that the television system has enough resolution that the difference between any pair of

adjacent lines is negligable. This assumption allows that any points taken from a pair of adjacent lines are from the same line or that the television system has a logical resolution of 306 lines per half-frame.

PRACTICAL CONSIDERATIONS

It was decided to digitize only one point from each actual line during a half-frame due to the speed limitations of the computer input section.

It was ascertained that a grey scale of 64 levels would provide sufficient intensity resolution. Also, a 64 level scale may be represented by a 6 bit binary number and this allows two image points to be packed into a single computer word.

It was also ascertained that a matrix of points with 256 columns and 256 rows would provide sufficient positional resolution. This requirement posed two intrinsic problems. One problem was that a 256 by 256 matrix of points requires 32,768 words of computer memory for storage even when the elements of the matrix are packed two to a word. The computer which is being utilized has exactly 32,768 words of memory, so the entire memory would be required to store an image. Another problem was that the master oscillator frequency would have to be multiplied by at least six in order to get enough time divisions during a horizontal line (45 cycles X 6 = 270 cycles). Also, the multiplied output would have to remain locked in sync with the other timing signals. The only reasonable way to assure both conditions is to do the frequency multiplication using a phase locked loop with digital feedback. Currently available phase locked loop circuits are limited to a maximum output frequency of about 12 MHertz. Since the multiplied frequency would be approximately 13.7 MHertz , the frequency

limitation precludes a direct application of the phase locked loop.

A solution to both of the above problems was attained by using a phase locked loop to multiply the master oscillator by three (45 cycles X 3 = 135 cycles) and allowing the computer to specify which phase of the multiplier output would be used to drive the horizontal addressing logic. This technique allows the computer to make a 128 horizontal by 256 vertical scan of the image at one oscillator phase to obtain half of the image, dump the scan to external storage, then make another 128 by 256 scan to pick up the other half of the information. The technique might be called a "horizontal interlace" since every other element in a row of the resulting matrix would come from an alternate scan.

Another practical consideration for the scanner design was to optimize the speed of scanning. If only one point is taken on a line, a total of 256 passes or 256 half-frame times are required to obtain all 256 columns. A twofold speed increase can be realized by utilizing the assumption about adjacent lines. Under this assumption, it is possible to scan off pairs of points in a double column order.One point of a pair would come from a column of the first line of a line pair and the other point would come from an adjacent column of the second line of a line pair. Figure 15 illustrates the order in which pairs of points would be scanned from the image.

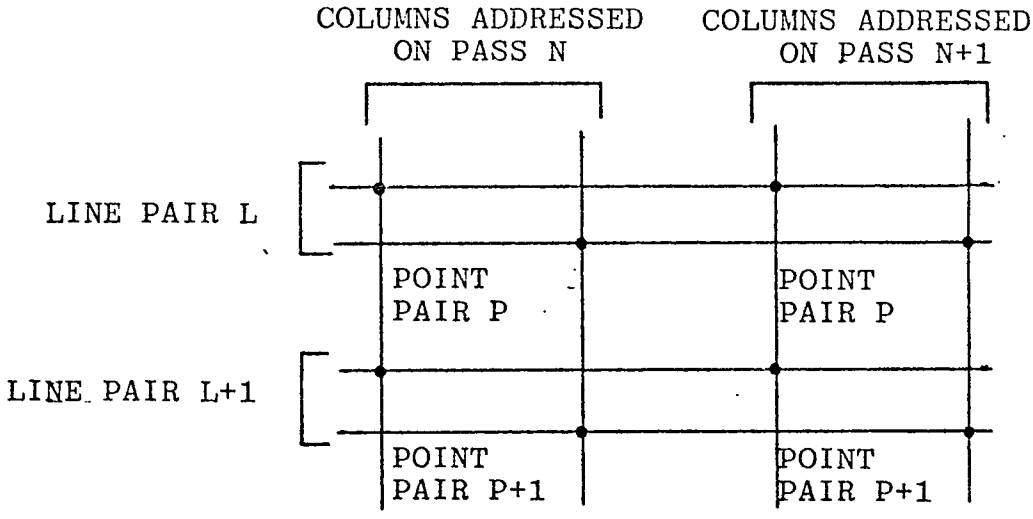


Figure 15

VARIABLE FORMAT

It was decided to make the scan format variable. A variable format capability was implemented which allows the user to specify any resolution up to 256 by 256.

The variable horizontal resolution was implemented by allowing the user to specify an initial horizontal address and an address increment with the address increment equal to the number of multiplied master oscillator cycles between columns of the image. The variable vertical resolution was implemented by logically separating all the horizontal lines in a half-frame into groups and allowing the user to specify the number of lines in a group. With this technique , a group of lines consists of the two lines from which a pair of points is taken plus a number of lines which are to be skipped. As an example,if the user wished to make a 64 by 64 scan, the horizontal increment would be 2 and the group size would be 4.

It was decided to make the operation of the scanner as automatic as possible. Toward this end, the scanner was designed to make a complete scan of the image with one control output operation. The only control information that changes between input passes is the initial horizontal address and the scanner was designed to automatically calculate the next initial address at the end of each input pass.

HARDWARE IMPLEMENTATION

A scanning system was implemented using the assumptions and practical considerations outlined in the beginning of this chapter. Figure 16 is a block diagram of this system. The system consists of four sections: the television system, the analog-to-digital interface, the addressing and sequencing section, and the scanner control section.The television system and the control section have been covered in previous chapters. The remainder of this chapter will be devoted to a discussion of the hardware for the analog-to-digital interface and the addressing and sequencing section.

ANALOG-TO-DIGITAL INTERFACE

The purpose of this section is to convert the raw video from the television system to binary numbers and pack two numbers into a 12 bit computer word. The modules within the section are as follows:

a. the signal conditioner
b. the analog-to-digital converter with sample and hold amplifier, and
c. the output controller.

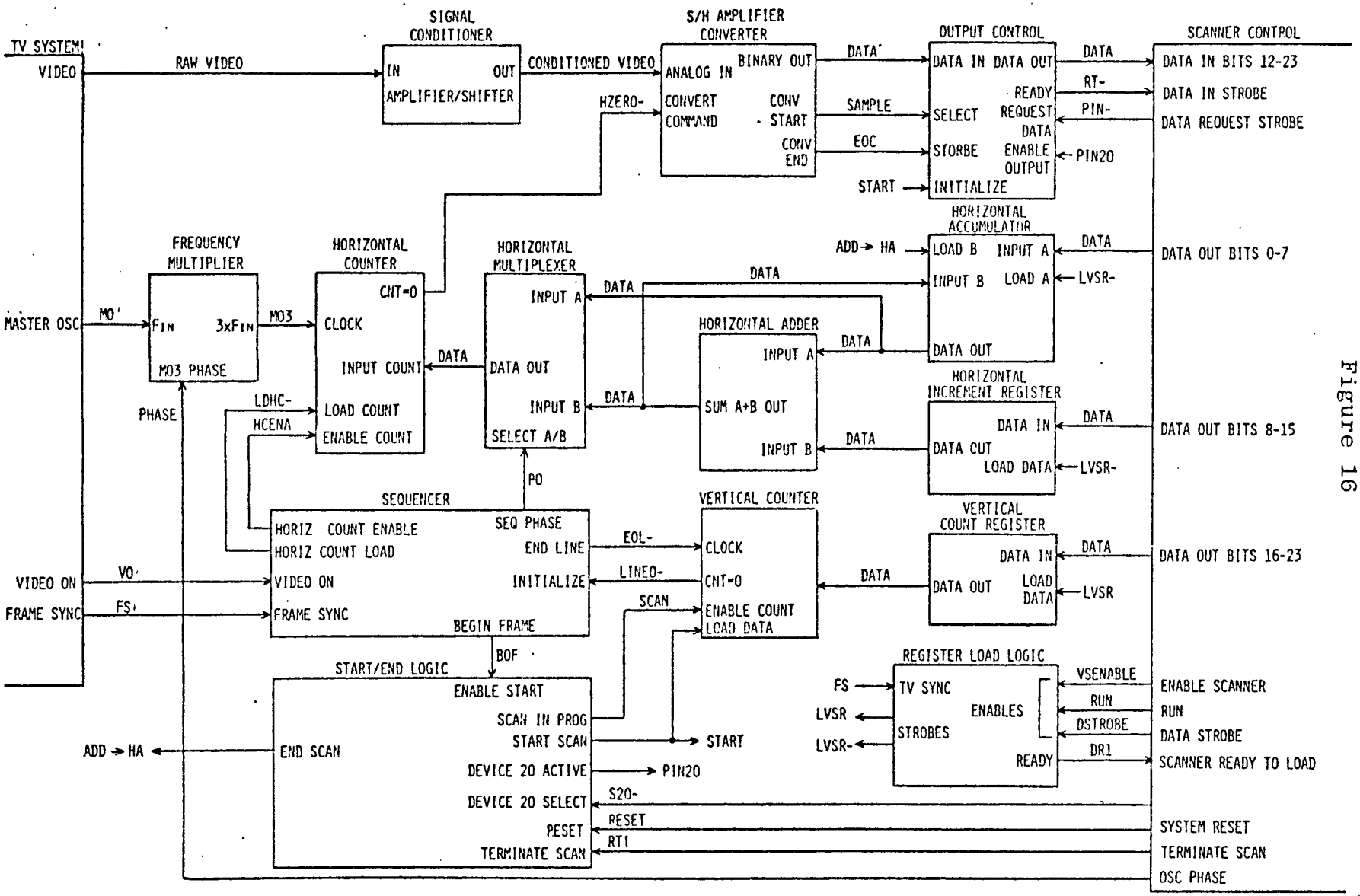

TV SYSTEM
VIDEO
RAW VIDEO
SIGNAL CONDITIONER
IN
OUT
AMPLIFIER/SHIFTER
CONDITIONED VIDEO
S/H AMPLIFIER CONVERTER
ANALOG IN
BINARY OUT
CONVERT COMMAND
CONV START
CONV END
HZERO-
DATA
SAMPLE
EOC
START
OUTPUT CONTROL
DATA IN
DATA OUT
SELECT
READY
REQUEST DATA
STORBE
ENABLE OUTPUT
INITIALIZE
PIN20
SCANNER CONTROL
DATA IN BITS 12-23
DATA IN STROBE
DATA REQUEST STROBE
RT-
PIN-
HORIZONTAL ACCUMULATOR
ADD→HA
LOAD B
INPUT A
INPUT B
LOAD A
LVSR-
DATA OUT BITS 0-7
FREQUENCY MULTIPLIER
MASTER OSC
MO'
FIN
3xFIN
MO3 PHASE
MO3
HORIZONTAL COUNTER
CNT=0
CLOCK
INPUT COUNT
LOAD COUNT
ENABLE COUNT
LDHC-
HCENA
PHASE
HORIZONTAL MULTIPLEXER
INPUT A
DATA OUT
INPUT B
SELECT A/B
PO
HORIZONTAL ADDER
SUM A+B OUT
HORIZONTAL INCREMENT REGISTER
LOAD DATA
DATA OUT BITS 8-15
SEQUENCER
HORIZ COUNT ENABLE
HORIZ COUNT LOAD
VIDEO ON
FRAME SYNC
SEQ PHASE
END LINE
INITIALIZE
BEGIN FRAME
VO'
FS'
VERTICAL COUNTER
EOL-
LINEO-
SCAN
ENABLE COUNT
LOAD DATA
VERTICAL COUNT REGISTER
DATA OUT BITS 16-23
BOF
START/END LOGIC
ENABLE START
SCAN IN PROG
START SCAN
END SCAN
DEVICE 20 ACTIVE
DEVICE 20 SELECT
PESET
TERMINATE SCAN
REGISTER LOAD LOGIC
TV SYNC
ENABLES
STROBES
VSENABLE
RUN
DSTROBE
DR1
ENABLE SCANNER
DATA STROBE
SCANNER READY TO LOAD
S20-
RESET
RTI
SYSTEM RESET
TERMINATE SCAN
OSC PHASE

Figure 16

SIGNAL CONDITIONER

Figure 17 is a circuit diagram of the signal conditioner , the sample and hold amplifier , and the converter. The circuit is constructed on a printed circuit board which plugs into slot 1 of the interface chassis. The signal conditioner converts the 1 volt video signal to a 0 to 2.5 volt level for input to the sample and hold amplifier.The shifting and amplifying is accomplished by the two type 715 operational amplifiers at the top of Figure 17. The first amplifier is a buffer and inverter. The second amplifier performs the amplifying and shifting functions and is also an inverter. Variable offset and amplification are provided by the offset and gain controls.

SAMPLE AND HOLD AMPLIFIER

The sample and hold amplifier is of the open ended type. This type of sample and hold gates the analog signal through to the output until commanded to hold. It then holds the output at the instantaneous value of the input just prior to the hold command. The hold operation is necessary so that the input to the analog-to-digital converter will be constant during the conversion cycle. The sample and hold amplifier returns to the sample mode as soon as the hold period is over.

ANALOG-TO-DIGITAL CONVERTER

The analog-to digital converter has a resolution of 8 bits and a cycle time of 4 microseconds. The input range of the converter is 0 to 10 volts so the 6 bit resolution required by the scanner is obtained by limiting the input swing to between 0 and 2.5 volts and taking the six least significant bits as the true output. A conversion cycle is initiated by

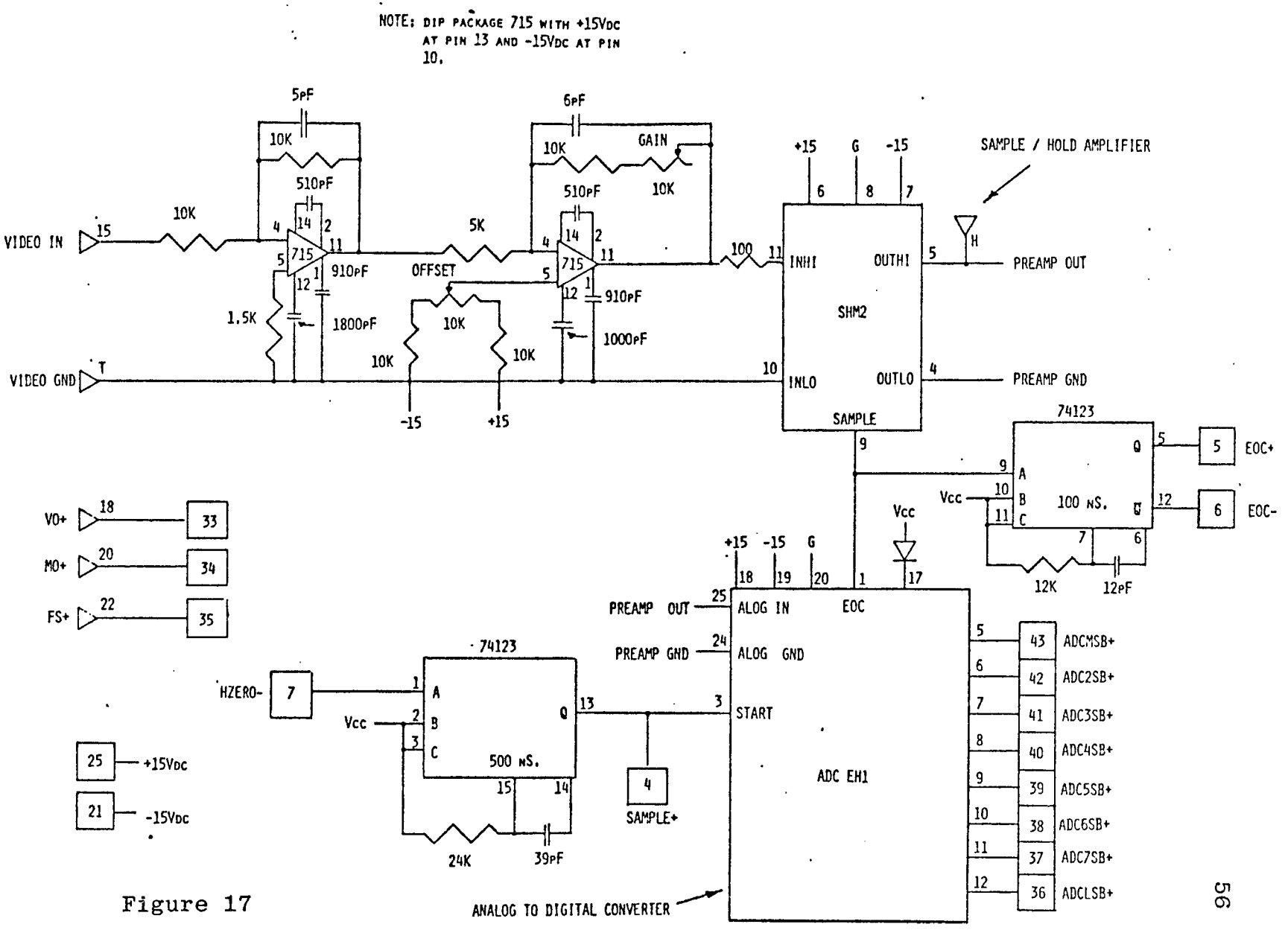

NOTE: DIP PACKAGE 715 WITH +15VDC AT PIN 13 AND -15VDC AT PIN 10.
SAMPLE / HOLD AMPLIFIER
VIDEO IN
VIDEO GND
5PF
10K
510PF
910PF
1800PF
1.5K
5K
OFFSET
6PF
GAIN
1000PF
100
INHI
OUTHI
SHM2
INLO
OUTLO
SAMPLE
PREAMP OUT
PREAMP GND
+15
-15
G
74123
100 NS.
12K
12PF
EOC+
EOC-
Vcc
VO+
MO+
FS+
HZERO-
500 NS.
24K
39PF
SAMPLE+
PREAMP OUT
PREAMP GND
ALOG IN
ALOG GND
START
EOC
ADC EH1
ADCMSB+
ADC2SB+
ADC3SB+
ADC4SB+
ADC5SB+
ADC6SB+
ADC7SB+
ADCLSB+
+15VDC
-15VDC
ANALOG TO DIGITAL CONVERTER

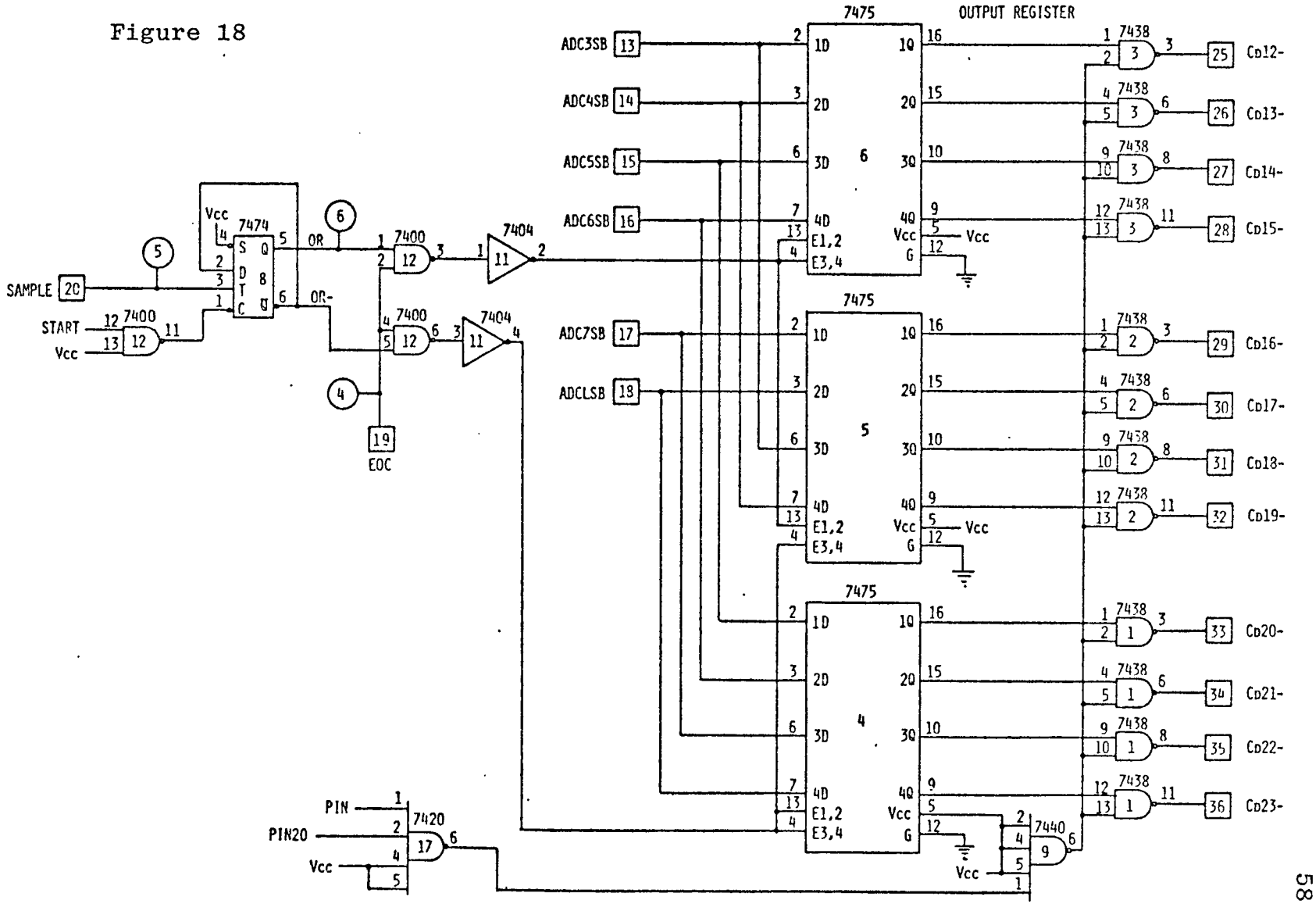
Figure 17

the leading edge of the HZERO- signal from the addressing and sequencing logic. The HZERO- leading edge fires the 74123 one-shot and generates the 500 nanosecond SAMPLE pulse. The SAMPLE pulse commands the converter to do a conversion cycle.The converter signals the sample and hold to hold by raising the busy indicator at pin 1 of the converter. The converter then performs a conversion cycle and produces the binary output at the lines marked ADCMSB to ADCLSB. The least significant six bits, ADC3SB to ADCLSB, are used by the output control module. At the end of the 4 microsecond conversion cycle , the converter drops the busy line to return the sample and hold to the sample state. The trailing edge of the busy signal fires a 74123 one-shot to produce the 100 nanosecond END OF CONVERSION (EOC) pulse.

OUTPUT CONTROL LOGIC

The output control logic uses the EOC and SAMPLE pulses to pack two of the six bit conversions into a 12 bit computer word. Figure 18 is a circuit diagram of the output control logic. The circuit is constructed on a printed circuit card which plugs into slot 9 of the interface chassis.The logic is initialized by a START pulse from the addressing and sequencing logic. This clears the 7474 flip-flop at location 8 and causes the line marked OR- to be high. The first SAMPLE pulse to occur causes the 7474 to toggle which makes the line marked OR go high. A subsequent EOC pulse gates the ADC3SB to ADCLSB levels into the 7475 latches at locations 5 and 6. A second SAMPLE pulse will cause the 7474 to toggle again and this raises the OR- line.The EOC pulse following the second SAMPLE pulse gates the outputs of the converter to the 7475 latches at 4 and 5. The outputs of the 7475 latches at 4, 5,

Figure 18


OUTPUT REGISTER
7475
7474
7400
7404
7420
7440
7438
ADC3SB
ADC4SB
ADC5SB
ADC6SB
ADC7SB
ADCLSB
SAMPLE
START
EOC
PIN
PIN20
Vcc
OR
OR-
CD12-
CD13-
CD14-
CD15-
CD16-
CD17-
CD18-
CD19-
CD20-
CD21-
CD22-
CD23-

and 6 are gated onto the interface data buss by the 7438 buffers at locations 1,2, and 3 with the coincidence of the PIN20 and PIN signals. PIN20 is a product of the addressing and sequencing logic and PIN is derived from the computer PIN- data input strobe.

READY HANDSHAKE LOGIC

The ready handshake logic is the part of the output control logic that signals the completion of the packing of a word to the computer.Figure 19 is a schematic of the ready handshake logic. The circuit is constructed on card 9 with the rest of the output control logic.

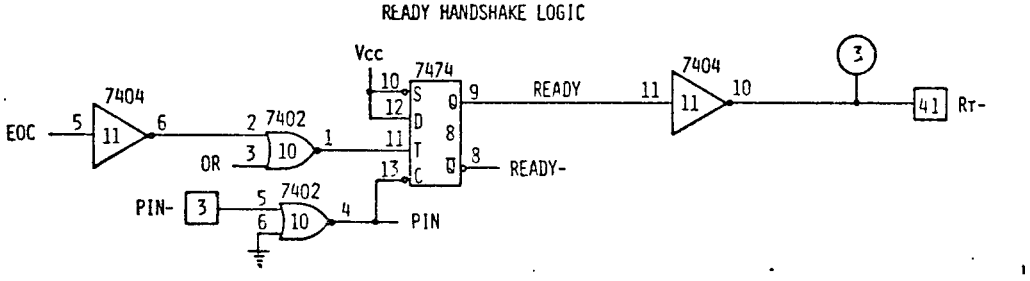


Figure 19

The OR signal is low when the second EOC occurs in the packing sequence. This causes the 7474 flip flop at location 8 to set and generate the READY signal . READY is inverted by the 7474 at location 11 and becomes the RT- signal to the computer. When RT- goes down, the computer generates the PIN- signal to strobe the data to the input data buss. PIN- also resets the READY flip-flop to complete the input operation. The scanner output logic is now ready to perform another packing operation on the next pair of conversions.

ADDRESSING AND SEQUENCING SECTION

The addressing and sequencing section controls the internal operation of the scanner. The section has four sub-sectionswhich are :

a. the register load logic,
b. the sequencing logic,
c. the horizontal addressing logic, and
d. the vertical addressing logic.

REGISTER LOAD LOGIC

The register load logic syncronizes the television system with the scanner control at the beginning of a pass. Figure 20 is a schematic diagram of the register load logic. The circuit is constructed on a printed circuit card which plugs into slot 6 of the interface chassis.

REGISTER LOAD LOGIC

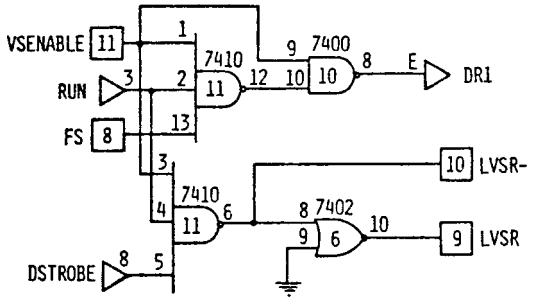


Figure 20

The VSENABLE and RUN signals are a product of the scanner control logic (see Chapter VI). VSENABLE and RUN are high when the scanner is enabled. DR1 is the ready signal to the scanner control logic and is held low until the FRAME SYNC (FS) signal is received from the television system.DR1 goes high when FS occurs and this signals that the scanner is ready

to receive control data from the data output lines of the computer interface. The scanner control logic answers the DR1 with a DSTROBE pulse. The conjunction of DSTROBE, VSENABLE, and RUN generates the LVSR and LVSR- pulses which load the scanner control data registers. Once the registers are loaded, the scanner has all the information necessary to perform a complete scan of the image. All addressing and sequencing is accomplished by the scanner and the computer has only to request input from the scanner to perform the scan.

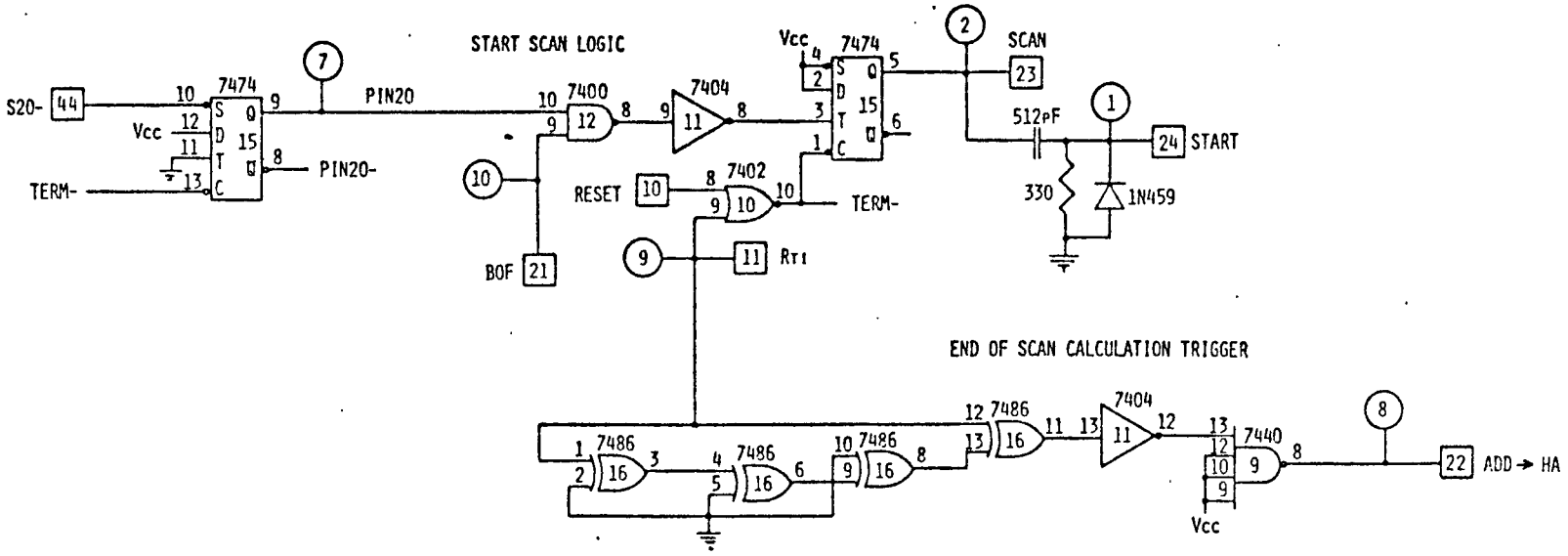
SEQUENCING LOGIC

The sequencing logic takes control of the scanner after the control data registers are loaded. The sequencing logic consists of two modules: the start/end logic and the run sequencer. The start/end logic controls the boundary condition operation of the scanner and the run sequencer controls operation within a pass.

START/END LOGIC

Figure 21 is a schematic of the start/end logic. The circuit is constructed on a printed circuit board which plugs into slot 9 of the interface chassis.

The S20- line from the general purpose interface goes down when the computer requests input from the scanner. This sets the 7474 flip-flop at location 15 and raises the PIN20 line. After PIN20 comes up, the scanner logic will wait for BOF to go down. BOF is a product of the run sequencer logic and will be explained later in this chapter. After BOF goes down, the 7474 flip-flop at location 15 sets to raise the SCAN condition. The SCAN condition enables the addressing logic



START/END LOGIC

Figure 21

and generates the START pulse which in turn initializes the run sequencer. Figure 22 is a timing diagram which illustrates the sequence of events from the loading of the control data registers to the generation of the START pulse.

RUN SEQUENCER

The run sequencer takes control of the scanner after the START pulse is generated. Figure 23 is a schematic of the run sequencer. The circuit is constructed on a printed circuit board which plugs into slot 6 of the interface chassis.The 74193 counter at location 17 implements a 16 line wait at the beginning of each half-frame. The first 16 lines are ignored because the vertical retrace blanking circuits in the television sytem sync generator are still going off during these lines and the lines contain no valid video data. The FRAME SYNC (FS) pulse causes the counter to be loaded with a count of 16 and makes the BOF line go high. The counter is then decremented each time the VOD pulse occurs. VOD is generated at the trailing edge of the VIDEO ON (VO) pulse.The counter continues to decrement until the count reaches zero. The counter is stopped when the count reaches zero and the BOF line goes low. The run sequencer is ready to take control when BOF goes low.The run sequencer will now drive the scanner through an addressing cycle.During the addressing cycle, the scanner will digitize a point from each of the first two lines in a group and then skip a predetermined number of lines to the beginning of the next group.

After BOF goes low (BOF- high), the next VO pulse to occur will fire the 74121 one-shot at location 1 to produce the LOAD HORIZONTAL COUNTER (LDHC-) pulse.LDHC- loads the horizontal address counter and sets the 7474 flip-flop at

LOAD / START SEQUENCE TIMING

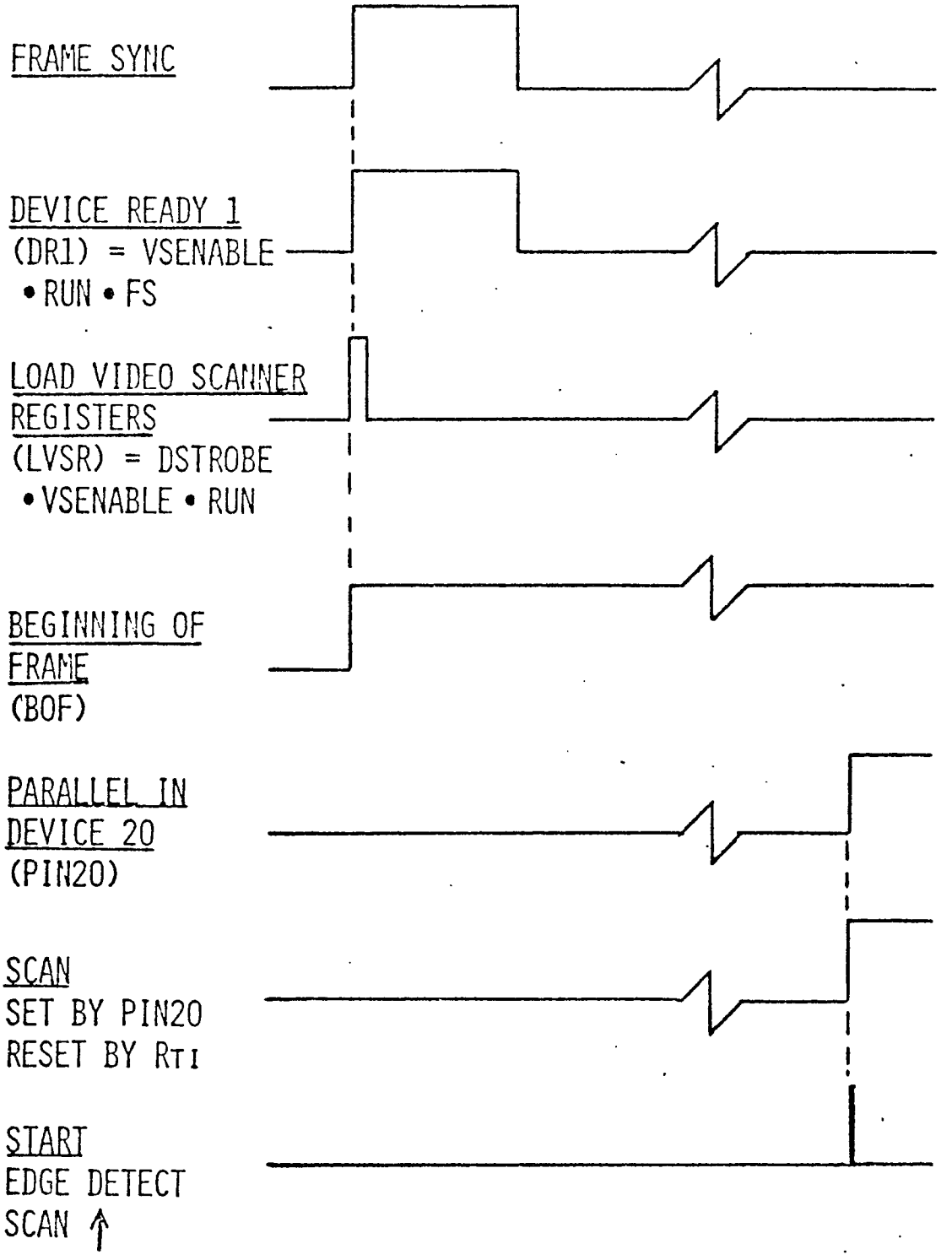
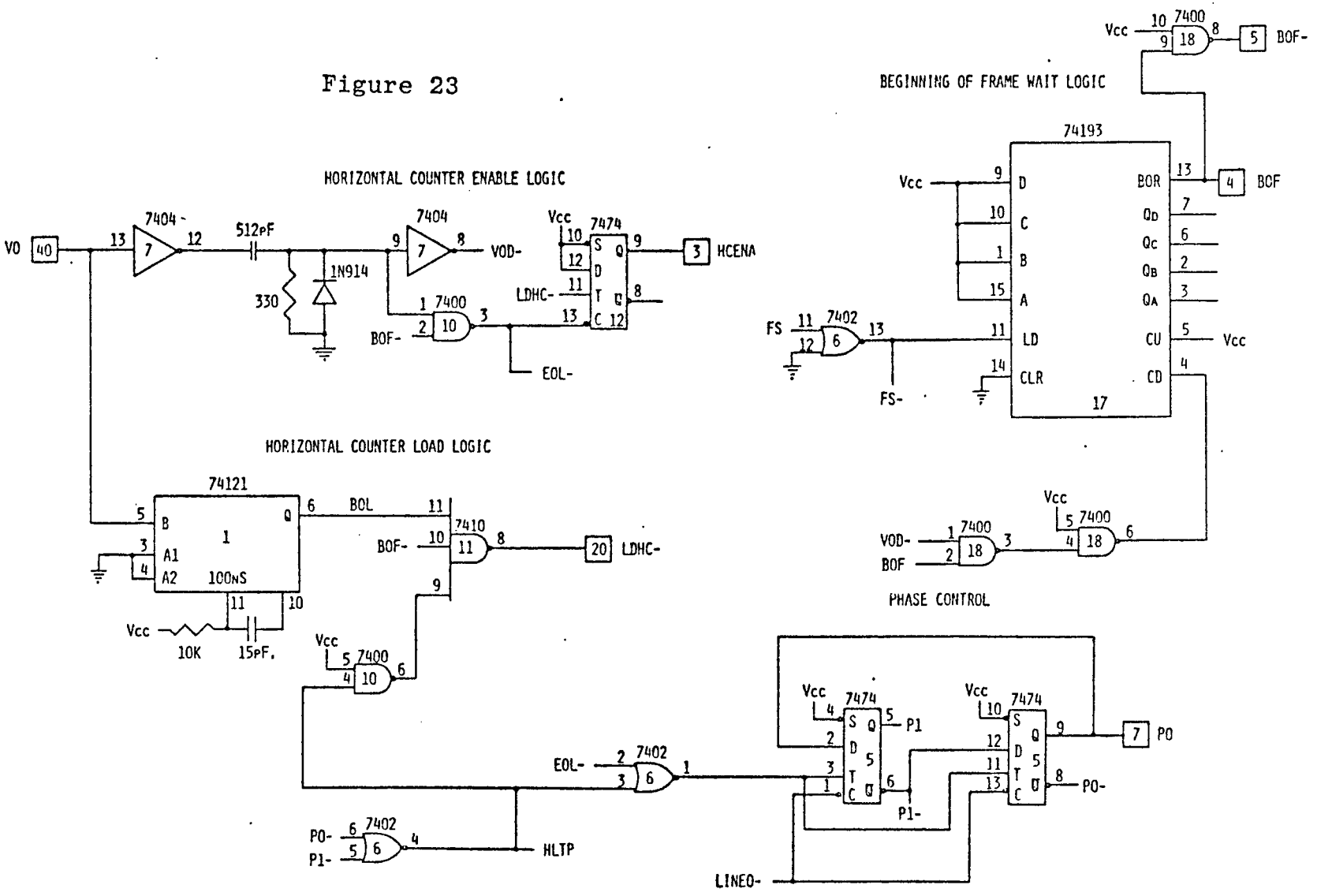


Figure 22

Figure 23


HORIZONTAL COUNTER ENABLE LOGIC
VO
40
7404
512pF
1N914
330
7404
VOD-
7474
Vcc
LDHC-
7400
BOF-
EOL-
HCENA
3
BEGINNING OF FRAME WAIT LOGIC
74193
Vcc
D
C
B
A
LD
CLR
BOR
QD
QC
QB
QA
CU
CD
BOF
7402
FS
FS-
HORIZONTAL COUNTER LOAD LOGIC
74121
B
A1
A2
100nS
BOL
7410
LDHC-
20
10K
15pF.
PHASE CONTROL
P1
P1-
PO
PO-
7
HLTP
LINEO-

location 12. This raises the HORIZONTAL COUNTER ENABLE (HCENA) line to enable the horizontal address counter.The horizontal addressing logic is now prepared to locate the first point to be digitized . The VO line will fall some time after the point is taken. When VO falls, the EOL- pulse is generated and this causes the phase counter (7474 flip-flops at location 5) to be advanced. Eol- also decrements the vertical group counter. Another LDHC- pulse is generated when the VO line comes up for the second line in the group. HCENA is set again and the horizontal addressing logic proceeds to find the second point in the pair.The EOL- pulse from the second line in the group will cause the phase counter to enter a state where P0- and P1- are both low. P0- and P1- low in conjunction raises the HALT PHASE (HLTP) line which disables the horizontal addressing logic and stalls the phase counter. The phase counter will remain in this state until the vertical group counter decrements to zero. The vertical addressing logic will generate the LINE ZERO (LINE0-) pulse when the vertical group counter reaches zero. LINE0- resets the phase counter and the addressing cycle begins again.

Figure 24 is a timing diagram for an example addressing sequence. In this example the vertical group size is 4, so 2 lines are skipped on every address cycle.

HORIZONTAL ADDRESSING LOGIC

The horizontal addressing logic has six modules:

a. the horizontal accumulator,
b. the horizontal increment register,
c. the horizontal multiplexer,
d. the horizontal adder,
e. the horizontal counter, and
f. the frequency multiplier.

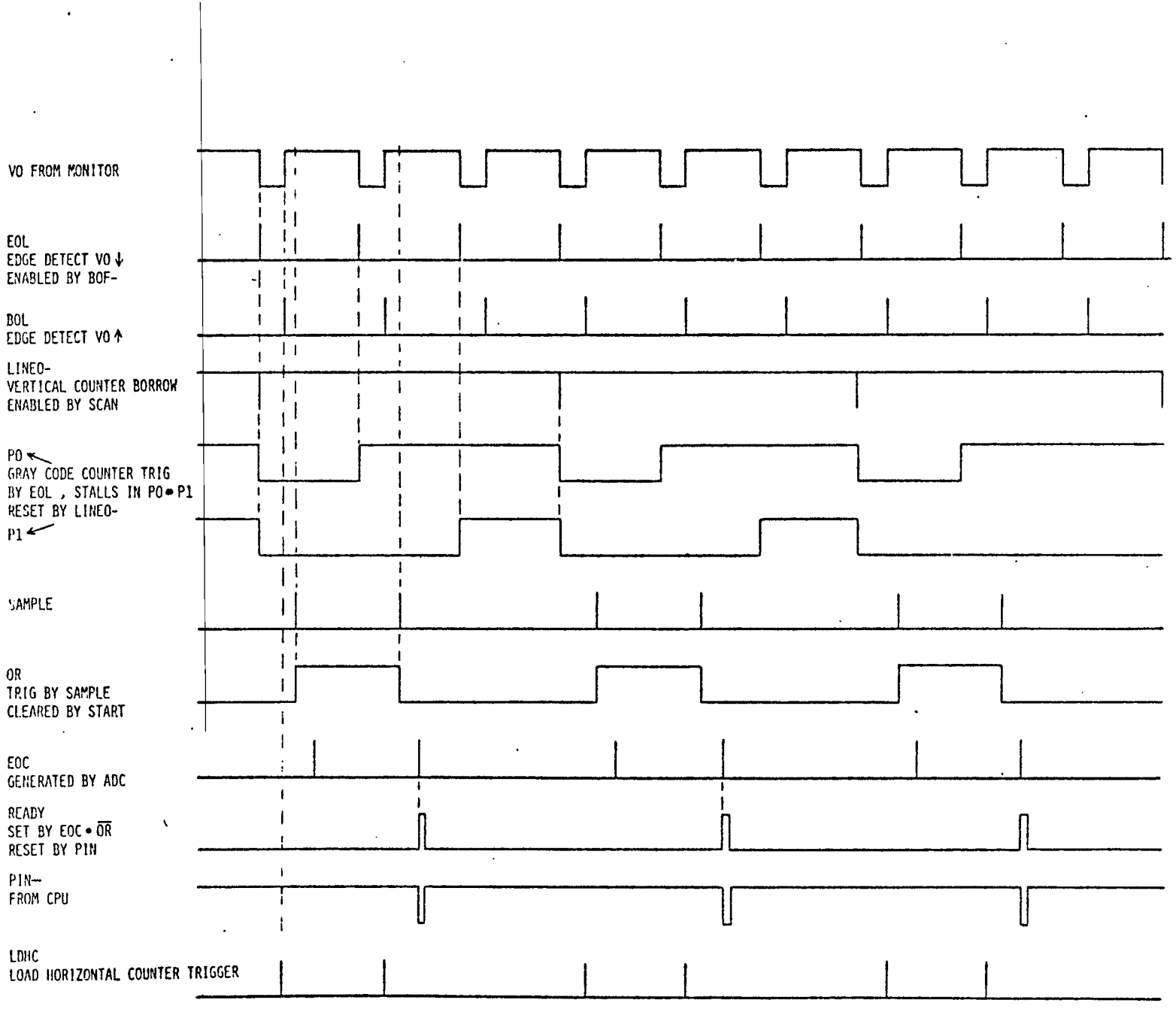


Figure 24
RUN SEQUENCE EXAMPLE

All modules of the horizontal addressing logic are constructed on a printed circuit card which plugs into slot 5 of the interface chassis.

Figure 25 is a schematic of the horizontal accumulator.The horizontal accumulator is a two port register. One port is tied to the interface data buss and is activated by the LVSR- pulse. The other port is tied to the output of the horizontal adder and is activated by the ADDER TO HORIZONTAL ACCUMULATOR (ADD - HA) pulse.

Figure 26 is a schematic of the horizontal increment register, horizontal adder, horizontal multiplexer, and horizontal counter.The horizontal increment register output is tied to one input of the horizontal adder and the horizontal accumulator output is tied to the other input of the horizontal multiplexer. P0, an output of the phase counter, determines which multiplexer input will be selected for loading into the horizontal counter. P0 is low during the first line of a group and the output of the horizontal accumulator will be gated to the counter. P0 is high during the second line of a group and the output of the adder will be gated to the counter. The horizontal accumulator always contains the address of the first point of a pair and the output of the adder is always the address of the second point of a pair.

The horizontal counter is implemented by the two 74193 counters at locations 16 and 18. The borrow output of the high order counter (HZERO-) goes high when the counter is loaded by the LDHC- pulse from the sequencer logic.When the HCENA line goes high, multiplied master oscillator pulses (MO3) decrement the counter until the count reaches zero. HZERO- falls at this point and triggers a video sample cycle. HZERO- also gates off the MO3 pulses and stops the counter.

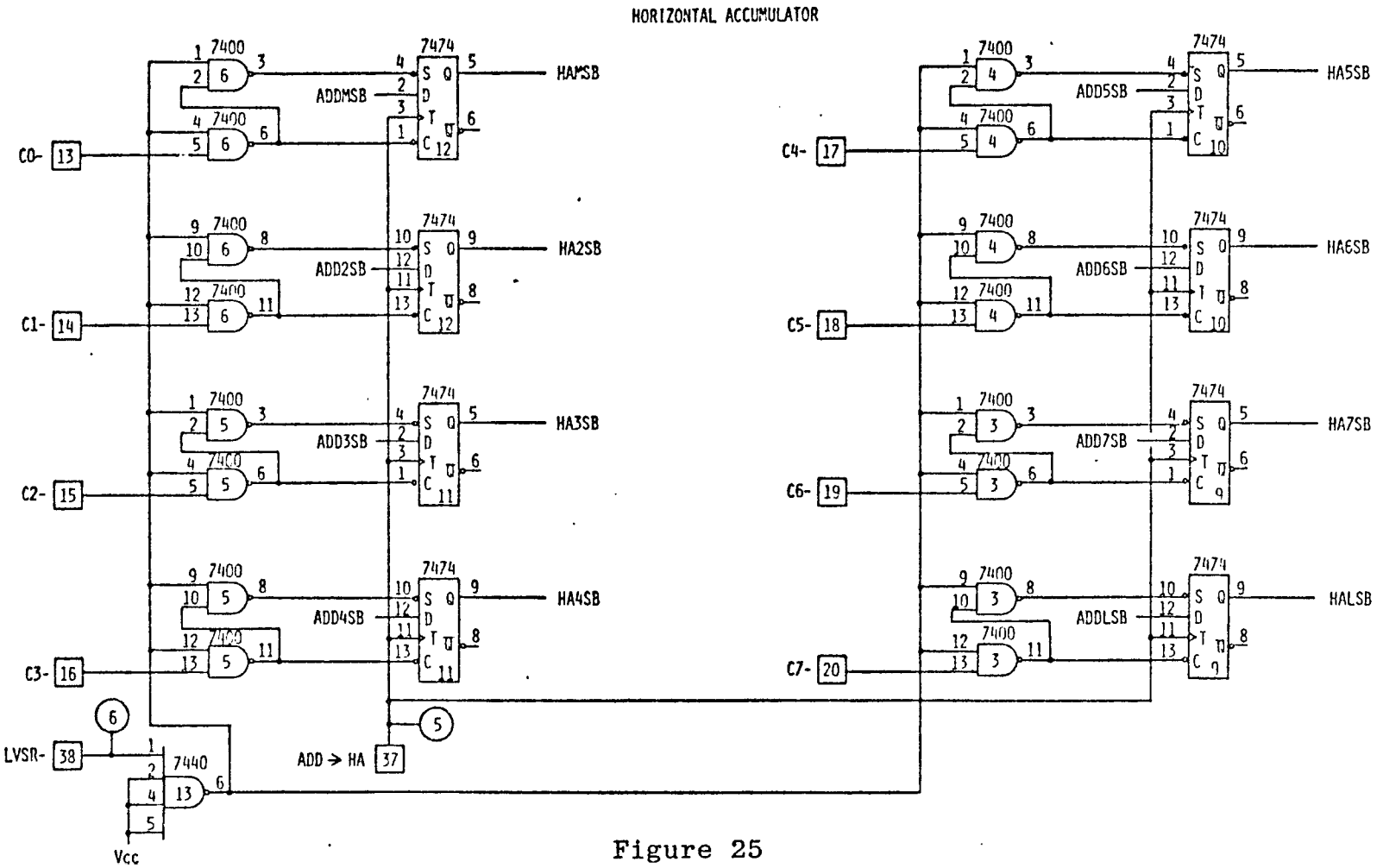

HORIZONTAL ACCUMULATOR
7400
7474
7440
HAMSB
HA2SB
HA3SB
HA4SB
HA5SB
HA6SB
HA7SB
HALSB
ADDMSB
ADD2SB
ADD3SB
ADD4SB
ADD5SB
ADD6SB
ADD7SB
ADDLSB
C0-
C1-
C2-
C3-
C4-
C5-
C6-
C7-
LVSR-
ADD → HA
Vcc

Figure 25

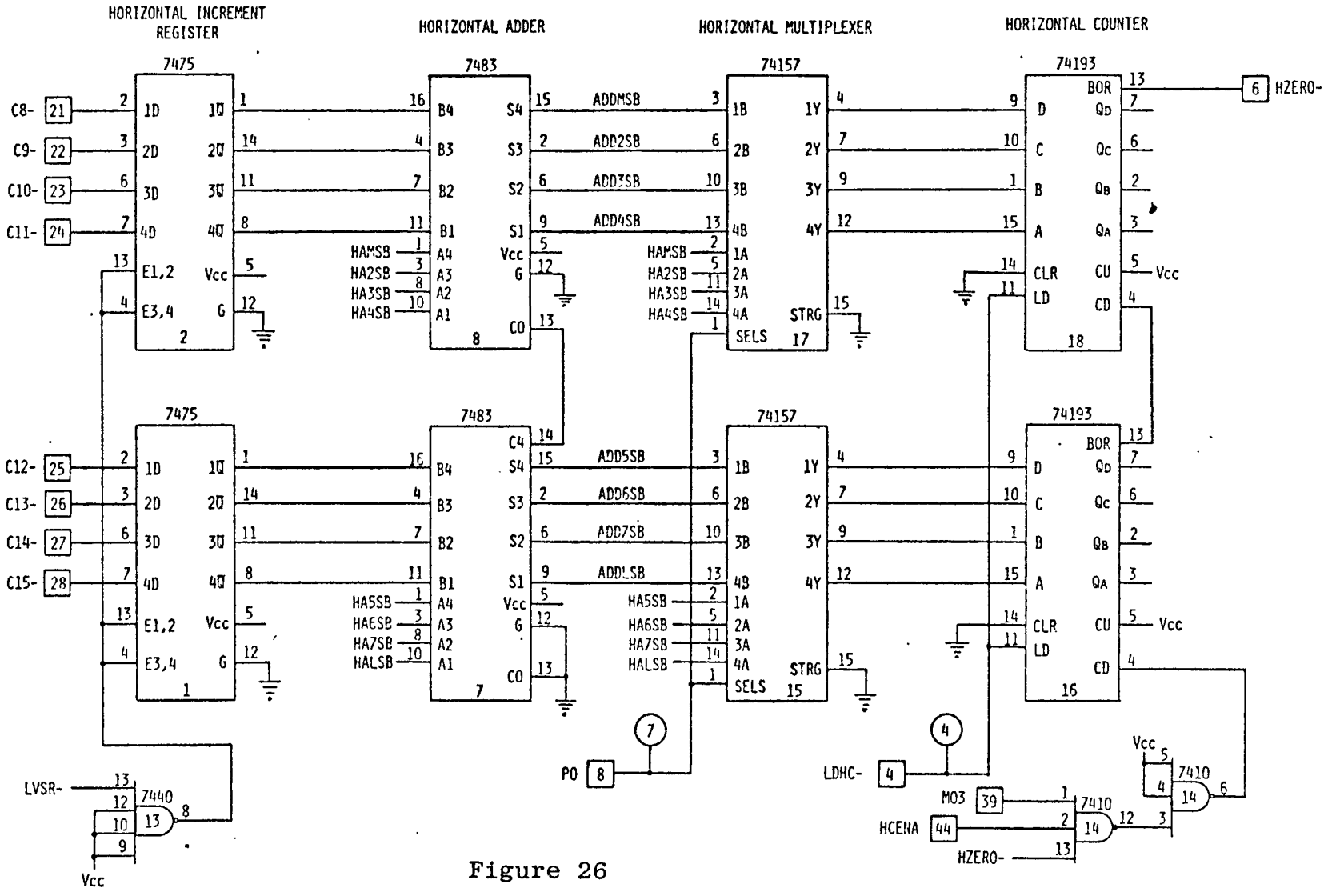

HORIZONTAL INCREMENT REGISTER
HORIZONTAL ADDER
HORIZONTAL MULTIPLEXER
HORIZONTAL COUNTER
7475
7483
74157
74193
C8-
C9-
C10-
C11-
C12-
C13-
C14-
C15-
1D
2D
3D
4D
1Q
2Q
3Q
4Q
E1,2
E3,4
Vcc
G
B4
B3
B2
B1
A4
A3
A2
A1
S4
S3
S2
S1
C0
C4
HAMSB
HA2SB
HA3SB
HA4SB
HA5SB
HA6SB
HA7SB
HALSB
ADDMSB
ADD2SB
ADD3SB
ADD4SB
ADD5SB
ADD6SB
ADD7SB
ADDLSB
1B
2B
3B
4B
1A
2A
3A
4A
1Y
2Y
3Y
4Y
SELS
STRG
BOR
D
C
B
A
CLR
LD
CU
CD
QD
QC
QB
QA
HZERO-
LVSR-
7440
PO
LDHC-
MO3
HCENA
7410
Vcc

Figure 26

FREQUENCY MULTIPLIER AND OSCILLATOR PHASE CONTROL

Figure 27 is a schematic of the frequency multiplier and oscillator phase control.The circuit is constructed on a printed circuit board which plugs into slot 3 of the interface chassis.

The NE562B phase locked loop circuit contains a phase comparator which is coupled to a voltage controlled oscillator (VCO). The phase comparator has two inputs. One input is coupled to the master oscillator of the television system (MO). The other input is coupled to a modulo 3 digital counter which is driven by the VCO output of the phase locked loop.In operation, the phase comparator compares the two inputs for exact coincidence. The phase comparator decreases the frequency of the VCO if the input coupled to the master oscillator is at a lower frequency than the signal coming from the output of the modulo 3 counter. Conversely, the phase comparator increases the frequency of the VCO if the master oscillator is running at a lower frequency than the signal coming from the modulo 3 counter. The net effect is that the loop stabilizes with the VCO output at three times the master oscillator frequency. The output of the VCO is coupled to the 74121 one-shot. The 74121 is adjusted to provide a square wave output. The PHASE signal from the scanner control selects the multiplied master oscillator (MO3) output to be in phase with the master oscillator or 180 degrees out of phase with the master oscillator. This part of the circuit provides the horizontal interlace capability.

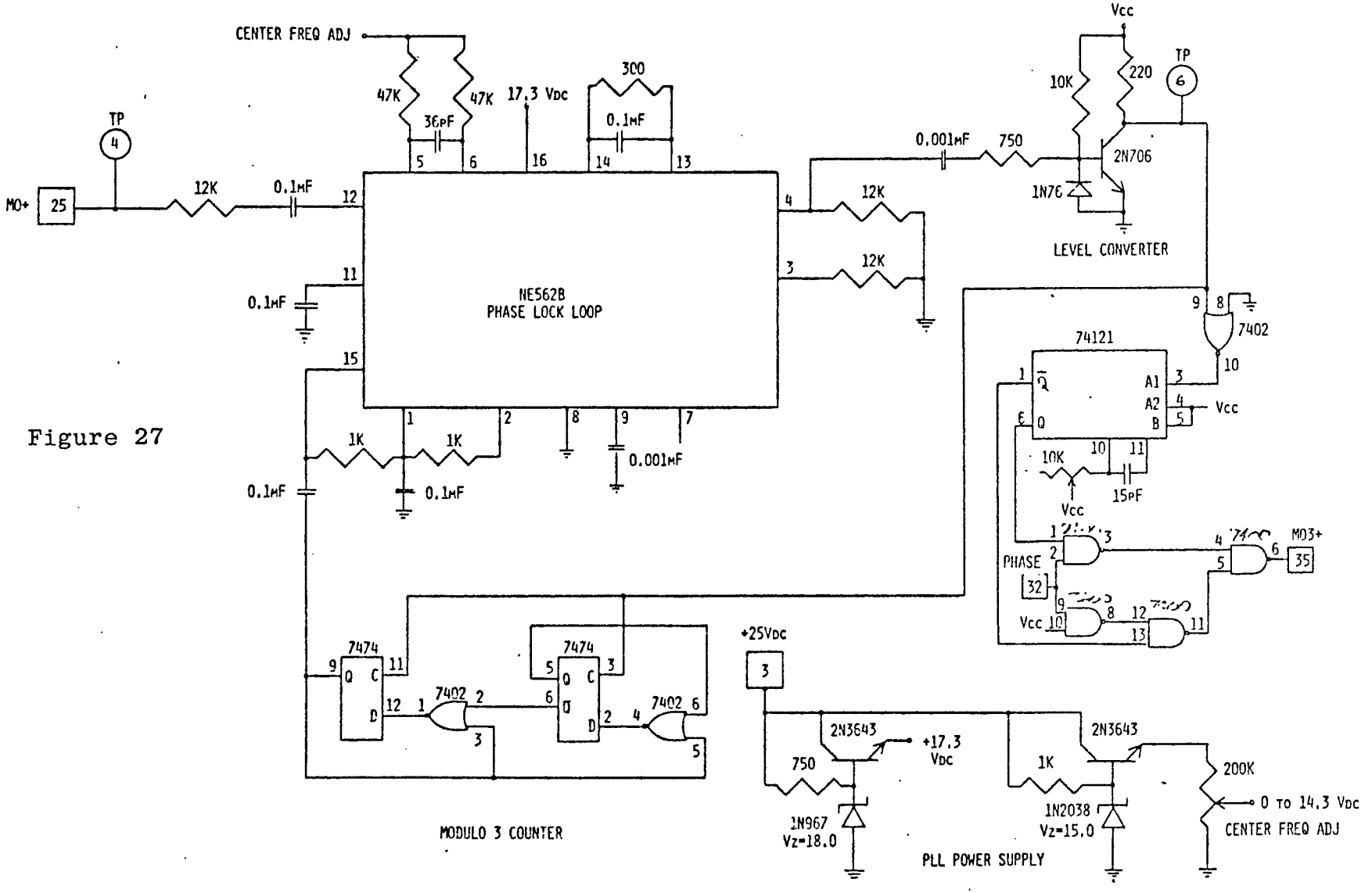

CENTER FREQ ADJ
47K
47K
36pF
17.3 Vdc
300
0.1mF
TP
4
MO+
25
12K
0.1mF
12
11
0.1mF
15
NE562B
PHASE LOCK LOOP
5
6
16
14
13
4
3
12K
12K
0.001mF
750
Vcc
10K
220
TP
6
2N706
1N76
LEVEL CONVERTER
9
8
7402
74121
10
1
A1
3
A2
4
B
5
Q
6
Vcc
10K
10
11
15pF
Vcc
PHASE
32
MO3+
35
Vcc
1K
1K
0.1mF
0.1mF
0.001mF
1
2
8
9
7
7474
9
Q
C
11
D
12
7402
2
3
7474
5
Q
C
3
D
2
7402
4
6
5
MODULO 3 COUNTER
+25Vdc
3
2N3643
+17.3
Vdc
750
1N967
Vz=18.0
2N3643
1K
1N2038
Vz=15.0
200K
0 to 14.3 Vdc
CENTER FREQ ADJ
PLL POWER SUPPLY

Figure 27

VERTICAL COUNT REGISTER AND COUNTER

Figure 28 is a schematic of the vertical count register and vertical group counter. The circuit is constructed on a printed circuit card which plugs into slot 6 of the interface chassis. The vertical count register is loaded with the number of lines in a group at the beginning of a scan. The vertical count register is implemented by the two 7475 latches at locations 2 and 3. The vertical counter is implemented by the two 74193 binary counters at locations 8 and 9. The vertical counter is loaded at every occurence of the LINE0- pulse. LINE0- is generated by the START pulse (from the start/end logic) or by the VZER0- pulse from the borrow output of the high order 74193 (location 9). The counter is continuously decremented by the EOL- pulses from the run sequencer for as long as the SCAN line is high. Since the counter is initialized by its own borrow output, it will generate LINE0- pulses as long as SCAN is high. The counter is disabled after SCAN goes down at the end of a pass and must then be restarted by the START pulse at the beginning of the next pass.

END-OF-PASS CALCULATION

Figure 29 is a timing diagram for the end-of-pass sequence generated by the start/end logic (see Figure 21). The computer generates the RTI pulse when it has input the last point pair of a pass. RTI generates the TERM- pulse which in turn resets the PIN20 flip-flop and the SCAN flip-flop. The scanner addressing logic and the run sequencer are disabled with SCAN and PIN20 down. The 7486 exclusive OR gate configuration generates a very narrow pulse at both edges of the RTI pulse. These two pulses are buffered by the 7440 NAND at location 9. The buffered output, ADD → HA, gates

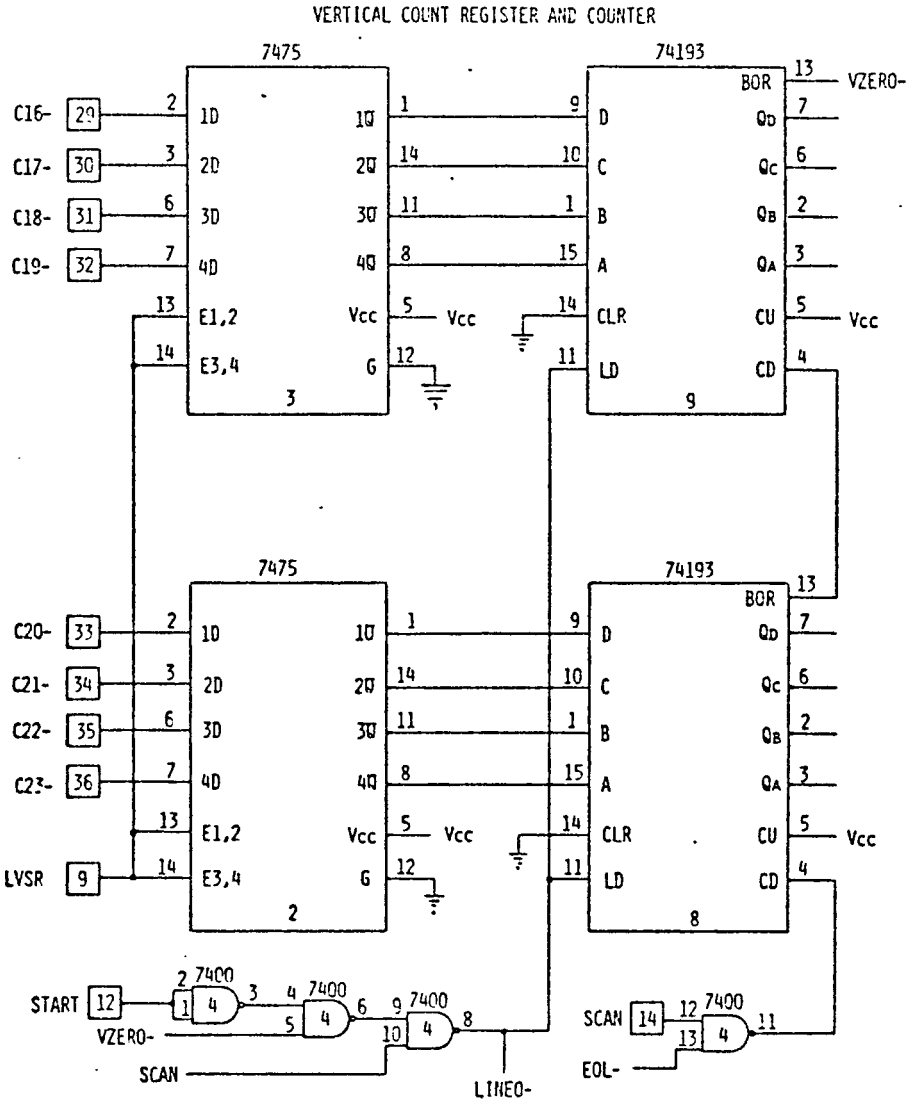
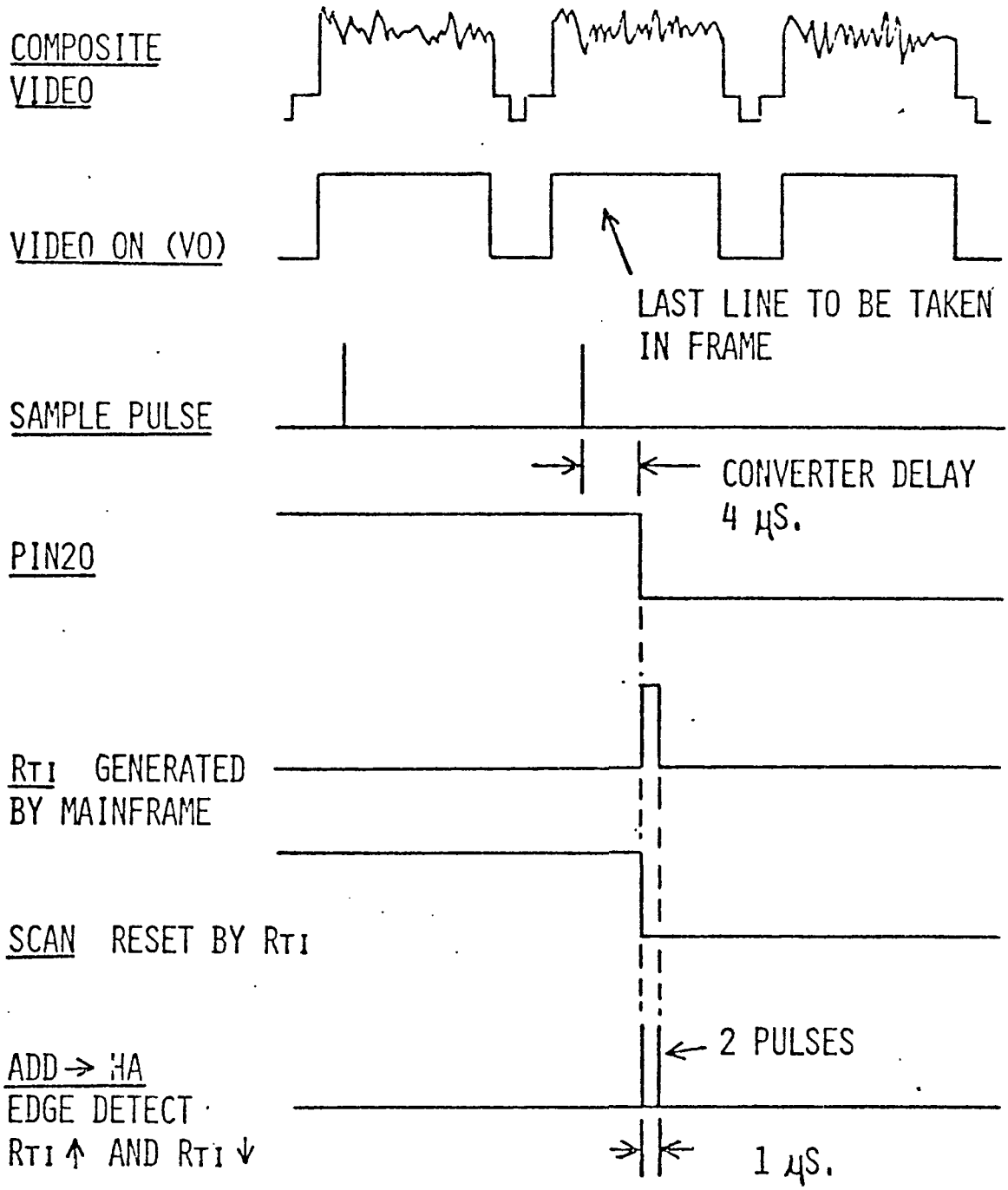

VERTICAL COUNT REGISTER AND COUNTER
7475
74193
C16-
C17-
C18-
C19-
C20-
C21-
C22-
C23-
LVSR
1D
2D
3D
4D
E1,2
E3,4
1Q
2Q
3Q
4Q
Vcc
G
D
C
B
A
CLR
LD
BOR
QD
QC
QB
QA
CU
CD
VZERO-
START
SCAN
EOL-
LINEO-
7400

Figure 28

Figure 29
END OF PASS TIMING SEQUENCE



the output of the adder into the horizontal accumulator twice in succession.This adds twice the horizontal increment to the original content of the accumulator . The new content of the accumulator is the horizontal address of the first point in a pair during the next pass.

CHAPTER VII

DESCRIPTION OF THE IMAGE DISPLAY SYSTEM

The image display system was constructed to provide a means of verifying the operation of the scanner. The display system allows the results of a scan to be displayed directly from the stored digital image so the user can get fast and easily interpreted feedback.The system uses a Tektronix Model 611 bistable storage monitor [8] as the display medium.

HORIZONTAL AND VERTICAL DEFLECTION

Horizontal and vertical deflection are accomplished with individual 8 bit digital-to-analog converters. Figure 31 is a schematic of the horizontal and vertical deflection section. The circuit is constructed on a printed circuit board which plugs into slot 8 of the interface chassis. DAC0 is the horizontal deflection converter and DAC1 is the vertical deflection converter. The 7475 latches are loaded from the interface data buss by the scanner control logic (see Chapter V).

VARIABLE INTENSITY SECTION

A third converter is used in conjunction with a pulse width modulator to provide variable intensity storage. Variable intensity is achieved by applying the modulated pulse output to the writing beam enable input of the bistabe storage monitor. Figure 32 is a schematic of the intensity converter. The circuit is constructed on a printed circuit board which plugs into slot 7 of the interface chassis. The 7474 flip-flops are loaded from the interface data buss on command from the scanner control logic. Figure 32 also shows the four drivers which implement the remote control of the ERASE, VIEW, NON-STORE, and WRITE THRU functions of the display monitor

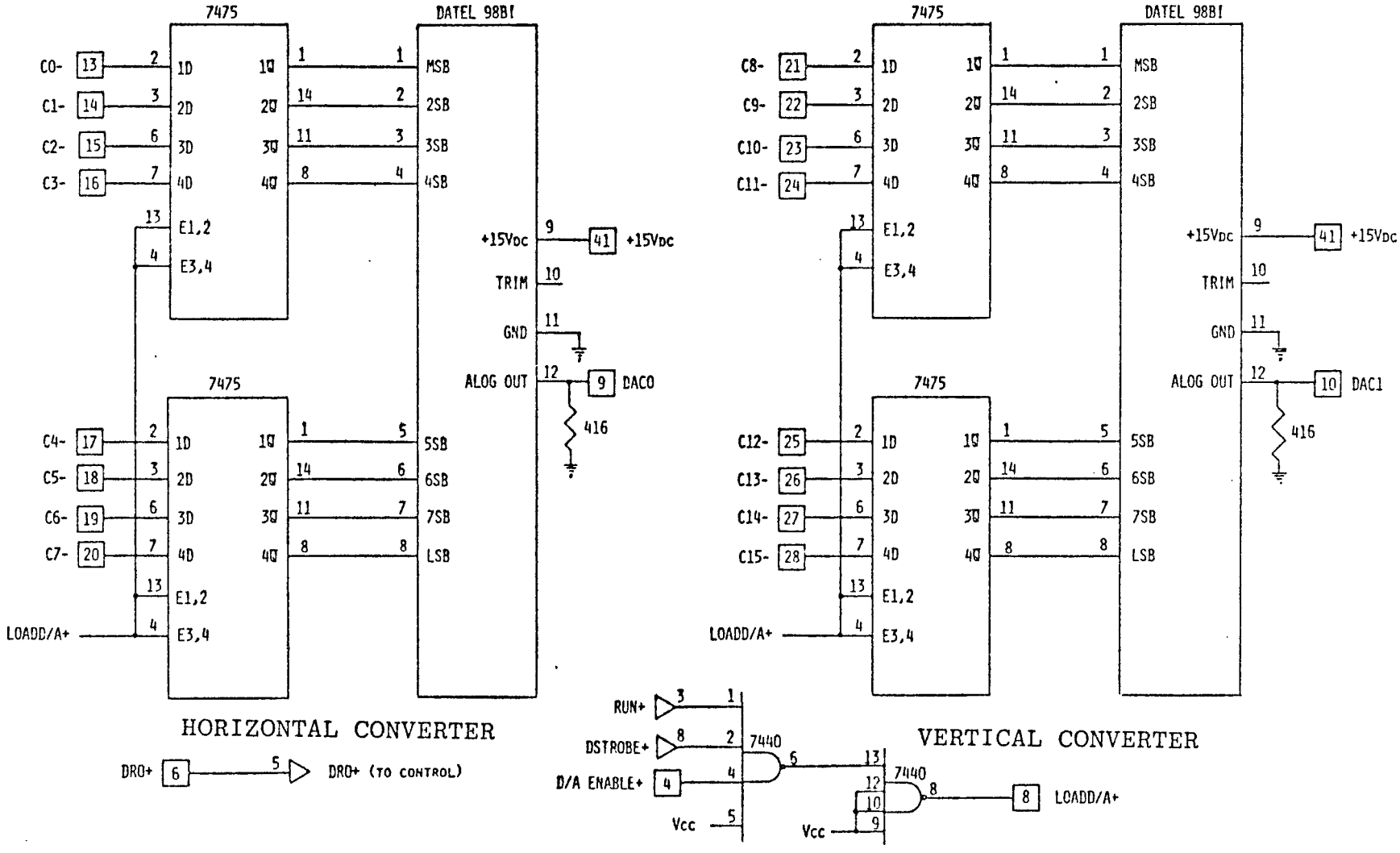
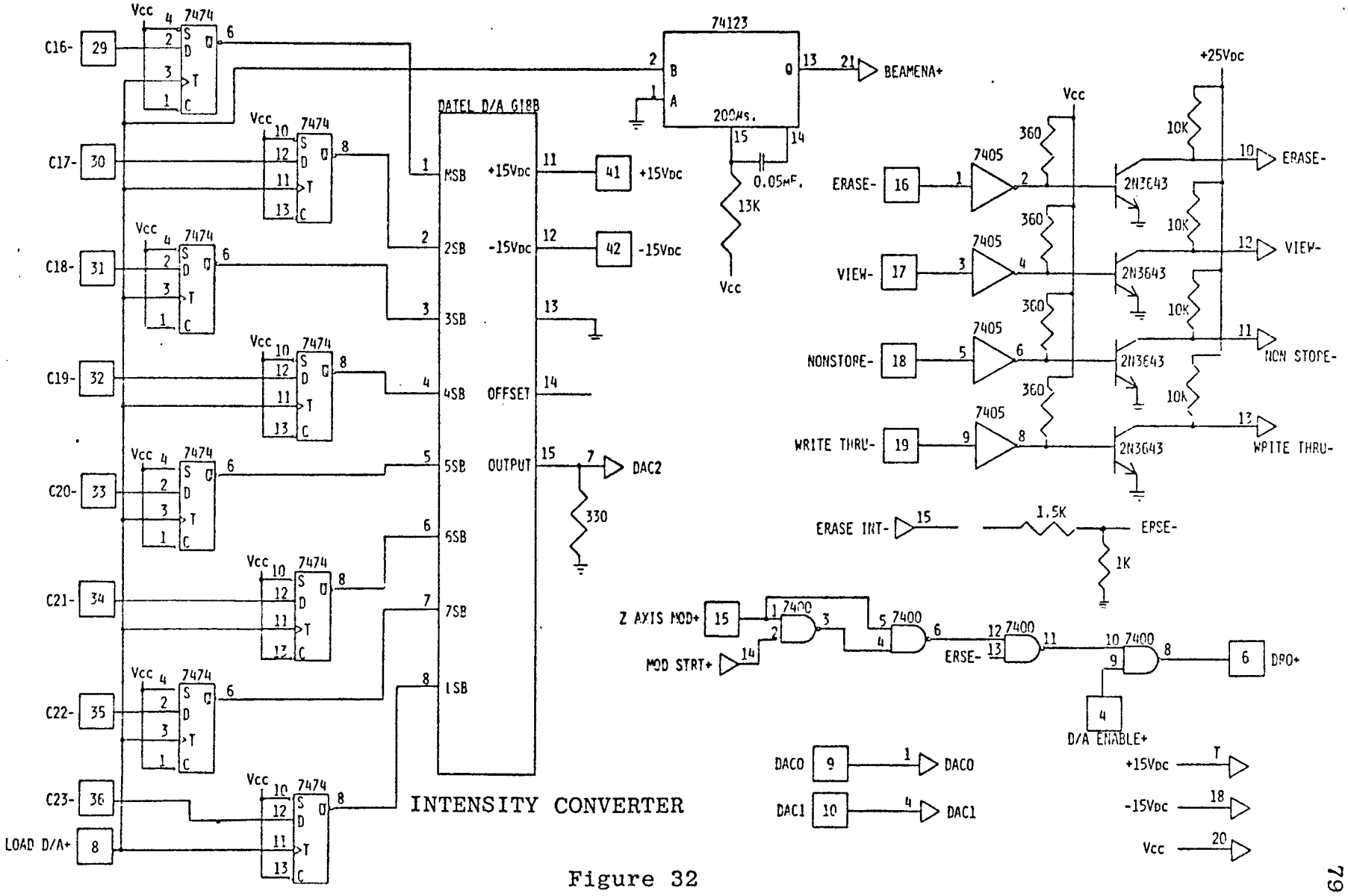

7475
DATEL 98BI
C0-
C1-
C2-
C3-
1D
2D
3D
4D
1Q
2Q
3Q
4Q
MSB
2SB
3SB
4SB
E1,2
E3,4
+15VDC
TRIM
GND
ALOG OUT
DAC0
416
C4-
C5-
C6-
C7-
5SB
6SB
7SB
LSB
LOADD/A+
HORIZONTAL CONVERTER
DRO+
DRO+ (TO CONTROL)
C8-
C9-
C10-
C11-
C12-
C13-
C14-
C15-
DAC1
RUN+
DSTROBE+
D/A ENABLE+
Vcc
7440
VERTICAL CONVERTER

Figure 31



INTENSITY CONVERTER

Figure 32

PULSE WIDTH MODULATOR

Figure 33 is a schematic of the pulse width modulator. The circuit is constructed in an enclosure which mounts in the television system control chassis. The modulator is a modified version of a circuit developed for slow scan reception of satelite pictures[11] . The modulator is capable of producing up to 256 different pulse widths, but the characteristics of the storage tube limit the perceivable intensity levels to about eight.

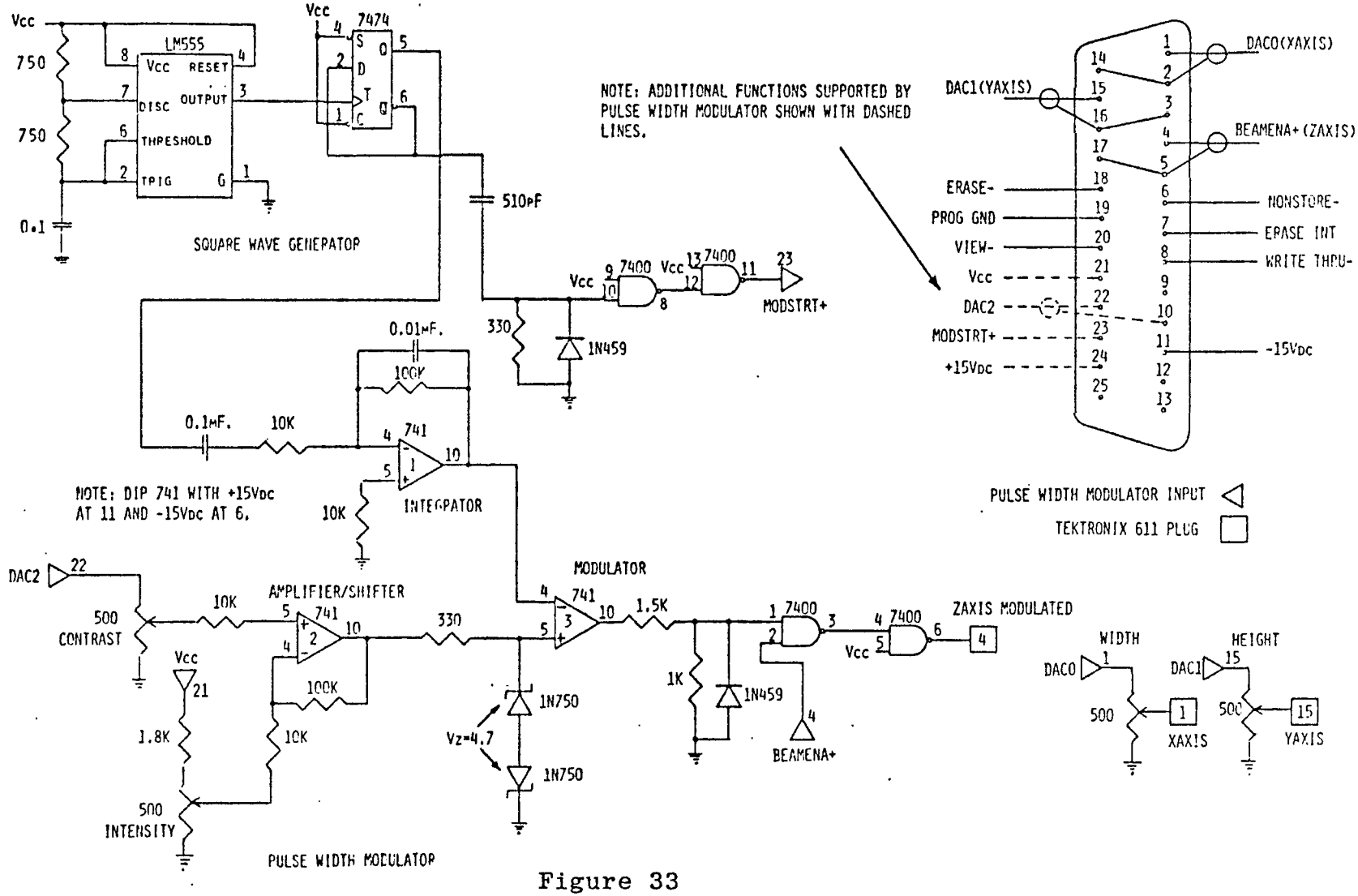

Vcc
750
750
0.1
LM555
Vcc
RESET
DISC
OUTPUT
THRESHOLD
TRIG
GND
SQUARE WAVE GENERATOR
7474
510pF
NOTE: ADDITIONAL FUNCTIONS SUPPORTED BY PULSE WIDTH MODULATOR SHOWN WITH DASHED LINES.
DAC1(YAXIS)
DAC0(XAXIS)
BEAMENA+(ZAXIS)
ERASE-
PROG GND
VIEW-
Vcc
DAC2
MODSTRT+
+15Vdc
NONSTORE-
ERASE INT
WRITE THRU-
-15Vdc
7400
MODSTRT+
330
1N459
0.01mF.
100K
0.1mF.
10K
741
INTEGRATOR
NOTE: DIP 741 WITH +15Vdc AT 11 AND -15Vdc AT 6.
PULSE WIDTH MODULATOR INPUT
TEKTRONIX 611 PLUG
DAC2
22
500
CONTRAST
10K
AMPLIFIER/SHIFTER
741
330
MODULATOR
741
1.5K
7400
ZAXIS MODULATED
Vcc
21
1.8K
100K
10K
500
INTENSITY
1N750
Vz=4.7
1N750
1K
1N459
BEAMENA+
WIDTH
HEIGHT
DAC0
DAC1
500
XAXIS
500
YAXIS
PULSE WIDTH MODULATOR

Figure 33

CHAPTER VIII
SOFTWARE CONSIDERATIONS FOR THE VIDEO SCANNER AND DISPLAY SYSTEMS

A basic software operating system was written for the video scanner and display system to aid in initial testing and evaluation. The software allows the operator to enter commands through the teletype keyboard to perform such functions as : scan an image into memory, display an image from memory, save an image on paper tape, or reset the hardware. The software package is an independent unit, but may be used in conjunction with the SDS Basic Utility Package (BUP) for convenience. All programming was done in SDS92 SYMBOL assembler language [7].

STRUCTURE

The operating system consists of a main program and several subroutine modules. The main program is the keyboard command decoder. Once a command has been decoded, the main program calls on an appropriate subroutine (command processor) to perform the indicated function or, if the command is not recognized, prints an error message '*ERROR' and waits for another command. The message 'READY' and a prompt character '>' are printed when the system is ready for another command.

COMMANDS

The commands implemented by the operating system are listed below.

COMMAND	PROCESSOR	RESULTS
CNTL	BUP	branches to location 045 in the

COMMAND	PROCESSOR	RESULTS
		SDS92 Basic Utility Package. This command was implemented as a convenience when checking out the software system.
DISP	DISPLAY	outputs a stored image to the display screen.
ERSE	ERASE	erases the display screen.
HOLD	HOLD	places the display device in hold mode.
MTST	MTEST	outputs an eight level test pattern to the display screen to help the operator to adjust the modulator controls.
PRNT	PRINT	prints a representation of a stored image on the teletype.
PNCH	PUNCH	punches a stored image to paper tape.
READ	READ	reads a punched image back into memory.
RSET	RESET	resets the hardware, erases the display screen, and places the software system in low resolution mode.
SCAN	SCAN	scans an image into memory. If low resolution mode is in effect (SRLO or RSET) a 128 x 128 image is scanned in. If high resolution mode is in effect (SRHI) , half of a 256 x 256 image is scanned in.
SRHI	SRHI	sets the software system to high resolution (256 x 256) mode.

COMMAND	PROCESSOR	RESULTS
SRLO	SRLO	sets the software system to low resolution (128 x 128) mode.
VIEW	VIEW	places the display device in view mode.

Note that even though the hardware is capable of any scan resolution in the range from 2 x 2 to 256 x 256 , the basic operating system implements only two resolutions, 128 x 128 and 256 x 256. Also note that only one half of a 256 x 256 image can be contained in memory with the software system resident. This last limitation is taken into consideration by the software and when in high resolution mode one half of the image is scanned or displayed alternately.

CONFIGURATION AND USE

The software system is supplied in three forms: symbolic, relocateable load modules, and BUP compatible. All three forms are on seven level paper tape.

In order to use the system, it must be loaded into memory in one of two ways. The system may be loaded by using the SDS92 Relocating Loader (QUBLDR) to load, relocate, and cross link each module. This is a time consuming process and should be used only when changes have been made to one of the modules. Once the system is loaded in this manner, it is ready for use; however, it is recommended that the modules be loaded and cross linked starting at address 03400 or higher so that the BUP may subsequently be loaded into memory between addresses 0 and 03400. Once the BUP is loaded, it may be used to punch out an absolute paper tape of the whole

software system. The tape produced by BUP can be loaded by BUP or by any of the several basic relocating bootstrap loaders.

FLOWCHARTS

Flowcharts of the software system are given in Appendix D.

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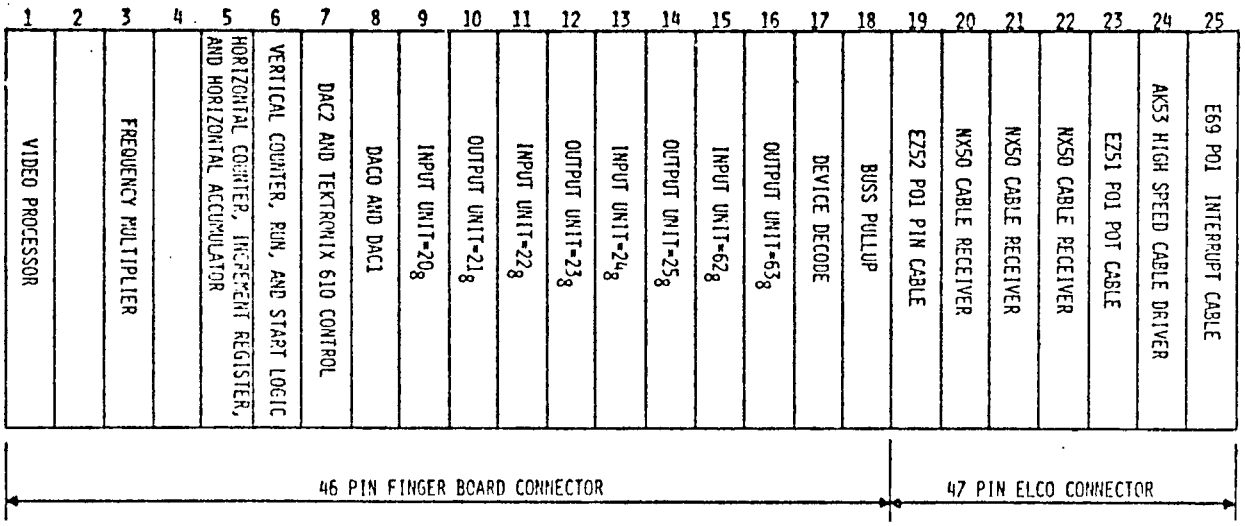
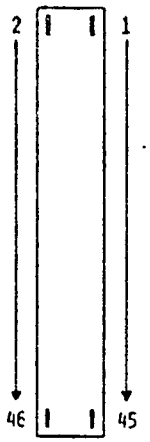
1. SDS Model 92 Computer Reference Manual, Scientific Data Systems, Palo Alto California, 1964.
2. TTL Data Book for Design Engineers, Texas Instruments, Inc., 1973.
3. Operating and Maintenance Manual for 6100 Series Television Cameras, COHU Electronics, Inc., 1969.
4. Operating and Maintenance Instructions for High Resolution Monochrome Television Camera Controls, COHU Electronics, 1969.
5. Operating and Maintenance Manual for Variable Scan Rate Sync Generators, COHU Electronics, 1969.
6. Installation and Operating Instructions for Conrac Television Monitor Model CQF, Conrac, Inc., Corvina California, 1965.
7. SDS SYMBOL Assembler Language Reference Manual, Scientific Data Systems, Inc., 1965.
8. Tektronix Model 611 Storage Display Monitor Operating and Maintenance Manual, Tektronix, Inc., Portland, Oregon, 1972.
9. "Datel Model SHM-2 Sample and Hold",applications literature, Datel Systems, Inc., 1973.
10. "Datel Model ADC-EH Analog-to-Digital Converter",applications literature, Datel Systems, Inc.,1973.
11. "Displaying Gray Scale Images on Bistable Storage Tubes", Burns, T.J. and G.E. Walker, Electronics , November 22,1973, p. 132.

APPENDIX A
PHYSICAL LOCATION DIAGRAMS

SLOT LAYOUT VIDEO SCANNER CHASSIS

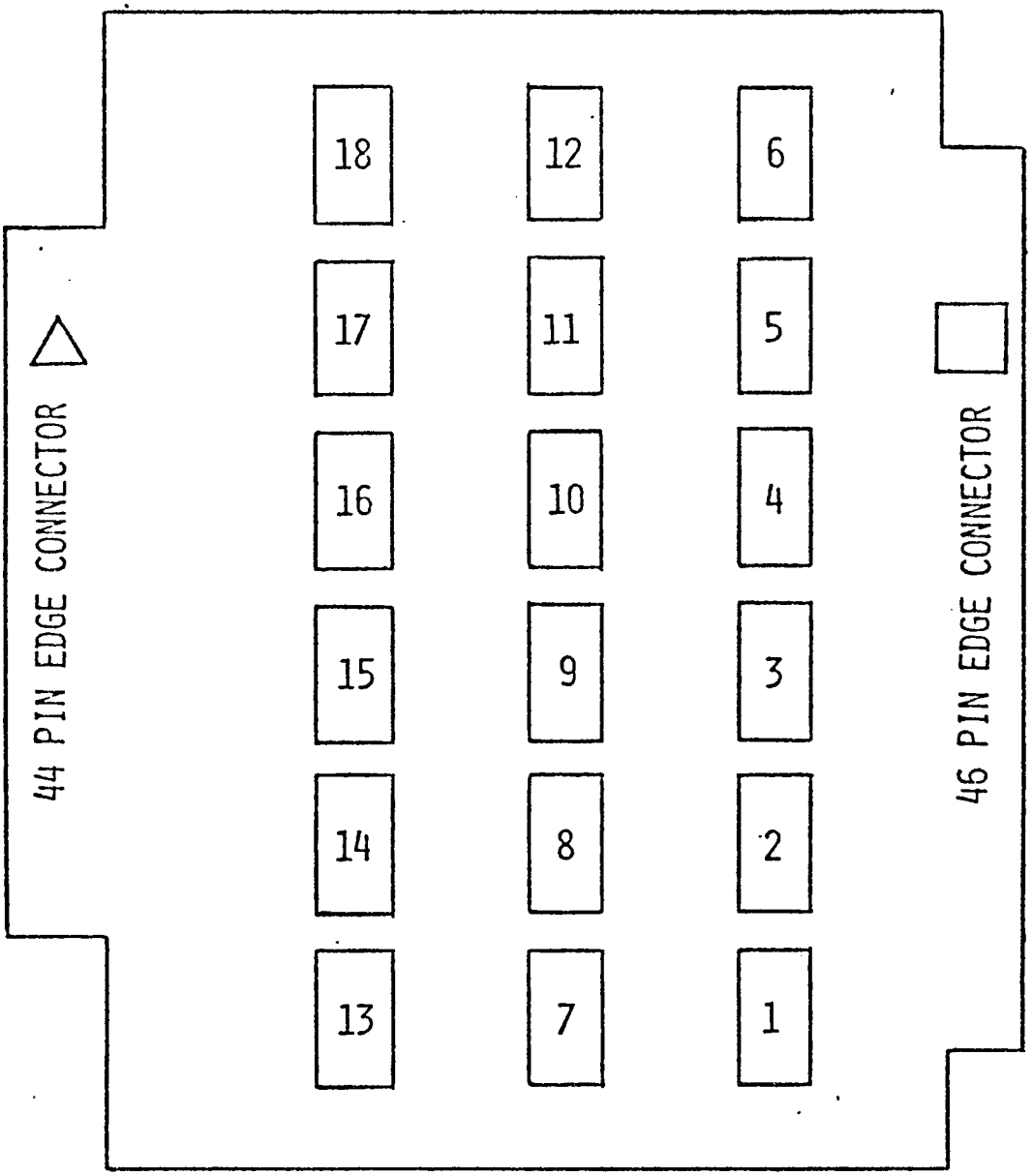




46 PIN FINGERBOARD CONNECTOR
PIN SIDE VIEW

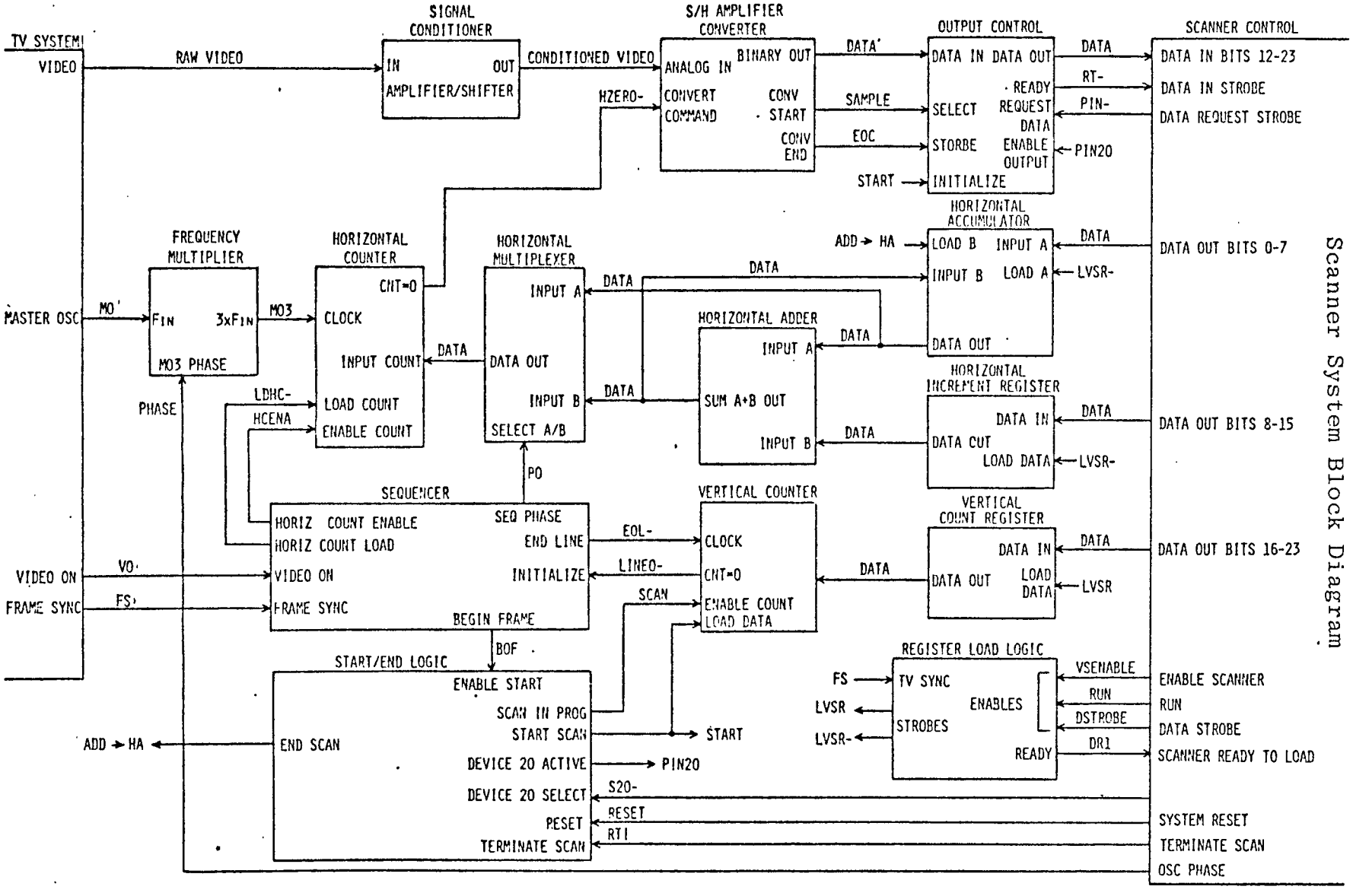
NOTE: PINS 1 AND 2 AT Vcc
PINS 45 AND 46 AT GND
PINS 3 - 44 CIRCUIT

COMPONENT NUMBERING

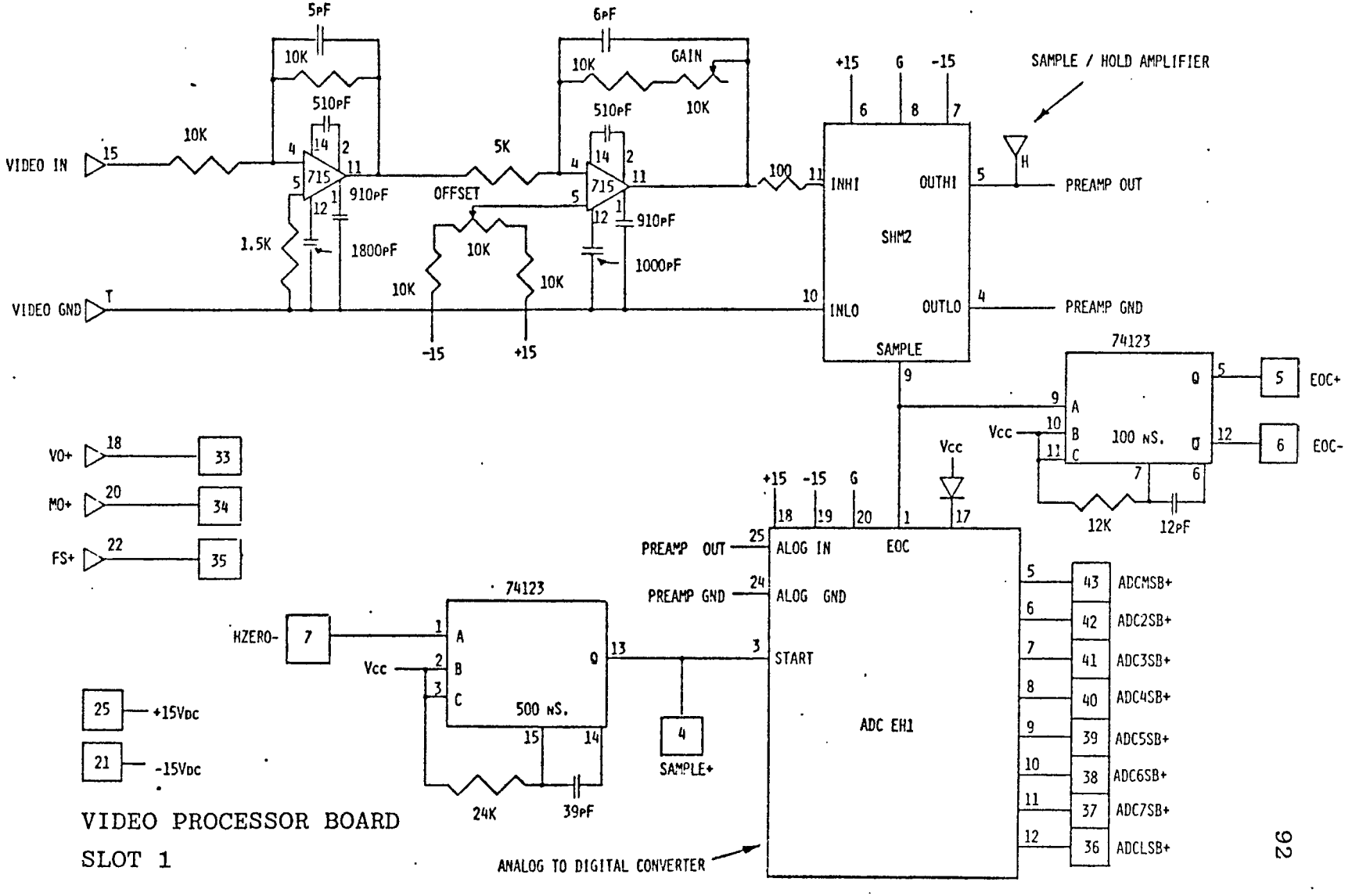


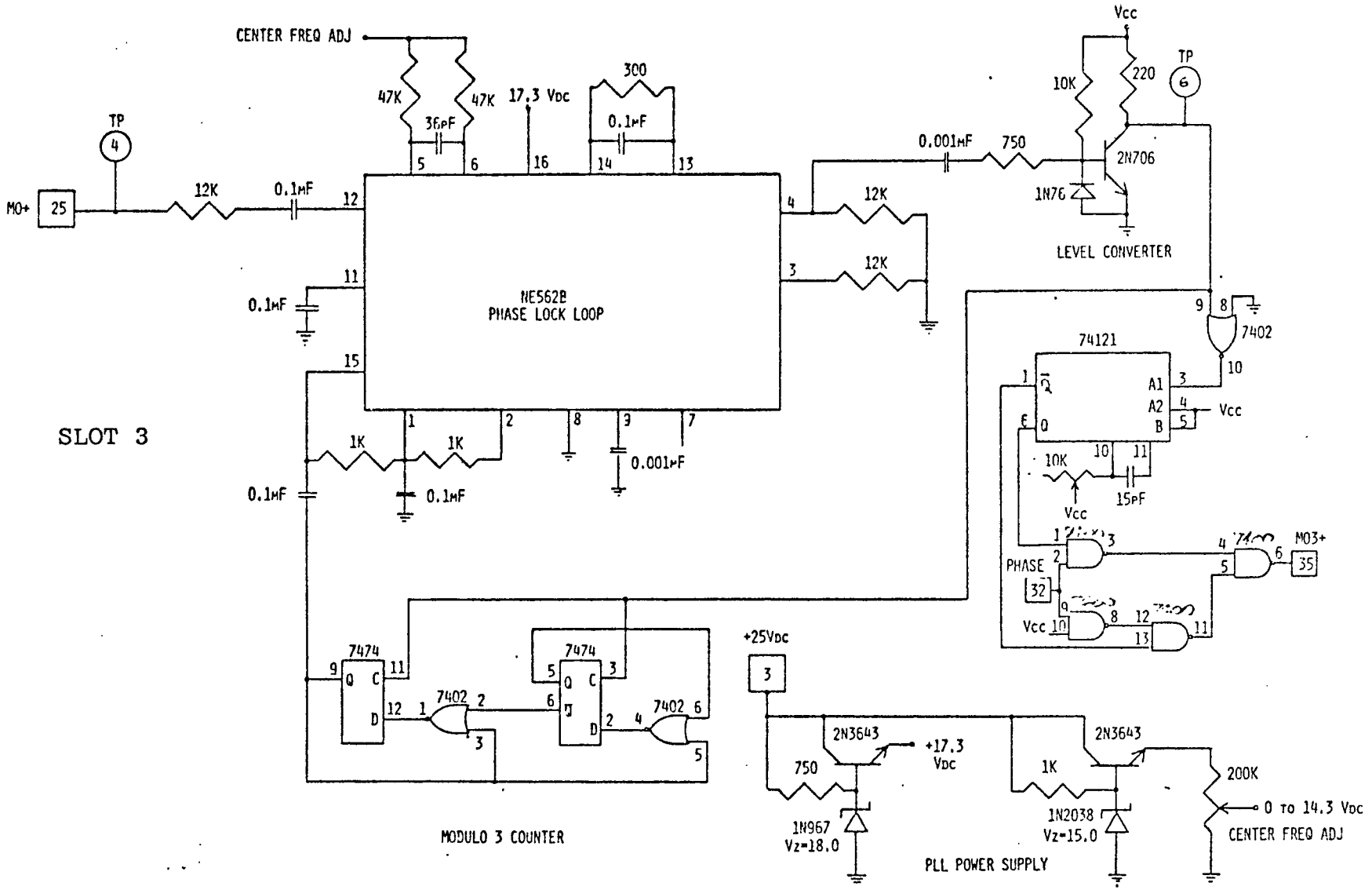
COMPONENT SIDE VIEW

APPENDIX B
CIRCUIT DIAGRAMS

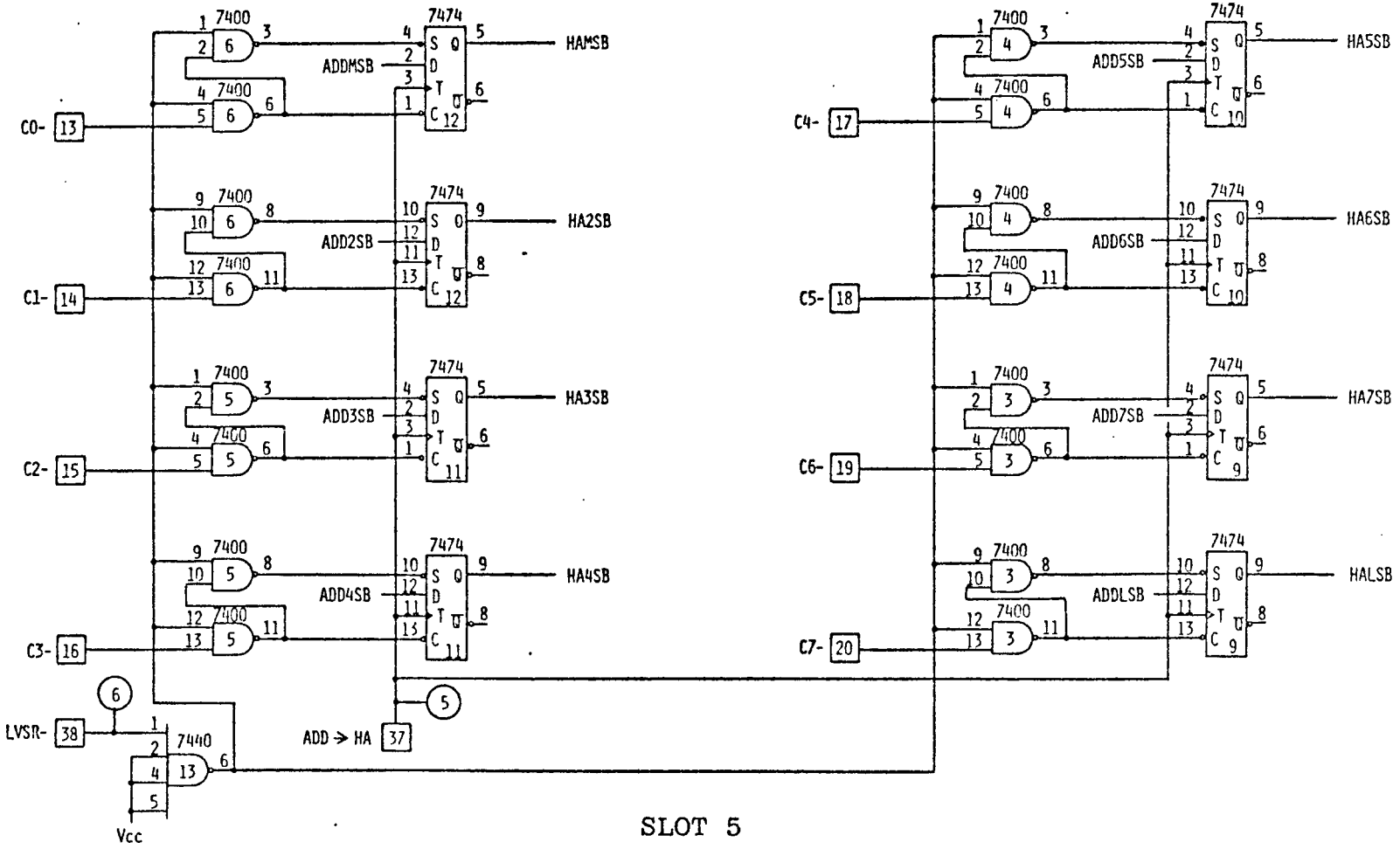


Scanner System Block Diagram

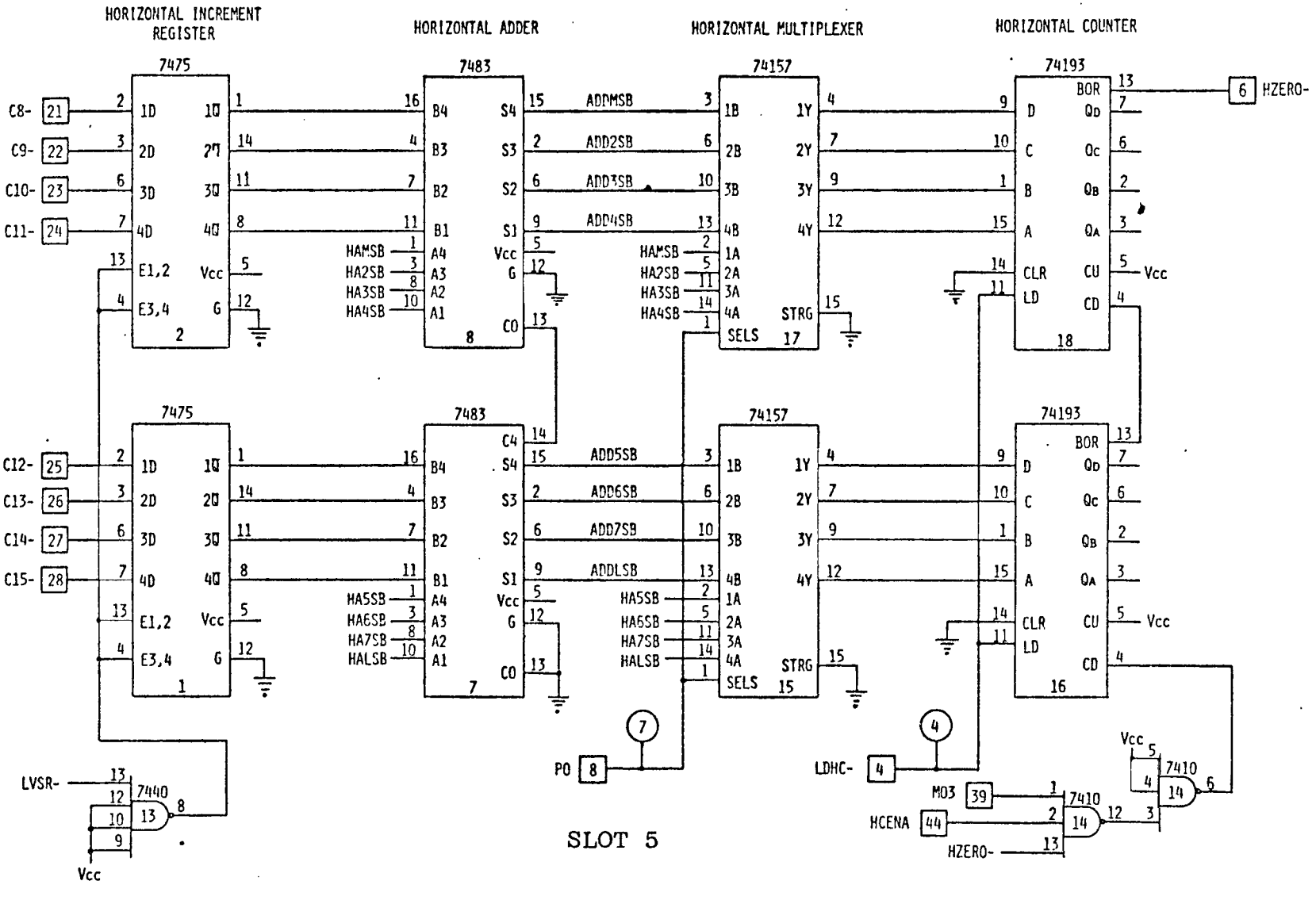

NOTE: DIP PACKAGE 715 WITH +15VDC AT PIN 13 AND -15VDC AT PIN 10.
VIDEO PROCESSOR BOARD
SLOT 1
SAMPLE / HOLD AMPLIFIER
VIDEO IN
VIDEO GND
PREAMP OUT
PREAMP GND
SHM2
INHI
OUTHI
INLO
OUTLO
SAMPLE
OFFSET
GAIN
5PF
6PF
10K
510PF
910PF
1800PF
1000PF
1.5K
5K
100
74123
100 NS.
500 NS.
12K
12PF
24K
39PF
EOC+
EOC-
VO+
MO+
FS+
HZERO-
+15VDC
-15VDC
SAMPLE+
ADC EH1
ALOG IN
ALOG GND
START
EOC
PREAMP OUT
PREAMP GND
ADCMSB+
ADC2SB+
ADC3SB+
ADC4SB+
ADC5SB+
ADC6SB+
ADC7SB+
ADCLSB+
ANALOG TO DIGITAL CONVERTER


SLOT 3
CENTER FREQ ADJ
47K
47K
36pF
17.3 Vdc
300
0.1mF
TP
4
MO+
25
12K
0.1mF
NE562B
PHASE LOCK LOOP
0.1mF
1K
1K
0.1mF
0.001mF
0.001mF
750
Vcc
10K
220
TP
6
2N706
1N76
LEVEL CONVERTER
12K
12K
74121
7402
10K
15pF
PHASE
32
MO3+
35
7474
7474
7402
7402
MODULO 3 COUNTER
+25Vdc
3
2N3643
2N3643
750
+17.3 Vdc
1K
200K
0 to 14.3 Vdc
CENTER FREQ ADJ
1N967
Vz=18.0
1N2038
Vz=15.0
PLL POWER SUPPLY

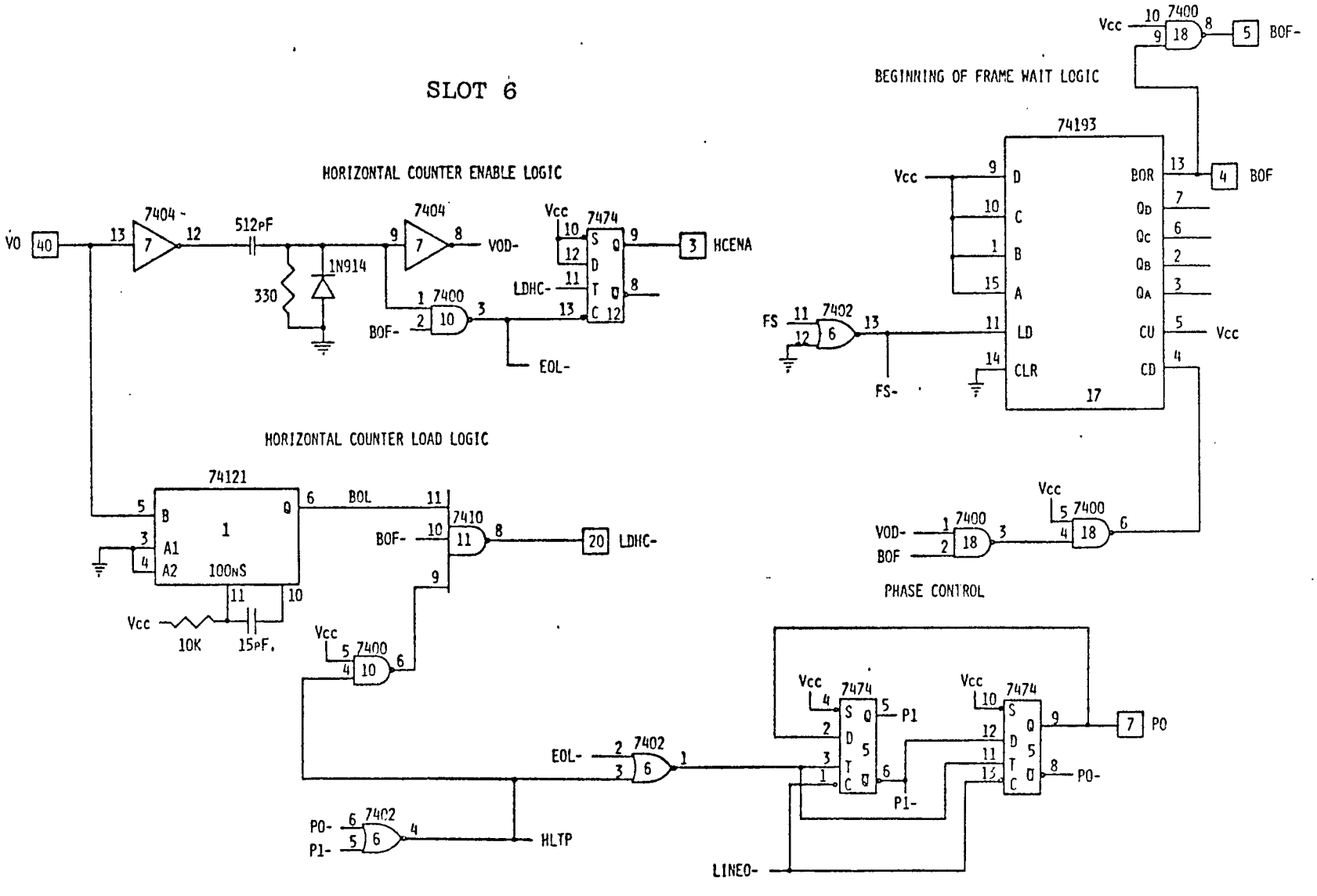
HORIZONTAL ACCUMULATOR



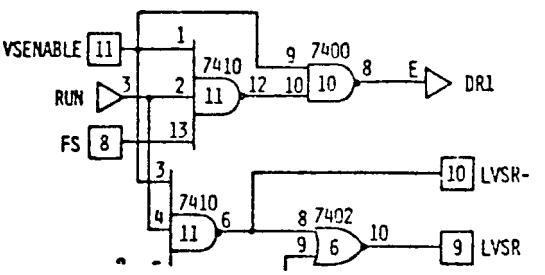
SLOT 5


HORIZONTAL INCREMENT REGISTER
HORIZONTAL ADDER
HORIZONTAL MULTIPLEXER
HORIZONTAL COUNTER
7475
7483
74157
74193
C8-
C9-
C10-
C11-
C12-
C13-
C14-
C15-
HAMSB
HA2SB
HA3SB
HA4SB
HA5SB
HA6SB
HA7SB
HALSB
ADDMSB
ADD2SB
ADD3SB
ADD4SB
ADD5SB
ADD6SB
ADD7SB
ADDLSB
HZERO-
Vcc
LVSR-
7440
PO
LDHC-
M03
HCENA
7410
SLOT 5

SLOT 6

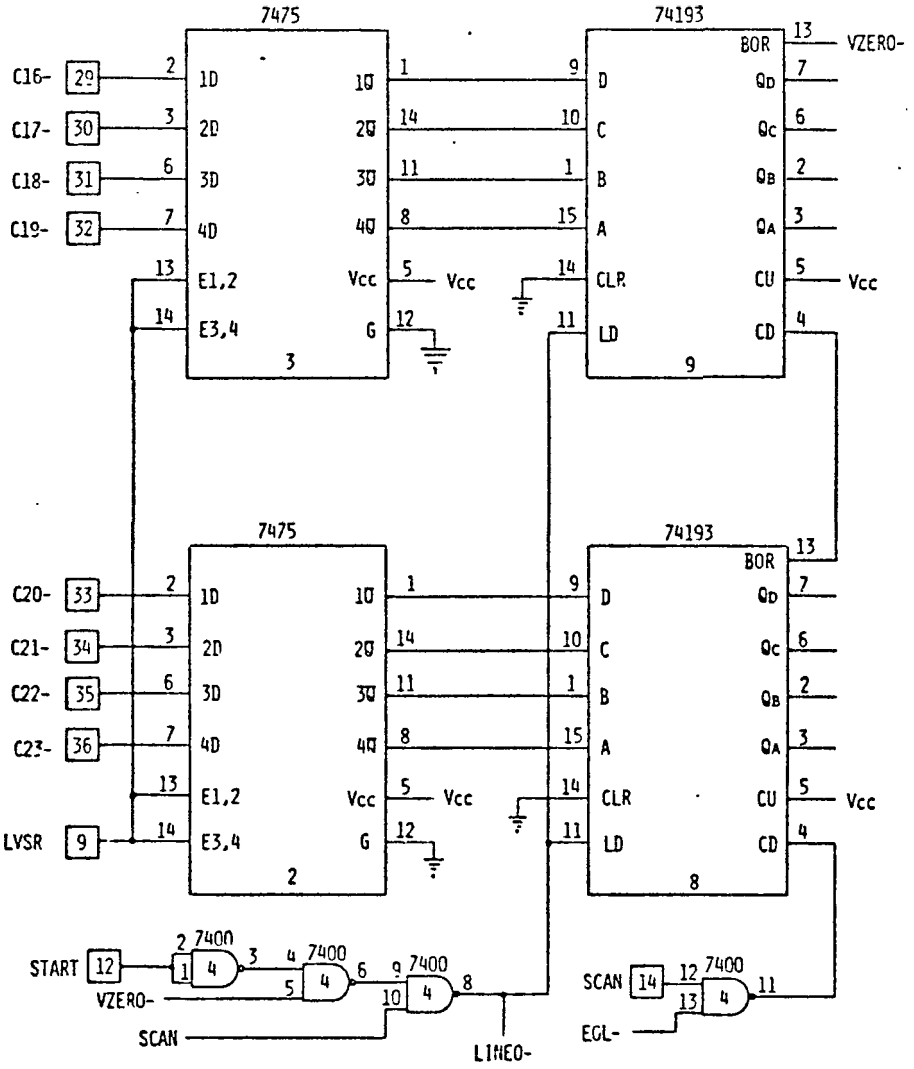

HORIZONTAL COUNTER ENABLE LOGIC
VO
40
7404
512pF
1N914
330
VOD-
7474
HCENA
LDHC-
7400
BOF-
EOL-
BEGINNING OF FRAME WAIT LOGIC
74193
Vcc
BOF-
BOF
FS
7402
FS-
CU
CD
HORIZONTAL COUNTER LOAD LOGIC
74121
BOL
7410
LDHC-
10K
15pF.
100NS
PHASE CONTROL
P1
P0
P1-
P0-
HLTP
LINEO-

REGISTER LOAD LOGIC

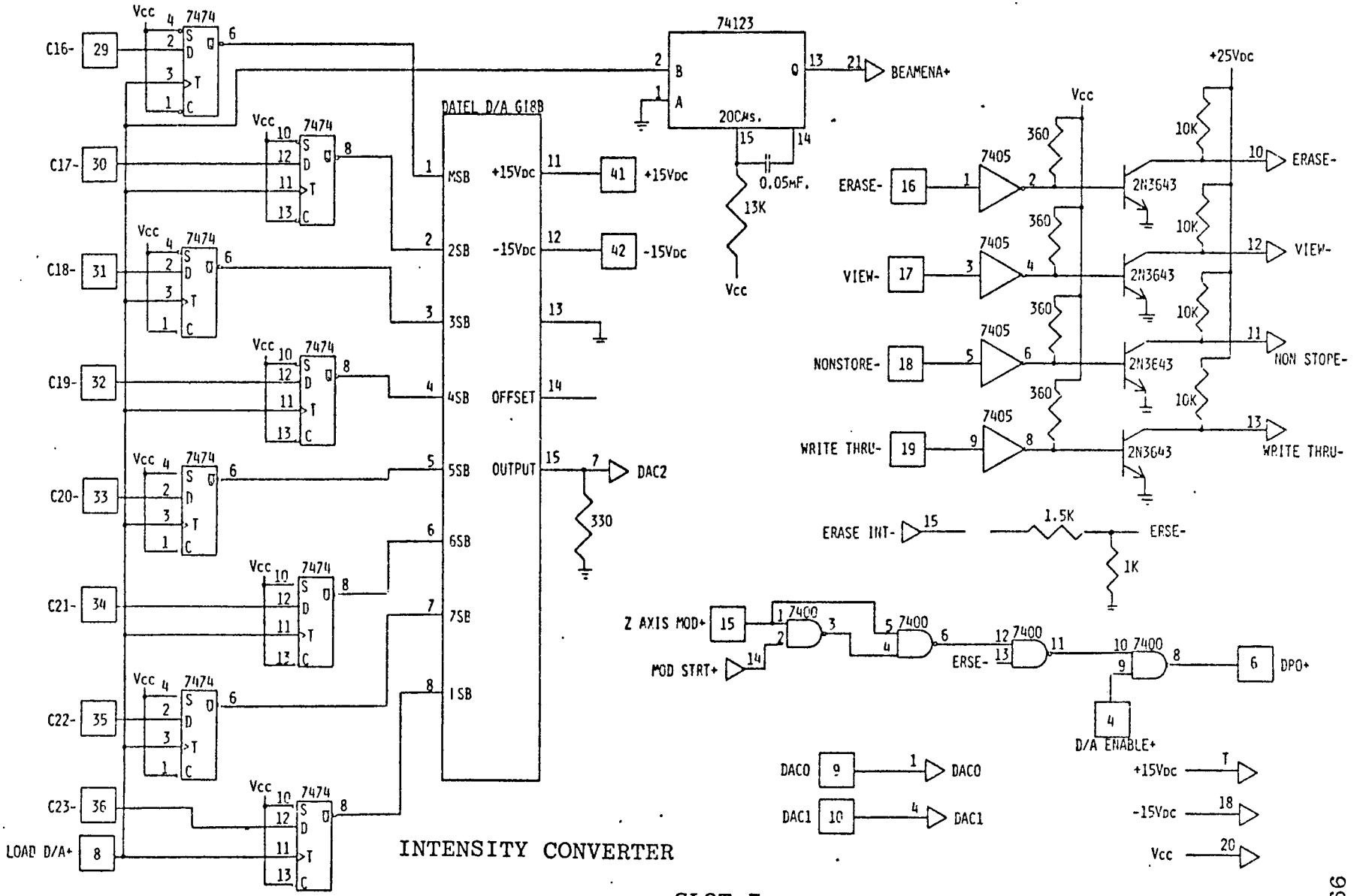


SLOT 6

VERTICAL COUNT REGISTER AND COUNTER

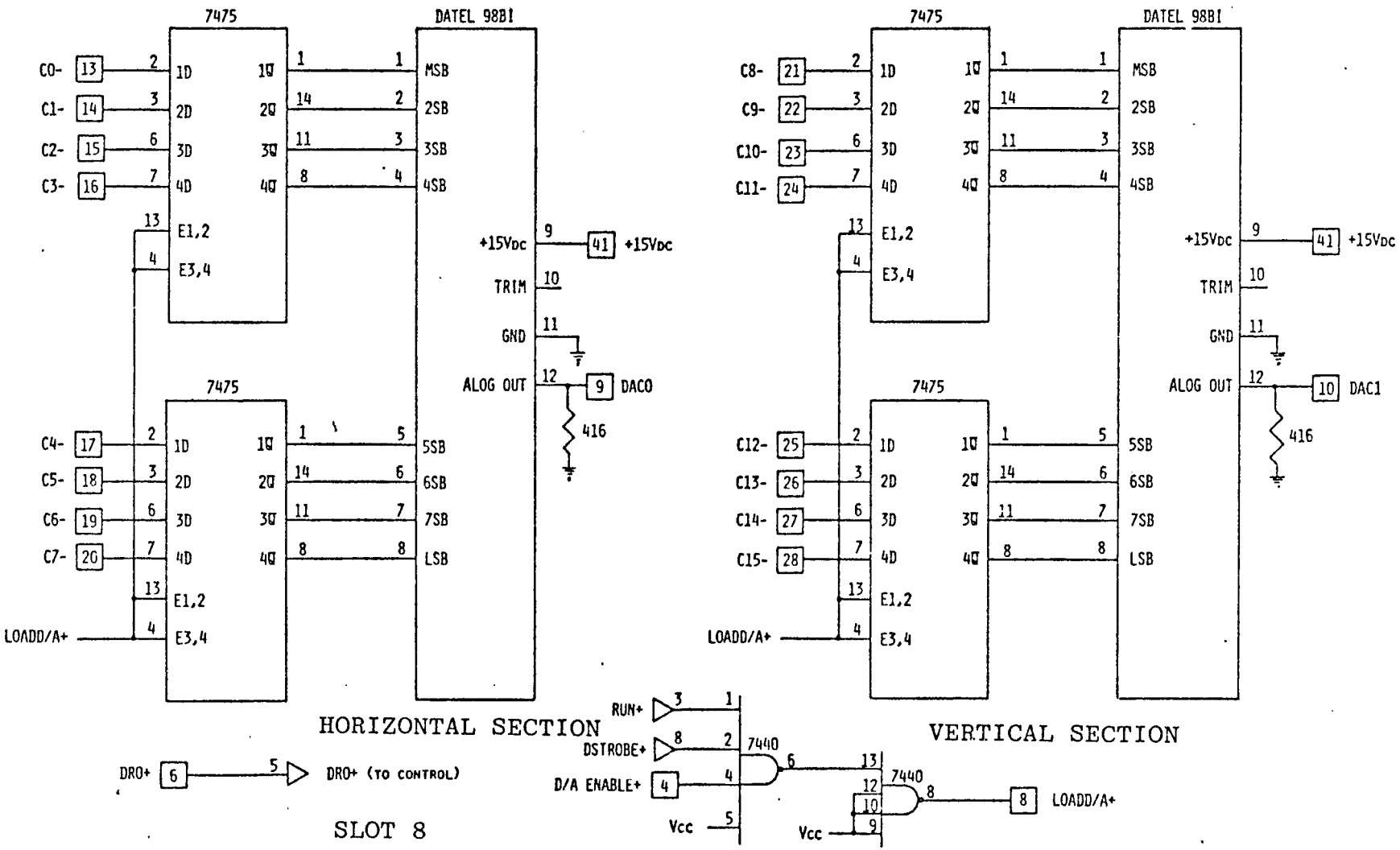


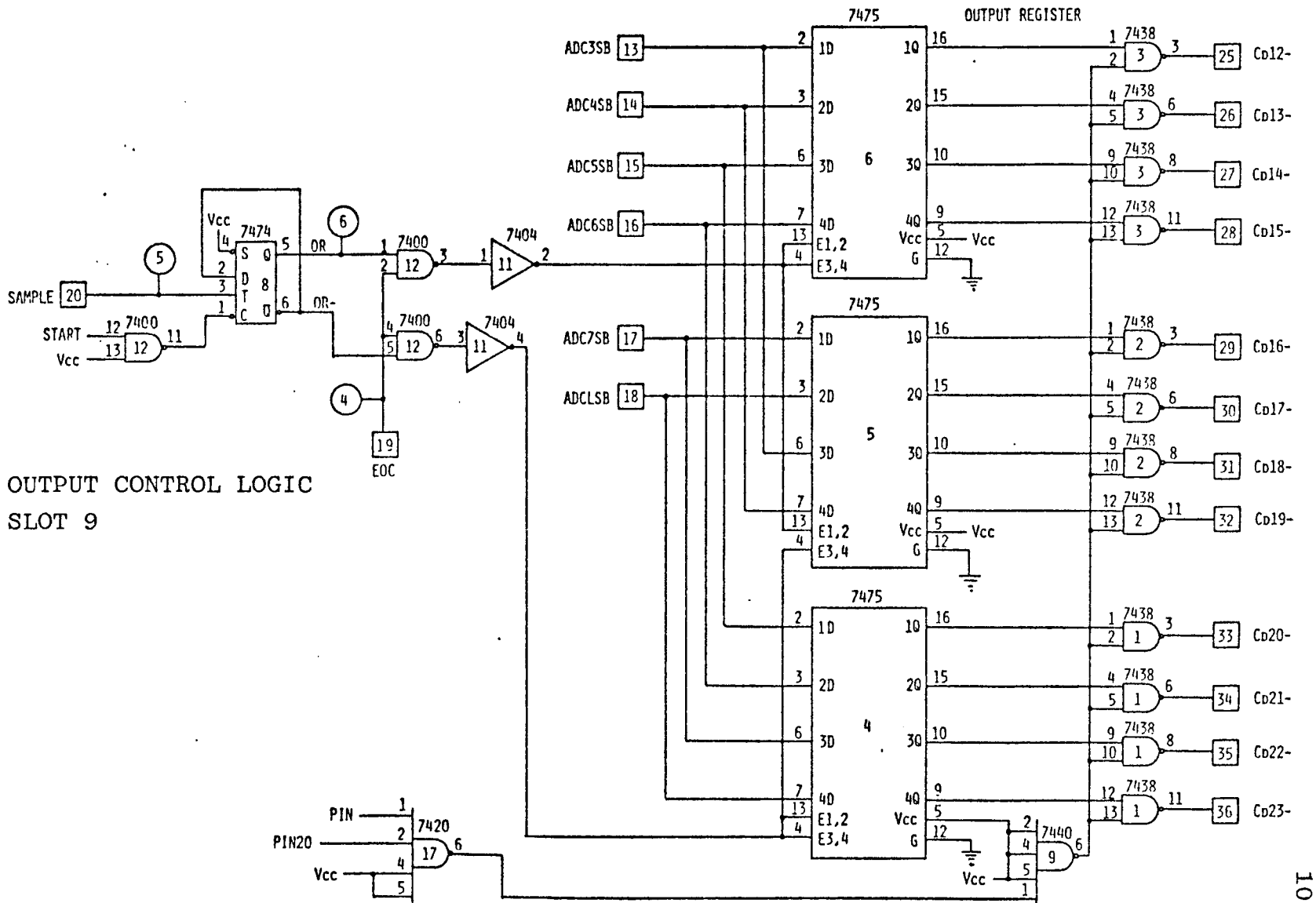
SLOT 6



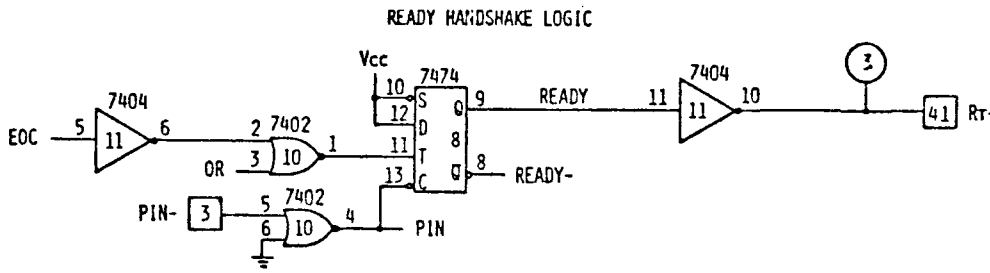
INTENSITY CONVERTER

SLOT 7

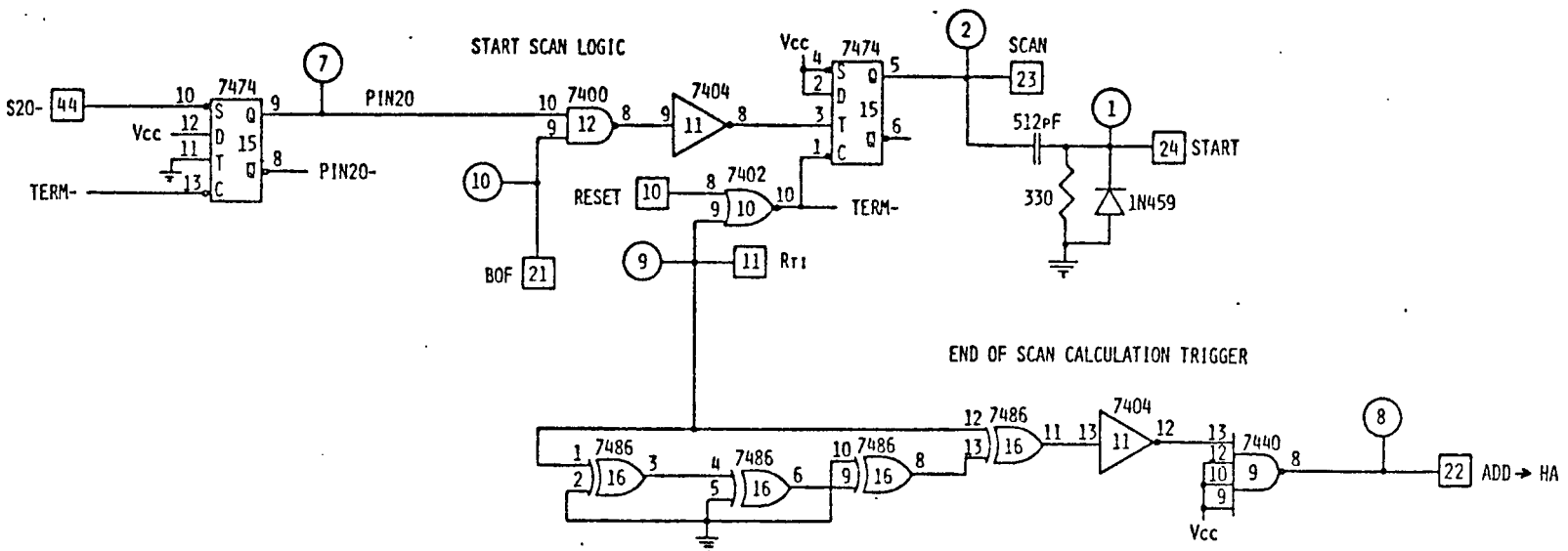

7475
DATEL 98BI
C0-
C1-
C2-
C3-
1D
2D
3D
4D
1Q
2Q
3Q
4Q
E1,2
E3,4
MSB
2SB
3SB
4SB
+15VDC
TRIM
GND
ALOG OUT
DAC0
416
C4-
C5-
C6-
C7-
5SB
6SB
7SB
LSB
LOADD/A+
C8-
C9-
C10-
C11-
DAC1
C12-
C13-
C14-
C15-
HORIZONTAL SECTION
VERTICAL SECTION
DRO+
DRO+ (TO CONTROL)
SLOT 8
RUN+
DSTROBE+
D/A ENABLE+
Vcc
7440



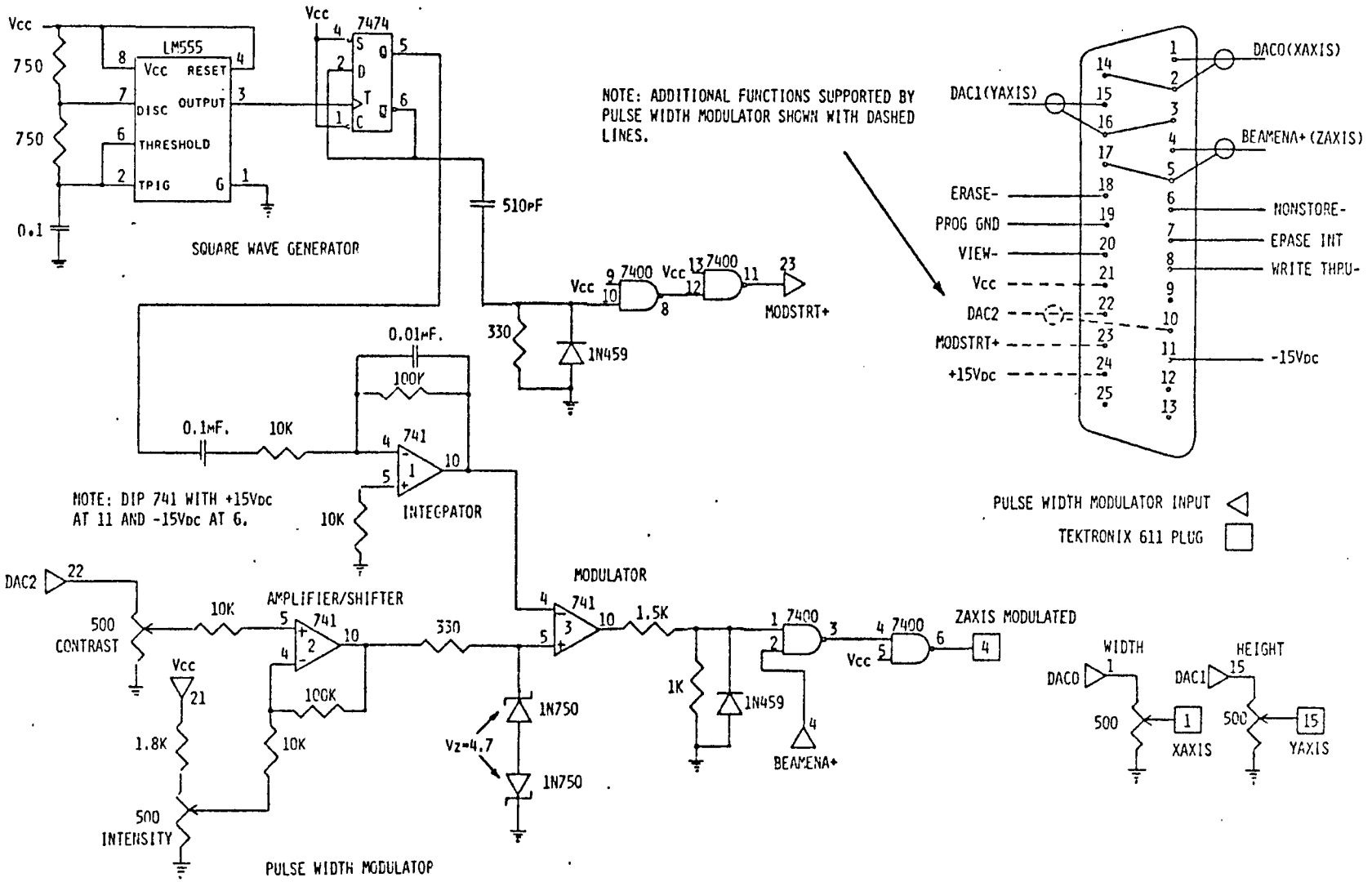
OUTPUT CONTROL LOGIC
SLOT 9


READY HANDSHAKE LOGIC
Vcc
7404
7474
7404
7402
7402
EOC
OR
PIN-
PIN
READY
READY-
Rt-

SLOT 9

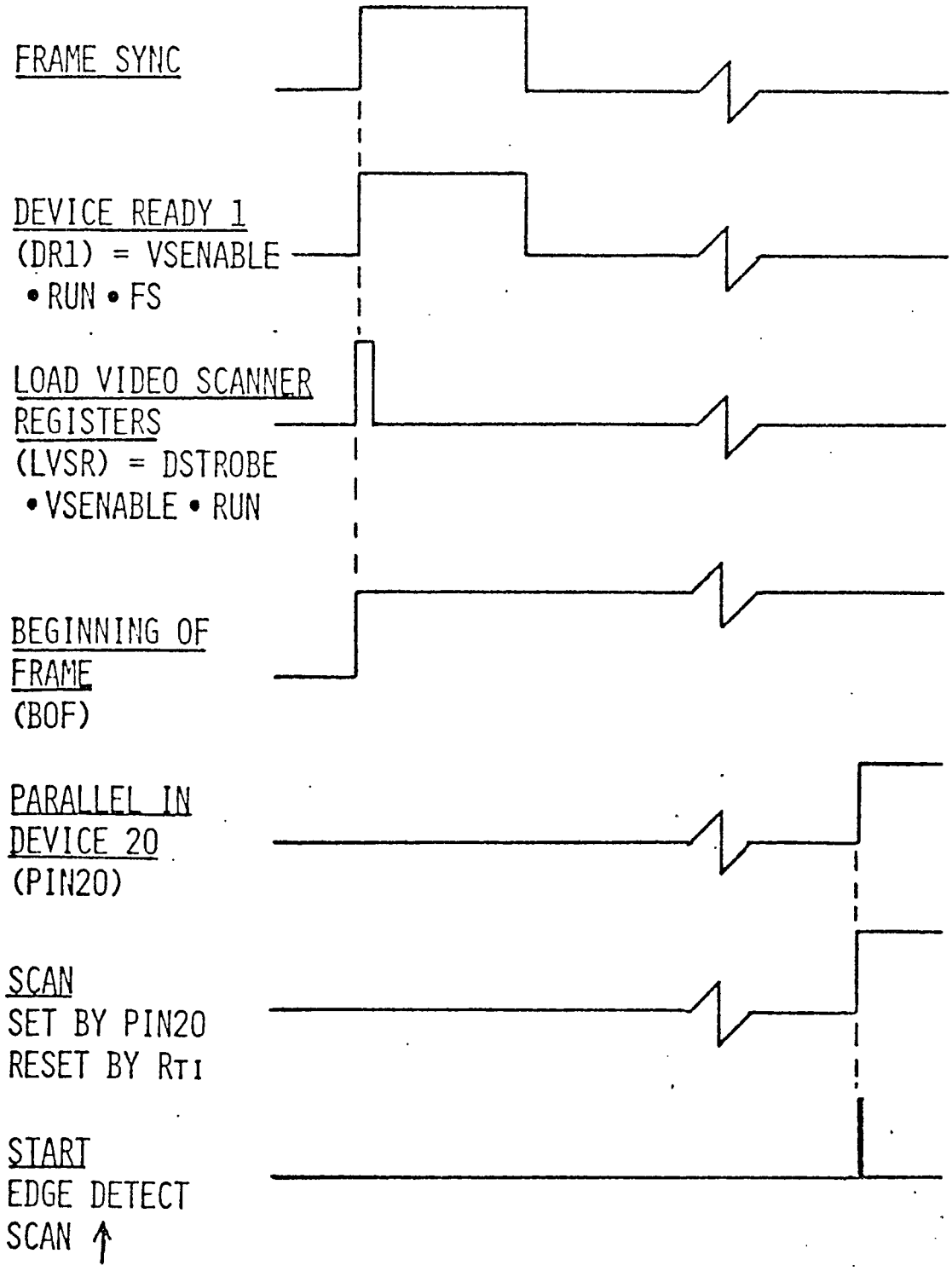

START SCAN LOGIC
S20-
44
7474
Vcc
TERM-
PIN20
PIN20-
7400
7404
7474
Vcc
SCAN
23
512pF
330
1N459
START
24
RESET
7402
TERM-
BOF
21
Rr1
END OF SCAN CALCULATION TRIGGER
7486
7404
7440
ADD → HA
22
Vcc

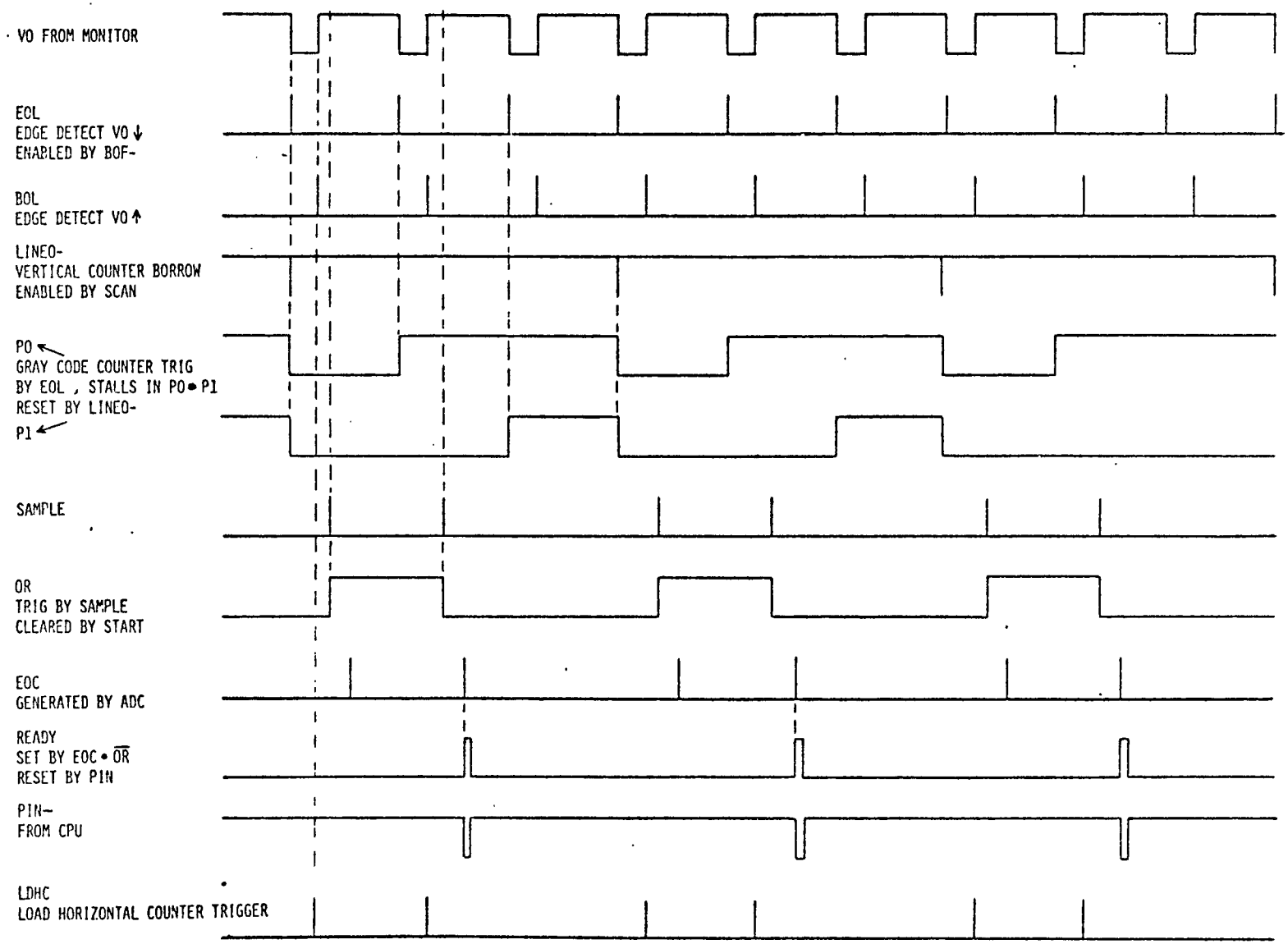
SLOT 9


Vcc
750
750
0.1
LM555
Vcc
RESET
DISC
OUTPUT
THRESHOLD
TRIG
GND
SQUARE WAVE GENERATOR
7474
510pF
7400
MODSTRT+
0.01mF.
100K
330
1N459
0.1mF.
10K
741
INTEGRATOR
NOTE: DIP 741 WITH +15Vdc AT 11 AND -15Vdc AT 6.
NOTE: ADDITIONAL FUNCTIONS SUPPORTED BY PULSE WIDTH MODULATOR SHOWN WITH DASHED LINES.
DAC0(XAXIS)
DAC1(YAXIS)
BEAMENA+ (ZAXIS)
ERASE-
PROG GND
VIEW-
DAC2
MODSTRT+
+15Vdc
NONSTORE-
ERASE INT
WRITE THRU-
-15Vdc
PULSE WIDTH MODULATOR INPUT
TEKTRONIX 611 PLUG
DAC2
500 CONTRAST
AMPLIFIER/SHIFTER
MODULATOR
1.5K
ZAXIS MODULATED
1K
1N459
BEAMENA+
1N750
Vz=4.7
1N750
1.8K
100K
500 INTENSITY
PULSE WIDTH MODULATOR
WIDTH
HEIGHT
DAC0
DAC1
500
XAXIS
YAXIS

APPENDIX C
TIMING DIAGRAMS

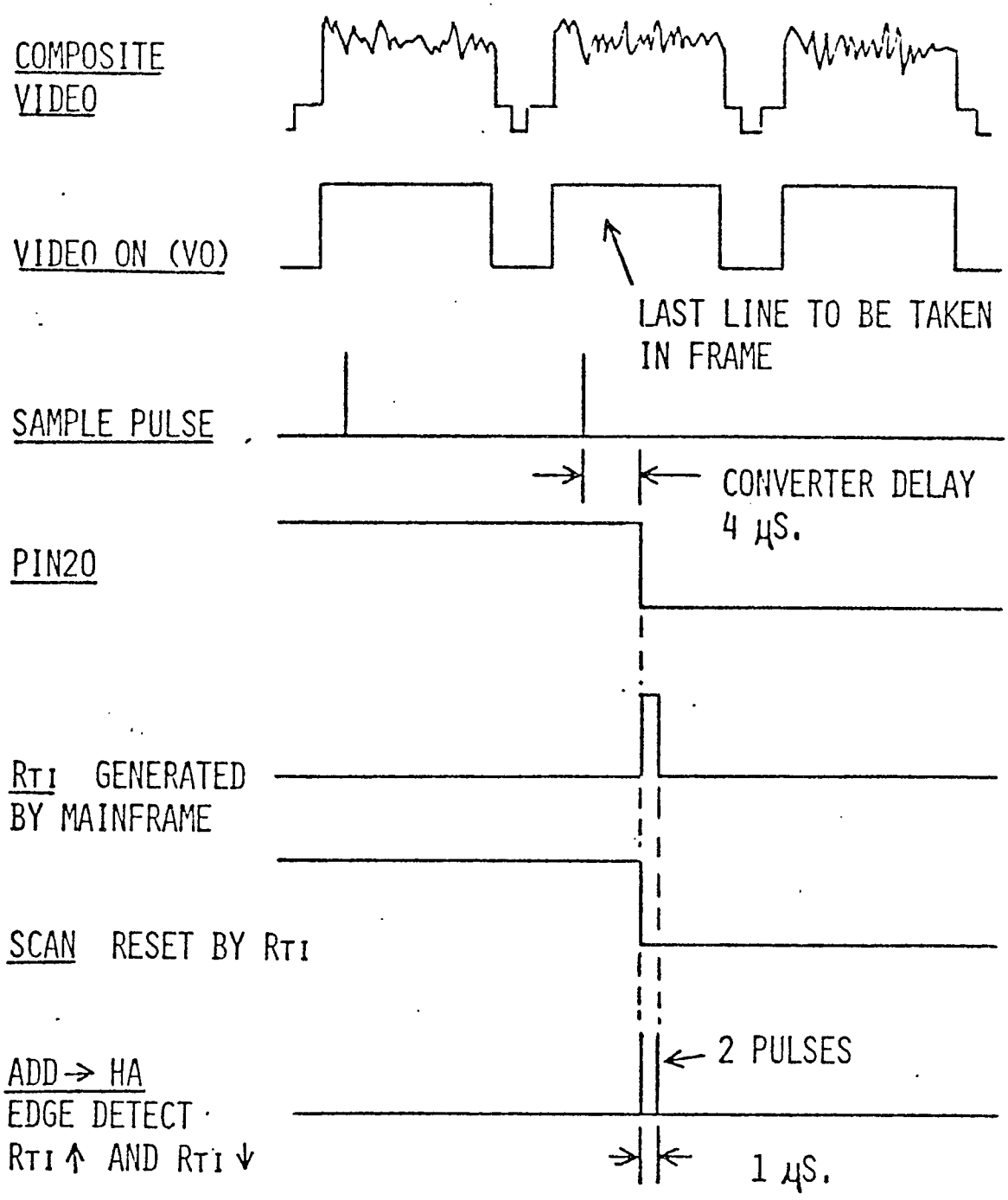
LOAD / START SEQUENCE TIMING





RUN SEQUENCE EXAMPLE

END SEQUENCE TIMING



APPENDIX D
FLOWCHARTS

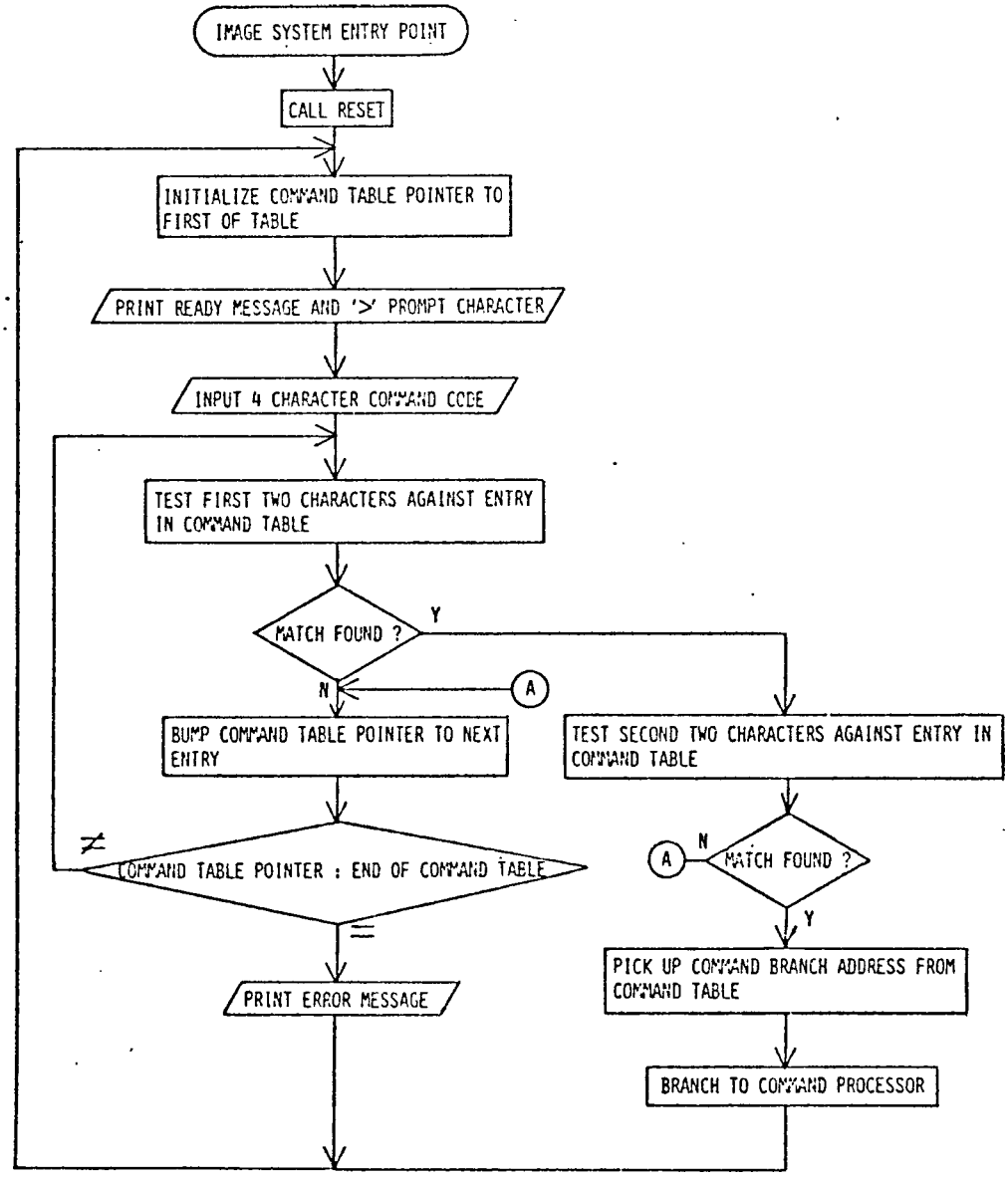
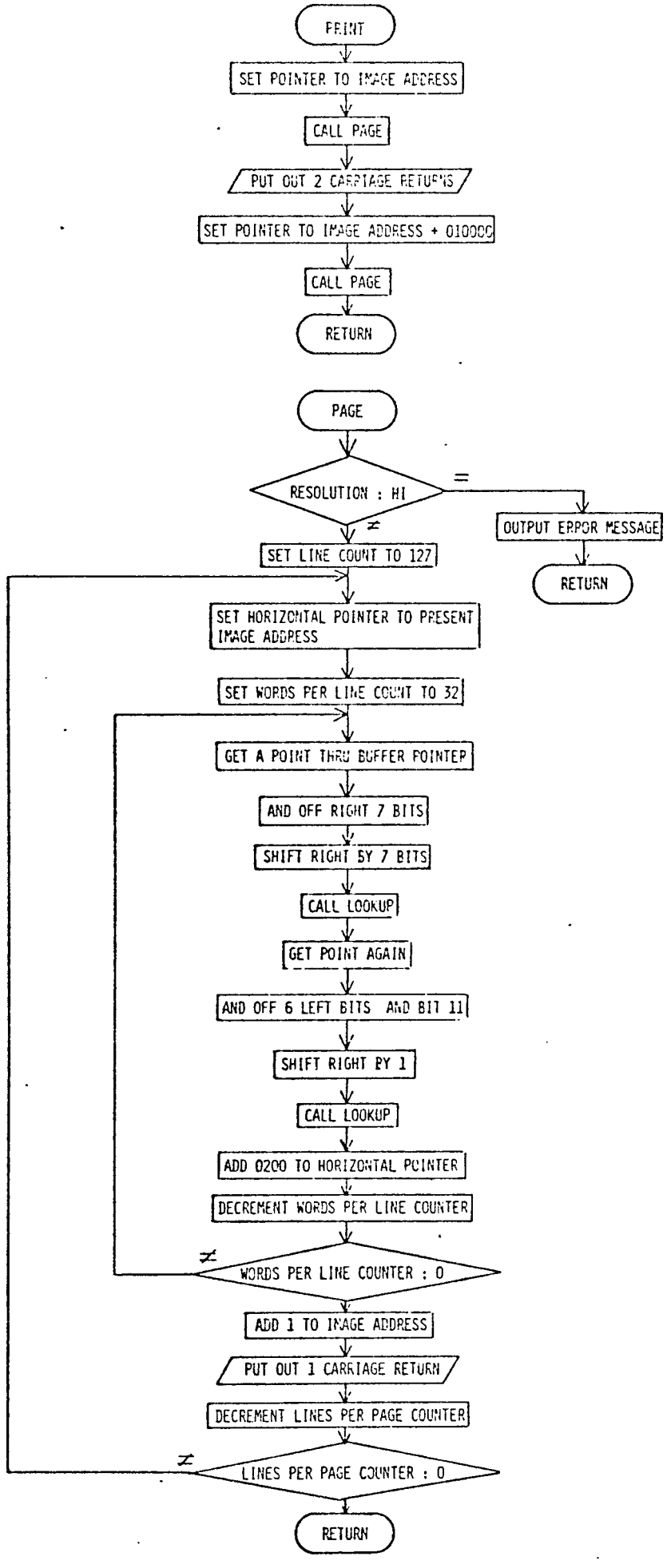
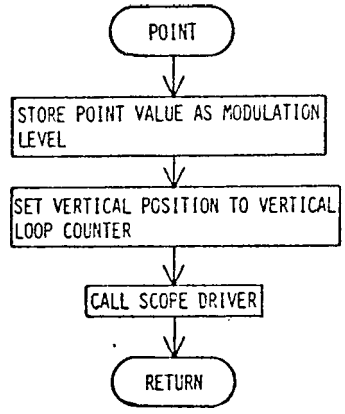
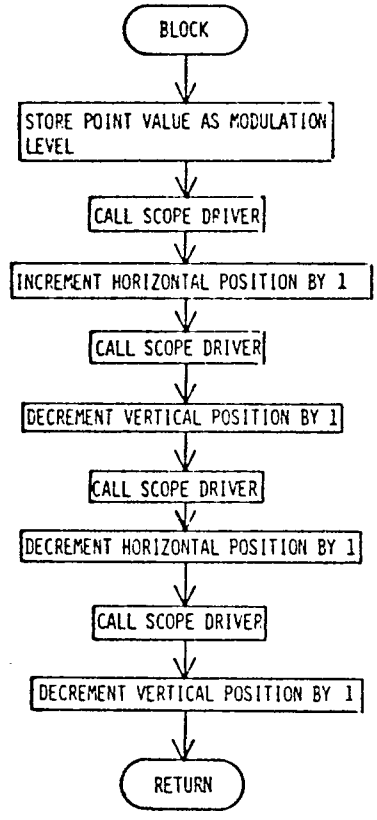
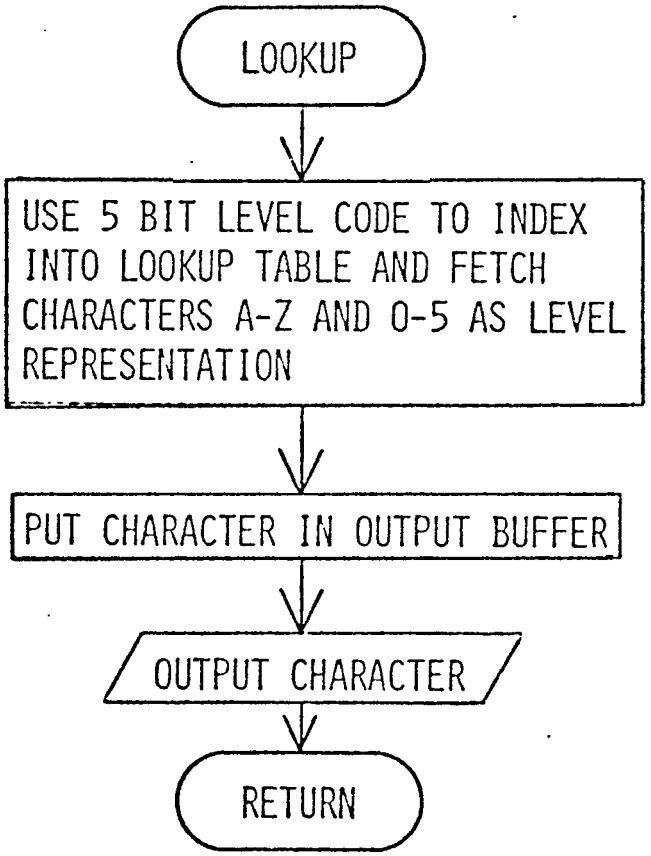


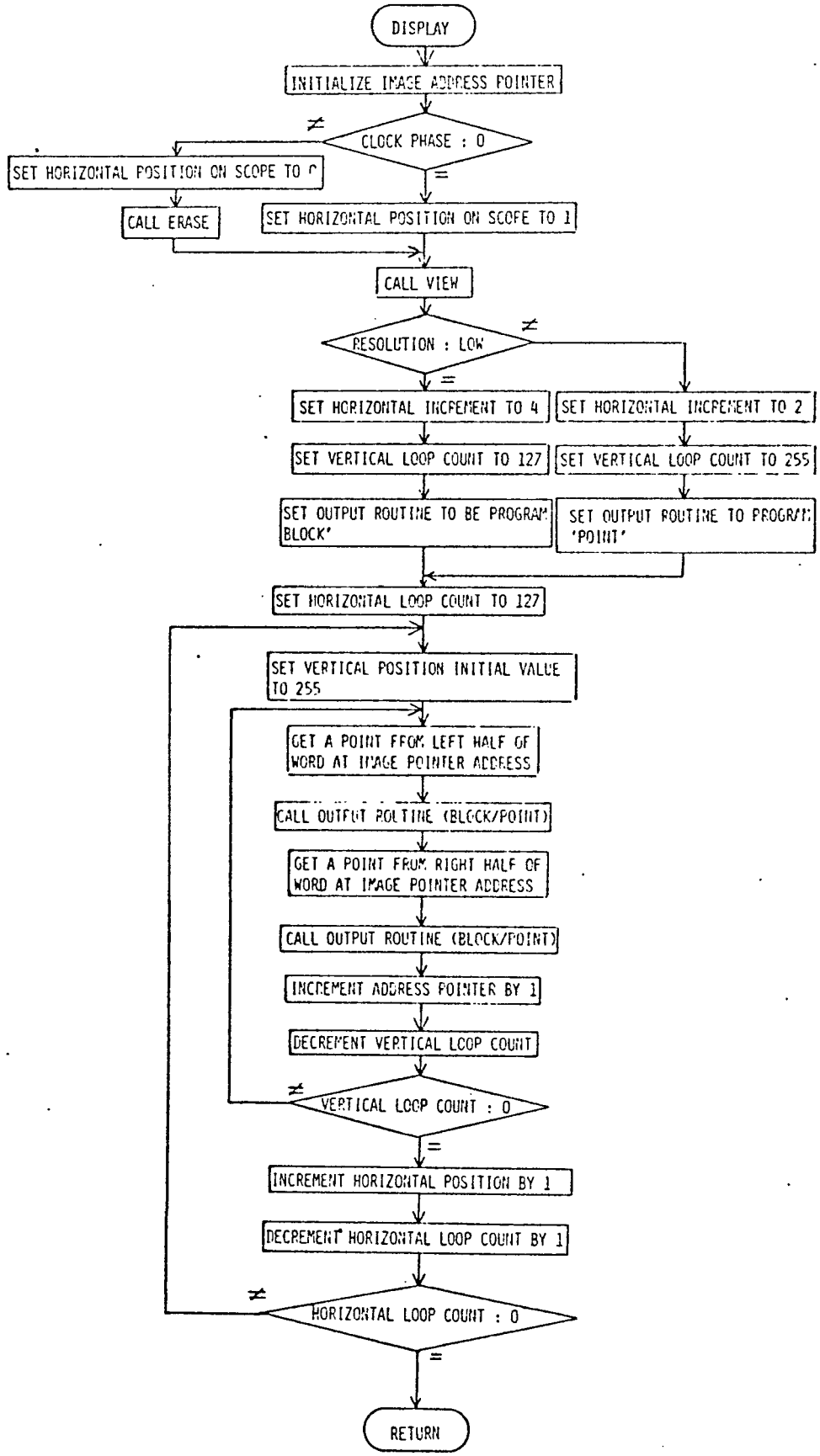
IMAGE SYSTEM ENTRY POINT
CALL RESET
INITIALIZE COMMAND TABLE POINTER TO FIRST OF TABLE
PRINT READY MESSAGE AND '>' PROMPT CHARACTER
INPUT 4 CHARACTER COMMAND CODE
TEST FIRST TWO CHARACTERS AGAINST ENTRY IN COMMAND TABLE
MATCH FOUND ?
Y
N
A
BUMP COMMAND TABLE POINTER TO NEXT ENTRY
TEST SECOND TWO CHARACTERS AGAINST ENTRY IN COMMAND TABLE
≠
COMMAND TABLE POINTER : END OF COMMAND TABLE
=
A
N
MATCH FOUND ?
Y
PRINT ERROR MESSAGE
PICK UP COMMAND BRANCH ADDRESS FROM COMMAND TABLE
BRANCH TO COMMAND PROCESSOR

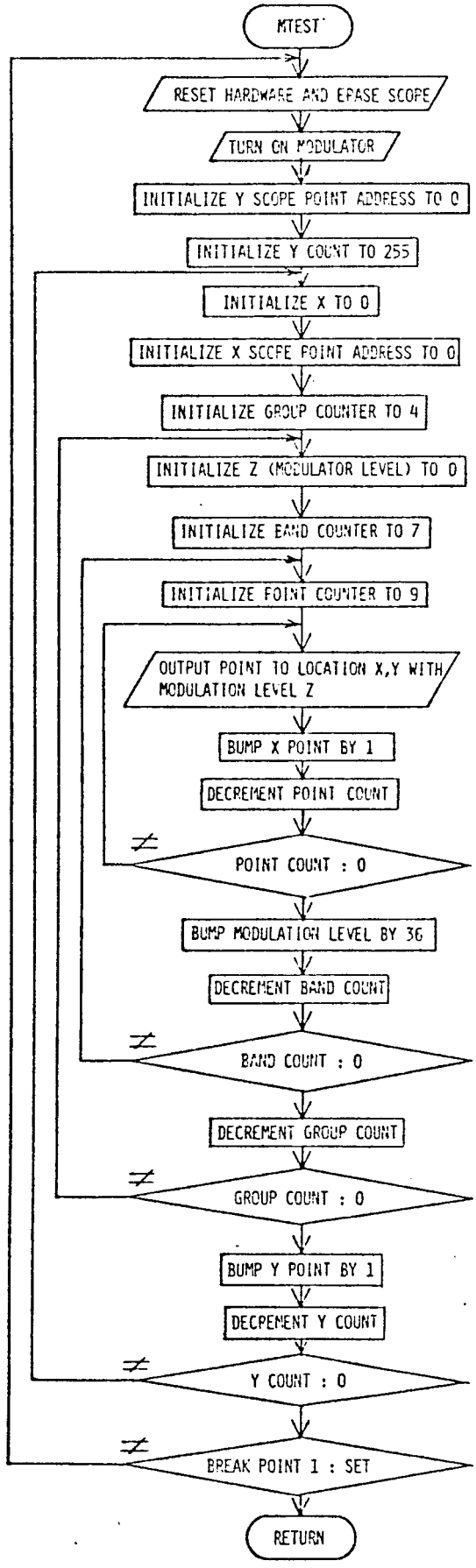

PRINT
SET POINTER TO IMAGE ADDRESS
CALL PAGE
PUT OUT 2 CARRIAGE RETURNS
SET POINTER TO IMAGE ADDRESS + 010000
CALL PAGE
RETURN
PAGE
RESOLUTION : HI
=
≠
OUTPUT ERROR MESSAGE
RETURN
SET LINE COUNT TO 127
SET HORIZONTAL POINTER TO PRESENT IMAGE ADDRESS
SET WORDS PER LINE COUNT TO 32
GET A POINT THRU BUFFER POINTER
AND OFF RIGHT 7 BITS
SHIFT RIGHT BY 7 BITS
CALL LOOKUP
GET POINT AGAIN
AND OFF 6 LEFT BITS AND BIT 11
SHIFT RIGHT BY 1
CALL LOOKUP
ADD 0200 TO HORIZONTAL POINTER
DECREMENT WORDS PER LINE COUNTER
≠
WORDS PER LINE COUNTER : 0
ADD 1 TO IMAGE ADDRESS
PUT OUT 1 CARRIAGE RETURN
DECREMENT LINES PER PAGE COUNTER
≠
LINES PER PAGE COUNTER : 0
RETURN

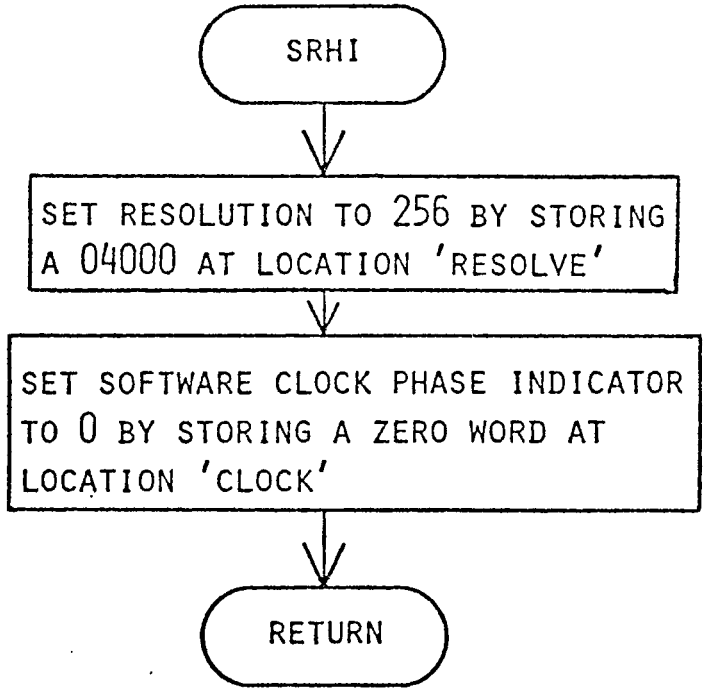

POINT
STORE POINT VALUE AS MODULATION LEVEL
SET VERTICAL POSITION TO VERTICAL LOOP COUNTER
CALL SCOPE DRIVER
RETURN

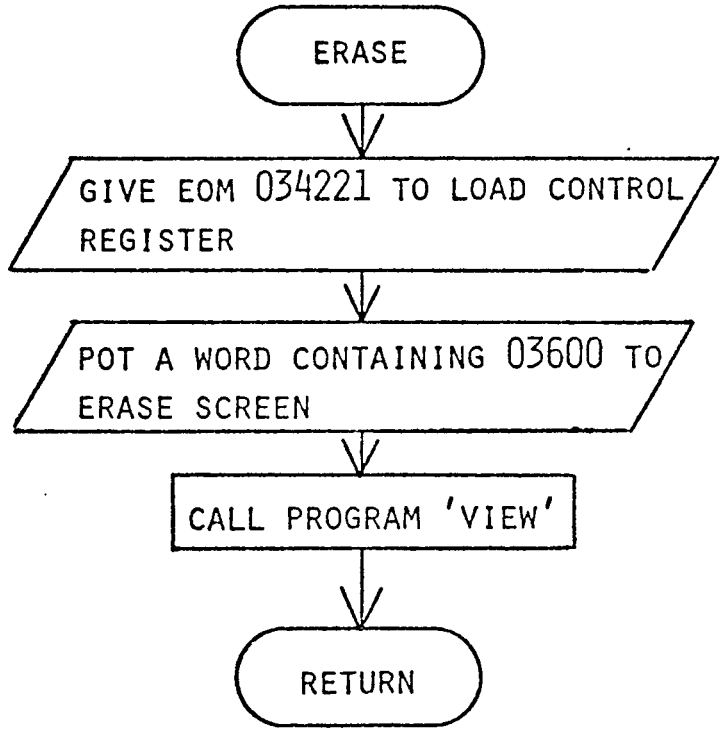

BLOCK
STORE POINT VALUE AS MODULATION LEVEL
CALL SCOPE DRIVER
INCREMENT HORIZONTAL POSITION BY 1
CALL SCOPE DRIVER
DECREMENT VERTICAL POSITION BY 1
CALL SCOPE DRIVER
DECREMENT HORIZONTAL POSITION BY 1
CALL SCOPE DRIVER
DECREMENT VERTICAL POSITION BY 1
RETURN

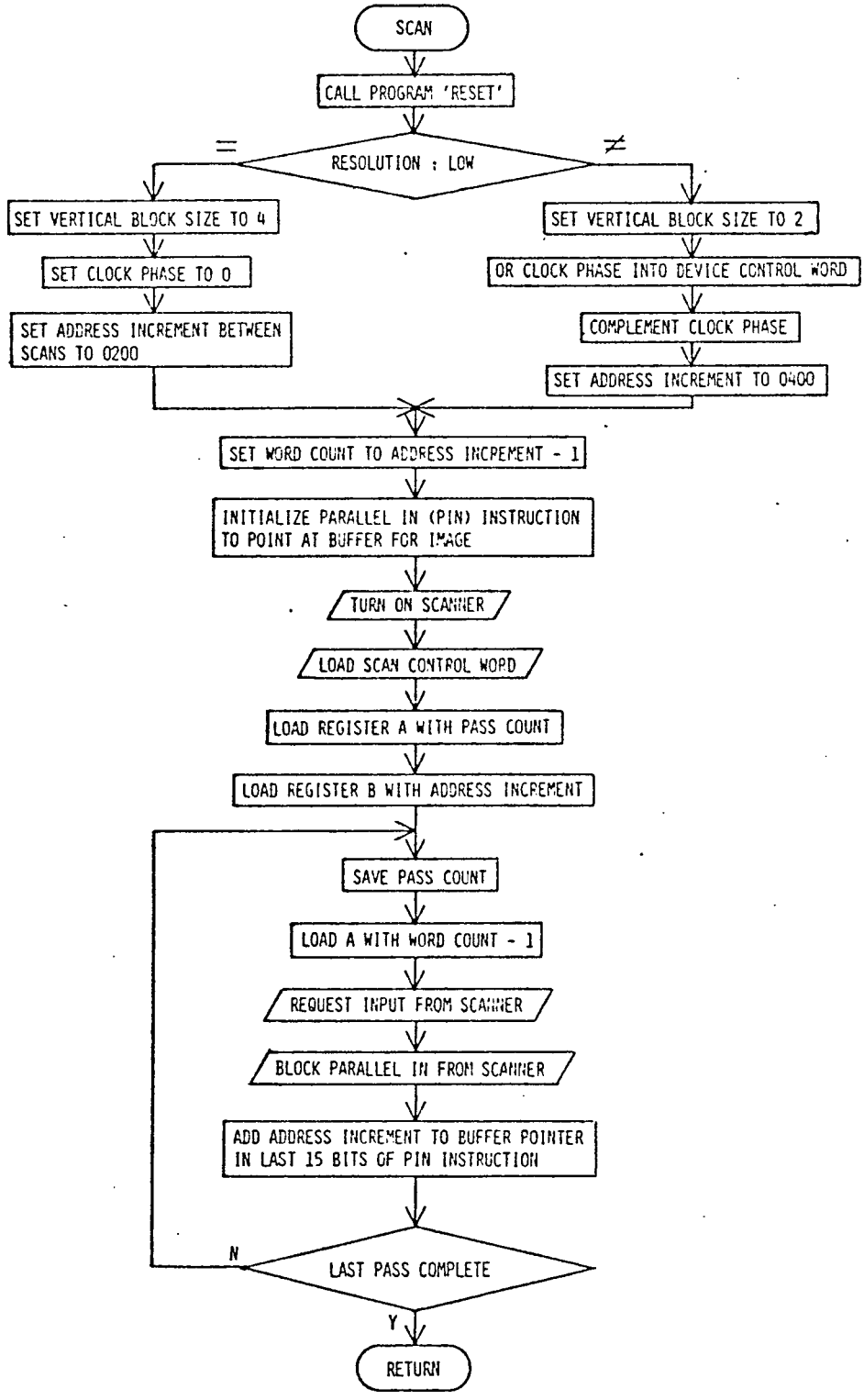

LOOKUP
USE 5 BIT LEVEL CODE TO INDEX INTO LOOKUP TABLE AND FETCH CHARACTERS A-Z AND 0-5 AS LEVEL REPRESENTATION
PUT CHARACTER IN OUTPUT BUFFER
OUTPUT CHARACTER
RETURN

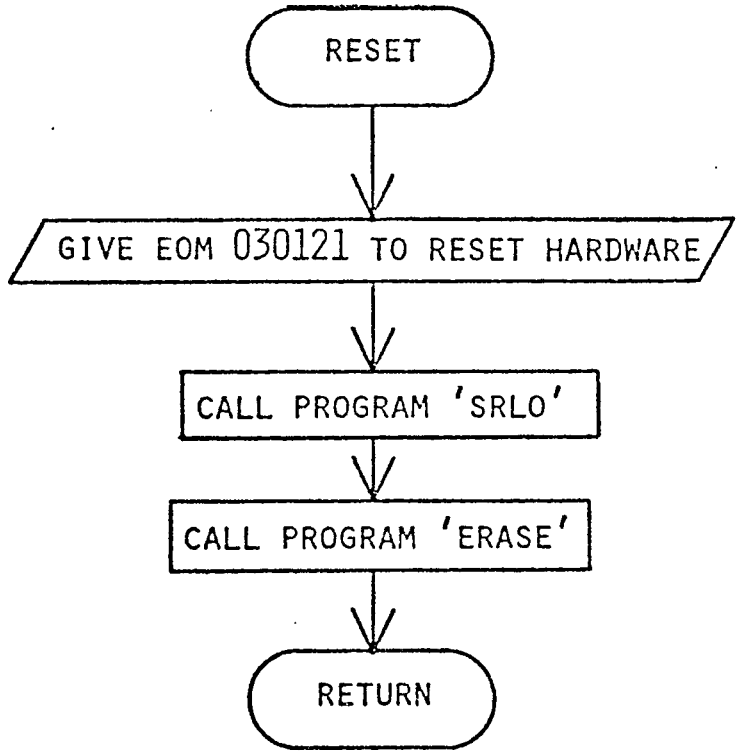

DISPLAY
INITIALIZE IMAGE ADDRESS POINTER
CLOCK PHASE : 0
≠
=
SET HORIZONTAL POSITION ON SCOPE TO 0
CALL ERASE
SET HORIZONTAL POSITION ON SCOPE TO 1
CALL VIEW
RESOLUTION : LOW
≠
=
SET HORIZONTAL INCREMENT TO 4
SET HORIZONTAL INCREMENT TO 2
SET VERTICAL LOOP COUNT TO 127
SET VERTICAL LOOP COUNT TO 255
SET OUTPUT ROUTINE TO BE PROGRAM 'BLOCK'
SET OUTPUT ROUTINE TO PROGRAM 'POINT'
SET HORIZONTAL LOOP COUNT TO 127
SET VERTICAL POSITION INITIAL VALUE TO 255
GET A POINT FROM LEFT HALF OF WORD AT IMAGE POINTER ADDRESS
CALL OUTPUT ROUTINE (BLOCK/POINT)
GET A POINT FROM RIGHT HALF OF WORD AT IMAGE POINTER ADDRESS
CALL OUTPUT ROUTINE (BLOCK/POINT)
INCREMENT ADDRESS POINTER BY 1
DECREMENT VERTICAL LOOP COUNT
VERTICAL LOOP COUNT : 0
≠
=
INCREMENT HORIZONTAL POSITION BY 1
DECREMENT HORIZONTAL LOOP COUNT BY 1
HORIZONTAL LOOP COUNT : 0
≠
=
RETURN

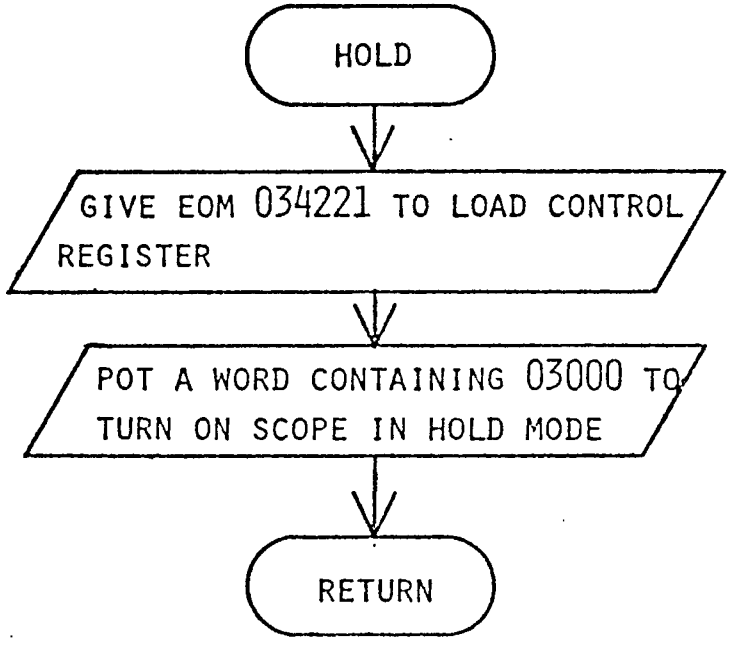

MTEST
RESET HARDWARE AND ERASE SCOPE
TURN ON MODULATOR
INITIALIZE Y SCOPE POINT ADDRESS TO 0
INITIALIZE Y COUNT TO 255
INITIALIZE X TO 0
INITIALIZE X SCOPE POINT ADDRESS TO 0
INITIALIZE GROUP COUNTER TO 4
INITIALIZE Z (MODULATOR LEVEL) TO 0
INITIALIZE BAND COUNTER TO 7
INITIALIZE POINT COUNTER TO 9
OUTPUT POINT TO LOCATION X,Y WITH MODULATION LEVEL Z
BUMP X POINT BY 1
DECREMENT POINT COUNT
≠
POINT COUNT : 0
BUMP MODULATION LEVEL BY 36
DECREMENT BAND COUNT
≠
BAND COUNT : 0
DECREMENT GROUP COUNT
≠
GROUP COUNT : 0
BUMP Y POINT BY 1
DECREMENT Y COUNT
≠
Y COUNT : 0
≠
BREAK POINT 1 : SET
RETURN

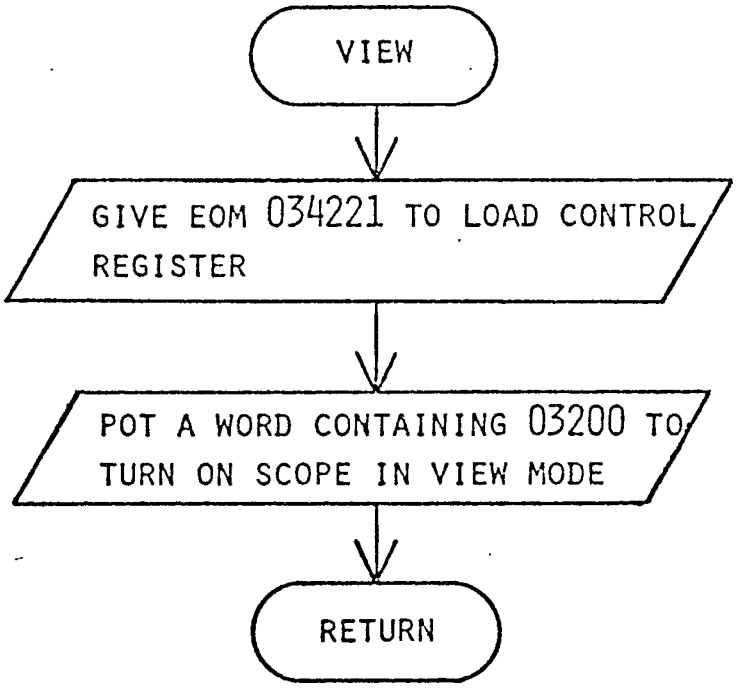

SRHI
SET RESOLUTION TO 256 BY STORING A 04000 AT LOCATION 'RESOLVE'
SET SOFTWARE CLOCK PHASE INDICATOR TO 0 BY STORING A ZERO WORD AT LOCATION 'CLOCK'
RETURN

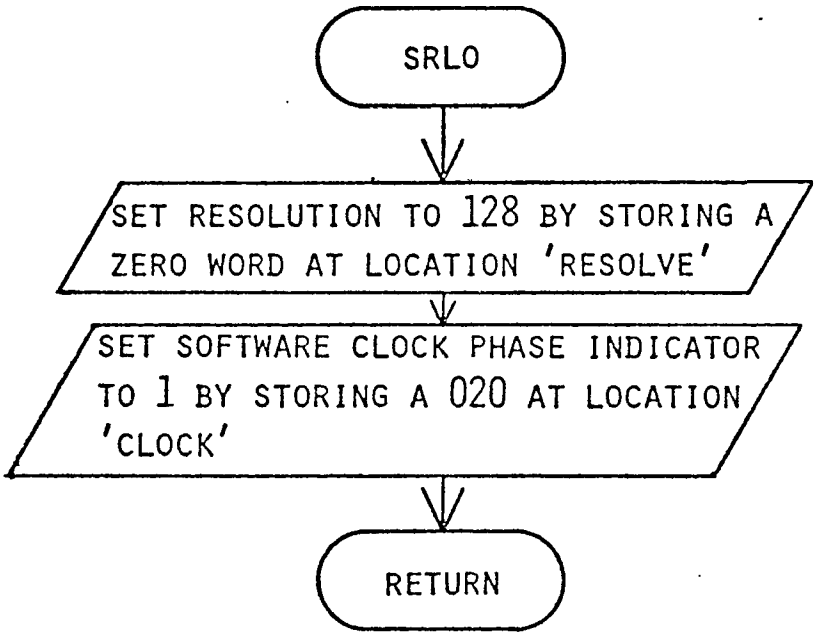

ERASE
GIVE EOM 034221 TO LOAD CONTROL REGISTER
POT A WORD CONTAINING 03600 TO ERASE SCREEN
CALL PROGRAM 'VIEW'
RETURN

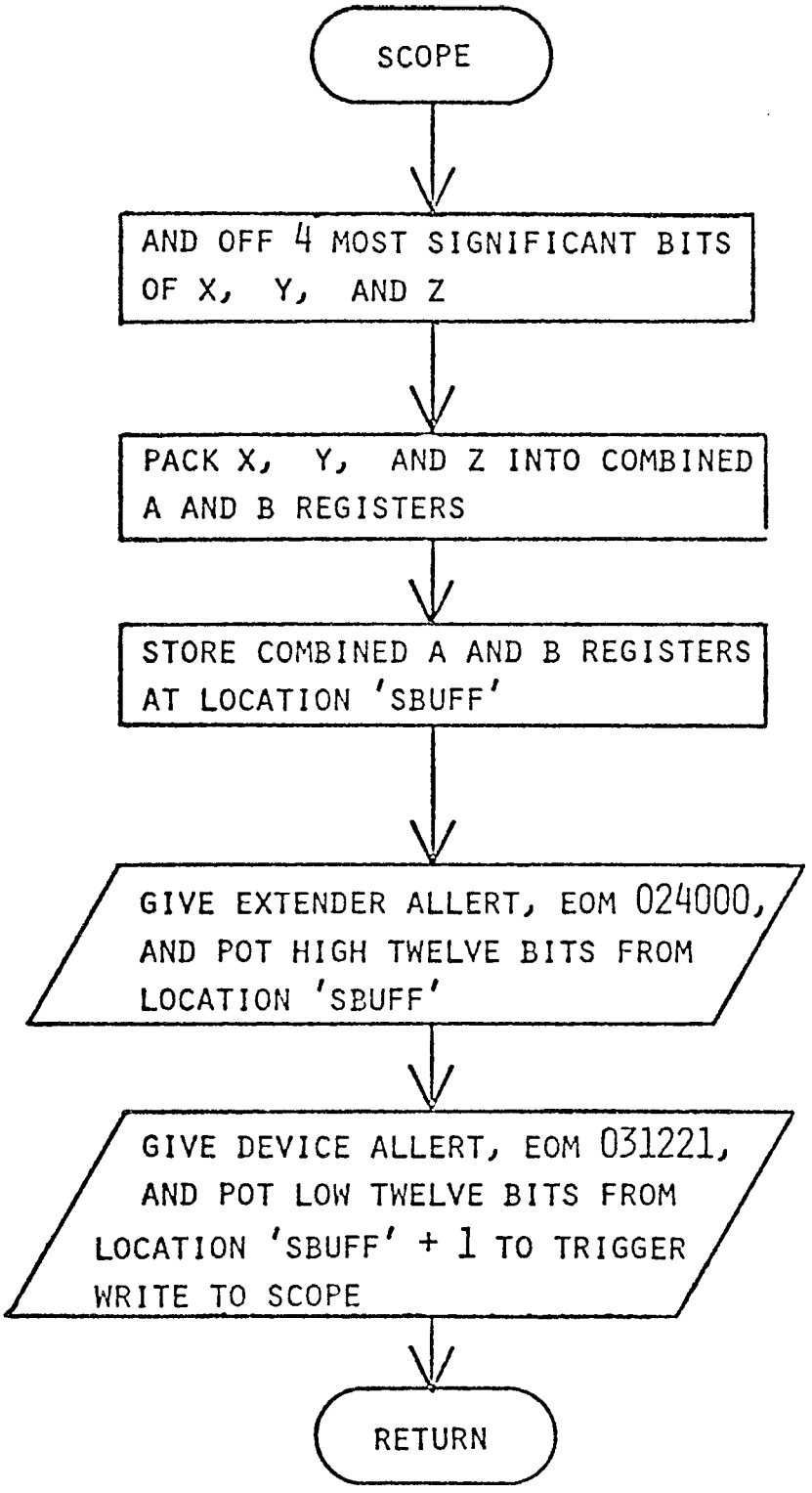

SCAN
CALL PROGRAM 'RESET'
RESOLUTION : LOW
=
≠
SET VERTICAL BLOCK SIZE TO 4
SET CLOCK PHASE TO 0
SET ADDRESS INCREMENT BETWEEN SCANS TO 0200
SET VERTICAL BLOCK SIZE TO 2
OR CLOCK PHASE INTO DEVICE CONTROL WORD
COMPLEMENT CLOCK PHASE
SET ADDRESS INCREMENT TO 0400
SET WORD COUNT TO ADDRESS INCREMENT - 1
INITIALIZE PARALLEL IN (PIN) INSTRUCTION TO POINT AT BUFFER FOR IMAGE
TURN ON SCANNER
LOAD SCAN CONTROL WORD
LOAD REGISTER A WITH PASS COUNT
LOAD REGISTER B WITH ADDRESS INCREMENT
SAVE PASS COUNT
LOAD A WITH WORD COUNT - 1
REQUEST INPUT FROM SCANNER
BLOCK PARALLEL IN FROM SCANNER
ADD ADDRESS INCREMENT TO BUFFER POINTER IN LAST 15 BITS OF PIN INSTRUCTION
N
LAST PASS COMPLETE
Y
RETURN

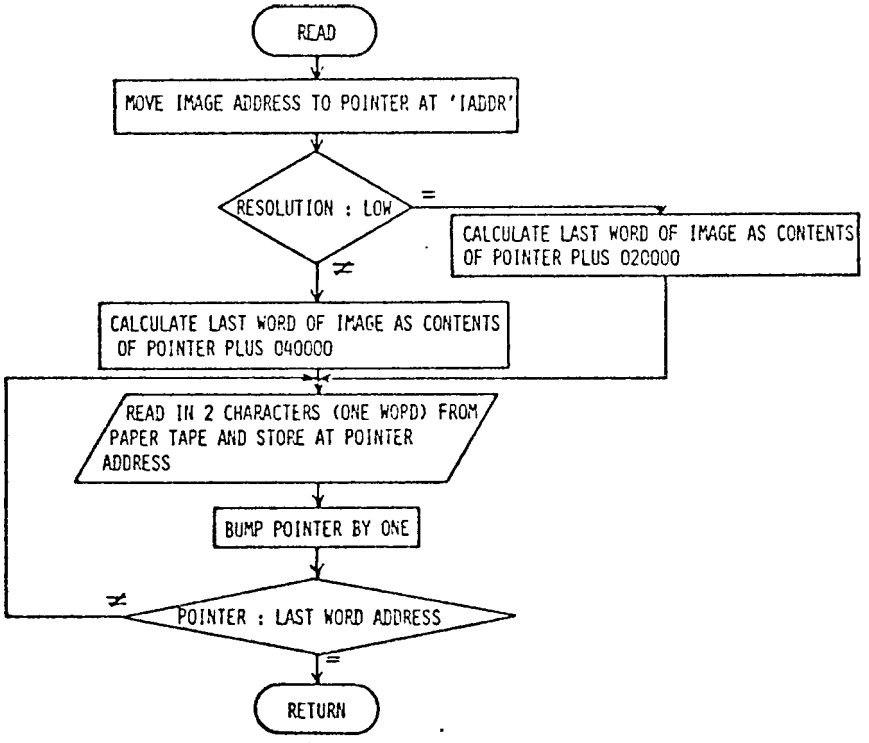

RESET
GIVE EOM 030121 TO RESET HARDWARE
CALL PROGRAM 'SRLO'
CALL PROGRAM 'ERASE'
RETURN

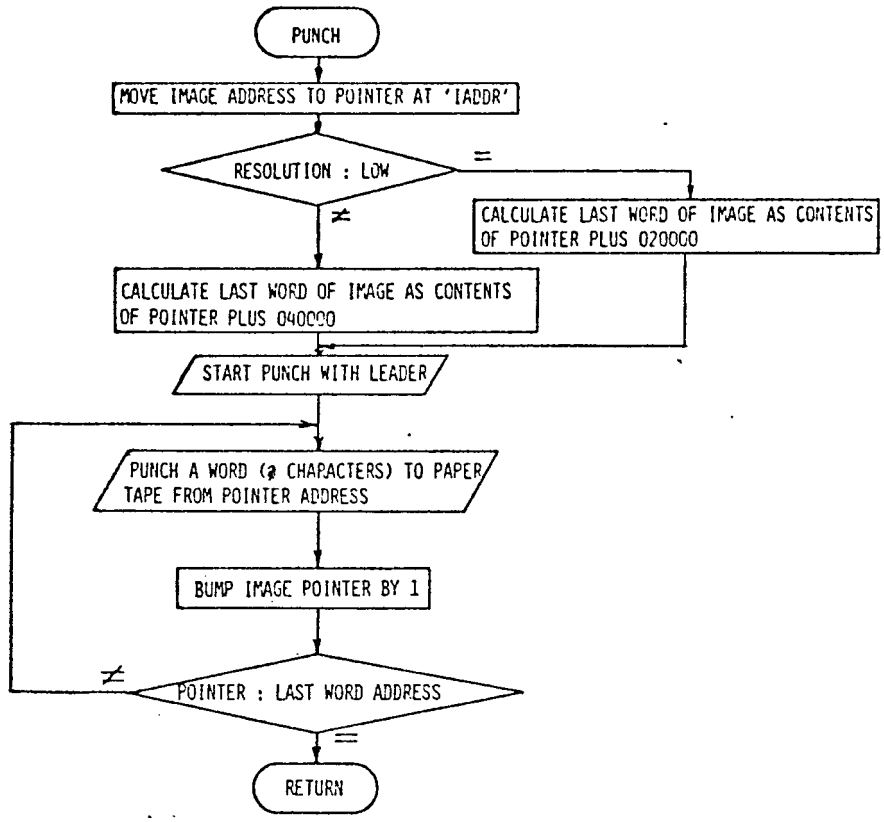

HOLD
GIVE EOM 034221 TO LOAD CONTROL REGISTER
POT A WORD CONTAINING 03000 TO TURN ON SCOPE IN HOLD MODE
RETURN


VIEW
GIVE EOM 034221 TO LOAD CONTROL REGISTER
POT A WORD CONTAINING 03200 TO TURN ON SCOPE IN VIEW MODE
RETURN


SRLO
SET RESOLUTION TO 128 BY STORING A ZERO WORD AT LOCATION 'RESOLVE'
SET SOFTWARE CLOCK PHASE INDICATOR TO 1 BY STORING A 020 AT LOCATION 'CLOCK'
RETURN


SCOPE
AND OFF 4 MOST SIGNIFICANT BITS OF X, Y, AND Z
PACK X, Y, AND Z INTO COMBINED A AND B REGISTERS
STORE COMBINED A AND B REGISTERS AT LOCATION 'SBUFF'
GIVE EXTENDER ALLERT, EOM 024000, AND POT HIGH TWELVE BITS FROM LOCATION 'SBUFF'
GIVE DEVICE ALLERT, EOM 031221, AND POT LOW TWELVE BITS FROM LOCATION 'SBUFF' + 1 TO TRIGGER WRITE TO SCOPE
RETURN


READ
MOVE IMAGE ADDRESS TO POINTER AT 'IADDR'
RESOLUTION : LOW
=
≠
CALCULATE LAST WORD OF IMAGE AS CONTENTS OF POINTER PLUS 020000
CALCULATE LAST WORD OF IMAGE AS CONTENTS OF POINTER PLUS 040000
READ IN 2 CHARACTERS (ONE WOPD) FROM PAPER TAPE AND STORE AT POINTER ADDRESS
BUMP POINTER BY ONE
≠
POINTER : LAST WORD ADDRESS
=
RETURN


PUNCH
MOVE IMAGE ADDRESS TO POINTER AT 'IADDR'
RESOLUTION : LOW
=
≠
CALCULATE LAST WORD OF IMAGE AS CONTENTS OF POINTER PLUS 020000
CALCULATE LAST WORD OF IMAGE AS CONTENTS OF POINTER PLUS 040000
START PUNCH WITH LEADER
PUNCH A WORD (2 CHARACTERS) TO PAPER TAPE FROM POINTER ADDRESS
BUMP IMAGE POINTER BY 1
≠
POINTER : LAST WORD ADDRESS
=
RETURN